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Cobalt Silicide Interconnection from a Si/W/Co Trilayer Structure

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ABSTRACT

A Si/W/Co trilayer structure which consists of a top insulating Si film, a middle buffering W film, and a bottom Co film is proposed to form cobalt silicide. Because the top Si layer can hinder the oxidants and contaminants from penetrating into the bottom layers, the silicidation process is insensitive to the annealing atmosphere. The middle W film can prevent the top Si layer from reacting with the bottom Co film to form an unwanted cobalt silicide film. It can also react with the bottom Co film to form a Co-W alloy. Thus, the unsilicided Co film can be completely transformed into the Co-W alloy which can be etched out with the same chemical etchant as that for the W film. By using the Si/W/Co (100 nm/50 nm/40 nm) trilayer structure on single-crystal Si substrates and silicidation at 700°-800°C for 30 min in flowing N_2, the obtainable sheet resistance is 1.7-2.0 Ω/□. This corresponds to a film resistivity of 20 μΩ · cm. Since Co is the dominant diffusion species in forming $CoSi_2$, and the Co-W alloy formed upon the oxide layer has a higher silicidation temperature than the pure Co film, cobalt silicide cannot grow laterally on top of the oxide layer.

With the advent of the VLSI era, new materials must be used to reduce the interconnection resistance and the contact resistance which turns out to be the dominant factor in determining circuit delay when devices are scaled down to the submicrometer range. Refractory metal silicides have been extensively studied as materials for interconnections and contacts, because they have lower resistivity than poly-Si, can withstand higher processing temperatures than Al, and are compatible with the conventional processing technology.

In a so-called salicide (self-aligned silicide) process, which forms silicide on top of both gate and source/drain regions simultaneously, titanium silicide (1-3) has been widely studied because of its lowest resistivity among all refractory metal silicides. On the other hand, cobalt silicide has drawn less attention in the past, since the resistivity of cobalt silicide (18-20 μΩ · cm) is a little higher than that of titanium silicide (13-15 μΩ · cm). But recently, many investigations (4-7) have focused on it because it presents few lateral-growth problems in forming salicide. This is because the dominant diffusion species in forming $CoSi_2$ is Co (8). However, cobalt is sensitive to residual oxygen in the annealing atmosphere. Therefore, if the environment-sensitive problem can be overcome, cobalt silicide is just as promising as titanium silicide in VLSI applications.

When a conventional furnace anneal is adopted (7), a specially designed furnace and a strict control of the residual oxygen in the annealing atmosphere are essential in forming a good-quality cobalt silicide film. In addition, a two-step annealing process is required since it has been pointed out (9) that a single annealing at 900°C for 30 min can cause cobalt silicide to grow laterally on top of the oxide layer. This possibility of lateral growth of $CoSi_2$ originates from the fact that the formation of the $CoSi_2$ is preceded by that of the CoSi which grows via Si atom motion (10).

Recently, RTA (rapid thermal anneal) has been favorably adopted by many investigations (4-6) to prevent the oxidation of the cobalt film, because the low-temperature loading and rapidly increasing annealing temperature can reduce the interaction between oxygen and cobalt. However, two problems are associated with the RTA process, *i.e.*, its small capacity and nonuniform results.

In this paper, the Si/W/Co trilayer structure is employed to cope with the environment-sensitive and possible lateral-growth problems in forming cobalt silicide. With the Si/W/Co trilayer structure, some interesting results are obtained and presented in the following sections.

Experimental

P-type (100) wafers with a resistivity of 2-20 Ω · cm were employed in this study as substrates. Two groups of samples were prepared to form cobalt silicide, both upon single-crystal Si substrates and n^+ poly-Si films. One group was oxidized to form 100 nm of SiO_2. Then 500 nm of poly-Si film was deposited and doped by a $POCl_3$ liquid source to form an n^+ poly-Si film with a sheet resistance of 15-20 Ω/□. Finally, 100 nm of polyoxide were grown and patterned. The other group was oxidized to form 100 nm of SiO_2 and patterned.

Immediately after dipping in a solution of $HF:H_2O$ (1:50) for 20s to remove the native oxide on the exposed Si or

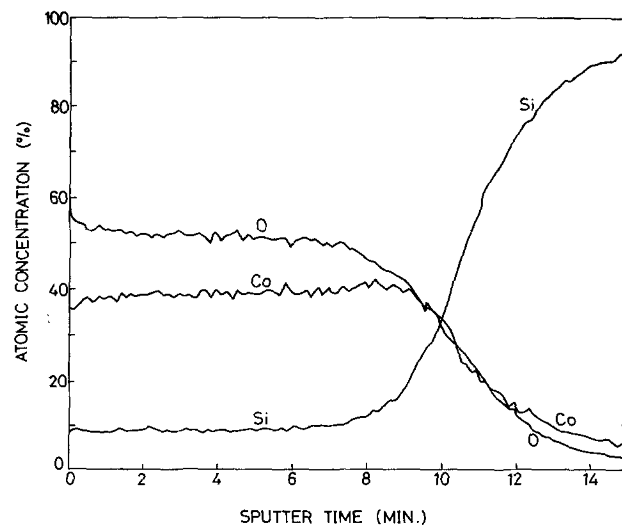

Fig. 1. The AES depth profile of 40 nm Co film on an n^+ poly-Si film after annealing at 700°C for 30 min in N_2.

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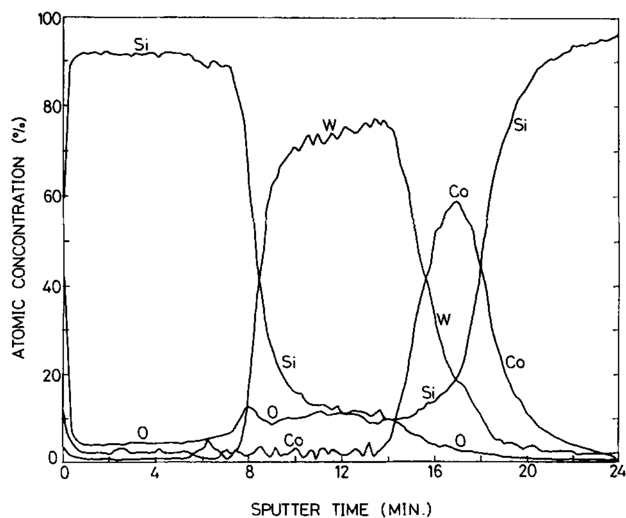
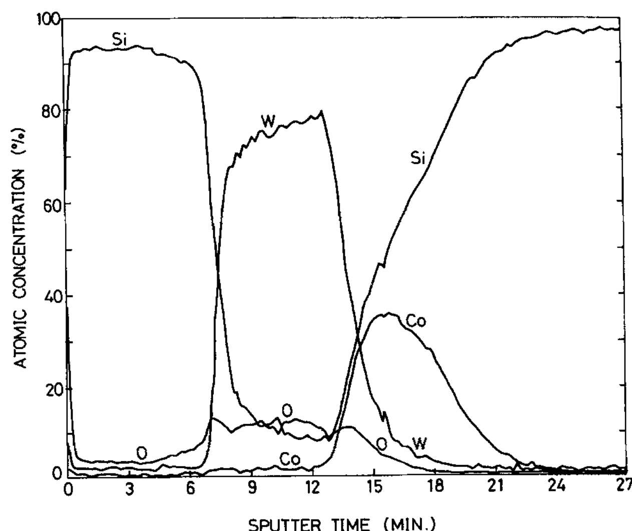




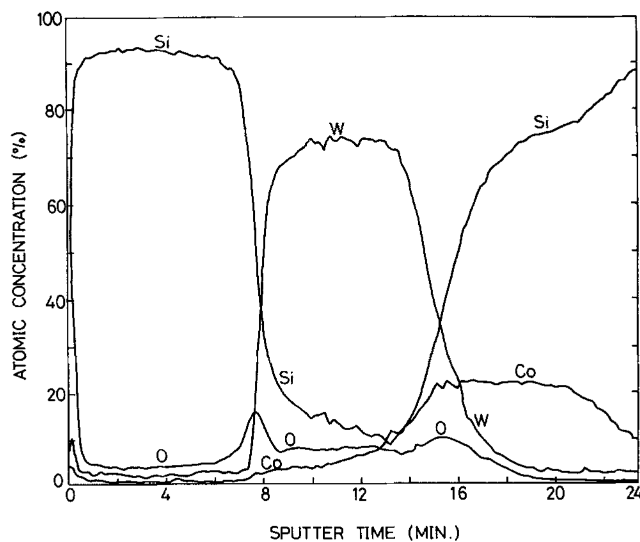
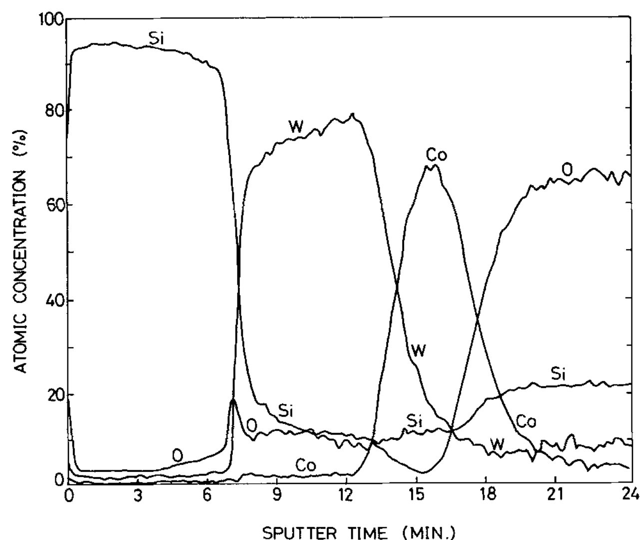


Fig. 2. The AES depth profiles of Si/W/Co (100 nm/50 nm/40 nm) structures on n^+ poly-Si films; (a, top left) as-deposited, (b, top right) after annealing at 400°C for 30 min in N_2, and (c, bottom left) after annealing at 700°C for 30 min in N_2.

poly-Si surface, the samples were put into the vacuum chamber of the dual-E-gun evaporator. After the chamber was pumped down to 5×10^{-6} torr, the Si/W/Co trilayer was deposited in sequence without opening the vacuum chamber. For comparison purposes, samples with a Co film only were also prepared.

After deposition, the samples were annealed at different temperatures in a conventional open-tube furnace with flowing N_2. The purity of N_2 was 99.99%, and the flow rate was set at 5 l/min for a 4 in. quartz tube. The purging N_2 did not receive any special treatment, such as Ti gettering, to remove the residual oxygen. After annealing, some of the samples were etched in a plasma etcher to remove the top protection Si layer. Then they were etched in a solution of H_2O_2:NH_4OH (1:1), at room temperature, to remove the middle W layer and the Co-W alloy formed during annealing. The bottom cobalt silicide layer was then uncovered for observations and measurements. In some cases there



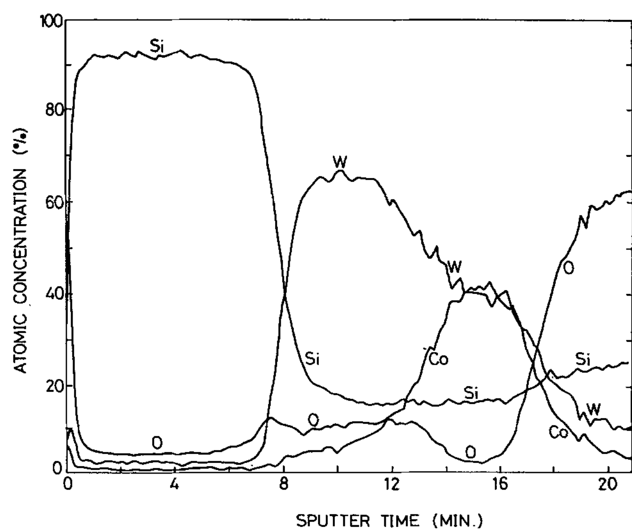


Fig. 3. The AES depth profiles of Si/W/Co (100 nm/50 nm/40 nm) structures on the oxide layer: (a, left) after annealing at 400°C for 30 min in N_2, and (b, right) after annealing at 700°C for 30 min in N_2.

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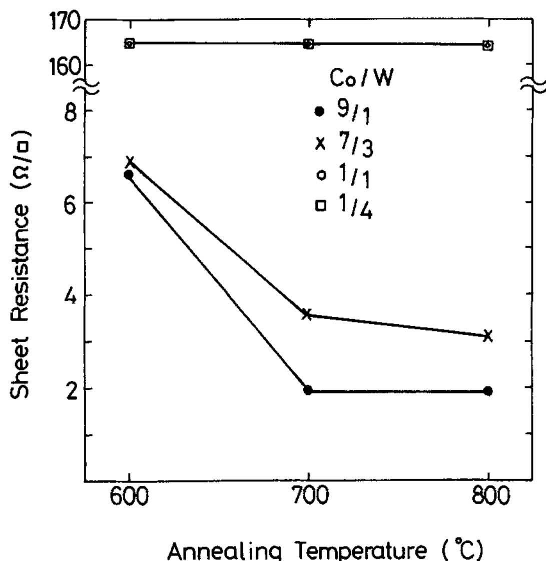

Fig. 4. The resulting sheet resistance *vs.* the annealing temperature for Si/W/Co-W (100 nm/50 nm/Co-W, with respective Co/W ratios of 9:1, 7:3, 1:1, and 1:4) structures on single-crystal Si substrates. The amount of Co deposited was constant corresponding to a thickness of 40 nm, and the ratios of Co/W were achieved by varying the amount of codeposited W.

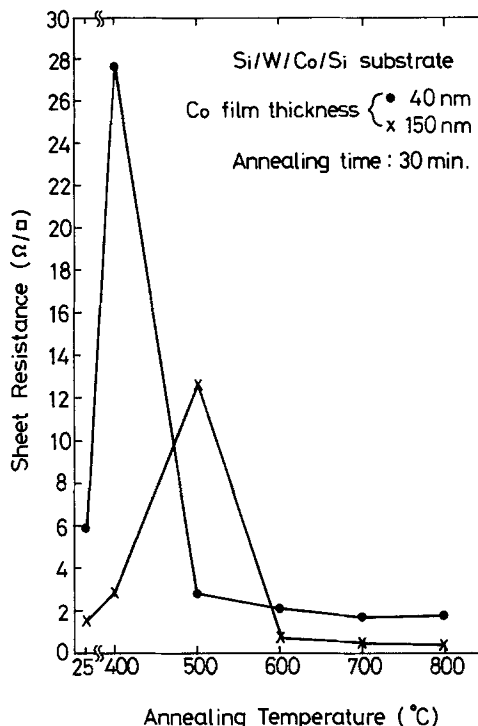

Fig. 5. The resulting sheet resistance as a function of the annealing temperature for Si/W/Co (100:50:40 nm and 100:50:150 nm) structures on single-crystal Si substrates.

remained a residual Co layer upon the oxide layer. This Co layer could be removed in a solution of $HCl:H_2O_2$ (3:1).

The sheet resistance of the cobalt silicide film after silicidation was measured by a four-point probe. The lateral-growth phenomenon after silicidation was observed by scanning electron microscopy (SEM). The depth profiles of the samples after silicidation were analyzed by Auger electron spectroscopy (AES).

Results and Discussion

In order to make a comparison between the Co monolayer and the Si/W/Co trilayer structures, a 40 nm Co film on the n^+ poly-Si film was annealed in a conventional open-tube furnace with N_2 flowing. The AES depth profile of the sample after annealing at 700°C for 30 min is shown in Fig. 1. It can be seen that cobalt has been oxidized completely and no cobalt silicide was formed. Thus, with the conventional furnace annealing process without stringent environmental control, cobalt silicide cannot be formed easily with the Co monolayer structure.

In the Si/W/Co trilayer structure, just as in Ref. (11 and 12), the purpose of the top Si layer is to prevent the oxidants and contaminants from reacting with the bottom Co layer. The middle W layer serves two purposes. First, it inhibits the top Si layer from reacting with the bottom Co layer to form unwanted cobalt silicide. Second, it forms the Co-W alloy which can suppress cobalt silicide from growing laterally on top of the oxide layer. If the unsilicided Co film is completely alloyed with the W film, both the Co-W alloy and the W film can be etched out with one solution instead of two.

Following heat-treatment at different temperatures for 30 min, the AES depth profiles of Si/W/Co trilayer structures on n^+ poly-Si films are given in Fig. 2a-2c. These depth profiles reveal that the top Si layer can effectively prevent the oxidation of the Co film, and just as in Ref. (11), the middle W layer does not react with the top Si layer since the annealing temperature is not high enough to form tungsten silicide. One interesting observation is that the oxygen contaminants incorporated during deposition are expelled from the cobalt silicide film and piled up at the $W/CoSi_x$ interface. Thus, a good-quality $CoSi_2$ film can be obtained by using a Si/W/Co trilayer structure if the annealing temperature is higher than 700°C.

The AES depth profiles of Si/W/Co trilayer structures upon the oxide layer after different heat-treatments are shown in Fig. 3a-3b. It can be seen that Co does not inter-

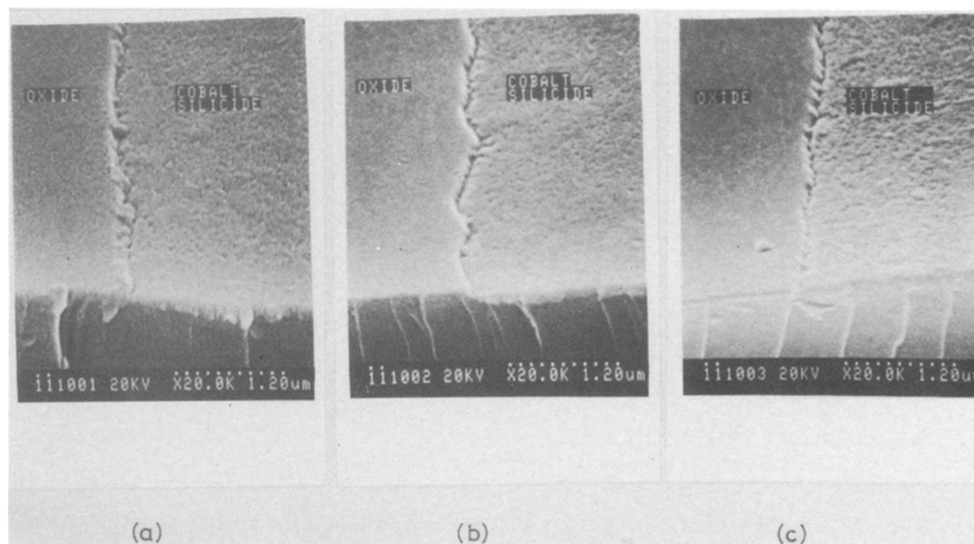

Fig. 6. SEM micrographs showing the surface morphology of the samples after annealing in N_2 for 30 min at: (a) 600°C, (b) 700°C, and (c) 800°C.

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act with the oxide layer under these annealing temperatures. Furthermore, the middle W layer reacts with the bottom Co layer to form a Co-W alloy, and the Co layer is completely converted into a Co-W alloy if the annealing temperature is higher than 700°C. From the phase diagram given in Ref. (13), it is seen that two intermetallic compounds do exist, namely, WCo_3 and W_6Co_7. Because the Co-W alloy can be etched in a solution of H_2O_2:NH_4OH (1:1) while Co cannot, this alloying can be further confirmed by etching all the samples in this solution to see whether there is a residual Co film. After etching in the solution, all those samples annealed above 700°C can unravel the bottom oxide layer, which means there is no residual Co film. But samples annealed below 700°C do have a residual Co film which can then be removed in a solution of HCl:H_2O_2 (3:1).

Because of this alloy formation, the Si/W/Co-W alloy structures were further investigated to see whether the Co-W alloys have a higher silicidation temperature than the pure Co films. The Co/W ratios that have been studied are 9:1, 7:3, 1:1, and 1:4. The alloys were formed by the codeposition of Co and W. The deposited amount of Co was fixed (equivalent to a Co thickness of 40 nm) and the Co/W ratios were achieved by changing the codeposited amount of W. The annealing was carried out between 600° and 800°C for 30 min in N_2. The resulting sheet resistance as a function of the annealing temperature is shown in Fig. 4. It can be seen that when the Co/W ratio is smaller than 1, no cobalt silicide can be formed, because the sheet resistance is constant for various annealing temperature and higher than that shown in Fig. 5, which is the result of the pure Co film. When the Co/W ratio is higher than 1, the smaller the Co/W ratio, the higher the sheet resistance is under the same annealing temperature. This means that the silicidation is retarded by the Co-W alloy. In other words, to obtain the same sheet resistance, higher silicidation temperature is required for samples with a smaller Co/W ratio. Thus, the conclusion can be made that when W atoms are incorporated in the Co film, the temperature needed to form cobalt silicide is raised. And the smaller the Co/W ratio, the higher the temperature is needed to form cobalt silicide. This phenomenon is similar to that in Ref. (14) where Ti-W alloys have higher silicidation temperatures than the pure Ti films. The possible explanations for the retarding effect of alloying upon silicide formation may be the same as that described in Ref. (15 and 16) for nickel silicide formation from a Ni-Cr alloy.

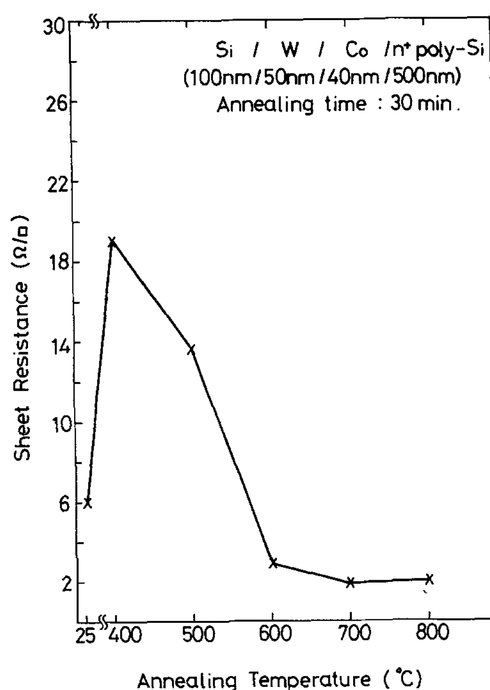

Fig. 7. The resulting sheet resistance as a function of the annealing temperature for Si/W/Co (100 nm/50 nm/40 nm) structures on n^+ poly-Si films.

Even though Co is the dominant diffusing species in forming $CoSi_2$ (8), a high-temperature (900°C) annealing (9) might cause the Si atoms to diffuse laterally on top of the oxide layer. Fortunately, as will be seen later, such a high annealing temperature is not necessary to form $CoSi_2$. Besides, from the above findings, the presence of a Co-W alloy layer upon the oxide layer can raise the silicidation temperature and thus prevent the possible formation of cobalt silicide upon the oxide layer. Indeed, it was found that no cobalt silicide can grow laterally on top of the oxide layer by using the Si/W/Co trilayer structure. The SEM pictures in Fig. 6 show that no lateral growth can be observed at those annealing temperatures of interest.

The resulting sheet resistance *vs.* the annealing temperature for Si/W/Co structures on single-crystal Si substrates and n^+ poly-Si films is shown in Fig. 5 and Fig. 7, respectively. These results are the same as those obtained in (7), except for one major discrepancy. The resulting sheet resistance of the 800°C annealing is a little higher than that of the 700°C annealing. Perhaps this is because of increased consumption of the Co film to form a thicker Co-W alloy as the annealing temperature is increased. Indeed, a thin Co-W layer is observed from Fig. 2. However, the formation of the initial cobalt silicide phases (Co_2Si and CoSi) are very fast at such high annealing temperatures (7, 8), and when the cobalt silicide front reached the Co-W alloy front, the formation of Co-W alloy is stopped. Thus, the thickness of the Co-W alloy formed upon single-Si substrates and poly-Si films is expected to be a weak function of annealing temperature. The resulting film resistivity of $CoSi_2$ is 20 $\mu\Omega \cdot$ cm which is calculated from the cobalt silicide thickness observed by SEM and the measured sheet resistance. This value is close to that obtained by other investigators (5,7). The thickness of the W film has been changed to 100 nm to observe its effect on the sheet resistance. No remarkable change of the sheet resistance is observed, unlike the case of titanium silicide (11) where sheet resistance is higher when a thick W film is used.

Conclusion

On the basis of the above results, the conclusion can be made that a good-quality and lateral-growth-free $CoSi_2$ can be formed easily by using a Si/W/Co trilayer structure and annealing at 700°-800°C for 30 min in an ordinary open-tube furnace with flowing N_2. The developed technique is simple, reproducible, and fully compatible with the conventional technology. Thus, it can be applied to the salicide process using cobalt silicide or other contact and interconnection formation technologies in VLSI.

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Study of Segregation Inhomogeneities in GaAs by Means of DSL Photoetching and EBIC Measurements

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ABSTRACT

Selective photoetching in HF-CrO_3 aqueous solutions (DSL method: diluted Sirtl-like etching with the use of light) and energy-dependent electron beam induced current (EBIC) have been employed to study segregation inhomogeneities in LEC grown n-type GaAs. The relationship between relative DSL etch depth and dopant concentration across growth striations has been established by means of local EBIC measurements of dopant concentration. It has been found that greater etch depths correspond to smaller dopant concentrations over a dopant concentration range of about one decade. These results are in agreement with the electrochemical model of GaAs etching in a DSL etching system, and can be explained in terms of surface recombination of the photogenerated carriers and cathodic protection.

Growth inhomogeneities (impurity and point defect segregation) are known to occur both in elemental and in compound semiconductors as a result of gravity-induced convection in the melt. They are usually recognized in the form of coring or striations which disappear under gravity-free conditions (1). Among the methods serving to reveal these inhomogeneities, wet chemical etching is most frequently used because of its simplicity and good resolution. Undoubtedly this resolution is strongly dependent on the sensitivity of the etchant, defined as the minimum etch depth required for clear visualization of the defects. In the case of III-V compounds, particularly GaAs, the so-called DSL etching system (2, 3) shows a very sensitive defect revealing action. Recently it has been demonstrated that when light is used an etch depth below 0.5 μm is sufficient to visualize clearly growth inhomogeneities in n-type and semi-insulating GaAs (4); some predictions about the photoetching behavior of an n/n^+ (mixed) system have also been made on the basis of both experimental observations and DSL etching theory (3). This paper is concerned with the calibration of DSL photoetching on n-type GaAs, containing well developed growth striations, by means of quantitative EBIC measurements in a scanning electron microscope.

Experimental

The samples were slices cut from liquid encapsulated Czochralski (LEC) grown n-type GaAs ingots. Sample no. 1 was <111> oriented, Si doped, and had a carrier concentration and mobility of about 2×10^{17} cm^{-3} and 3600 cm^2/V · s, respectively. Sample no. 2 was <100> oriented, Si-In codoped and had a carrier concentration and mobility of about 4×10^{17} cm^{-3} and 2600 cm^2/V · s, respectively. After cutting and mechanical polishing the samples were mechanochemically polished with a PA-7 solution (5) to get rid of any surface damage. Just before photoetching the samples were dipped in a HCl-H_2O solution. Both samples were photoetched for 30s in a $D_{1:1}S_{1/5}$ solution, *i.e.*, a 1:1 aqueous solution of the basic HF-CrO_3 mixture which contains 1 volume part of HF [48 weight percent (w/o)] and 5 volume parts of CrO_3 (33 w/o aqueous solution). During etching, the samples were illuminated by a large beam halogen lamp with an output power of about 320 mW/cm^2. Surface features after photoetching were examined by means of interference contrast microscopy, scanning electron microscopy, and step profiling.

EBIC measurements were performed in the same regions which had been investigated by photoetching, using Schottky barriers perpendicular to the electron beam. For precise quantitative EBIC measurements good electrical contacts to the samples are required. Therefore, after photoetching the samples were etched again in concentrated HCl to remove any residual oxide. The samples were then rinsed with isopropyl alcohol and dried with N_2 just before putting them in an evaporation unit (vacuum ~ 10^{-6} torr) for metallization. Very low resistivity ohmic contacts were obtained on the back surface by evaporating a $Au_{0.88}$-$Ge_{0.12}$ alloy and annealing the samples at 430°C for 5 min. Schottky barriers on the photoetched surfaces were obtained by evaporating gold at room temperature. All diodes had an indeality factor smaller than 1.05 as measured by current-voltage characteristics. Capacitance-voltage (C-V) measurements were employed to assess the quality of the diodes (*e.g.*, the barrier height which was (0.95 ± 0.05) eV for all diodes) as well as to evaluate the average dopant concentration in the diode areas which were 1-2 mm in diam.

Exact evaluation of local dopant concentration at segregation inhomogeneities was achieved by an EBIC method with a spatial resolution of about 10 μm (6). The method is

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