國 立 交 通 大 學

電信工程研究所

碩 士 論 文

使用摺疊電壓隨耦器以提升線性度之
互補金氧半轉導放大器設計

CMOS Operational Transconductor Amplifiers with Linearity Improving by Flipped Voltage Follower

研究生：陳伽維

指導教授：洪崇智 博士

中 華 民 國 九十九 年 九 月

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摘 要

近年來因為 CMOS 製程的發展，跟隨而來的短通道效應已經改變了許多類比電路的設計，因為製程由深次微米朝向奈米技術發展，短通道效應變成了一個主要的設計課題。短通道效應影響轉導放大器的線性度效能越來越明顯，而電晶體飽和區的公式將會受到短通道效應的嚴重影響，因此許多由理想電流公式所衍伸出的傳統轉導放大器架構在先進的製程中所受到的非理想效應，比起過去製程將會更多。

本論文提出兩種以減少非理想的小信號電阻之方法提升線性度，用以補償短通道效應所產生之非線性諧波成分。此外，本論文將介紹轉導放大器的主要應用：轉導電容式濾波器。於論文最後，將介紹一個轉導電容式四階低通濾波器的設計過程與完成。

本文提出的第一個轉導放大器是基於源極退化架構的轉導放大器並以摺疊式翻轉電壓隨耦器及正回授的迴路增強其線性度。此轉導放大器以台積電 0.18μm

CMOS 製程實現，其消耗功率 3.7mW，工作電壓為 1.8V。結果顯示當輸入信號為振幅為 0.6Vpp 且頻率 10MHz 時，達到第三次諧波失真為-70dB。此轉導放大器含接腳使用面積為 0.5mm × 0.395mm。

本文提出的第二個轉導放大器是基於虛差動對輸入轉導放大器並以改進過的摺疊式翻轉電壓隨耦器增強其線性度。此轉導放大器以台積電 0.18μm CMOS 製程實現，其消耗功率 0.7mW，工作電壓為 1.8V。結果顯示當輸入信號為振幅為 0.6Vpp 且頻率 10MHz 時，達到第三次諧波失真為-78dB。此轉導放大器使用面積小於 0.01 mm^2。 使用此轉導放大器作為建構濾波器的區塊，製作一個頻率 5Mhz 的轉導電容式濾波器，此濾波器的諧波失真為-48dB，其消耗功率 9.14mW，含接腳使用面積為 0.502mm × 0.612mm。

CMOS Operational Transconductance Amplifiers with Linearity Improving by Flipped Voltage Follower

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ABSTRACT

In recent years, the short channel effect has changed the way of designing analog circuits, which becomes a main issue as the technology marches to deep-submicron fields. The impact of the short channel effect on the design of the operational transconductance amplifier (OTA) becomes more serious and makes the circuit performance deviated from the ideal voltage-current equation, especially the performance of the linearity.

This paper presents two fully balanced structures of CMOS Operational Transconductance Amplifier (OTA) with high linearity, and its applications to Gm-C filters. The transconductors are designed for highly linear applications using methods which reduce non-ideal small signal resistance.

The proposed first circuit based on the source-degeneration structure and enhanced with modified Folded Flipped Voltage Follower and positive feedback for linearity improving was designed by the TSMC 0.18μm CMOS technology and

dissipates 3.7mW power with 1.8V voltage supply. The result shows the HD3 of -70dB with 0.6Vpp 10MHz input signal. It occupies the area of 0.5mm * 0.395mm, including pads.

The proposed second circuit based on the conventional pseudo-differential structure and enhanced with modified Folded Flipped Voltage Follower for linearity improving was designed by the TSMC 0.18μm CMOS technology and dissipates 0.7mW power with 1.8V voltage supply. The result shows the HD3 of -58dB with 0.6Vpp 10MHz input signal. The active area uses less than 0.01 mm^2. Using this OTA as building blocks, a 5MHz Gm-C low-pass filter was designed with the HD3 of -48dB. It consumes 9.14mW and occupies the area of 0.502mm * 0.612mm, including pads.

誌　　謝

隨著這份碩士論文的完成，六年來在交大的求學生涯也跟著告一個段落，往後迎接著我的，又是另一段嶄新的人生旅程。本論文得以順利完成，最先要感謝的，當然是我的指導教授洪崇智老師。這兩年的研究生涯中，給予我無微不至的指導與照顧，且讓我在研究主題上有無限的發展空間。而類比積體電路實驗室所提供完備的軟硬體資源，讓我在短短兩年碩士班研究中，學習到如何開始設計類比積體電路，乃至於量測電路，甚至單獨面對及思考問題的所在。此外要感謝陳富強教授，洪浩喬教授和闕河鳴教授撥冗擔任我的口試委員並提供寶貴意見，使得本論文更為完整。也感謝國家晶片系統設計中心提供先進的半導體製程，讓我有機會將所設計的電路加以實現並完成驗證。

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陳伽維 于 交通大學工程四館 718 實驗室

2010.9.20

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Chapter 1

Introduction

1.1 Motivation

The purpose of transconductor, operational transconductance amplifier (OTA), is ideally performing a linear conversion of input voltage to output current with an infinite bandwidth and output impedance [1]-[3]. Because the passive components relatively occupy much more area than the active elements in VLSI process, thus the passive resistances are replaced by transconductor which can save a lot of cost but degrade the linearity. Recently, current mode signal processing circuits demonstrated many advantages over voltage mode in the performance of bandwidth and lower supply voltage requirement. More and more researches about transconductor are proceeding, and now the transconductor become one of most important building blocks in analog and mix-signal circuits, including continuous-time Gm-C filters, continuous-time delta-sigma modulators, voltage controlled oscillator and multipliers.

Integrated analog filters play an important role in present communication systems and system-on-chip (SOC) solutions. The most popular technique for

realizing such analog filter is continuous-time filter, which can process the high speed signal continuously in time domain. There are three main techniques to implement integrated continuous-time filter: active-RC, MOSFET-C and G_m-C. The active-RC filter can provide very good linearity but cost a lot of die area for resistances and capacitors. The configuration of MOSFET-C filter has poor linearity due to the nonlinearity characteristic of the MOS transistors but it has better frequency response than the active-RC and MOSFET-C because of the open-loop operation of the OTA.

The performance of the G_m-C filter is highly dependent on the OTA building block, including the linearity and speed since it is formed only by OTAs and capacitors. Thus, most of the papers and researches are focus on to the linearity of the voltage-to-current conversion to improve the features of the filter [4]-[7].

The concepts of improving linearity under pseudo-differential topology are introduced in this thesis. There are many ways to improve linearity of conventional pseudo- differential circuit such as mobility compensation [8] which uses a well-sized weak inversion transistor to compensate the short-channel effects which generates harmonic distortion and lead to non-ideal voltage to current conversion or using two out-of-phase transconductor with unequal G_m value to cancel out the dominant distortion term [9] but this also cause the overall transconductance reduced because the main signal of output gets eliminated simultaneously. The concept proposed in this paper is to reduce the small-signal resistance connects to the pseudo-differential input pair which acts like a pair of resistors without losing the structural advantage of speed from pseudo-differential circuit using a modified version of folded flipped voltage follower.

1.2 Analog Filters

Filtering is such a common process that we often take it for granted. When we make a cell phone call, the receiver filters out all other channels so we only receive our unique channel. When we adjust the equalizer on a stereo system, we are selectively increasing or decreasing the audio signal in a particular frequency band, using a bandpass filter.

Filters play a key role in virtually all sampled data systems. Most A/D converters (ADCs) are preceded by a filter which removes frequency components that are beyond the ADC's range. Some ADCs have filtering inherent in their topology. In a sampled data system, frequency components greater than half the sampling rate "alias" (shift) into the frequency band of interest. Most of the time, aliasing has an undesirable side effect, so the "undersampled" higher frequencies are simply filtered out before the A/D stage. But sometimes, the undersampling is deliberate and the aliasing causes the A/D system to function as a mixer.

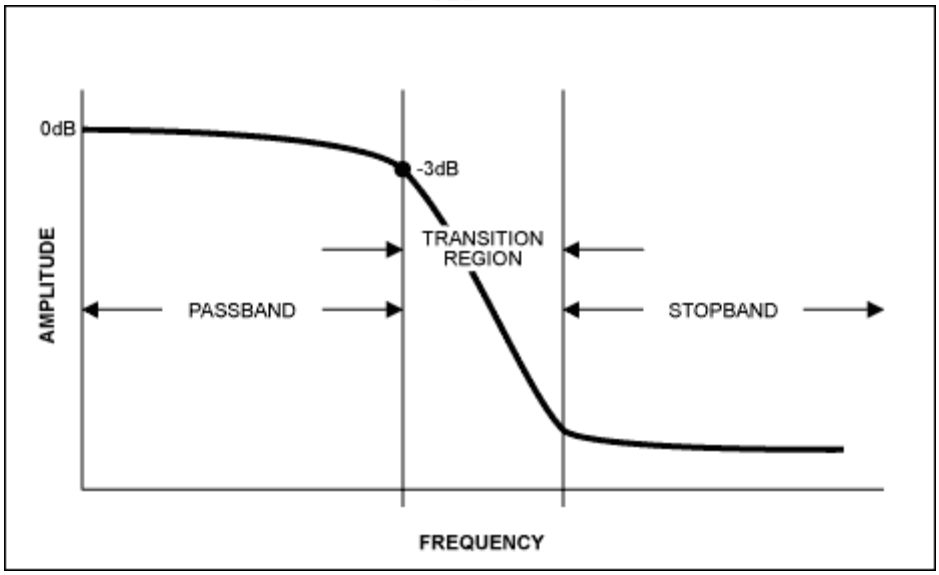


Figure 1

When selecting a filter, the goal is to provide a cutoff frequency that removes

unwanted signals from the ADC input or at least attenuates them to the point that they will not adversely affect the circuit. An anti-aliasing filter is a low-pass filter that accomplishes this. The key parameters that need observation are the amount of attenuation (or ripple) in the passband, the desired filter rolloff in the stopband, the steepness in the transition region and the phase relationship of the different frequencies as they pass through the filter. An graph of transfer function of filter is shown in figure 1.

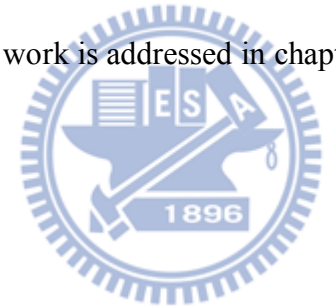
Nowadays, time continuous techniques are an alternative in low-frequency applications. Moreover, these techniques allow the integration of filters to operate from 1MHz to several hundreds of MHz. Continuous-time filters can deal with the analog signal without sampling, so they do not need pre-filtering and post-filtering to prevent aliasing problems. However, the precision of these filters is the major disadvantage.

In general, the active RC filters are suitable for low-frequency applications. The MOSFET-C filters are based on the active RC filters. The resistors of active RC filters are substituted for the CMOS, which is operated in triode region. One major drawback of this approach is the distortion. Moreover, the operating frequency of the filters is limited due to using the OPAMPs. Consequently, The MOSFET-C filters are not suitable for high-frequency applications. The operational transconductance amplifier-capacitor (OTA-C) filters, also called G_m-C filters, offer many advantages over other continuous-time filters that will be shown in this thesis.

This filter presented in chapter 4 can be used for video anti-aliasing and reconstruction filtering for composite (CVBS) or S-Video signals in standard definition digital TV (SDTV) applications.

1.3 Thesis Overview

This introduction is followed by chapter 2 which introduce some basic structures of transconductor operate with high linearity. It describes the advantages, disadvantages and circuit characteristics of these structures. Furthermore, some techniques for linearity-improving are described as well. Chapter 3 introduces the proposed circuit of transconductors, which presents a combination of couple concepts for linearity enhancement. Also, two applications are described in details including the circuit mechanisms, transconductance values, common-mode feedback, and noise analysis. Chapter 4 presents the construction of the G_m-C filter. Chapter 5 is the simulation and experimental results of fabricated circuits for both OTA and filter. Finally, the conclusion of this work is addressed in chapter 6.



Chapter 2

Transconductors

2.1 Introduction

The operational transconductance amplifiers are basic and important building blocks for various current-mode analog circuits and systems [1]-[3]. The purpose of the transconductor is ideally performing a linear conversion of input voltage to output current with an infinite bandwidth and output impedance. Because the passive components relatively occupy much more area than the active elements in the VLSI process, the passive resistances are replaced by the transconductor. More and more researches about transconductor are proceeding and the applications in analog and mix-signal fields including continuous-time G_m-C filters [4], continuous-time delta-sigma modulators, voltage controlled oscillator and multipliers have been developed. The main non-ideal properties of transconductor are limited output impedance, finite signal to noise ratio, finite bandwidth and most important of all, the limited linearity.

Several different techniques researches to compensate short channel effects have been published. Mobility compensation [10] uses a well-sized weak-inversion transistor to compensate the short-channel effect. Besides, two out-of-phase transconductors with unequal G_m values can cancel the unwanted components of

output signal as well [11]. However, the overall Gm may be reduced through this way because the main signal of output was eliminated simultaneously.

Accordingly, in this thesis, a technique of flipped voltage follower for compensating short channel effect is proposed. Also the technique can be applied to two basic transconductor structures which are pseudo-differential and source-degeneration structures. Basic and linearity improving transconductor circuits will be shown later in the chapter.

2.2 Basic transconductor structures

There are several basic operational transconductance amplifier discussed in this section alone with equations derived from ideal CMOS voltage to current relation. The pros and cons of these structures will also be discussed.

2.2.1 Differential input pair

A typical operational transconductance amplifier is discussed in this section. It is based on a differential CMOS input pair which is shown in figure 2.1. The ideal transistor current equations are used to verify its functionality.

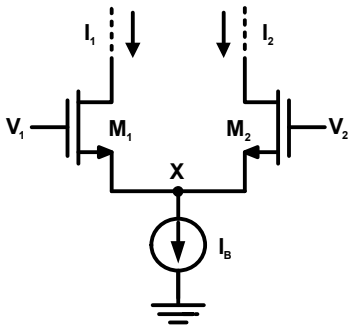


Figure 2.1 Differential input pair

This is a simple approach to maintain transconductance. The transistors M_1 and M_2 are operating in saturation region and I_B represent an ideal current bias. According to the transistor voltage-current equation, the output currents I_1 and I_2 are derived as

$$I_1=\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_1 (V_1-V_x-V_{thn})^2$$
$$I_2=\frac{1}{2}\mu_n C_{OX}\left(\frac{W}{L}\right)_2 (V_2-V_x-V_{thn})^2 \quad (2.1)$$

In equation (2.1) V_x is the voltage of node X in the figure 2.1, V_{thn} is the threshold voltage of NMOS M_1 and M_2 with the sizes $(W/L)_1=(W/L)_2$. The operational transconductance amplifier's output current I_O can be simply found by the difference between two drain currents I_2 - I_1:

$$I_O = I_2-I_1 = \mu_n C_{OX}\left(\frac{W}{L}\right)_{1,2}(V_2-V_1)(V_{CM}-V_X-V_{thn}) \quad (2.2)$$

Where V_{cm} is the common-mode voltage of circuit inputs and it suppose to be a constant DC voltage. According to the equation (2.2), we can see that the differential output current I_o will be perfectly proportional to differential input signal V_2-V_1 if V_x is a constant. Since parameters V_{cm} and V_{thn} are both constants. The drain voltage V_x can be expressed as

$$V_X = \sqrt{\frac{2I_B}{K_{I_B}}} \quad (2.3)$$

where K_{I_B} represent the process parameter $\mu_0 C_{OX}(W/L)_{I_B}$. In this analysis, we assume the current source I_B to be a constant, so the drain voltage of input pair V_x is also a constant. From small signal perspective, for an ideal tail current, the output resistance of the tail current is infinite which makes the node X virtual ground for small signal. Therefore the overall voltage to current transformation is linear with a constant transconductance value G_m

$$G_m = \frac{I_O}{V_2\text{-}V_1} = \mu_n C_{OX}\left(\frac{W}{L}\right)_{1,2}\left(V_{CM}\text{-}V_X\text{-}V_{thn}\right) \tag{2.4}$$

The circuit Gm value can be tuned by properly sizing the current source transistor or setting the bias current I_B.

In real life applications, the tail current voltage drop will not be a constant which is one of the sources of circuit's non-linear behavior. The voltage varies with input signal and process variation. Since I_B is typically formed by transistor current mirror, non-ideal terms are within it which makes V_X variant. The drain-source voltage of transistor also cause cannel length modulation which changes the effective resistance value $1/g_m$ and creates non-linear terms. Therefore, several techniques to maintain constant tail current voltage drop are proposed.

2.2.2 Pseudo-differential input pair

There is another typical structure of operational transconductance amplifier named pseudo-differential pair shown in figure 2.2. The configuration is similar to the basic CMOS differential pair but it is without a tail current to avoid the problem caused by varying tail current voltage drop.

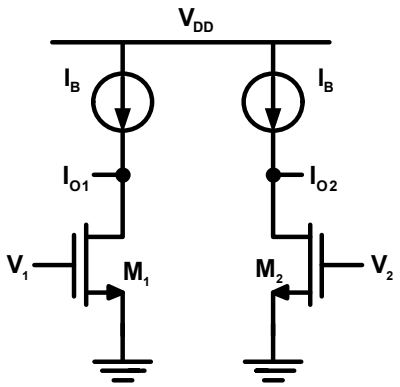


Figure 2.2 Pseudo-differential input pair

As the circuit shown above, the node V_X from figure 2.1 which affected by tail current I_B and caused many non-ideal effects is now grounded. Hence this modification of transconductor is developed with the absence of tail current to achieve better linearity. The pseudo-differential structure can be functional under lower power supply voltage since it is without the voltage drop across the tail current source. In addition, pseudo-differential structure is commonly used in low power or high frequency applications owing to its simple and compact configuration.

The formula of output current I_O is derived using ideal transistor current equation in saturation region. It is equal to I_2 - I_1 in figure 2.2:

$$I_O = I_{O2} - I_{O1} = \mu_n C_{OX} \left(\frac{W}{L} \right)_{1,2} (V_2 - V_1)(V_{CM} - V_{thn}) \tag{2.5}$$

where V_{CM} is the common-mode signal of input voltage V_1 and V_2. Comparing equation (2.2) and (2.5), the term V_X is absent in pseudo-differential structure equation which leads to better linearity. The voltage to current transformation transconductance value G_m of this circuit is shown as

$$G_m = \frac{I_O}{V_2 - V_1} = \mu_n C_{OX} \left(\frac{W}{L} \right)_{1,2} (V_{CM} - V_{thn}) \tag{2.6}$$

The pseudo-differential pair offers quality linearity, larger headroom, and operates at higher frequency. However, the structure does have some shortcomings such as its incapability to rejecting the common-mode signal and limited tuning range of transconductance.

The tuning of pseudo-differential structure can be achieved by tuning the voltage of body to adjust threshold voltage. This method offers limited tuning ability because the concern of leakage current. It can also be tuned by adjusting the input common-mode voltage, but the linearity performance is changed simultaneously. The linearity can be improved by increasing the gate overdrive voltage. Another problem

is its incapability to rejecting the common-mode signal which requires additional circuits to improve common-mode rejection ratio (CMRR). The CMRR is the ratio of the magnitude of the differential gain to the common-mode gain. An ideal differential amplifier has no common-mode gain and therefore has infinite CMRR. In this case, common-mode feedforward (CMFF) circuit is required which is shown in figure 2.3.

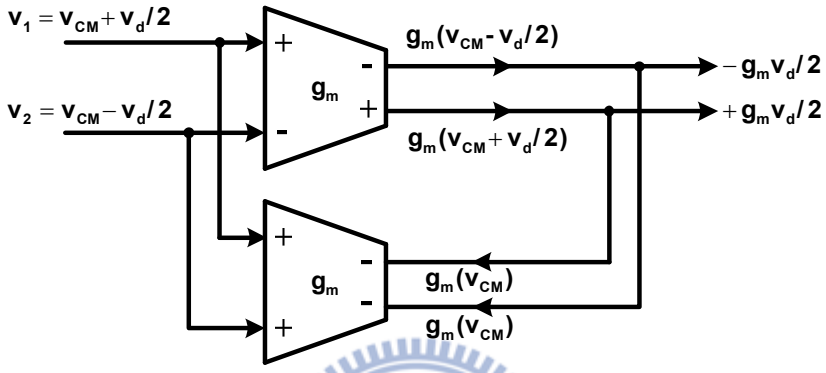


Figure 2.3 Conceptual graph of CMFF technique

The concept of common-mode feedforward is creating an input common-mode signal through another signal path to output node. The common-mode signals can be canceled out and leave only differential signals at output node. In other words, it suppressed common-mode gain and leaves differential-gain to obtain high common-mode rejection ratio.

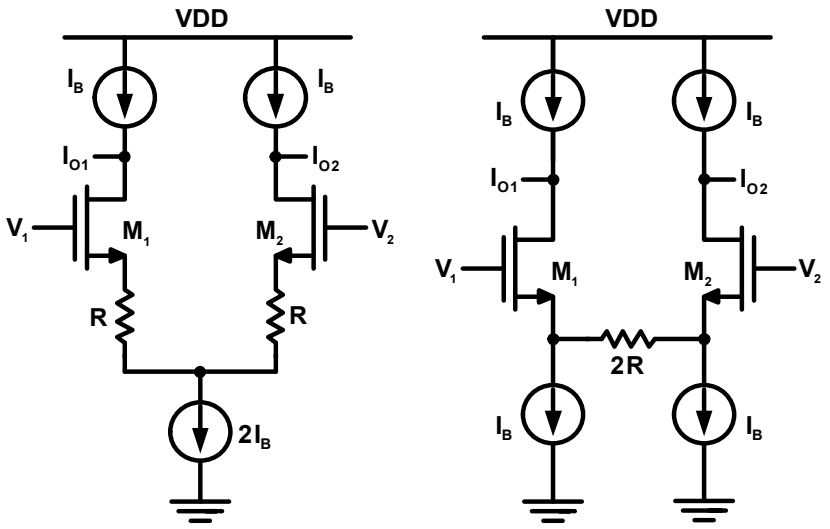
2.3 Linearity improving techniques

The purpose of the transconductor is ideally performing a linear conversion of input voltage to output current. Nevertheless, linearity has been an issue for all operational transconductance amplifiers especially the two conventional transconductor structures in the previous section since linearity in both circuits is

highly related to the transistor which is affected by process variation. In this section, five techniques for transconductor linearity enhancement are introduced.

2.3.1 Source Degeneration Differential Pair

Source degeneration structure is a widely used transconductor structure. The circuit is shown in figure 2.4. The main difference between source degeneration and original differential CMOS pair is the resistor connected between the sources of input transistors. The idea of this structure is to make signals from both input nodes go through transistor unchanged. The voltage drop over the resistor is thus the difference of two inputs; therefore the output current is generated from resistor and can be mirrored to output stage. Since the current is generated by resistor, it does not have non-ideal components from transistor like it does in other structures, thus leads to greater linearity performance.



(a) (b)

Figure 2.4 Source degeneration schematics

However, there are still non-ideal terms in this structure. By analyzing transistors from small signal perspective, the equivalent input resistance between V_1 and V_2 is not 2R. It has small signal resistance $2/g_{m1,2}$ between source node of transistor and resistor. The actual total resistance is $2/g_{m1,2}$ + 2R. The term $2/g_{m1,2}$ can be ignored if R is much larger than small signal resistance, therefore the nonlinear term $1/g_m$ will have minimal effect on the circuit. There are several ways to make the equivalent small signal resistance smaller to obtain higher linearity that will be discussed later this chapter.

The relationship of output current to the input voltage is shown as the following equation [1]:

$$i_o = \sqrt{1-\left(\frac{v_{id}}{2(1+N)V_{DS(sat)}}\right)^2} \times \left(\frac{\sqrt{2K_{1,2}I_b}}{1+N}\right)v_{id} \tag{2.7}$$

and the overall transconductance of input cell is:

$$G_m = \frac{1}{R}\left(\frac{N}{1+N}\right) \tag{2.8}$$

where $v_{id} = V_2 - V_1$, $V_{DS(sat)} = V_{GS(M1,M2)} - V_{tn}$ and $N = g_{m(1,2)}R$ is the source degeneration factor. By the equation (2.8), we can find the transconductance value is reduced by a factor of 1 + N. And the Taylor expansion of equation (2.7) can be derived and the third order harmonic term is shown as follow:

$$HD3 = \frac{1}{32}\left(\frac{1}{1+N}\right)^2\left(\frac{v_{id}}{V_{DS(sat)}}\right)^2 \tag{2.9}$$

In the equation (2.9), obviously, the HD3 of source degeneration pair degrades as the factor N becomes large. It means the circuit can reach high linearity by choosing large resistor R. However, the overall G_m will decrease as well.

In figure 2.4, two structures of source degeneration are presented, and both can be described by the same voltage to current transformation equation as in (2.7).

However, there some advantages and disadvantages for each circuit. In figure 2.4(a), the resistor requires a voltage drop, and then the range of the common-mode voltage is reduced, also the higher voltage supply is required. In figure 2.4(b), the noise of current source will appear at the output because two ways of current sources can generate unequal noise and feed to input transistor M_1 and M_2 separately. Otherwise the mismatch of the current source would reflect as the input offset.

2.3.2 Triode Transistor Input Pair

All the input pairs described above are operating in saturation region. In this subsection, we will introduce the transconductor input pair with transistors working in the triode region. When the transistor works in triode region, the voltage restriction $V_{DS} < V_{GS} - V_{tn}$ is satisfied. From the classical model equation for an n-channel transistor operating in the triode region:

$$I_D = \mu_n C_{OX}\left(\frac{W}{L}\right)\left[(V_{GS}-V_{tn})V_{DS}-\frac{V_{DS}^2}{2}\right] \tag{2.10}$$

To reduce even-order distortion products as almost all the practical continuous-time circuit, the differential structure is adopted. When the triode transistors arranged in differential type, we can derive that the output current and input voltage relation:

$$I_O = I_{O2}-I_{O1} = \mu_n C_{OX}\left(\frac{W}{L}\right)_{1,2} V_{DS}V_d \tag{2.11}$$

where V_d is the voltage difference between input voltage V_1 and V_2. We can see that

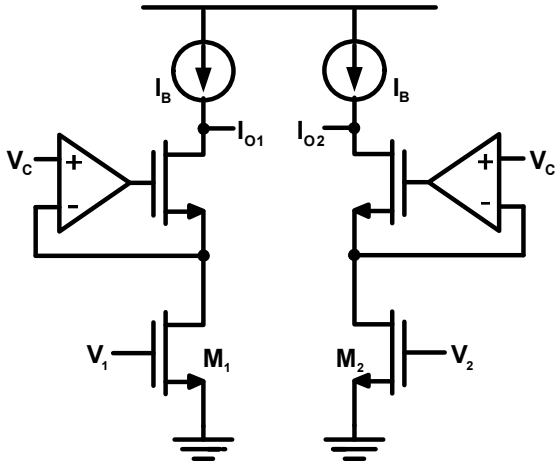


Figure 2.5 Constant drain-source voltage transconductor

the output current not only proportions to V_d but also V_{DS}. Therefore, if we want to get a linear voltage-current conversion, the drain-source voltage of the input transistors must keep constant. Figure 2.5 shows the circuit to implement the constant drain-source voltage transconductor with triode input pair M_1 and M_2. The virtual short feature of the OPamp can force the drain-source voltage of M_1 and M_2 equal to V_C, and thus the transconductance value can be tuned by voltage V_C as the equation described.

2.3.3 Flipped Voltage Followers

In this section, a basic cell for low-power or low voltage operation is introduced. Flipped voltage follower is one popular approach for low-voltage low-power circuit design, including the OTA design. The circuit is shown in figure 2.6 [12].

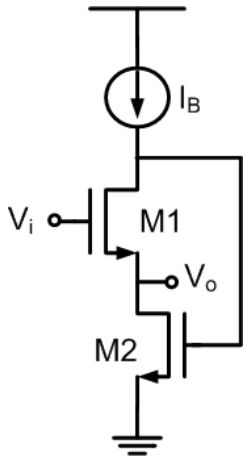


Figure 2.6 the Flipped Voltage Follower

The transistor M1 acts as a voltage follower which provides high input impedance while M2 forms a loop to create a low impedance node at the source of M1. Unlike the conventional voltage follower, the circuit is able to sink a large amount of current. However, the current source limits the sourcing capability. The large sinking capability is due to the low impedance at the output node. By analyzing the circuit, we can derive the output impedance $r_o = 1/g_{m1}g_{m2}r_{o1}$ approximately, where g_{mi} and r_{oi} are the transconductance and output resistance of transistor Mi, respectively.

2.3.4 Folded Flipped Voltage Followers

Another transconductor is shown in Fin. 2.7. This is another version of flipped voltage follower showed similar characteristics.

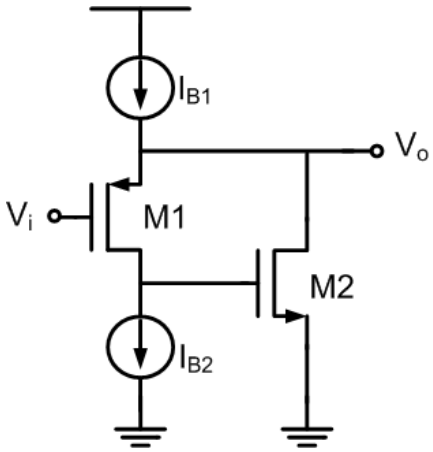


Figure 2.7 the Super Source Follower

The transistor M1 acts as a voltage follower which provides high input impedance while M2 forms a loop to create a low impedance node at the source of M1. The main behaviors are similar to flipped voltage follower. The major advantage of this structure over the original flipped voltage follower is that the input range is much larger, but at the cost of an extra current branch flows through M2. The properties of the super source follower are as follow. The output impedance of the super source follower is the same order as the flipped voltage follower, which is approximately $r_o = 1/g_{m1}g_{m2}r_{o1}$. Moreover, to acquire a correct operation point for the transistors M1 and M2, the condition $I_{B1}>I_{B2}$ must be satisfied.

2.3.5 Source Degeneration Differential Pairs with Positive Feedback

A transconductor with source-degenerated differential pair and a positive feedback gm-boosting circuit is shown in figure 2.8[13].

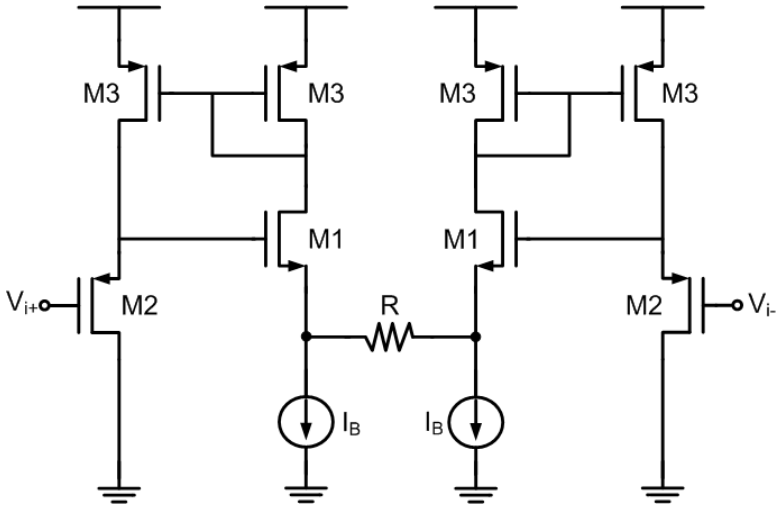


Figure 2.8 Source-degenerated Differential Pair with a Positive Feedback

The structure is based on the source degeneration differential pair and an extra boosting circuit. The main boosting circuit consists of transistors M2 and M3, with g_m of transistor M1 to be boosted. By choosing adequate M1 and M2 device dimensions, the positive feedback loop reduces the high source resistance to 50Ω. The approximate expression is as

$$R_s = \frac{1}{g_{m1}} - \frac{1}{g_{m2}} \tag{2.12}$$

where g_{mi} is the transconductance of transistor M_i. This equation suggests the linearity is inversely proportional to resistance.

Chapter 3

Proposed Operational Transconductance Amplifiers for High Linearity Applications

3.1 Introduction

An operational transconducance amplifier has the shortcoming of poor linearity. In the last chapter, several basic transconductor cells and methods for improving linearity are introduced. However, the overall linearity may not be sufficient for some applications.

With the advance of CMOS process technology, short-channel effects influence the performance seriously, especially in linearity. The voltage-current conversion no longer an ideal square function, more and more nonideal effects affect the circuits developed from this equation. Therefore, many compensation methods were proposed to improve linearity performance of a conventional transconductance circuit. Mobility compensation [10] uses a well-sized weak-inversion transistor to compensate for short-channel effect. Besides, two out-of-phase transconductors with unequal G_m values can be combined to cancel out unwanted components of output signal [11]. However, the overall G_m may be reduced through this way.

Therefore, there are two operational transconductance amplifier presented for

two types of basic structure including pseudo-differential input and source-degeneration input in this chapter that achieved high linearity and suitable for many applications.

3.2 Proposed Operational Transconductance Amplifier with Linearity Enhanced by Flipped Voltage Follower and Positive Feedback

A linearity enhanced operational transconductance amplifier which combines the flipped voltage follower with positive feedback is proposed. The FVF structure has great characteristics for high linearity OTA design as mentioned in chapter 2. Moreover, positive feedback loop is implemented with FVF thus achieved better linearity.

3.2.1 Transconductor Gm stage

The proposed transconductor has two stages of operation. One of those is the Gm stage, and another one is programmable current mirror stage. G_m stage is introduced in this subsection.

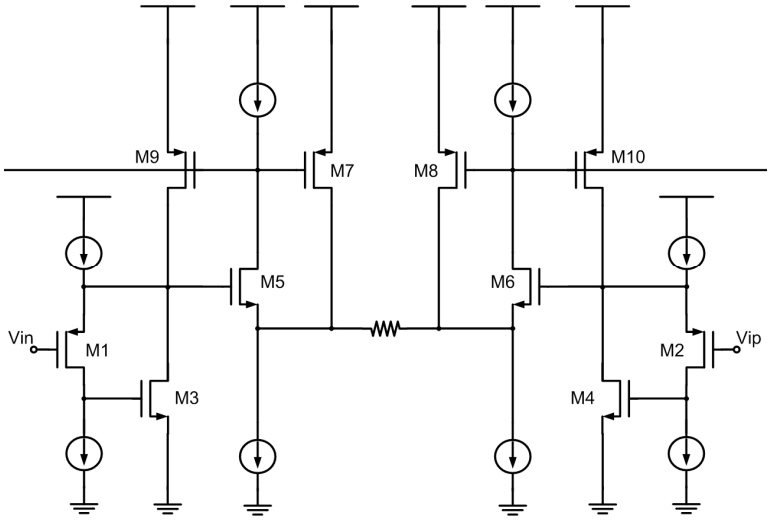


Figure 3.1 Transconductor G_m Stage

Transistors M1 to M4 and M5 to M8 are two pairs of folded flipped voltage follower. Negative feedback loops formed by these flipped voltage followers make the source of M1, M2, M5 and M6 became low impedance nodes. Moreover, with a same aspect ratio of M7 to M10, the positive feedback loops formed by M7 to M10 between voltage followers reduced the output impedance of nodes on both sides of resistor further more. The output impedance X and Y at source of M5 and M6 is given by

$$R_X \cong \frac{1}{g_{m5}g_{m7}r_{o5}} - \frac{1}{g_{m1}g_{m3}r_{o1}} \tag{3.1}$$

$$R_Y \cong \frac{1}{g_{m6}g_{m8}r_{o6}} - \frac{1}{g_{m2}g_{m4}r_{o2}} \tag{3.2}$$

This result is derived through several steps. At first, we transfer figure 3.1 into small signal model. And then, assuming the body effect is ignored for simplicity. Furthermore, the equations can be expressed by using the Kirchhoff's current law (KCL) and Kirchhoff's voltage law (KVL). Finally, the result is derived from these equations.

The value of R_X could approximate to zero by choosing appropriate device size for M1 to M8. By comparing the term with equation (2.12), the first and second terms of R_X are quite less than R_S. Therefore, the mismatch caused by process variation could be minimized. From the equations (3.1) and (3.2), the transconductance can be presented as

$$G_m = \frac{i}{V_{IP} - V_{IN}} = \frac{1}{R_{total} + R_X + R_Y} \tag{3.3}$$

where R_{total} is the sum of R_1, R_2 and R_{tune}. Minimizing the R_X can suppress the nonlinearity to acquire better total harmonic distortion (THD). As mentioned before, tuning the gate voltage of M25 can vary the transconductance.

Although this circuit is with many loops, stability of this circuit did not became an issue. The reason is that the output impedance and capacitance are larger than other nodes. As a result, the dominant pole is located at the output. Because the impedance and intrinsic capacitance of the other nodes are much lower than the output node, the second pole is in high frequency without affecting stability. The oscillation caused by positive feedback could be settled by larger common-mode feedback gain at cost of larger power consumption.

3.2.2 Programmable Current Mirror

Operational transconductance amplifier is an important building block of analog circuits. It is usually built with programmable characterics for versitile usage. Since the gm stage presented in previous section is lack of tuning mechanism. A current mirror with additional tuning ability is combined with the highly linear transconductance stage in the previous subsection. This operational transconductance amplifier is introduced in this section [15] [16].

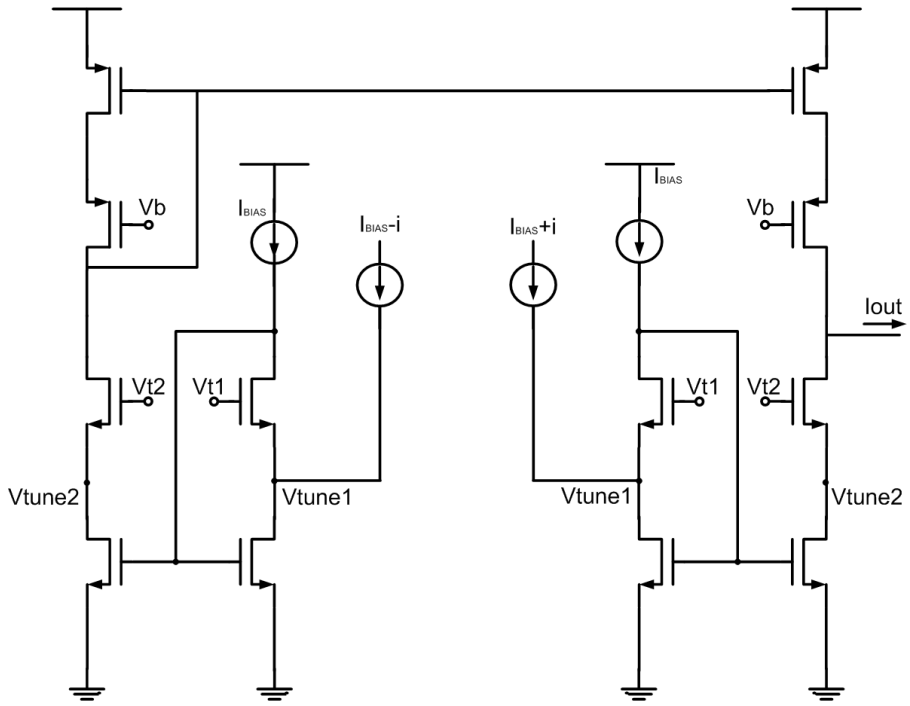


Figure 3.2 Programmable Current Mirror

The current mirror used transistors operating in triode region and external tuning voltage to achieve transconductance tuning. NMOS in this current mirror act as conventional low voltage cascode current mirrors. Bottom four transistors are the ones operate in triode region by controlling voltage V_{t1} and V_{t2} to make V_{DS} less than V_{DSSat}. Current flow into this current mirror from main G_m stage is scaled also by controlling voltage V_{t1} and V_{t2}.

The equation for transistor working in triode region is:

$$I_D = \beta\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS} \tag{3.4}$$

where

$$\beta = \mu_n C_{ox}\left(\frac{W}{L}\right) \tag{3.5}$$

If all the transistors are ideal, voltage equations $V_{tune1} = V_{tune2}$ applies. Thus current flow through transistor on the input side is

$$I_D = \beta\left(V_{GS} - V_{TH} - \frac{V_{tune1}}{2}\right)V_{tune1} = I_{BIAS} + i \tag{3.6}$$

and current flow through transistor on the output side is

$$I_D = I_{out1} = \beta\left(\left(\left(\frac{I_{BIAS} + i}{\beta} + \frac{V_{tune1}}{2}\right)/V_{tune1}\right) - \frac{V_{tune2}}{2}\right)V_{tune2} \tag{3.7}$$

Total output current is substraction of two sides of whole circuit.

$$I_{\text{out}} = I_{out1} - I_{out2} = 2\frac{V_{tune2}}{V_{tune1}}I_{\text{in}} \tag{3.8}$$

Gm value for the whole circuits is able to be adjusted by tuning the ratio of both of tuning voltages. The Gm of complete circuit is: $g_m = \frac{I_{out}}{V_d} = 2\frac{V_{tune2}}{V_{tune1}}/R$ ， R in this equation is the resistor used in the main Gm stage. The conventional method of using a MOS working in linear region to substitute for resistor provides a simple way to adjust transconductance. However, it suffers from the extra non-ideal effects generated from transistor used. These non-ideal terms affect parameters such as linearity, bandwidth, and gain, also makes the parameters vary with g_m. The programmable current mirror had been proposed to overcome this problem. It made that not to use transistor working in linear region possible which leads to higher linearity and fixed parameters such as bandwidth and gain.

3.2.3 Complete Transconductor Structure

A combination of previously mentioned gm stage and programmable current mirror made the complete transconductor structure.

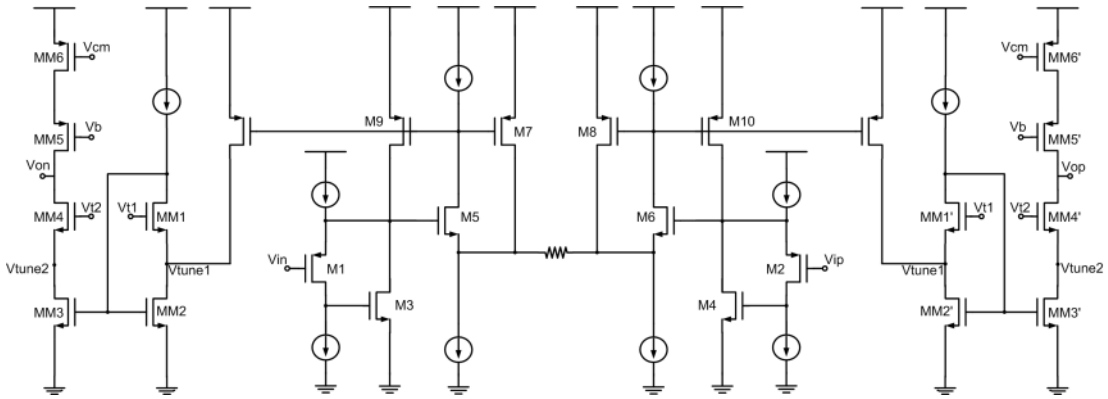


Figure 3.3 Complete Transconductor Structure

A highly linear operational transconductance amplifier is proposed. The new design makes use of the conventional source-degeneration structure, proposes a gm stage combines folded flipped voltage follower and positive feedback to improve linearity, and adds tuning functionality through a programmable current mirror while maintaining advantages of high linearity.

3.2.4 Common-Mode Feedback

In applications of G_m-C filter, the output of transconductor generally connects to input of the next transconductor. One specific common-mode voltage is designed with the circuit. Consequently, a common-mode feedback circuit is required to maintain correct voltage at both input and output nodes of transconductor cells.

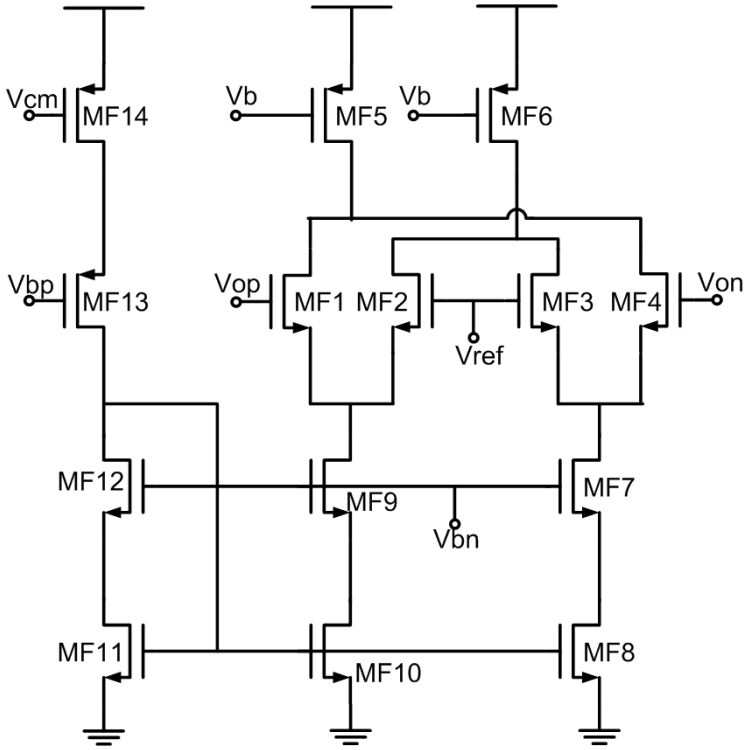


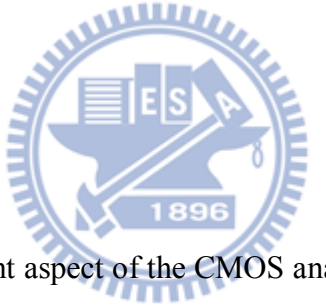
Figure 3.4 Common-Mode Feedback

The input transistors MF1 to MF4 are utilized to detect the common mode voltage and compare with the reference voltage. If the common mode voltage of the operational transconductance amplifier output signal is equal to the designed voltage V_{REF}, the current through MF10 will keep constant thus the voltage V_{CM} is fixed. Nevertheless, the common mode of the operational transconductance amplifier output signal is not the same as V_{REF} all the time. The voltage difference between them is mirrored through MF10 to vary V_{CM}, thus making the output common mode voltage to the designed value. For example, if the output common mode voltages are larger than the V_{REF}, the drain current of MF10 increases with it. The current mirror also makes the current through MF11 increase, thereby V_{CM} increased. In the output stage of transconductor, increasing V_{CM} leads to decrease of the output common mode voltage. This mechanism of negative feedback loop makes the output common mode voltage equal to V_{REF}.

When the operational transconductance amplifier operates at higher frequency, common-mode feedback circuit must be stable as well. The open loop gain of the common-mode feedback circuit is

$$A_{CMFB}(s) \cong g_{CMFB}(s) \times R_{out} = \frac{g_{mf1,mf4} \times R_{out}}{\left(1 + s\frac{C_A}{g_{mf10}}\right)\left(1 + s\frac{C_B}{g_{mf14}}\right)(1 + sC_L \times R_{out})} \quad (3.9)$$

where C_A and C_B are the total capacitance at the points of transistor 10 and transistor 14, respectively. From the equation (3.9), the dominant pole is at $1/(C_L \times R_{out})$ and the non-dominant poles are at g_{mf10}/C_A and g_{mf14}/C_B. The non-dominant poles should be designed far away from the unit gain frequency to increase the phase margin of the operational transconductance amplifier.



3.2.5 Noise Analysis

Noise is another important aspect of the CMOS analysis. Several source of noise are influential in CMOS component. Thermal noise is due to the random motion of electron which is independent to the DC current flow. Flicker noise is also called "1/f noise" which has a spectral density inversely proportion to the frequency. For high speed circuit, the most significant noise source of a transistor is the thermal noise. For simpler derivation, the channel noise is modeled by a current source connected between the drain and source with a spectral density

$$\overline{I_n^2} = 4kT\,\delta g_m(1+\eta) \quad (3.10)$$

where k is the Boltzmann constant, T is absolute temperature, δ is device noise parameter which is dependent on the operation region of the transistor, g_m is the small signal transconductance from gate to channel and η is defined as g_{mbs}/g_m which

depend on the bulk source voltage of transistor. By thermal noise model, the noise spectral density evaluated at the output node of proposed transconductor is derived as equation (3.11).

$$\overline{I_{n,out}^2} = 8kT\left\{\begin{array}{l}\delta\left(g_{mm3}+g_{mm6}\right)+\delta\left(g_{m1}+g_{m3}+g_{m7}+g_{m9}+g_{mm1}\right)\left(\frac{g_{mm3}}{g_{mm2}}\right)^2 \\ +\left[\left(\frac{R_{total}}{2}+\delta\right)\left(g_{m5}+g_{m7}\right)+\delta g_{mT1}R_{total}^2\right]\times\left(\frac{1}{1+R_{total}}\right)^2\end{array}\right\} \quad (3.11)$$

where g_{mT1} is the transconductance of tail current transistors. From equation (3.11), the source follower adds the input-referred noise while providing a voltage gain less than unity. The increase in degeneration factor, R_{total}, increases the noise contribution of the tail current transistors since it is split in an unbalanced way causing differential output noise. Moreover, it can be the most significant noise component for large degeneration factors. Thermal noise can be reduced at cost of lowering transconductance.

3.3 Proposed Tunable Pseudo-Differential Transconductor

Linearity of the operational tranconductance amplifier is one of the most important arguments in recent research. It can seriously affect the performance of the circuit constructed by operational tranconductance amplifier such as Gm-C filters. As described in previous section, a major non-linear term is approximately g_m which is a non-linear term that interferes the voltage to current conversion. Moreover, from experimental results of first chip, the linearity enhancement from flipped voltage follower is proven. The second chip makes use of it with another linearity enhancing technique: pseudo-differential structure and achieved better simulation result.

3.3.1 Modified Flipped Voltage Follower

To reduce non-linear terms generated from circuit, Folded Flipped Voltage Follower is introduced in chapter 2. This structure provides a low impedance node at source end of M1. The loop formed between transistor M1 and M2 makes impedance of the source node of M1 approximately $1/g_{m1}g_{m2}r_{o1}$, which is much smaller than original $1/g_{m1}$. In this section, a modified version is proposed.

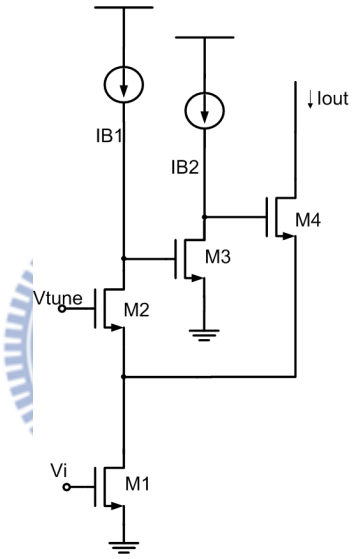


Figure 3.5 Modified Flipped Voltage Follower

A modified folded flipped voltage follower shown in figure 3 is proposed to maintain the merits of both pseudo-differential structure and flipped voltage follower. This modified circuit provides path to extract current to output from M1 to M4. The circuit has one extra single stage amplifier in signal path to make the gain higher which also makes equivalent impedance smaller

$$r_{eq} \cong \frac{1}{g_{m2}g_{m3}g_{m4}r_{o2}} \tag{3.12}$$

thus has reduced effects to resistor-like M1 to obtain higher linearity. This extra

single stage amplifier is used in the signal path to make it possible to use NMOS as M4 which results in lower supply voltage requirement. Current through M1 also has to be larger than I_{B1} to maintain proper functionality. Meanwhile, the voltage restriction at drain end of M4 is also reduced by one V_{GS} from $V_{GS}+2V_{DS}$ to $2V_{DS}$, which makes the design of output node at the same stage possible.

The idea of this circuit is to make use of the small resistance at the source of M2. When connected to a triode region transistor which is equivalent to a resistor, the effects of resistance are minimized, thus obtain highly linear results.

The tuning voltage V_{tune} is to control the drain voltage of input transistor working in triode region. Since the current flow through a triode region transistor is controlled by both drain voltage and gate voltage, controlling V_{tune} to alter the drain voltage is a good way to achieve transconductance tuning.

3.3.2 Complete Transconductor Structure

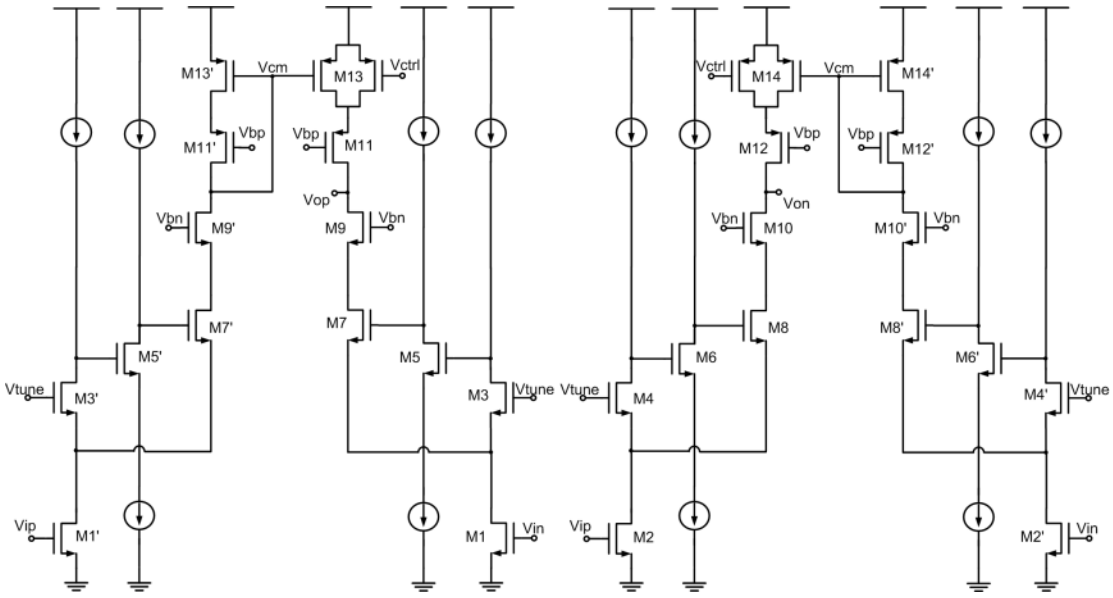


Figure 3.6 Complete Transconductor Structure

The complete schematic is shown in figure 5. M1 to M14 make the main OTA G_m stage [16], [25]-[28]. M1 and M2 are the input pair. From small signal perspective, we see the drain current is linear with respect to the applied drain-source voltage. Thus a small-signal resistance of

$$r_{DS} = \frac{1}{\mu_n C_{OX}\left(\frac{W}{L}\right)(V_{GS}-V_{tn})} \tag{3.13}$$

As the input transistor working in linear region acts like a resistor, the resistance would be proportional to the gate bias voltage and transconductance tuning can be added by following circuits. M3 to M8 creates a low impedance node connecting to M1 and M2 also provides a current path to subtract and gain output current. The drain-source voltage of input transistor can be tuned by simply altering the gate voltage of M3. From the low impedance node it created a equivalent small signal resistance of

$$r_{eq} \cong \frac{1}{g_{m2}g_{m3}g_{m4}r_{o2}} \tag{3.14}$$

which effects the input transistor much less than the original pseudo-differential transconductor $1/g_{m1}$.

The r_{eq} in series of input transistor is a major distortion term which can be minimized by circuit proposed. The disadvantage of pseudo-differential transconductor is the sensitivity of the input common-mode voltage. Additional distortion terms are produced by common-mode signal since there is only one signal path for both common-mode signal and differential- mode signal. Therefore, M1' to M14' are to make the common-mode signal path to output node in order to cancel out common-mode small signal thus make CMRR higher which is required in

pseudo-differential structure. The two paths does not only make common-mode signal cancel out at the output nodes, also makes the voltage amplitude and current flow at output node twice as much with same gm value and at the same power consumption as other feedforward techniques.

3.3.3 Common-Mode Feedback Circuit

When using a fully-differential circuit, if the output stage bias current which is mirrored from the previous stage has a mismatch due to the fabrication variation, the output DC level will be directly affected. The key to solving this problem is to sense the increase or decrease of output voltage and form a negative feedback loop circuit to react against the variation. The common-mode feedback scheme will be able to stabilize the common-mode output voltages of differential amplifier.

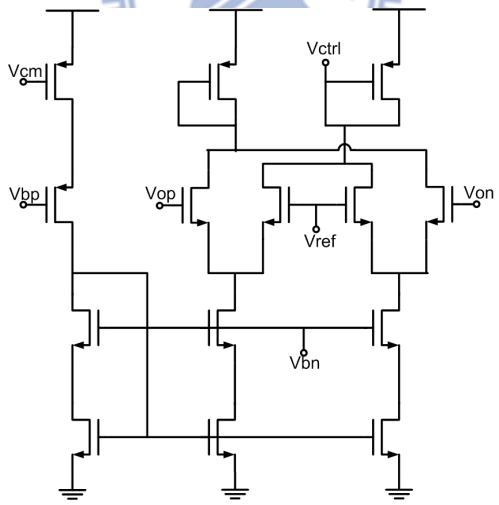


Figure 3.7 Common-Mode Feedback

The common-mode rejection ratio is generally worse on pseudo-differential structure than source degeneration ones due to the absence of tail current to control total current. Therefore an additional common-mode feedforward mechanism is

required otherwise transconductor will suffer from large common mode variation at output [17]-[19].

The extra circuit [24] to make output common mode voltage same as input common mode voltage is also required because when an OTA used as G_m of G_m-C filter, the output voltage is also the input voltage of the next stage. The input common-mode voltage is designed in the beginning. Therefore if there is difference between output voltage and the input voltage of next stage, the circuit might not function properly.

The common-mode feedback circuit [20] used to maintain the output voltage at the designed value which is shown in figure 3.7. There are 2 sets of common-mode feedback circuit used on each side of the circuit due to different V_{cm} on each side. Its currents are controlled by V_{cm} to make common-mode small signal flow through so common mode signals are able to cancel out at the output node.

3.3.4 Noise Analysis

For high speed circuit, the most significant noise source of a transistor is the thermal noise. The noise model for the channel noise of transistor is introduced in subsection 3.2.5. The model is constructed by a current source connected between the drain and source with a spectral density

$$\overline{I_{n,out}^{\ 2}} = 8kT\left\{\begin{array}{l}\left[\delta_{lin}g_{m1}+\delta_{sat}\left(g_{m3}g_{m5}g_{m7}+g_{m5}g_{m7}\right)\right]+\\ \left[\delta_{lin}g_{m1'}+\delta_{sat}g_{m5'}g_{m7'}\left(1+g_{m3'}\right)\right]\left(\frac{g_{m13}}{g_{m13'}}\right)^2\end{array}\right\} \tag{3.15}$$

where δ_{sat} and δ_{lin} are noise parameters at saturation and linear region respectively. Thermal noise can be reduced at cost of lowering transconductance.

Chapter 4

Transconductance-C Filters

4.1 Introduction

Filters play a key role in virtually all sampled data systems. Most A/D converters are preceded by a filter which removes frequency components that are beyond the ADC's range. Some ADCs have filtering inherent in their topology. The most popular technique for realizing such an analog filter is a continuous-time filter, which can process high-speed signals continuously in time domain. There are three main techniques to implement an integrated continuous-time filter: active-RC filter, MOSFET-C filter and G_m-C filter. The active-RC filter is constructed by OP amplifiers and passive elements resistors and capacitors. This filter structure provides good linearity and requires only designing a well performing OP amplifier. However, the resistors and capacitors it uses occupied enormous die area and significantly increased cost. The configuration of MOSFET-C filters replaces the resistors in an active-RC filter with the MOS transistors. Therefore, the resistance can be enhanced or depleted by applying an electrical field from a gate node. Nevertheless, the MOSFET-C filter generally has worse linearity due to the nonlinearity characteristics from the MOS transistors.

On the other hand, the Gm-C filter is formed by the capacitors and operational transconductance amplifiers which are basic and important building blocks for various current-mode analog circuits and systems [1]-[3]. The transconductance-C filter has a better frequency response than the active-RC and MOSFET-C structures because of the open-loop operation and simple circuit structure of the transconductor. However, the performance of the transconductance-C filter highly depends on the transconductor building block, including the linearity and working speed. Therefore, most researches focus on the linearity improvement in the voltage-to-current conversion blocks of the filter [4]-[6].

For design of Gm-C filter [21]-[23], all types of filters such as Biquad (second-order filter), Maximally flat magnitude filter, Chebyshev magnitude filter, Cauer filter, or LC ladder filter can be realized by Gm-C transconductance-capacitor filter. This circuit is designed using Chebyshev magnitude filter structure. The advantage of using Chebyshev magnitude lowpass filter is the performance of Q value is good compare to other structures under the same order which means the transfer function has a sharper difference between passband and stopband. The Q value is worse than Cauer filter, the reason not using Cauer filter is that fully differential type of Cauer filter requires more capacitors. Single-end OTAs are usually used under Cauer filter structure which leads to lower chip area demand under signal path theory.

The OTA introduced in section above is now used as a building block of Gm-C filter. Figure 6 showed a 4^{th}-order Chebyshev lowpass filter built by gm blocks. Since all stages are with its own input and output nodes. A common-mode feedback circuit is indispensable to maintain dc voltages the same as designed value.

4.2 Elementary Building Blocks for Gm-C filters

The filter is composed of only gm block and passive capacitors so the specification of OTA is critical to the performance of filter. The linearity of gm block is also proportional to filter linearity. The design of active filter is developed from the passive filter, which is constructed by resistors, capacitors and inductors. And the active-RC filter is consisted of resistors, capacitors and integrators. Both passive and active-RC filter have developed detailed design process including transfer functions design and circuits level implementation. If we can construct elements have a same effective loading as passive elements, all the researches about passive and active filter can be transferred to the transconductor-C filter just by replacing the transconductor-based building blocks into original elements. The passband of filter cannot surpass the unit-gain frequency of gm block; moreover, the passband can be adjusted by transconductance tuning. This tuning mechanism can be used to overcome the process and temperature variation applied to filter thus made the cutoff frequency accurate. Elementary building blocks for a Gm-C filter [14] are introduced in the following sections.

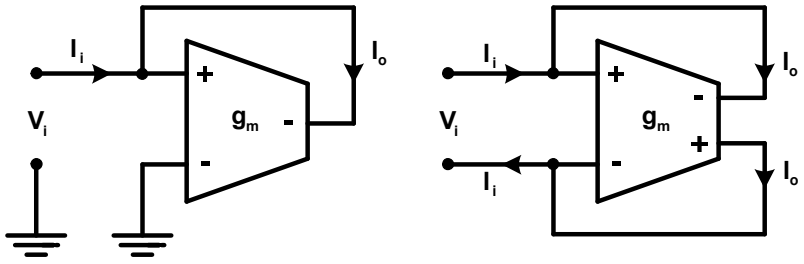
4.2.1 Resistors

There is generally little need for resistors in the area of Gm-C filters with the exception of source and load resistors in doubly terminated LC ladders. However, the resistor is a necessary element in active and passive filter for low-sensitivity design. Thus we should develop a Gm-based resistor for the fundamental building block before designing a Gm-C filter.

The configuration in figure 4.1(a) shows a transconductor with its negative

output terminal connected back to its positive input node. Since the transconductor input is ideally an open circuit, the input current I_i is equal to the transconductor output current. Thus

$$I_i = I_o = g_m V_i \tag{4.1}$$



(a) (b)

Figure 4.1 Resistor simulations with transconductors (a) grounded; (b) differential

Consequently, the circuit's equivalent resistance value is

$$R = \frac{V_i}{I_i} = \frac{V_i}{I_o} = \frac{1}{g_m} \tag{4.2}$$

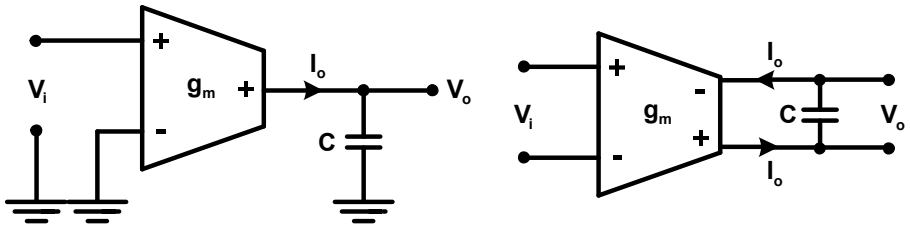
Note that this is a grounded resistor because V_i is referenced to ground and the inverse input node of transconductor is shorted to ground as well. For the differential usage, circuit is shown in figure 4.1(b). Notice that the feedback is negative as shown. A negative resistor with the resistance $-1/g_m$ would be created if positive feedback is used. This differential type Gm-based resistor has a resistance value of

$$R = \frac{V_+ - V_-}{I_i} = \frac{V_i}{I_o} = \frac{1}{g_m} \tag{4.3}$$

as in figure 4.1(b), the negative feedback makes the input current equal to the output current then the resistance $1/g_m$ is obtained. In addition, negative resistance could be used to compensate transconductor losses or to eliminate inductor losses when very small but real spiral-wound inductors are used on ICs for filters at highest frequencies.

4.2.2 Integrators

The implementation of an integrator is our next subject. An integrator is the main building block for most continuous-time filter. The fundamental circuit is obtained by loading a transconductor by an impedance which in a capacitor in this case. The circuit is as shown in figure 4.2.



(a) (b)

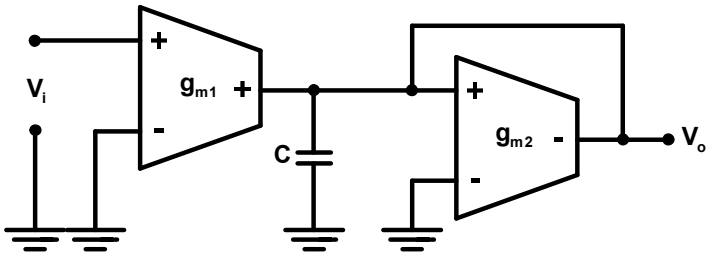
Figure 4.2 Transconductor-based integrator (a) grounded; (b) differential

As shown in figure 4.2(a), the circuit realizes

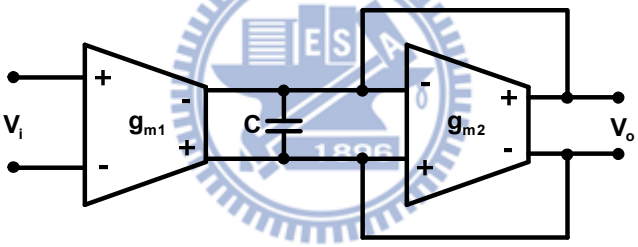
$$V_o = \frac{g_m}{sC} V_i \tag{4.4}$$

thus the fundamental building block of G_m-C filter which is the G_m-C integrator is obtained. In this block, integrator has differential inputs, that is, if an inverting or non-inverting integrator needs to be realized, we may use the same circuit with simply changing signs of inputs without separate inverter used. This analysis is based on that if we assume the integrator is ideal. In reality, the voltage controlled current source is loaded by extra parasitic capacitance and resistance. It follows that the integration capacitor is increased by the parasitic output capacitance of the gm cell. The integrator also has finite dc gain which is $g_m/g_o=g_m r_o$. From these conditions, one can see the reason for having as large an output resistance as possible in a transconductor. Also that if the loading capacitor is not large enough, output parasitic capacitance must be taken into consideration during design procedures.

For differential type transconductor, the Gm-C integrator was implemented in figure 4.2(b), and the relation between input and output is identical with grounded type integrator as in equation (4.4). This model converts the voltage $V_o = V_i^+ - V_i^-$ into a current by the transconductor; then the current is integrated on capacitor C to generate the voltage $V_o=(g_m/sC)V_i$.



(a) single-end transconductor



(b) differential transconductor

Figure 4.3 A lossy integrator as a simple first-order lowpass filter

For a filter based on two-integrator loops, one of the integrators must be lossy. One resistor connected in parallel with capacitor is the only thing needs to be done making a lossy integrator as shown in figure 4.3. The transfer function of this circuit is

$$\frac{V_o}{V_i} = \frac{g_{m1}}{sC + g_{m2}} \tag{4.5}$$

For the differential integrator shown in figure 4.3(b), it is conceptually two single-ended integrators. One is for positive signal path and another one is for

negative signal path. It has the same transfer function as single-ended integrator.

4.2.3 Gyrators

Gyrator is also a useful elementary building block. It is a two-port device whose input impedance is inversely proportional to load impedance. Its most useful characteristic is that it allows converting a capacitor into inductor.

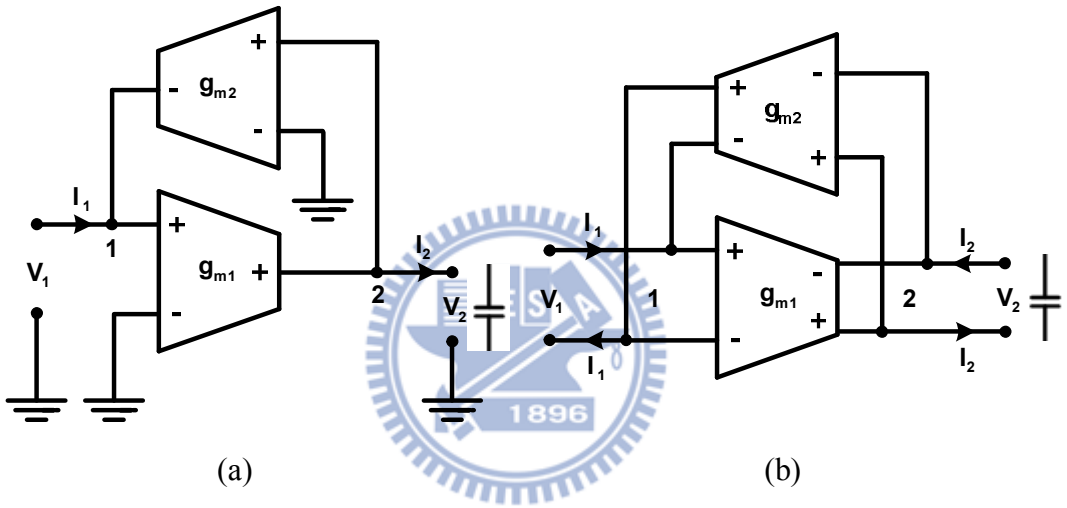


Figure 4.4 Design of (a) grounded transconductor-based; (b) differential transconductor-based, impedance inverter, the gyrator

A design of gyrator is shown in figure 4.4. It is realized with transconductors since there are difficulties doing it with operational amplifiers because it is fundamentally a connection of an inverting and non-inverting voltage-controlled current source. The gyrator shown in figure is characterized by these equations:

$$I_1 = g_{m2}V_2 \quad \text{and} \quad I_2 = g_{m1}V_1 \tag{4.6}$$

the impedance relation between $Z_1 = V_1/I_1$ and $Z_2 = V_2/I_2$ can be derived as

$$Z_1 = \frac{V_1}{I_1} = \frac{1}{g_{m1}g_{m2}}\frac{I_2}{V_2} = \frac{1}{g_{m1}g_{m2}}\frac{1}{Z_2} \tag{4.7}$$

From this equation, if Z_2 is a capacitor, Z_1 is an inductor with a value of $L=C/(g_{m1}g_{m2})$. Likewise, we can make a differential type gyrator by combining two single-ended gyrators and result in figure 4.4(b). When the loading capacitor is applied at node 2, we will get an equivalent inductor derived as follow

$$Z_1 = \frac{1}{g_{m1}g_{m2}} \frac{1}{1/sC_{load}} = \frac{1}{g_{m1}g_{m2}} sC_{load} \tag{4.8}$$

$$Z_{inductor} = s \cdot L_{eq} = s \cdot \frac{C_{load}}{g_{m1}g_{m2}} \quad \rightarrow \quad L_{eq} = \frac{C_{load}}{g_{m1}g_{m2}} \tag{4.9}$$

and the transconductor-based inductor is constructed. Base on the elements introduced in this section, including resistor, integrator and gyrator, various types of continuous-time filter can be converted into G_m-C form.

4.3 Fourth-order filter implementation

Design of high-order g_m-C filter proceeds along the same line as the design of operational amplifier based high-order filter. There are two fundamental methods available which are the cascade approach and the ladder approach. The cascade design is used in this thesis and firstly we will discuss elementary first and second-order filter block. Then the higher-order filters can be implemented by simply cascading basic filter blocks.

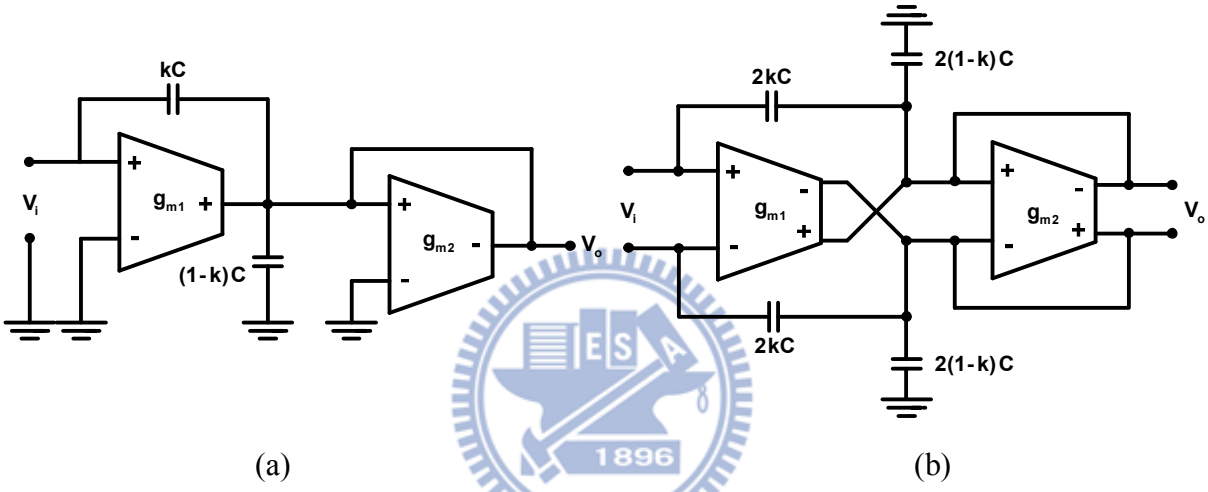
4.3.1 First order filter

A universal first-order filter can be based on the lossy integrator introduced in previous section. The lossy integrator needs only to be augmented with one additional capacitor to generate a general first-order numerator. This first-order filter is shown in figure 4.5. A fraction kC of the integrator is lifted off ground and be used to feed a

portion of input signal directly to C. Current equation at the output node can be found by the Kirchhoff's current law, thus we obtain

$$V_o(sC + g_{m2}) = V_i(g_{m1} + skC) \rightarrow \frac{V_o}{V_i} = \frac{skC + g_{m1}}{sC + g_{m2}} \tag{4.10}$$

Various filters can be realized by this general transfer function. A first-order highpass filter can be obtained by removing g_{m1}. Allpass filter can be achieved by choosing $g_{m1}=-g_{m2}$ and k=1. A lowpass filter that will be used in next section is gained by setting k equals zero.

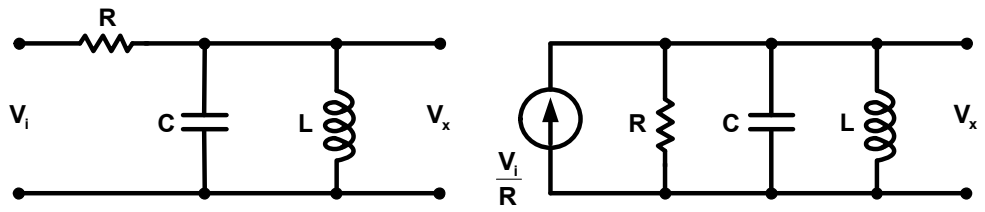


(a) (b)

Figure 4.5 First-order section in (a) grounded type; (b) differential type

4.3.2 Second-order section

A second-order g_m-C filter is transformed from passive RLC circuit in figure 4.6(a). Figure 4.6(b) is from source transform of figure 4.6(a). We can use blocks introduced in section 4.2 to substitute passive elements and obtain the transconductance-C implementation shown in figure 4.6(c).



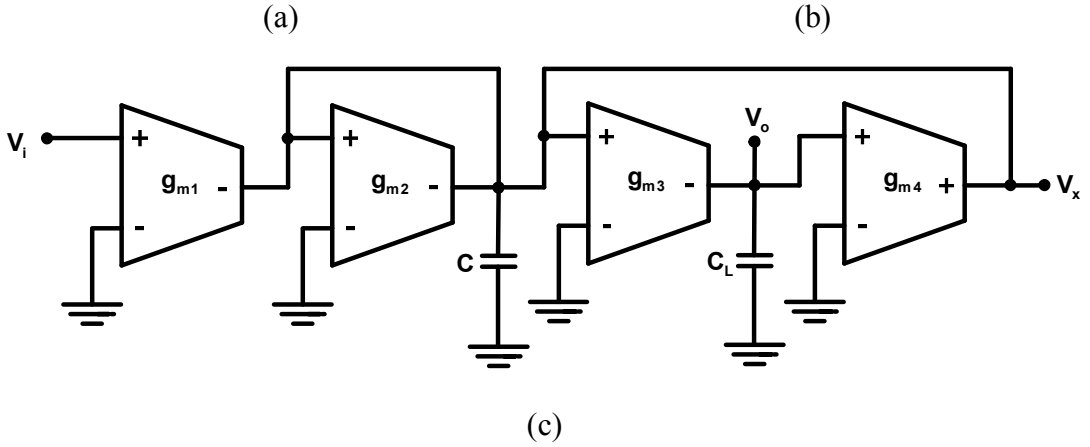


Figure 4.6 The steps of converting a passive RLC filter to the G_m - C filter

g_{m1} converts the input voltage to a current, g_{m2} represent the grounded resistor R, the capacitor C is unchanged, and g_{m3} and g_{m4} form a gyrator, which implements the inductor L together with the capacitor C_L. Transfer function of this filter is

$$\frac{V_x}{V_i} = \frac{G}{G + sC + \frac{1}{sL}} \tag{4.11}$$

where G is the conductance of resistor R. By substituting equivalent impedance of G_m-C building block into equation (4.11), the transfer function becomes

$$\frac{V_x}{V_i} = -\frac{g_{m1}}{g_{m2} + sC + \frac{g_{m3}g_{m4}}{sC_L}} = -\frac{sC_L g_{m1}}{s^2 C_L C + sC_L g_{m2} + g_{m3}g_{m4}} \tag{4.12}$$

where the minus sign of the function comes from the polarity of output current of g_{m1}. Notice that in figure 4.6(c), the node V_x is not our desired output, and the replaced one is the node marked V_o, which correlates with V_x in the relation of

$$V_o = -\frac{g_{m3}}{sC_L} V_x \tag{4.13}$$

so that the node V_o has a lowpass output

$$\frac{V_o}{V_i} = -\frac{g_{m3}}{sC_L}\frac{V_x}{V_i} = \frac{g_{m1}g_{m3}}{s^2 C_L C + sC_L g_{m2} + g_{m3}g_{m4}} \tag{4.14}$$

A general form of transconductor-C biquad section is also made and shown in

figure 4.7. In this circuit, we use two parameters "m" and "n" to control the overall transfer function by changing capacitors' ratio. Two additional inputs V_3 and V_4 are applied to generate arbitrary transmission zeros. The node equations of V_2 and V_o is derived as equation (4.15) and (4.16) respectively.

$$V_2 s(1-m)C_1 + V_2 g_{m2} = g_{m1}V_1 + g_{m4}V_o + (V_3 - V_2)smC_1 \tag{4.15}$$

$$(V_4 - V_o)snC_2 = V_2 g_{m3} + V_o s(1-n)C_2 \tag{4.16}$$

then eliminate V_2 from these equations, the transfer function will be

$$T(s) = \frac{V_o}{V_i} = \frac{s^2 nC_1C_2\frac{V_4}{V_i} + s\left(nC_2 g_{m2}\frac{V_4}{V_i} - mC_1 g_{m3}\frac{V_3}{V_i}\right) + g_{m1}g_{m3}\frac{V_1}{V_i}}{s^2 C_1C_2 + sC_2 g_{m2} + g_{m3}g_{m4}} \tag{4.17}$$

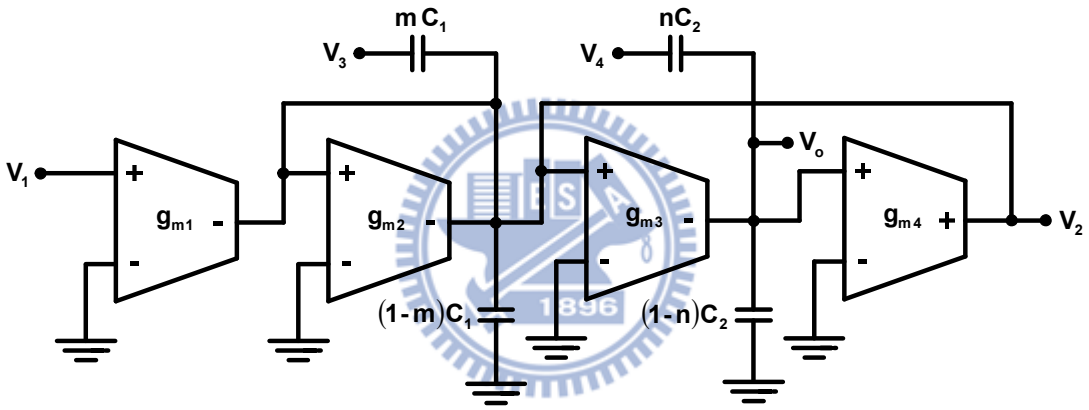


Figure 4.7 The general form of transconductor-C biquad section

where the voltage ratios in the numerator will be determined as ± 1 or 0. For example if we want to create a lowpass filter, then we set the input V_1 equal to V_i, and V_3 and V_4 are set to ground. Thus the circuit is same as figure 4.6. The fully-differential form of the circuit is shown in figure 4.8. Notice that if we want to obtain a same transfer function as derived in equation (4.17), the size of capacitors should be twice.

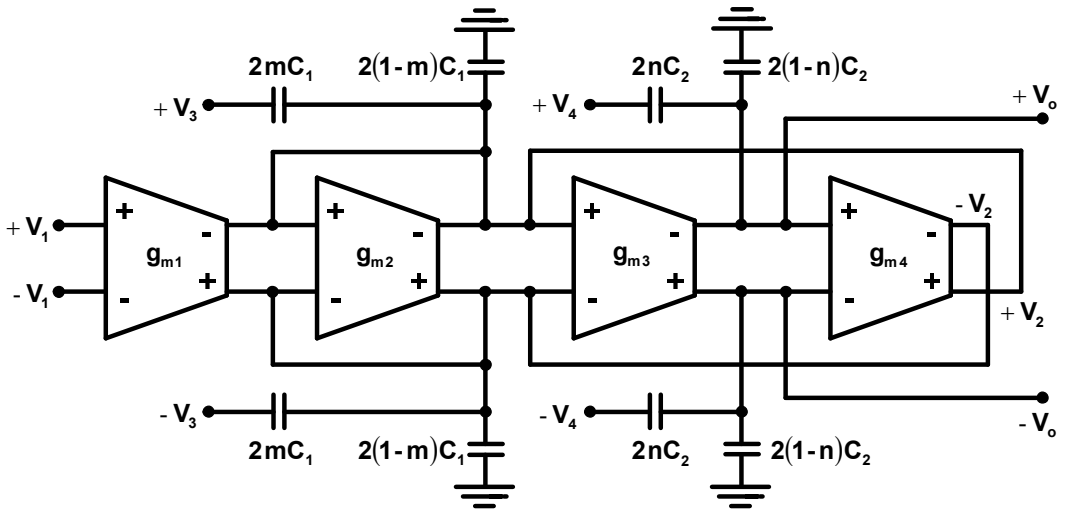


Figure 4.8 The transconductor-C biquad section in fully-differential form

4.3.3 Fourth-order filter

There are several types of filter have been developed, including Butterworth response, Chebyshev response and Elliptic response. Chebyshev response is choosen to be the transfer function of the filter because it occupies less silicon area while having moderate performance.

In the practical applications, it requires filters having ability to reject the outband signal strongly to attain high transmission quality. Generally the fourth-order filter is required. The fourth-order lowpass Chebyshev transfer function with will be

$$T(s) = \underbrace{\frac{03563}{s^2 + 0.8466s + 0.3563}}_{biquad\ 1} \cdot \underbrace{\frac{1.0636}{s^2 + 0.3508s + 1.0636}}_{biquad\ 2} \tag{4.18}$$

for biquad one and two, the Q values are 0.7051 and 2.9399, respectively; α_{max} = 0.5dB. The choice of capacitors depends on the g_m value and the desired cutoff frequency. We can find the design equations for the two capacitors:

$$C_1 = \frac{g_m}{\omega_0} Q \qquad C_2 = \frac{g_m}{\omega_0} \frac{1}{Q} \tag{4.19}$$

where ω_0 is the cutoff frequency of the filter in the dimension of rad/s. Notice that the

capacitor ratio equals Q^2, thus the high Q system is not suitable for transconductor-C filter.

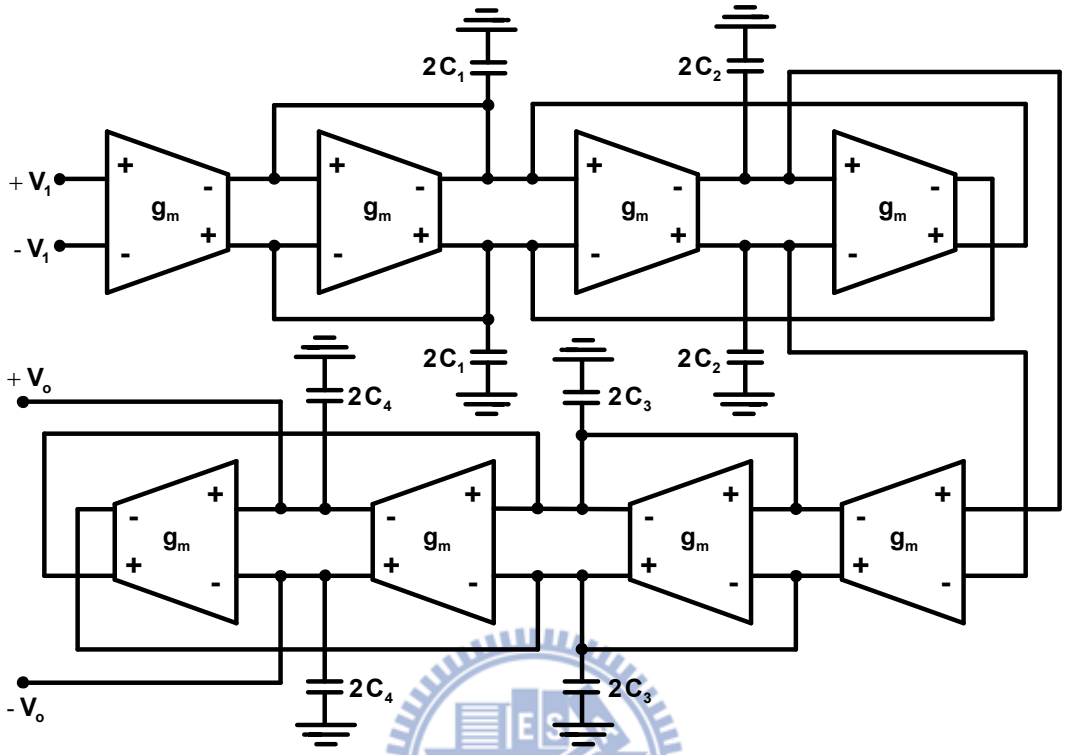


Figure 4.9 The fourth-order Chebyshev response lowpass filter realized in transconductor-C architecture

Chapter 5

Simulation and Experimental Results

5.1 Introduction

There are numbers of transconductor specifications such as total harmonic distortion, third-order harmonic distortion, common-mode rejection ratio, power supply rejection ratio, and power consumption. These parameters will be explained in this section.

5.1.1 Total harmonic distortion (THD)

The total harmonic distortion is a measurement of distortion in output signal. It is defined as ratio of the sum of all harmonic signals to fundamental signal. Equation 5.1 is a common definition for measurement based on amplitudes and equation 5.2 is the one used for measuring transconductor distortion which uses dB as its unit.

$$THD = \frac{V_{D2}^2 + V_{D3}^2 + \ldots + V_{Dn}^2}{V_1^2} \tag{5.1}$$

$$THD = 10\log\left(\frac{H_{D2}^2 + H_{D3}^2 + \ldots + H_{Dn}^2}{H_1^2}\right) \tag{5.2}$$

V_1 and H_1 are the fundamental signal and power. V_{Dn} and H_{Dn} represent the amplitude and energy of nth-order harmonic component respectively.

For a nonlinear system which has an input signal $v_i(t)$ and an output signal $v_o(t)$. The output signal can be written in Taylor series expansion of the input signal. In a fully differential system, the even order harmonic terms gets cancelled ideally. Moreover, the harmonic terms get lower as number of order increases thus can be neglected. For a simpler measurement, we use the third-order term to approximate the distortion in circuit. Output signal can be expressed as:

$$v_o(t) \cong a_1 v_i(t) + a_3 v_{in}^3(t) \tag{5.3}$$

where a_1 and a_3 characterize the linear parameter and third-order parameter in transfer function respectively. When the sinusoidal signal $v_i(t) = A\cos(\omega t)$ is given at the input, output signal is derived as

$$v_o(t) \cong H_1 \cos(\omega t) + H_3 \cos(3\omega t) \tag{5.4}$$

where

$$H_1 = a_1 A \tag{5.5}$$

$$H_3 = \frac{a_3}{4} A^3 \tag{5.6}$$

and finally the third-order harmonic distortion ratio is given by

$$HD3 = \frac{H_3}{H_1} = \left(\frac{a_3}{4a_1} \right) A^2 \tag{5.7}$$

which can be used to approximate total harmonic distortion in a device.

5.1.2 Common-mode rejection ratio (CMRR)

Common-mode rejection ratio is the tendency of a device to reject input signals that is common to both input ends. A high common-mode rejection ratio implies the circuit has better quality processing two ended signal. A differential device ideally takes voltages from both ends and produces differential signal with differential gain

A_D and rest with common-mode gain A_{cm}.

$$V_o = A_D(V_+ - V_-) + \frac{1}{2} A_{cm}(V_+ + V_-) \tag{5.8}$$

CMRR is the ratio of the differential gain A_D over the common-mode gain A_{cm} as shown in equation (5.13). An ideal differential amplifier has a zero common-mode gain A_{cm} and therefore has infinite CMRR.

$$CMRR = \left| \frac{A_D}{A_{cm}} \right| \tag{5.9}$$

5.1.3 Power supply rejection ratio (PSRR)

The term power supply rejection ratio is used to describe the amount of noise and voltage variation from power supply a device can reject. PSRR is defined as the product of ratio of the change in supply voltage to the change in output voltage of the circuit caused by the change in the power supply and the open-loop gain of the circuit. Therefore

$$PSRR = \frac{\Delta V_{Supply}}{\Delta V_{OUT}} \cdot A_D = \frac{A_D}{A_P} \tag{5.10}$$

where A_D is the differential gain and A_P is the gain from power supply to the output of the circuit. It is usually given with different frequencies other than DC.

5.1.4 Power

Electric power is defined as the rate at which electrical energy is transferred by an electric circuit. In the field of electric, the power of a circuit is defined as

$$P = I \cdot V \tag{5.11}$$

where the voltage V is the power supply voltage and the I is the current transferred from the power supply.

5.2 Performance of OTA with Linearity Enhanced by Flipped Voltage Follower and Positive Feedback

There are numbers of simulations run to obtain various properties of the transconductor proposed. Simulation results will show specifications such as transconductance value, frequency response, phase response, harmonic distortion, common-mode rejection ratio, and power supply rejection ratio. These simulations will be shown in the following text. This section also contains measurement results and chip micrograph.

5.2.1 Simulations

The transconductance values with different tuning voltage is shown in figure 5.1. Vertical axis represents the transconductance value and horizontal axis shows the input range.

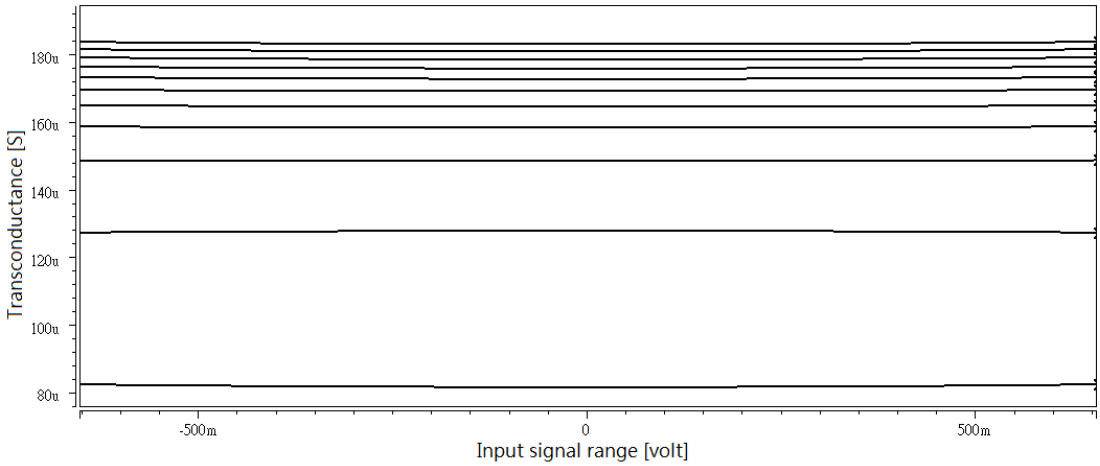


Figure 5.1 Transconductance value with different tuning voltage

The transconductance value varies from 130u to 185μA/V as tuning voltage goes up from 0.1v to 0.45v. The values stay almost the same which indicates that distortion will be small.

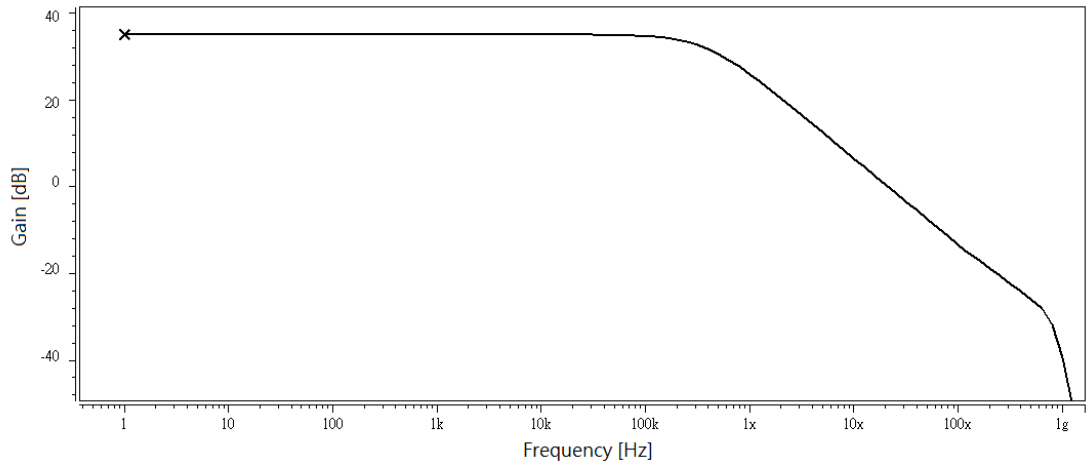


Figure 5.2 Frequency response

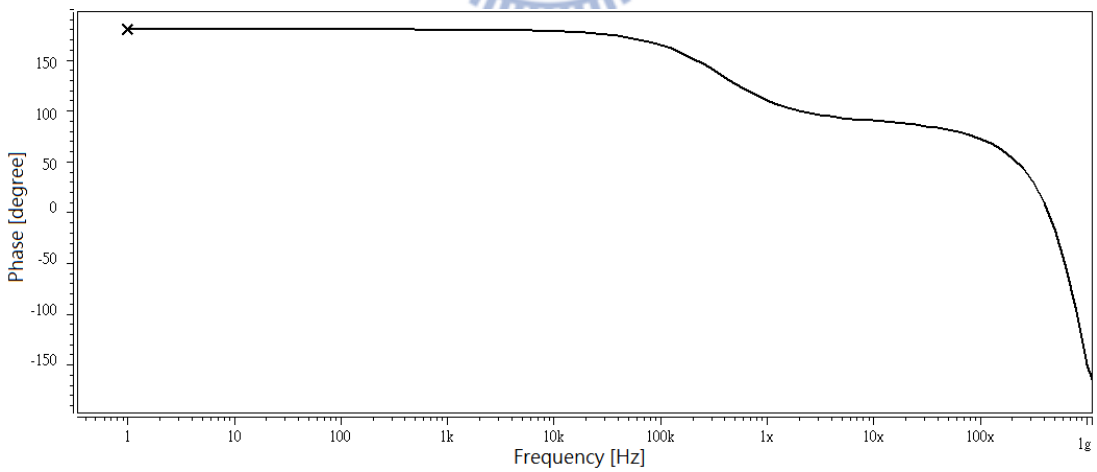


Figure 5.3 Phase response

Frequency and phase response of the transconductor is shown in figure 5.2 and 5.3 respectively. The simulation result shows the DC gain of transconductor is 35 dB and cutoff frequency at about 18 megahertz. The phase margin of transconductor is

87.3 degrees.

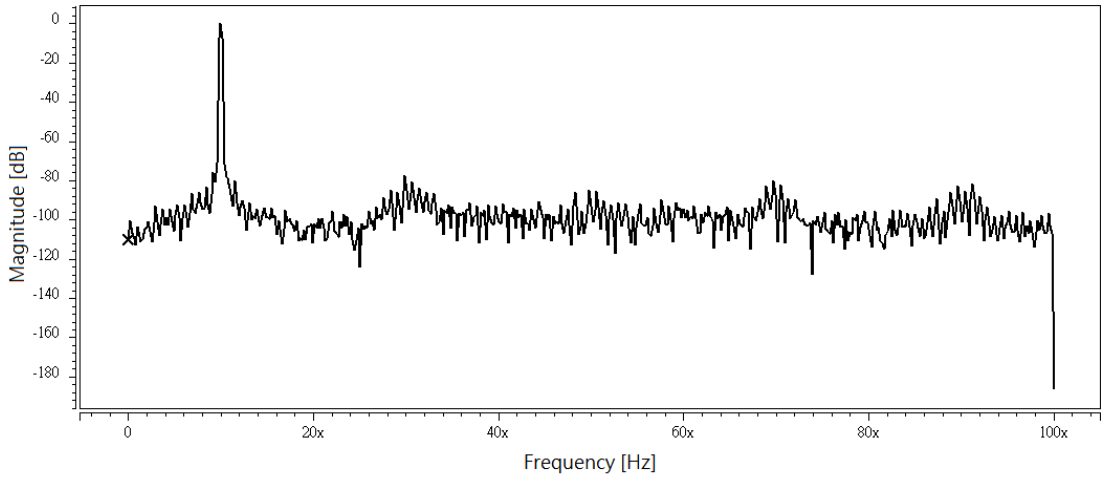


Figure 5.4 FFT Spectrum with input signal at 10MHz and 0.6v_{p-p}

The input pins of transconductor is injected with a 10 megahertz signal with amplitude of 0.6v peak to peak. Result shown the third order harmonic distortion is at -73 dB.

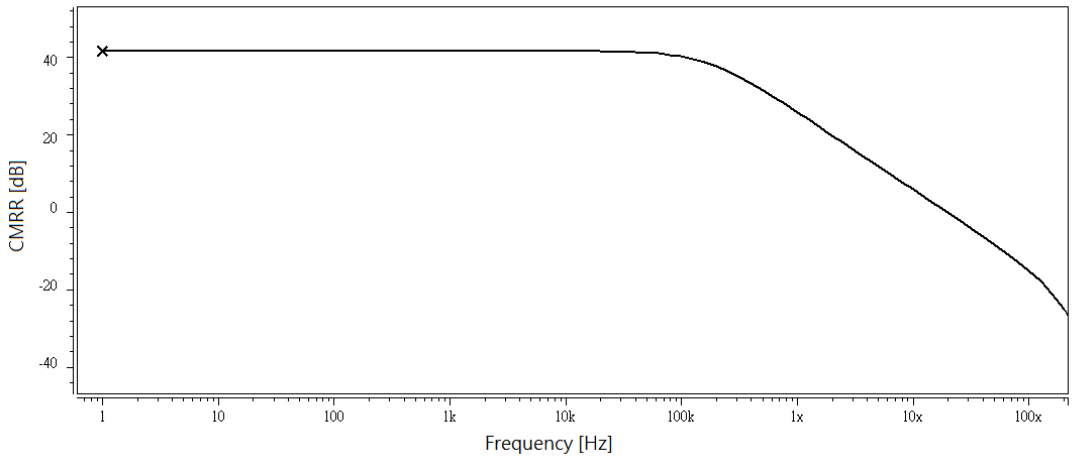


Figure 5.5 Common Mode Rejection Ratio

The common-mode rejection ratio exceeds 40 dB at DC but only has lower

value at higher frequency.

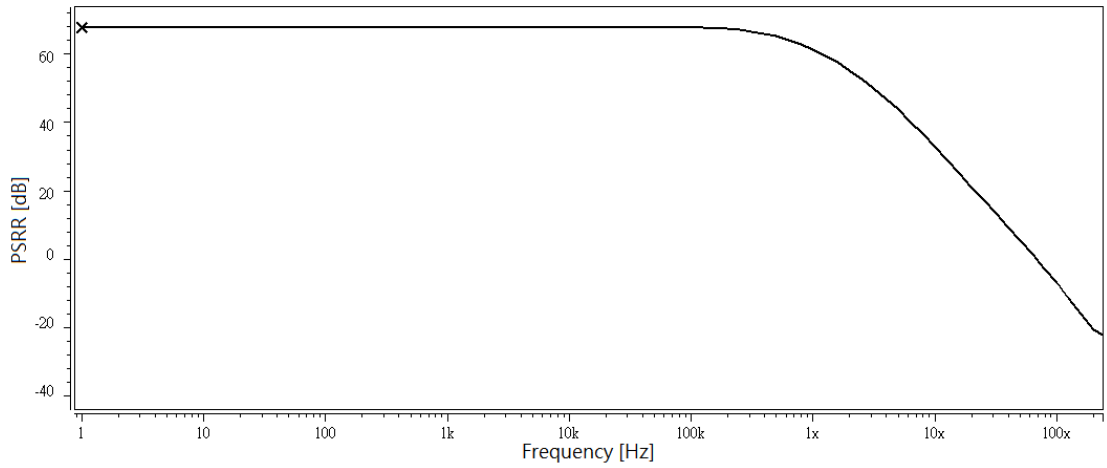


Figure 5.6 Power Supply Rejection Ratio

The circuit has PSRR value of 67.8 dB at DC and around 30dB at cutoff frequency.

5.2.2 Layout and measurements

Figure 5.7 and 5.8 show the layout scheme and micrograph of the chip. The die area is dominated by the pad number and occupies 0.5 x 0.395 mm^2 in final tape out.

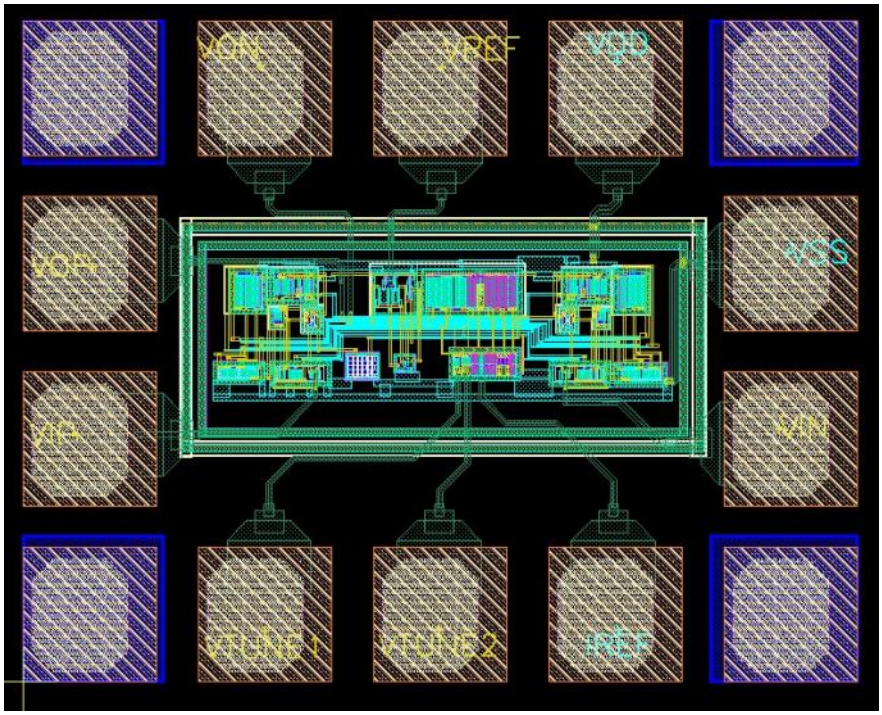


Figure 5.7 Layout scheme of the proposed transconductor

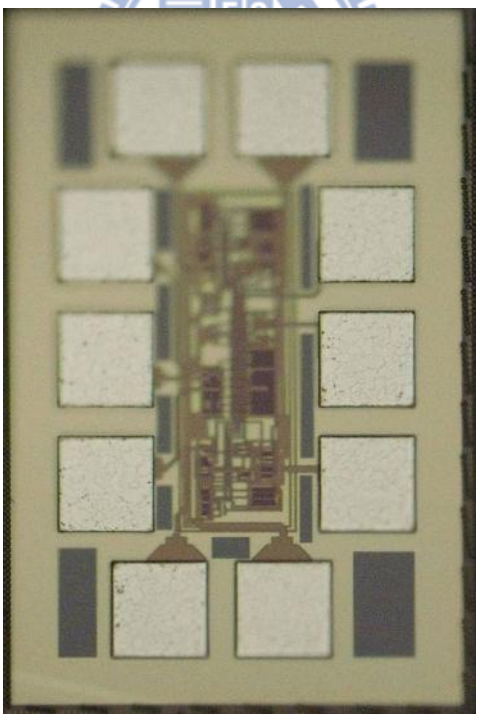


Figure 5.8 Die micrograph

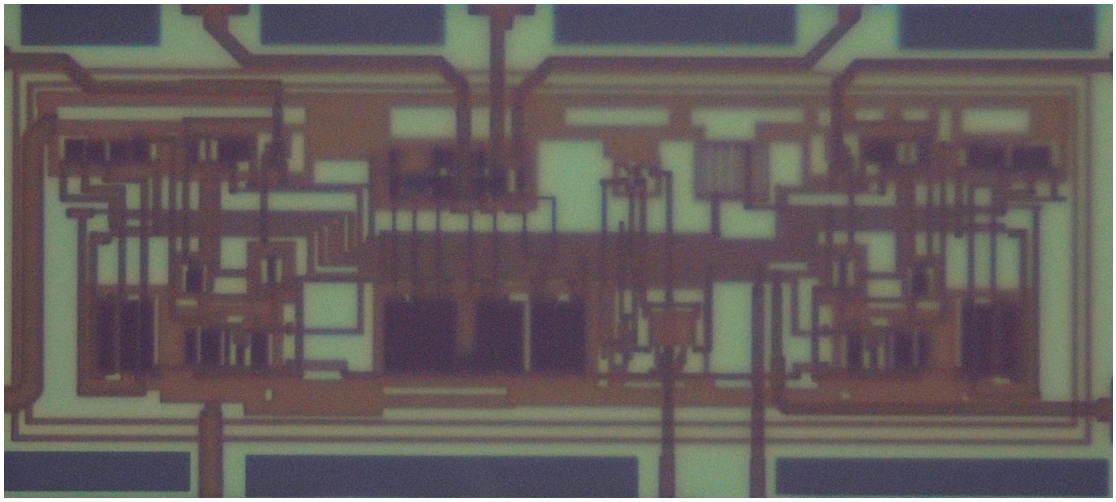


Figure 5.9 Die micrograph without pad

The following graphs figure 5.10 to 5.12 are the spectrum of transconductor at different frequencies.

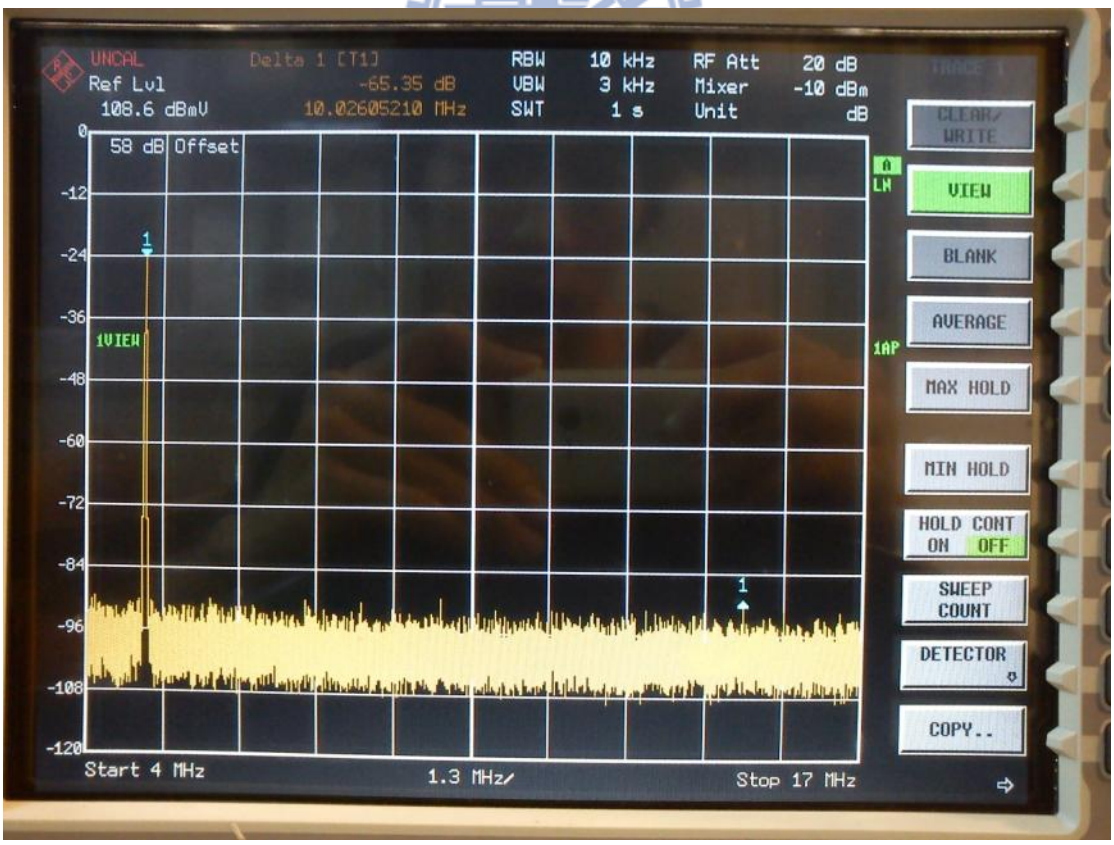


Figure 5.10 Spectrum of input signal at 5Mhz

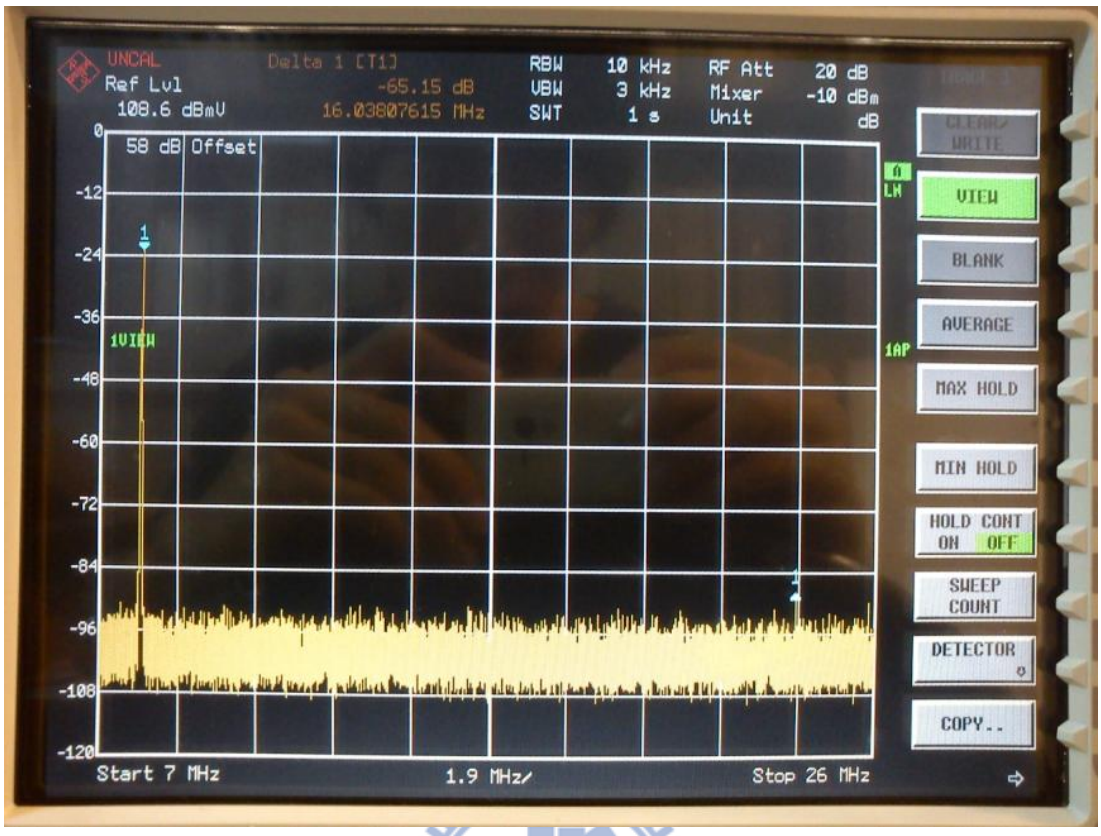


Figure 5.11 Spectrum of input signal at 8Mhz

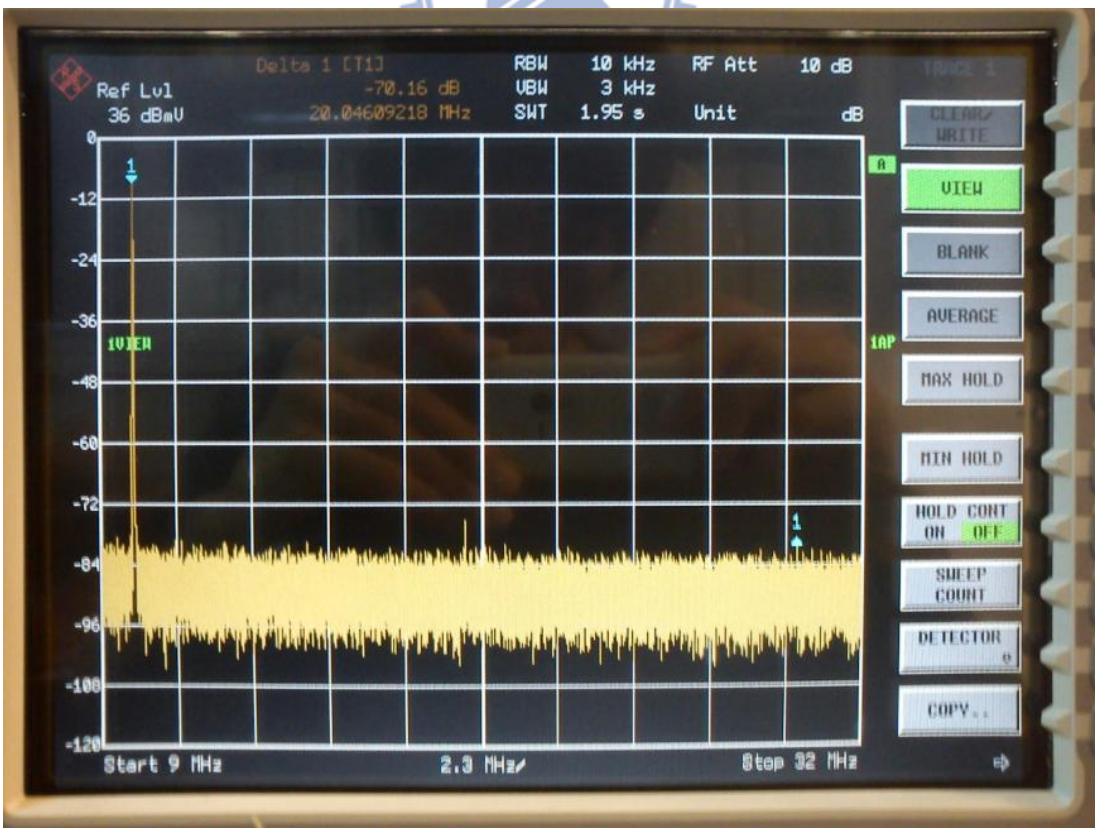


Figure 5.12 Spectrum of input signal at 10Mhz

5.2.3 Performance summary

TABLE 5.1 Specification of the transconductor

Parameter	Value
Power supply	1.8V
Power dissipation	3.689mW
DC gain	35dB
GM value	80μS - 180μS
HD3	-70.16dB
Vin (peak-peak)	0.6V
@Frequency	10MHz
CMRR	41.6dB
PSRR	67.8dB
Phase margin	88.3°

TABLE 5.2 Comparison chart

Referance	2003 [18]	2006 [29]	2009 [24]	This work
Technology	0.5-μm CMOS (Measurement)	0.18-μm CMOS (Simulation)	0.5-μm CMOS (Measurement)	0.18-μm CMOS (Measurement)
HD3	-43dB HD3 at 30MHz	-65dB HD3 at 1MHz	-67dB HD3 at 1MHz	-70.16dB HD3 at 10MHz
Input swing Range	0.9 Vpp	0.6 Vpp	1 Vpp	0.6 Vpp
Trans-Conductance	1065μs	20μs	165μs	180μs
Supply	3.3V	1.8V	1.8V	1.8V
Power consumption	10.7mW	145μW	0.36mW	3.689mW
FoM	80.49	76.68	85.11	89.75

In order to compare different transconductors, a definition of figure of merit (FoM) is made. It takes the transconductance value, linearity performance, speed, input swing range and power consumption into account and it is expressed as:

$$FoM = 10\log\left(\frac{G_m \times V_{id} \times IM3_{linear} \times f_0}{power}\right)$$

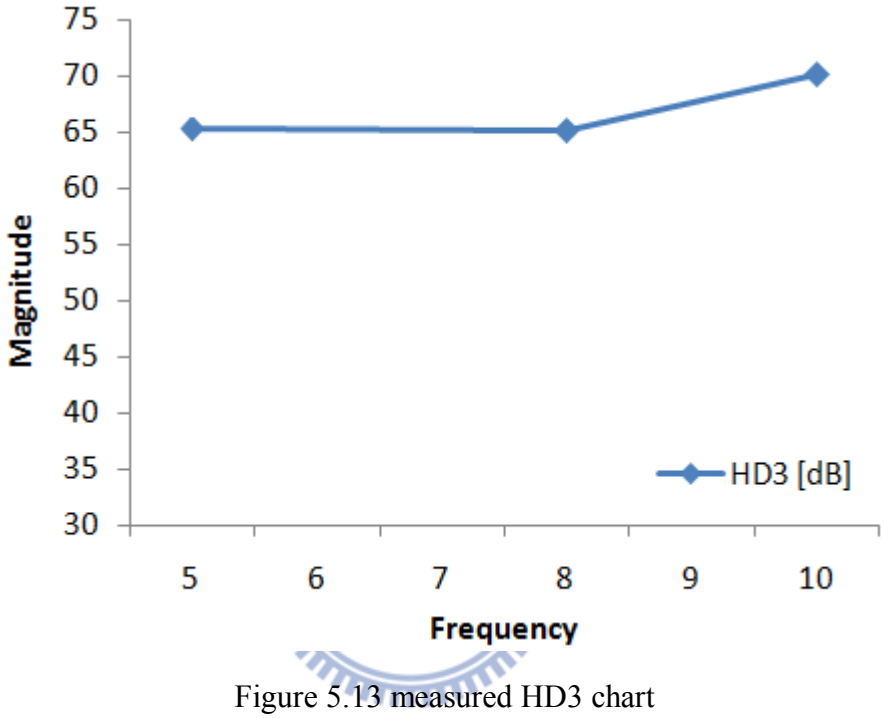


Figure 5.13 measured HD3 chart

5.3 Performance of Tunable Pseudo-Differential

Transconductor and fourth-order filter

The simulations ran for OTA in last section will also be shown in this section. In addition, the transconductor is used as a building block and constructed a fourth-order filter. The spectrum and transfer function of filter will also be shown in this section.

5.3.1 Simulations

The transconductance values with different tuning voltages are shown in figure 5.14. Vertical axis represents the transconductance value and horizontal axis shows the input range.

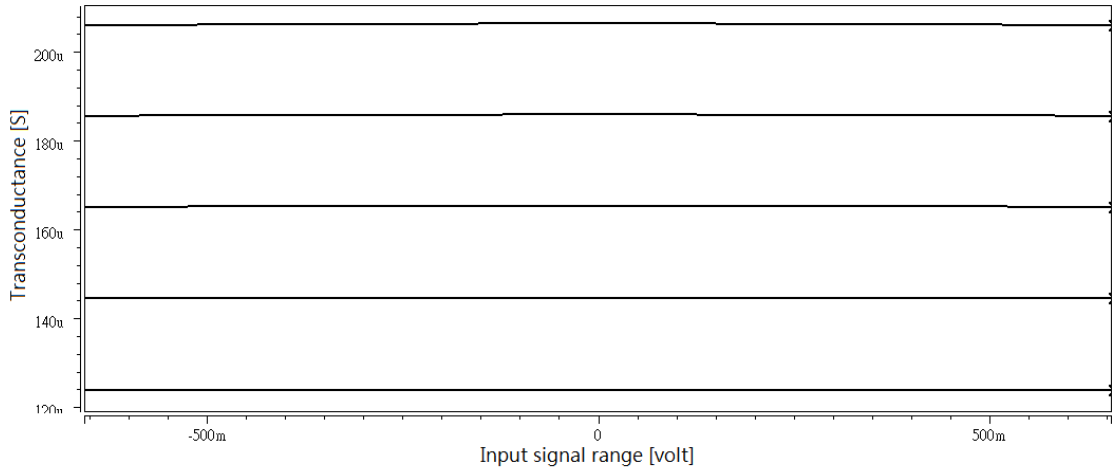


Figure 5.14 Transconductance value with different tuning voltage

As figure 5.14 above showed, the Gm tuning range is between 124μ to 206μA/V, the linear input range is 0.6Vpeak-peak, HD3 between this tuning range are all below -76.4dB. Gm tuning ability makes this design more flexible in multiple applications, many effects from fabrication mismatch are able to be tuned back to the values designed be the tuning voltage from outside the circuit, which makes the stability of this design better.

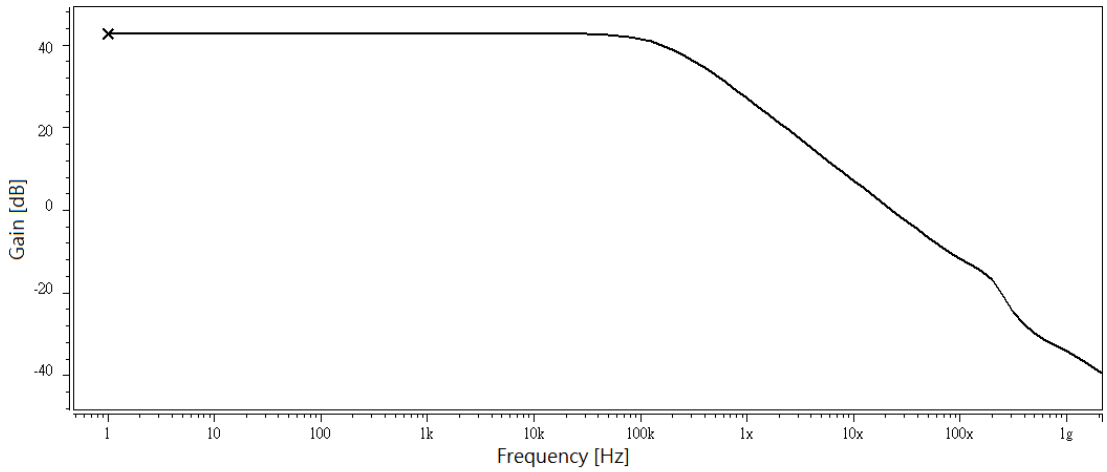


Figure 5.15 Frequency response

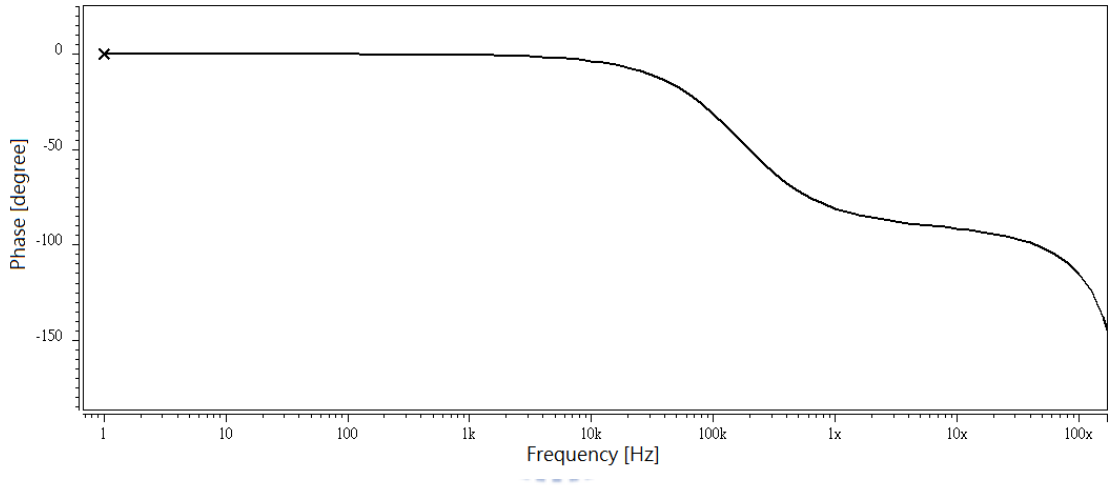


Figure 5.16 Phase response

Frequency and phase response of the transconductor is shown in figure 5.15 and 5.16 respectively. The simulation result shows the DC gain of transconductor is 42.8 dB and cutoff frequency at about 18 megahertz. In order to be used as a block of Gm-C filter, Phase Margin should be made as close to 90 degrees as possible to reduce group delay. In the simulations, phase margin is about 85 degrees which is enough.

Since the circuit uses pseudo-differential structure, it suffers from altering current with corners. But in this design, the gains of all corners are above 30dB which is enough for transconductors, and bandwidth are all above 10Mhz as designed.

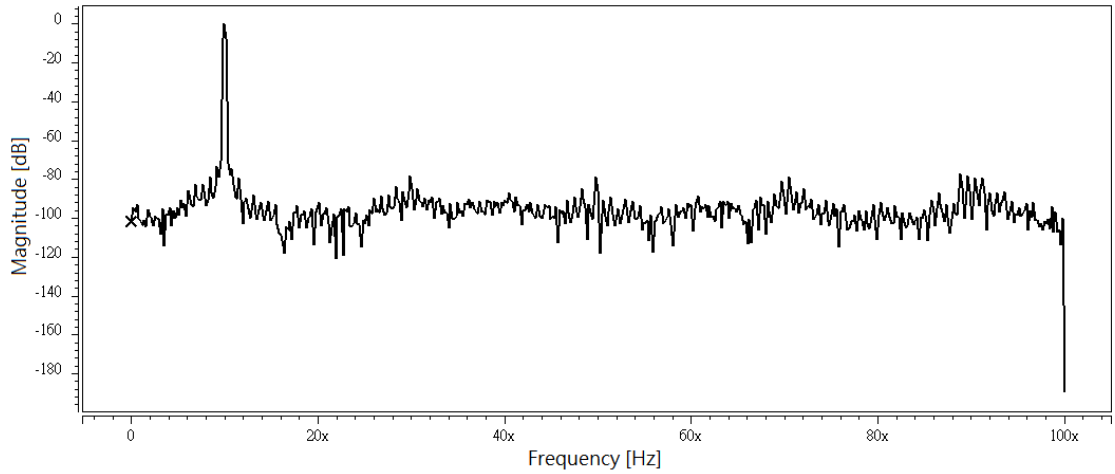


Figure 5.17 FFT Spectrum with input signal at 10MHz and 0.6v_{p-p}

The input pins of transconductor are injected with a 10 megahertz signal with amplitude of 0.6v peak to peak. Result shown the third order harmonic distortion is at -77 dB.

Other minor data such as Common Mode Rejection Ratio (CMRR) and Power Supply Rejection Ratio are simulated.

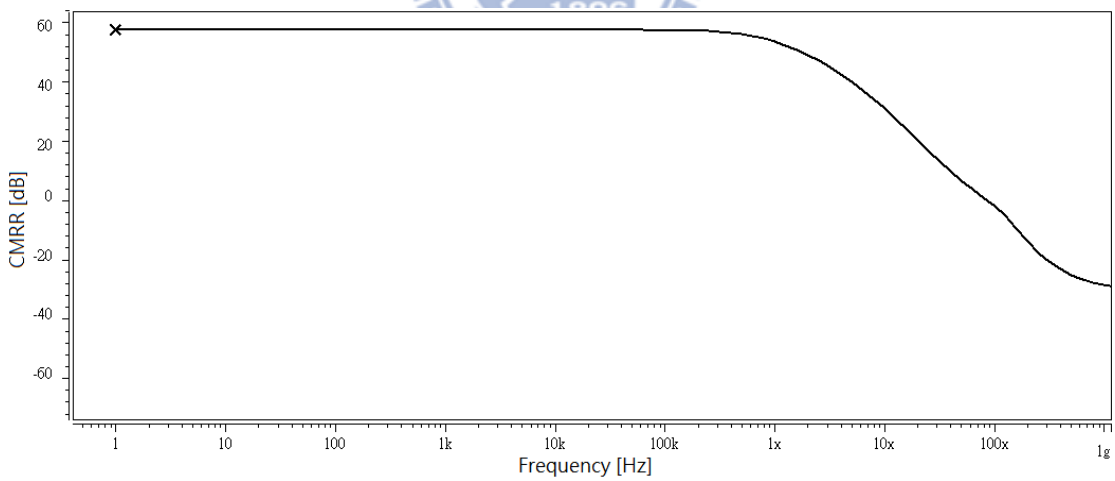


Figure 5.18 Common Mode Rejection Ratio

The common-mode rejection ratio is 65.1 dB at DC and around 30 dB at cutoff frequency.

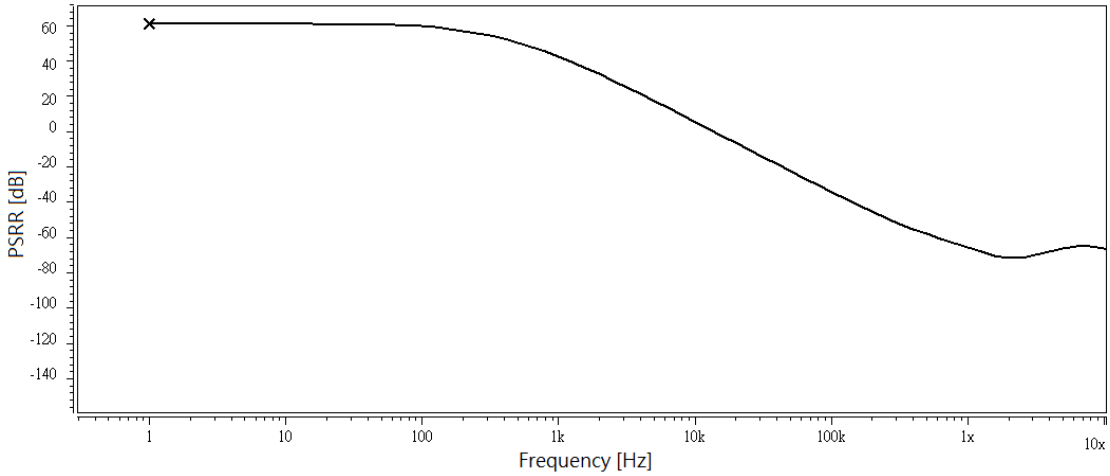


Figure 5.19 Power Supply Rejection Ratio

The circuit has PSRR value of 60.7 dB at DC but lower at higher frequency. However, the power supply noise is mostly at low frequency.

The simulation result of the fourth-order Chebyshev lowpass filter is shown in figure 5.20 and 5.21.

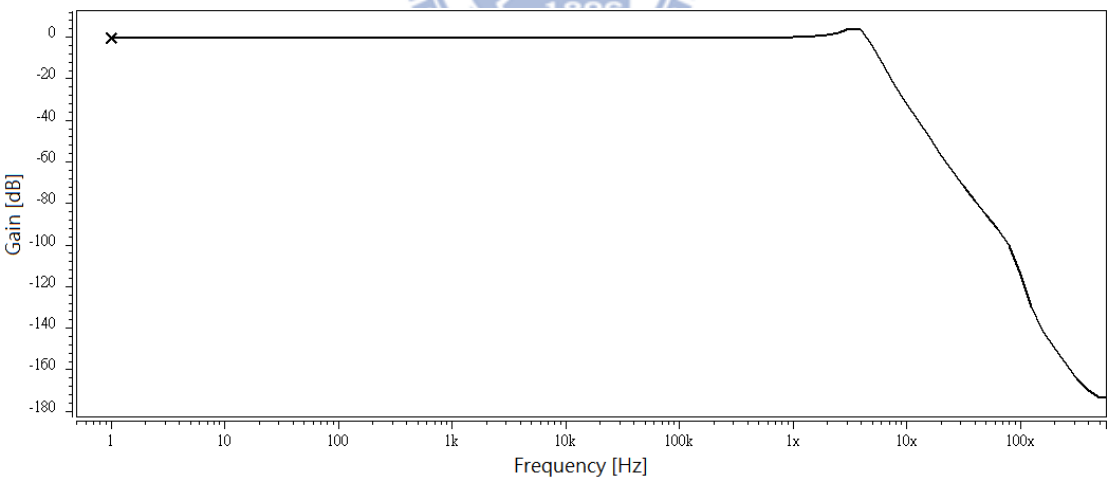


Figure 5.20 Frequency response of filter

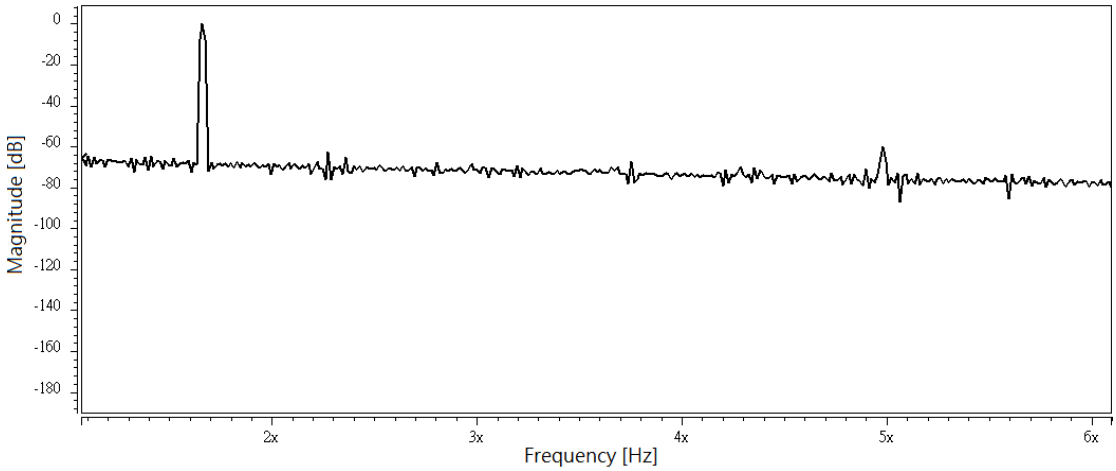


Figure 5.21 FFT Spectrum of Filter with 1.66Mhz input signal

Figures 5.20 and 5.21 are the simulation results of filter. In contrast to the results of pre-sim, the cutoff frequency of post-sim results is a bit lower. This is due to the parasitic capacitor formed between layers caused the increment of equivalent total capacitance which also made pole position moved to lower frequency. Error from both parasitic capacitance and corner variation could be compensated by G_m tuning.

To avoid distortion signal getting filtered at the output, 1.66 Mhz input signal is used so distortion signal will be inside the passband 5Mhz.

5.3.2 Layout and measurements

Figure 5.22 to 5.25 show the layout scheme and micrograph of the chip. The die area is dominated by the pad number and occupies 0.29 x 0.395 mm^2 in final tape out. The filter costs 0.502 x 0.612 mm^2 of die area.

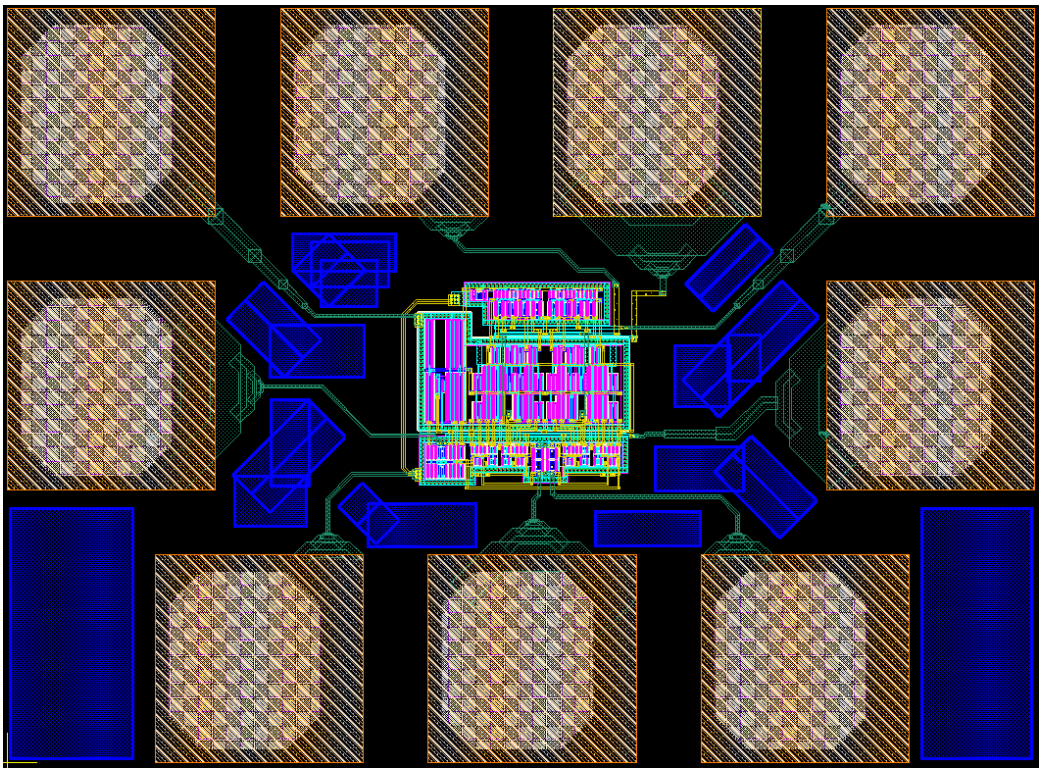


Figure 5.22 Layout scheme of the proposed transconductor

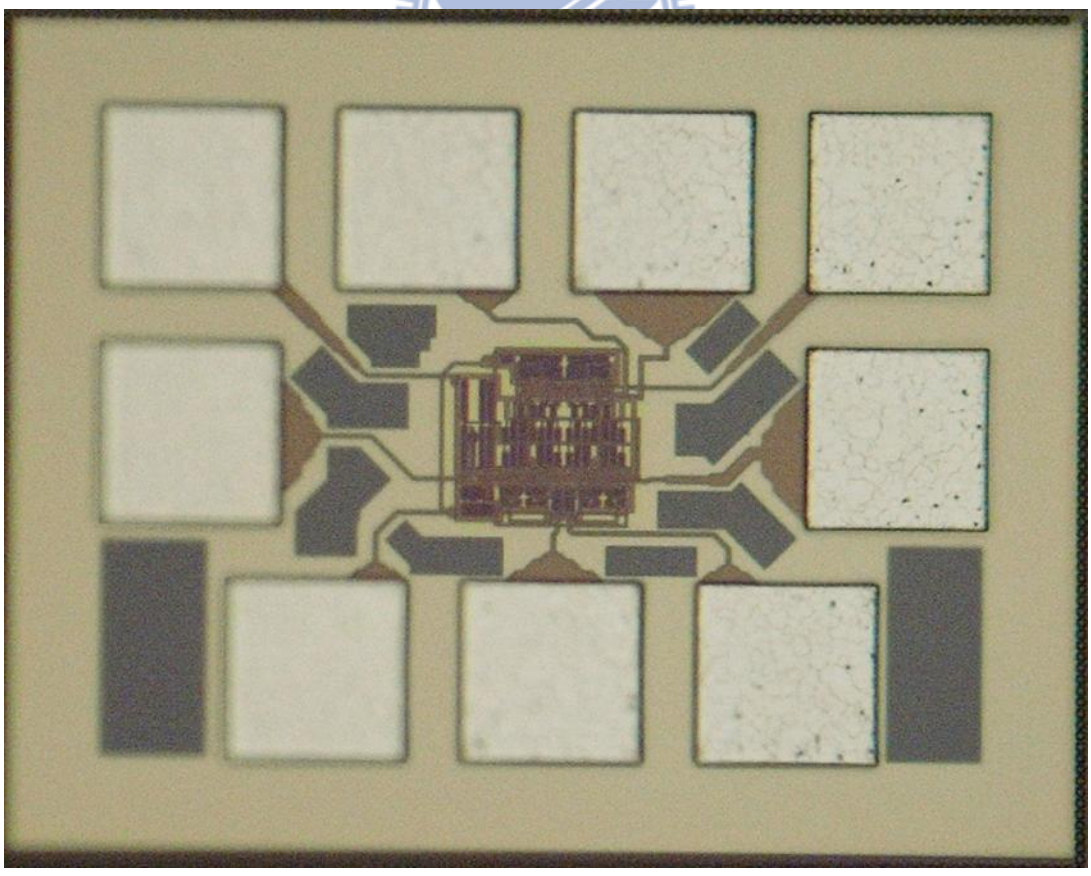


Figure 5.23 Die micrograph

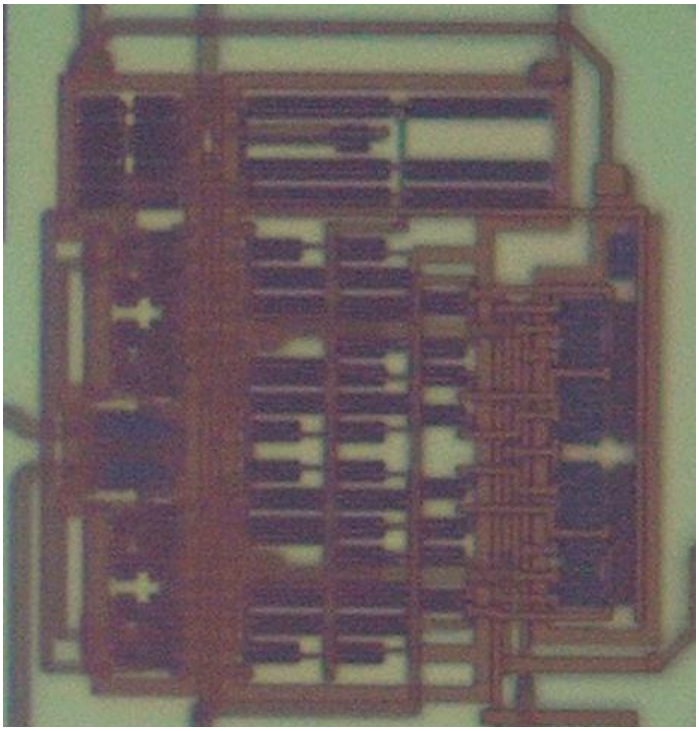


Figure 5.24 Die micrograph without pad

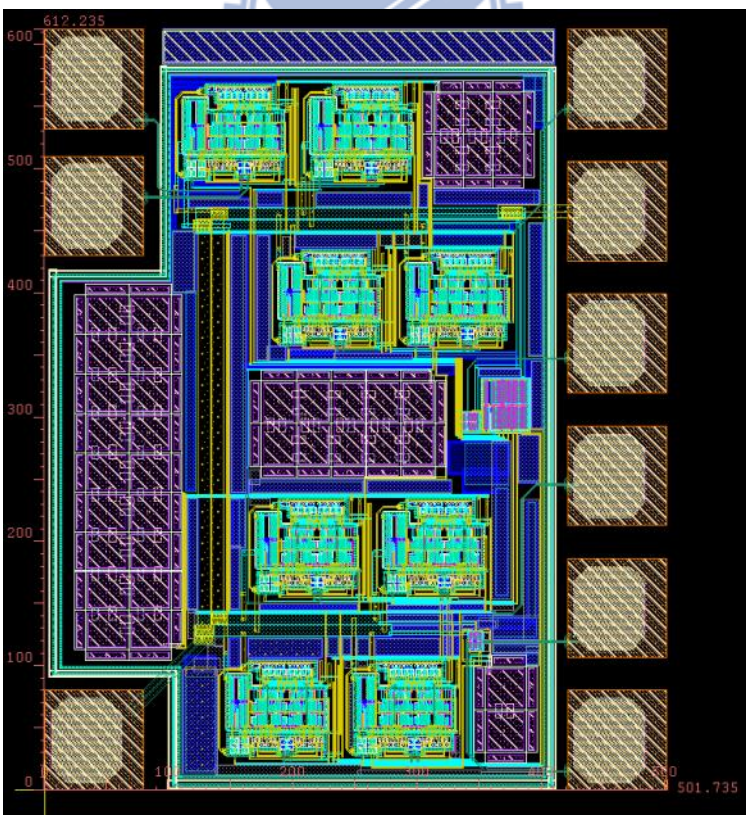


Figure 5.25 Layout scheme of filter

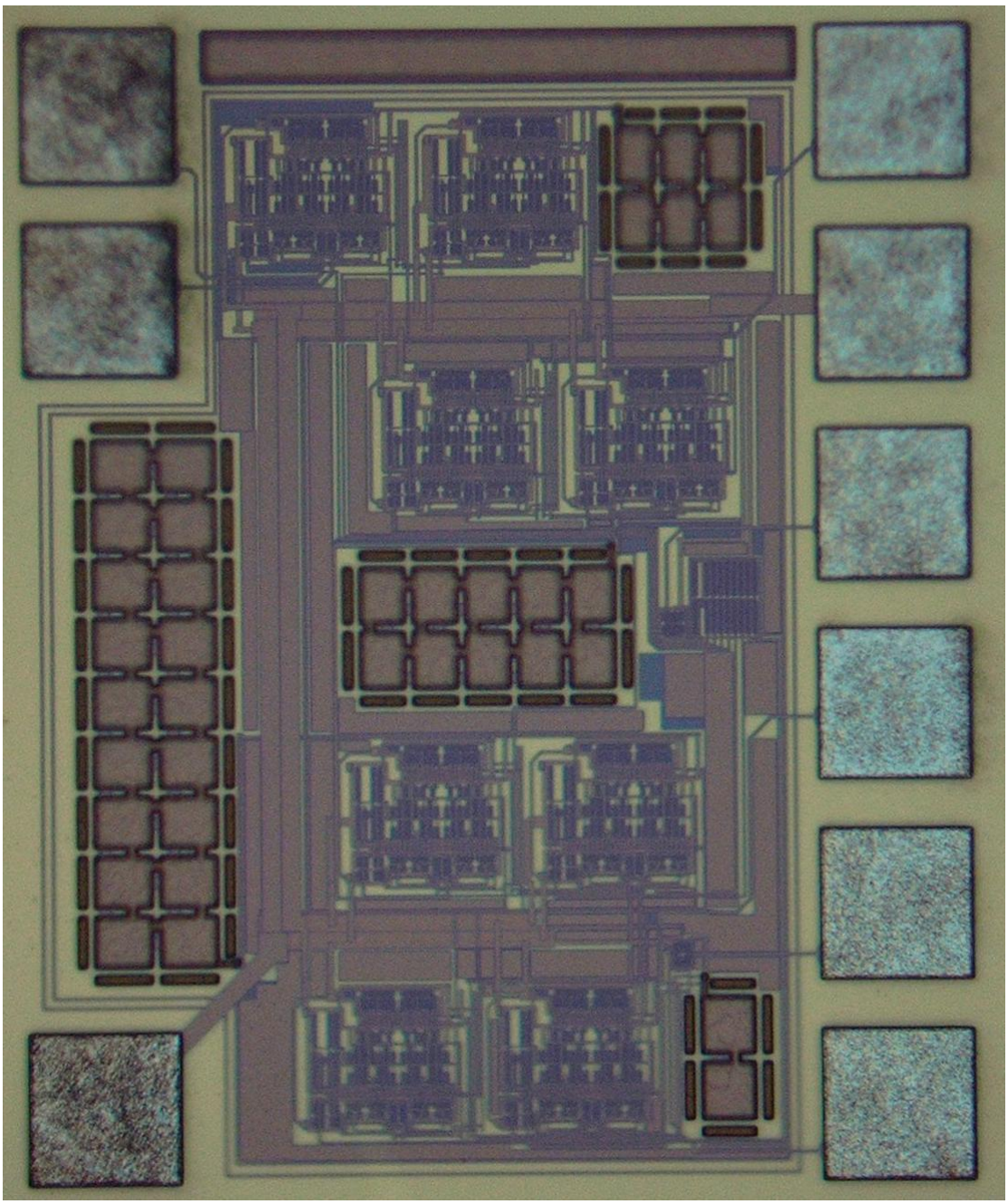


Figure 5.26 Die micrograph of filter

The following figures 5.27 to 5.31 are the spectrum of transconductor at different frequencies.

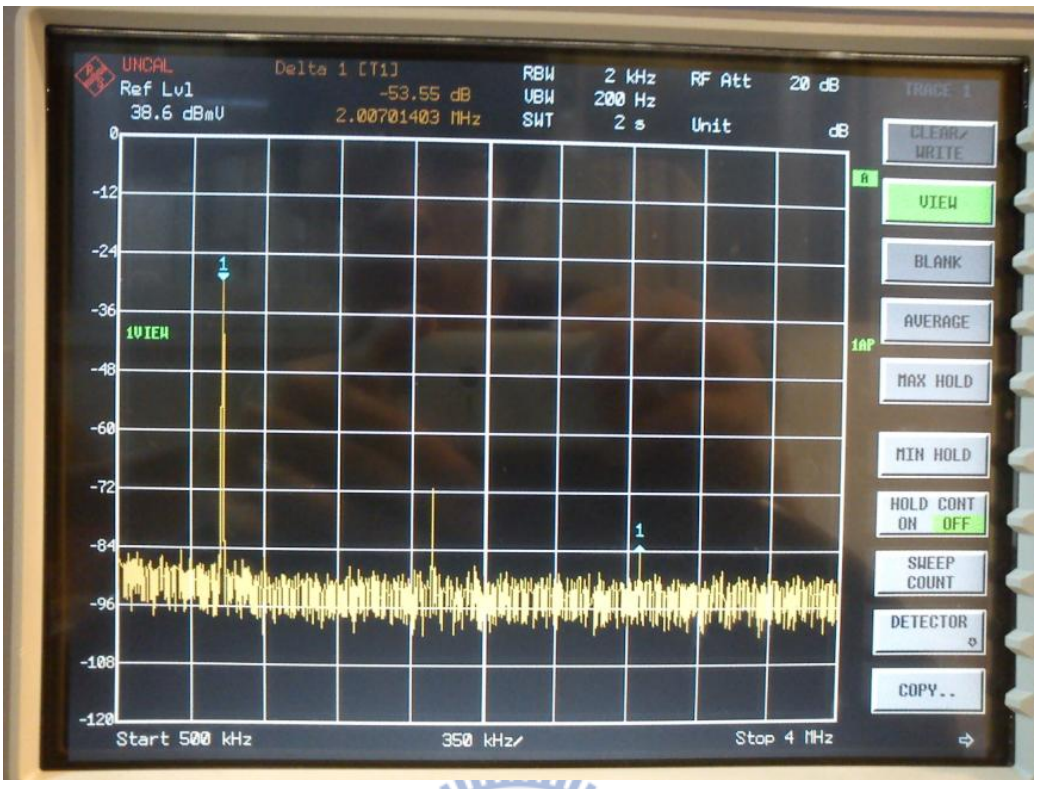


Figure 5.27 Spectrum of input signal at 1Mhz

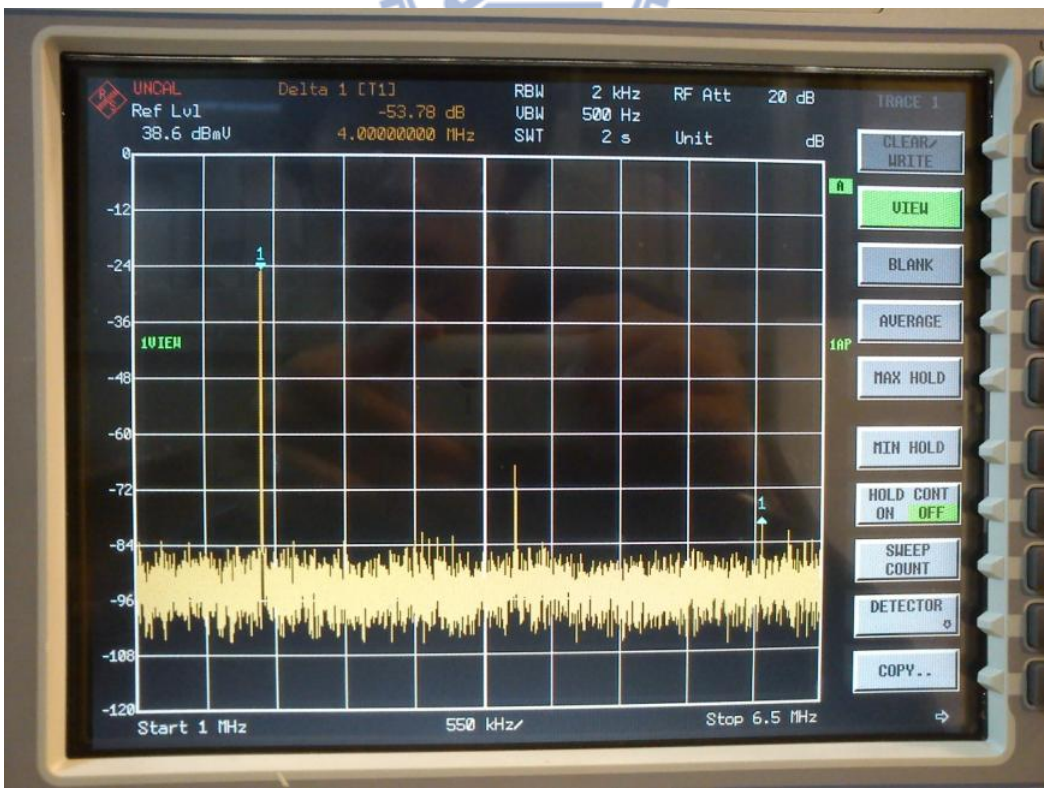


Figure 5.28 Spectrum of input signal at 2Mhz

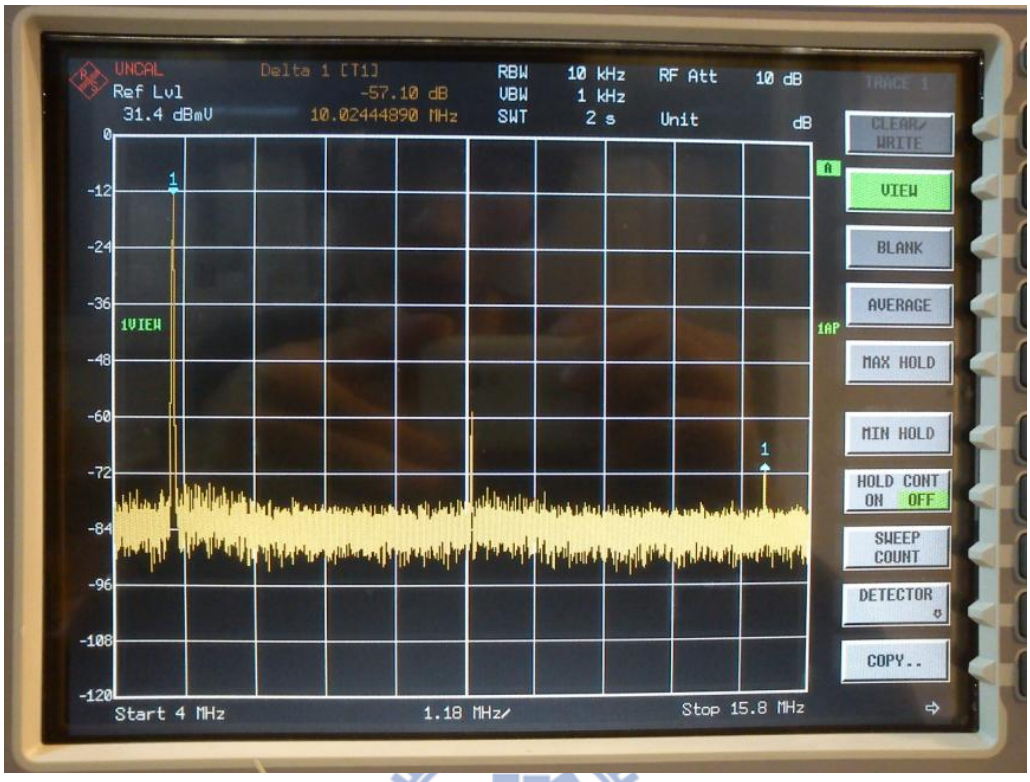


Figure 5.29 Spectrum of input signal at 5Mhz

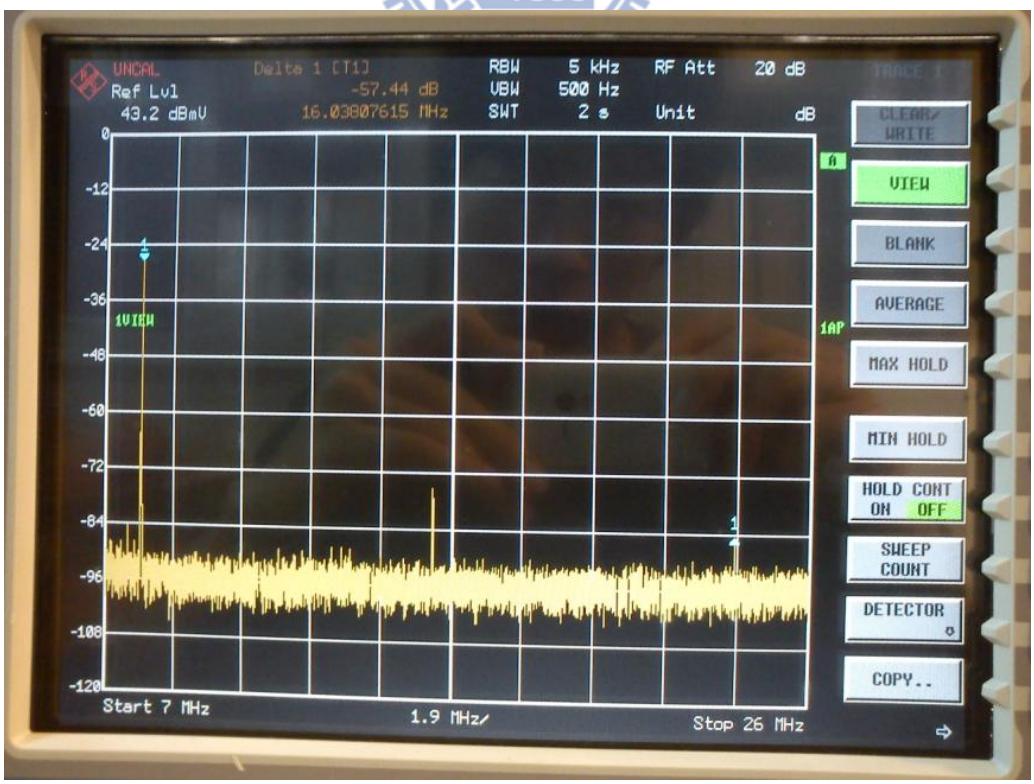


Figure 5.30 Spectrum of input signal at 8Mhz

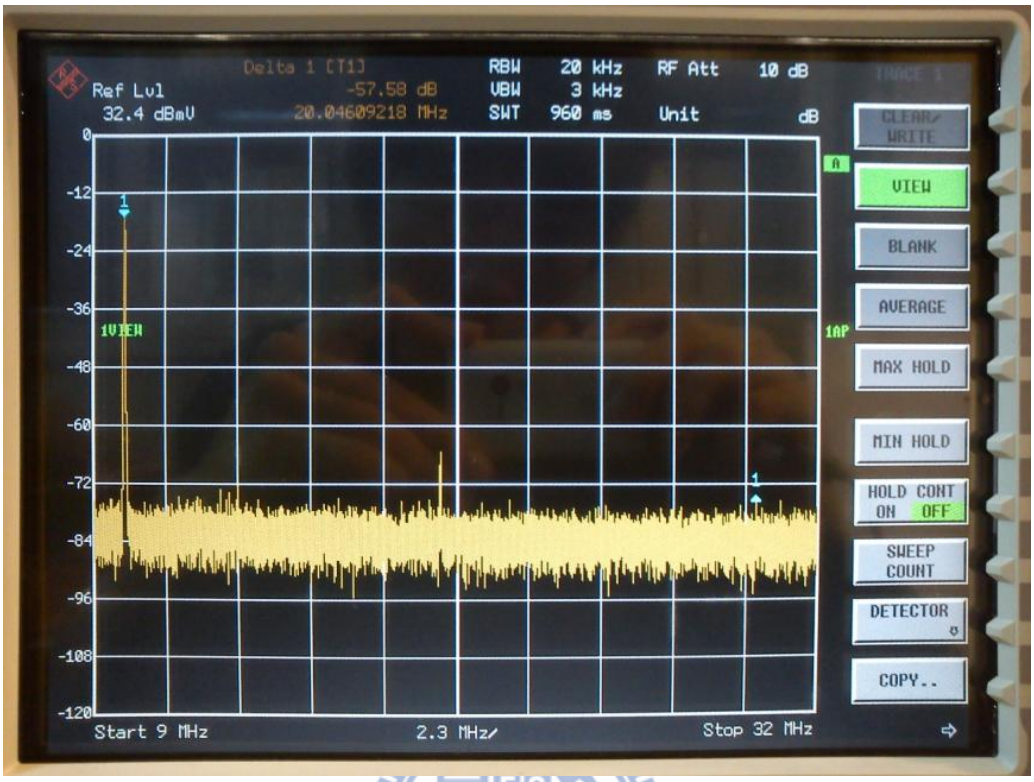


Figure 5.31 Spectrum of input signal at 10Mhz

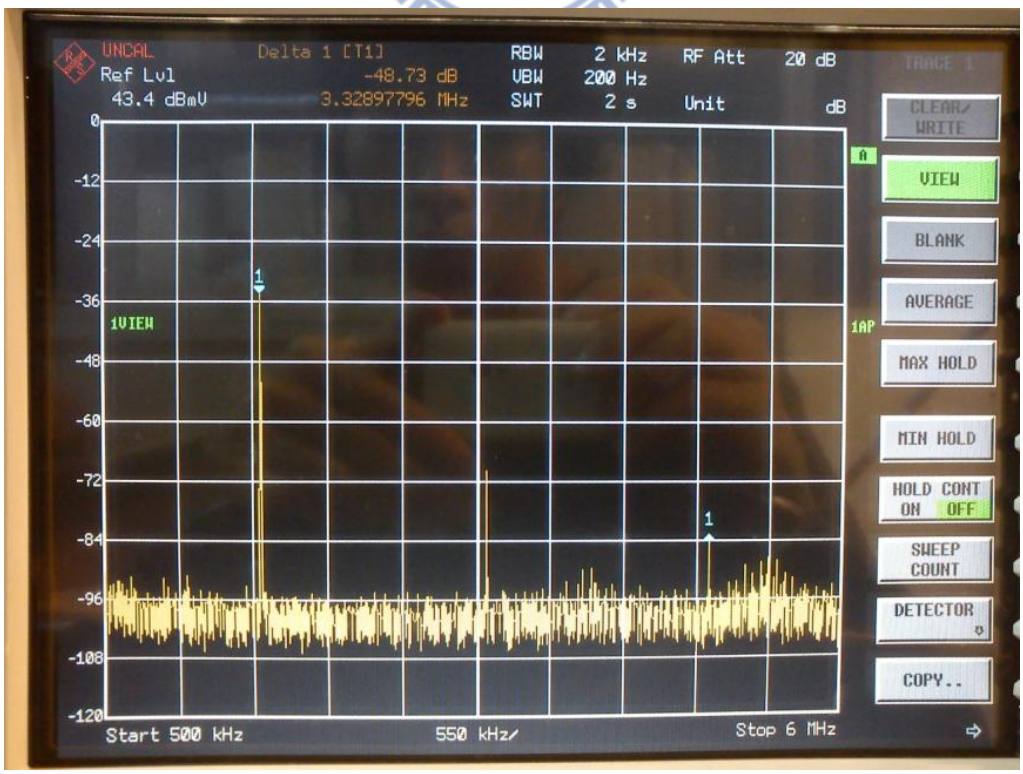


Figure 5.32 Filter Spectrum of input signal at 1.66Mhz

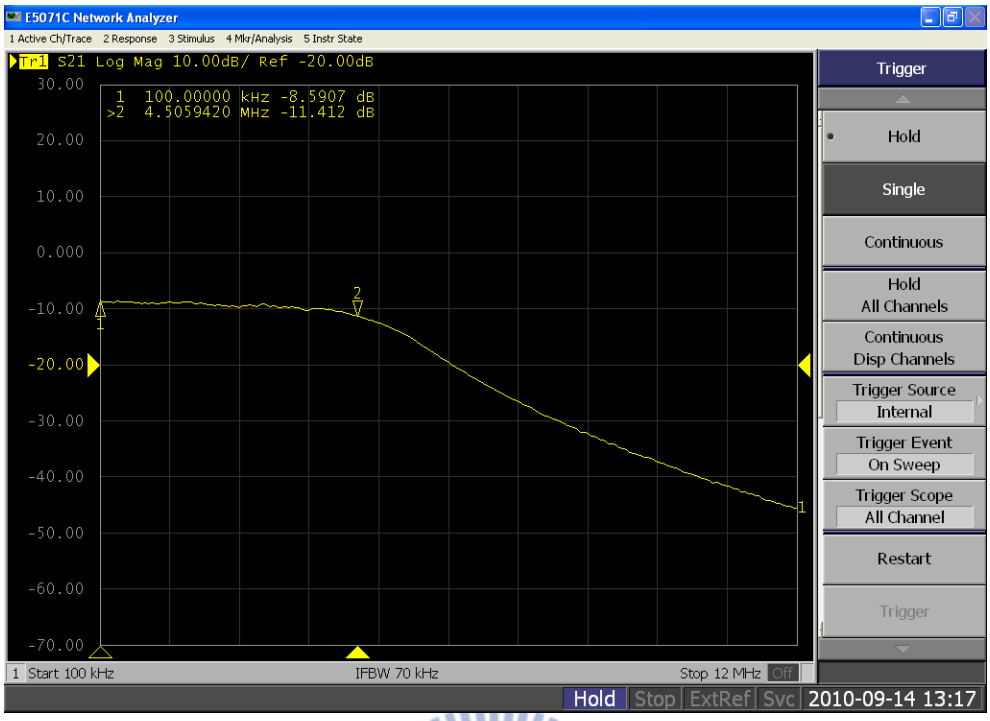


Figure 5.33 Filter Frequency response (4.5Mhz)

Figure 5.34 Filter Frequency response (5Mhz)

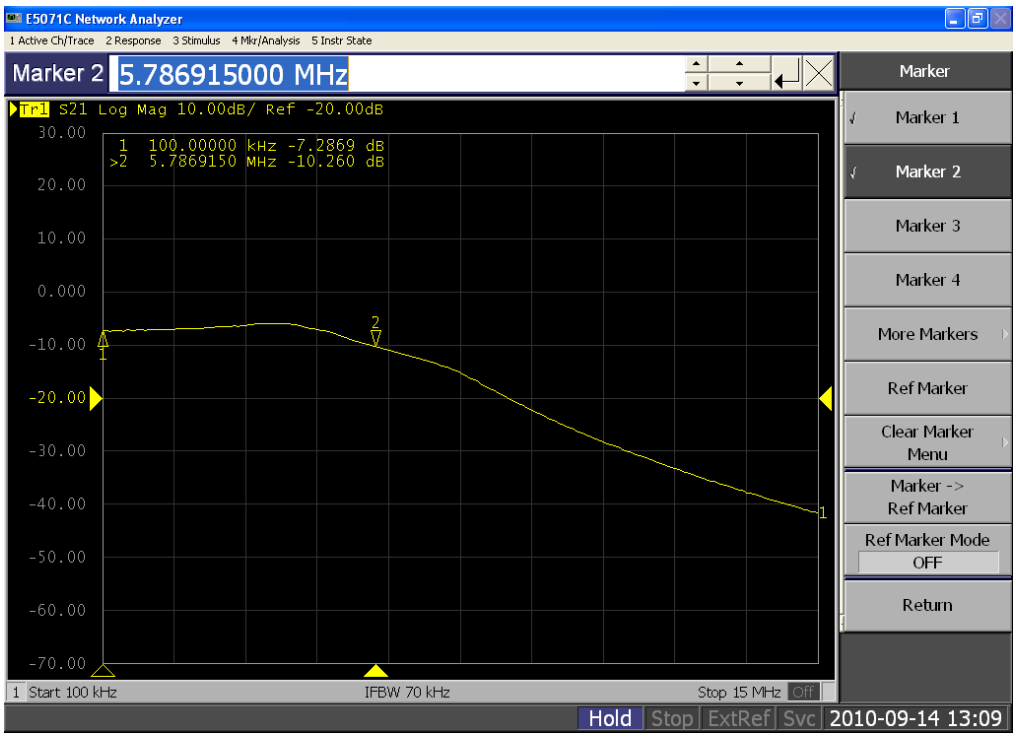


Figure 5.35 Filter Frequency response (5.8Mhz)

Figure 5.27 to 5.31 are spectrums of transconductor shown a significant 2nd-order harmonic tone which is generated from mismatch due to fabrication. This could be improved by layout techniques such as making current mirror transistors separated. Figure 5.33 to 5.35 show filter passband at different frequencies.

5.3.3 Performance summary

TABLE 5.3 Specification of the transconductor

Parameter	Value
Power supply	1.8V
Power dissipation	0.762mW
DC gain	42.9dB
GM value	124μS - 206μS
HD3	-57.58dB
Vin (peak-peak)	0.6V
@Frequency	10MHz
CMRR	57.5dB
PSRR	60.9dB
Phase margin	85.4°

TABLE 5.4 Comparison chart

Referance	2003 [18]	2006 [29]	2009 [24]	This work
Technology	0.5-μm CMOS (Measurement)	0.18-μm CMOS (Simulation)	0.5-μm CMOS (Measurement)	0.18-μm CMOS (Measurement)
HD3	-43dB HD3 at 30MHz	-65dB HD3 at 1MHz	-67dB HD3 at 1MHz	-57.58dB HD3 at 10MHz
Input swing Range	0.9 Vpp	0.6 Vpp	1 Vpp	0.6 Vpp
Trans-Conductance	1065μs	20μs	165μs	206μs
Supply	3.3V	1.8V	1.8V	1.8V
Power consumption	10.7mW	145μW	0.36mW	0.762mW
FoM	80.49	76.68	85.11	85.89

$$FoM = 10\log\left(\frac{G_m \times V_{id} \times IM3_{linear} \times f_0}{power}\right)$$

TABLE 5.5 Specification of the filter

Parameter	Value
Power supply	1.8V
Power dissipation	8.351 mW
Order	4^{th} Chebyshev
HD3	-48.73dB
Vin (peak-peak)	0.6V
@Frequency	5MHz
Chip size	$0.502\times0.612mm^2$

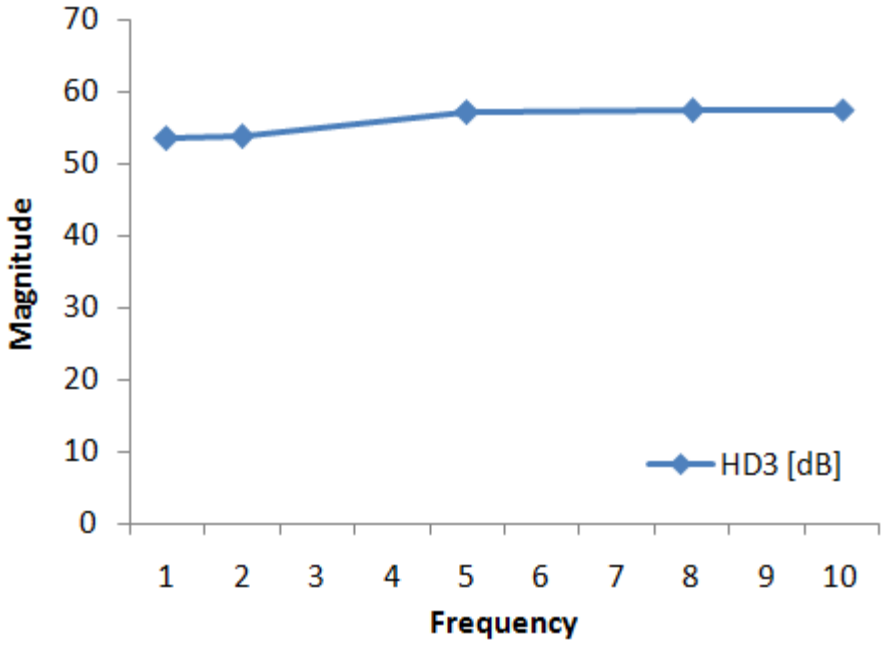


Figure 5.36 measured OTA HD3 chart

Chapter 6

Conclusions

6.1 Conclusion

Integrated analog filters play an important role in present communication systems and system-on-chip solutions. The most popular technique for realizing such analog filter is continuous-time filter, which can process the high speed signal continuously in time domain. The performance of a G_m-C filter is highly dependent on the OTA building block, including the linearity and speed since it is formed only by OTAs and capacitors. Thus, most of the papers and researches are focus on to the linearity of the voltage-to-current conversion to improve the features of the filter.

Two highly linear operational transconductance amplifier and a highly linear G_m-C filter is proposed. The importance of linearity in the OTA of the G_m-C filter is described. One design is made by using two FVF cell and a feedback loop to cancel non-ideal small signal resistance and a tunable current mirror. The other new design makes use of the conventional pseudo-differential structure, proposes a modified FVF cell to improve linearity, and adds tuning functionality while maintaining advantages of fast operating speed and wide tuning range from pseudo-differential structure.

These proposed OTA circuits achieved over -60dB HD3 distortion. The filter has -50dB distortion consuming 9mW. Its high linearity and wide tuning range make it suitable for more applications.

6.2 Future Works

With the advance of technology, more and more applications of integrated circuits are used for portable device. A main difficulty in portable electronics is it has limited energy supply which requires lower power consumption and lower supply voltage to make a product economic. Thus building circuits with lower voltage supply is a worthy of a try. In addition, the idea of lowering equivalent small signal resistance with two flipped-voltage follower might also be able to be applied to pseudo-differential structure. There are even more possibilities waiting to be explored.

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