國立交通大學

電信工程研究所

碩士論文

16奈米場效應電晶體特性擾動抑制暨 TFT-LCD驅動電路設計優化之研究

Suppression of 16-nm MOSFET Characteristic Fluctuation and Design Optimization of TFT-LCD ASG Driver Circuit

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摘要

本論文主要分為兩部份，這兩部份皆與類比暨前瞻通訊應用上有相關性，其中甲部分為半導體 16 奈米場效應電晶體特性擾動抑制分析，乙部分為 TFT-LCD 驅動電路設計優化之研究。分述如下:

甲部分:

隨著手機應用越來越廣泛，使得頻率區段使用變的極為競爭且激烈，然而高頻段區域尚未有使用執照的限定與規範，因此為了提升動態特性，就加速了半導體元件微縮在類比電路上的應用。

但是伴隨著金屬氧化半導體場效應電晶體(MOSFET)元件通道尺寸依循摩爾定律被迅速缩小，元件特性變異成為主要挑戰且對電路設計上極為重要。而隨機離散摻雜所導致的擾動(RDF)是這些特性變異的主要來源。透過檢驗元件變異所造成類比電路上的特性變異便成極迫切的議題，在16奈米技術上去壓抑隨機離散摻雜所造成的特性擾動是個熱門的研究方向。

在本研究中，我們首次探討了兩種不同的雙邊非對稱金屬閘極元件來壓抑由16奈米金屬氧化半導體場效應電晶體 (MOSFET)元件隨機摻雜效應(RDF)所導致在元件直流(DC)特性擾動，例如:臨界電壓(V_{th})、導通電流(I_{on})、夾止電流(I_{off})等等。然而同樣的壓抑現象卻不能實現在非對稱雙金屬閘極(DMG)元件的交流(AC)特性上，例如電容(C_g)。這是因為空乏區电容是被通道區域的摻雜分佈和有效的氧化層厚度所影響。為了有效壓抑離散隨機摻雜所導致的交流特性擾動，我們進一步探討16奈米隨機摻雜分佈的元件的非對稱現象，主要分為靠近源極端摻雜和汲極端的摻雜。在通道區域中靠近源極端離散摻

雜和靠近汲極端離散摻雜導致不同閘極電容和動態特性的擾動。基於所觀察到的非對稱特性，我們使用此橫向不對稱性通道摻雜分佈的方法來壓抑在元件和電路由隨機摻雜所導致的擾動。本研究結果發現，在靠近汲極端離散摻雜的元件和一般所使用的元件比較中，臨界電壓擾動(σV_{th})、導通電流擾動(σI_{on})、電導擾動 (σg_m)、元件阻抗擾動(σr_o)、閘極電容擾動 (σC_g)、電路增益擾動、3dB 頻寬擾動以及单位增益擾動，同時分別降低33.4%, 32.8%, 11.9%, 80.6%, 68.8%, 31.2%, 37.6% 和 47%。所以這樣的橫向不對稱通道摻雜可以有效使用來設計壓抑電晶體的特性擾動。

乙部分:

近年來，隨著面板產業的蓬勃發展，非晶矽薄膜電晶體液晶顯示器(a-Si:H TFT-LCD)已被廣泛應用於手機之顯示系統。而以非晶矽薄膜電晶體為元件的閘極驅動電路（TFT-ASG circuit），在薄膜電晶體液體顯示器（TFT-LCD）面板的製造上已扮演重要的角色。但是，設計薄膜液晶顯示器面板驅動電路的工作是相當複雜以及費時，工程師必須不斷地調整電晶體參數以滿足節能產品之需求，像是:降低充放電的時間、降低漣漪電壓以及降低消耗等顯示規格。

在這篇論文中，我們使用兩個不同的電路架構來改善動態特性並且對這些動態特性進行電晶體尺寸的最佳化。所使用的最佳化技巧主要是在統合性的最佳化架構下，以模擬為基礎並結合基因演算法與電路模擬器的演化式方法。其中第一個含有 14 顆 TFT 的電路除了設計上要求上升時間及下降時間小於 1.5 微秒，漣漪電壓小於 3 伏特之外，也同時考慮電路面積的最小化；此電路主要用於大型面顯示器。第二個含有 8 顆 TFT 及 2 顆電容的電路不僅設計上要求上升時間、下降時間以及漣漪電壓小於 2 微秒和 2 伏特外，還多增加了功率小於 2 毫瓦特的要求；此電路主要用於手機面板。經過最佳化的結果，所有動態特性和功率消耗全部符合預期所設定的限制。並且在含有 14 顆 TFT 電路的總元件尺寸上有 35%的降低，而經過敏感度分析測試之後，更發現這些最佳參數具有優異的穩定性。

接著使用標準的 TFT 4 微米的製程技術，將這些最佳化過後的電路一一實做出來進行動態特性量測與分析，14 顆 TFT 電路在量測分析中上升和下降時間均維持在要求的規格中，並且在漣漪電壓上有 71%的改善，模擬與實際量測誤差值更是相符合，而在 8 顆 TFT 電路上，上升和下降時間也均符合規格

要求，漣漪電壓更是有 49%上之改善，另外值得注意的是與原始對照組的電路面積比較，最佳過後的電路面積更是微縮了 36%之多。

透過統合性的最佳化架構,以模擬為基礎並結合基因演算法與電路模擬器的演化式方法，自動調整電晶體參數來最佳化面板閘極驅動電路的設計，這將對面板市場和閘極電路設計獲益良多。

總而言之,不管是甲部分還是乙部分,本論文的研究對目前台灣兩兆雙星產業:半導體和面板帶來技術諸多優勢以及經濟利潤許多遠景。

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Abstract (English)

This thesis consists of two research topics: the suppression of 16-nm MOSFET Characteristic fluctuation and design optimization of TFT-LCD amorphous silicon gate (ASG) driver circuit. The abstract of each study is organized as follows.

PART A :

As the minimum feature size of metal-oxide-semiconductor field effect transistor (MOSFET) has been rapidly scaled down, characteristic variability becomes a major challenge to device technologies and crucial for circuit design. The random dopant fluctuation (RDF) has shown as the major source of variation. It is stringent to examine the device-variability induced characteristic fluctuations of analog circuit and suppression of RD-induced threshold voltage (V_{th}) fluctuation is urgent for 16-nm device technologies. In this part, we for the first time explore the dual materials gate (DMG) and inverse DMG (inDMG) devices for suppressing RDF-induced DC characteristics fluctuation in 16-nm MOSFET devices. However, the same phenomenon can not enjoy the advantage in AC characteristics of DMG

device because the capacitance of depletion region is affected by doping distribution of channel region and effective oxide thickness. Then, we further explore the asymmetric sketch of random dopants distribution near the source end and the drain end in 16 nm MOSFETs. Discrete dopants near the source and drain ends of channel region induce rather different fluctuations in gate capacitance and dynamic characteristics. Based upon the observed asymmetry properties, a lateral asymmetry channel doping profile engineering is then proposed to suppress the random-dopant-induced characteristic fluctuations in the examined devices and circuits. The results of this study indicate the fluctuations of threshold voltage (V_{th}), on-current (I_{on}), transconductance (g_m), intrinsic output resistance (r_o), gate capacitance (C_g), circuit gain, 3dB bandwidth, and unity-gain bandwidth for the cases with dopants near the drain side could be simultaneously reduced by 33.4%, 32.8%, 11.9%, 80.6%, 68.8%, 31.2%, 37.6% and 47%, respectively. Consequently, such lateral asymmetry channel doping profile could be considered to design intrinsic parameter fluctuation resistant transistors.

PART B :

Recently, a-Si:H thin film transistor liquid-crystal display (a-Si:H TFT-LCD) has been widely used in display system of mobile phone. For TFT-LCD panel manufacturing, gate driver circuit with hydrogenated amorphous silicon thin-film transistor (TFT-ASG circuit) plays an important role. Unfortunately, to meet specified display performances of product, such as low power display system, high dynamic characteristics, and so on, system designers have to manually and iteratively adjust the designing parameters of the a-Si:H TFT-ASG driver circuit, which make the design of a-Si:H TFT-ASG driver circuit system complicated and time-consuming. In this part, we propose two different ASG driver circuit topologies to improve circuits' dynamic characteristics. The optimization work is conducted by the adopted simulation-based evolutionary method integrating genetic algorithm and circuit simulator on the unified optimization framework. The first circuit consisting of fourteen hydrogenated amorphous silicon TFTs (a-Si:H TFTs) used in a large panel is optimized for the specifications of the rise time < 1.5 μs, the fall time < 1.5 μs and the ripple voltage < 3 V with the minimization of total layout area. The second one with eight a-Si:H TFTs and two capacitors used in a display panel of mobile phone is optimized with the further condition that power dissipation < 2 mW. By optimizing the devices' width and passive components, the optimized results of this study successfully meet the desired specifications, where the sensitivity analysis is conducted to verify the characteristic variation with respect to the optimized parameters. To validate the results, the optimized circuits are fabricated in standard 4-μm a-Si:H TFT technology and the experimental results confirm the practicability of achieved design. The ripple voltage of 1.9 V is successfully obtained while the rise and fall times satisfying the required specifications for the first circuit's fabricated sample. A 35% reduction of the optimized total devices width of a-Si:H TFTs is also achieved. For the second circuit, the 49% improvement of ripple voltage and 36% reduction of circuit area are obtained from fabricated sample.

In summary, we have studied two important issues for advance semiconductor and current photonics industries. The results of these studies may benefit 16-nm MOSFET technologies and TFT-LCD circuit design.

誌　　謝

兩年來在電信工程研究所的求學過程，隨著論文的付梓，即將劃上句點，心中除了高興，更充滿無盡的感激。高興之情將在我的懷中日漸晶瑩光耀，感激之心將使我的人生成就勇氣。

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求學期間，感謝周復芳老師半導體元件物理上的啟蒙、李義明老師在半導體模擬、電路輔助模擬設計以及最佳化理論上的傳授與悉心指導、洪浩喬、蔡嘉明和蔡尚滐老師在類比積體電路和數位電路上的設計經驗傳授、陳冠能老師在三維積體電路製造上的精闢解說以及渡邊浩志老師在量子力學的觀念灌輸與匡正，使學生累積了豐富的專業知識和視野，為今後的工作打下了堅實的基礎。他們敏銳的思維和平易近人的作風都令學生非常欽佩。

論文口試期間，承蒙國立交通大學電子系黃調元和電機系趙昌博教授，奇美電子公司技術副理黃堃宇博士撥冗細審，惠予寶貴意見與殷切指正使本論文更臻完備。首先謝謝黃調元老師細心研讀學生的碩士論文，逐頁修改错字和文法上的匡正，並且給予正面且實用的建議，也謝謝趙昌博老師也在電路設計上給予良多的意見和指導，最後也要感謝黃堃宇博士在奇美電子公司給予的最直接的協助和幫忙，甚至還給予學生模擬方法上的修正。由於有這些老師的用心和細心，讓學生這本碩士論文能夠更完整，謝謝老師、博士們。

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中華民國九十九年八月
于國立交通大學電信工程研究所
平行與科學計算實驗室

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Chapter 1

Introduction

1.1 Suppression of 16-nm MOSFET Characteristic Fluctuation

In this section, we brief the motivation, literature review and the study of the suppression of 16-nm MOSFET characteristic fluctuation.

1.1.1 Motivation

The mobile-handset market continues to be a dynamic and growing one, enabled by technology advances that include increased bandwidth, greater processing performance, increased power efficiency, and improved display technologies to deliver compelling user experiences. As for multi-Gb/s wireless communications which allocated in the unlicensed spectrum around 60 GHz have been the topic of intense research in the recent past and devices are expected to hit the market shortly. Key aspects behind the increasing interest for technology deployment are the feasibility of the radio in scaled CMOS and the successful demonstration of Gb/s transmissions.

Although the scaling of Complementary metal-oxide-semiconductor (CMOS) devices feature size offer the possibility of operation beyond 100 GHz where new applications are envisioned in the near future, including imaging and spectroscopy systems for scientific, medical, space, and industrial applications at low cost, light weight and easy assembly [1]. The physical gate length of metal-oxide-semiconductor field effect transistors (MOSFETs) roll-off follows the International Technology Roadmap for Semiconductors (ITRS), as shown in Fig. 1.1. However, as the dimension of CMOS devices shrunk into sub-65 nm, double-digit channel dopants make transistor behaviors more complicated to be characterized with conventional ”continuum modeling”. Random nature of discrete dopant distribution results in significantly random fluctuations, such as the deviation of threshold voltage (V_{th}), drive current mismatch, dynamic characteristic fluctuations, and so on. The modern scaled-down devices and characteristics mismatches make maintaining an acceptable dynamic characteristic in analog circuit becomes more challenging.

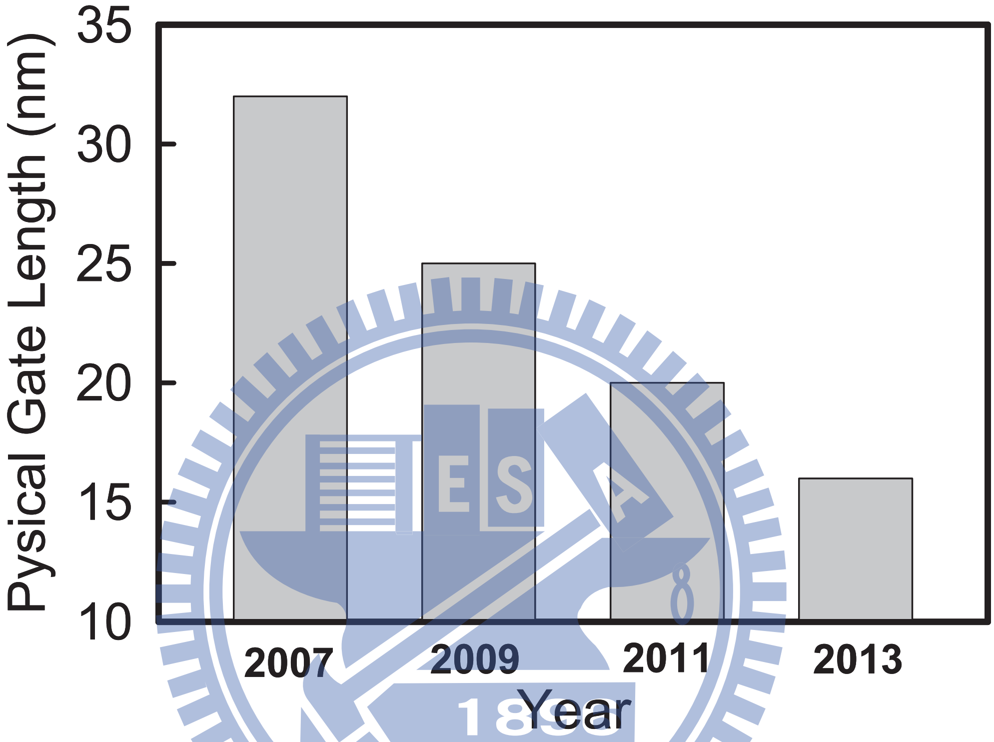


Figure 1.1: The continuously scaling of physical gate length with years from ITRS Roadmap 2007 [2]. The physical gate length is decreased from 32 nm to 16 nm during year 2007 to 2013.

1.1.2 Literature Review

Silicon-based devices are scaled down continually in order to increase density and speed. The gate lengths of scaled metal-oxide-semiconductor field effect transistors (MOSFETs) have been the sub-30 nm for 45 nm node high-performance circuit design [3]. Moreover, the devices with sub-10-nm-gate lengths have been currently investigated [4-7]. For the radio-frequency/mixed-signal applications in mobile phone, a cutoff frequency higher than 200 GHz have been also reported [8,9]. In device point of view, dual material gate (DMG) and lateral asymmetric channel (LAC) were recently proposed to improve device and dynamic performance sequentially [10]. Yield analysis and optimization, which take into account the manufacturing tolerances, model uncertainties, variations in the process parameters, etc., are known as indispensable components of the circuit design methodology [11-15]. However, attention is seldom drawn to the existence of dynamic characteristic fluctuations of active device due to random dopant placement. With geometries of MOSFET shrink, the intrinsic device parameter variations such as line edge roughness [16], the granularity of the polysilicon gate [17,18], random discrete dopants [19-38] effects have brought significant impacts on device characteristic fluctuations; and it is imperative to model and mitigate them in silicon technology. Furthermore, various randomness effects resulting from the random nature of manufacturing process, such as ion implantation, diffusion, and thermal annealing, have induced significant fluctuations of electrical characteristics in nanometer scale (nanoscale) MOSFETs. The number of dopants is of the order of tens in the depletion region of a nanoscale MOSFET, whose influence on device characteristic is large enough to be distinct [19].

Various random dopant effects have been recently studied in both experimental and theoretical approaches [19-38]. Fluctuations of characteristics are caused not only by a variation in an average doping density, which is associated with a fluctuation in the number of impurities, but also with a particular random distribution of impurities in the channel region. Diverse approaches have recently been reported to study fluctuation-related issues in semiconductor devices [19-36] and digital integrated circuit [37-41]. Unfortunately, these studies are mostly focused on the fluctuations of threshold voltage and DC characteristics. However, the investigation of RDF on gate capacitance as well as dynamic characteristics due to random dopant placement is still not clear for nanoscale MOSFET circuit. Dynamic characteristic fluctuations of the nanoscale transistor circuit induced by random dopants and the effectiveness of fluctuation suppression technique are thus intensively explored.

1.1.3 The Study of This Part

In this thesis, an experimental validated three-dimensional (3D) ”atomistic” coupled device-circuit simulation approach will be employed to analyze the discrete-dopant-induced gate capacitance dynamic characteristic fluctuations for the tested 16 nm MOSFET and analog circuits, concurrently capturing ”dopant concentration variation” and ”dopant position fluctuation”. Not only current mirror circuit but also common source amplifier had been investigated in this work. The statistically generated large-scale doping profiles are similar to the physical process of ion implantation and thermal annealing [39]. Based on the statistically (totally randomly) generated large-scale doping profiles, device simulation is performed by solving a set of 3D drift-diffusion equations with quantum corrections by the density gradient method, which is conducted using a parallel computing system [39-45]. In estimation of the characteristics variations in circuit, for obtaining more physical insight device and pursuing higher accuracy, a coupled device-circuit simulation with discrete dopant distribution is conducted to examine the associated behavior of circuit, which concurrently considers the discrete-dopant-number- and discrete- dopant-position-induced fluctuations. Notably, the statistically sound analyzing methodology was quantitatively verified with the experimentally measured data of 20 nm CMOS for the best accuracy [27].

We are then proposed the DMG and inverse DMG devices for suppressing RDF-induced DC characteristics fluctuation in 16-nm MOSFET devices. The physical mechanism of DMG devices to suppress RDF-induced DC characteristics fluctuation are investigated and discussed. Then based upon the asymmetric sketch of the random dopants distribution near the source end and the drain end, it is found that discrete dopants near the source and drain ends of channel region induce rather different fluctuations in gate capacitance and dynamic characteristics. This asymmetry property is utilized to design a lateral asymmetry channel doping profile for the reduction of random-dopant-induced characteristic fluctuations. Consequently, fluctuations of DC characteristics, average gate capacitance, circuit gain, 3dB bandwidth, and unity-gain bandwidth for the devices with dopants near the drain side are significantly reduced. The lateral asymmetry channel doping profile could be considered to design intrinsic parameter fluctuation resistant transistors. The function-dependent and circuit-topology- dependent characteristic fluctuations resulted from random nature of discrete dopants are thus for the first time discussed in this thesis.

1.2 Design Optimization of TFT-LCD ASG Driver Circuit

In this section, the introduction to this study of design optimization of TFT-LCD ASG driver circuit is stated briefly.

1.2.1 Motivation

Hydrogenated amorphous silicon thin film transistors (a-Si:H TFT) are famous for their uniform and low-cost process. Such characteristics have attracted more attention in various applications such as active-matrix organic light-emitting diode (AMOLED) pixels, sensor amplifier, oscillator and gate driver. Furthermore, using the technology of integrated a-Si TFT gate driver on medium and large size TFT-LCD has become the main stream to reduce the cost of manufacturing. The reason is that the gate IC's and display panel are fabricated individually and combined each other by bonding process of conventional design, as shown in Fig. 1.2. However, the bonding process may results in mechanical reliability problem. Therefore, the integrated circuits using a-Si:H TFTs have been proposed to handle reliability and give several advantages such as mature manufacturing technology which can be fabricated with the standard 5 or 4 mask processes, low temperature, low-cost processing, and elimination of the driver ICs. Although the integrated a-Si gate driver circuit has advantage of lowering fabrication cost, it is important and requested to achieve superior and stable output waveform of a-Si integrated gate (ASG) driver circuit in modern TFT-LCD panel industry. To meet specified display performances of product, trial-and-error method is generally adopted by circuit designers to tune circuit parameters of the a-Si:H TFT-LCD circuit, which make the design of a-Si:H TFT-LCD system complicated and time-consuming. As a result, reducing time-consuming while maintain the superior dynamic characteristics is crucial issue and challenging.

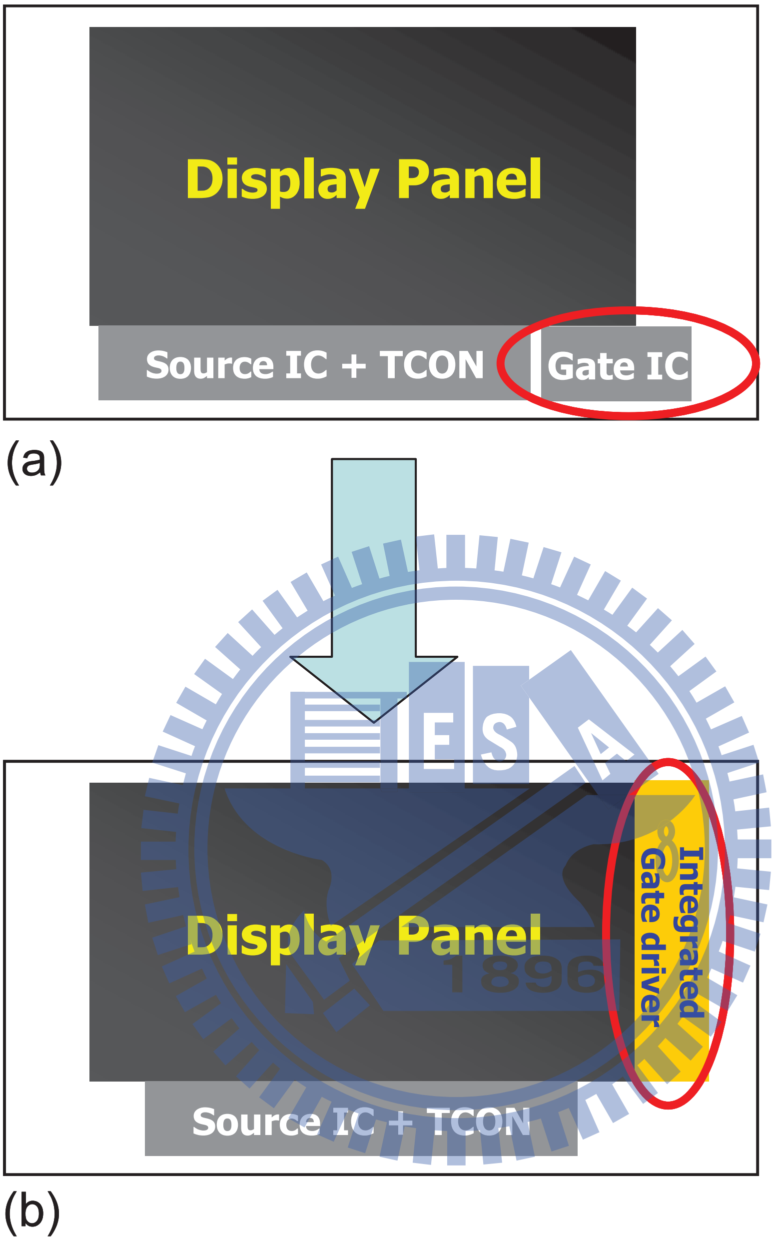


Figure 1.2: (a) Combining display panel and gate IC's by bonding process of the convention design (b) Display panel and integrated gate driver circuit are fabricated simultaneously of the on going design.

1.2.2 Literature Review

LCD displays for application of smart phone is being developed rapidly in points of resolution, pixels per inch (PPI), number of color and brightness. Thus, integrating driver circuit on the TFT backplane is one of the fascinated challenge in QVGA resolution LCD panel because of its many advantages such as overall cost reduction, compactness, and mechanical reliability [46-50]. Diverse approaches such as low temperature polycrystalline silicon (LTPS), hydrogenated amorphous silicon (a-Si:H) [50,51], and zinc-oxide (ZnO) [53,54] are proposed as an active channel material in n-channel thin-film-transistors (TFTs) as well as gate driver circuits sequentially. However, the additional processes which resulted in increasing cost are necessary in LTPS technology. Furthermore, there are several reliable problems of amorphous silicon gate (ASG) driver circuit should be concerned in ZnO film [55]. Therefore, a-Si process has been main stream in gate driver circuit of TFT-LCD for mobile application because of the cost merits due to simple process and high yield in nowadays [56-58]. In general, the ASG driver circuit is requested to achieve superior and stable output waveform. Therefore, dynamic characteristics are usually obtained empirically to meet the required specifications [59-61] for given ASG circuits. Trial-and-error method is generally adopted by circuit designers to tune circuit parameters including device geometry, biasing, etc. This design flow generally is a time-consuming task to meet all desired specifications in display circuit manufacturing. In addition, the methodology of simulation-based evolutionary approach has recently been proposed for optimizing device's doping profile [62-64] and equivalent circuit model parameter extraction [65] in our previous works. Optimization results of these studies computationally have confirmed the robustness and efficiency of the proposed method. Systematical optimization approach, based upon simulation-based evolutionary methodology, will be an interesting study for optimal design of TFT-LCD panel circuits, and thus benefit their manufacturing.

1.2.3 The Study of This Part

In this thesis, we will demonstrate two optimized gate driver circuits on glass substrate to improve dynamic characteristics. Then simulation-based evolutionary algorithm on the unified optimization framework [66] is successfully advanced on performing optimal design of these two circuits on the a-Si:H TFT-LCD panel. The first proposed circuit consists of three pull-up control devices, three pull-down control devices, three pull-up output devices and five pull-down output devices, where all devices' widths are parameters to be designed for the specifications of the rise time $< 1.5\ \mu$s, the fall time $< 1.5\ \mu$s and the ripple voltage < 3 V while we simultaneously consider the minimization of total layout area. The second proposed circuit consists of two pull-up control devices, one pull-down control device, three pull-up output devices and two pull-down devices, where the eight devices' widths and two charged capacitances are tuning parameters to be optimized, and the rise time < 2 μs, the fall time < 2 μs, the ripple voltage < 2 V and the power dissipation $<$ 2 mW are adopted as targets to be achieved. As for the optimized solutions achieved by the method, the sensitivity analysis is simultaneously considered to verify how the variation in dynamic characteristics of optimized circuits. We analyze a selected and modified solution for two ASG driver circuits by $\pm$ 0.5 μm of each width and $\pm$ 0.2 μm of each length with optimized widths sequentially. The final optimized ASG driver circuits are further fabricated with 4-μm process a-Si:H TFT technology. The comparison of dynamic characteristics of measurement and simulation are discussed in detail.

1.3 Outline

The first part of thesis is organized as follows. The fabrication process, physical modeling and numerical methods, analyzing technique for studying the random dopants effect in nanoscale device and circuit are given in Chap. 2. In Chap. 3, we examine the discrete-dopant-induced characteristic fluctuations in the 16-nm MOSFET devices and circuits. Then, the suppression techniques for discrete-dopant-induced fluctuations are proposed and discussed in Chap. 4.

As for the second part, the genetic algorithm and the implemented simulation-based optimization method are introduced in Chap. 5. In Chap. 6, the explored ASG driver circuits are optimized and discussed. In Chap. 7, the fabricated and measured results are shown to validate our theoretical results. Finally, conclusions and suggested future work of the thesis are drawn in Chap. 8.

PART A

Suppression of 16-nm MOSFET Characteristic Fluctuation

Chapter 2

Simulation and Fabrication

In this chapter, a large-scale statistically sound "atomistic" device-circuit coupled simulation approach is proposed to characterize the random-dopant-induced characteristic fluctuations when the gate length of MOSFET integrated circuits is down to 16 nm concurrently capturing the discrete-dopant-number- and discrete-dopant-position-induced fluctuations. We experimentally quantified the random dopant fluctuation (RDF) induced threshold voltage (V_{th}) standard deviation up to 40 mV for sub-20-nm-gate planar metal-oxide-semiconductor field effect transistors. The accuracy of the simulation technique is confirmed by the use of experimentally calibrated transistor physical model.

2.1 Manufacturing Process

The standard MOSFET process flow at National Nano Device Laboratories (NDL) could be summarized as follows:

1. Active area patterning;

2. Shallow trench isolation (STI) formation (chemical-mechanical polishing (CMP));

3. Narrow width device trimmed down upon STI etching;

4. P/N-well implant;

5. Gate oxide and poly gate patterning (I-line ready, deep-UV under planning);

6. Re-oxidation;

7. N/P halo and lightly doped drain shallow junction;

8. SiN MSW;

9. N+/P+ source/drain;

10. Spike rapid thermal anneal (RTA);

11. Low-temperature annealing NiSi;

12. Strained SiN contact etch stop layer (CESL) and interlayer dielectric (ILD);

13. Contact patterning (I-line ready, deep-UV under planning);

14. Ti/TiN/AlCuSi/TiN deposition;

15. M1 patterning;

16. Interlayer dielectric deposition and chemical-mechanical polishing (CMP);

17. Via patterning;

18. Ti/TiN/AlCuSi/TiN deposition; and

19. Sintering.

The entire process flow for planar MOSFET contains about 150 steps, which may take 3 to 4 months. Fig. 2.1 illustrates several key process steps for planar MOSFET. The process is started from active area patterning. After shallow-trench isolation (STI) formation, the device width is trimmed down upon STI etching. Channel doping is performed to adjust threshold voltage (V_{th}) of transistor, using masked ion implantation. To relieve the etch damage; a sacrificial oxide is removed before gate oxidation. Thermal oxide is grown and in-situ heavily doped N+ poly-silicon is deposited. After the deposition and trimmed down of gate hard mask, the pocket implantation technique is used for the suppression of the short channel effect. Composite spacer of silicon oxide and nitride are deposited and etched anisotropically. After the gate and spacer formation, heavily doped N+ junction is made with Arsenic implantation. Low-thermalbudget activation process is used for dopant activation and control of doping profile. After inter-layer-dielectric deposition, tungsten is used for metal contact plugging and copper is used for interconnection. Finally, alloying anneal is performed. We notice that the narrow width device trimmed down upon STI etching and low-thermal-budget activation process are the critical steps in fabrication of sub-20 nm transistor [67].

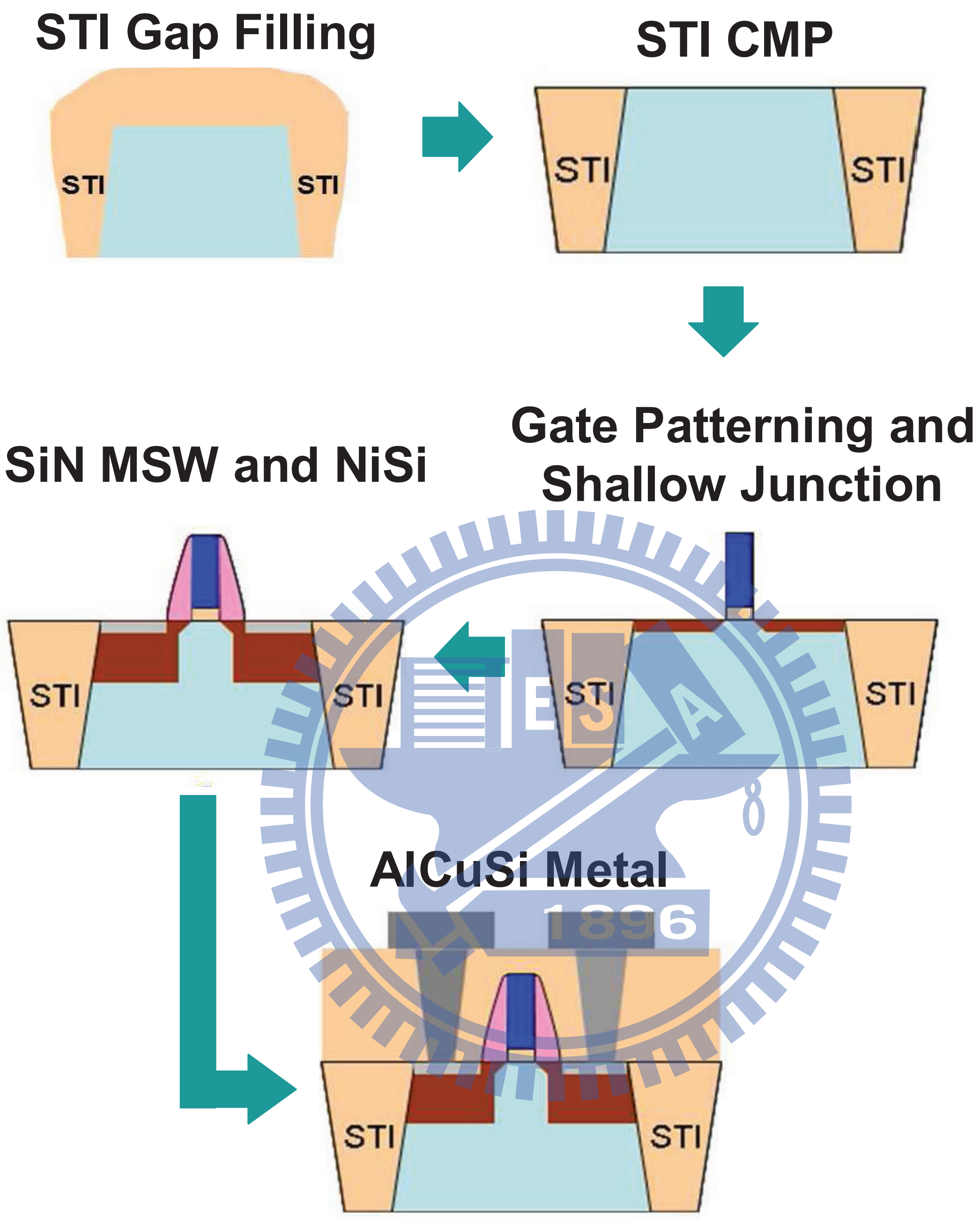


Figure 2.1: Illustrations of planar MOSFET flow in National Nano Device Laboratories (NDL). The process flow consists of 150 steps for planar devices.

2.2 Physical Modeling and Numerical Methods

The technology computer-aided design (TCAD) simulations, such as process and device simulations, are widely used for the analysis of semiconductor devices. The process simulation can generate the device geometry and doping profile according to the parameters of the fabrication processes. The output of process simulation is then used in the device simulation to estimate device characteristics. The drift-diffusion (DD) and hydrodynamic (HD) models play a crucial role in the development of semiconductor device simulator in the macroscopic point of view. The DD model was derived from Maxwell's equation as well as charges' conservation law and has been successfully applied to study device transport behavior, in the past decades. It assumes local isothermal conditions and is still widely employed in semiconductor device design.

Classical drift-diffusion model consists of at least three coupled partial differential equations (PDEs), such as electrostatic potential and electron-hole densities. When device channel is specified, a set of the DD equations in semiconductor device simulation is solved:

$$\triangle\phi = \frac{q}{\varepsilon_s}(n - p + D), \tag{2.1}$$

$$\frac{1}{q} \bigtriangledown \cdot J_n = R(n, p), \tag{2.2}$$

and

$$\frac{1}{q} \bigtriangledown \cdot J_p = -R(n, p), \tag{2.3}$$

where ϕ is the electrostatic potential and its unit is volt. n and p are classical electron and hole concentrations (cm^{-3}). q is the elementary charge and its unit is coulomb. The net doping concentration is $D(x,y,z) = N_D^+(x,y,z) - N_A^-(x,y,z)$. R is the net recombination rate ($cm^{-3}s^{-1}$). The carrier's currents densities are given by

$$J_n = -q\mu_n n \bigtriangledown \phi + qD_n \bigtriangledown n, \tag{2.4}$$

and

$$J_p = -q\mu_p p \bigtriangledown \phi - qD_p \bigtriangledown p, \tag{2.5}$$

where μ_n and μ_p are the carrier mobility ($cm^2/V - s$). The diffusion coefficients, D_n and D_p (cm^2/s), satisfy the Einstein relation.

According to Mathiessen's rule [29-31], the mobility models used in the device simulation can be expressed as:

$$\frac{1}{\mu} = \frac{D}{\mu_{surf\_aps}} + \frac{D}{\mu_{surf\_rs}} + \frac{1}{\mu_{bulk}}, \tag{2.6}$$

where $D = \exp{(x/l_{crit})}$, x is the distance from the interface and l_{crit} is a fitting parameter. The mobility consists of three parts: (1) the surface contribution due to acoustic phonon scattering, $\mu_{surf\_aps} = \frac{B}{\mathbf{E}} + \frac{C(N_i/N_0)^{\tau}}{\mathbf{E}^{1/3}(T/T_0)^K}$, where N_i = N_A + N_D, T_0 = 300 K, $\mathbf{E}$ is the transverse electric field normal to the interface of semiconductor and insulator, B and C are parameters which based on physically derived quantities, N_0 and τ are fitting parameters,

T is lattice temperature, and K is the temperature dependence of the probability of surface phonon scattering; (2) the contribution attributed to surface roughness scattering is $\mu_{surf\_rs} = (\frac{(\mathbf{E}/\mathbf{E_ref})^{\mathbf{\Xi}}}{\delta} + \frac{\mathbf{E^3}}{\eta})^{-1}$, where $\Xi = A + \frac{\alpha \cdot (n+p) N_{ref}^{v}}{(N_i + N_1)^{v}}$, E_{ref} = 1 V/cm is a reference electric field to ensure a unitless numerator in μ_{surf_rs}, N_{ref} = 1 cm^{-3} is a reference doping concentration to cancel the unit of the term raised to the power v in the denominator of Ξ, δ is a constant that depends on the details of the technology, such as oxide growth conditions, N_1 = 1 cm^{-3}, A, α, and η are fitting parameters; (3) and the bulk mobility is $\mu_{bulk} = \mu_L (\frac{T}{T_0})^{-\xi}$, where μ_L is the mobility due to bulk phonon scattering and ξ is a fitting parameter.

The quantum mechanical effects should be considered in the device simulation when the dimensions of the devices shrunk into nanometer scale. Various theoretical approaches have been presented to study the quantum confinement effects, such as full quantum mechanical model (e.g. nonequilibrium Green's function) and quantum corrections to the classical drift-diffusion (DD) or hydrodynamic (HD) transport models. A set of Schrodinger-Poisson (SP) equations have been applied to study the quantum confinement effect in the inversion layers as well as the quantum transport between source and drain, but it is a time consuming task in the TCAD application to realize device characterization. Therefore, various quantum correction models, density gradient (DG) [42-45], Hansch [68], modified local density approximation (MLDA) [69], effective potential (EP) [70-72], and unified quantum correction Model [73], have been proposed for classical DD or HD transport models. In this investigation, the density-gradient is coupled with the DD model and solved for the quantum mechanical effects. The density-gradient equation can be expressed as,

$$\vec{J_n} = -q\mu_n n \bigtriangledown \phi + qD_n \bigtriangledown n - qn\mu_n \bigtriangledown \gamma_n, \tag{2.7}$$

$$\vec{J_p} = -q\mu_p p \bigtriangledown \phi - qD_p \bigtriangledown p + qp\mu_p \bigtriangledown \gamma_p, \tag{2.8}$$

where γ_n and γ_p are the quantum potentials for electrons and holes: $\gamma_n = 2b_n\frac{\bigtriangledown^2\sqrt{n}}{\sqrt{n}}$ and $\gamma_p = 2b_p\frac{\bigtriangledown^2\sqrt{p}}{\sqrt{p}}$ b_n; and b_p are density-gradient coefficients for electrons and holes. $b_n = \hbar^2/(12qm_n^*)$ and $b_p = \hbar^2/(12qm_p^*)$. m_n^* and m_p^* are effective masses for the electrons and holes. $\hbar$ is the Planck constant. b_n and b_p in Eqs. (2.7) and (2.8) are the density gradient coefficient which determines the strength of the gradient effect in the electron and hole gas. The last term in the right hand side of Eqs. (2.7) and (2.8) are referred to as "quantum diffusion", which makes the electron continuity equation having a fourth-order partial differential equation. Therefore, such an approach is highly sensitive to noise in the local carrier density, and the methodology is highly important in cases of strong quantization. To calculate the numerical solution of the multidimensional density-gradient model, firstly we decouple the coupled partial differential equations (PDEs); and approximate each decoupled PDE with the finite volume method over nonuniform mesh. The corresponding system of the nonlinear algebraic equations is then solved with the monotone iteration method. Iteration will be terminated and post-processes will be performed when the specified stopping criteria for inner and outer iteration loops are satisfied, respectively.

2.3 Simulation Technique

Threshold voltage is one of the key device parameters in the characteristics of nanoscale metal-oxide-semiconductor field effect transistors. This section presents the characterization technique for intrinsic parameter fluctuations consisting of line edge roughness (LER), oxide thickness fluctuation (OTF), random-dopant-fluctuation (RDF), and an emerging fluctuation source: work-function fluctuation (WKF). The characterization approaches are examined with experiment data. Base upon the independent of random variables, the total threshold voltage fluctuation, $\sigma V_{th,total}$ is expressed as follows [74]:

$$\sigma^2 V_{th,total} \approx \sigma^2 V_{th,RDF} + \sigma^2 V_{th,LER} + \sigma^2 V_{th,OTF} + \sigma^2 V_{th,WKF}, \tag{2.9}$$

where $\sigma V_{th,RDF}$, $\sigma V_{th,LER}$, $\sigma V_{th,OTF}$, and $\sigma V_{th,WKF}$ are the threshold voltage fluctuations caused by the random-dopant-fluctuation, line edge roughness, oxide thickness fluctuation, and the workfunction fluctuation, respectively. The statistical addition of individual fluctuation sources herein, as shown in Equation (2.9), simplifies the variability analysis of nano-devices and circuits, significantly [74]. In addition, the methodology of LER, OTF and WKF has been proposed and LER- ,OTF- and WKF-induced V_{th} fluctuations are examined in our previous work [74]. However, the result shows that the RDF dominates the V_{th} fluctuation in NMOSFETs, as disclosed in Fig. 2.2.

Therefore, in this thesis, we focus on the characteristic fluctuations induced by random dopant and propose suppression technique to mitigate RDF. The nominal channel doping concentration of the control devices is 1.5×10^{18} cm^{-3}. They have a 16-nm gate, a TiN/HfSiON gate stack of 0.8-nm EOT, and a workfunction of 4.52 eV. Outside the channel, the doping concentrations in the source/drain and background are 1.0×10^{20} cm^{-3} and 1.0×10^{15} cm^{-3}, respectively. For the channel region, to consider the effect of random fluctuation of the number and location of discrete channel dopants, 1327 dopants are firstly randomly generated in a large cube (96 nm)^3, in which the equivalent doping concentration is 1.5×10^{18} cm^{-3}, as shown in Fig. 2.3(a). The (96 nm)^3 cube is then partitioned into 216 sub cubes of 16 nm^3. The number of dopants may vary from zero to 14, and the average number is six, as shown in Figs. 2.3(b) and 2.3(c), respectively. In principle, 3D device simulation with the 216 channel structures almost covers cases, shown in Fig. 2.4, and thus will be fairly meaningful to reflect statistical randomness of dopant number. We have noticed that in this simulation only dopant within the channel region is treated discretely. The doping concentrations remain continuous in the source/drain region because the volume of source/drain region is two-order magnitude greater than that of channel region. These sub-cubes are equivalently mapped into the device channel for the 3D "atomistic" device simulation with discrete dopants, as shown in Fig. 2.5(a). In "atomistic" device simulation, the resolution of individual charges within a classical drift-diffusion simulation using a fine mesh creates problems associated with singularities in the Coulomb potential [75-77]. The potential becomes too steep with fine mesh, and therefore, the majority carriers are unphysically trapped by ionized impurities, and the mobile carrier density is reduced [75-77]. Thus, the density-gradient approximation is used to handle discrete charges by properly introducing related quantum-mechanical effects, and coupled with Poisson equation as well as electron-hole current continuity equations [42-44,78-82].

Without loss of generality, the dual material gate (DMG) and inverse dual material gate (inDMG) are with 16-nm-gate and 1.5×10^{18} cm^{-3} equivalent channel doping concentration. The estimated device with dual material gate has two types, DMG and inverse DMG, as shown in Figs. 2.5(b) and 2.5(c). For DMG device, the workfunction (WK) at the source and drain sides are WK1 and WK2, respectively, and WK1 $>$ WK2. The inverse DMG device are designed accordingly, and WK1 $<$ WK2. The gate materials could be MoN, TiN, and Ta, whose distributions of grain orientation and work-function are summarized in Fig. 2.5(d) [10].

As for the generation of lateral asymmetry doping, the adapted near-drain-end and near-source-end channel doping profile are shown in Figs. 2.6(a) and 2.6(b). Only half of the channel is doped and 1327 dopants are randomly generated in a large rectangular solid (gate width, source-drain direction, channel depth: 48 nm × 96 nm × 96 nm). Therefore, effective channel doping concentration is still 1.5×10^{18} cm^{-3}. Then the large cube is partitioned into 216 sub-cubes ((8 nm) × (16 nm) × (16 nm)) and mapped into drain-end of channel region for discrete dopant simulation. Similarly, the dopants in sub-cubes may vary from zero to 14 (the average number is six) within its sub-cubes, as shown in Figs. 2.7 and 2.8. To estimate the device characteristics on the same basis, the threshold voltage for all devices are calibrated to 250 mV according to ITRS roadmap 2007 [2] for low-operating-power application.

In estimating current mismatch of current mirror circuit, dynamic characteristics of common source amplifier, ultra-small nanoscale devices, and for capturing the discrete-dopant-position-induced fluctuations, a device-circuit coupled simulation approach [33] is employed. The nodal voltage and loop current in the circuit can be calculated. The formulation of circuit equations is mainly base upon the Kirchhoff's current law. The circuit nodal equation of current mirror, as illustrated in Fig. 2.9, is shown in below:

$$\mathrm{Node1} : \mathrm{V_1} = \mathrm{V_{DD}}, \tag{2.10}$$

$$\mathrm{Node2} : \mathrm{V_2} = \mathrm{V_{DD}} - \mathrm{I_{REF}} \mathrm{R_{REF}}, \tag{2.11}$$

$$\mathrm{Node3} : \mathrm{V_3} = 0, \tag{2.12}$$

$$\mathrm{Node4} : \mathrm{V_4} = \mathrm{V_{DD}} - \mathrm{I_{OUT}} \mathrm{R_L}, \tag{2.13}$$

and

$$\mathrm{Node1} : \mathrm{V_5} = \mathrm{V_{DD}}. \tag{2.14}$$

The current mismatch of current mirror circuit and dynamic characteristics of common source amplifier is then estimated. Similarly, the circuit nodal equation of common source amplifier, as displayed in Fig. 2.10(b), is shown in below:

$$\mathrm{Node1} : \mathrm{V_1} = \mathrm{V_{in}}, \tag{2.15}$$

$$\mathrm{Node2} : \mathrm{V_2} = \mathrm{V_{DD}}, \tag{2.16}$$

$$\mathrm{Node3} : \mathrm{V_3} = \mathrm{V_{DD}} - \mathrm{I_D R_1}, \tag{2.17}$$

$$\mathrm{Node4} : \frac{\mathrm{V_4}}{\mathrm{R_2}} + \mathrm{C}\frac{\mathrm{dV_4}}{\mathrm{dt}} = \mathrm{I_D}, \tag{2.18}$$

and

$$\mathrm{Node5} : \mathrm{V_5} = 0. \tag{2.19}$$

The operation bias of common-source circuit is $V_{IN} = 0.5V$ with sinusoid input wave, as shown in Fig. 2.10(a), which is used as a tested circuit to explore the fluctuation of dynamic characteristics. The time-domain simulation results are simultaneously used for the calculation of the property of the frequency response, where the frequency is swept from 1×10^8 Hz to 1×10^{13} Hz. The common-source amplifier circuit with control devices is first explored to illustrate the details of random-dopant-fluctuation in high-frequency integrated circuits. Thus, all device and circuit characteristics are obtained without any devices' equivalent circuit models. The flowchart for mix-mode simulation method is shown in Fig. 2.11. The characteristics of devices of tested circuit are first estimated by solving the device transport equations and using as initial guesses in the device-circuit coupled simulation. The circuit nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix containing the circuit and device equations), which are solved simultaneously to obtain the circuit characteristics [33]. The flowchart of decoupled PDE is shown in Fig. 2.12. First we solve the nonlinear Poisson equation until it is convergence, and then the current continuity equations of electron and hole are following solved. If the error is less than the tolerance, the program stops and output the initial solution of device's potential and perform the mixed-mode simulation. We solve the device's equations coupled with circuit nodal equations until it is convergence. Figure 2.13 shows the flow for solving decoupled PDE. First, the simulation domain has to be discretized. Applying the finite element approximation to the decoupled PDE, we obtained the nonlinear algebraic equations corresponding to the discretized grid. The Newton linearization method is then used to linearize the nonlinear equations. Finally, the linear algebraic equations can be solved using either direct or iterative method.

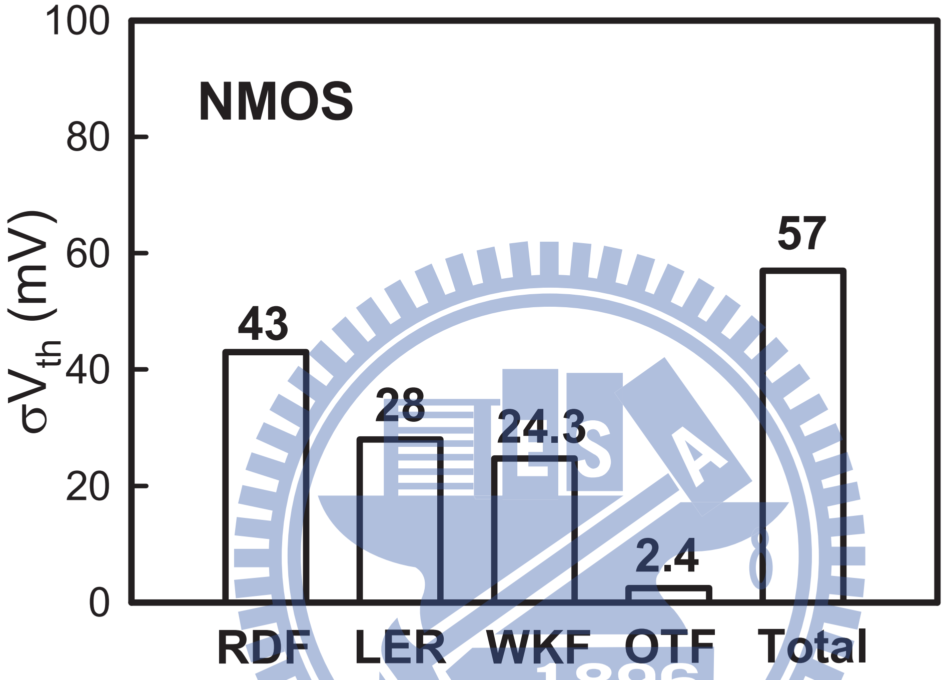


Figure 2.2: The RDF-, LER-, WKF-, OTF-induced V_{th} fluctuation for NMOS devices, where the total σV_{th} is calculated with Eq. 2.9.

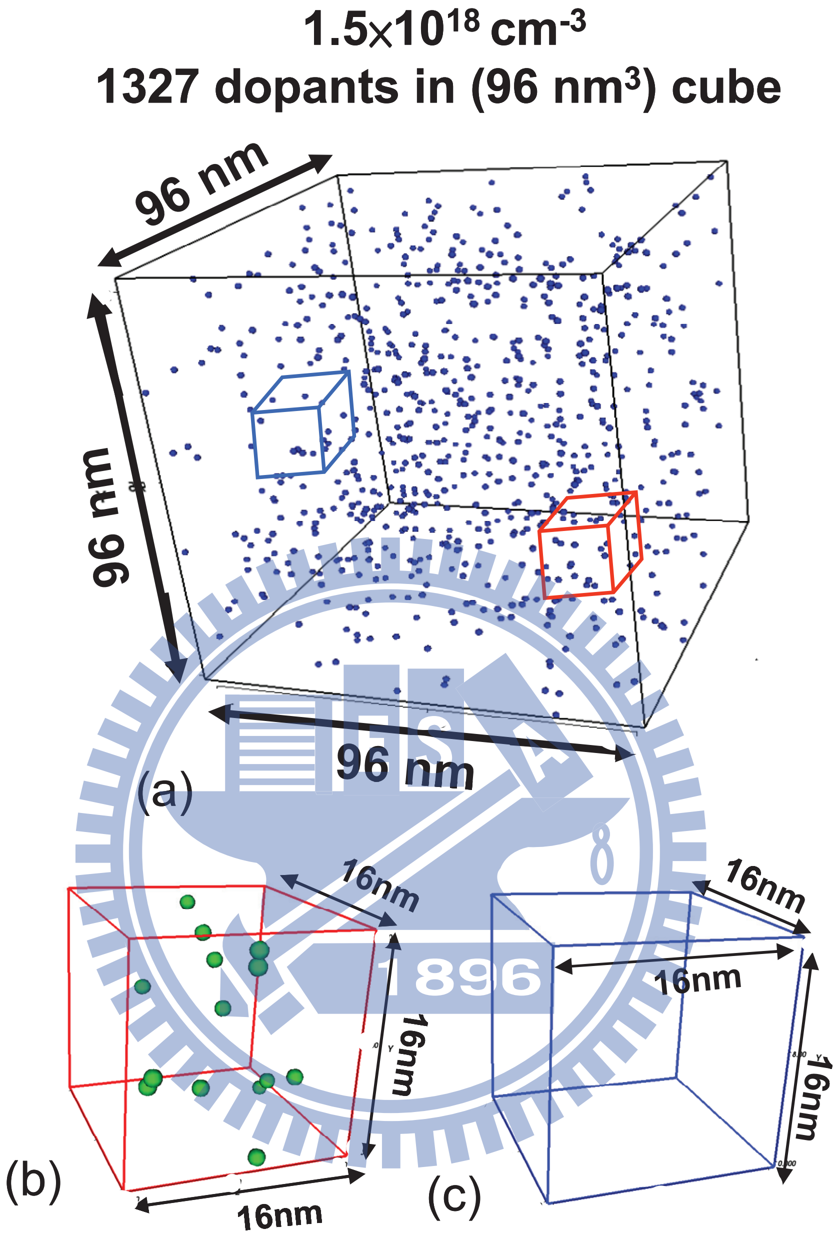


Figure 2.3: (a) Discrete dopants randomly distributed in the (96 nm)^3 cube with the average concentration of 1.5×10^{18} cm^{-3}. There will be 1327 dopants within the cube, but dopants may vary from 0 to 14 (the average number is 6) within its 216 sub cubes of 16 nm × 16 nm × 16 nm ((b) and (c)).

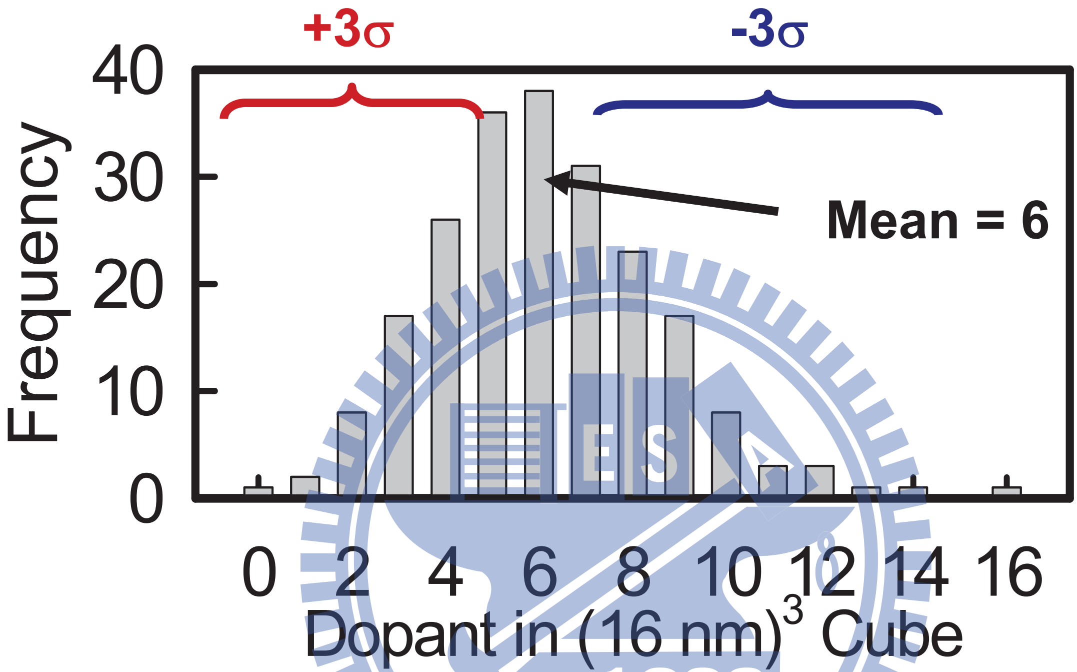
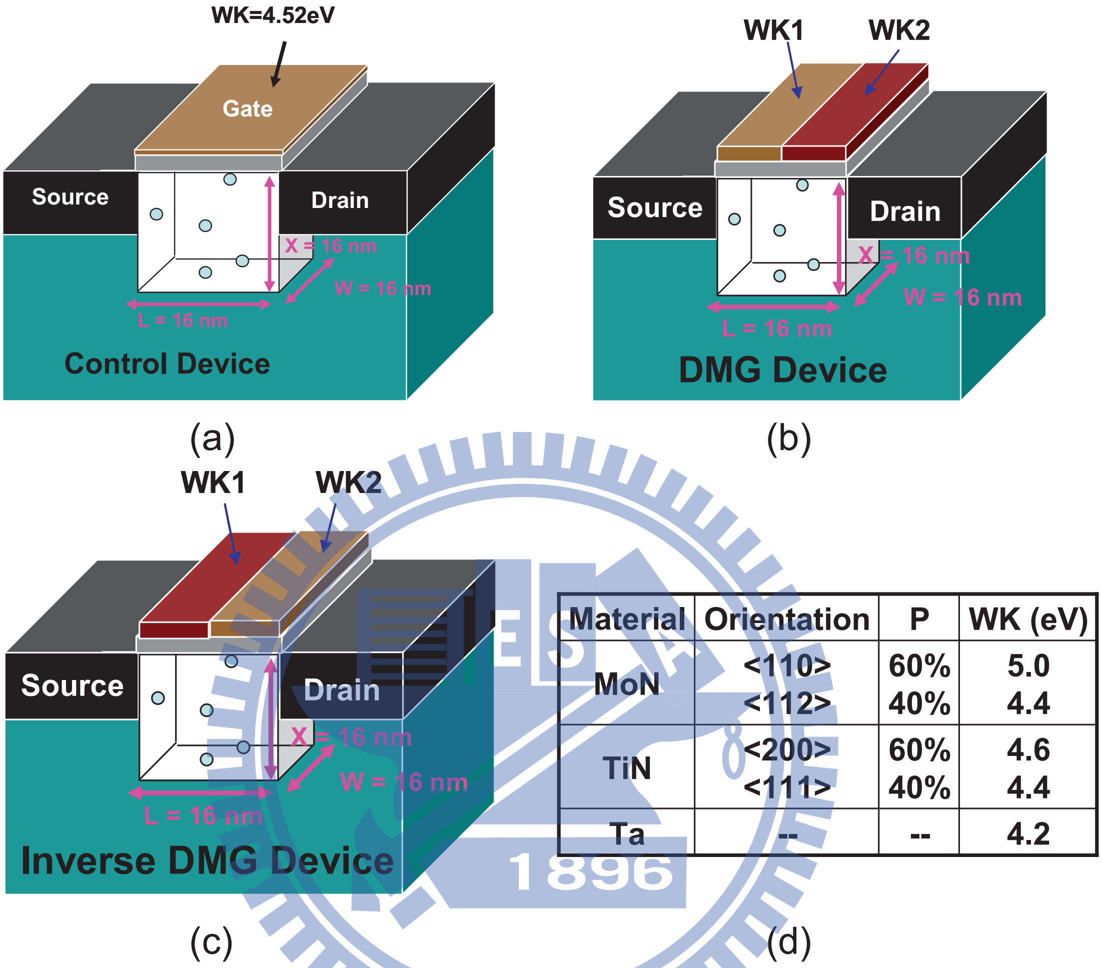


Figure 2.4: The histogram of the dopants in 216 sub cubes for 16 nm devices. The dopants number can be describe by Gaussian Distribution with a mean of six.



Material	Orientation	P	WK (eV)
MoN	<110> <112>	60% 40%	5.0 4.4
TiN	<200> <111>	60% 40%	4.6 4.4
Ta	--	--	4.2

Figure 2.5: The sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in MOSFET (a) control, (b) DMG, and (c) inverse DMG devices, respectively. (d) The properties of metal material used in this study.

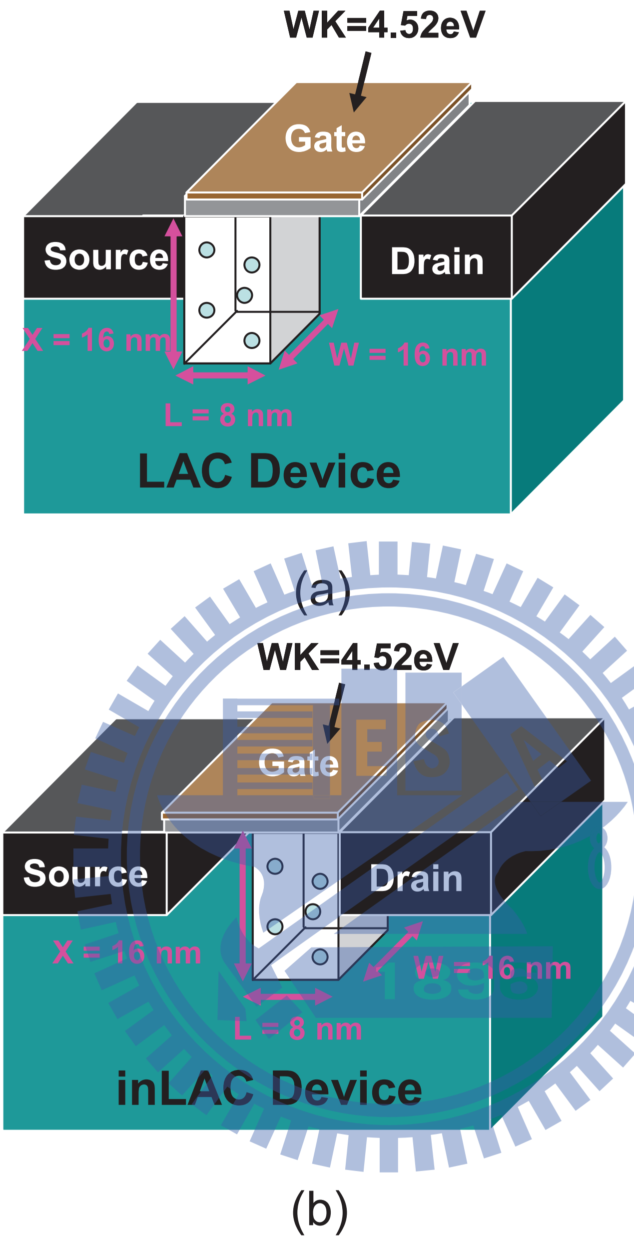


Figure 2.6: The sub-cubes are equivalently mapped into channel region for discrete dopant simulation as shown in MOSFET (b) conventional lateral asymmetric channel (LAC) and (b) inverse LAC devices, respectively.

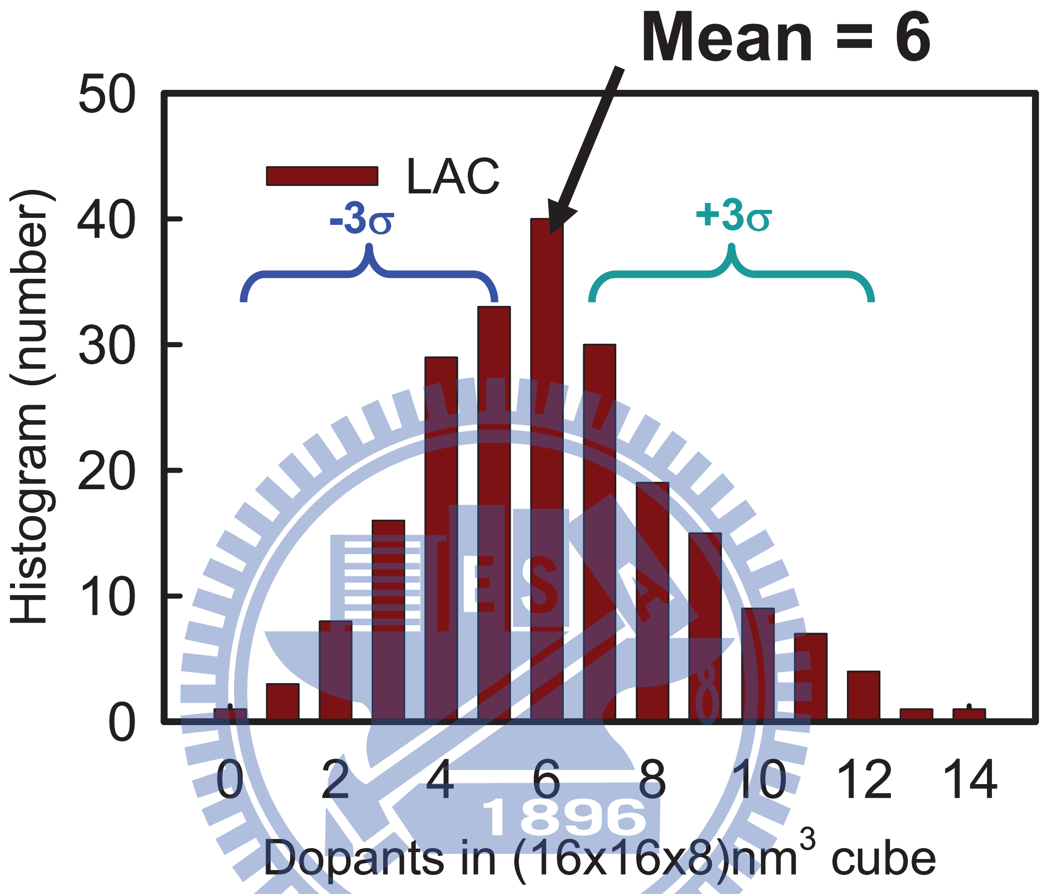


Figure 2.7: The histogram of the dopants in 216 sub cubes (16 nm × 16 nm × 8 nm) for near-source-end channel doping profile of conventional LAC device. The dopants number can be describe by Gaussian Distribution with a mean of six.

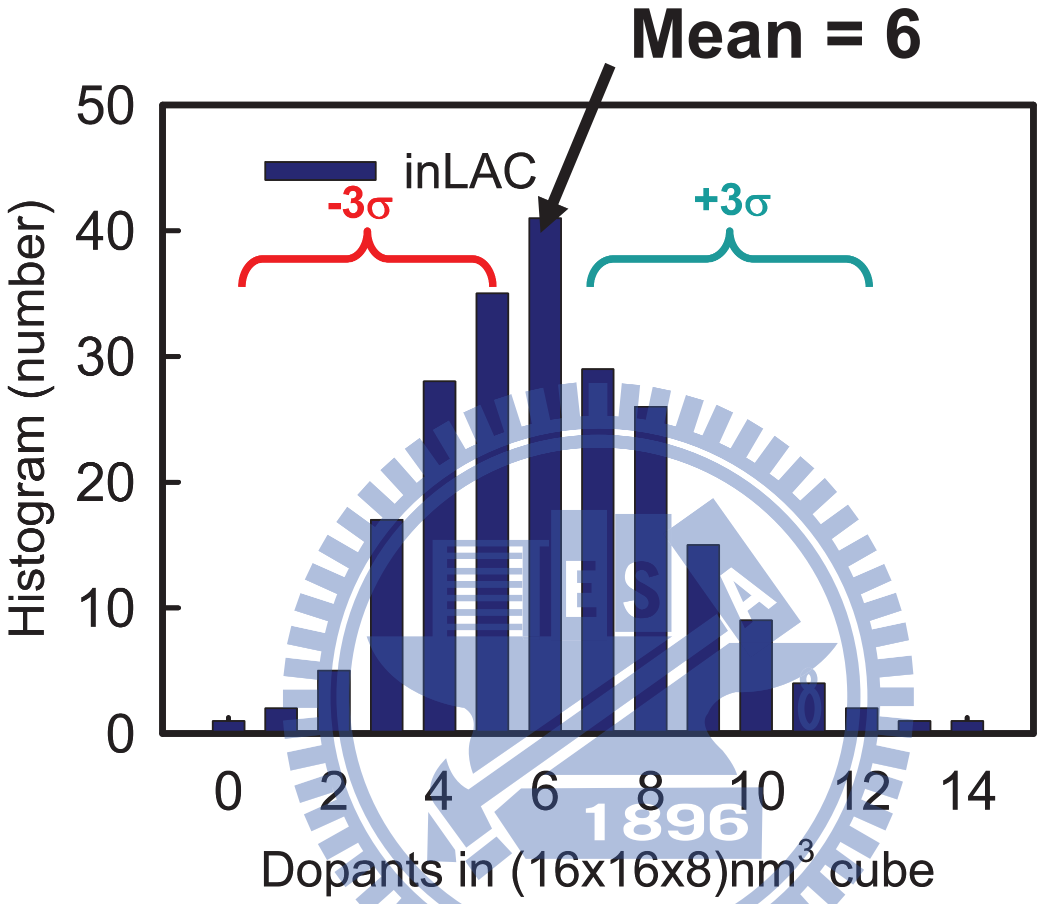


Figure 2.8: The histogram of the dopants in 216 sub cubes (16 nm × 16 nm × 8 nm) for near-drain-end channel doping profile of inverse LAC device. The dopants number can be describe by Gaussian Distribution with a mean of six.

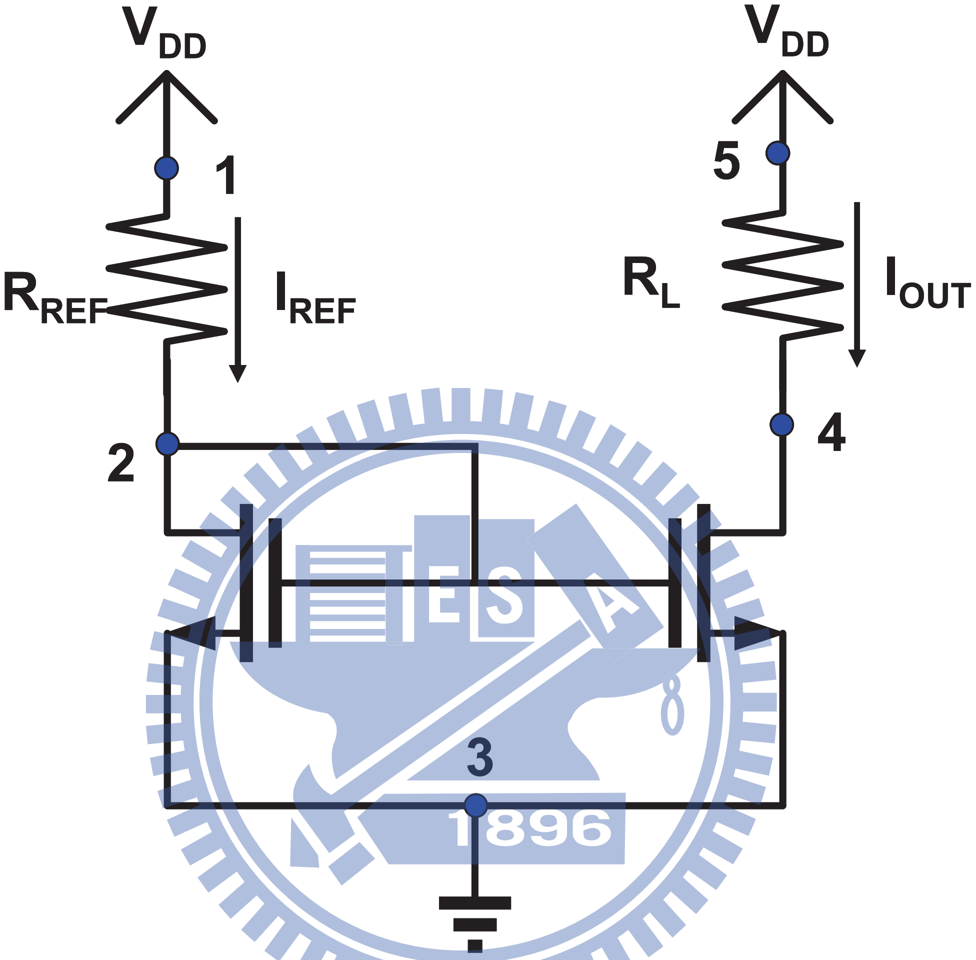


Figure 2.9: The current mirror of analog circuit consisted of NMOS for exploring the variation sources induced current (I_{REF}/I_{OUT}) mismatch.

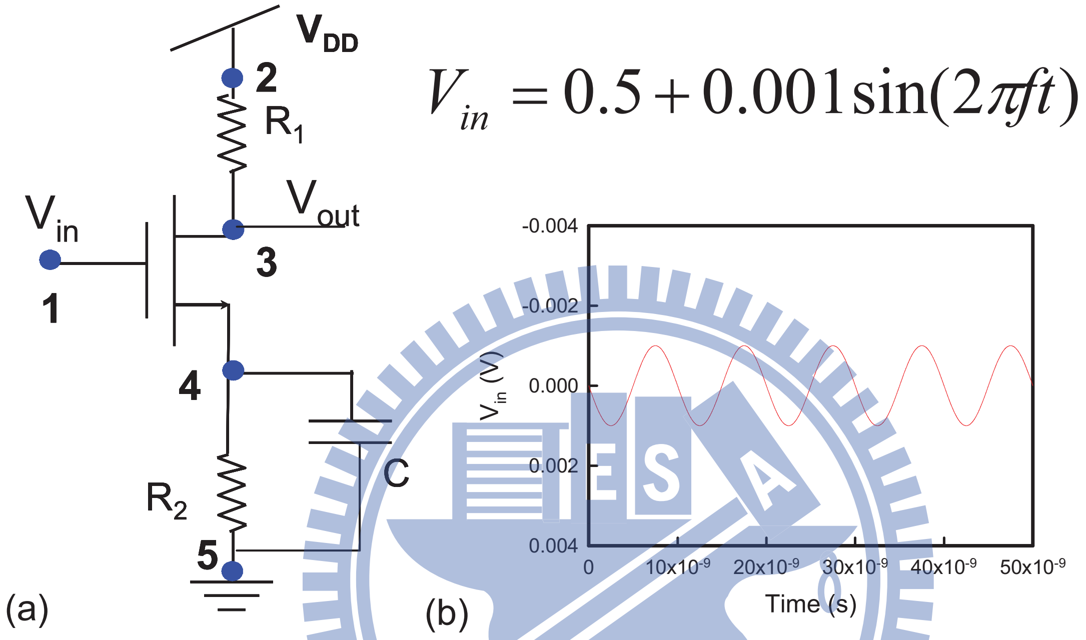


Figure 2.10: (a) The common-source circuit is used as a tested circuit to explore the fluctuation of high-frequency characteristics. (b) The input signal is a sinusoid input wave with 0.5 V offset. The frequency is swept from 1×10^{8} Hz to 1×10^{13} Hz [33].

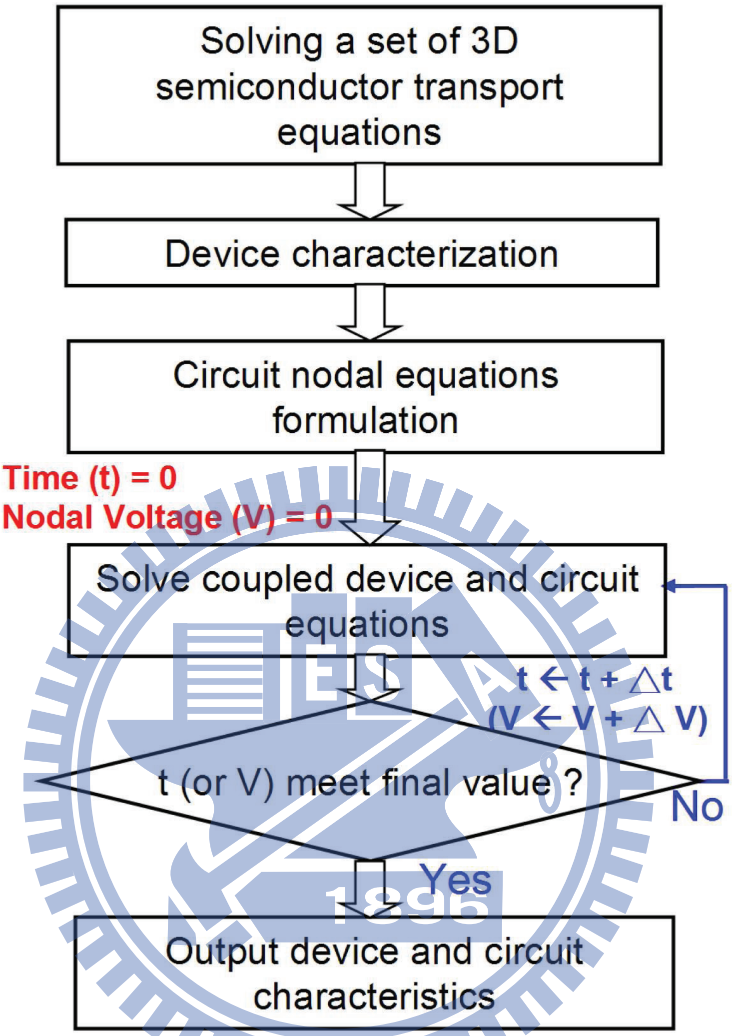


Figure 2.11: The flowchart for the mixed-mode device circuit coupling simulation. The devices simulation is performed first and get the initial solution of the devices potential. The mixed-mode simulation is then executed until the final step [83].

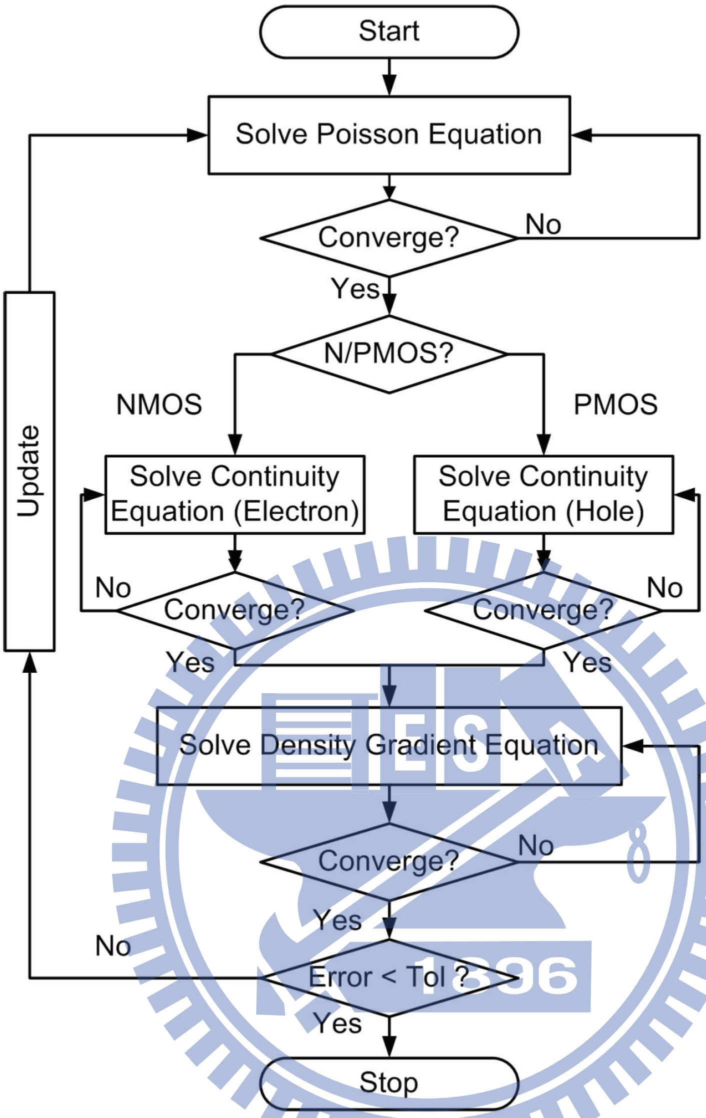


Figure 2.12: A flowchart of the decoupling algorithm. First we solve the nonlinear Poisson equation until it is convergence, and then the current continuity equation of electron and hole is following solved. If the error is less than the tolerance, the program stops.

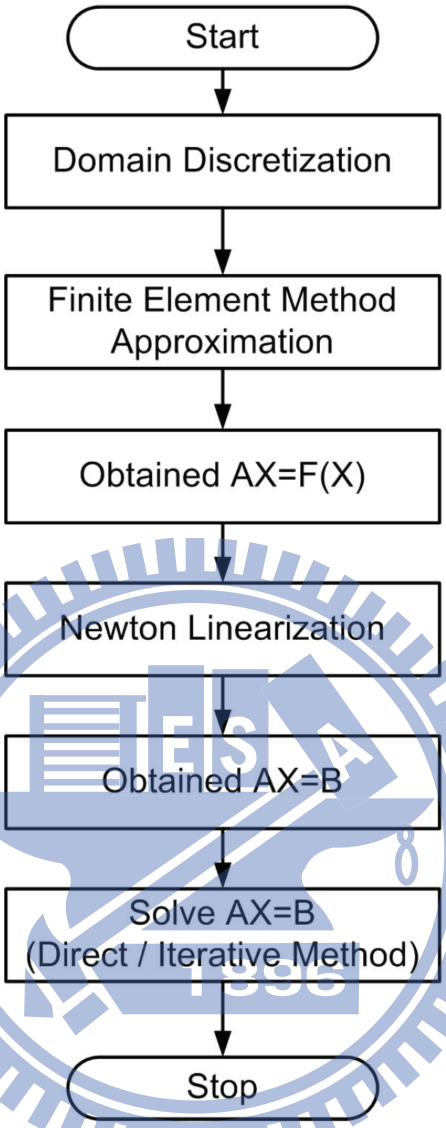


Figure 2.13: A flowchart for solving decoupled PDE. First the simulation domain have to be discretized. Applying the finite element method approximation to the decoupled PDE, we obtained the nonlinear algebraic equations corresponding to the discretized grid. The Newton linearization method is then used to linearized the nonlinear equations. Finally, the linear algebraic equationscan be solved using either direct or iterative method [84].

2.4 Summary of this Chapter

In this chapter, we have presented a standard MOSFET fabrication process and physical model of device simulation. The characterization approach for random dopants fluctuation which dominates the V_{th} fluctuation in NMOSFETs was then introduced. Based on the large-scale statistical approach, the fluctuation of explored transistors, such as control, LAC, inLAC, DMG and inDMG devices could be calculated by solving the device transport equations. The accuracy of control device has been confirmed by experimentally measured data for ensuring the best accuracy.

Chapter 3

RDF Effects in Planar MOSFET and Analog Circuits

In this chapter, the DC characteristics, AC characteristics, and analog circuit characteristics induced by RDF are investigated, such as the electrostatic potential, $I_D - V_G$ characteristics, $C_G - V_G$ characteristics, current mismatch of current mirror circuit, and dynamic characteristics of common source amplifier. The random-dopant-induced V_{th}, I_{on}, I_{off} , g_m, r_o are further discussed in 16-nm-gate planar MOSFETs, respectively. The current mismatch, circuit gain, 3dB bandwidth, and unity-gain bandwidth of analog circuits (current mirror and common source amplifier) are also discussed.

3.1 DC Characteristic Fluctuations

Both the randomness of dopants in the channel and source/drain (S/D) regions may induce the V_{th} fluctuation in a control device. In order to verify the importance of the RDF in the channel region, the RDF in source and drain regions is also investigated. An example of a 16-nm-gate control device with atomistic doping profiles both in the channel and source/drain regions is shown in Fig. 3.1. The actual location of random discrete dopants and the electrostatic potential are illustrated in Fig. 3.1(a). Note that the atomistic doping in the source/drain of device will not only introduce the electrostatic potential fluctuation but also the variations in the effective length of the channel as shown in Fig. 3.1(b). Figure 3.2 shows the comparison of RDF effect in channel versus source/drain region. The V_{th} fluctuations are 42.8 mV and 20 mV in channel and source/drain RDF only devices, respectively. Moreover, the fluctuation is only 47.1 mV for both channel and source/drain RDF devices. It can be seen that the influence of channel RDF on V_{th} fluctuation is around 90%, which means the V_{th} fluctuation in our control device is dominated by the randomness of dopants in the channel rather than the source/drain region. Therefore, RDF in the source/drain region can be neglected and won't be considered in the following study.

Figure 3.3 shows the $I_D - V_G$ characteristic fluctuations of the discrete-dopant fluctuated control devices, where the solid line shows the nominal device, whose channel doping profile is continuously doped with 1.5×10^{18} cm^{-3}, and the dashed lines are random-dopant-fluctuated devices. From the random-dopant-number point of view, the equivalent channel doping concentration is increased when the dopant number increases, which substantially alters the $I_D - V_G$ characteristic, threshold voltage (V_{th}), on-state currents (I_{on}), off-state currents (I_{off}) and transconductance (g_m) as shown in Figs. 3.4. The threshold voltage is determined from a current criterion that the drain current larger than 10^{-7} (W/L) ampere, as marked in Fig 3.3. As the number of dopants in channel is increased, the device's V_{th} is increased and thus decreases the on- and off-state current, as disclosed in Figs. 3.4(a)-(c). The transconductance (g_m) is the change in the drain-source current (I_{on}) divided by the change in the gate-source voltage (V_{GS}) with a constant drain-source voltage (V_{DS}), which is defined by

$$g_m = \frac{\partial I_{on}}{\partial V_g} \propto V_{GS} - V_{th}. \tag{3.1}$$

When the dopant number is increased, according to the definition of g_m, V_{th} will increase and so let g_m decrease, as shown in Fig. 3.4(d). The fluctuation of V_{th} is 42.8 mV in our control devices. Compared V_{th} fluctuation of 31 mV which calculated by analytical formula shown in [15].

$$\sigma V_{th,RDF} = 3.19 \times 10^{-8} \frac{t_{ox} N_A^{0.4}}{\sqrt{L_{eff} W_{eff}}}, \tag{3.2}$$

where the t_{ox} is the thickness of gate oxide; W and L are the width and length of the transistor. However, the analytical formula can only consider the random dopant concentration but the random dopant position. The position of random dopants induced different fluctuation of characteristics in spite of the same number of dopants. The physical mechanism can be briefly described by band profile. Figures 3.5(a) and 3.5(c) show the extracted band profile for the same discrete dopants with different discrete-dopant-location devices from Fig. 3.5(b), respectively. In Fig 3.5(a), the band profile is smooth due to the discrete dopants located below surface. However, there are several potential barriers in the discrete dopant located in surface, as shown in Fig. 3.5(c). These potential barriers are induced by the corresponding dopants in device's channel and therefore change the threshold voltage. Finally, the normalized V_{th}, I_{on}, I_{off}, and g_m variations (the standard deviation divided by the mean value of DC characteristics) in the control device are 16.4$\%$, 10.7$\%$, 73.8$\%$, and 2.6$\%$, respectively.

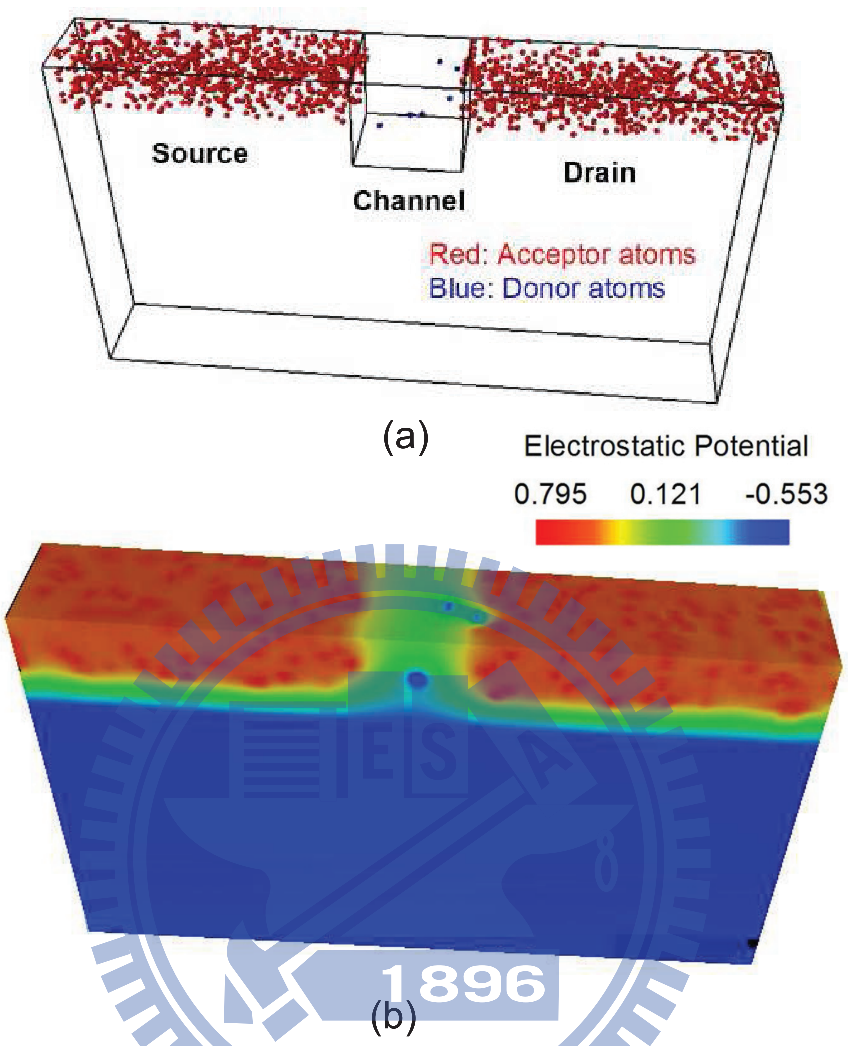


Figure 3.1: Example of a 16-nm planar MOSFET with atomistic doping profiles both in the channel and S/D regions. (a) The actual locations of random discrete dopants and (b) the fluctuation in electrostatic potential are illustrated. There are 7 and 358 dopants located in channel region and S/D region, respectively.

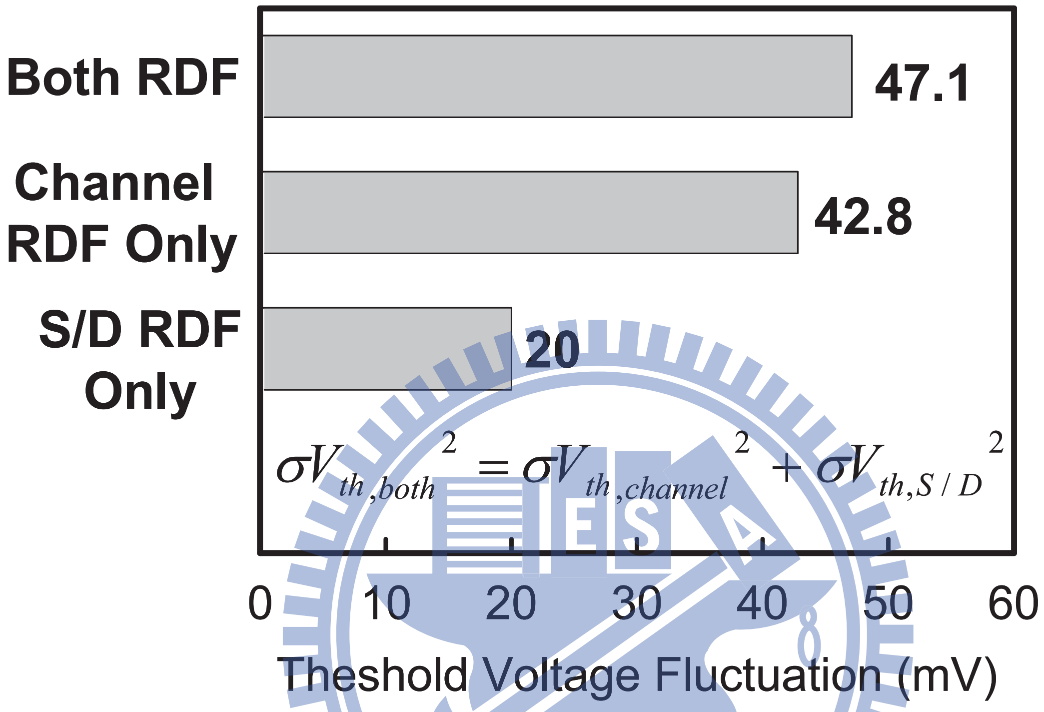


Figure 3.2: Comparison of RDF effect in channel versus S/D region of a planar MOSFET. The V_{th} fluctuations are 42.8 mV and 20 mV for channel and S/D RDF only cases, respectively. The V_{th} fluctuation is 47.1 mV for both channel and S/D RDF cases. Note that the channel RDF introduced around 90% of V_{th} fluctuation.

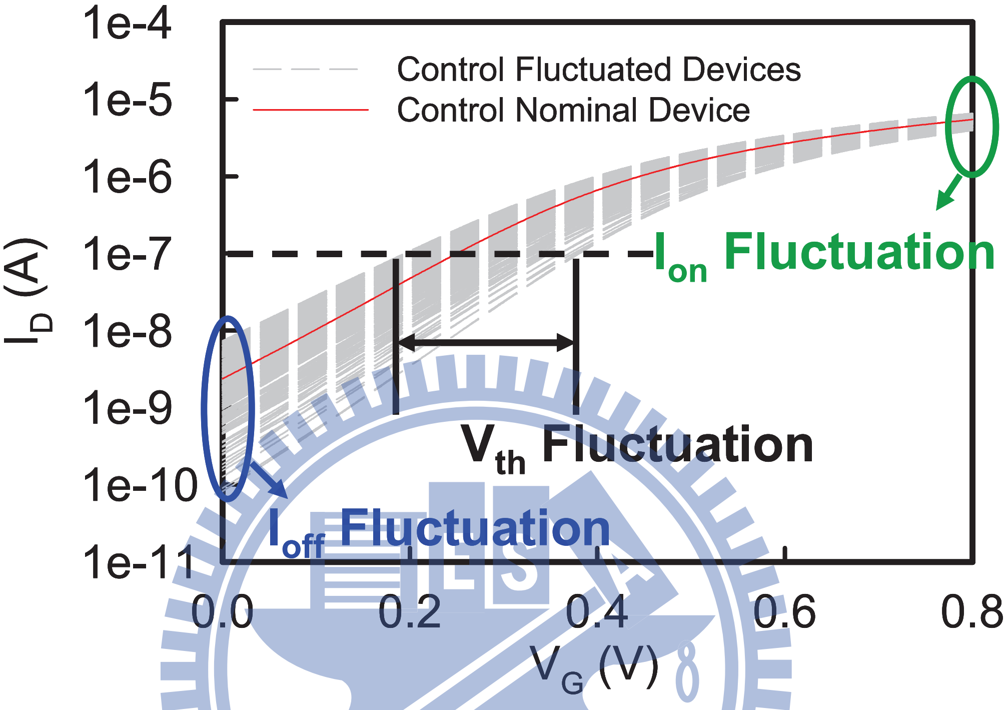


Figure 3.3: DC characteristic fluctuations of $I_D - V_G$ characteristics, where the solid line shows the nominal device, whose channel doping profile is continuously doped with 1.5×10^{18} cm^{-3}, and the dashed lines are random-dopant-fluctuated devices. The threshold voltage is determined from a current criterion that the drain current larger than 10^{-7}A. Ion is determined at V_G = 0.8 V and I_{off} is determined at V_G = 0 V.

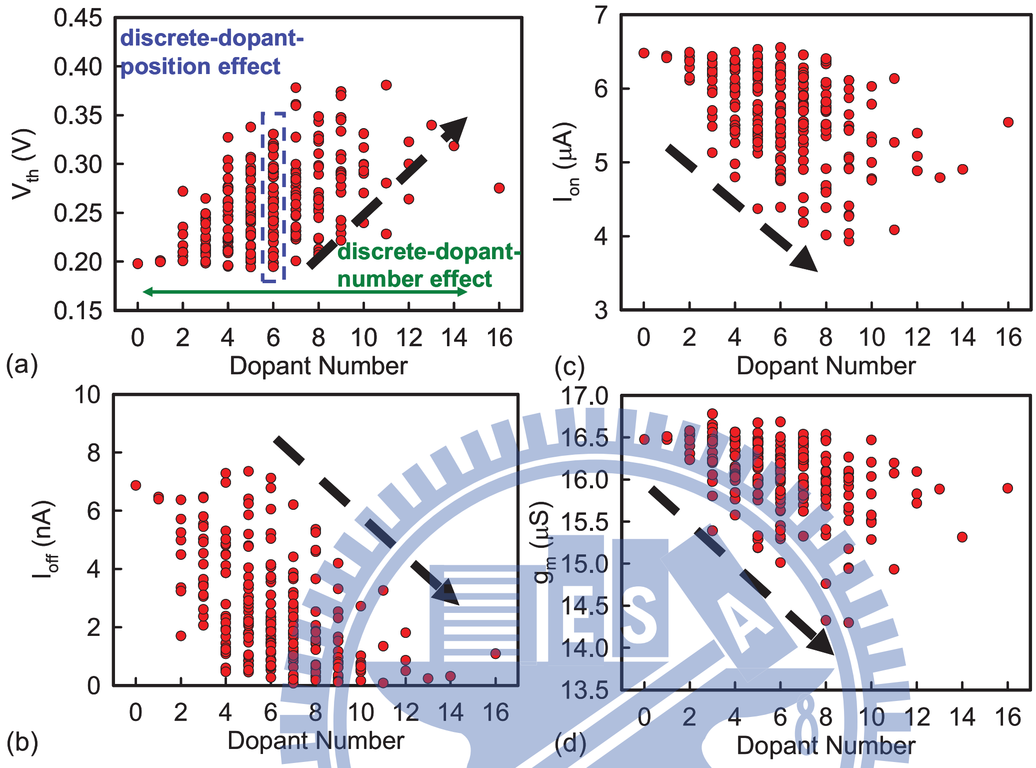


Figure 3.4: DC characteristic fluctuations of (a) V_{th}, (b) I_{off}, (c) I_{on}, and (d) g_m characteristics. As the number of dopants in channel is increased, the devices V_{th} is increased and thus decreases the on- and off-state current and transconductance. The magnitude of the spread characteristics increases as the number of dopants increase. Furthermore, the position of random dopants induced different fluctuation of characteristics in spite of the same number of dopants.

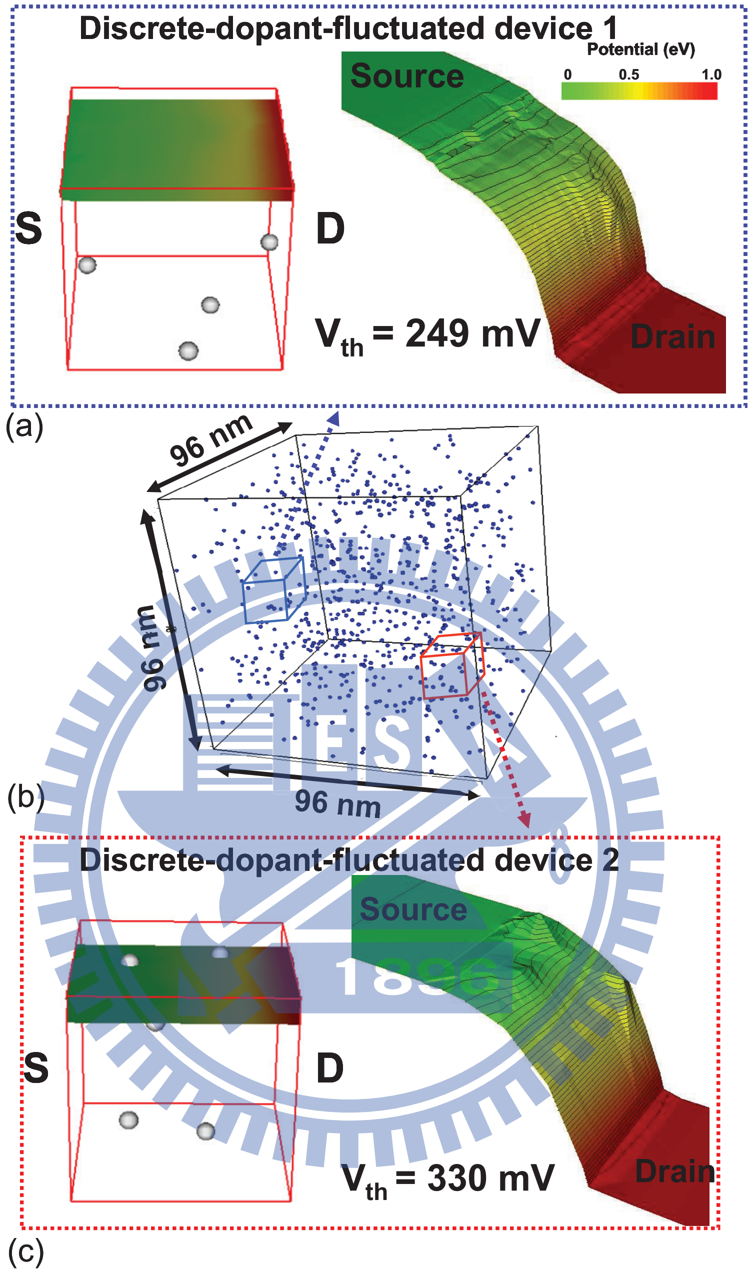


Figure 3.5: Extracted band profile for (a) discrete dopant-located below surface and (c) discrete-dopant-located in the surface devices. Several potential barriers in the discrete-dopant-located in the surface device are induced by the corresponding dopants in devices channel and therefore change the threshold voltage. (b) Discrete dopants randomly distributed in the (96 nm)^3 cube with the average concentration of 1.5×10^{18} cm^{-3}.

3.2 AC Characteristic Fluctuations

Figure 3.7(a) shows the spreading ranges of C-V characteristics for the 216 discrete-dopant-fluctuated control devices with zero and 0.8 V drain bias voltage. The shift and fluctuation of C-V curves are observed. The total gate capacitance ($C_{g,total}$) results from the shunt of the gate-drain capacitance (C_{gd}), the gate-source capacitance (C_{gs}), and the gate-bulk capacitance (C_{gb}), as disclosed in Fig. 3.6. Then corresponding fluctuation of $C_{g,total}$ ($\sigma C_{g,total}$) is shown in Fig. 3.7(b). As the drain voltage is increased, the maximum $C_{g,total}$ is reduced and shift the position of the maximum $C_{g,total}$. To properly explain this phenomenon, the fluctuations of C_{gd}, C_{gs}, and C_{gb} (σC_{gd}, σC_{gs}, and σC_{gb}) with different drain bias are further explored. Figures 3.8-3.10 show the components of C_{gd}, C_{gs} and C_{gb}, where the symbol and error bar denote the characteristics of normal device and fluctuation, respectively; as the V_D changes from 0 V (circles) to 0.8 V (squares), the C_{gd} and the σC_{gd} are decreased due to the wider of depletion layer near the drain junction and the effect of channel pinch-off, as displayed in Fig. 3.8. Then, the C_{gs} and its fluctuation are increased, as shown in Fig. 3.9. It's because of the channel length modulation at drain voltage of 0.8 V, the charges are accumulated near the source junction. As for the C_{gb}, the fluctuation is small due relatively larger distance between gate and substrate and could be neglected, as shown in Fig. 3.10. The drain bias induced different variations in C_{gd} and C_{gs} are observed in this section.

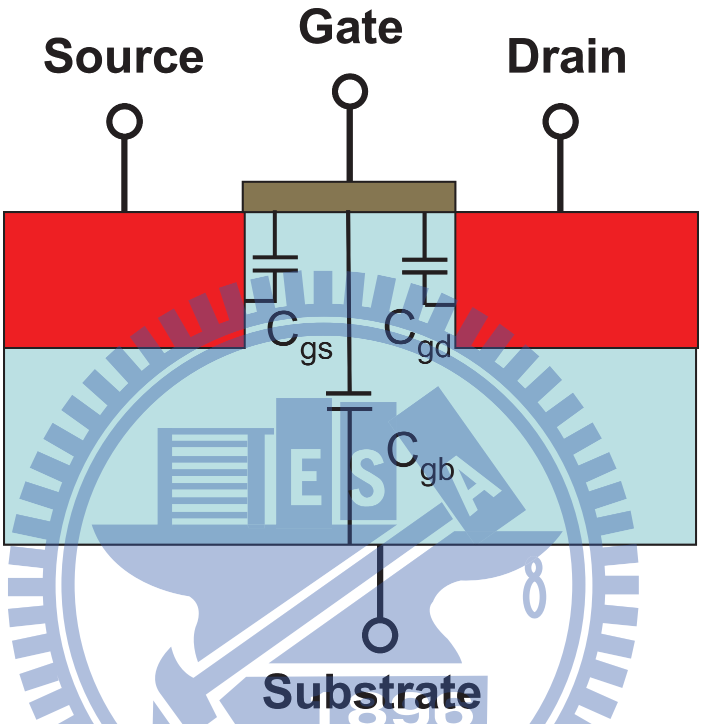


Figure 3.6: The total gate capacitance ($C_{g,total}$) results from the shunt of the gate-drain capacitance (C_{gd}), the gate-source capacitance (C_{gs}), and the gate-bulk capacitance (C_{gb}).

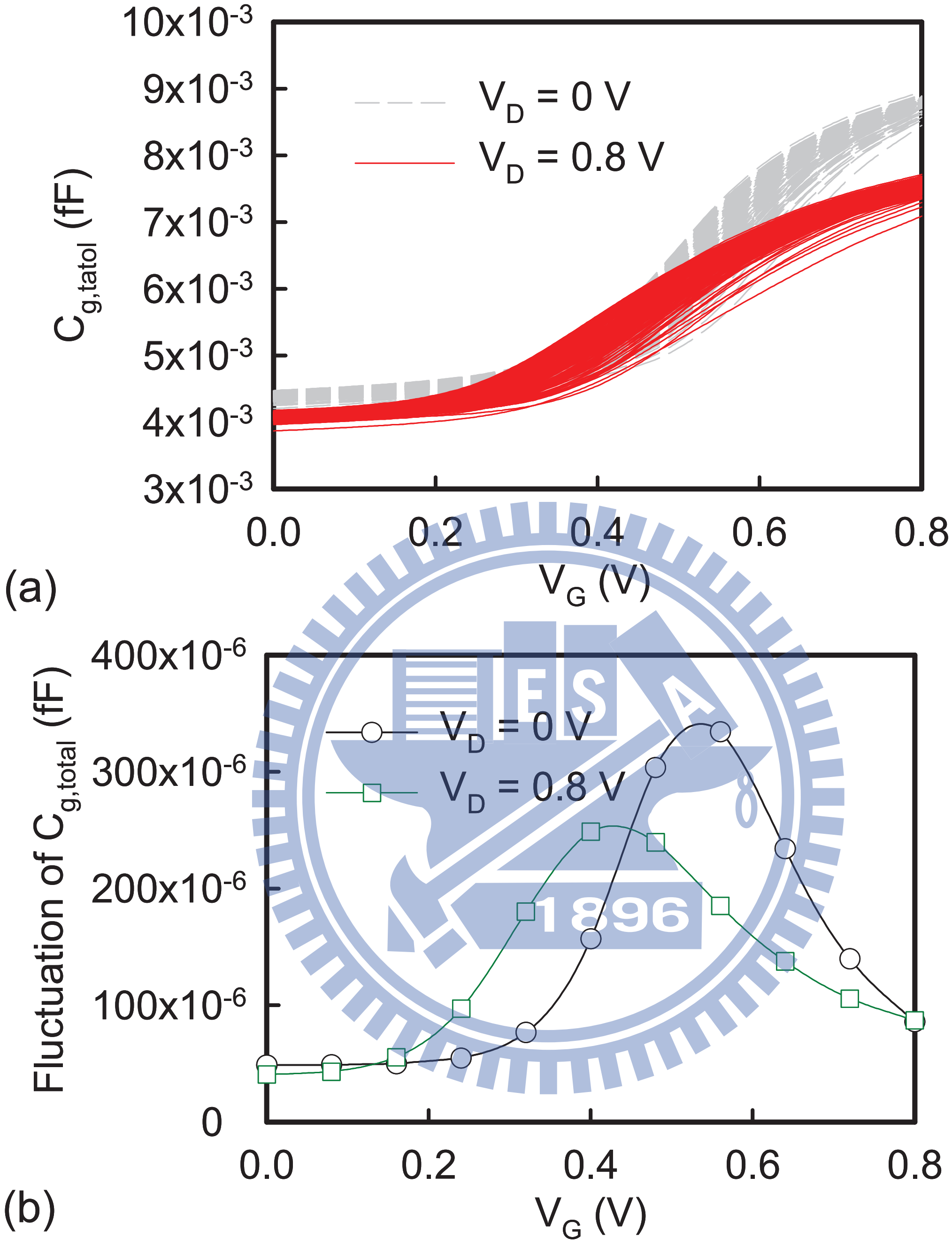


Figure 3.7: (a) The $C_G - V_G$ characteristics of the 216 discrete-dopant-fluctuated control devices. The red solid lines indicate the devices with 0.8 drain bias voltage and gray dash lines are the devices with zero drain bias voltage. (b) Fluctuation of total gate capacitance ($C_{g,total}$) of the 216 discrete dopant fluctuated 16-nm-gate control devices with zero and 0.8 drain bias voltage. The total gate capacitance ($C_{g,total}$) results from the shunt of the gate-drain capacitance (C_{gd}), the gate-source capacitance (C_{gs}), and the gate-bulk capacitance (C_{gb}).

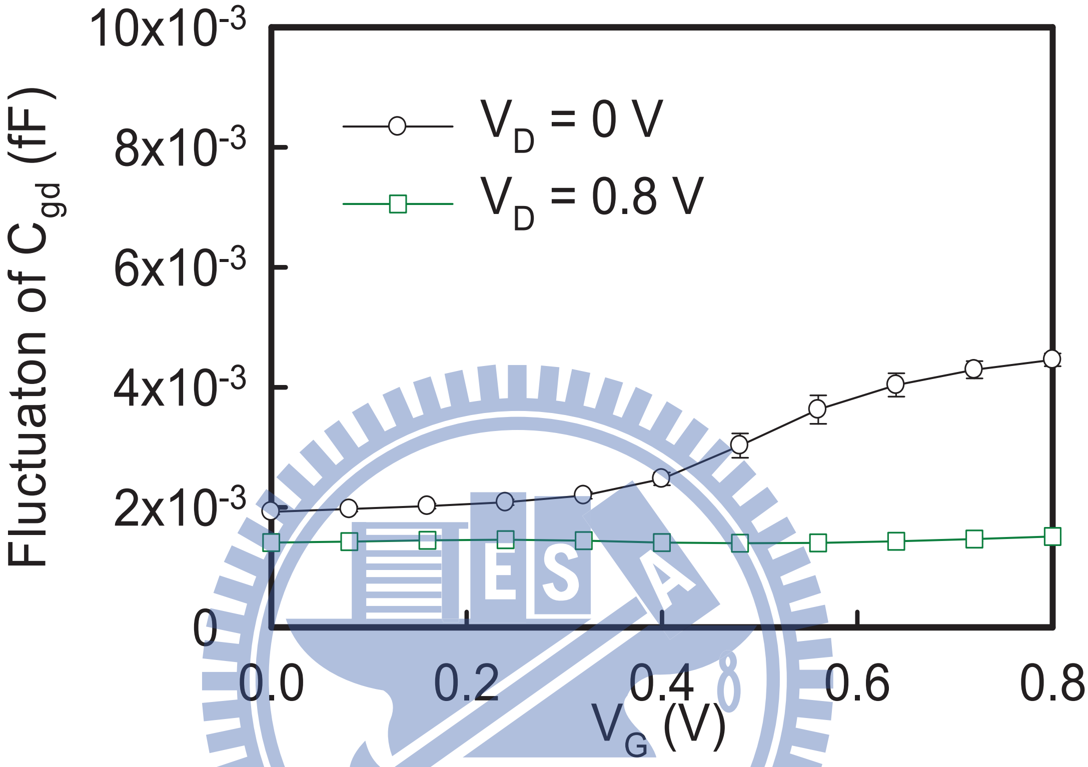


Figure 3.8: Fluctuation of gate-drain capacitance (C_{gd}) for the 216 discrete dopant fluctuated 16-nm-gate planar MOSFETs. The symbol and error bar denote the characteristics of nominal device and fluctuation, respectively. As the V_D changes from 0 V (circles) to 0.8 V (squares), the wider of depletion layer at the drain junction decreases the C_{gd} and thus exhibits less fluctuation.

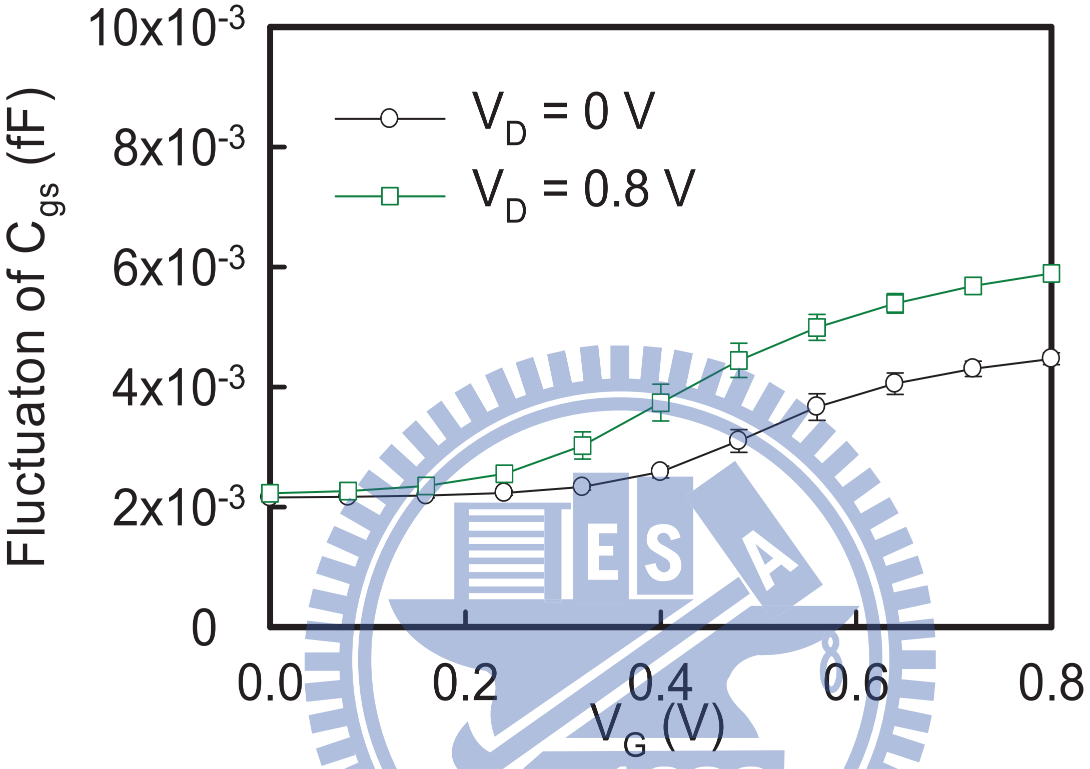


Figure 3.9: Fluctuation of gate-source capacitance (C_{gs}) for the 216 discrete dopant fluctuated 16-nm-gate control device. The symbol and error bar denote the characteristics of nominal device and fluctuation, respectively. The C_{gs} is increased because of the channel length modulation at drain voltage of 0.8 V.

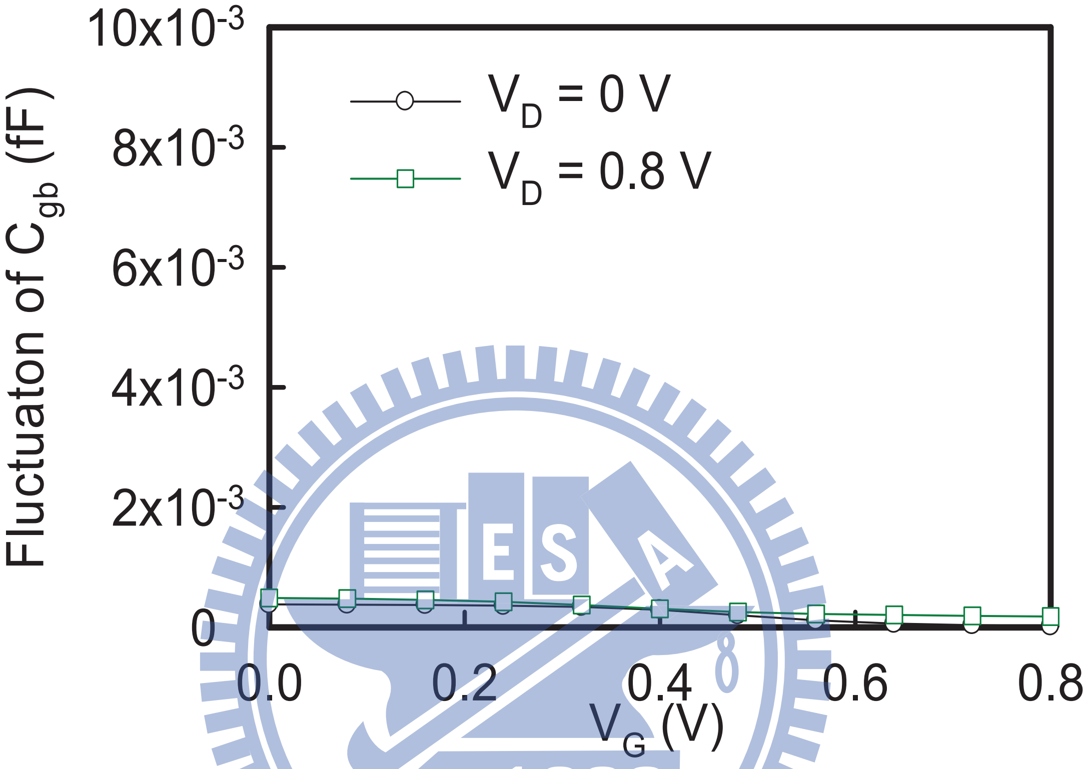


Figure 3.10: Fluctuation of gate-body capacitance (C_{gb}) of the 216 discrete dopant fluctuated 16-nm-gate control device. The symbol and error bar denote the characteristics of nominal device and fluctuation, respectively. C_{gb} is insignificant due to the relatively larger distance between gate and substrate.

3.3 Characteristic Fluctuations of Analog Circuits

In this section, the RDF impacts on driving current of current mirror circuits are studied. The implication of device variability in a common source amplifier is presented as follow.

3.3.1 Current Mirror

The analytical formula of current mismatch for the current mirror circuit which induced by random dopants is expressed as below:

$$\frac{I_{REF}}{I_{OUT}} = \frac{\frac{1}{2}\mu_{n,M1}C_{ox,M1}\frac{W_{M1}}{L_{M1}}[V_{GS1}-(V_{th,M1})]^2}{\frac{1}{2}\mu_{n,M2}C_{ox,M2}\frac{W_{M2}}{L_{M2}}[V_{GS2}-(V_{th,M2})]^2}, \tag{3.3}$$

where the $\mu'_{n,M1}$, $C'_{ox,M1}$, W_{M1}, L_{M1}, V_{GS1}, $V_{th,M2}$, and $\mu'_{n,M2}$, $C'_{ox,M1}$, W_{M2}, L_{M2}, V_{GS2}, $V_{th,M2}$ are the parameters of transistors M1 and M2. If M1 and M2 is matched, the corresponding values are the same, the current ratio is 1. However, these parameters will be different for each device if considering random dopants fluctuation of devices. Here we assume μ'_n, C'_{ox}, W, L, and V_{GS} are constant with respect to RDF, the only term which affects the current mismatch is the threshold voltage fluctuation. To depict the phenomenon clearly, the I_{REF} corresponding to I_{OUT} for each RDF-induced fluctuated circuits are explored in Fig. 3.11. The solid symbols indicated the fluctuated devices and open symbol is nominal device. The I_{OUT} mean (μ) and fluctuation (σ) of NMOSFET-current mirror circuit are 6.19 μA and 0.58 μA, as displayed in inset table of Fig. 3.11. The driving current mismatch of NMOSFET-current mirror circuit (normalized I_{OUT} fluctuation) induced by RDF is calculated by following formula:

$$Normalized \quad I_{OUT} \quad Fluctuation(\%) = \frac{\sigma(I_{REF} - I_{OUT})}{I_{REF}} \times 100\%, \tag{3.4}$$

where the I_{REF} and I_{OUT} are the currents, as shown in Fig. 2.9. The RDF-induced current mismatches are 8.43$\%$ for NMOSFET current mirror circuits. This is due to the I_{REF} and I_{OUT} depend on V_{th} of transistors.

3.3.2 Common Source Amplifier

Figure 3.12 is the intrinsic output resistance of transistor (r_o) versus dopant number, where defined as change in the drain-source current divided by the change in the drain-source voltage, and the relationship with V_{th} can be written as

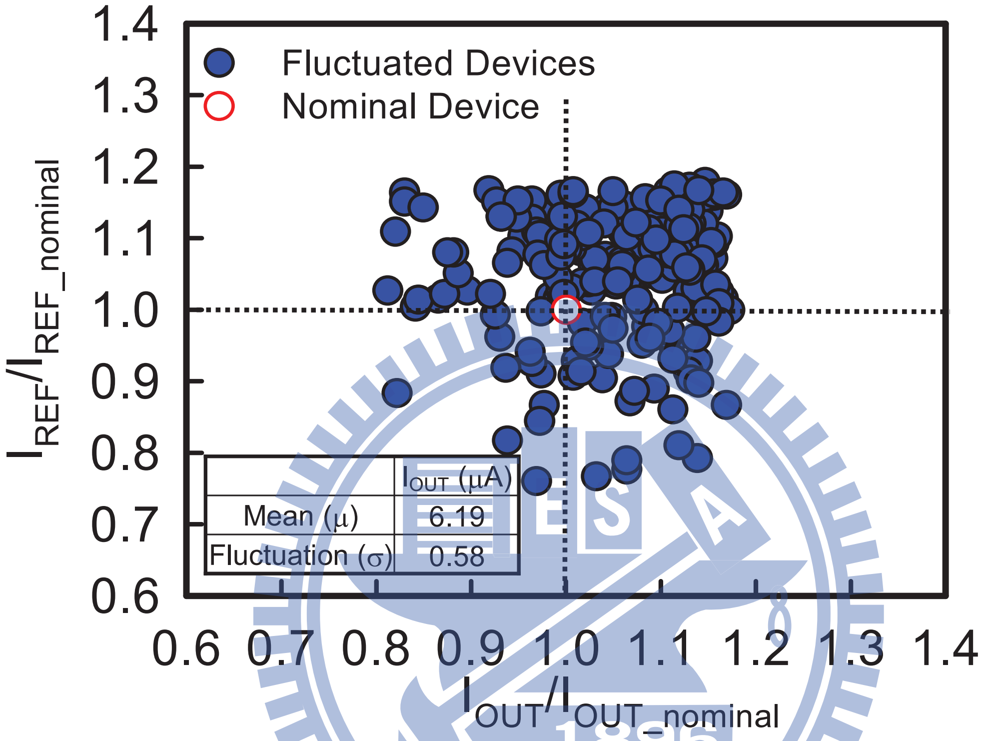
$$r_o = \frac{\partial V_{ds}}{\partial I_D} \propto \frac{1}{(V_{GS} - V_{th})^2}. \tag{3.5}$$

According to Eq. (3.5), since the threshold voltage is increased with increasing channel doping concentration and thus r_o is increased. The position of random dopants induced different fluctuation of r_o in spite of the same number of dopants. Furthermore, the magnitude of the spread characteristics increases as the number of dopants increases. Therefore, the discrete dopant fluctuation not only impacts r_o, but also the operation points of circuits and thus influences the magnitude of output signal.

Figure 3.13 shows the circuit gain versus operation frequency for all fluctuated devices, where the solid line shows the nominal device. The circuit gain, 3dB bandwidth, and unity-gain bandwidth of the nominal case are 11.02 dB, 64 GHz, and 432 GHz, respectively. The corresponding dynamic characteristic fluctuations for the explore circuit are explored, as shown in Figs. 3.13(b)-3.13(d), where the insets show the trend of circuit gain, 3dB bandwidth, and unity-gain bandwidth as a function of device characteristic and circuit element. The gain of the studied circuit is proportional to transconductance multiplied by output resistance of circuit. The circuit output resistance, R_{out}, is given by

$$R_{out} = (\frac{1}{R_1} + \frac{1}{r_o})^{-1}, \tag{3.6}$$

where R_1 is constant value, 500kΩ of the studied circuit. As the number of dopants in device channel is increased, the output resistance of transistor, r_o, is increased. Therefore, the circuit output resistance, R_{out}, is increased as r_o is increased. We notice that although the dependence of R_{out} and g_m on threshold voltage is opposed, the trend of circuit gain fluctuation is dominated the R_{out} due to the square dependence of r_o on $V_{GS} - V_{th}$. Therefore, the trend of circuit gain fluctuation is also dominated by the R_{out} and increased as number of dopant is increased, as shown in Fig. 3.13(b). Figures 3.13(c) and 3.13(d) show the fluctuation of 3dB bandwidth and the unity-gain bandwidth of the nano-MOSFET circuit, which indicate the variations of switching speed nano-MOSFET circuit resulted from random discrete dopants. The insets of Figs. 3.13(c) and 3.13(d) show the main sources of variations contributed from device characteristics fluctuations, g_m, r_o, and C_g. As the number of dopant in device channel is increased, the depletion width is decreased, and then increases the gate capacitance. The fluctuation of C_g accompanied with increasing r_o and decreasing g_m result in a decrement of 3dB bandwidth and the unity-gain bandwidth on increasing dopant number. Similar to the DC characteristic of device, the dynamic characteristic fluctuation of the nanoscale MOSFET circuit is much more scattered as number of dopants is increased. The normalized dynamic characteristic fluctuations are 4.04$\%$, 9.37$\%$, and 4.05$\%$ for circuit gain, 3dB bandwidth, and unity-gain bandwidth, respectively, which are summarized in Table 3.1.



	I_{OUT} (μA)
Mean (μ)	6.19
Fluctuation (σ)	0.58

Figure 3.11: The scatter plot of current mirror current for discrete-dopant-induced fluctuated devices. The filled-in blue symbols indicates the fluctuated devices and open symbol is nominal devices, respectively.

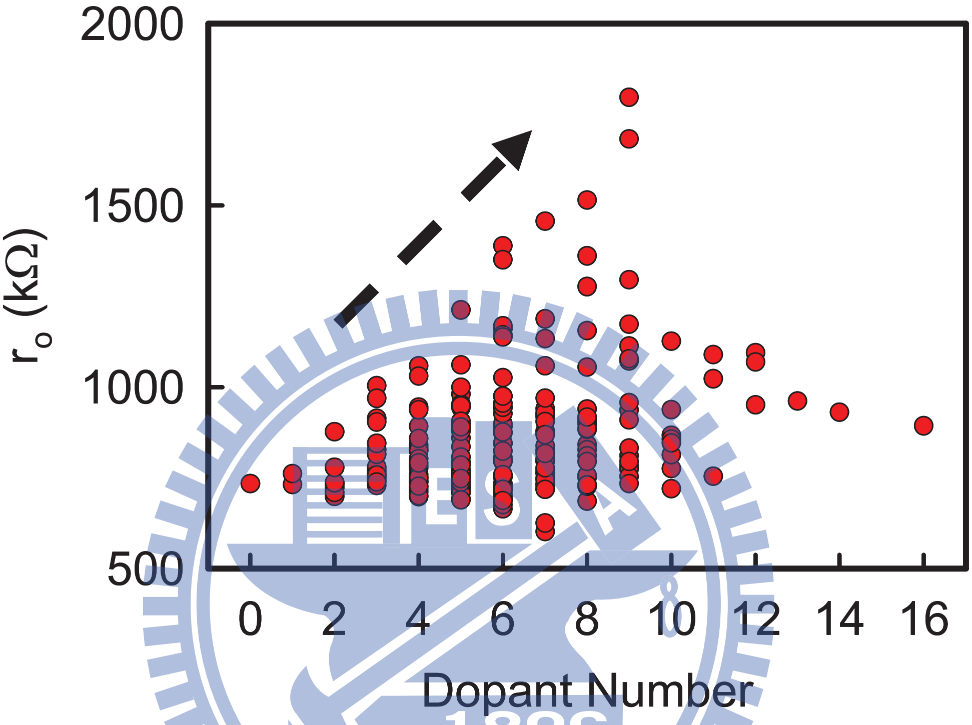


Figure 3.12: DC characteristic fluctuations of r_o of the 216 discrete dopant fluctuated 16-nm-gate control device. As the dopant number is increased, the devices V_{th} is increased and thus decreased r_o.

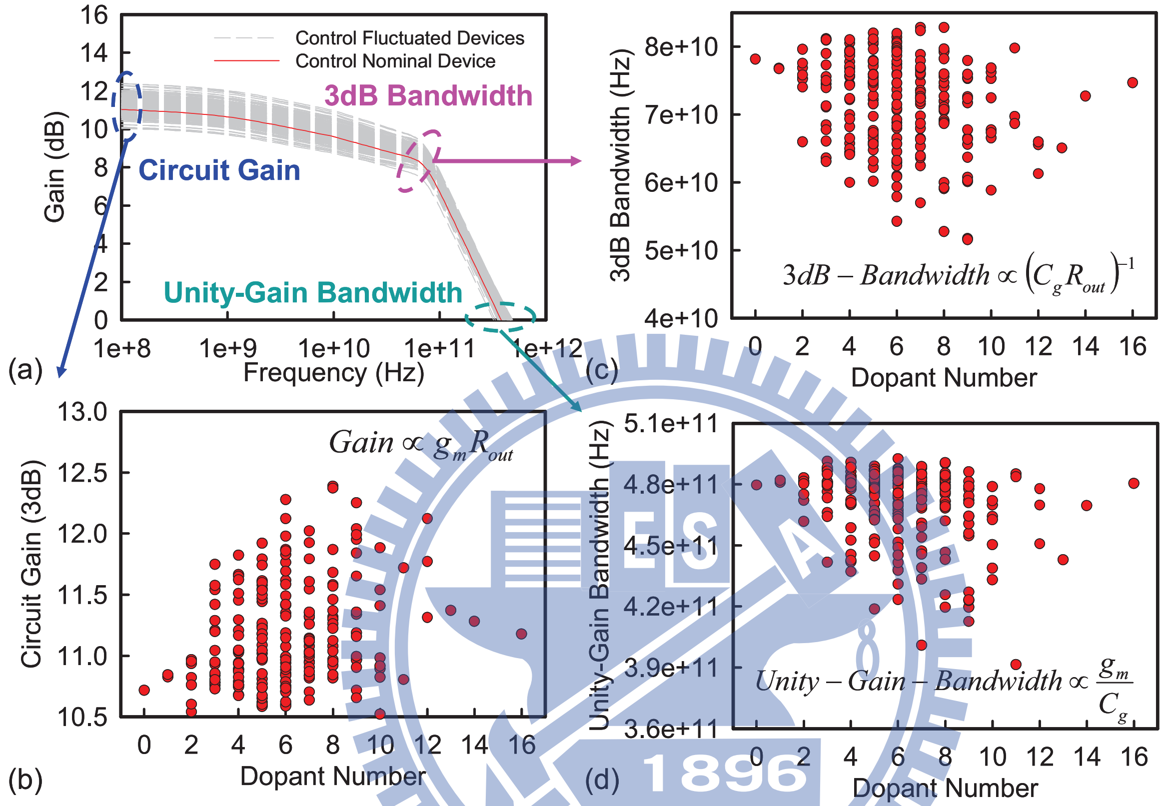


Figure 3.13: The (a) frequency response, (b) high-frequency circuit gain, (c) 3dB bandwidth, (d) and unity-gain bandwidth fluctuations of the studied discrete-dopant-fluctuated 16-nm-gate common source amplifier.

Table 3.1: Summarized dynamic characteristic fluctuations of the nano-MOSFETs circuit.

Dynamic Characteristics	Circuit Gain (dB)	3dB bandwidth (Hz)	Unity-gain bandwidth
Nominal value	11.02	6.43×10^{10}	4.32×10^{11}
Fluctuation	0.45	6.72×10^{9}	1.9×10^{9}
Normalized variation (%)	4.04	4.05	9.37

3.4 Summary of this Chapter

In this chapter, the random dopants- induced DC and AC characteristics of control devices have been investigated. The result shows that the V_{th} fluctuation induced by random dopants is extremely high (about 43 mV fluctuation for device with V_{th}=250 mV) which may result in large current mismatch of current mirror. The random dopants induced gate capacitance as well as dynamic characteristics of common source amplifier circuit have been further explored.

Chapter 4

RDF Suppression Approaches

In this chapter, the physical mechanism of DMG devices to suppress RDF-induced DC characteristic fluctuations are investigated and discussed. Then, a lateral asymmetry channel doping profile engineering is proposed to suppress the random-dopant-induced characteristic fluctuations for the examined devices and circuits.

4.1 Characteristic Fluctuations of Dual Material Gate Device

In this section, we explore the dual materials gate (DMG) and inverse DMG (inDMG) devices for suppressing RDF-induced characteristics fluctuation in 16-nm MOSFET devices. For the higher workfunction (WK) near the source side or the drain side, it may induce higher intrinsic electrostatic potential barrier for both on- and off-state, as shown in Fig. 4.1. The random dopants induce rather different potential profiles due to WK difference in spite of the same number and position of dopants, as disclosed in Figs. 4.2(a)-4.2(c). Therefore, the $I_D - V_G$ fluctuations induced by random dopants for inverse DMG and DMG devices are further presented in Fig. 4.3. The inset tables of Figs. 4.3(a) and 4.3(b) list their nominal value and normalized variations. The DMG device shows smaller DC characteristic fluctuations, the V_{th} are 51.9 mV and 30.8 mV for inverse DMG and DMG devices, respectively. The normalized I_{on} and I_{off} variations of DMG device are 14$\%$ and 80$\%$, and they are smaller than those of inverse DMG device, 18$\%$ and 87$\%$. To examine the physical insights, the same dopants number and position induced potential energies are shown in Fig. 4.4. The dopants will induce potential deviation ϕ_{dopant}, and the high, low, and control WK-induced potential barriers are ϕ_H, ϕ_L and ϕ_M, respectively, as shown in Fig. 4.4. In Figs. 4.4(b)-4.4(d), the dopant will induce relatively smaller potential deviation in DMG due to a larger initial potential barrier existed (ϕ_{dopant}/ϕ_H, compared with ϕ_{dopant}/ϕ_L and ϕ_{dopant}/ϕ_M) in the cross-sectional view of potential energies for dopant near the source side. Therefore, the DC characteristic fluctuations in DMG are dramatically reduced. However, the same phenomenon for dopant near the drain side can not enjoy the advantage in the inverse DMG structure because the carrier controllability is totally decided at the source edge, as shown in Figs. 4.5(a)-4.5(d). The comparison of $I_D - V_G$, potential, electron velocity, and lateral electric field for DMG and control devices are further examined, as shown in Fig. 4.6. For Fig. 4.6(a), the DMG device shows an abrupt potential step in the middle of the channel. This abrupt potential step mainly comes from the WK difference of different gate materials and this potential profile of the DMG device results in locally enhanced lateral electric field inside the channel. For Fig. 4.6(b), the control device attains its maximal electric field peak near the drain according to a classical electric field profile. However, the studied DMG device has electric field peak inside the channel as well as near the drain. Locally generated electric field inside the channel results in a relatively higher carrier velocity, where Fig. 4.6(c) shows velocity profiles along the channel direction. Therefore, DMG device has larger I_{on} in the similar I_{off} compared with the control device, as shown in Fig. 4.6(d). The trend of the dopant number and position effect in DC characteristics of DMG and control device could be confirmed according to the discussion in Chap. 3, as display in Figs. 4.7(a)-4.7(d). For the dopant number increases as equivalent channel doping concentration increases, this substantially alters the V_{th}, the I_{on} and I_{off}. Additionally, the position of random dopants induces different fluctuations of characteristics in spite of the same number of dopants, as marked in inset of Fig. 4.7(d). The improvement of DMG for suppressing the RDF-induced V_{th}, I_{on}, and I_{off} fluctuation are 28$\%$, 12.3$\%$, and 59$\%$, respectively. However, the same suppression of AC characteristic fluctuations can not enjoy the advantage of DMG device because the capacitance of depletion region is affected by doping distribution of channel region and effective oxide thickness, as shown in Fig. 4.8. Therefore, the suppression considering DMG technique will not be discussed for the interested of analog circuit. We now continuously examine the lateral asymmetric channel (LAC) device and circuit.

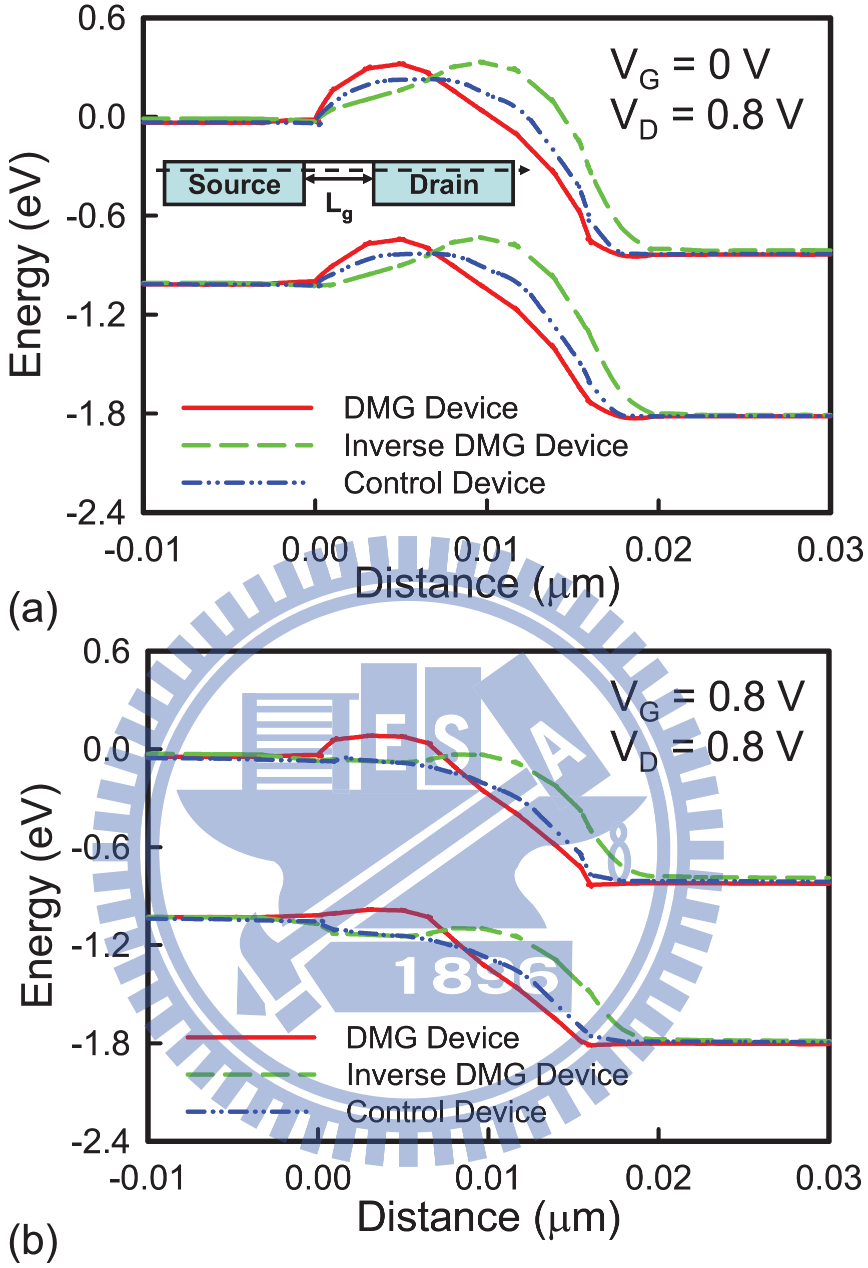


Figure 4.1: The energy band diagram of (a) off-state and (b) on-state for control, DMG and inverse DMG nominal device, respectively. For the higher WK near the source side or the drain side, it may induce higher intrinsic electrostatic potential barrier for both off- and on-state.

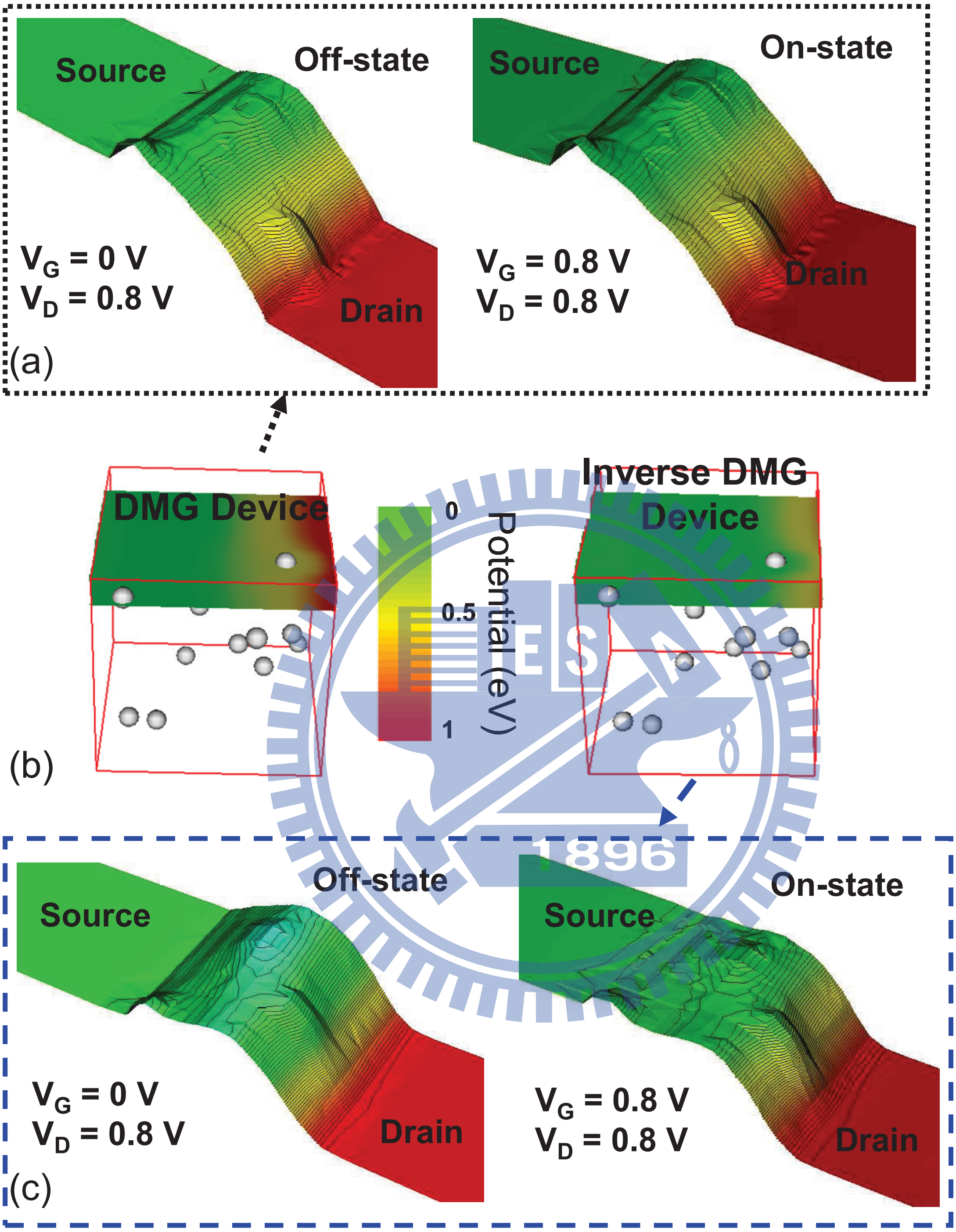
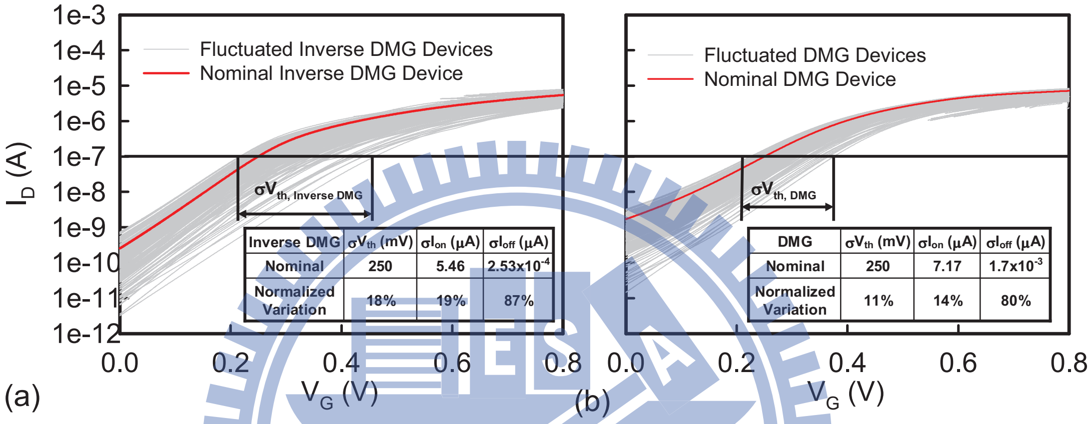


Figure 4.2: The 14 random dopants induce rather different potential profiles due to WK difference in spite of the same number and position of dopants which are extracted from (b) between on-state and off-state for (a) DMG and (c) inverse DMG device.



Inverse DMG	σV_{th} (mV)	σI_{on} (μA)	σI_{off} (μA)
Nominal	250	5.46	2.53×10^{-4}
Normalized Variation	18%	19%	87%

DMG	σV_{th} (mV)	σI_{on} (μA)	σI_{off} (μA)
Nominal	250	7.17	1.7×10^{-3}
Normalized Variation	11%	14%	80%

Figure 4.3: The $I_D - V_G$ curves of (a) inverse DMG and (b) DMG devices. The nominal values and normalized characteristic variations for inverse DMG and DMG devices are summarized in the insets, respectively.

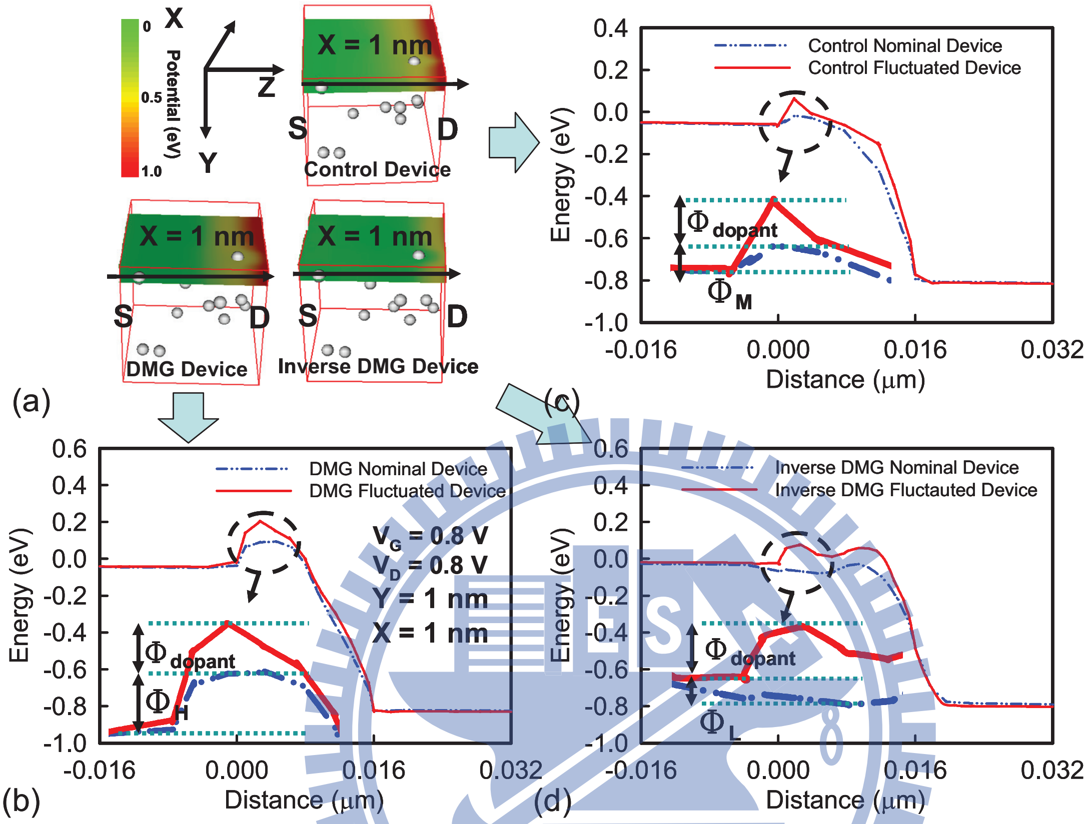


Figure 4.4: (a) The surface potential energy induced by 14 random dopants for control, DMG and inverse DMG devices, respectively. (b)-(d) the slices of potential energy for dopant near source side of control, DMG and inverse DMG devices, respectively. The dopants will induce potential deviation ϕ_{dopant}, and the high, low, and control WK-induced potential barriers are ϕ_H, ϕ_L and ϕ_M, respectively.

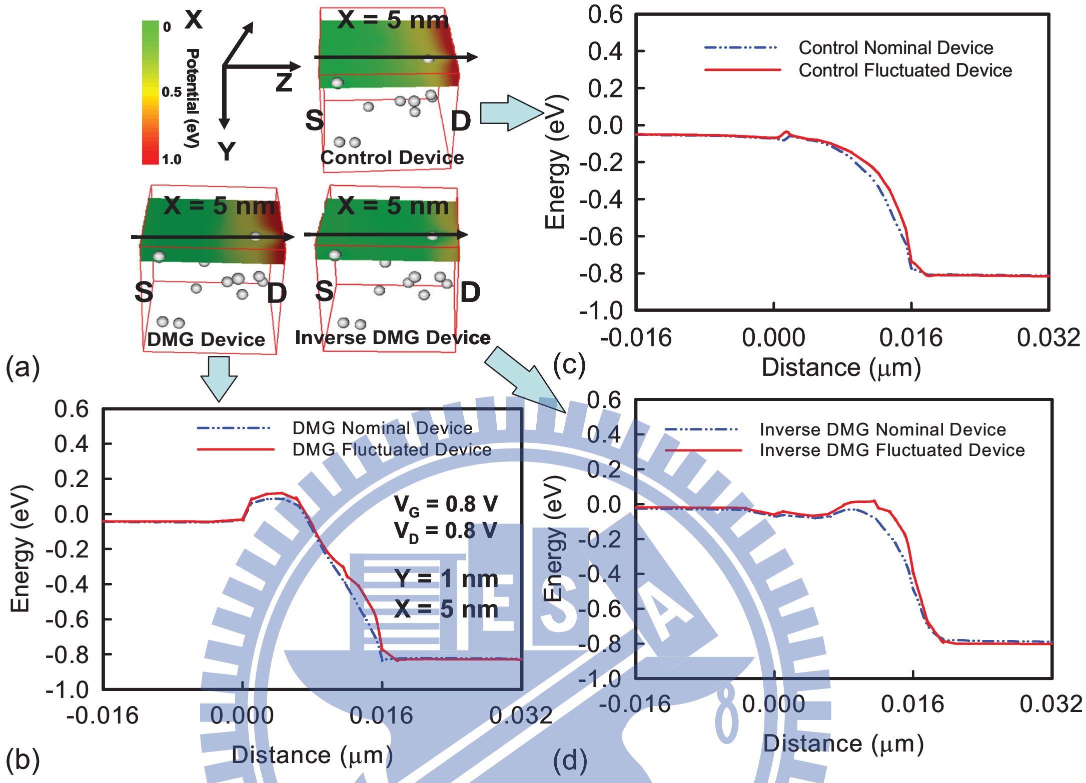


Figure 4.5: (a) The surface potential energy induced by 14 random dopants for control, DMG and inverse DMG devices, respectively. (b)-(d) the slices of potential energy for dopant near drain side of control, DMG and inverse DMG devices, respectively. The phenomenon for dopant near the drain side can not enjoy the advantage in the inverse DMG structure because the carrier controllability is totally decided at the source edge.

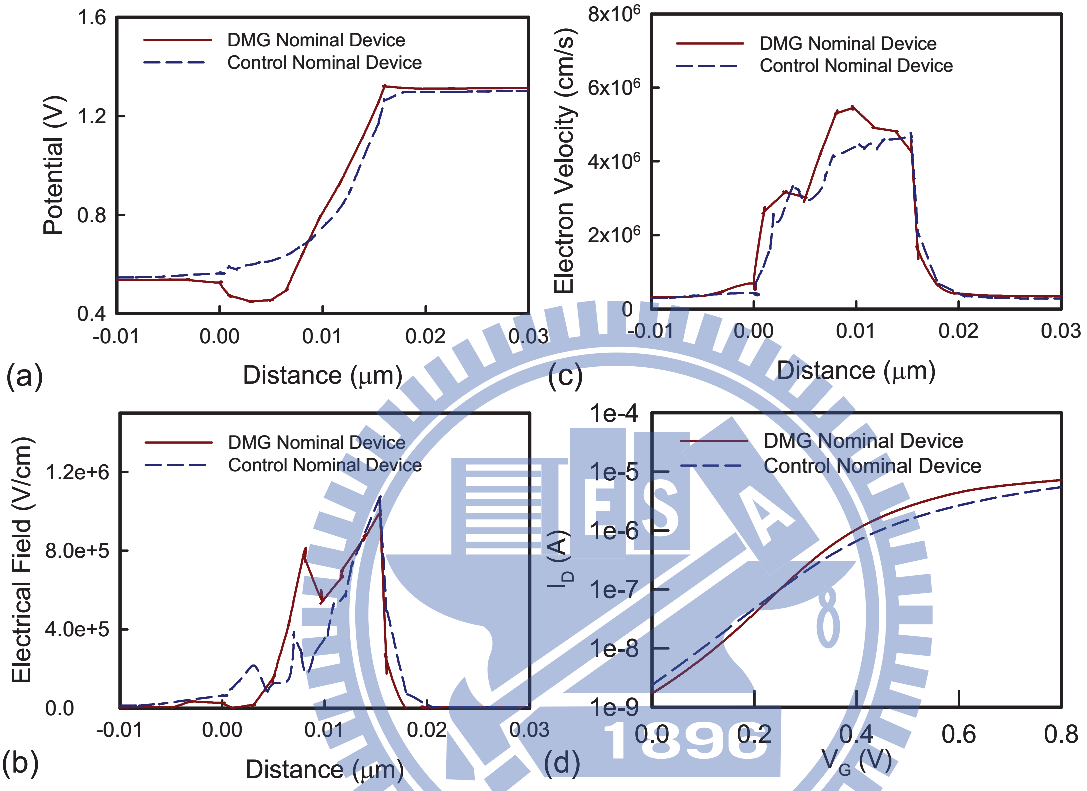


Figure 4.6: Comparison of nominal (a) surface potential, (b) lateral electric field, (c) electron velocity, and (d) $I_D - V_G$ curve for DMG device and control devices.

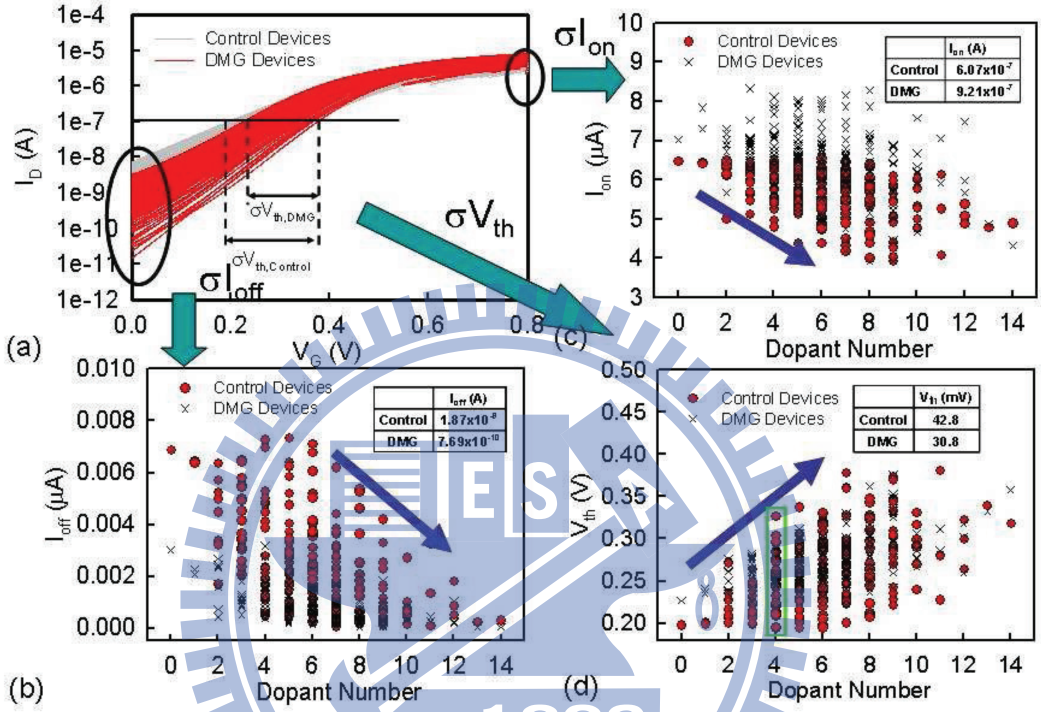


Figure 4.7: (a) Comparison of discrete-dopant-fluctuated $I_D - V_G$ curves of DMG device (red line) and control device (gray line). (b) I_{off}, (c) I_{on}, and (d) V_{th} fluctuations which extracted from (a).

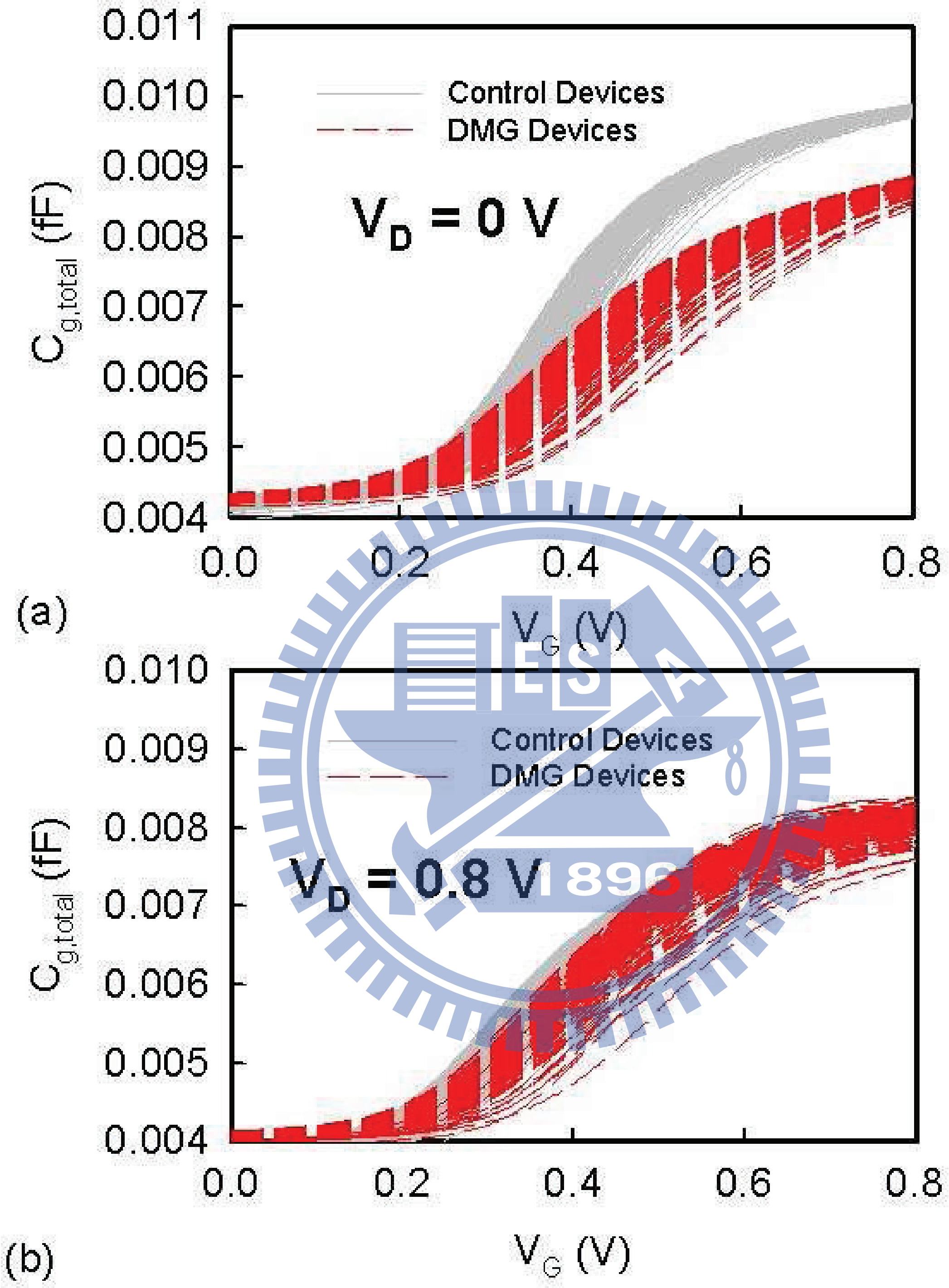


Figure 4.8: The $C_G - V_G$ characteristics of the 216 discrete-dopant-fluctuated control and DMG devices with (a) zero volt drain bias and (b) 0.8 volt drain bias voltage. The gray solid lines indicate the control devices and red dash lines are the DMG devices.

4.2 Characteristic Fluctuations of Lateral Asymmetric Channel Device

In this section, to further suppress the discrete-dopant-induced V_{th}, C_g, as well as dynamic characteristic fluctuations, the discrete-dopant fluctuated transistors are classified into the lateral asymmetric channel (LAC) and inverse LAC (inLAC) devices for the studying of the asymmetry sketch of characteristics fluctuations. Then, a lateral asymmetry doping profile is implemented to examine the associated fluctuation suppression technique.

4.2.1 Characteristic Fluctuations in Asymmetric Device

The dependence of C_g on different V_D is explored in Chap. 2 and motivates the design of lateral asymmetry doping profile along the source-drain direction. In this subsection, we examined the fluctuations of gate capacitance induced by random dopants for LAC and inLAC devices. At first, we generate 432 discrete-dopant-fluctuated transistors exploiting similar approach, as shown in Fig. 2.3, and classify them into two groups according to the random distribution of discrete dopants: the cases of dopants near the source-end and the drain-end , as shown in Fig. 4.9, where the inset describes the selection criteria. To strengthen and make the phenomenon clearly, the difference of dopant numbers near the source-end and the drain-end must be larger than two. There are 216 LAC device and 216 inLAC devices. For the LAC device, the selection criterion is that device has more than three dopants in the near-source-end channel but with zero or one dopant locating near the other end. The inLAC devices are then selected accordingly. The effect of LAC and inLAC on fluctuations of gate capacitances is then examined. For the devices with V_D = 0 V, Fig. 4.10(a) presents the average total gate capacitance versus the gate bias for the LAC and inLAC, respectively. Both the cases of dopants near the source-end and the drain-end exhibit a quite similar C-V characteristics under V_D = 0 V and V_D = 0.8 V, as shown in Fig. 4.10(b). Though the total C-V characteristics of the two groups are very similar, the fluctuation of the total C-V curves is outright different, as shown in Figs. 4.11(a) and 4.11(b). For devices are with V_D = 0 V, as shown in Fig. 4.11(a), both devices of LAC and inLAC exhibit resembling characteristic fluctuation. However, for devices are at bias of V_D = 0.8 V, as shown in Fig. 4.11(b), the $C_{g,total}$ fluctuation ($\sigma C_{g,total}$) of the LAC devices show a significantly large fluctuation, compared with the inLAC devices. Therefore, the corresponding C_{gd} fluctuation (σC_{gd}) and C_{gs} fluctuation (σC_{gs}) of devices with V_D = 0 V and 0.8 V are further calculated. The σC_{gd} and σC_{gs} of devices with V_D = 0 V, as shown in Fig. 4.12, indicate that the σC_{gs} is more pronounced and becomes major source of fluctuation for the LAC devices. Similarly, the σC_{gd} dominates the fluctuation of gate capacitance for the inLAC device. The random dopants located near the source-end or the drain-end in the devices' channel exhibits different C_{gd} and C_{gs} characteristics in spite of the same $C_{g,total}$

and $\sigma C_{g,total}$. Notably, since the drain bias will induce different characteristics in C_{gd} and C_{gs}, as discussed in chapter 3. The fluctuations of C_{gd} and C_{gs} for devices with V_D = 0.8 V are calculated, as shown in Fig. 4.13; for device under strong drain bias, the fluctuation of C_{gd} is significantly reduced, as shown in Fig. 4.13(a), compared with the result of Fig. 4.12(a). On the contrary, the fluctuation of C_{gs}, as shown in Fig. 4.13(b), is increased, in contrast with the result of Fig. 4.12(b). We observe that the fluctuation of C_{gd} is below 0.1 aF, as shown in Fig. 4.13(a). Therefore, for inLAC devices, since the major source of fluctuation is contributed by C_{gd}, the $\sigma C_{g,total}$ is well controlled. However, for the LAC devices, the major source of fluctuation, that is the fluctuation of C_{gs}, could not be reduced.

Besides the fluctuation of various components of gate capacitance, we further compare the discrete-dopant-induced $I_D - V_G$ characteristic fluctuations of LAC device which has high channel concentration near the source-end [85] and the inLAC device which has high channel concentration near the drain-end, as shown in Fig. 4.14. The calculation of threshold voltage here is as same as aforementioned in Chap. 2, determined from a current criterion for the drain current larger than 10^{-7} (W/L) ampere, as marked in Fig. 4.14. Then the inset tables of Figs. 4.14(a) and 4.14(b) list their nominal value and normalized variations. Notably, the V_{th} of the proposed inLAC device is 1.78 times smaller than the LAC device because of the smaller fluctuation of injection velocity and thus a smaller current variation for dopants located near the drain-end of the channel. The normalized I_{on}, I_{off}, and

g_m variations of inLAC device are 6.9%, 66%, and 2.3% and they are smaller than those of inLAC device, 13%, 88.3%, and 3.2%. Therefore, the comparison of DC characteristic fluctuations between the inLAC and control device are further examined, as displayed in Fig. 4.15. The "×" and "o" indicate the distribution of DC characteristics versus the dopant number for the inLAC and control devices, where the doping profiles of the inLAC devices have been illustrated in Figs. 2.7 and 2.8. The inset tables of Figs. 4.15(b)-(d) indicate the DC characteristic fluctuations (σV_{th}, σI_{on}, and σI_{off}) for inLAC and control devices. The σV_{th}, and σI_{on}, σg_m significantly reduced from 42.8 mV, 0.61 μA, and 0.421 μS to 28.5 mV, 0.41 μA, and 0.371 μS, respectively. However, the fluctuation of I_{off} is still large, as shown in Fig. 4.15(b), due to the weakened channel controllability, compared with the control device with original doping profile. Therefore, analog circuits, as shown in Fig. 2.9 and 2.10, using the proposed inLAC device is implemented and compared with planar MOSFETs (where the MOSFETs are with symmetric channel doping) to estimate the current mismatch and dynamic characteristic fluctuations, respectively.

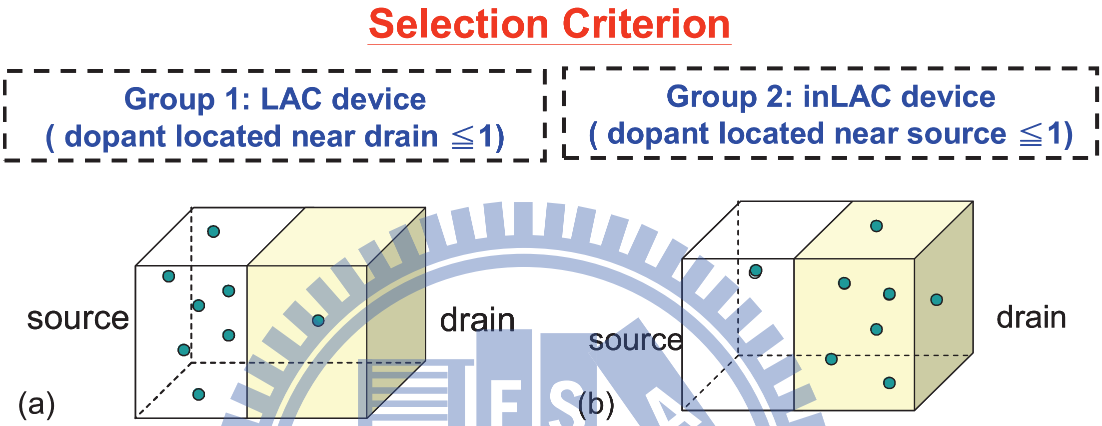


Figure 4.9: The discrete dopant fluctuated devices are then classified into two groups: (a) LAC devices with dopants near source end and (b) inLAC devices with dopants near drain end. For the LAC device, the selection criterion is that device has more than three dopants in the near-source-end channel but with zero or one dopant locating near the other end. The inLAC devices are then selected accordingly.

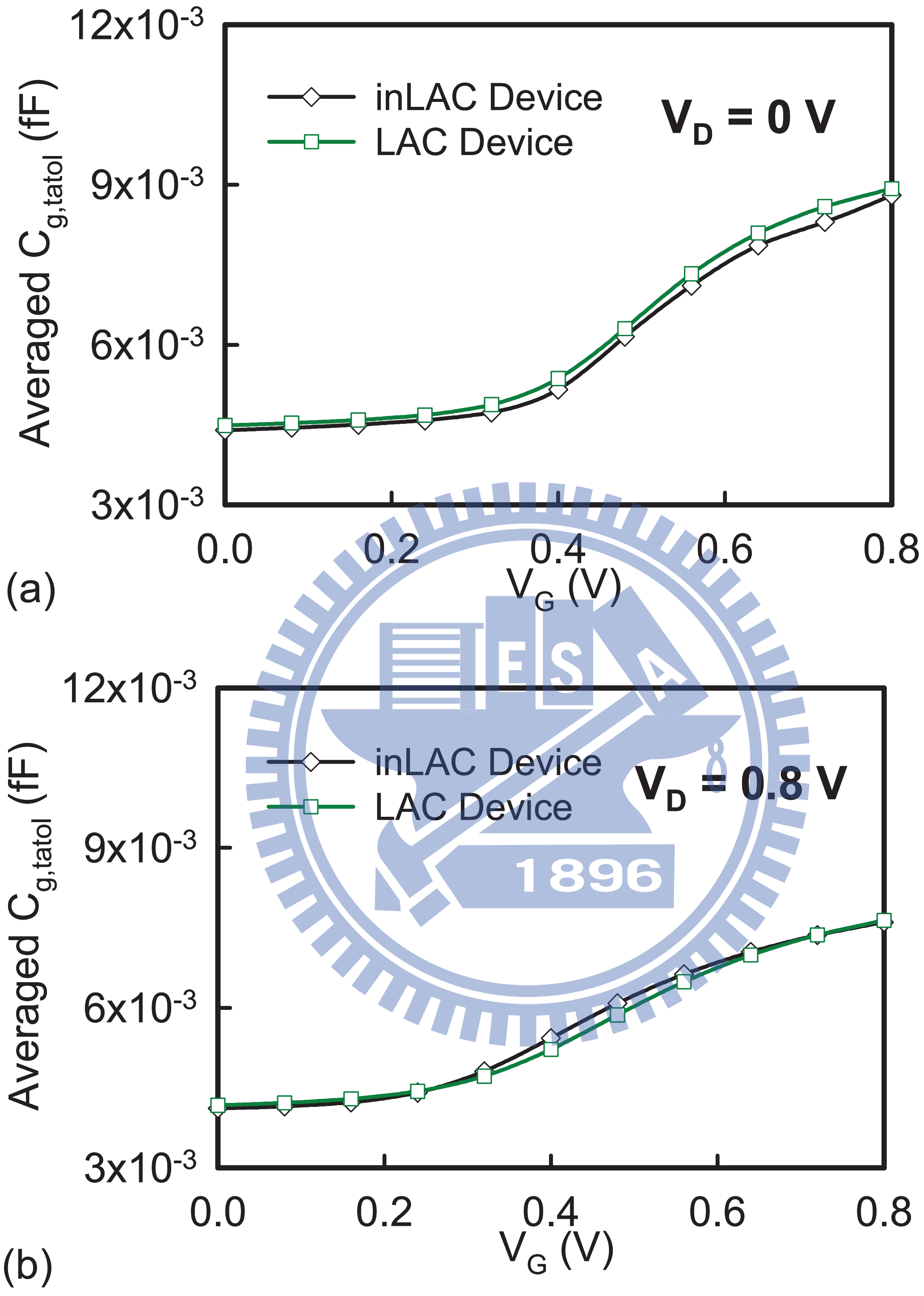


Figure 4.10: The Averaged of total gate capacitance ($C_{g,total}$) for LAC and inLAC devices at (a) V_D = 0 V and (b) V_D = 0.8 V.Both LAC and inLAC devices exhibit a quite similar C-V characteristics under V_D = 0 V and V_D = 0.8 V.

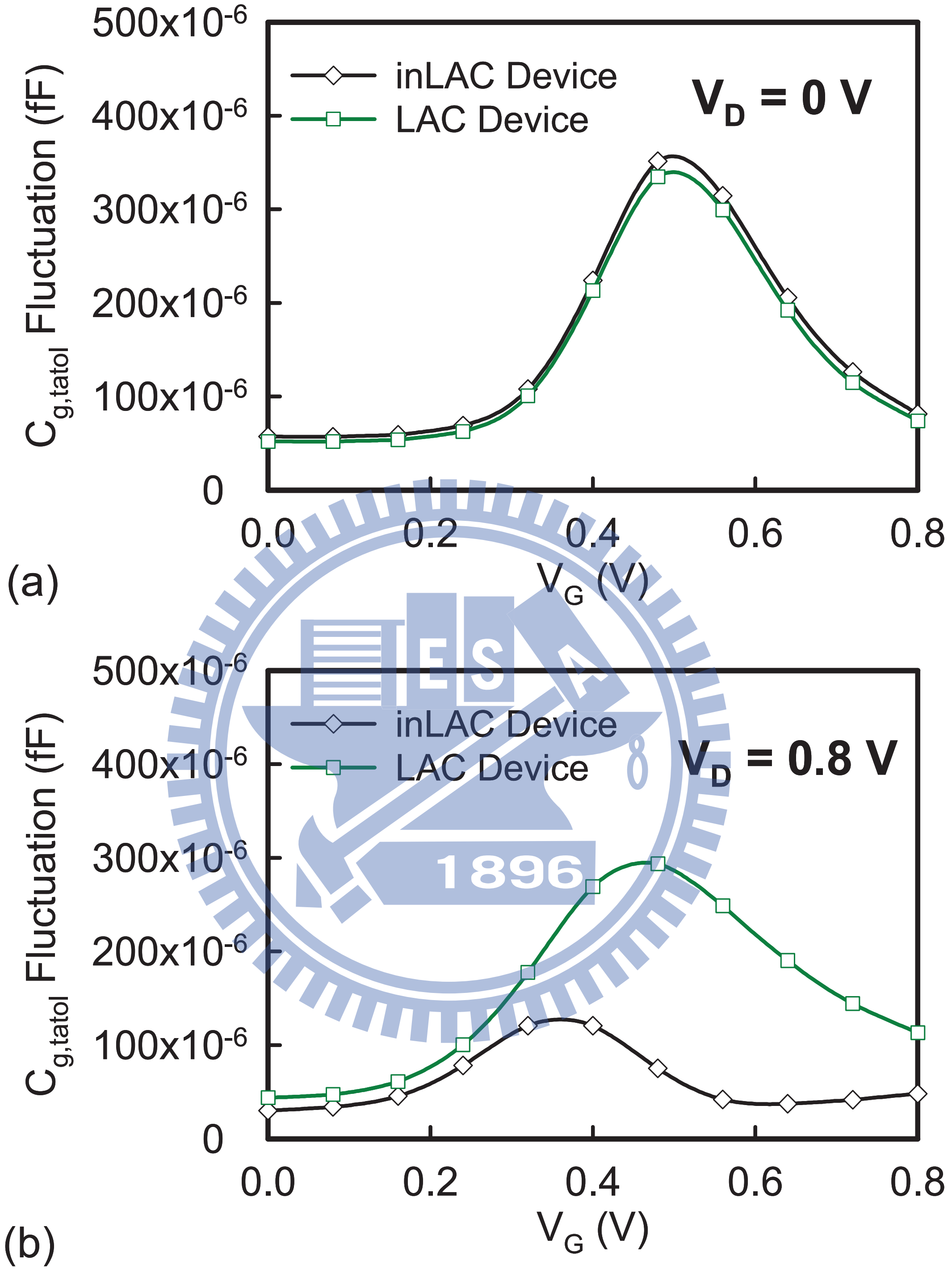


Figure 4.11: Fluctuations of total gate capacitance for LAC and inLAC devices at (a) $V_D = 0$ V (b) $V_D = 0.8$ V. The $\sigma C_{g,total}$ of the LAC devices show a significantly large fluctuation as compared to the inLAC devices at $V_D = 0.8$ V.

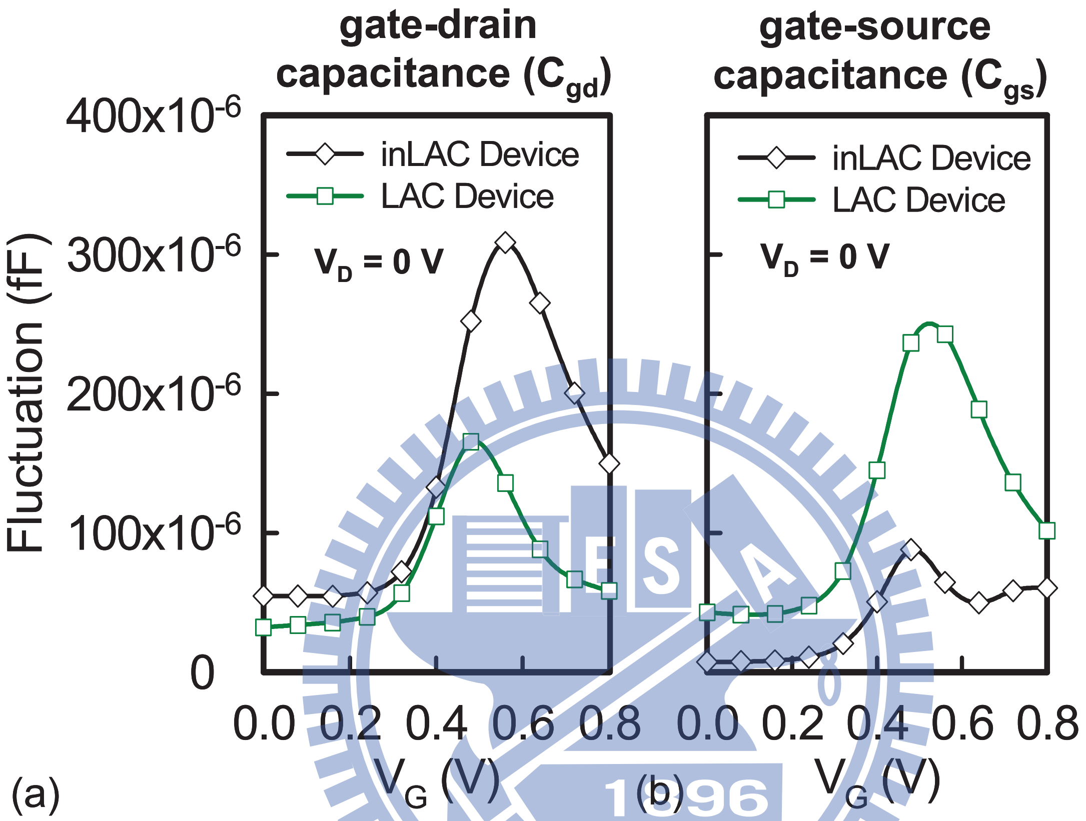


Figure 4.12: Fluctuations of (a) C_{gd} and (b) C_{gs} at $V_D = 0$ V. The σC_{gs} is more pronounced and becomes major source of fluctuation for the LAC devices. Similarly, the σC_{gd} dominates the fluctuation of gate capacitance for the inLAC device.

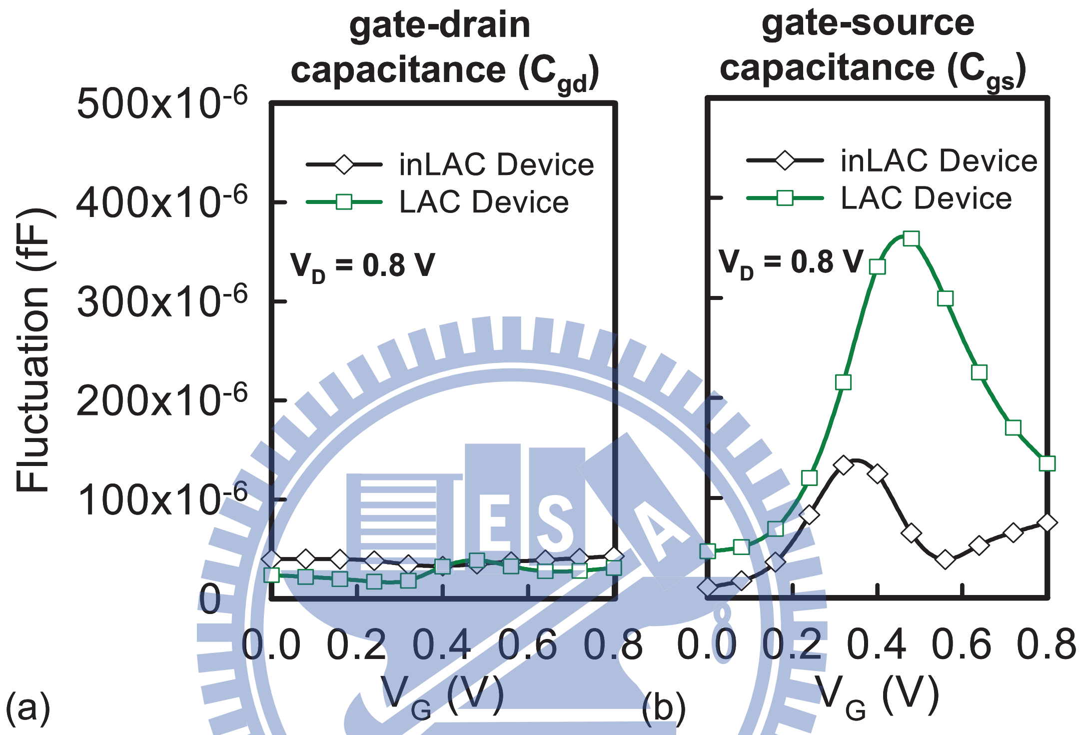
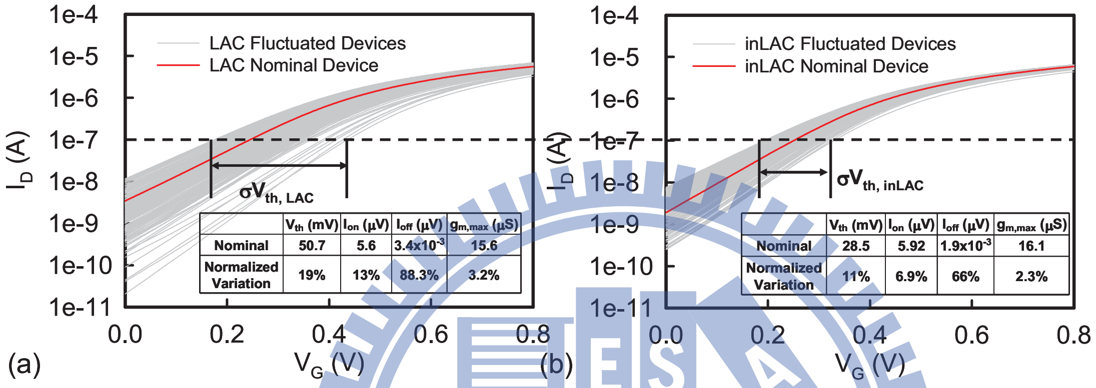


Figure 4.13: Fluctuations of (a) C_{gd} and (b) C_{gs} at V_D = 0.8 V. For inLAC devices, since the major source of fluctuation is contributed by C_{gd}, the $\sigma C_{g,tatol}$ is well controlled. For the LAC devices, the major source of fluctuation, that is the σC_{gs}, could not be reduced.



	V_{th} (mV)	I_{on} (μV)	I_{off} (μV)	$g_{m,max}$ (μS)
Nominal	50.7	5.6	$3.4\text{x}10^{-3}$	15.6
Normalized Variation	19%	13%	88.3%	3.2%

	V_{th} (mV)	I_{on} (μV)	I_{off} (μV)	$g_{m,max}$ (μS)
Nominal	28.5	5.92	$1.9\text{x}10^{-3}$	16.1
Normalized Variation	11%	6.9%	66%	2.3%

Figure 4.14: The discrete-dopant-induced $I_D - V_G$ characteristic fluctuations of (a) LAC and (b) inLAC devices, respectively. The σV_{th} of inLAC device is 1.78 times smaller than LAC device because of the smaller fluctuation of injection velocity and thus a smaller current variation for dopants located near the drain-end of the channel.

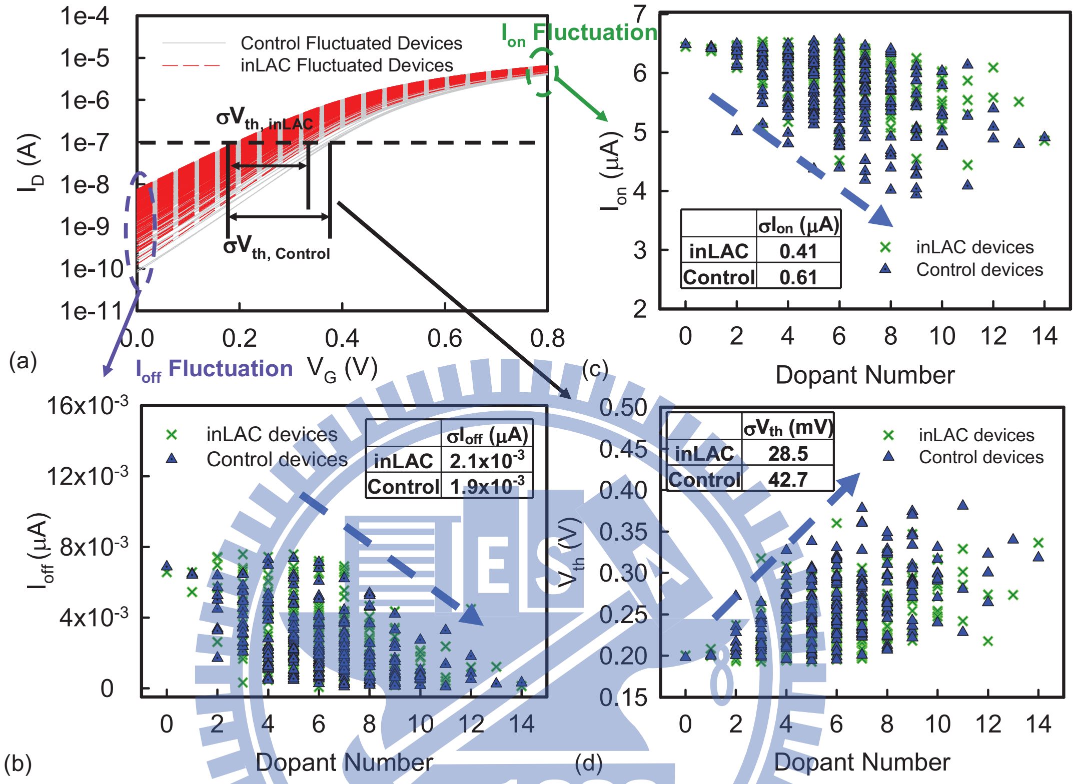


Figure 4.15: (a) The comparison of $I_D - V_G$ characteristics, where the solid lines show the control devices and the dashed lines are inLAC devices, respectively. The DC characteristic fluctuations of, (b) I_{off}, (c) I_{on}, and (d) V_{th}, where the triangle symbols show the control devices and the cross symbols are inLAC devices, respectively.

4.2.2 Characteristic Fluctuations in Analog Circuits

This subsection presents the implication of device variability in analog circuits. At first, we compared current mismatch between control and inLAC device in current mirror circuit. Based upon the V_{th} is significantly suppressed form 43.3 mV and 28.5 mV for NMOS devices, the normalized I_{OUT} fluctuation of the studied circuits caused by random dopants is reduced to 4.66$\%$, as shown in Fig. 4.16. To disclose the suppression more clearly, the I_{REF} corresponding to I_{OUT} for each discrete-dopant-induced fluctuated device of control and inLAC devices are explored in Fig 4.17, respectively. The solid symbols indicated the control device and open symbols are inLAC devices. The I_{OUT} of inLAC devices is 1.74 times smaller than the current mirror with control devices. Comparing dynamic characteristic fluctuations between the inLAC and LAC devices are then examined in Fig. 4.18. The inLAC device exhibits better immunity against RDF. The fluctuations of calculated quantities are summarized in inset of Fig. 4.18, where the horizontal ratio is calculated by Ratio = fluctuation of LAC devices / fluctuations of inLAC devices. The inset shows the fluctuation ratio of circuit gain, 3dB bandwidth, and unity-gain bandwidth for LAC device which dopants located near the source-end are 1.59, 1.21, and 2.16 times larger than those of inLAC device with dopants near the drain-end. Therefore, the intrinsic output resistance (r_o), transconductance (g_m), gate capacitance, and dynamic characteristic fluctuations of the inLAC device and control device are further explored. Figure 4.19 shows the smaller

g_m and r_o fluctuation of inLAC device as compared with control device which meant less impact on magnitude of output signal and thus exhibits less the influence on circuit gain. Figure 4.20 explores the $C_G - V_G$ characteristics of the discrete-dopant fluctuated inLAC (dashed lines) and the original (solid lines) devices, respectively. The spreading range of the lateral asymmetry doping profile is reduced, which implies the suppression of C_g and dynamic characteristic fluctuations, as marked in Fig. 4.20. The high-frequency response of the nano-MOSFET circuit is then studied in Fig. 4.21(a), where the solid lines are control devices and the dashed lines show the inLAC devices. The spreading range of the inLAC devices is reduced significantly due to the suppression of r_o, g_m, and C_g. As shown in Figs. 4.21(b)-4.21(d), the high frequency characteristic fluctuations of the circuit gain, the 3dB bandwidth, and the unity-gain bandwidth are reduced by 31.2%, 37.6% and 47% for inLAC device, respectively. Notably, since the g_m and C_g are factors of circuit gain, 3dB bandwidth and unity-gain bandwidth, the dynamic characteristics have similar fluctuation suppression.

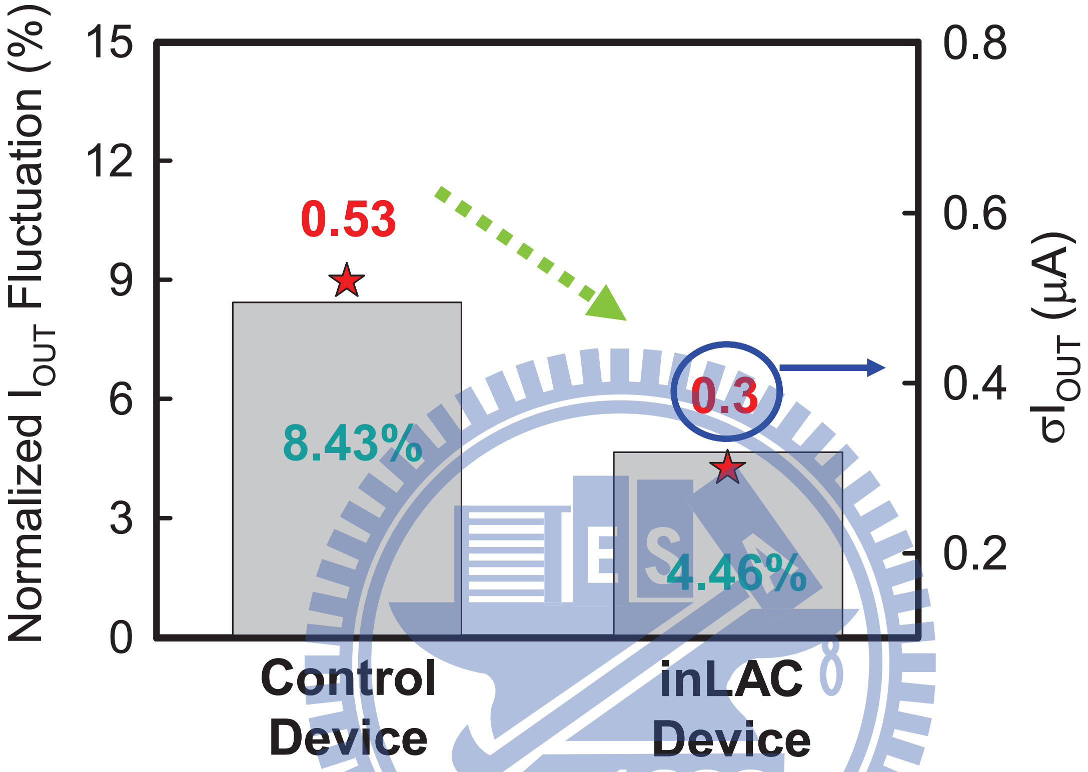


Figure 4.16: The I_{OUT} fluctuation (σI_{OUT}) and normalized I_{OUT} fluctuations for the studied current mirror circuit with control device and inLAC device, respectively, where the normalized I_{OUT} fluctuations are defined by standard deviation of absolute difference of I_{OUT} and I_{REF} divide by I_{REF}.

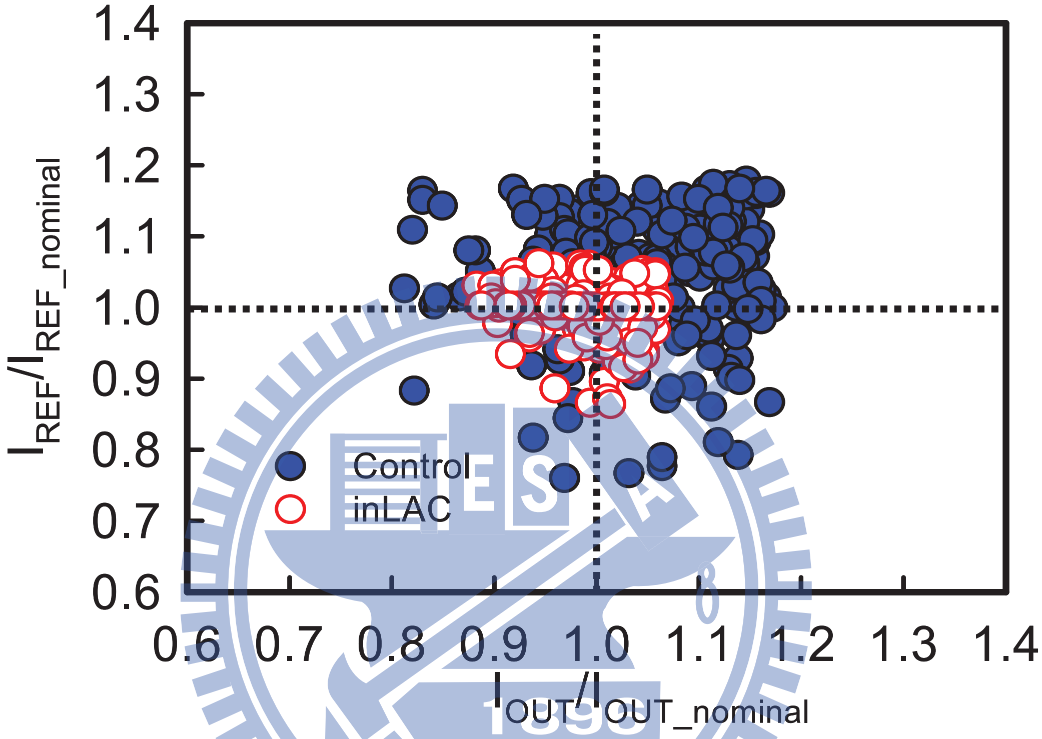


Figure 4.17: The scatter plots for comparing the current mirror current with control devices (filled-in blue symbols) and inLAC (open symbols) devices, respectively.

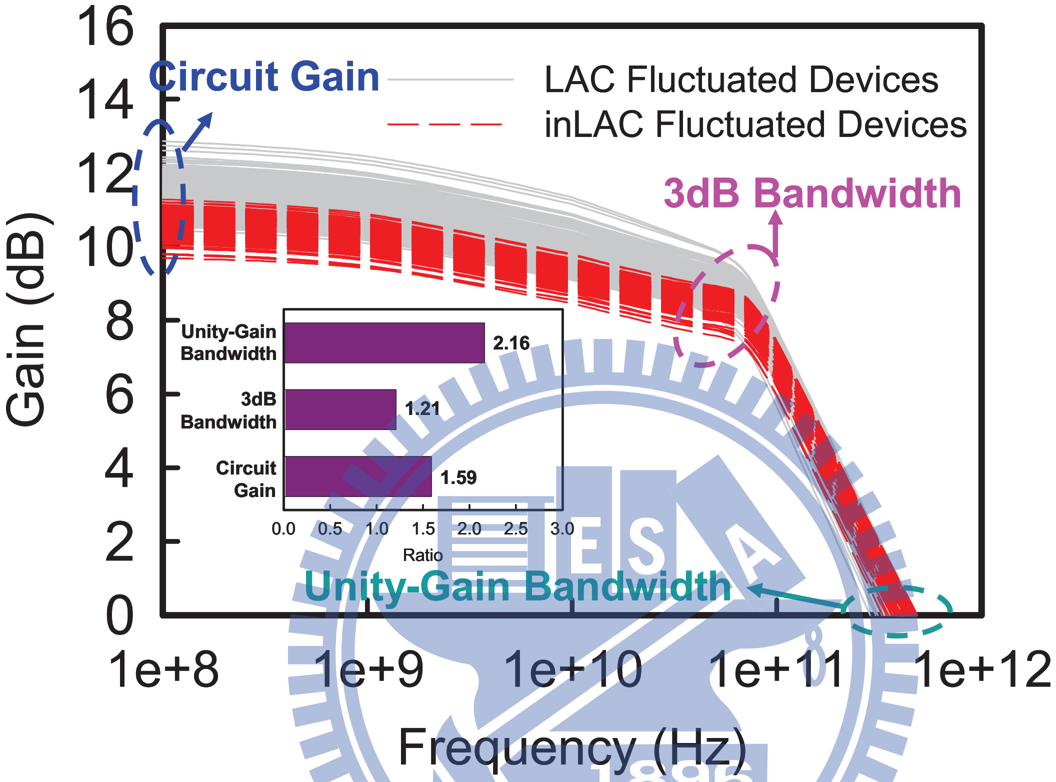


Figure 4.18: High frequency response of the studied circuits. The solid lines are the results of inLAC devices and the dash lines are for the results of LAC devices. The inset is comparison of different fluctuation components between the studied two group devices.

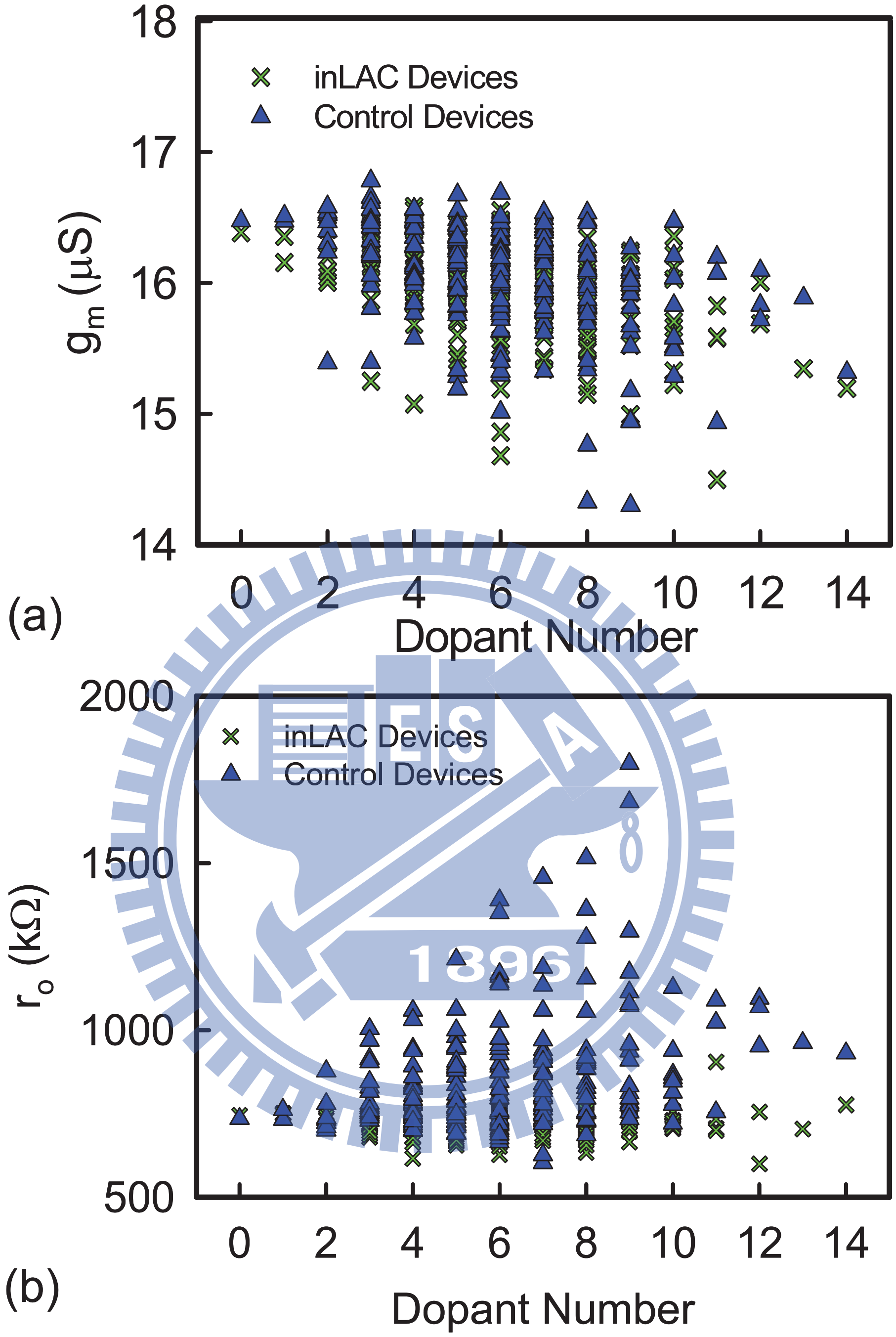


Figure 4.19: DC characteristic fluctuation of (a) g_m and (b) r_o between control and inLAC devices. As the dopant number is increased, the devices V_{th} is increased and thus increased ro and decreases transconductance. The triangle symbols show the control devices and the cross symbols are inLAC devices, respectively.

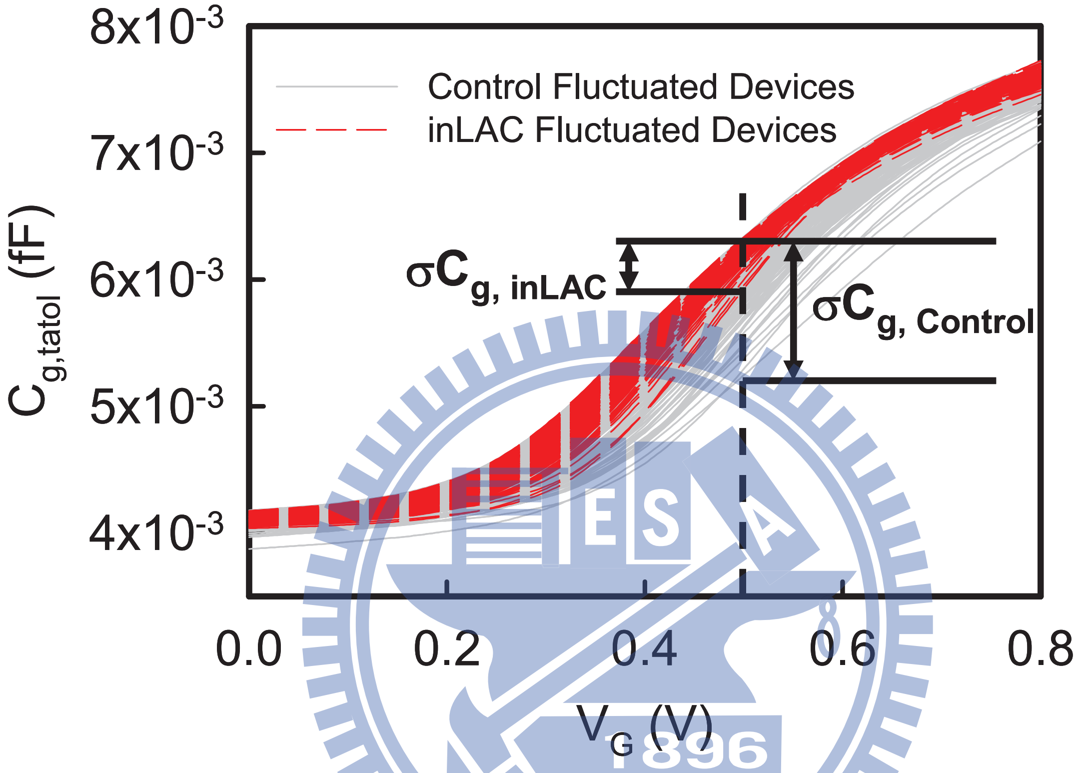


Figure 4.20: Comparison of gate capacitance fluctuations of the discrete-dopant-fluctuated 16-nm-gate devices generated from the proposed inLAC devices (dashed line) and control device (solid line).

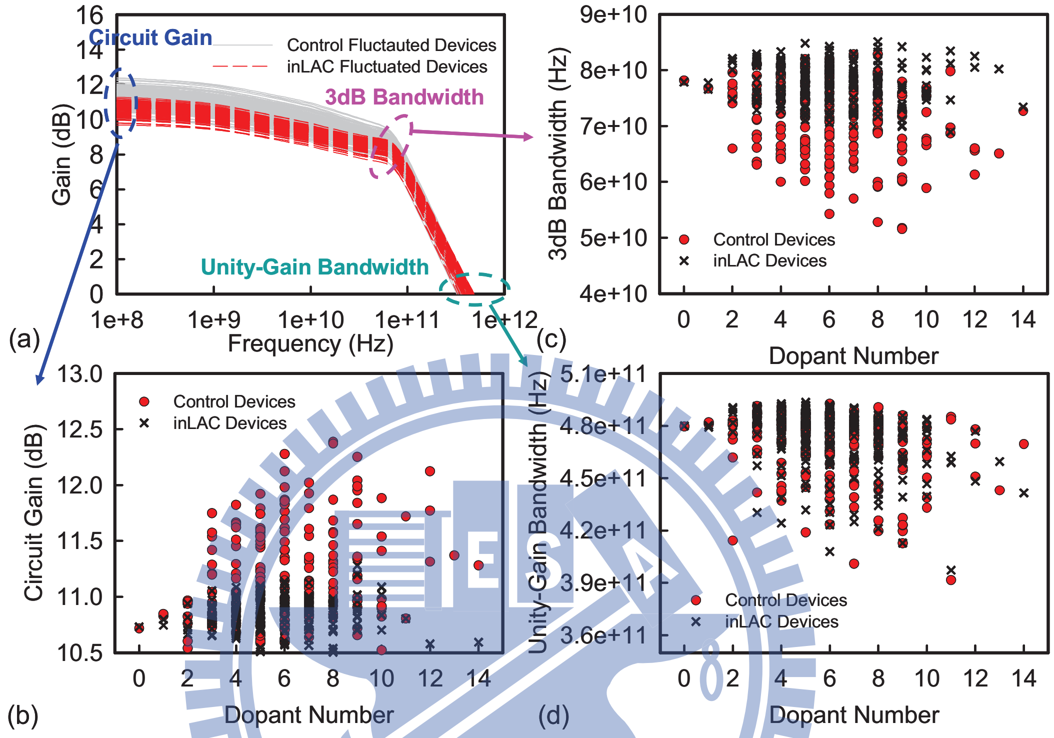


Figure 4.21: Comparison of (a) frequency response fluctuations, (b) circuit gain, (c) 3dB bandwidth, (d) and unity-gain bandwidth fluctuations of the 216 discrete-dopant fluctuated 16-nm-gate planar MOSFET circuit with inLAC and control devices. The circle symbols show the control devices and the cross symbols are inLAC devices, respectively.

4.3 Summary of this Chapter

In this chapter, we have presented two techniques to suppress RDF-induced characteristics fluctuation. For the DMG device, the dopant will induce relatively small potential deviation in DMG due to a large initial potential barrier existed (ϕ_{dopant}/ϕ_H, compared with ϕ_{dopant}/ϕ_L and ϕ_{dopant}/ϕ_M) in the cross-sectional view of potential energies for dopant near the source side. However, the same suppression of AC characteristic fluctuations can not enjoy the advantage of DMG device because the capacitance of depletion region is affected by doping distribution of channel region and effective oxide thickness. Therefore, the inLAC device was proposed to suppress AC characteristics sequentially. The inLAC device has exhibited less characteristic fluctuations due to the well controlled of major fluctuation source of C_{gd}. Moreover, in contrast to the control device, the fluctuations of V_{th}, I_{on}, g_m, r_o, C_g, circuit gain, 3dB bandwidth, and unity-gain were simultaneously reduced by 33.4$\%$, 32.8$\%$, 11.9$\%$, 80.6$\%$, 68.8$\%$, 31.2$\%$, 37.6$\%$ and 47$\%$, respectively.

PART B

Design Optimization of TFT-LCD ASG Driver Circuit

Chapter 5

Optimization Technique

In this chapter, the evolutionary algorithm, genetic algorithm and implemented simulation-based optimization method is introduced. At first, we give a brief introduction of the evolutionary algorithm, genetic algorithm (GA), in this work. Then we show the algorithm scheme of the solver to optimize the tested amorphous silicon gate (ASG) driver circuits in Chap. 6.

5.1 Genetic Algorithm

GA is a kind of evolutionary algorithms which are based on simple concepts inspired by the evolutionary biology theory such as selection, crossover, mutation, and so on [62-65,86,87]. GA works with a population of individuals which evolve from one generation to next one. This evolution is able to search all the possible solutions by totally exploring the searching space and lead us to find the global solution of the optimization problem. Generally, GA includes the following parts as shown in Fig. 5.1; each of the components must be specified in order to define a particular GA.

1. Representation;
2. Evaluation;
3. Population;
4. Parent Selection mechanism;
5. Variation Operator;
6. Survivor selection mechanism; and
7. Initialization Procedure and Terminal. Condition

As for the representation, it is the method to link the "real world" to "GA world". The possible solution of real world will be "encoded" to the specified form which is called chromosome and usually represents a candidate solution. Evaluation forms the basis for selection. Usually, specific fitness function depending on the problems of the candidates will be calculated and provide the information to the selection mechanism. Parent selection mechanism is to choose better candidates which will be sent in the mating pool and thus variation operators are applied on them. There are two critical variation operators in GA: recombination and mutation. The basic idea of recombination is inheriting information from two parents, and mutation is supposed to cause a random, unbiased change. The offspring will be created after applied variation operators on the candidates in the mating pool. After that, the survivor selection mechanism which is similar to parent selection but used in the different stage of GA is enabled. Age factor is also usually considered in this selection. If no survivor achieves the desired targets, the process repeats until a specified number of generations.

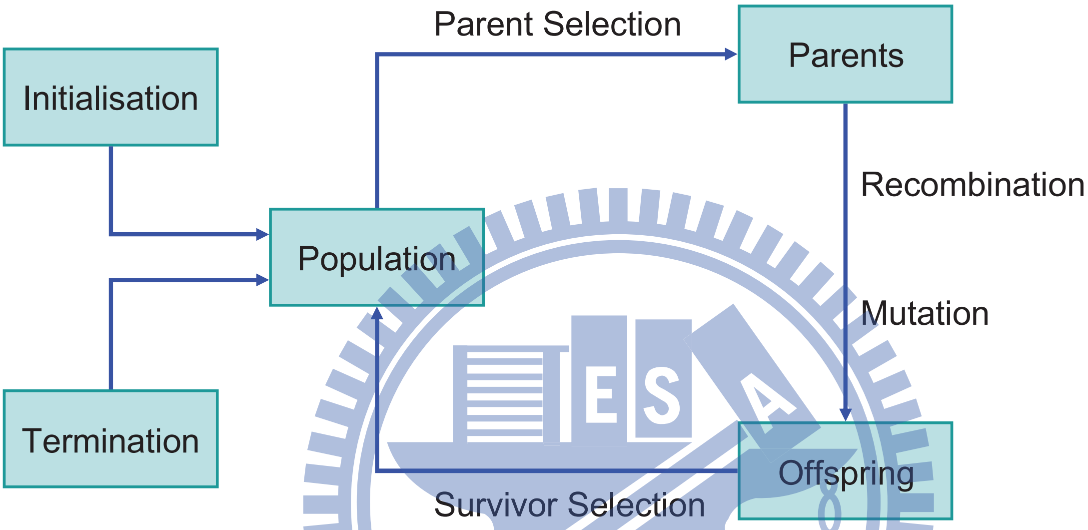


Figure 5.1: The general scheme of an evolutionary algorithm consist of population, parent selection mechanism, variation operator, survivor selection mechanism, initialization procedure and terminal condition .

5.2 Variation of Operator in the Genetic Algorithm

After selection step, the crossover operator is used to generate the next generation solution. According to crossover probability and crossover strategy, the crossover operator generates the offspring from two parent individuals chosen from the population by selection. The offspring will substitute their parents in the next populations and may result better fitness score based upon an appropriate crossover strategy. Generally, the crossover methods include one-point crossover [88,89], two-point crossover [88,89], and uniform crossover [64,88-90]. In this thesis, one-point crossover is used to optimize the proposed ASG driver circuit. The one-point crossover is randomly determine one crossover point, and the gene of the offspring from beginning to crossover point will be inherited by one parent individual, and the rest will be inherited by the other parent, as disclosed in Fig. 5.2(a).

After crossover operator, the mutation operator enables to randomly choose two gene in one individual and exchange them with mutation rate, as shown in Fig. 5.2(b). In addition, mutation operator is necessary to maintain genetic diversity to evaluate all the searching space and therefore avoid local optimal solution. The mutation rate is the probability of applying certain randomized change to an individual. Notably, the mutation rate is must be carefully determined. If the mutation rate is too high, it may interrupt the process and imply the loss of optimal solution. If the mutation rate is too low, the genetic diversity may not be increased and then sticks in the local optimal. More detail setting is discussed in the next subsection.

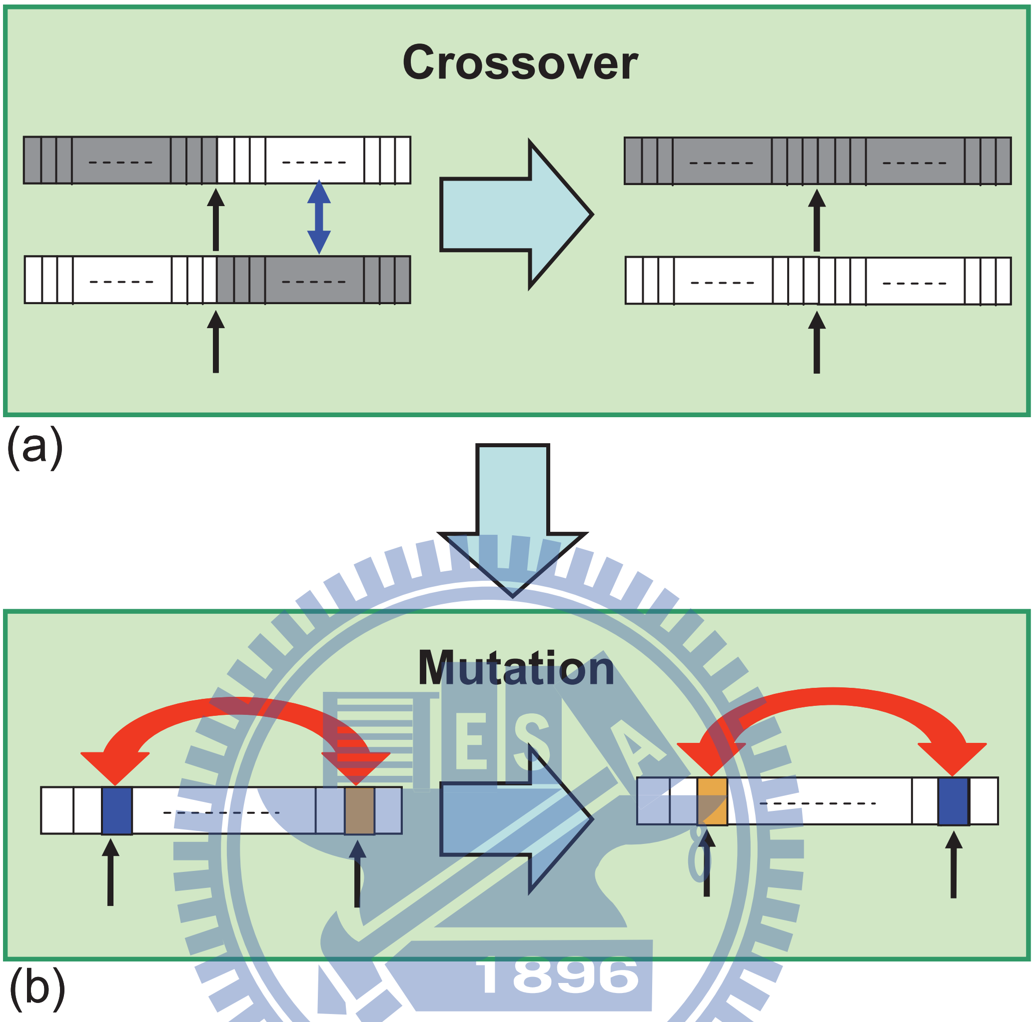


Figure 5.2: The variation operators, (a) crossover and (b) mutation, used in this work. For the crossover, we randomly choose one point and split two parents at the point, then we exchange the tails of them to create two offspring. After that, the mutation enable to randomly choose two gene in one individual and exchange them with mutation rate.

5.3 The Simulation-Based Optimization Methodology

5.3.1 The Optimization Flow

The unified optimization framework (UOF) [66] enables us to implement the optimization method to design ASG driver circuit with the most suitable parameters. The UOF can evolve the parameter configuration of circuit by genetic algorithm [64,86,87,91-93] and achieve particular performance of the circuit with the parameter configuration as fitness value by executing external circuit simulator [94-97]. The flow is shown in Fig. 5.3; for a script file of netlist depending on the ASG driver circuit topology, we define the parameters of ASG driver circuit to be optimized. Then, the initial population of these parameters is generated by engineering design or random selection. The evaluation mechanism is putting the parameters into script file to obtain the complete circuit netlist file, and then send the file into circuit simulator to acquire the circuit characteristics automatically. If the characteristics meet the requirement prescribed by the circuit designer, we output the final optimized solution. If the error between the specifications and characteristics does not meet the convergence criterion, the UOF performs GA to assess the designed parameters. The process will be iterated until the specifications are matched.

5.3.2 The Performance of Developed Optimization Methodology

The parameters setting of GA in circuit design optimization is summarized in Table 5.1. By considering the experiment, Figs. 5.4(a) and 5.4(b) show a comparison of the score convergence behavior among population sizes, where the crossover and mutation rate is fixed at 0.6. The fitness score versus the number of generation suggests that the score convergence behavior does not have a satisfied result if the population size is too small. According to our experience, the population size = 100 is good for the optimal design of ASG driver circuit. In addition, Figs. 5.5(a) and 5.5(b) show the fitness score convergence behavior for the circuit optimization with different mutation rate, where the population size = 100. The results suggest that the mutation = 0.6 keeps the population diversity and finally has better evolutionary results.

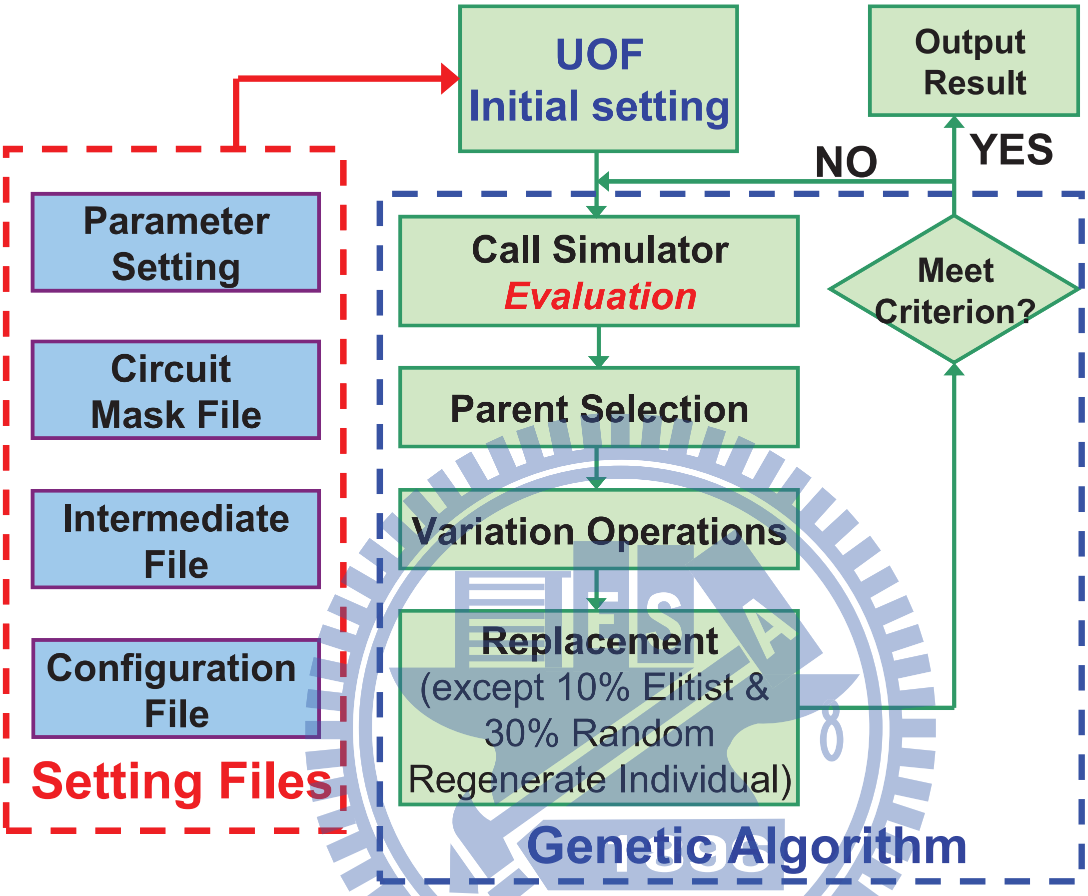


Figure 5.3: The algorithm scheme of the solver to optimize the proposed ASG driver circuits in this thesis.The replacement is age-based but with 10% elitist and 30% regenerate random individual. After replacement complete, we check whether the solution meets requirements or the max generation is reached.

Table 5.1: The parameters setting of genetic algorithm in our circuit design optimization experiments. The designed parameters of population size, crossover rate, and mutation rate are suitable for ASG driver circuits.

Parameters Setting of Genetic Algorithm	value
Population Size	100
Max Generation	100
Crossover Rate	0.6
Mutation Rate	0.6

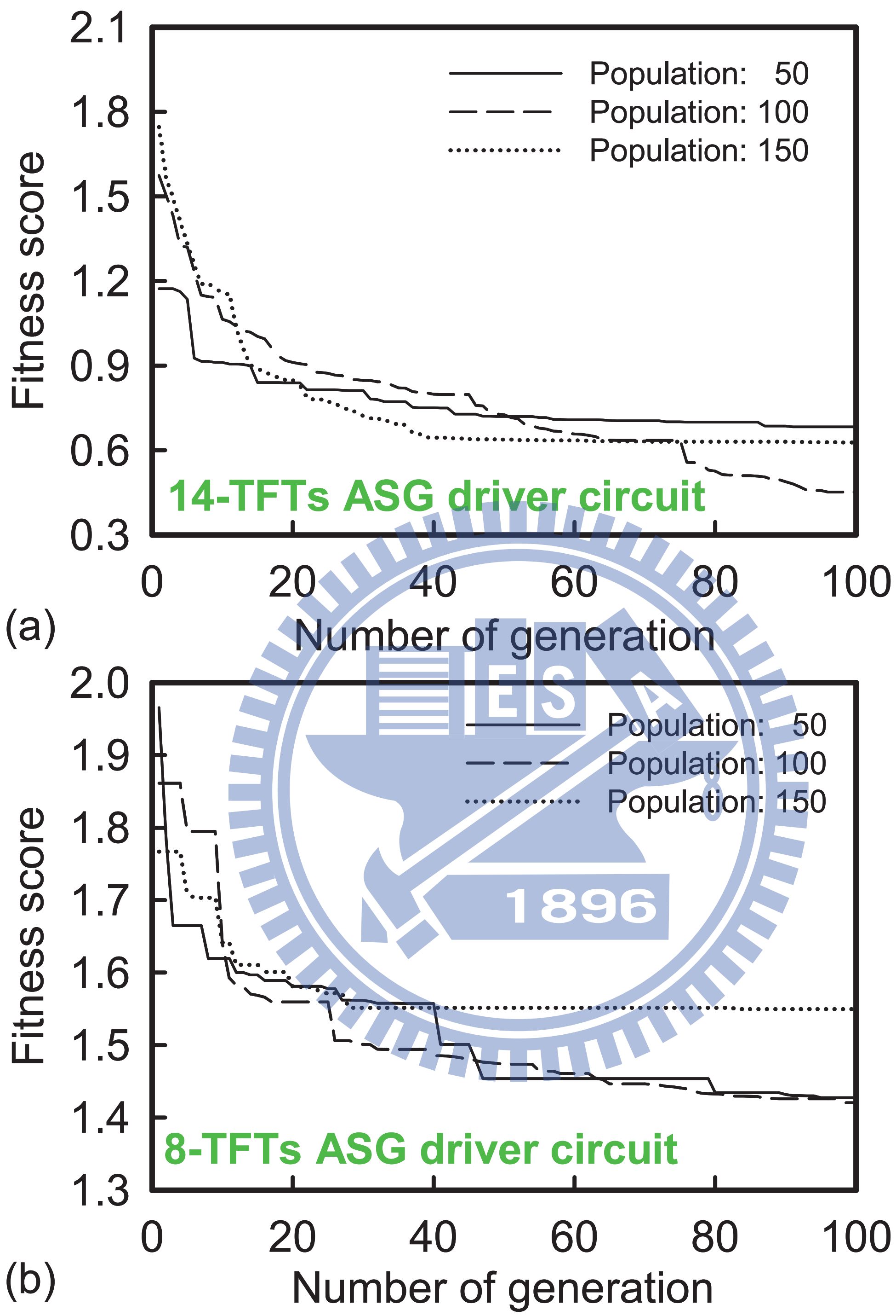


Figure 5.4: (a) and (b) The comparison of the score convergence behavior of the algorithm in two ASG driver circuits among population sizes are 50, 100, and 150, where the crossover and mutation rate is fixed at 0.6, respectively.

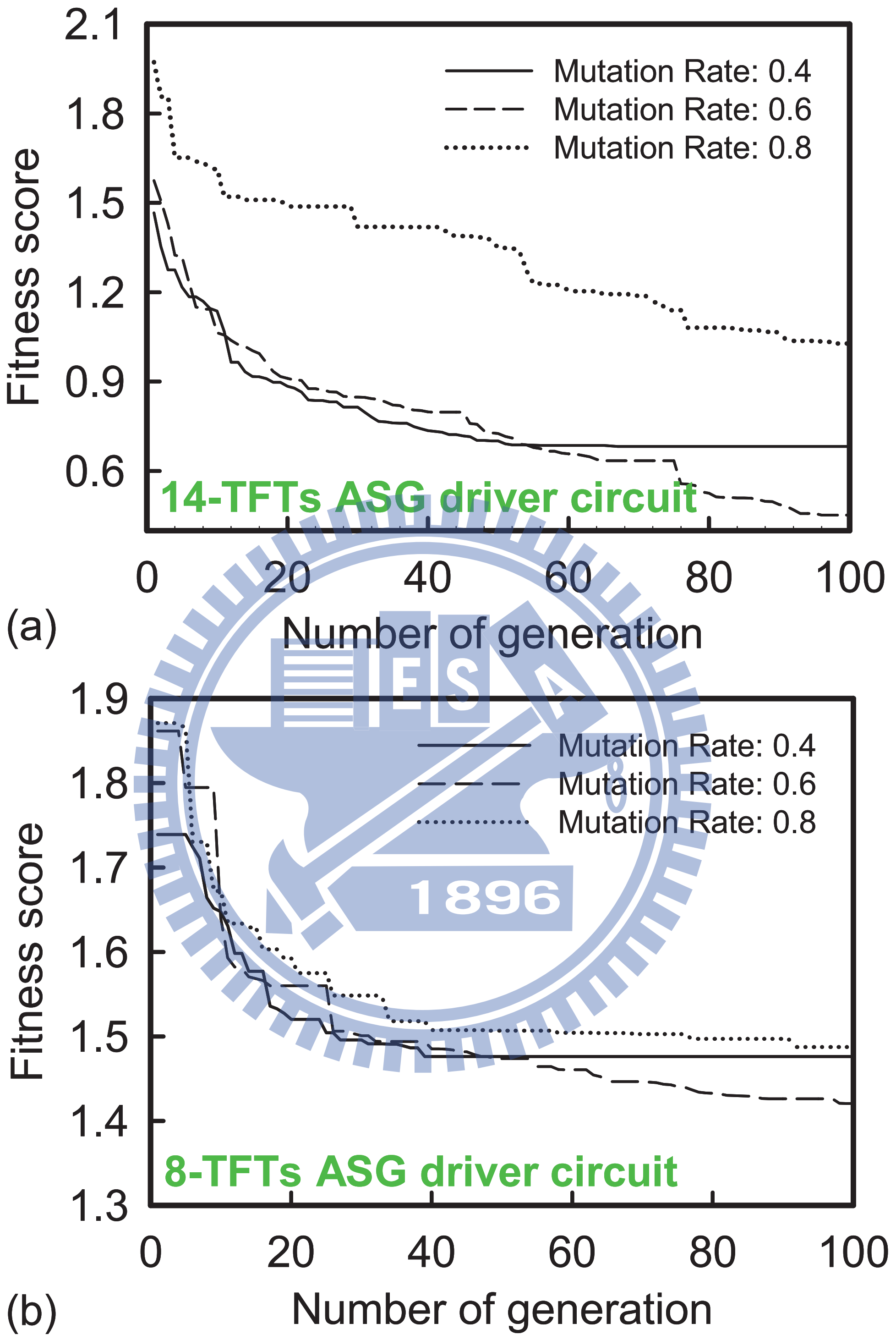


Figure 5.5: (a) and (b) The comparison of the score convergence behavior of the algorithm in two ASG driver circuits among mutation rates are 0.4, 0.6, and 0.8, where the crossover a is fixed at 0.6 and population size is fixed at 100, respectively.

5.4 Summary of this Chapter

The genetic algorithm was introduced briefly in this chapter. Then, detail implementation of optimization flow by UOF was also shown in this chapter. By considering the experiment, the parameters setting of GA, such as population sizes and mutation rate in circuit design optimization were then investigated.

Chapter 6

The ASG Driver Circuit and Simulation Results

In this chapter, the original and optimization simulation results of proposed amorphous silicon gate (ASG) driver circuits are discussed. At first, we brief the operation of explored ASG driver circuits. Then the numerical experiments for the proposed explored ASG driver circuits are realized and discussed. Finally, the sensitivity analysis verifies the characteristic variations of optimized circuits.

6.1 Operation of ASG Driver Circuit

The proposed ASG driver circuits are used for different products as compared with conventional one [94]. A schematic of active matrix liquid crystal display (LCD) panel controlled by ASG driver circuit in product is shown in Fig. 6.1(a); each stage ASG driver circuit consists of pull-up and pull-down control circuits, pull-up and pull-down output circuits, as show in Fig. 6.1(b). The output state, VGH, and rise time of output waveform are influenced by designed pull-up output circuit. The steady state, VGL, and fall time of output waveform are affected by designed pull-down output circuit, respectively. Figures. 6.2(a) and 6.3(a) show one stage circuit of the proposed ASG driver circuits used in different products and its timing diagram. The different between Fig. 6.2(a) and Fig. 6.3(a) is the Pull-up control circuit, Pull-down control circuit and Pull-down output circuit. The reason is that the ASG driver circuit with 14-TFTs used in large loading products such as monitor and screen of TV, whereas the ASG driver circuit with 8-TFTs used in display panel of cell phone, as disclosed in Figs. 6.2(b) and 6.3(b). Thus, the circuit of Fig. 6.2(a) needs more transistors than that of Fig. 6.3(a) to accelerate charge and discharge time. However, the function of two ASG driver circuits is almost the same. Then in these circuits' topologies, the CLK and CLKB denote the clock signal and clock bar signal; VGL is the steady state voltage, and STV/V_{n-1} is inputted pulse signal. The V_n and V_N are the output signal which supply for the panel and next stage, respectively. Fig. 6.4 shows timing diagram of ASG driver circuit with 14-TFTs and the operation of 14-TFTs-ASG driver circuit is as follows. When the input signal is high, the Q_1 node is charged by the input signal (STV/V_{n-1}); then, as CLK is changed from low to high, the Q_1 node voltage is boosted up due to the gate-drain capacitive coupling of M10. Therefore, the output driving ability (V_n and V_N) is achieved through M7 and M10. At this time, the high voltage of the Q_1 node is applied to the gates of M4 simultaneously. Therefore, M11 is turned off, and the high voltage is kept at the Q_1 node. After generating an output voltage, the Q_1 node voltage is discharged when the output signal of next stage (V_n) is applied to the gate of M12. After that, the Q_1 node is alternately discharged through M13 by using the CLKB signal.

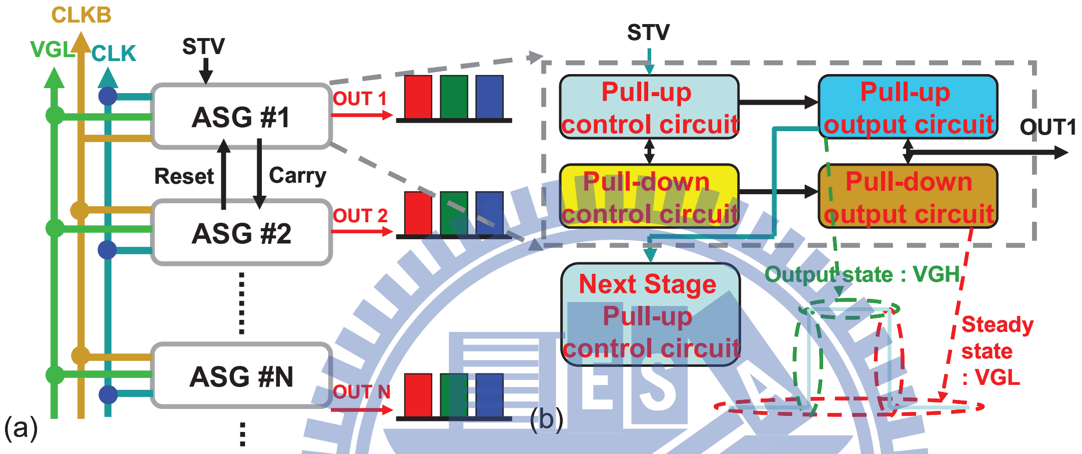


Figure 6.1: (a) The common schematic of active matrix liquid-crystal display panel controlled by ASG driver circuit in real product. (b) The components of one stage ASG driver circuit and the output waveform affected by corresponding component of ASG driver circuit.

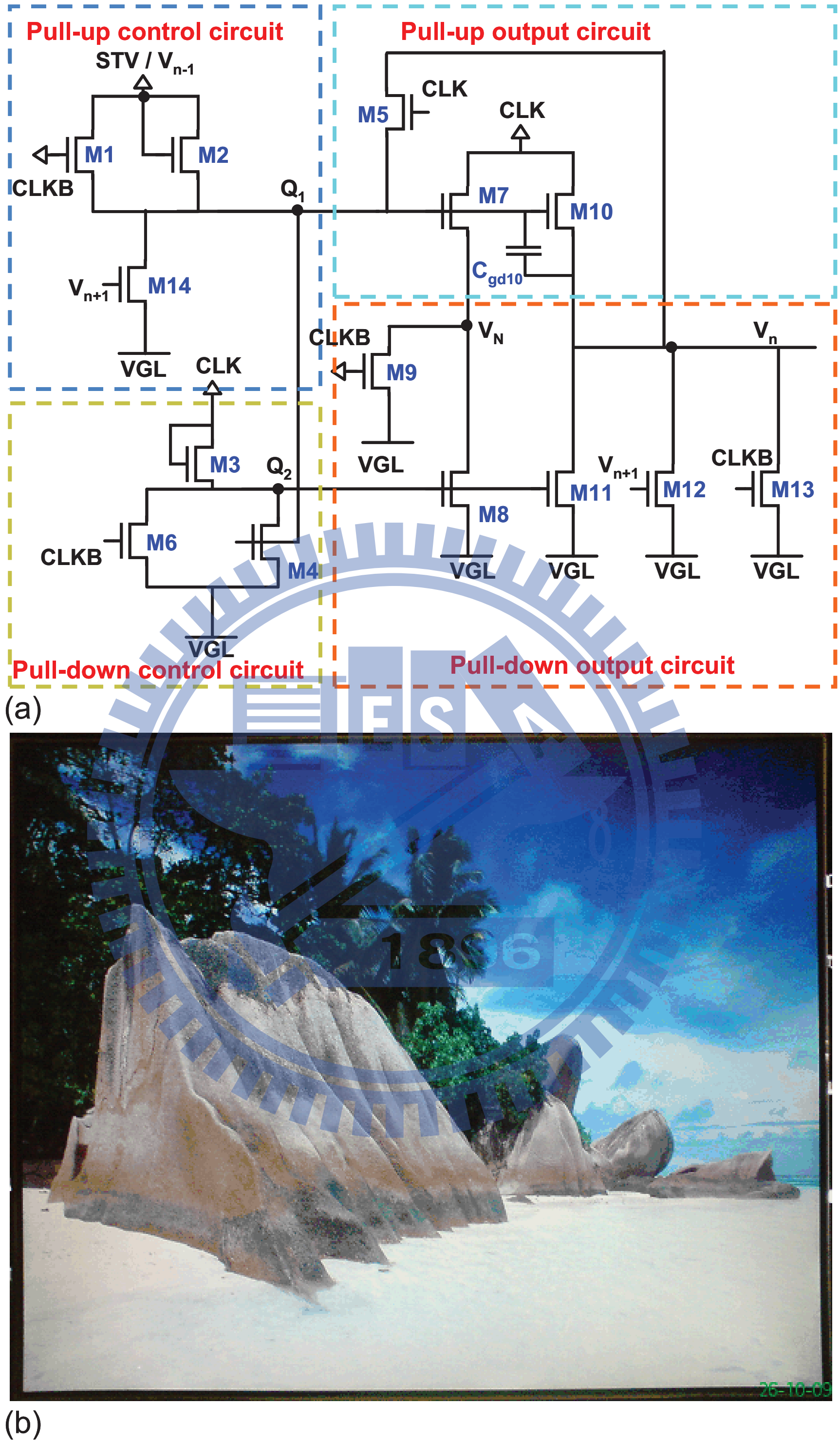
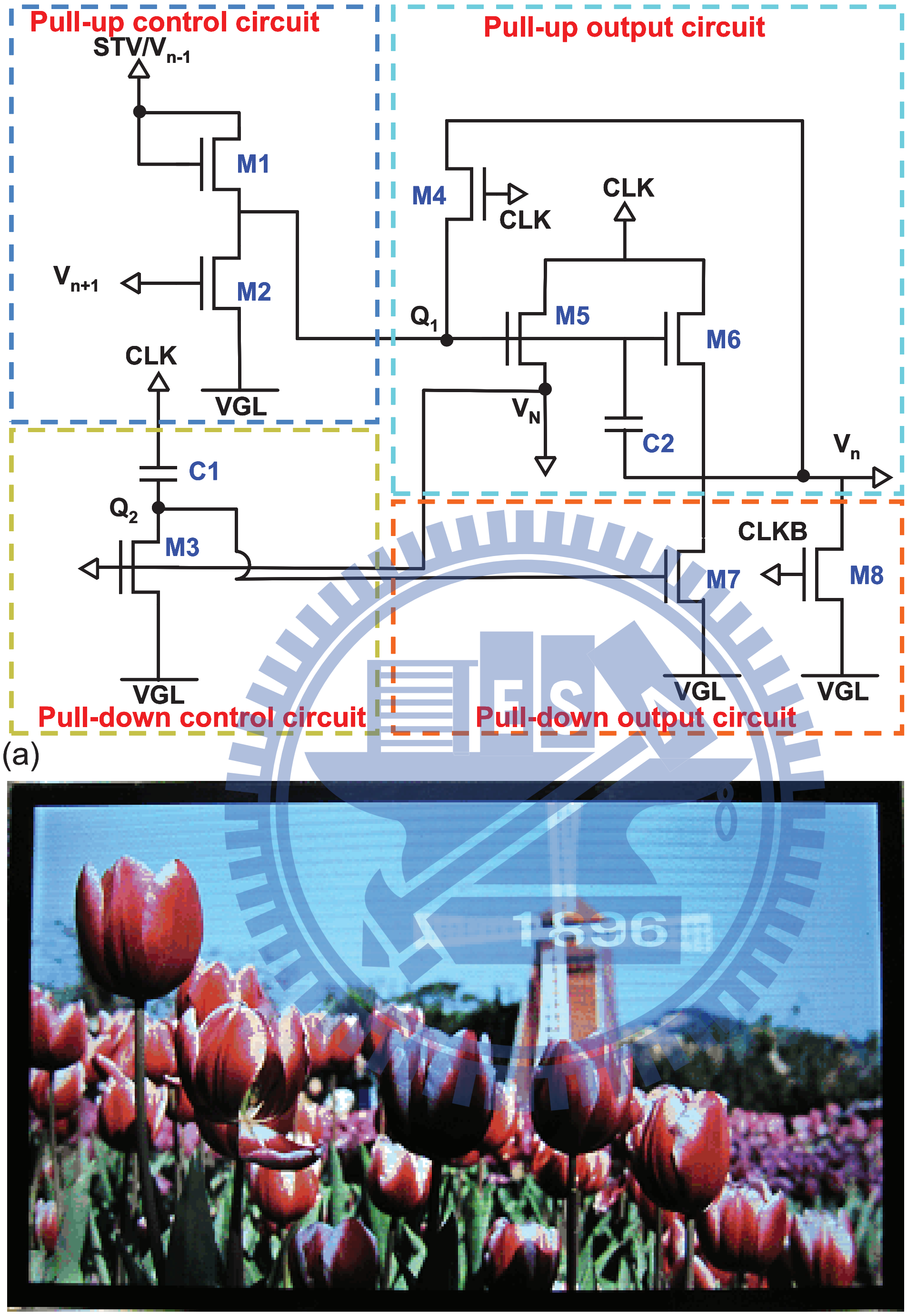


Figure 6.2: The first ASG driver circuit (a) has fourteen a-Si:H TFTs which consisted of 3 pull-up control devices, 3 pull-down control devices, 3 pull-up output devices and 5 pull-down output devices and (b) used in large loading products such as monitor and screen of TV (17 inch).



(a)

(b)

Figure 6.3: The second one has (a) eight a-Si:H TFTs and two capacitors which consisted of 2 pull-up control devices, 2 pull-down control devices, 4 pull-up output devices and 2 pull-down output devices and (b) used in small loading products such as display panel of cell phone (3.3 inch).

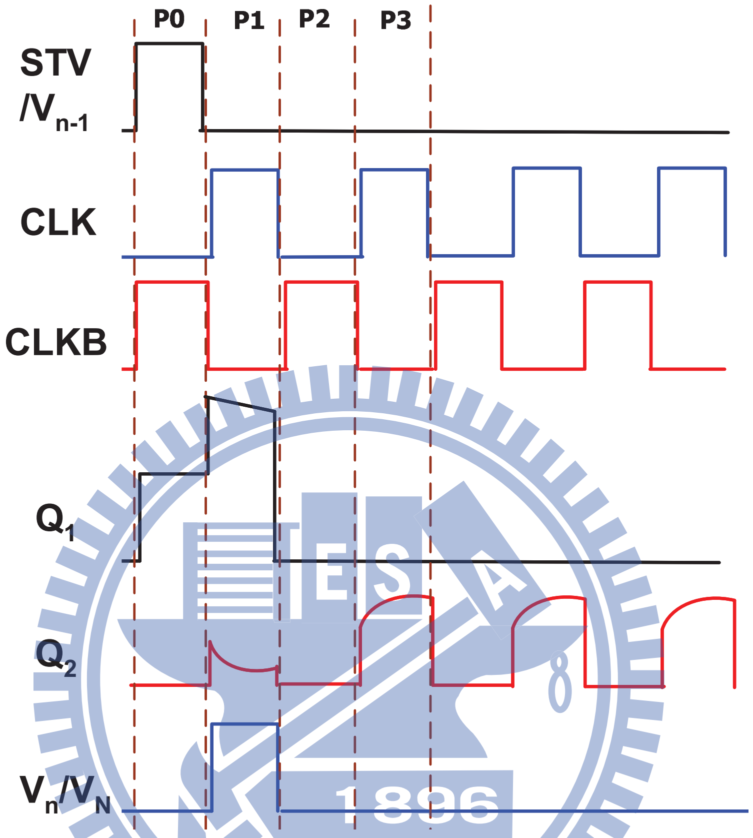
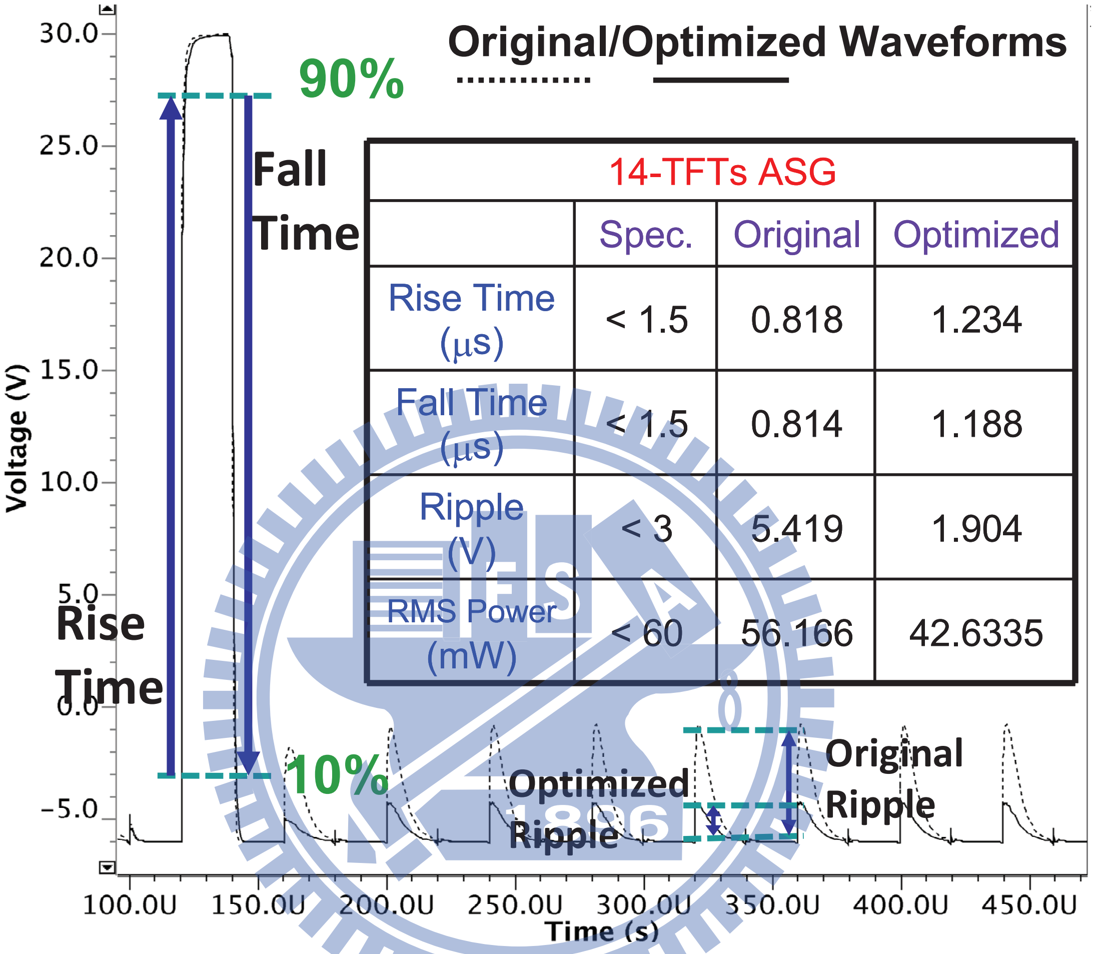


Figure 6.4: The timing diagram of 14-TFTs-ASG driver circuit. The CLK and CLKB denote the clock signal and clock bar signal and STV/V_{n-1} is inputted pulse signal. The V_n and V_N are the output signal which supply for the panel and next stage, respectively.

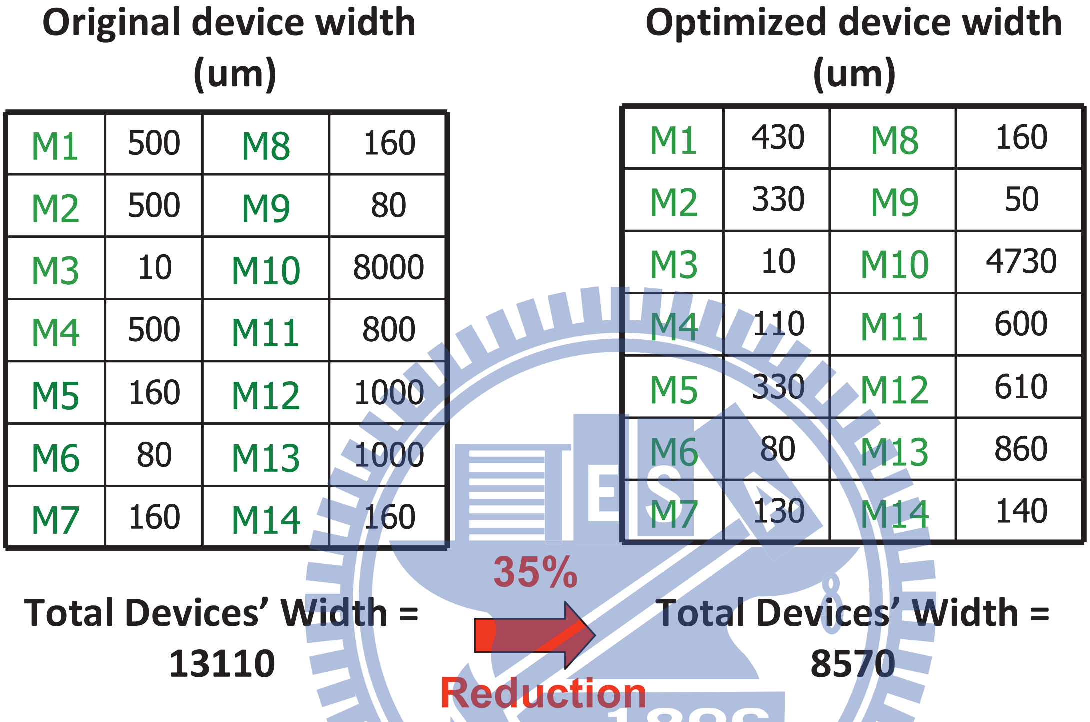
6.2 Simulation Results of 14-TFTs-ASG Driver Circuit

The designed parameters of 14-TFTs-ASG driver circuit are widths of a-Si:H TFT devices, as shown in Fig. 6.2(a). The original (dashed line) and optimized (solid line) results of the output signal which contains the fall time, the rise time and the ripple voltage in the ASG driver circuit are shown in Fig. 6.5, respectively. The rise time is defined by the interval of time required for leading edge of a pulse raised from 10% to 90% in the peak pulse amplitude and the definition of fall time is contrary to rise time. The ripple voltage is defined by maximum peak to peak voltage after the pulse. These three electrical characteristics are the required specifications in the ASG driver circuit design generally. The inset table of Fig. 6.5 indicates the specifications, original and optimized results. The original result shows that the fall time and the rise time are lower than the given specifications; however, the ripple voltage compared with our setting criteria is extremely high. Therefore, the established optimization kernel in the unified optimization framework is activated to find the feasible configuration of device widths based on the netlist file of the initial circuit. Finally, the ripple voltage after optimization decreases significantly from 5.419 V to 1.904 V while we keep the rise time and fall time satisfied the required specifications. Fig. 6.6 shows the initial device widths of this circuit by expert experience and our optimized results. There is 35% reduction of the optimized total devices width of a-Si:H TFTs compared with the initial one in this explored ASG driver circuit.



14-TFTs ASG			
	Spec.	Original	Optimized
Rise Time (μs)	< 1.5	0.818	1.234
Fall Time (μs)	< 1.5	0.814	1.188
Ripple (V)	< 3	5.419	1.904
RMS Power (mW)	< 60	56.166	42.6335

Figure 6.5: The original/optimized simulation results of 14-TFTs-ASG driver circuit. The inset table indicates specifications, original and optimized results of electrical characteristics.



Original device width (um)

M1	500	M8	160
M2	500	M9	80
M3	10	M10	8000
M4	500	M11	800
M5	160	M12	1000
M6	80	M13	1000
M7	160	M14	160

Total Devices' Width = 13110

Optimized device width (um)

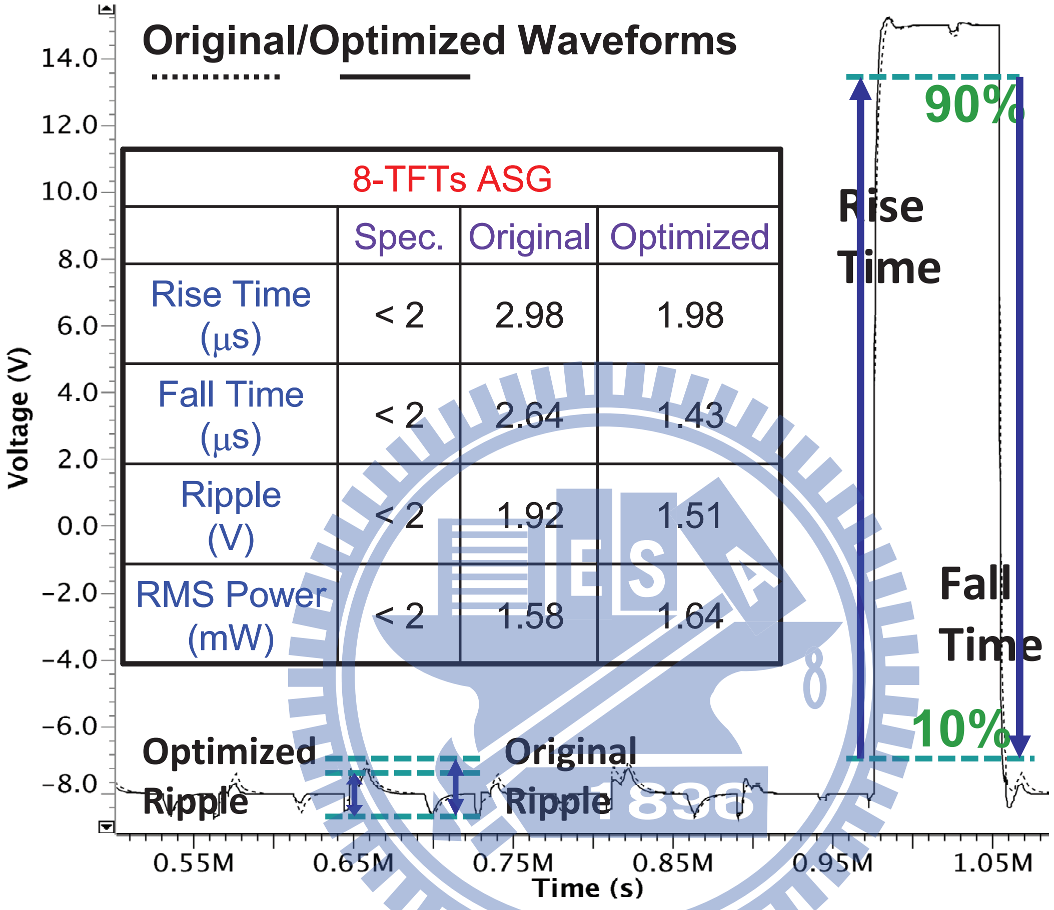
M1	430	M8	160
M2	330	M9	50
M3	10	M10	4730
M4	110	M11	600
M5	330	M12	610
M6	80	M13	860
M7	130	M14	140

Total Devices' Width = 8570

Figure 6.6: The comparison of TFT widths in original/optimized results of 14-TFTs-ASG driver circuit. From our optimized results, there is 35% reduction of the total devices width as compared to the original one.

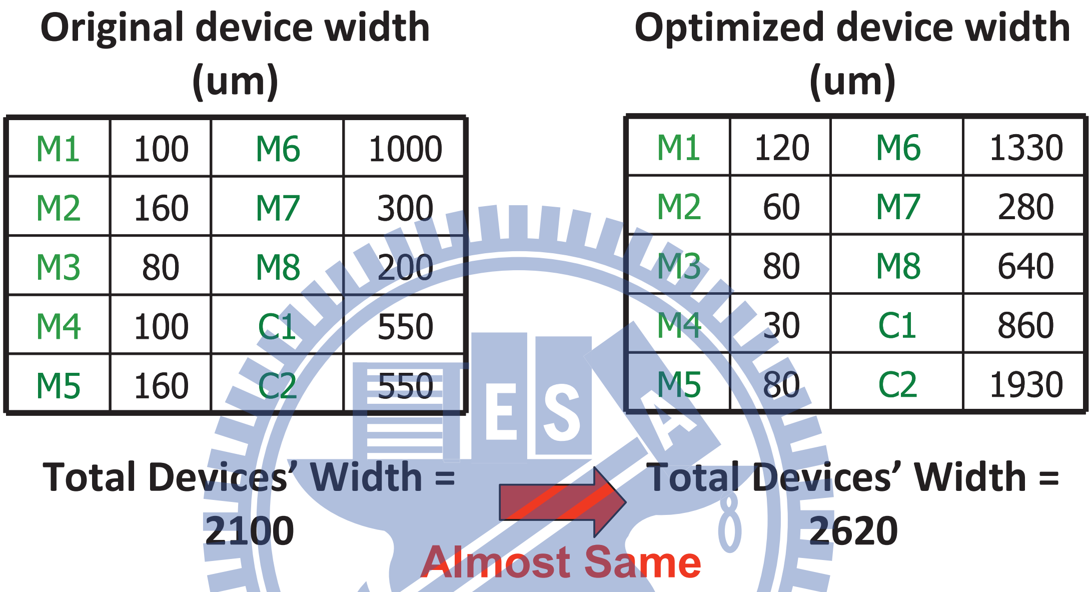
6.3 Simulation Results of 8-TFTs-ASG Driver Circuit

Similarly, eight widths of the a-Si:H TFT devices and two charged capacitors are needed to be optimized, as shown in Fig. 6.3(a). Figure 6.7 shows the information of simulation result of the output signal and power dissipation in the second tested circuit before/after optimization. The definition of rise time, fall time and ripple are the same as aforementioned. Then the optimized rise time, fall time and ripple voltage are significantly reduced from 2.9827 s, 2.6435 s and 1.9166 V to 1.9828 s, 1.435 s and 1.571 V, which are summarized in inset table of Fig. 6.7, respectively. Under these electrical characteristic, although we release a little power dissipation, we still maintain it about 1.64 mW which satisfied its specification. The Fig. 6.8 shows the devices' width comparison of original and optimized results. There is almost same of total devices width. For the given targets and specifications, it shows that this methodology provides an automatic mechanic to design the parameters of the explored ASG driver circuit.



8-TFTs ASG			
	Spec.	Original	Optimized
Rise Time (μs)	< 2	2.98	1.98
Fall Time (μs)	< 2	2.64	1.43
Ripple (V)	< 2	1.92	1.51
RMS Power (mW)	< 2	1.58	1.64

Figure 6.7: The original/optimized simulation results of 8-TFTs-ASG driver circuit. The inset table indicates specifications, original and optimized results of electrical characteristics.



Original device width (um)

M1	100	M6	1000
M2	160	M7	300
M3	80	M8	200
M4	100	C1	550
M5	160	C2	550

Total Devices' Width = 2100

Optimized device width (um)

M1	120	M6	1330
M2	60	M7	280
M3	80	M8	640
M4	30	C1	860
M5	80	C2	1930

Total Devices' Width = 2620

Figure 6.8: The comparison of TFT widths in original/optimized results of 8-TFTs-ASG driver circuit. Comparing with initial total device width, the optimized result is almost same.

6.4 Sensitivity Analysis

Sensitivity analysis is a technique which considers how small changes in decision variables affecting the function outputs. For designed parameters which fulfill aforementioned specifications, We analyze a selected and modified solution for two ASG driver circuits by $\pm$ 0.5 μm of each width and $\pm$ 0.2 μm of each length with optimized widths sequentially. In the mathematical statement, if $f_0(x^*)$ represents the function value in the analysis point, then we can observe the variation of the function with small perturbation of x^*, then the sensitivity of f in x^* respect to x_i can be expressed as [99]:

$$Z_i = |\frac{\partial f_0^*/f_0^*}{\partial x_i/x_i}| \times 100\%, \tag{6.1}$$

where x_i is each decision variable. Figures 6.9 and 6.10 show the sensitivity of 14-TFTs-ASG and 8-TFTs-ASG driver circuits which may result from process variation effects in the circuit, respectively. In Fig. 6.9(a), the sensitivity of 14 parameters is almost lower than 10%. However, the electrical characteristics are rather susceptible to the parameter W10 which controlled the charge ability of the TFT array devices of display panel. Therefore, the parameter W10 induces larger sensitivity. Similarly, Fig. 6.10(a) shows small sensitivity of 8-TFTs-ASG driver circuit and the parameter W6 induces lager sensitivity due to the same reason which is aforementioned. We further examine the sensitivity of length variation with optimized widths, as explored in Figs. 6.9(b) and 6.10(b). The same phenomena are observed in these ASG driver circuits. The sensitivity of electrical characteristics is also dominated by W10 of 14-TFT-ASG driver circuit and W6 of 8-TFT-ASG driver circuit, respectively. Moreover, due to parameter L12 and L13 of 14-TFTs-ASG driver circuit and L7 of 8-TFTs-ASG driver circuit are component of pull-down output circuit, the sensitivity of fall time is quite large. Finally, the result can guarantee the robustness of our optimized design and confirm promising characteristics of these ASG driver circuits which have benefits to manufacturing of TFT-LCD panel.

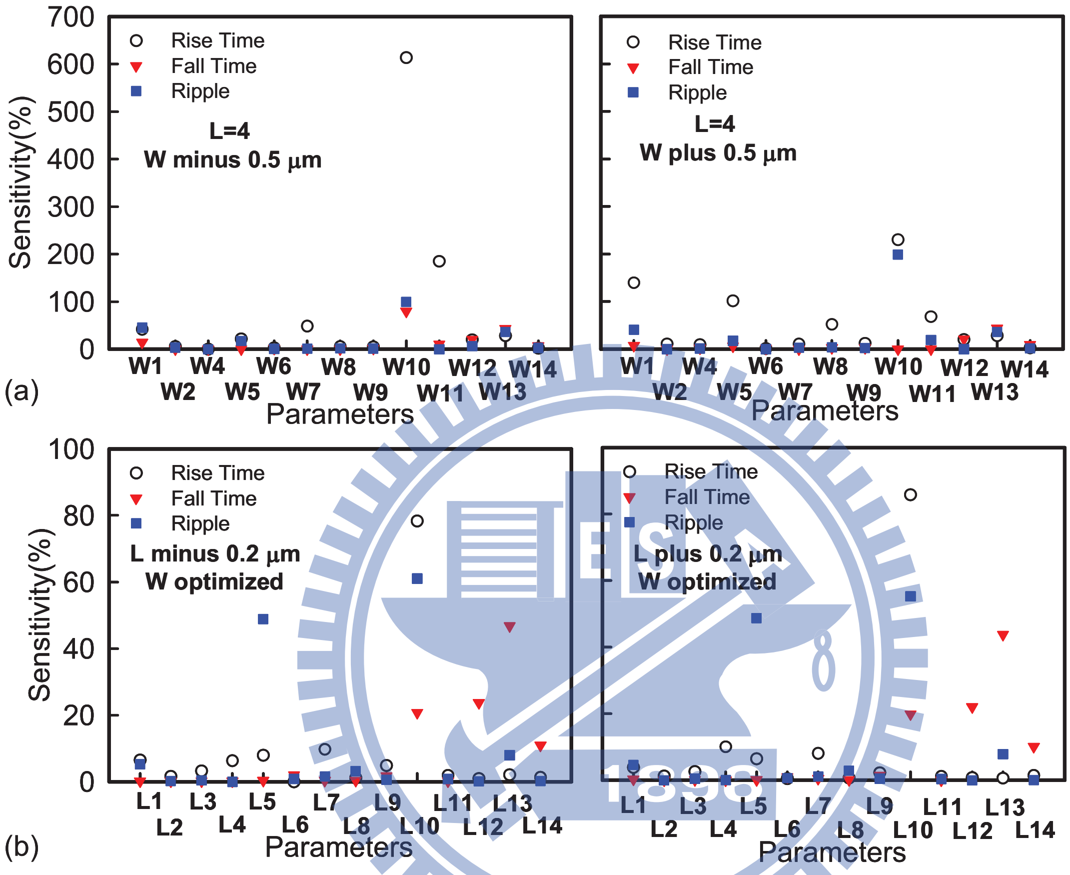


Figure 6.9: The sensitivity analysis of the14-TFTs-ASG driver circuit. (a) ± 0.5 μm of each width with L=4 μm (b) ± 0.2 μm of each length with optimized widths sequentially.

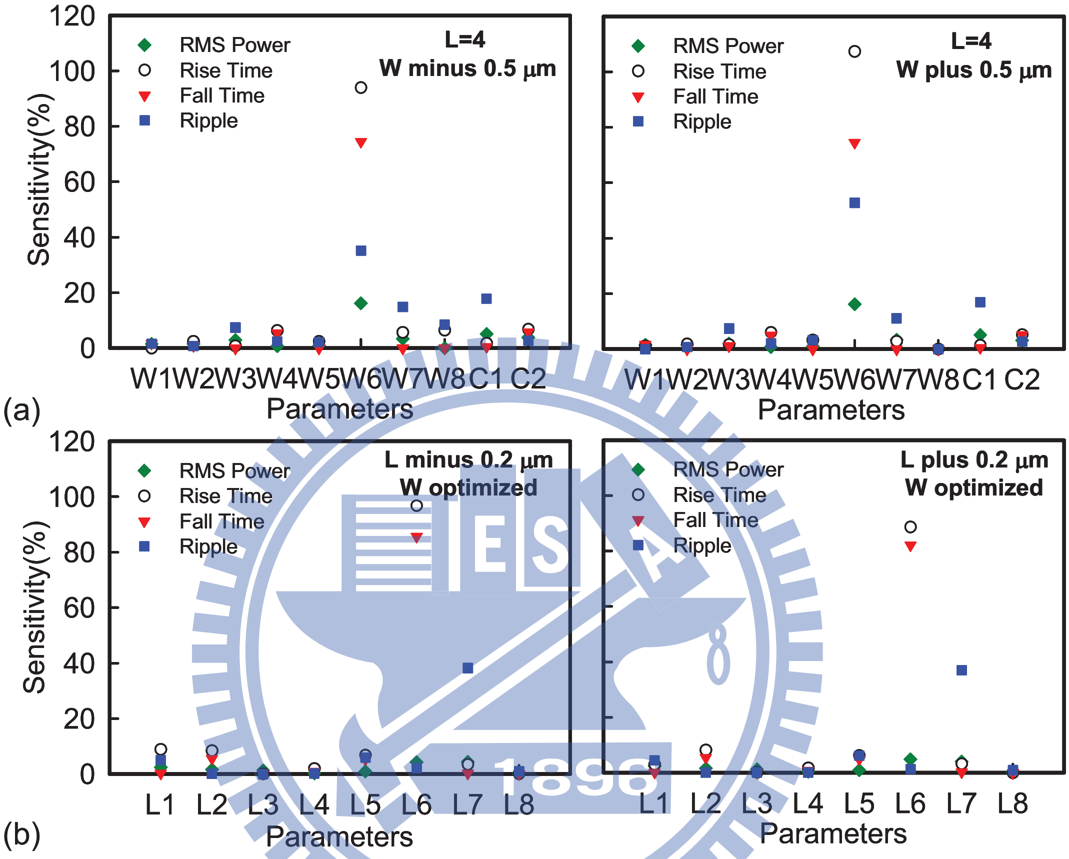


Figure 6.10: The sensitivity analysis of the 8-TFTs-ASG driver circuit. (a) ± 0.5 μm of each width with L=4 μm (b) ± 0.2 μm of each length with optimized widths sequentially.

6.5 Summary of this Chapter

In this chapter, we were briefed the operation of explored 14-TFTs-ASG driver circuits as an example. Then, comprehensive simulation analysis of ASG driver circuits was conducted by genetic algorithm and sensitivity analysis. The optimized ASG driver circuits with excellent performance and stability were achieved. Moreover, the total device width of the14-TFTs-ASG driver circuit has 35% reduction which implies the reduction of circuit area.

Chapter 7

Design, Fabrication and Measurement

In this chapter, the standard process flow of thin film transistors is considered for the sample fabrication of optimized amorphous silicon gate (ASG) driver circuits. The measurement results of rise time, fall time, and ripple voltage of samples are discussed in detail.

7.1 Process Flow of a-Si:H Thin Film Transistors

The inverted-staggered back-channel etched (BCE) type of a-Si:H TFTs fabricated on glass substrate was used for gate driver circuit. First, the gate electrode of 300-nm-thick Mo/AlNd (GE) alloy is deposited by physical vapor deposition method on the glass substrate and patterned. Thereafter, the 380-nm-thick silicon-nitride (SiN_x), 150-nm-thick undoped a-Si:H layer, 50-nm-thick n+ a-Si:H are deposited by chemical vapor deposition method and the a-Si:H layers are patterned. The silicon-nitride layer is served as the gate insulator and deposition temperature is about 300-350 ^{o}C. The undoped a-Si:H layer is served as the active layer and deposition temperature is about 220-350 ^{o}C. The n+ a-Si:H layer is used to form the ohmic contacts at source/drain (S/D) electrodes, which are deposited by physical vapor deposition method and then patterned. The n+ a-Si:H layer in TFT channel region was etched off by dry etching method and then overetched until the undoped a-Si:H layer. The back channel passivation layer (Si_3N_4) of 200-nm-thick is deposited by chemical vapor deposition method and patterned. Finally, the contact hole was deposited with 50-nm ITO layer by physical vapor deposition method, as a pixel electrode (connected with source or drain). All the process is depicted in the Fig. 7.1. The cross-section view of SEM picture of fabricated TFT sample is shown in the Fig. 7.2(a). The device is with 18 μm channel width, 4 μm channel, and 150 nm channel thickness. In addition, the process variation of lengths of ASG driver circuits which make agree with the assumptions of sensitivity analysis is shown in Figs. 7.2(b)-(e).

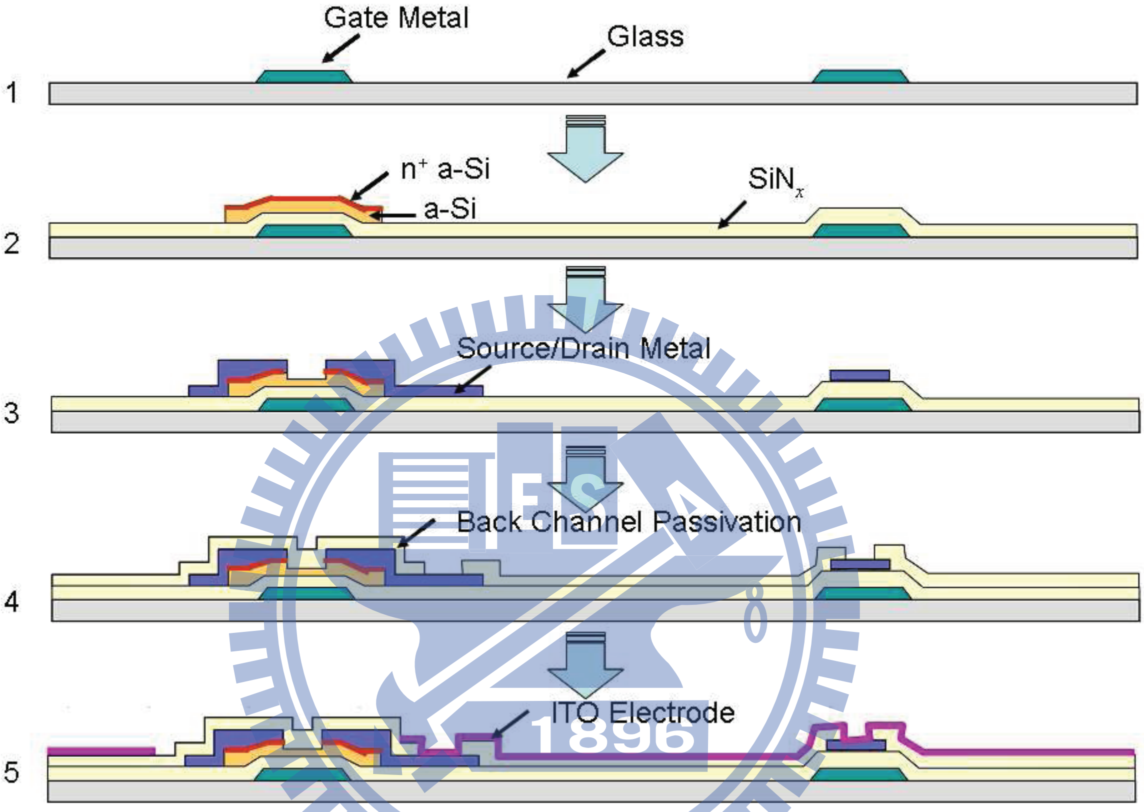


Figure 7.1: The process flow of inverted-staggered back-channel etched (BCE) type of a-Si:H TFT.

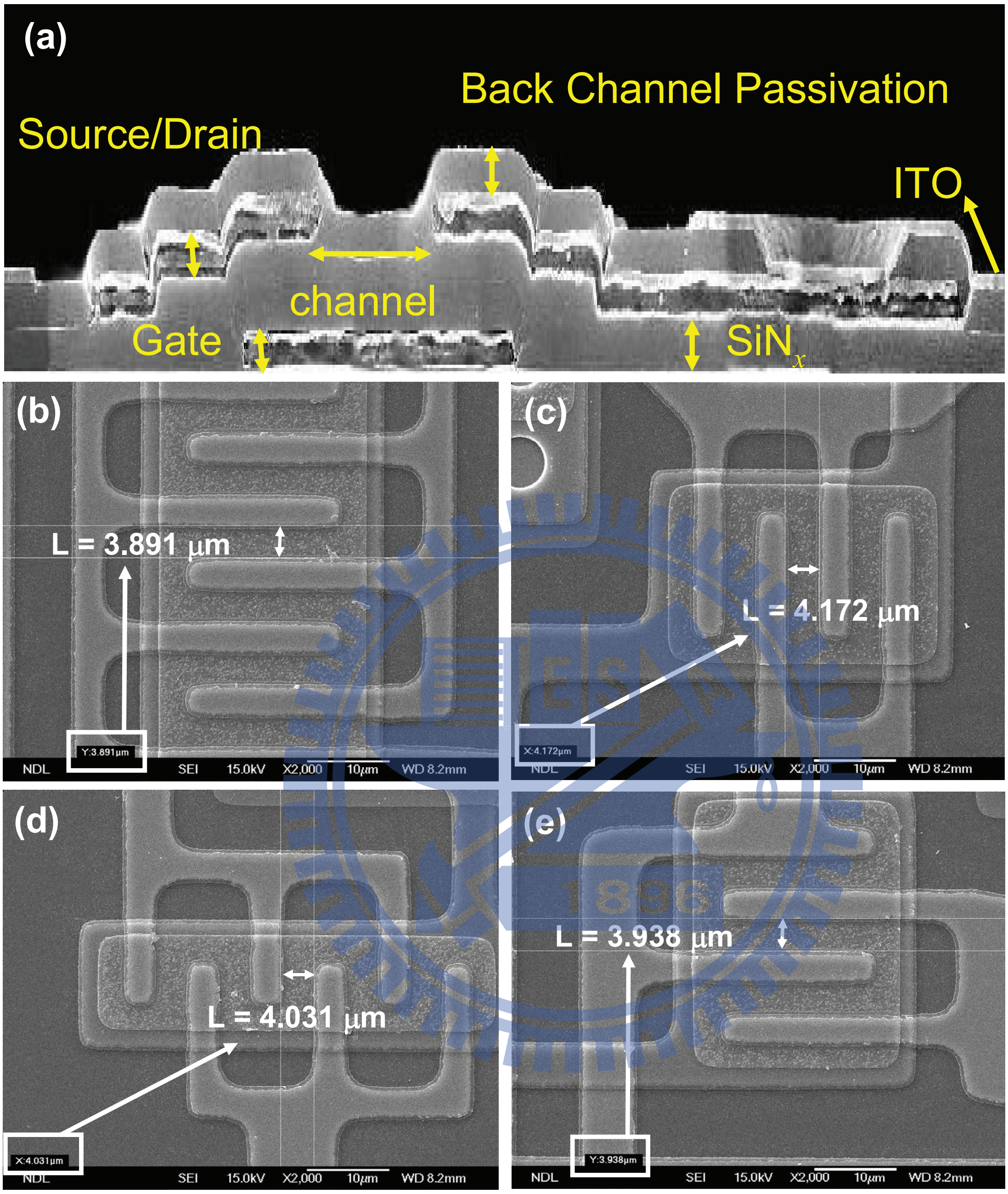


Figure 7.2: (a) The cross-section view of SEM picture of fabricated TFT sample. The process variation of (b) L5 and (c) L11 of 14-TFTs-ASG driver circuit and (d) L3 and (e) L6 of 8-TFTs-ASG driver circuit, respectively.

7.2 Experimental Results of 14-TFTs-ASG Driver Circuit

Test chips of the optimized 14-TFTs-ASG driver circuit are fabricated in the standard 4-μm a-Si:H TFT technology. We examine and depict the tested layout which consisted of six stages gate driver circuit and occupies the area of 1.386 mm^2, as shown in Fig. 7.3. Fig. 7.4 displays a Chroma 58162-E signal generator and a Tektronix DP04054 oscilloscope which were used to carry out the aforementioned input signal. As for the measurements more precisely, the input signal, STV (SP), CLK, CLKb, and VSS are set as same as the simulation, as disclosed in Fig. 7.5. Then the measured dynamic characteristics of the chip are illustrated in Fig. 7.6, where the rise time, fall time and ripple voltage is 1.23 μs, 1.18 μs and 1.9 V, respectively. Comprehensive comparison among the fabrication data of the original/optimized setting and the specifications are disclosed in Fig. 7.7(a). The improvement of ripple voltage is 71% for 14-TFTs-ASG driver circuit while we also successfully maintain the rise time and the fall time within the required specifications. In additional, the experimental characterization results are close to the simulation results or even better than the theoretically estimated data, as listed in Fig. 7.7(b). Figure 7.8 shows the optical image of our optimized one stage ASG driver circuit with 14-TFTs by using SEM and occupied the area of 0.231 mm^2 (1050 μm × 220 μm). Comparing with original circuit area (302 μm × 780 μm = 0.236 mm^2), there is only 2% reduction of our layout technique which should be improved in our future work.

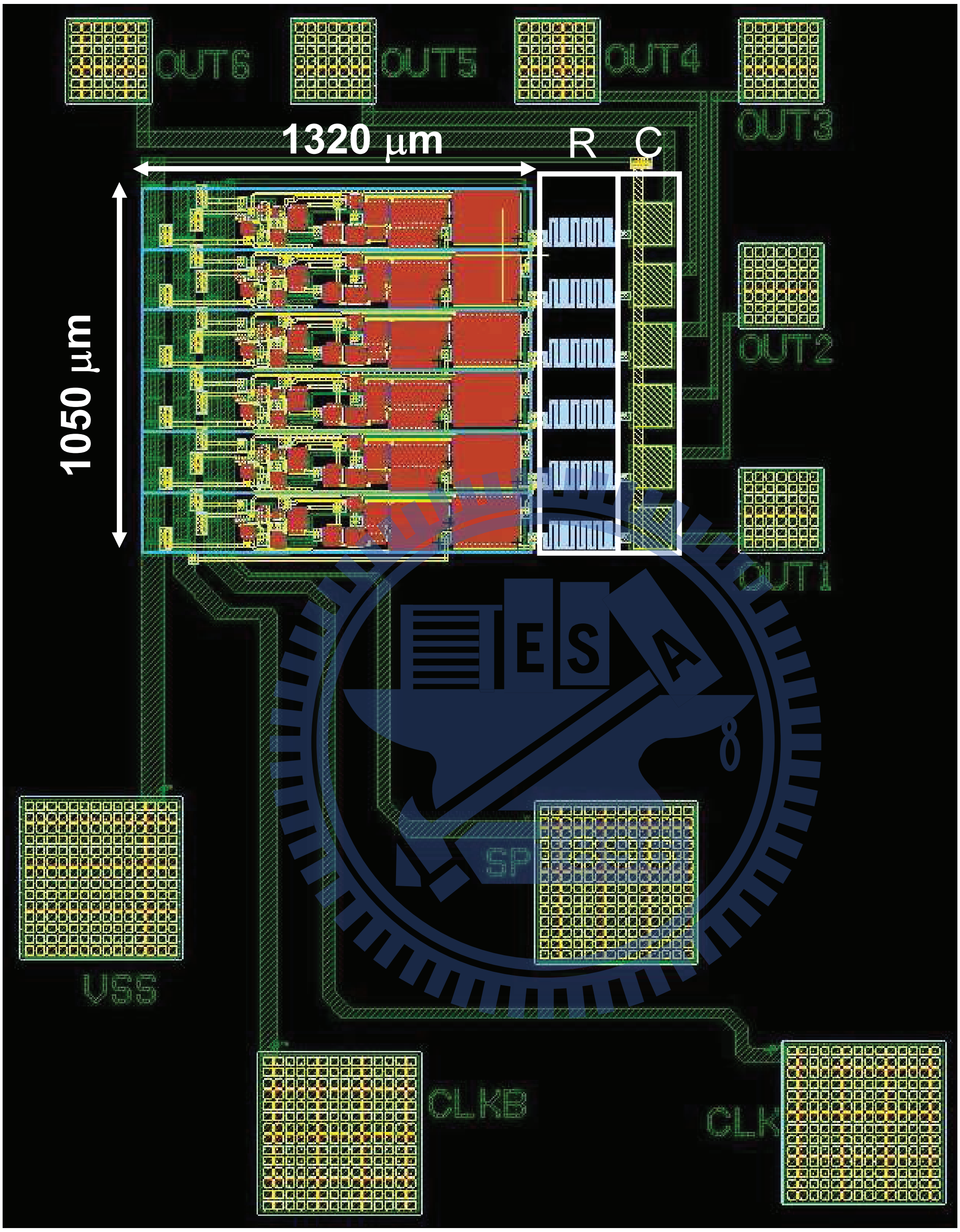
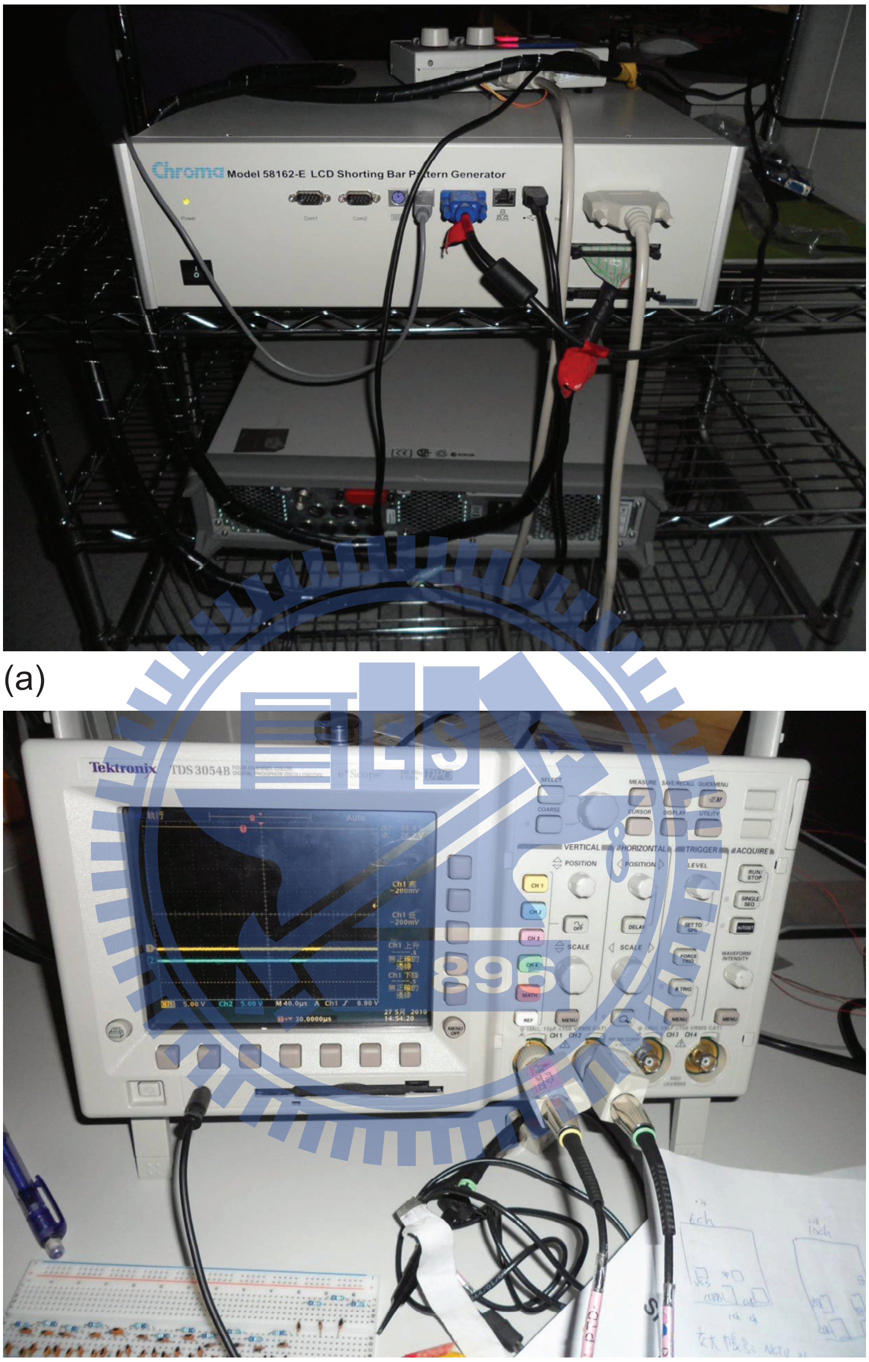


Figure 7.3: The tested chip layout of six stages gate driver circuit which is 1320 μm wide and 1050 μm high and occupied the area of 1.386 mm^2.



(a)

(b)

Figure 7.4: The equipments of (a) a Chroma 58162-E signal generator and (b) a Tektronix DP04054 oscilloscope which we used to carry out the measurement results.

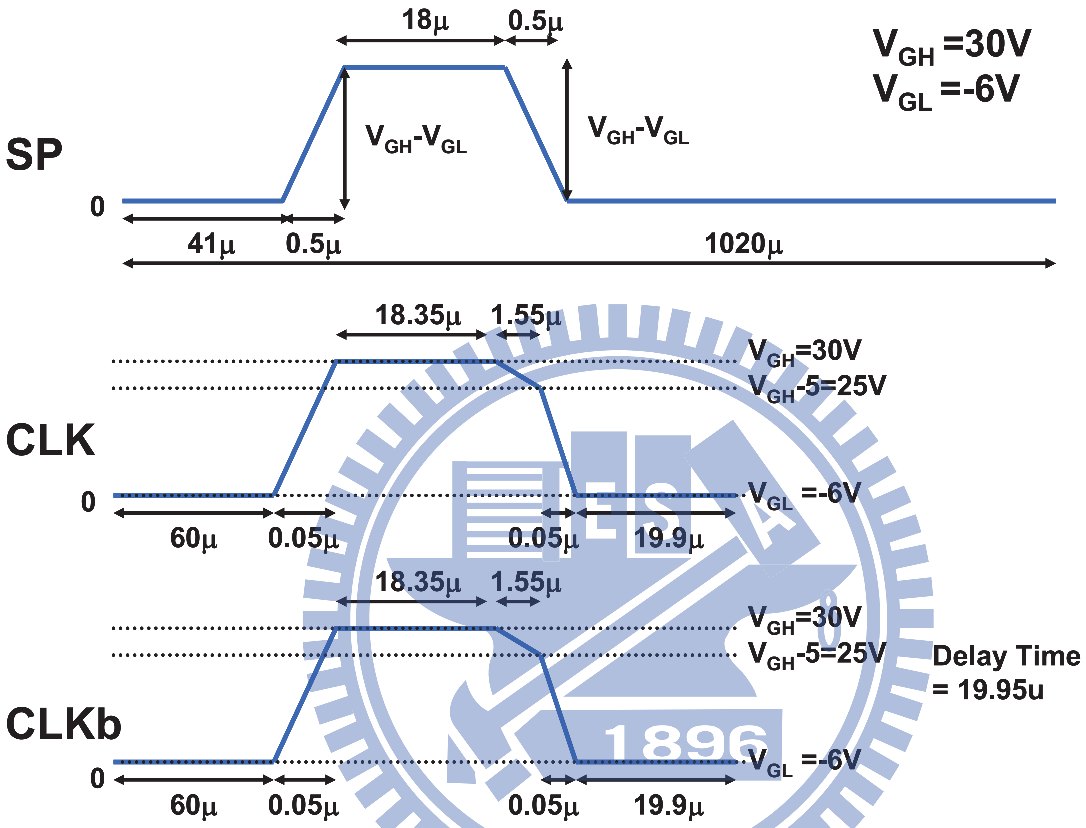


Figure 7.5: The detail setting of input signal of 14-TFTs-ASG driver circuit by using a Chroma 58162-E signal generator.

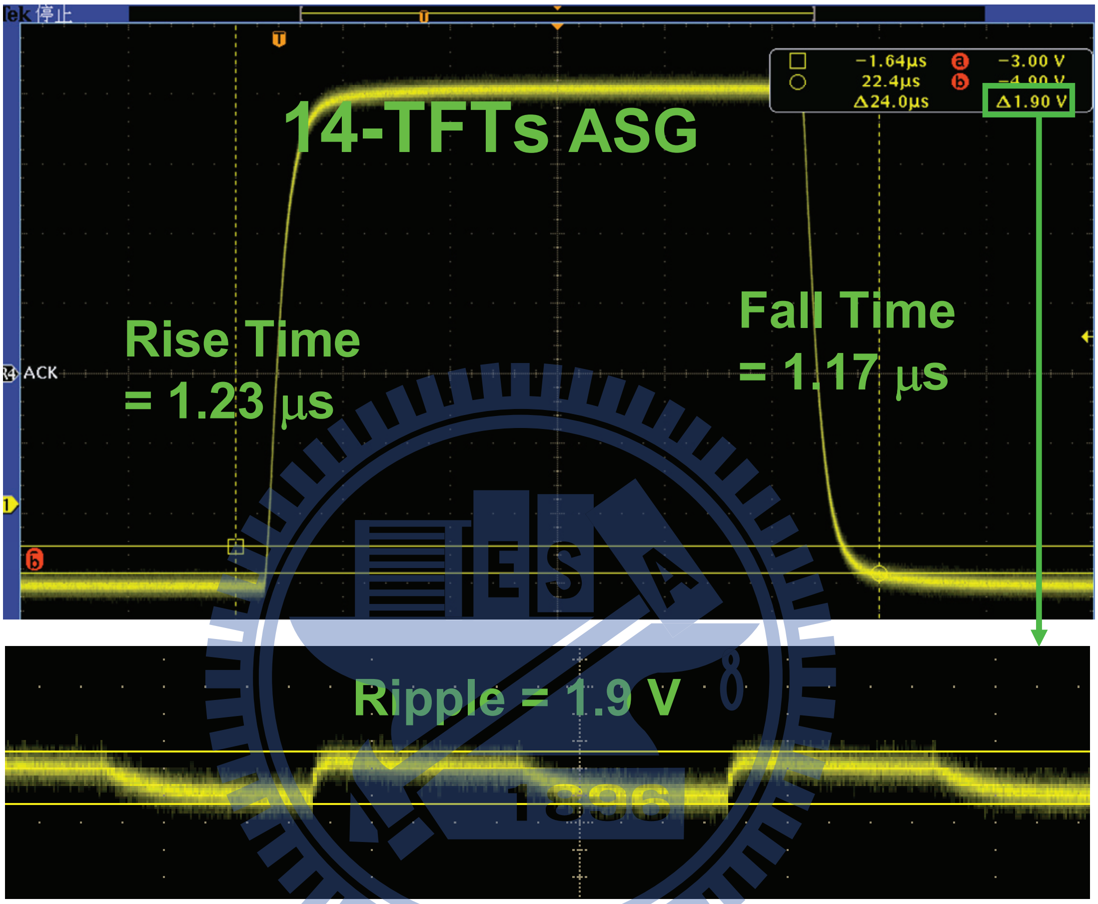
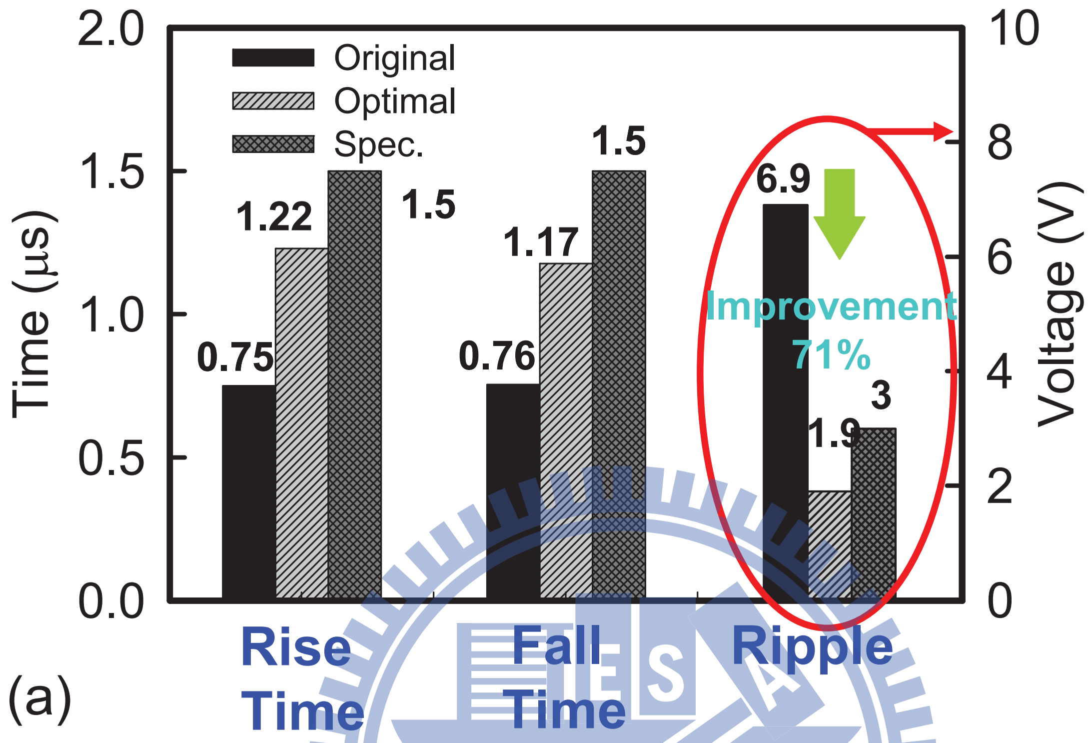


Figure 7.6: The experimental results of rise time, fall time and ripple voltage for 14-TFTs-ASG driver circuit are measured by using a Tektronix DP04054 oscilloscope.



(b)

14-TFTs ASG Driver Circuit			
	Fabrication	**Simulation**	**Error (%)**
Rise Time (μs)	1.229	1.234	0.41
Fall Time (μs)	1.177	1.188	0.93
Ripple Voltage (V)	1.9	1.904	0.21

Figure 7.7: (a) Comprehensive comparison among the fabrication data of the original/optimized setting and the specifications. (b) The comparison of simulation and characterization results of 14-TFTs-ASG driver circuit.

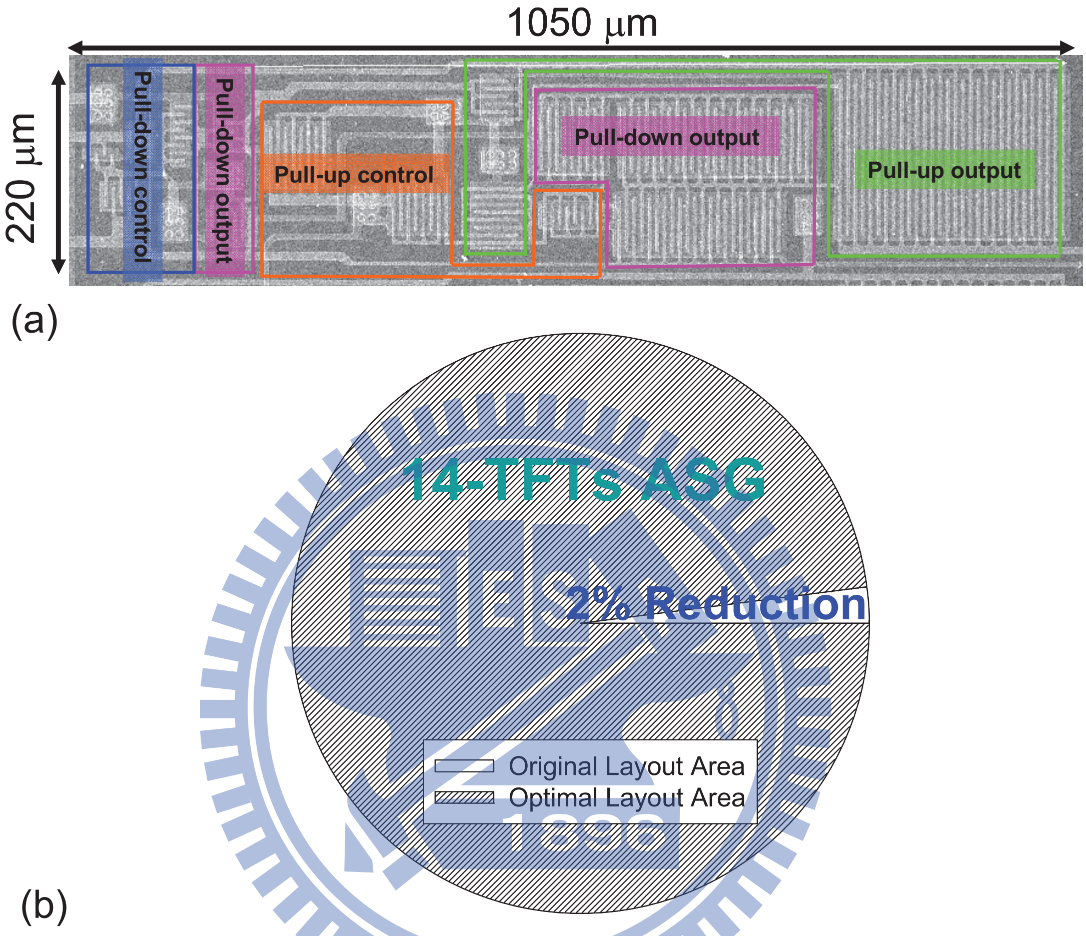


Figure 7.8: (a) The optical image of the fabricated 14-TFTs-ASG driver circuit which occupied the area of 0.231 mm^2 (1050 μm × 220 μm) . (b) The comparison of a single-stage circuits area for 14-TFTs-ASG driver circuit.

7.3 Experimental Results of 8-TFTs-ASG Driver Circuit

As same as previous subsection, test chips of the optimized ASG driver circuit which consisted of eight TFTs and two charged capacitances were also fabricated. The test layout which consisted of eleven stages gate driver circuit and occupies the area of 1.795 mm^2, as shown in Fig. 7.9. The input signals of 8-TFTs-ASG driver circuit which is different from 14-TFTs-ASG driver circuit are set, as displayed in Fig. 7.10. Then the measured dynamic characteristic of the rise time, fall time and ripple voltage is 1.464 μs, 1.362 μs and 2.1 V, respectively, as disclosed in Fig. 7.11. According to our complete comparison in Fig. 7.12(a), the optimized ripple voltage has 49% improvement while we also successfully maintain the same rise time and fall time as compared with original fabrication results. However, there have almost 30% errors between simulation and fabrication results which should be improved, as listed in Fig. 7.12(b). In addition, the optical image of our optimized one stage ASG driver circuit with 8-TFTs by using scanning electron microscope is shown in Fig. 7.13. Notably, Comparison with original chip area (252 μm $\times$ 939 μm = 0.237 mm^2), there is 36% reduction of our layout technique and occupied the area of 0.152 mm^2 (304 μm $\times$ 500 μm).

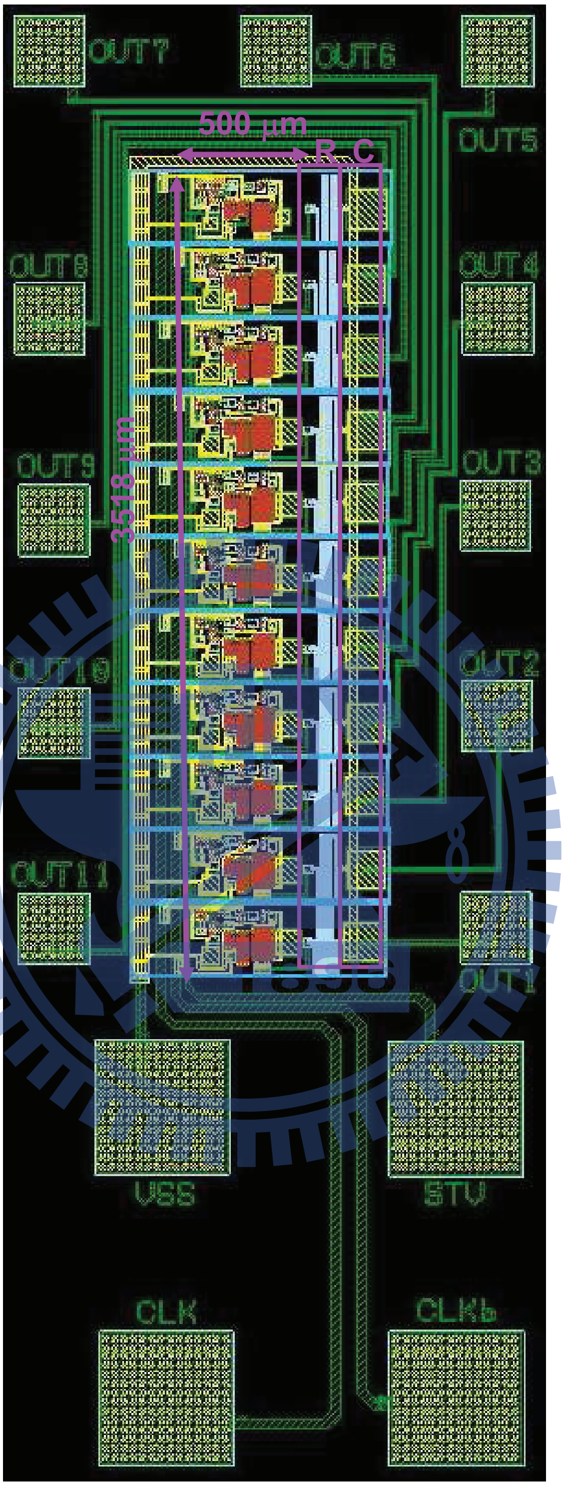


Figure 7.9: The tested chip layout of eleven stages gate driver circuit which is 500 μm wide and 3218 μm high and occupied the area of 1.795 mm^2.

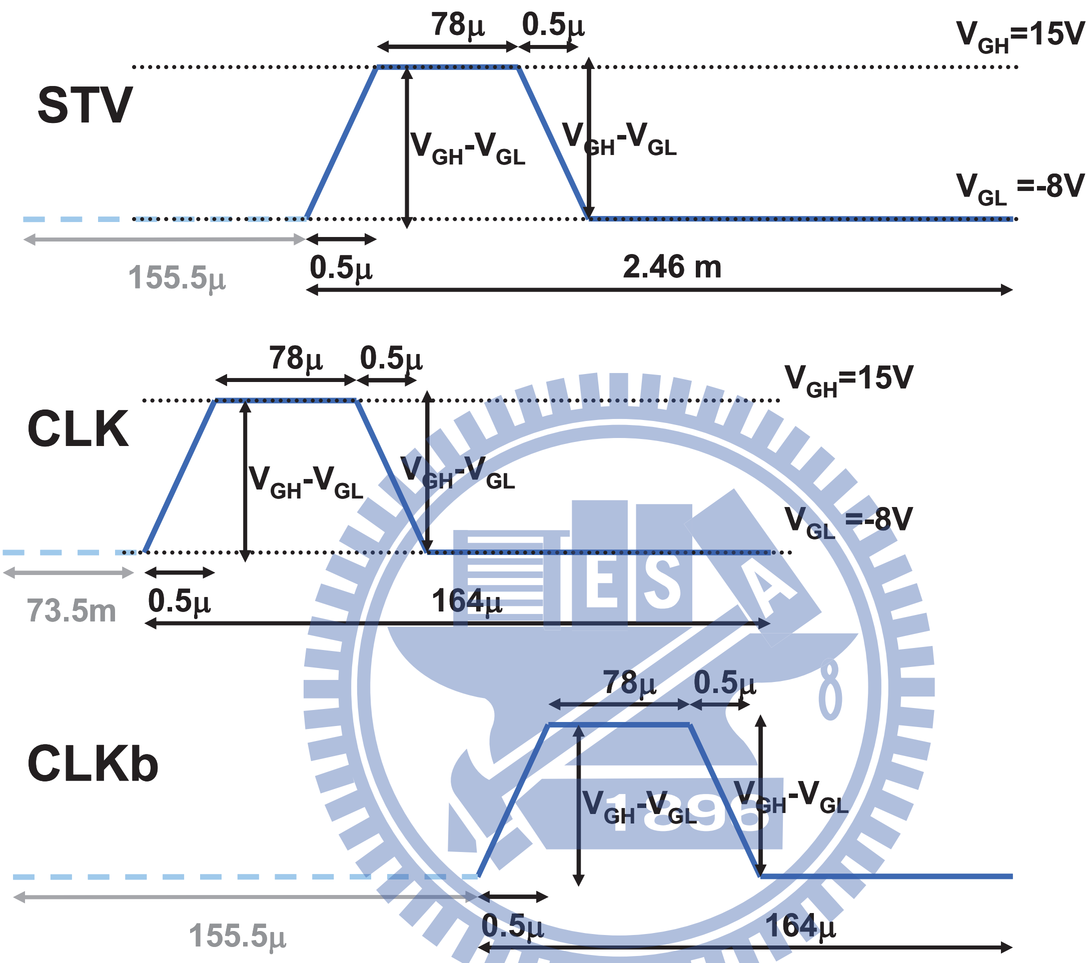
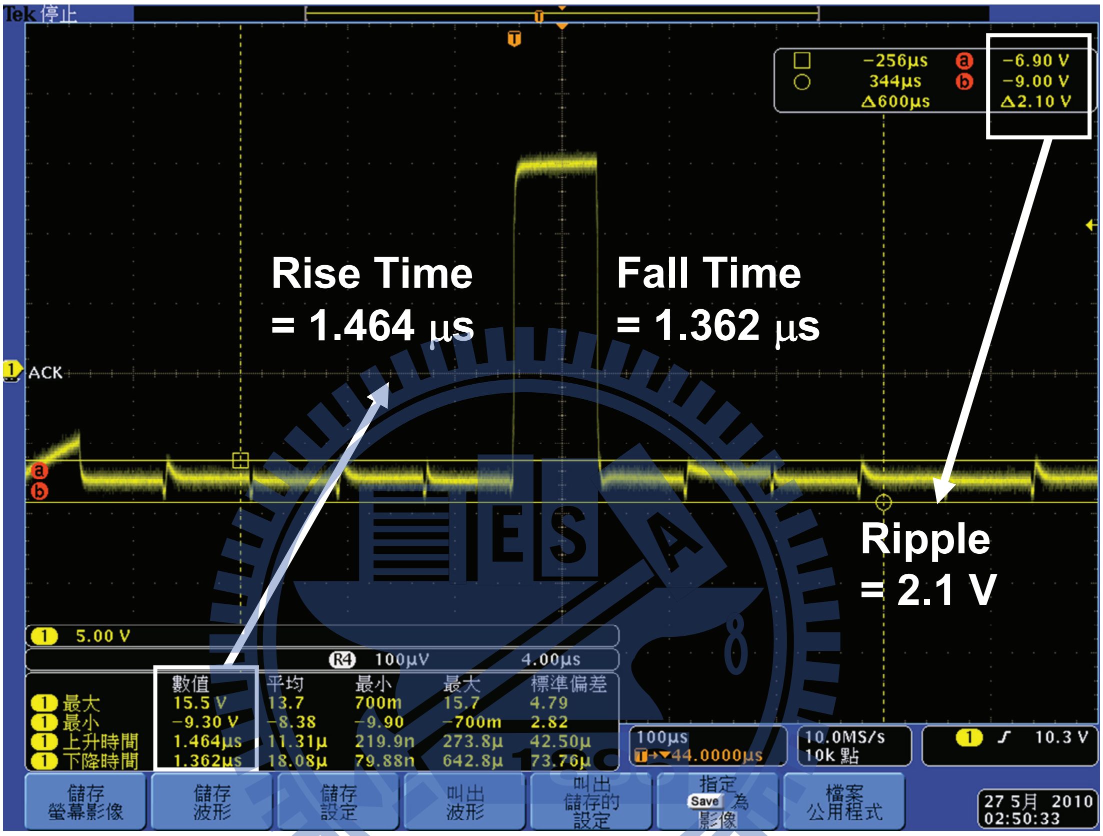


Figure 7.10: The detail setting of input signal of 8-TFTs-ASG driver circuit by using a Chroma 58162-E signal generator.

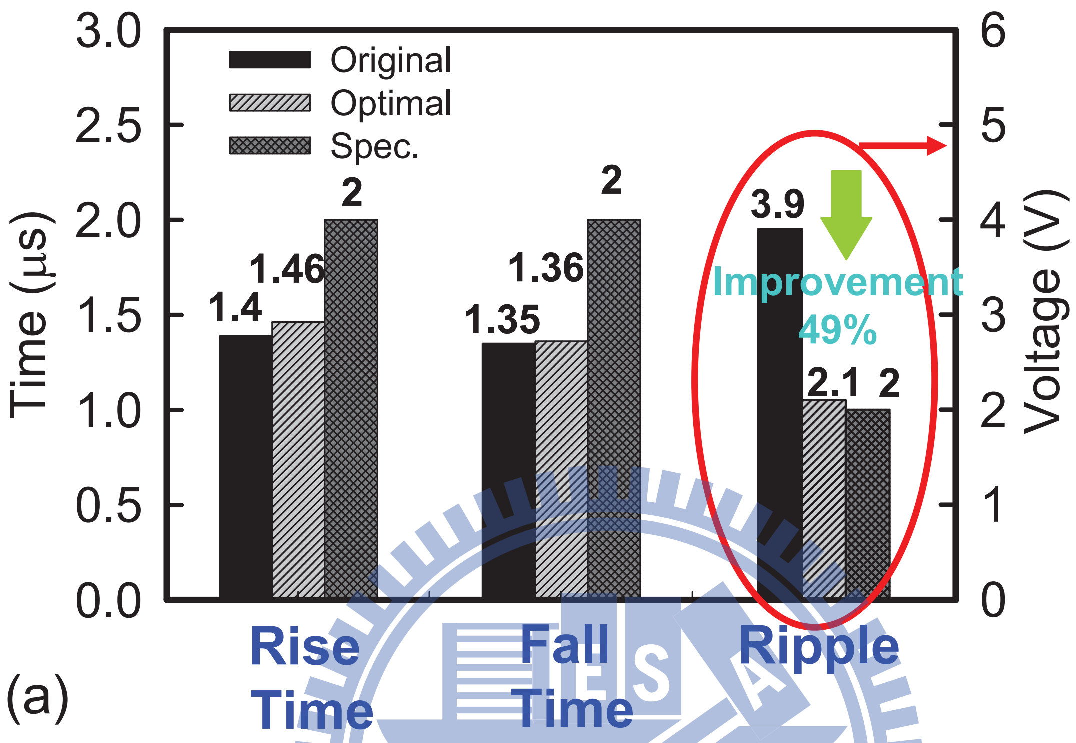

Rise Time = 1.464 µs

Fall Time = 1.362 µs

Ripple = 2.1 V

	數值	平均	最小	最大	標準偏差
① 最大	15.5 V	13.7	700m	15.7	4.79
① 最小	−9.30 V	−8.38	−9.90	−700m	2.82
① 上升時間	1.464µs	11.31µ	219.9n	273.8µ	42.50µ
① 下降時間	1.362µs	18.08µ	79.88n	642.8µ	73.76µ

Figure 7.11: The experimental results of rise time, fall time and ripple voltage for 8-TFTs-ASG driver circuit are measured by using a Tektronix DP04054 oscilloscope.



(b)

8-TFTs ASG Driver Circuit			
	Fabrication	**Simulation**	**Error (%)**
Rise Time (μs)	1.464	1.98	+26.05%
Fall Time (μs)	1.362	1.43	+4.76%
Ripple Voltage (V)	2.1	1.51	-33.8%

Figure 7.12: (a) Comprehensive comparison among the fabrication data of the original/optimized setting and the specifications. (b) The comparison of simulation and characterization results of 8-TFTs-ASG driver circuit.

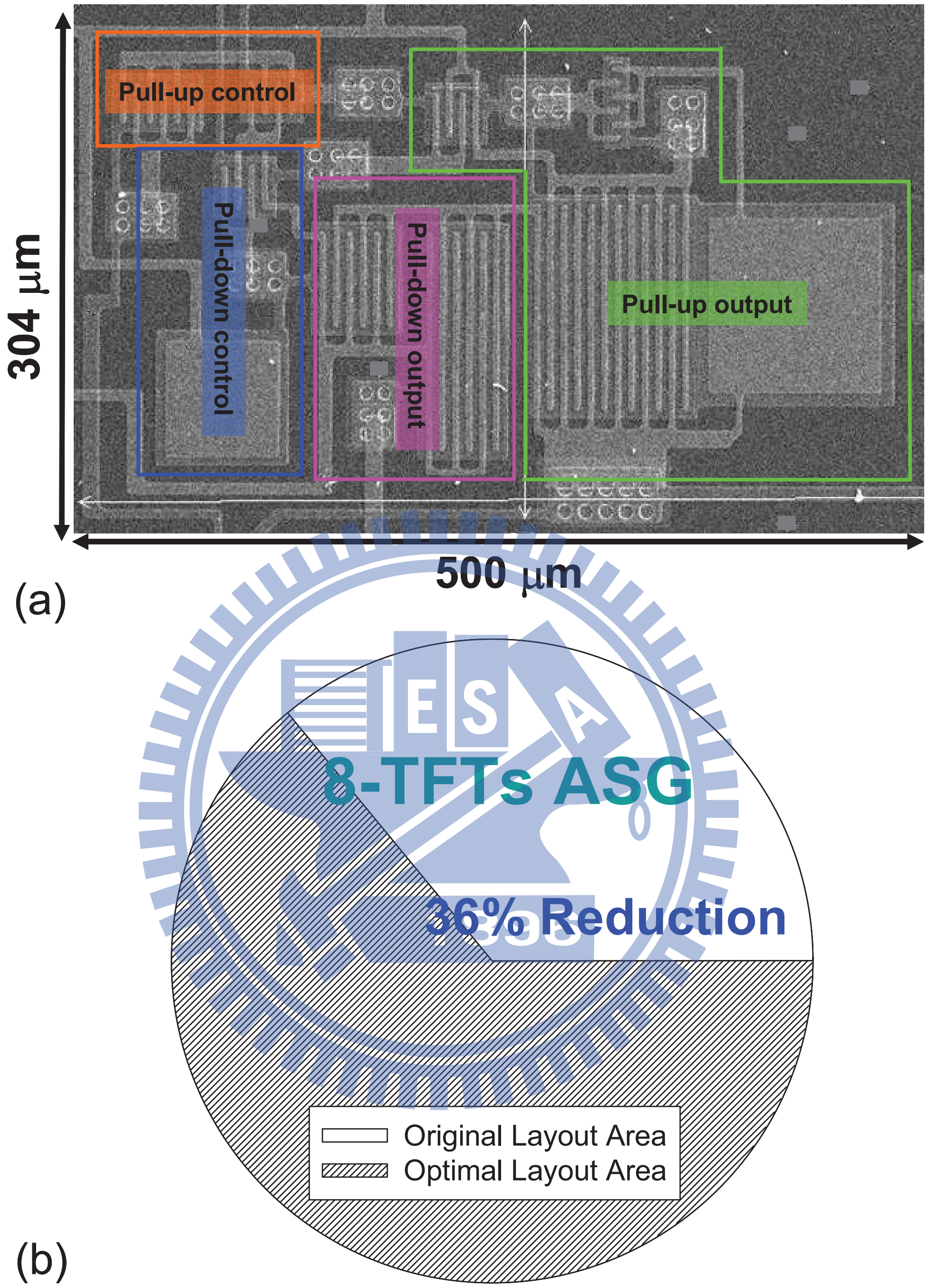


Figure 7.13: (a) The optical image of the fabricated 8-TFTs-ASG driver circuit which occupied the area of 0.152 mm^2. (b) The comparison of a single-stage circuits area for 8-TFTs-ASG driver circuit.

7.4 Summary of this Chapter

After optimization of Chap. 6, the optimized circuits were fabricated using the standard 4-μm a-Si:H TFT technology. For the 14-TFTs-ASG driver circuit, the optimized ripple voltage was improved which is 71$\%$ reduction as compared with original fabricated result. Also, the improvement of ripple voltage of optimized 8-TFTs-ASG driver circuit is 49$\%$. Additionally, there are 2$\%$ and 36$\%$ reduction of chip area for 14-TFTs-ASG and 8-TFTs-ASG driver circuits, respectively.

Chapter 8

Conclusions

In this chapter, we have drawn the conclusion. In the Sec. 8.1, we summarize the work and suggested future work of the suppressing 16-nm MOSFET characteristic fluctuation. Then in Sec. 8.2 the work and suggested future work of TFT-LCD ASG driver circuit design optimization are summarized.

8.1 Suppression of 16-nm MOSFET Characteristic Fluctuation

8.1.1 Summary

In this thesis, an experimentally validated three-dimensional ”atomistic” coupled device circuit simulation approach has been advanced to investigate the dependence of random dopants fluctuation in nano-MOSFET analog circuit, concurrently capturing the random discrete-dopant-number- and random discrete-dopant-position-induced fluctuations. The results have shown that the discrete-dopant fluctuated current mirror circuit exhibits 8.43$\%$ variation of current mismatch. Additionally, there are 4.04$\%$, 9.37$\%$, and 4.05$\%$ variation for circuit gain, 3dB bandwidth, and unity-gain bandwidth of common source amplifier, respectively. Result has also confirmed the importance of discrete-dopant-position induced characteristic fluctuations in nanoscale transistors, which may be underestimated in analytical or compact modeling approach. To further suppress the characteristic fluctuations of devices as well as dynamic characteristic fluctuations of circuits, we have estimated DMG and inverse DMG techniques for suppressing RD-induced characteristics fluctuations for 16-nm MOSFET devices. The device with DMG exhibits the most effective way to reduce DC characteristic fluctuations, compared with the inverse DMG and control devices. the improvement of DMG for suppressing the RDF-induced V_{th}, I_{on}, and I_{off} fluctuation are

28%, 12.3%, and 59%, respectively, which is a enthralling method compared with other suppression techniques. However, the AC characteristics doesn't suppressed due to the capacitance of depletion region is affected by doping distribution of channel region and effective oxide thickness. Hence, the asymmetric scenario of LAC and inLAC devices in 16 nm MOSFET are future explored in its capacitance and dynamic characteristic fluctuations. The inLAC device exhibits less characteristic fluctuations due to the well controlled of major fluctuation source of C_{gd}. The fluctuations of average gate capacitance, circuit gain, 3dB bandwidth, and unity-gain bandwidth of the LAC device are substantially larger than those of inLAC device. Moreover, in contrast to the control device, the fluctuations of V_{th}, I_{on}, g_m, r_o, C_g, circuit gain, 3dB bandwidth, and unity-gain are simultaneously reduced by 33.4%, 32.8%, 11.9%, 80.6%, 68.8%, 31.2%, 37.6% and 47%, respectively, as summarized in Fig. 8.1. Moreover, the current mismatch of proposed suppression technique is also significantly reduced to only 4.66%. Finally, the comparison of suppression techniques such as, EOT is reduced to 0.4 [69] and increase WK [26], is listed in Table 8.1. According to comparative examinations and discussions throughout this thesis, the proposed inLAC device demonstrates very different fluctuation behaviors of DC and dynamic characteristics, compared with LAC and control device, which may used for the design of novel sub-20-nm MOSFETs. This study provides an insight into the design of doping profile to suppress the random-dopant-induced characteristic fluctuations and show the design trade-off between performance and fluctuation.

Table 8.1: The comparison of suppression techniques.

Improvement	DMG	inLAC	reduce EOT to 0.4 [106]	incease WK [27]
V_{th} fluctuation	✓	✓	✓	–
I_{on} fluctuation	✓	✓	✓	–
I_{off} fluctuation	✓	×	✓	–
g_m fluctuation	×	✓	–	–
r_o fluctuation	×	✓	–	–
C_g fluctuation	×	✓	–	–
Circuit Gain	×	✓	–	–
3dB Bandwidth	×	✓	–	–
Unity-gain Bandwidth	×	✓	–	–

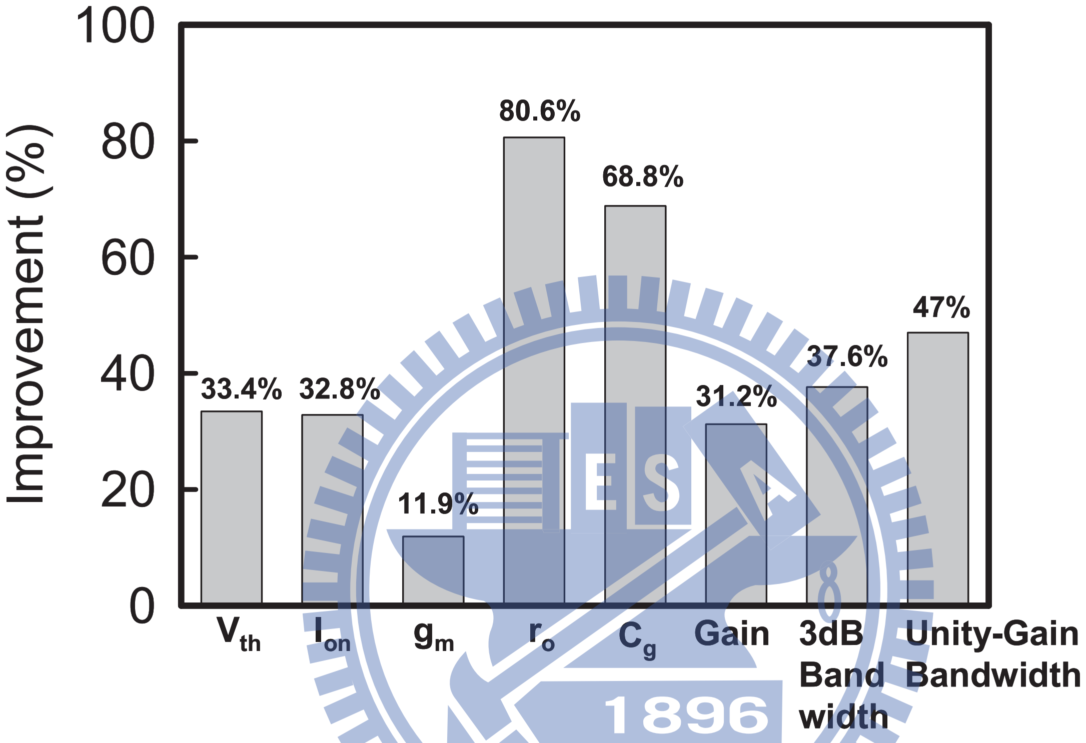


Figure 8.1: The effectiveness of the fluctuation suppression in both the inLAC-device and common source amplifier, compared with the results of control-device and circuit.

8.1.2 Future Work

We have discussed the random-dopant-effect induced characteristics fluctuation of 16-nm-gate length planar MOSFET and analog circuits in this thesis. Although the LAC device is a superior approach to suppress RDF-induced characteristic fluctuations of device and circuit, the gate leakage is extremely important for analog circuits of mobile phone application and the fluctuation of gate leakage should be examined. Moreover, we believe that the mismatch of threshold voltage in the larger circuit such as differential amplifier and LNA circuits will significantly impact the performance in the future. Additionally, the high-κ metal gate is emerging technology in the manufacturing of devices and brings two kinds of new random variation sources: (1) work-function dependency due to the metal grain orientation and (2) traps in Si/high-κ interface [100-105], which should be taken consideration in nanoscale device and circuit.

8.2 Design Optimization of TFT-LCD ASG Driver Circuit

8.2.1 Summary

In this thesis, we have demonstrated two optimized amorphous silicon gate (ASG) driver circuits for manufacturing using the simulation-based evolutionary approach. This approach combines genetic algorithm (GA) with circuit simulator on the unified optimization framework to execute the optimization flow automatically. It successfully extracts the designed parameters in these circuits. Figure 8.2 shows the summery of this study. The ripple voltage of 14-TFTs-ASG driver circuit is significantly decreased from 5.419 V to 1.904 V while we simultaneously maintain its dynamic characteristics within the required specifications. As for the 8-TFTs-ASG driver, the rise time and fall time are also reduced from 2.9827 μs and 2.6435 μs to 1.9166 μs and 1.9828 μs while maintaining the power dissipation within its specification. Sensitivity analysis has further shown promising and stable electrical characteristics of optimized parameters. The optimized ASG driver circuits were fabricated using standard process of 4-μm a-Si TFTs technology. The experimental results of 14-TFTs-ASG driver circuit is close to simulation results and the improvement of ripple voltage is 71% as compared with original fabrication. As for the 8-TFTs-ASG driver circuit, the improvement of ripple voltage is 49% while maintain the same dynamic characteristics as compared with original fabrication. Additionally, there are 2% and 36%

reduction of 14-TFTs-ASG and 8-TFTs-ASG driver circuit area. Consequently, this approach is highly extensible to design different functional block of display panel circuits.

	14-TFTs-ASG Driver Circuit				
Application	Monitor and screen of TV				
State	Spec.	Origi. Sim.	Opt. Sim.	Origi. Fab.	Opt. Fab.
Rise Time (μs)	< 1.5	0.818	1.234	0.75	1.22
Fall Time (μs)	< 1.5	0.814	1.188	0.76	1.17
Ripple (V)	< 3	5.419	1.904	6.9	1.9
RMS Power (mW)	< 60	56.166	42.634	--	--
Total Device Width (μm)	--	13110	8570	--	--
Circuit Area (mm^2)	--	--	--	0.236	0.231
	8-TFTs-ASG Driver Circuit				
Application	Display panel of cell phone				
State	Spec.	Origi. Sim.	Opt. Sim.	Origi. Fab.	Opt. Sim.
Rise Time (μs)	< 2	2.98	1.98	1.4	1.46
Fall Time (μs)	< 2	2.64	1.43	1.35	1.36
Ripple (V)	< 2	1.92	1.51	3.9	2.1
RMS Power (mW)	< 2	1.58	1.64	--	--
Total Device Width (μm)	--	2100	2620	--	--
Circuit Area (mm^2)	--	--	--	0.237	0.152

Figure 8.2: The dynamic characteristics and circuit area of ASG driver circuits are compared among specification, original simulation, optimized simulation, original fabrication, and optimized fabrication.

8.2.2 Future Work

We have successfully implemented the design optimization of ASG driver circuit by UOF in this thesis. However, the reliabilities such as temperature and bias-stress in ASG driver circuits are currently examined. Notably, layout technique of 14-TFTs-ASG driver circuit could be improved empirically for approaching to the theoretical estimation of 35% reduction of total layout. Additionally, more ASG driver circuits can be optimized by this approach and further examine the characteristics not only simulation but also measurement. Finally, we can improve the optimization kernel with hybrid approaches such as integrating the evolutionary algorithm, numerical optimization methods, and the empirical knowledge in our future work.

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Publication List:

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1. **Kuo-Fu Lee**, Zhong-Cheng Su, Yiming Li, Chih-Hong Hwang and Tien-Yeh Li, "Device and Circuit Level Suppression Techniques for Random-Dopant-Induced Static Noise Margin Fluctuation in 16-nm-Gate SRAM Cell" *Microelectronic Reliability,* vol. 50, no. 5, pp. 647-651, 2010.

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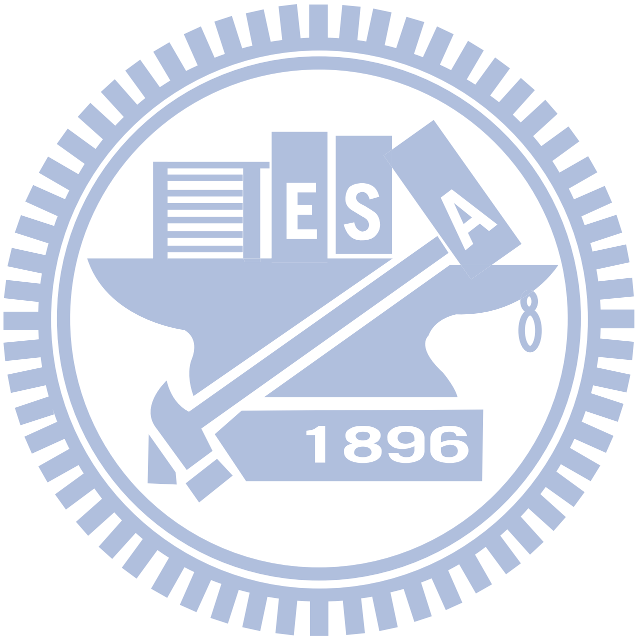
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