國 立 交 通 大 學

電信工程研究所

碩 士 論 文

新型低相位雜訊電流再利用四相位震盪器之設計與研究

Design of the New Architecture for Low Phase Noise Current-Reused Quadrature VCO

研究生：吳冠儀

指導教授：周復芳　博士

中　華　民　國　九　十　九　年　六　月

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碩　士　論　文

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中　文　摘　要

本論文討論分為兩部分，其中各部分所提出電路之晶片製作皆由 TSMC 0.18μm mixed-signal/RF CMOS 1P6M 製程來實現。

第一部分為一個採用後閘極耦合 (Back-Gate Coupled)方式產生四相位輸出之電流再利用震盪器。此四相位震盪器利用雙回授機制來達成改良型自發性轉移電導匹配 (Modified Spontaneous Transconductance Match, M-STM)，可有效降低 NMOS 與 PMOS 因製程變異對於轉移電導匹配上的影響，而可獲得更佳的輸出振幅平衡。根據量測結果顯示:本 QVCO 震盪頻率為 4.84 - 5.17 GHz，在供應電壓為 1.3V 之條件下，功率損耗約為 5.04mW，相位雜訊為 -117.4 dBc/Hz @ 1MHz，而 figure-of-merit (FOM)則為-184.07 dBc/Hz。

第二部分則提出一種新型的低雜訊電容耦合方式來完成注入鎖定，產生所需的四相位輸出訊號，並且利用此大訊號弦波輸出來達成尾端電流之自我偏壓切換 (Self-Switching Bias)，這種新型態的電容耦合與尾端電流自我偏壓切換震盪器可以同時達成低雜訊與低功率損耗的優點。根據量測結果顯示:本 QVCO 震盪頻率為 4.83-5.30 GHz，在供應電壓為 1.3V 之條件下，功率損耗約為 3.64mW，相位雜訊為 -125.8 dBc/Hz @ 1MHz，而 figure-of-merit (FOM)則為-193.87 dBc/Hz。

Design of the New Architecture for Low Phase Noise Current-Reused Quadrature VCO

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Abstract

This thesis consists of two parts. All the proposed circuits were implemented in TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology.

Part I presents a back-gate coupled current-reused quadrature VCO (CR-QVCO) which use double feedback mechanism to accomplish modified spontaneous transconductance match (M-STM) technique. This method is able to eliminate the transconductance difference between NMOS and PMOS transistors so that high output amplitude balance can be achieved. According to the measured results, the oscillation frequency is 4.84 - 5.17 GHz, and the power consumption is about 5.04mW at the supply voltage of 1.3V. The phase noise at 1MHz offset is -117.4dBc/Hz and the figure-of-merit (FOM) of the proposed QVCO is about -184.07dBc/Hz.

Part II proposes a novel low noise capacitor-coupling method to perform injection locking, and therefore quadrature signals at the output can be obtained. Moreover, by using these large signal sine-wave outputs to make the tail-current transistors self-switching, the advantage of lower phase noise and lower power consumption can be simultaneously achieved. According to the measured results, the oscillation frequency is 4.83 - 5.30 GHz, and the power consumption is about 3.64mW at the supply voltage of 1.3V. The phase noise at

1MHz offset is -125.8 dBc/Hz and the figure-of-merit (FOM) of the proposed QVCO is about -193.87 dBc/Hz.

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吳冠儀

於　新竹交通大學

2010 年　夏

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Chapter 1

Introduction

1.1 Background and Motivation

As increasing demand for personal wireless communications, the requirements of low-cost and low-power for wireless system have dramatically increased. Compact circuits, with minimum area, are required to reduce the equipment size and cost. Thus, we need a very high degree of integration, if possible a transceiver on a chip, either without or with a reduced number of external component. In addition to area and cost, it is very important to reduce the voltage supply and the power consumption. Wireless transceivers for many standards, including GSM, Bluetooth, WLAN, and Wireless Personal Area Network (WPAN) require low-power design techniques to enhance their battery lifetime and to improve their portability. At the same time, the development of advanced CMOS technology with the shrunk channel length is achieving higher cut-off frequency. Instead of bipolar and GaAs (Gallium Arsenide), CMOS is very attractive for RFIC due to the ability of system-on-chip (SOC) implementation. In addition to this benefit, scaling CMOS technology also satisfies the requirement of reduced cost and smaller size.

In the wireless transceiver blocks, phase-locked loops (PLL) are widely utilized such as frequency synthesizers, as shown in Fig. 1 - 1. Since the voltage-controlled oscillators (VCO) play a key role in the PLL circuits and the phase noise of the VCO directly affect the performance of the PLL circuits, the low-power and low-phase noise of VCOs are required.

Table 1 - 1 Wireless communication system characteristic

System	Cellular phones	WLAN		WPAN	
	WCDMA	802.11 b/g	802.11 a	Bluetooth	UWB
Frequency (GHz)	1.92~1.98 2.11~2.17	2.4~2.4835	5.15~5.35	2.4~2.48	3.1~10.6
Modulation	QPSK	QPSK/OFDM	OFDM	GFSK	DSSS or QPSK
Channel Bandwidth	5 MHz	20 MHz	20 MHz	1 MHz	528 MHz (QPSK)
Data Rate (bit/sec)	384 k/2 M	11/54 M	54 M	1 M	110/480 M (QPSK)

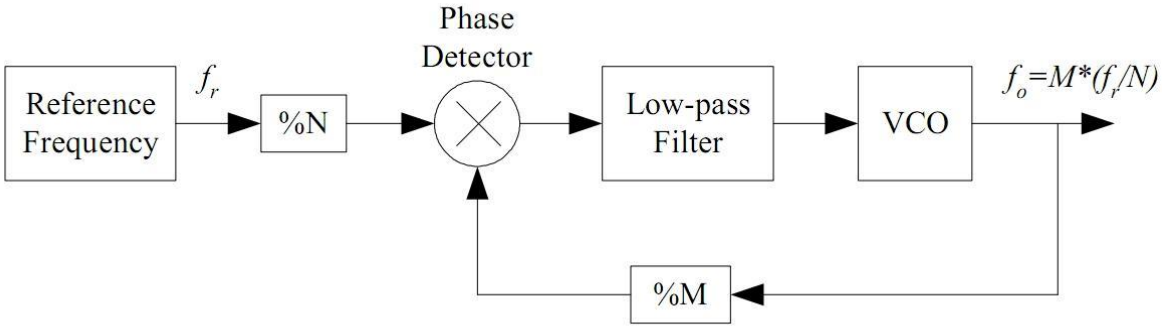

Fig. 1 - 1 Block diagram of PLL-based frequency synthesizer

Due to the requirements of quadrature local oscillator (LO) generation for up-conversions and down-conversions with image-reject mixing in wireless transceiver blocks, a quadrature VCO (QVCO) with quadra-phase outputs is a general design.

In 2002, the Federal Communications Commission (FCC) has allocated 7500 MHz of spectrum for ultra-wideband (UWB) system in 3.1~10.6 GHz frequency range [1]. According to FCC's definition, UWB system occupied a bandwidth is equal to or greater than 500MHz

when center frequency is over than 2.5GHz, or has a fractional bandwidth is equal to or greater than 20% of the center frequency when the center frequency is less than 2.5GHz. There are two proposals for UWB system: DS-CDMA (Direct-Sequence Code Division Multiplexing Access) and MB-OFDM (Multi-Band Orthogonal Frequency Division Multiplexing).

DS-CDMA uses a sequence of Gaussian monocycle pulses which their spectrum is spread as in Fig. 1 - 2. The lower band occupies the spectrum from 3.1 to 4.85 GHz and the upper band occupies the spectrum from 6.2 to 9.7 GHz [2]. The 5-6 GHz band is dedicated to WLAN 802.11a systems.

In MB-OFDM UWB, see Fig. 1 - 3, frequency span is grouped into five major band groups which are in turn sub-divided into 14 bands in total, each band is 528 MHz bandwidth [3] .

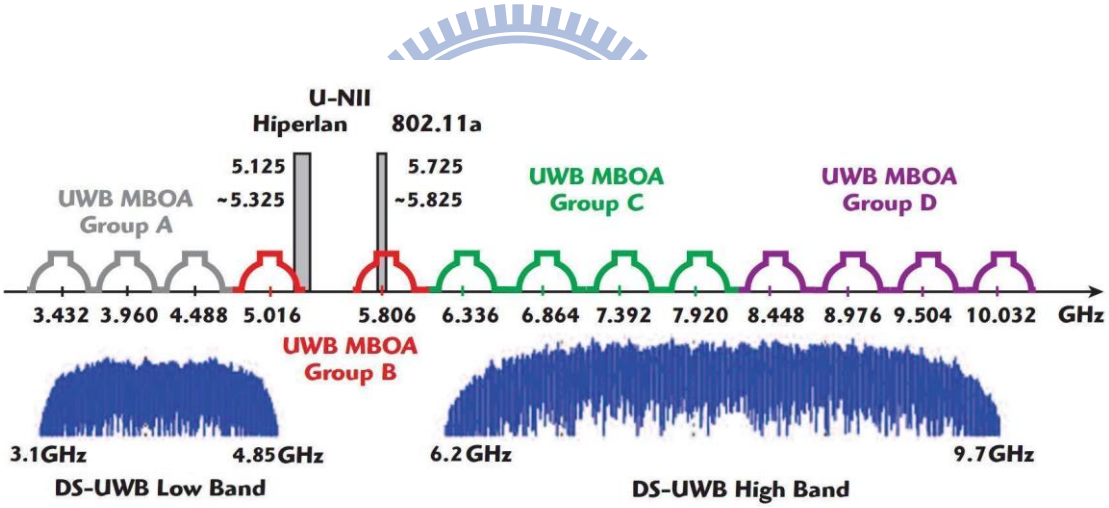

Fig. 1 - 2 DS-UWB spectrum allocation

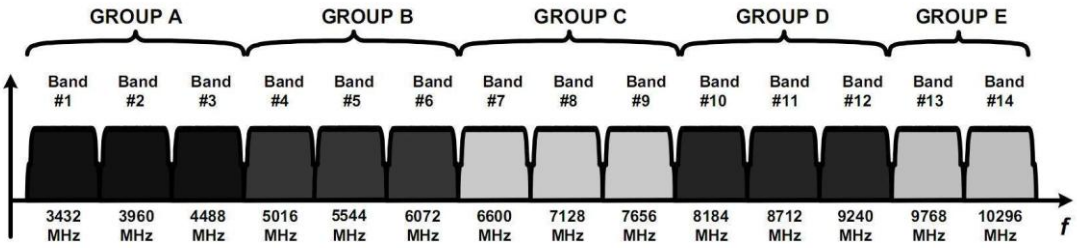

Fig. 1 - 3 Multi-band spectrum allocation

1.2 Oscillator Fundamental

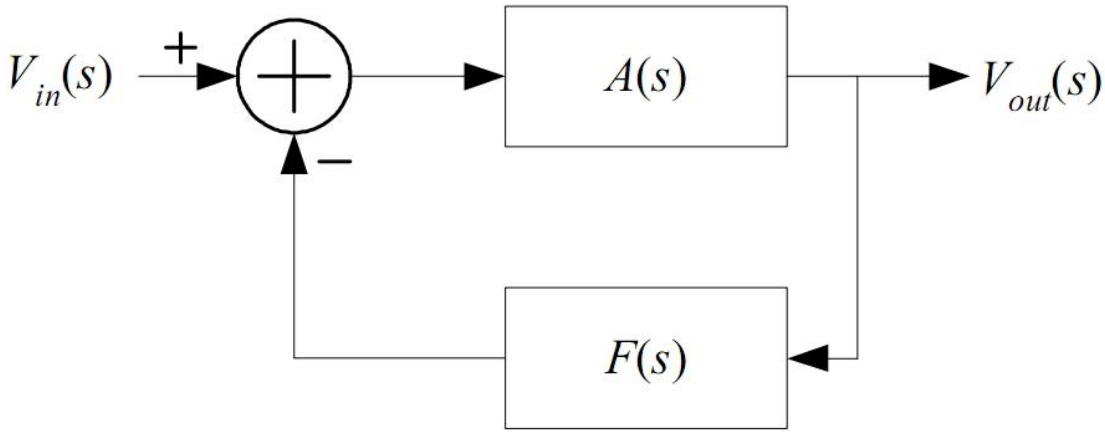

Fig. 1 - 4 Block diagram of negative feedback systems

In spite of oscillators are nonlinear in nature, they are usually viewed as a linear time-invariant feedback system as shown in Fig. 1 - 4. Although we can easily write the two block diagram, which are a gain block and a feedback block, to describe the negative feedback system, the main design issues are in the details of how these two circuits interact and how this interaction cause oscillation to occur. In the s-domain, the transfer function of this negative feedback system is given by

$$\frac{V_{out}}{V_{in}}(s) = \frac{A(s)}{1 + A(s)F(s)} \tag{1. 1}$$

The denominator of the transfer function goes to zero when the loop gain A(s)F(s) is equal to –1 at a specific frequency ω_o, implying that there is an output without a driving input signal, just what is needed for an oscillator. This is the well-known "Barkhausen criteria" and they allow the circuit designer to look at the amplifier and feedback blocks to determine the conditions for oscillation. Note that Barkhausen criteria are necessary but not sufficient for oscillation.

1.3 Phase Noise

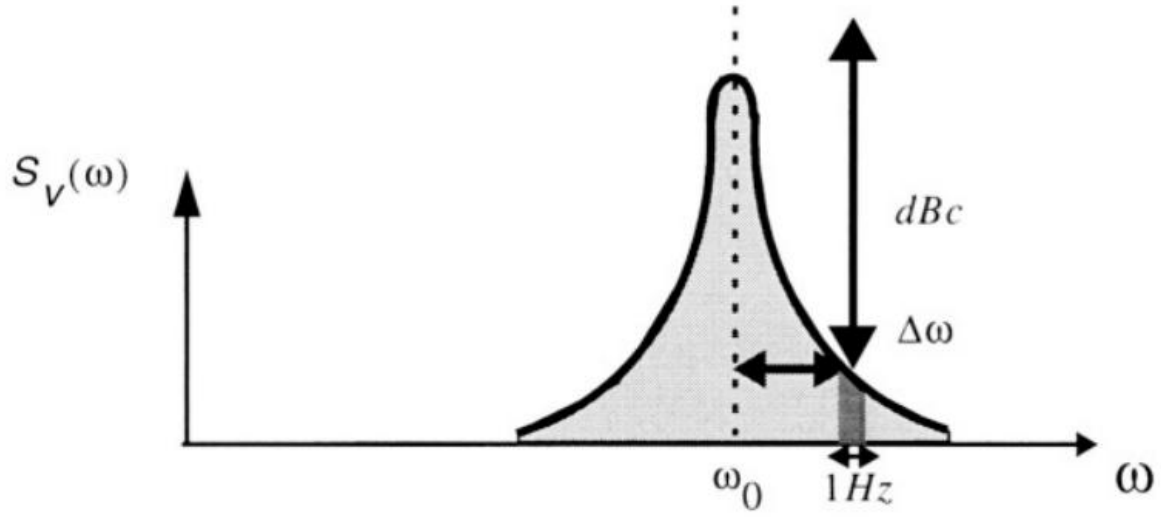

Fig. 1 - 5 The phase noise per unit bandwidth

The output purity of VCOs is quantified as phase noise, i.e., the cyclic uncertainty induced by the noise of the active and passive devices. The phase noise is defined as "the relative noise power per unit bandwidth at certain offset with respect to the carrier power". That is,

$$L_{tot}\{\Delta\omega\} = 10\log\left[\frac{P_{sideband}(\omega_o+\Delta\omega, 1Hz)}{P_{carrier}}\right] \quad (1.2)$$

where $P_{sideband}(\omega_o+\Delta\omega,1Hz)$ represents the single sideband power at a frequency offset, $\Delta\omega$, from the carrier in a measurement bandwidth of 1Hz, as shown in Fig. 1 - 5, and $P_{carrier}$ is the total power under the power spectrum.

Phase noise is the most critical parameter in the design of a high performance voltage controlled oscillator (VCO). Any practical oscillator has fluctuations in both the amplitude and the phase. Such fluctuations are caused by both the internal noise generated by passive and

active devices and the external interference coupled from the power supply or substrate. The amplitude noise is usually less important in comparison with the phase noise for oscillators, since it is suppressed by the intrinsic nonlinear nature of oscillators. Hence, the amplitude fluctuations will fall away after a period of time in oscillators. The concept of amplitude restoration can be visualized in the state-space portrait of the oscillator shown in Fig. 1 - 6, [33]. The effect of this restoring mechanism is pictured as a closed trajectory in state-space. The state of the system finally approaches this trajectory, called a limit cycle, irrespective of its starting point. On the other hand, the phase noise will be accumulated, resulting in the severe performance degradation of the system where the oscillator is used. Therefore, wireless communication systems usually impose strict specifications on the phase noise performance. If one plots $L_{total}\{\Delta\omega\}$ for a free-running oscillator as a function of $\Delta\omega$ on logarithmic scales, regions with different slopes may be observed as shown in Fig. 1 - 7, [33]. At large offset frequencies, there is a flat noise floor. At small offsets, one may identify regions with a slope of $1/f^2$ and $1/f^3$, where the corner between $1/f^2$ and $1/f^3$ regions is called ω_{1/f^3}. Finally the spectrum becomes flat again at very small offset frequencies.

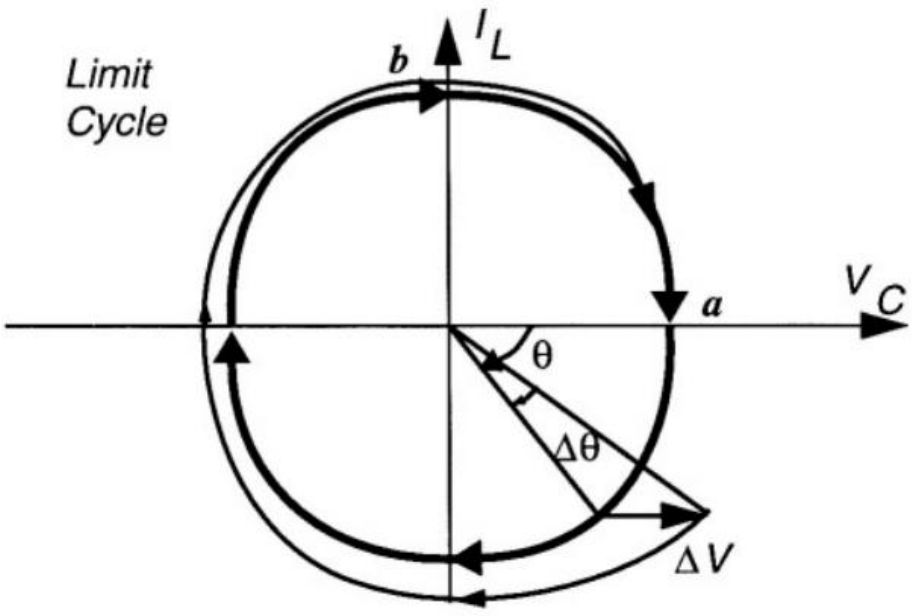

Fig. 1 - 6 Limit-cycle due to amplitude restoring mechanism , [33]

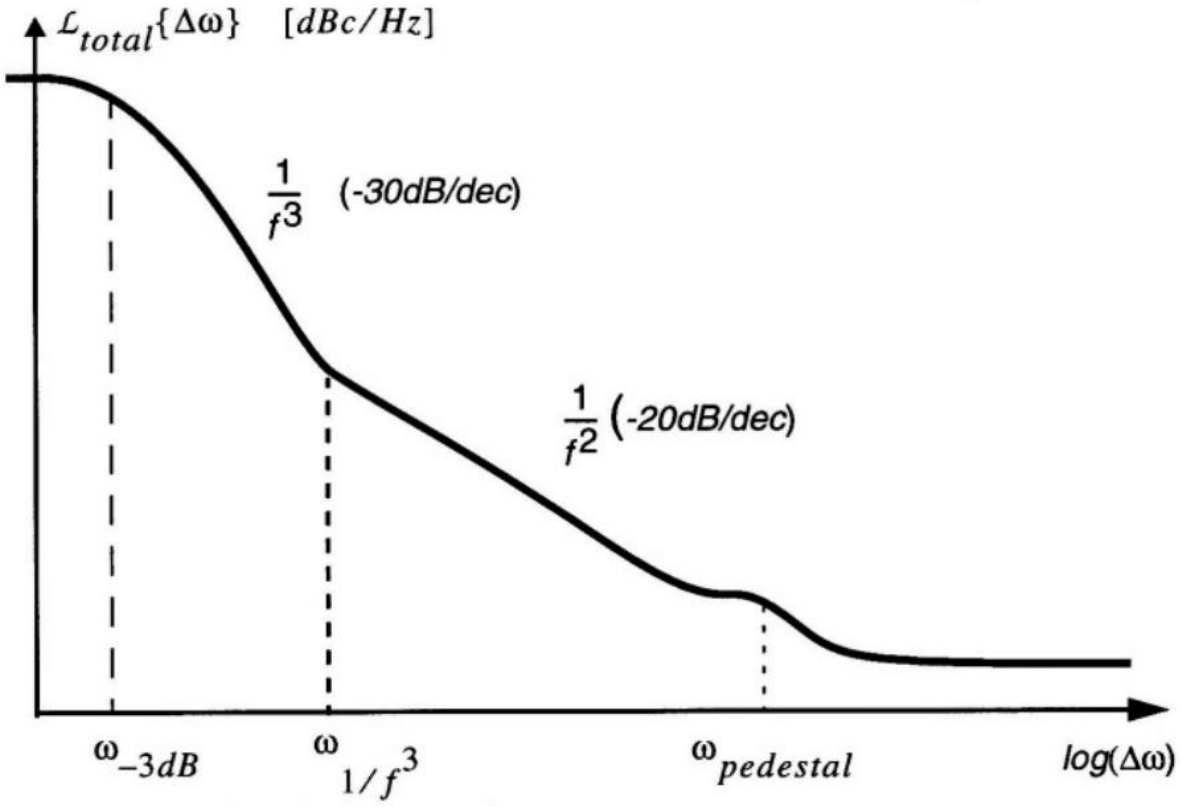

Fig. 1 - 7 A typical phase noise plot for a free running oscillator, [33]

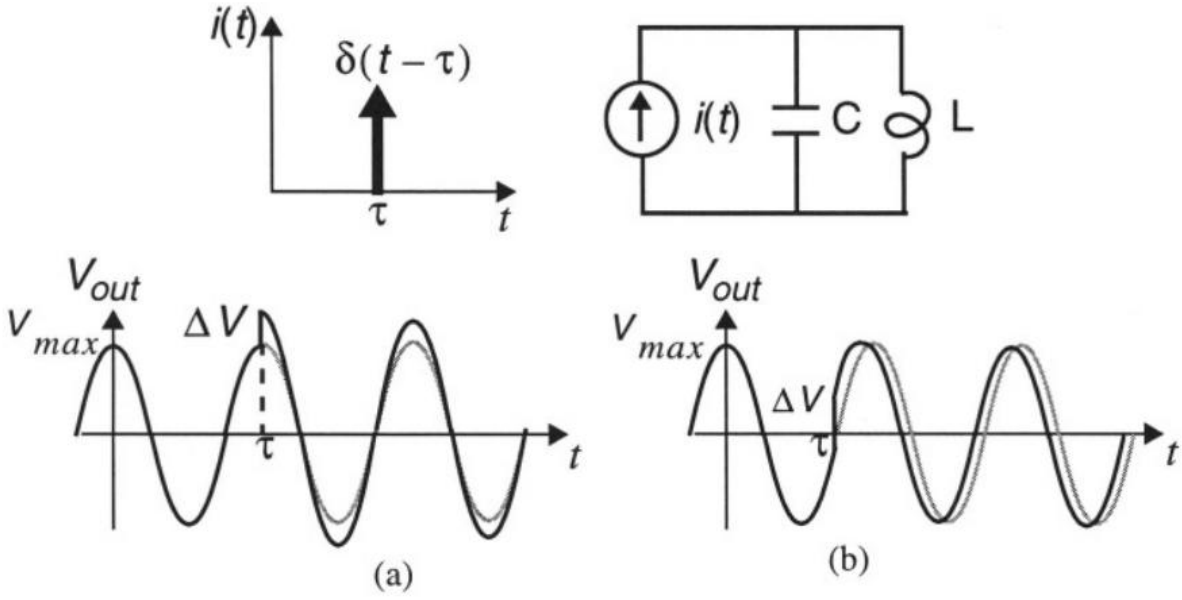

Fig. 1 - 8 Impulse response of an ideal LC oscillator, [33]

The phase-noise model proposed by Hajimiri and Lee in [33] is based on the impulse sensitivity function (ISF), which is a measure of the sensitivity of the oscillator to an impulsive input. It is a dimensionless periodic function in 2π that is independent of the output frequency and amplitude, describing phase shift result from applying a unit impulse at any point in time. Fig. 1 - 8 illustrates this sensitivity for an LC resonator with the impulse applied at the zero crossing and the peak of its output waveform [33]. If one injects an impulse of current at the voltage maximum, only the voltage across the capacitor changes; there is no effect on the current through the inductor. Therefore, the tank voltage changes instantaneously, as shown in Fig. 1 - 8 (a). On the other hand, if this impulse is applied at the zero crossing, it has the maximum effect on the excess phase, $\phi(t)$, and the minimum effect on the amplitude, as depicted in Fig. 1 - 8 (b).

For a small injected charge Δq, the resulting phase shift $\Delta\phi$ is proportional to the voltage change, ΔV, and hence to the injected charge, Δq. Therefore $\Delta\phi$ can be written as

$$\Delta\phi = \Gamma(\omega_O\tau)\cdot\frac{\Delta V}{V_{max}} = \Gamma(\omega_O\tau)\cdot\frac{\Delta q}{q_{max}} \qquad \Delta q \ll q_{max} \qquad (1.3)$$

where V_{max} is the voltage swing across the capacitor and q_{max} is the maximum charge swing. The function, $\Gamma(\omega_O\tau)$, is the so-called impulse sensitivity function (ISF). As long as the injected charge is small, the equivalent systems for amplitude and phase can be fully characterized using their linear time-variant unit impulse response, $h_\phi(t,\tau)$ and $h_A(t,\tau)$. Note that the introduced phase shift persists indefinitely, the unity phase impulse response can be easily calculated from above equation to be

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_O\tau)}{q_{max}}\cdot u(t-\tau) \qquad (1.4)$$

Therefore, the output excess phase can be calculated using the superposition integral as

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) \cdot i(\tau)\, d\tau = \int_{-\infty}^{\infty} \frac{\Gamma(\omega_O \tau)}{q_{max}} \cdot i(\tau)\, d\tau \qquad (1.5)$$

where $i(\tau)$ represents the input noise current injected into the node of interest. Since the ISF is periodic, it can be expanded in a Fourier series as

$$\Gamma(\omega_O \tau) = c_0 + \sum_{n=1}^{\infty} c_n \cos(n\omega_O \tau + \theta_n) \qquad (1.6)$$

where the coefficients c_n are real-valued, and θ_n is the phase of the nth harmonic. Using equation (1.6) for $\Gamma(\omega_O \tau)$ in the superposition integral and exchanging the order of summation and integration, the following is obtained

$$\phi(t) = \frac{1}{q_{max}} \left[c_0 \int_{-\infty}^{t} i(\tau)\, d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_O \tau)\, d\tau \right] \qquad (1.7)$$

Equation (1.7) identifies individual contribution to the total $\phi(t)$ for an arbitrary input current i(t) injected into any circuit node, in terms of various Fourier coefficients of the ISF. The decomposition implicit in equation (1.7) can be better understood with the equivalent block diagram shown in Fig. 1 - 9, [33].

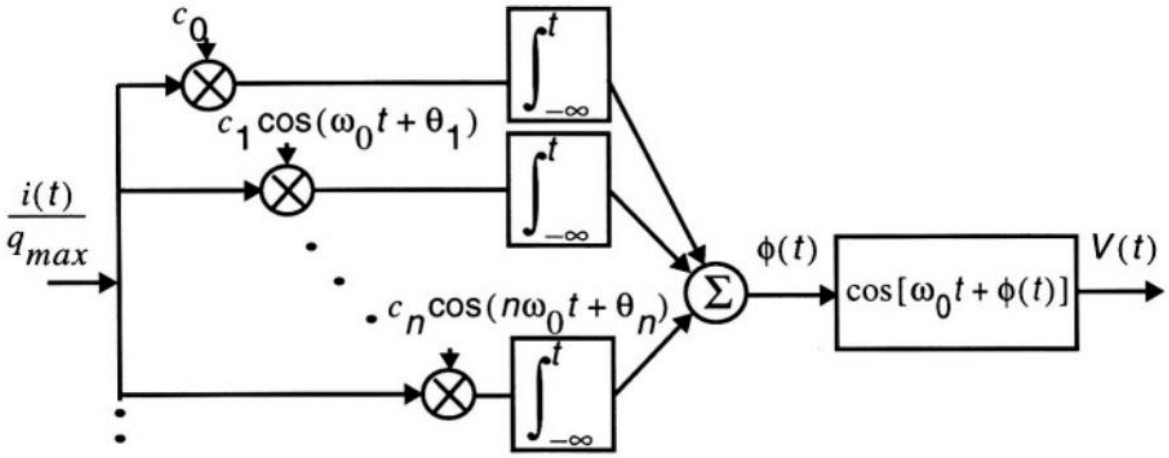

Fig. 1 - 9 The equivalent system for ISF decomposition, [33]

To investigate the effect of low frequency perturbations on the oscillator phase, a low frequency sinusoidal perturbation current, $i(t)=I_0\cos(\Delta\omega t)$, is injected into the oscillator at a frequency of $\Delta\omega \ll \omega_O$. The arguments of all the integrals associated with c_n, n=1,...∞ in equation (1.7) are at frequency higher than $\Delta\omega$ and are significantly attenuated by the averaging nature of the integration, except the term arising from the first integral (the first branch in the equivalent block diagram of Fig. 1 - 9), which involves c_0. Therefore, the resulting excess phase can be approximated as

$$\phi(t)=\frac{I_0\sin(\Delta\omega t)}{q_{\max}\cdot\Delta\omega}+\sum_{n=1}^{\infty}\frac{I_0 c_n}{2\cdot q_{\max}}\left[\frac{\sin((n\omega_O+\Delta\omega)\cdot t)}{n\omega_O+\Delta\omega}+\frac{\sin((n\omega_O-\Delta\omega)\cdot t)}{n\omega_O-\Delta\omega}\right]$$

$$\phi(t)\cong\frac{I_0 c_0\sin(\Delta\omega t)}{q_{\max}\cdot\Delta\omega} \qquad (1.8)$$

As a result, there will be two impulses at $\pm\Delta\omega$ in the power spectral density of $\phi(t)$, denoted as $S_\phi(\omega)$ as shown in Fig. 1 - 10, [33].

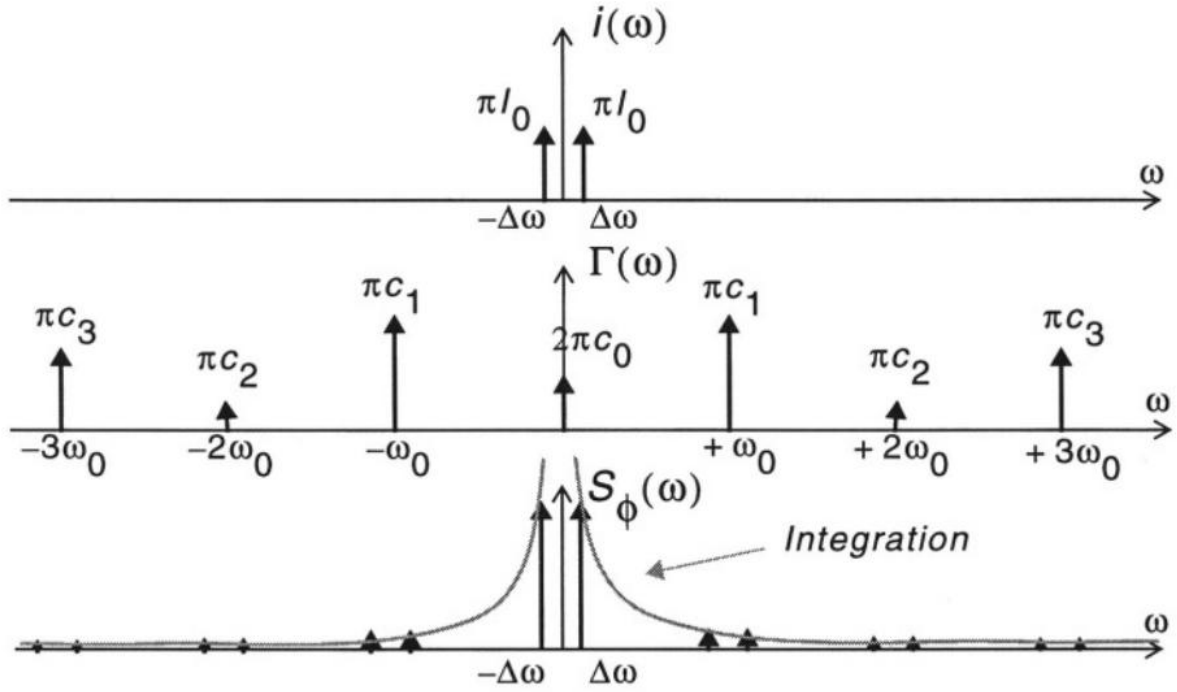

Fig. 1 - 10 Conversion of a low frequency sinusoidal current to phase, [33]

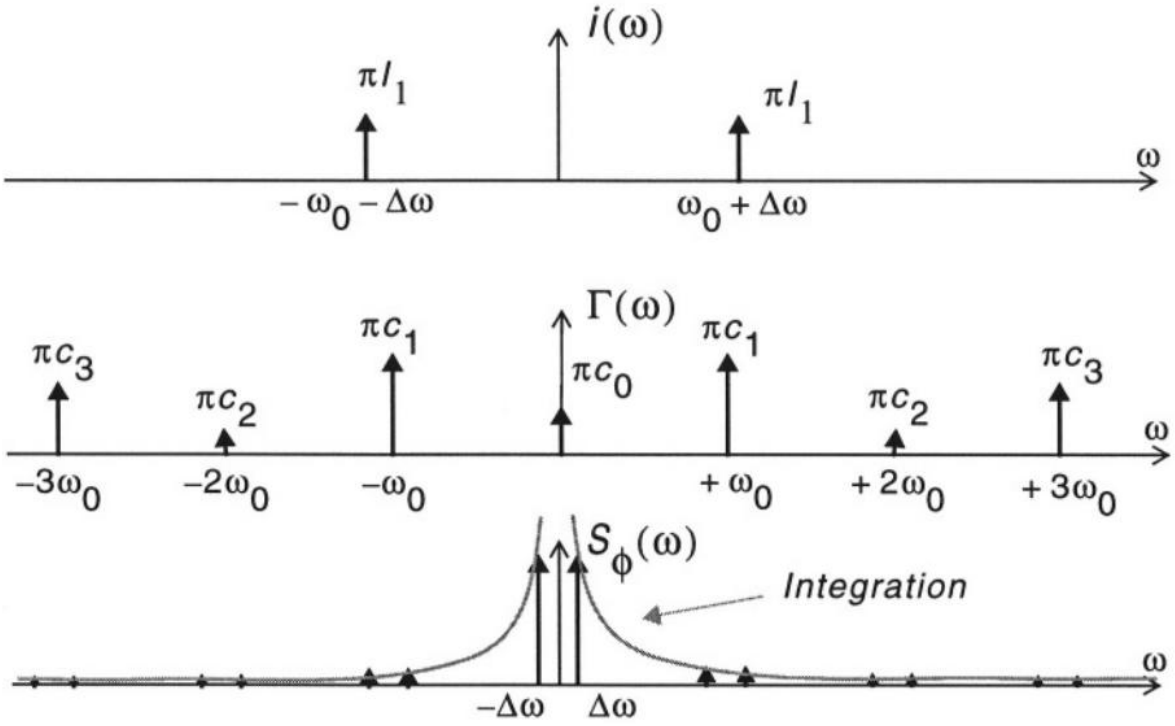

Fig. 1 - 11 Conversion of a tone in the vicinity of ω_o, [33]

As another important special case, consider a current at a frequency close to the oscillation frequency given by $i(t) = I_0 \cos\left[(\omega_O + \Delta\omega)t\right]$. A process similar to that of the previous case occurs except that the spectrum of i(t) consists of two impulses at $\pm(\omega_O + \Delta\omega)$, as shown in Fig. 1 - 11, [33]. This time the dominate term will be the second integral corresponding to n=1. Therefore, $\phi(t)$ is given by

$$\phi(t) \cong \frac{I_1 c_1 \sin(\Delta\omega t)}{q_{\max} \cdot \Delta\omega} \qquad (1.9)$$

which again results in two equal sidebands at $\pm\Delta\omega$ in $S_\phi(\omega)$.

The amount of phase error due to a given sinusoidal current can thus be calculated using equation (1.8) and equation (1.9). Computing the power spectral density (PSD) of the oscillator output voltage, $S_v(\omega)$, requires knowledge of how the output voltage relates to the excess phase variations. The phase-to-voltage conversion process for a single tone is now considered. For small value of $\phi(t)$, $\cos\left[\omega_O t + \phi(t)\right]$ can be approximate as

$$\cos\left[\omega_O t + \phi(t)\right] = \cos(\omega_O t)\cos[\phi(t)] - \sin(\omega_O t)\sin[\phi(t)]$$

$$\cos\left[\omega_O t + \phi(t)\right] \cong \cos(\omega_O t) - \phi(t)\sin(\omega_O t) \qquad (1.10)$$

$$\cos\left[\omega_O t + \phi(t)\right] \cong \cos(\omega_O t) + \frac{I_n c_n}{4 \cdot q_{\max}\Delta\omega}\left[\cos((\omega_O + \Delta\omega)t) - \cos((\omega_O - \Delta\omega)t)\right] \qquad (1.11)$$

where it is assumed that $\cos[\phi(t)] \cong 1$ and $\sin[\phi(t)] \cong \phi(t)$ for small values of $\phi(t)$. The excess phase is then converted to a pair of equal sidebands at $\omega_O + \Delta\omega$. The sideband power relative to the carrier can be calculated as

$$L(\Delta\omega) = 10\log\left[\frac{I_0^2 c_0^{\,2} + 2\sum_{n=1}^{\infty} I_n^2 c_n^2}{8q_{\max}^2 \Delta\omega^2}\right]^2 \qquad (1.12)$$

Consider a random noise current source $i_n(t)$, whose power spectral density has both a flat region and a $1/f$ region, as shown in Fig. 1 - 12, [33]. Equation (1.7) shows that noise components located near integer multiples of the oscillation frequency are weighted by Fourier coefficients of the ISF and integrated to form the low noise frequency noise sidebands for $S_\phi(\omega)$. These sidebands in turn become close-in phase noise in the spectrum of $S_v(\omega)$ through phase modulation (PM), as shown in Fig. 1 - 12. The definition of the ISF can be expanded to take into account the presence of cyclostationary noise sources such as the channel noise of a MOS transistor. Its statistical properties vary with time in a periodic manner because the noise power is modulated by the gate-source overdrive voltage.

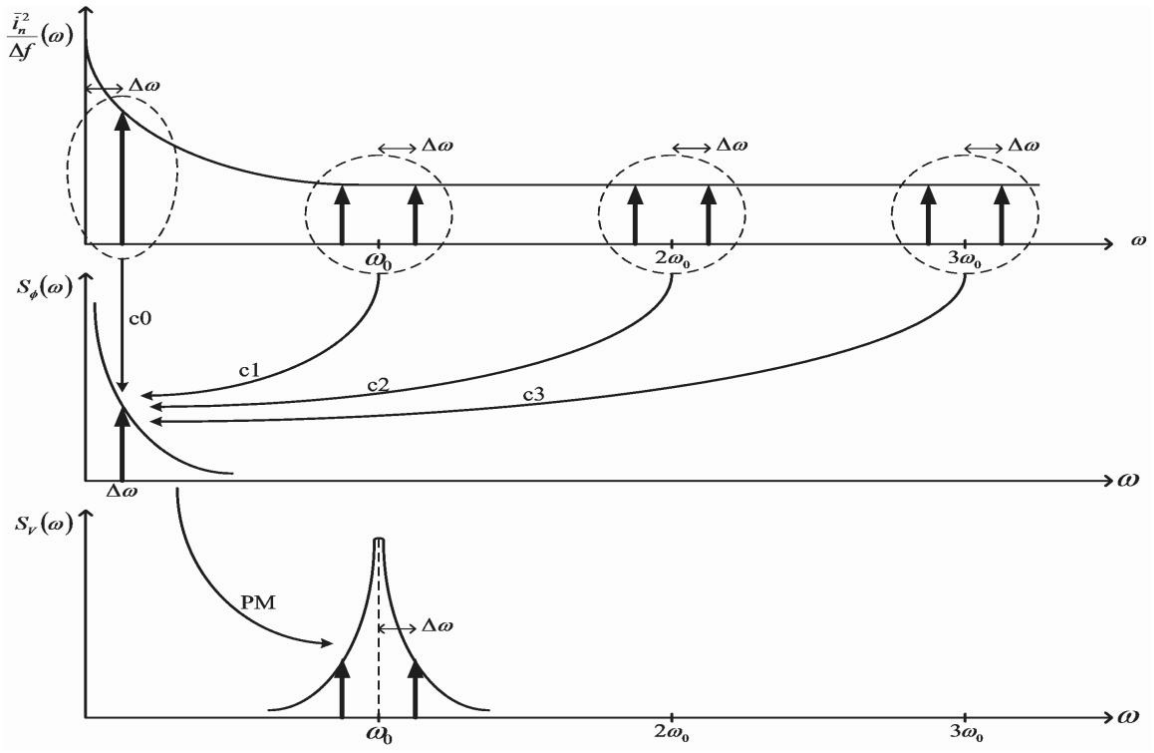

Fig. 1 - 12 Conversion of circuit noise to excess phase, and then to phase-noise sideband

Now consider with a white input noise current with power spectral density $i_n^2/\Delta f$. Note that I_n in equation (1.12) represents the peak and not the rms amplitude, hence, $I_n^2/2 = \overline{i_n^2}/\Delta f$ for $\Delta f = 1\text{Hz}$. Noise power around the frequency $n\omega_O + \Delta\omega$ causes two equal sidebands at $\omega_O \pm \Delta\omega$, as shown in Fig. 1 - 11. However, it is important to recognize that noise power at $n\omega_O - \Delta\omega$ also has a similar effect. Therefore, twice the power of noise at $n\omega_O + \Delta\omega$ should be taken into account, and hence equation (1.12) becomes

$$L(\Delta\omega) = 10\log\left[\frac{\left(c_0^2 + 2\sum_{n=1}^{\infty} c_n^2\right)\cdot\frac{\overline{i_n^2}}{\Delta f}}{8q_{\max}^2\Delta\omega^2}\right] \qquad (1.13)$$

According to Parseval's relation,

$$2\Gamma_{rms}^2 = \frac{1}{\pi}\int_0^{2\pi}|\Gamma(x)|^2\,dx = \frac{c_0^2}{2} + \sum_{n=1}^{\infty} c_n^2 \qquad (1.14)$$

where Γ_{rms} is the rms value of $\Gamma(x)$. As a result equation (1.13) becomes

$$L(\Delta\omega) = 10\log\left[\frac{\Gamma_{rms}^2\cdot\frac{\overline{i_n^2}}{\Delta f}}{2q_{\max}^2\Delta\omega^2}\right] \qquad (1.15)$$

This equation gives the phase noise spectrum of an arbitrary oscillator in the $1/f^2$ region of the phase noise spectrum.

Many active and passive devices exhibits low frequency noise with a power spectrum that is approximately inversely proportional to the frequency. It is for this reason that noise source with this behavior are referred to as $1/f$ noise. Noting that device noise in the $1/f$

region can be described by

$$\overline{i_{n,1/f}^2} = \overline{i_n^2} \cdot \frac{\omega_{1/f}}{\Delta\omega} \qquad \Delta\omega < \omega_{1/f} \qquad (1.16)$$

where $\omega_{1/f}$ is the corner frequency of device $1/f$ noise. Hence, the sideband power relative to the carrier in the $1/f^3$ portion of the phase noise spectrum can be expressed as

$$L(\Delta\omega) = 10\log\left[\frac{c_0^2 \cdot \frac{\overline{i_n^2}}{\Delta f} \cdot \frac{\omega_{1/f}}{\Delta\omega}}{8q_{\max}^2\Delta\omega^2}\right] \qquad (1.17)$$

The phase noise $1/f^3$ corner, $\Delta\omega_{1/f^3}$, is the frequency where the sideband power due to the white noise given by equation (1.15) is equal to the sideband power arising from the $1/f$ noise given by equation (1.17), as shown in Fig. 1 - 13.

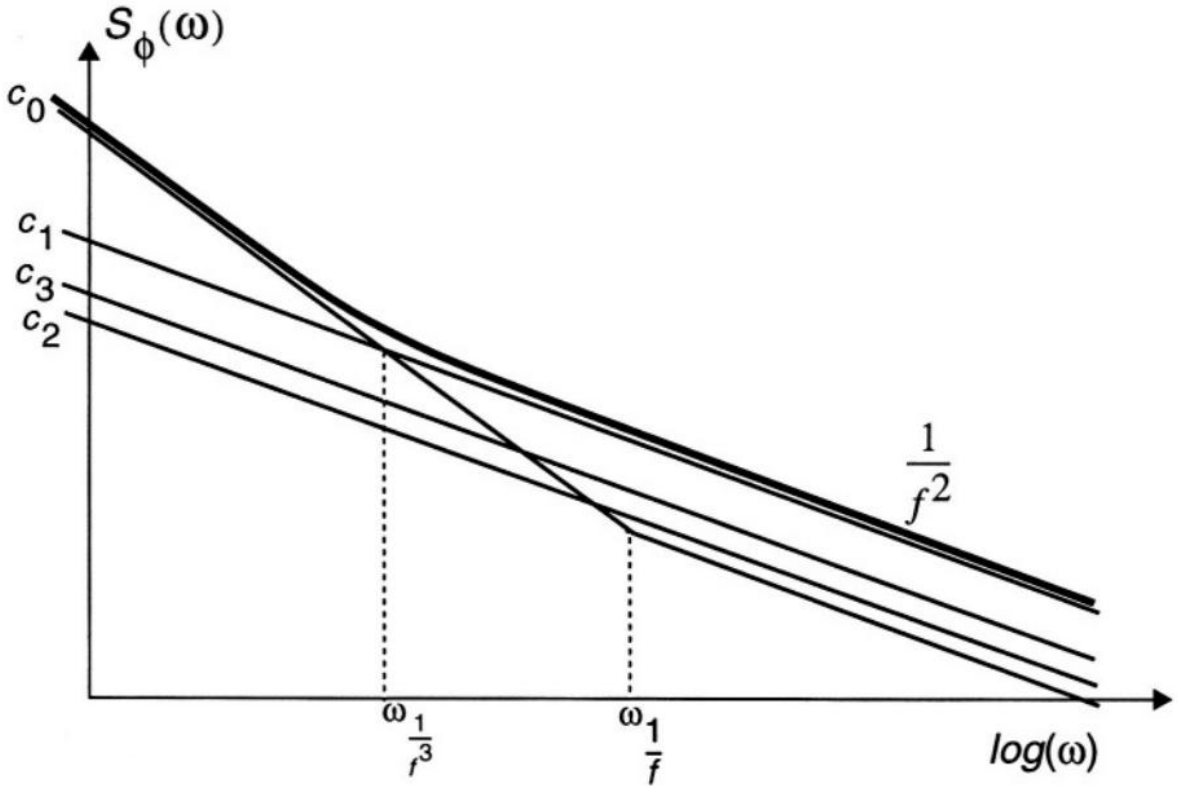

Fig. 1 - 13 $S_\phi(\omega)$ on a log-log axis, [33]

Solving for $\Delta\omega_{1/f^3}$ resulting in the following expression for the $1/f^3$ corner in the phase noise spectrum:

$$\Delta\omega_{1/f^3} = \omega_{1/f} \cdot \left(\frac{c_0}{\Gamma_{rms}}\right)^2 \tag{1.18}$$

As can be seen, the $1/f^3$ phase noise corner is not equal to the $1/f$ device noise corner but smaller by a factor equal to $\left(\frac{c_0}{\Gamma_{rms}}\right)^2$, where c_0 is the dc value of ISF,

$$c_0 = \frac{1}{2\pi}\int_0^{2\pi}\Gamma(x)dx \tag{1.19}$$

Therefore, if the circuit can be designed such that the ISF corresponding to each transistor noise source has no DC component, the flicker noise will not have any effect on the phase noise of the VCO.

A white cyclostationary noise current $i_n(t)$ can always be decomposed as

$$i_n(t) = i_{n0}(t)\alpha(\omega_O t) \tag{1.20}$$

where $i_{n0}(t)$ is a white stationary process and $\alpha(\omega_O t)$ is a deterministic periodic function describing the noise amplitude modulation and therefore is referred to as the noise modulating function (NMF). The NMF is normalized to a maximal value of one and can be easily derived from the device noise characteristics and noiseless steady-state waveform. Therefore, the expression for the excess phase resulting from a cyclostationary noise source can be written as

$$\phi(t) = \int_{-\infty}^{t} i_{n0}(\tau)\frac{\alpha(\omega_O t)\cdot\Gamma(\omega_O\tau)}{q_{max}}d\tau \tag{1.21}$$

As can be seen, cyclostationary noise can be treated as a stationary noise applied to a system with a new ISF given by $\Gamma_{NMF}(x) = \Gamma(x) \cdot \alpha(x)$ where $\alpha(\omega_O t)$ can be derived easily from device noise characteristics and the noiseless steady-state waveform.

In summary, the linear time-variant phase-noise model proposed by Hajimiri and Lee can accurately predict phase noise of most practical oscillators by taking into account the cyclostationary properties of the random noise sources. The introduced ISF accurately describes the contribution to phase perturbation by each individual noise source, allowing efficient optimization of phase noise performance.

1.4 Thesis Organization

In this thesis, two current-reused quadrature VCO (CR-QVCO) and a wideband CMOS down-converting mixer for W-band receiver are realized in TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology, another mixer with the integrated LO frequency doubler has also been proposed.

Chapter 1 discusses the motivation and challenges in low-phase-noise CMOS QVCO design, and gives a brief introduction to the oscillator and phase noise.

Chapter 2 presents a back-gate coupled current-reused quadrature VCO (CR-QVCO) which use feedback mechanism to accomplish modified spontaneous transconductance match (M-STM) technique. This method is able to eliminate the transconductance difference between NMOS and PMOS transistors so that high output amplitude balance can be achieved.

Chapter 3 will propose a novel low noise capacitor-coupling method to perform injection locking, and therefore quadrature signals at the output can be obtained. Moreover, by using these large signal sine-wave outputs to make the tail-current transistors self-switching, the advantage of lower phase noise and lower power consumption can be simultaneously achieved.

Chapter 4 gives the conclusions, summary of contributions, and future work plan.

Finally, Appendix focuses on a wideband CMOS down-converting mixer for W-band receiver application. This mixer has the RF frequency chosen to be 8.7-17.4GHz, LO frequency fix at 17.5GHz, and IF frequency close to DC~8.8GHz. In order to reduce the difficulty in designing the corresponding LO module, another mixer with the integrated LO frequency doubler has also been proposed.

Chapter 2

Current-Reused Quadrature VCO with Modified Spontaneous Transconductance Match

2.1 Introduction

Modern RF receivers and transmitters require oscillators with accurate quadrature and low phase noise. Since most of the current wireless communication systems are employing quadrature modulation, there have been various research results to obtain accurate quadrature local oscillator (LO) signals with low phase noise. For quadrature signals, in-phase and quadrature-phase (I/Q) match is an important requirement while meeting the requirements of low-phase noise and low power for integrated VCOs. The quadrature characteristics can be evaluated in terms of phase error and amplitude imbalance. Quadrature LO signals can be obtained in various ways:

I. A poly-phase filter (PFF) following a VCO running at the required LO frequency [4]. Usually, the PFF for quadrature phase shift is implemented with a passive RC network, which introduces power loss and additional phase noise. If a wide frequency range is required, high order PFF has to be used and the power loss and phase noise become much large. Additional power might have to be dissipated in the LO buffer compensating the power loss in the passive PFF[5].

II. A divide-by-two frequency divider following a VCO running at double the required LO

frequency, as shown in Fig. 2 - 1 (a). This method has the drawback of very large power consumption due to the high operating frequency of VCO and frequency divider.

III. By means of Quadrature coupling the differential VCOs[6]-[9], as shown in Fig. 2 - 1 (b). The quadrature coupling method is widely used because of its better phase noise performance. Therefore, in this chapter we use the quadrature coupling method to generate the quadrature LO signals.

In order to achieve low power consumption, current-reused VCO (CR-VCO) configuration is one of the most widely used solutions. Fig. 2 - 2 shows the schematic of the conventional NMOS-based current-reused VCO (CR-VCO) by stacking switching transistors in series like a cascode [10].

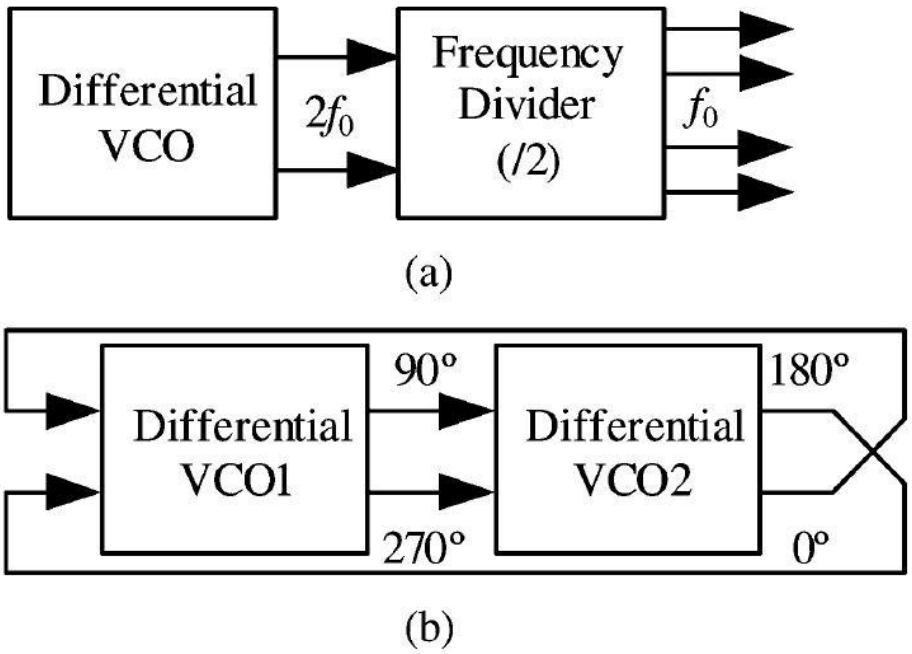

Fig. 2 - 1 Examples of quadrature signal generation methods
(a)frequency division (b)quadrature coupling

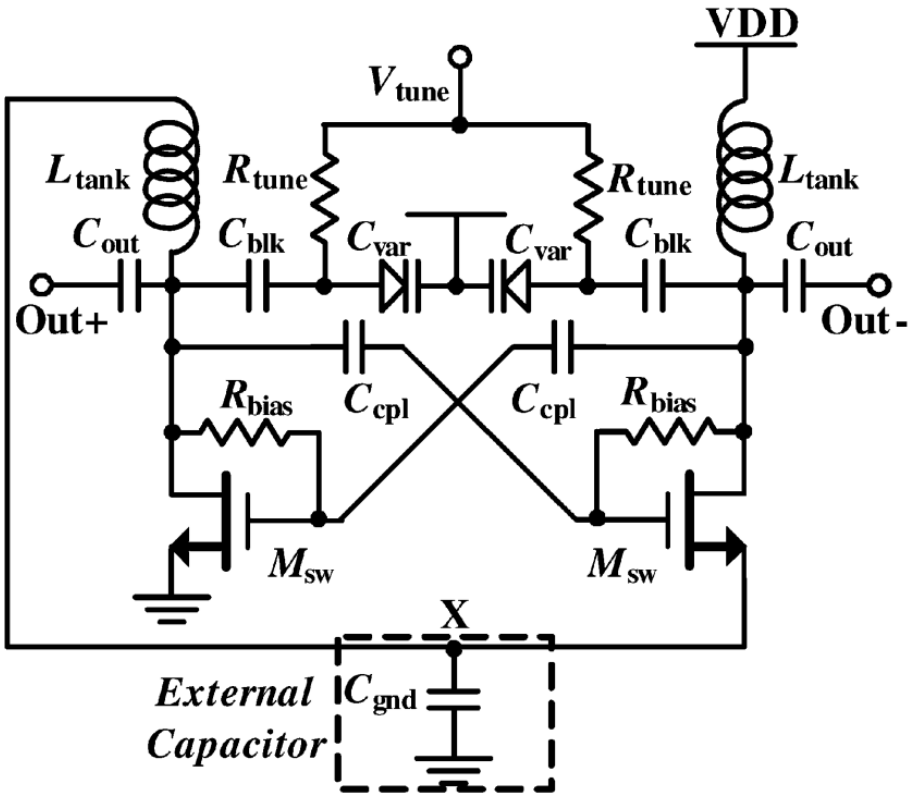

Fig. 2 - 2 Schematic of the conventional current-reused topology

Unfortunately, There are three drawbacks of this type CR-VCO. First, As compared to the generic VCO, the frequency tuning range of this type CR-VCO is narrower. Because the DC levels at the two sides of the varactors are different, the capacitors C_{blk} must be added for dc block and ac short to have the identical voltage drop across the varactors. Besides, the capacitors C_{cpl} and resistors R_{bias} should be added to biasing the transistors properly. Therefore, the capacitance tuning range C_{max} / C_{min} will be smaller due to the addition of extra capacitors. Involving too large number of capacitors and hence higher capacitive load at the output node also restrict the oscillation frequency. Second, A large capacitor C_{gnd}, even an external one, should be added at the node X. Since the node X is pulled up when each one of the differential NMOS turns on, the frequency at the node X is twice as the frequency at the VCO output. A large capacitor C_{gnd} should be used to have a tight ground effect, symmetric differential output swing and suppress the high frequency noise at node X. Third, the amplitude

imbalance of the output signals is relatively larger than the conventional cross-coupled VCO due to the unsymmetric circuit structure.

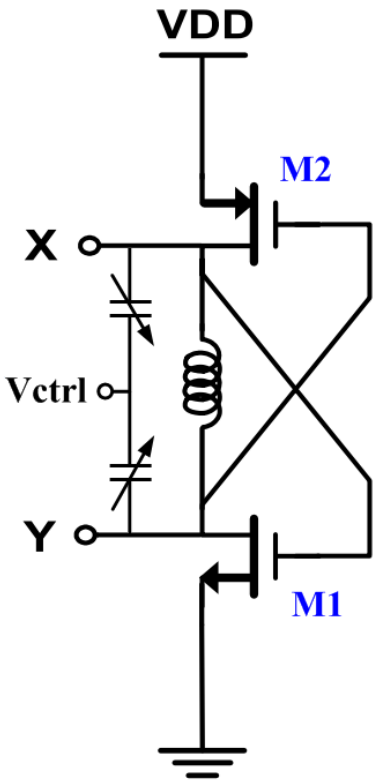

Fig. 2 - 3 Schematic of another conventional current-reused topology

Another type of CR-QVCO has been reported in [11], as shown in Fig. 2 - 3. It replaces one of the NMOS transistors of a conventional differential LC-VCO with a PMOS transistor. The biasing of this complementary current-reused VCO (CR-VCO) topology is much easier than the NMOS-based cascode current-reused VCO (CR-VCO) topology. That is, the DC levels at the two sides of the varactors are the same and no extra capacitors are needed. Therefore, the problem of involving too large number of capacitors and hence higher capacitive load at the output node can be solved.

Although the CR-QVCO using the configuration shown in Fig. 2 - 3 has excellent low power consumption, there is an drawback that the amplitude imbalance of the output signals

is relatively larger than the conventional cross-coupled VCO due to the asymmetric circuit structure. To solve this problem, a passive degenerative resistor is added at the source node of the NMOS transistor to balance the transconductance difference between PMOS and NMOS transistors. Unfortunately, this method requires an accurate resistance value to have good imbalance suppression and the inserted resistor dissipated an extra amount of power. The VCO reported in [18] used MOS transistors biased in the triode region as a variable resistor to replace the degenerative resistor. By connecting the gate terminals to the center-tapped inductor, which was called spontaneous transconductance match (STM) technique, the VCO is able to automatically eliminate the signal imbalance such that high amplitude balance and low power consumption can be simultaneously achieved without using any accurate resistors.

The circuit we proposed in this chapter has slightly modified the so-called STM-technique by connecting the gate terminals to the another side of the output. Because of feedback mechanism, much better performance of transconductance matching than original one can be achieved. We give it a name modified spontaneous transconductance match (M-STM) technique. The circuit design consideration will be discussed in next section.

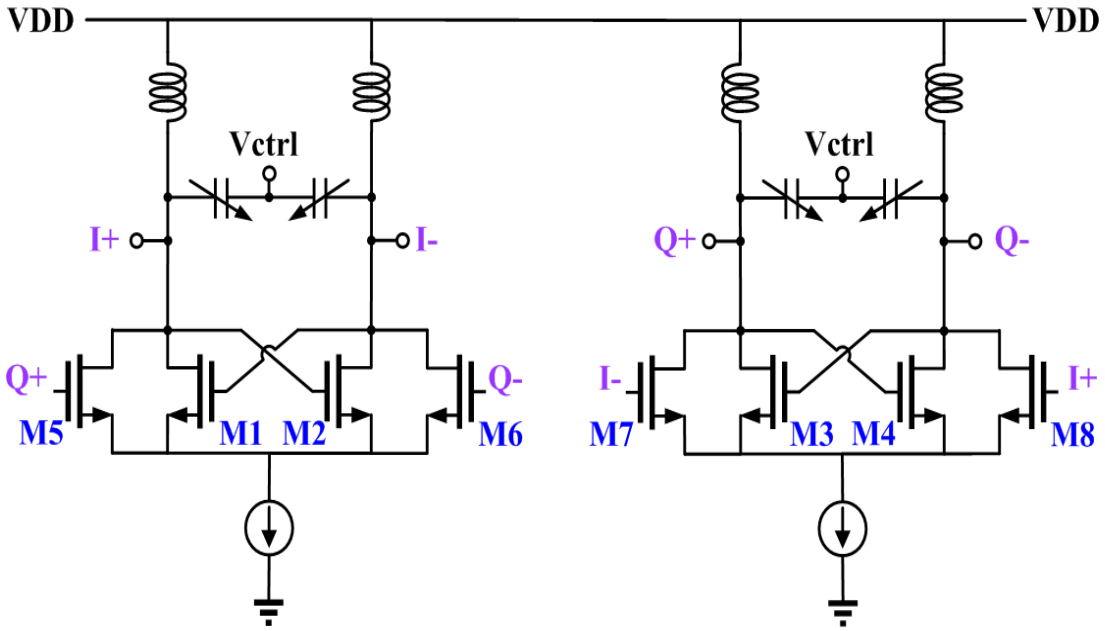

Fig. 2 - 4 Schematic of the conventional parallel-coupled QVCO (P-QVCO) topology

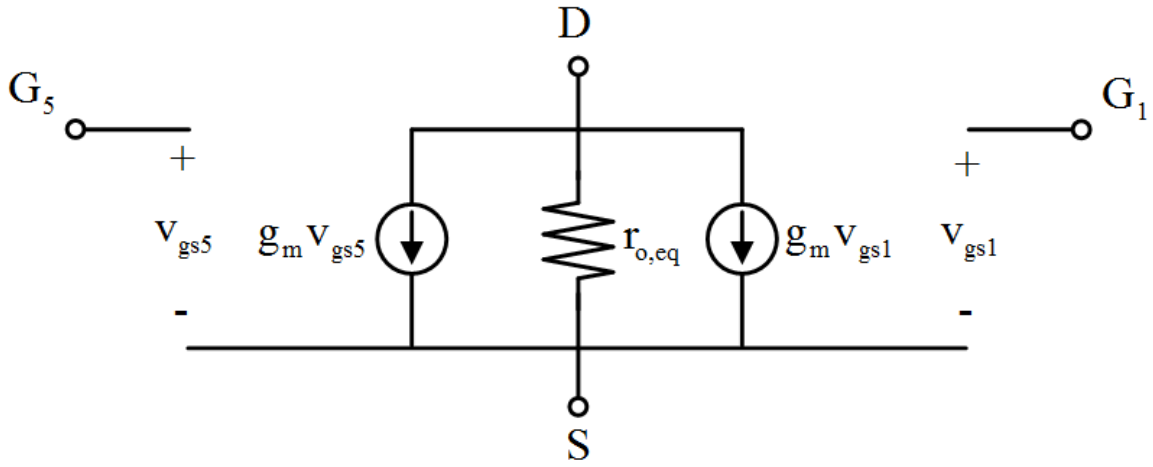

Fig. 2 - 5 Small signal equivalent circuit of the switching- and parallel-coupling transistor

Fig. 2 - 4 shows the conventional parallel QVCO (P-QVCO) where I and Q signals are generated by coupling two differential VCOs through coupling transistors M_5 - M_8 in parallel with switching transistors M_1 - M_4. Fig. 2 - 5 shows the small signal equivalent circuit of the switching and corresponding coupling transistors [6]. From Fig. 2 - 5, the coupling strength α between the two VCOs of the P-QVCO can be defined as

$$\alpha = \frac{g_{m,couple}}{g_{m,switching}} = \frac{g_{m5}}{g_{m1}} = \frac{W_5}{W_1}$$

where $g_{m,couple}$ and $g_{m,switching}$ are the transconductance of coupling transistor and switching transistor, respectively. In P-QVCO, the coupling strength α has a strong effect on phase noise and phase error which defines the phase difference from 90° between I and Q signals. For example, the increase in α degrades the phase noise significantly while the phase error is reduced, or vice versa. The phase noise degradation is induced by the increase in transconductance of the coupling transistors. In addition, the increase in α leads to a higher amount of power dissipation.

Another method to generate quadrature signals has been reported in [17], as shown in Fig. 2 - 6. In Fig. 2 - 6, the back-gate (body terminal) of the PMOS transistor in one pair of the VCO is used as the quadrature phase coupling element to the other pair. Consequently the four quadrature-coupling transistors in the conventional P-QVCO are not needed and their noise contribution to the oscillator vanishes. As mention above, the P-QVCO has trade-off between phase noise and phase error. However, in the back-gate-coupling QVCO, phase error can be reduced without sacrificing phase noise as the coupling involves no additional transistors. From Fig. 2 - 7, the coupling strength α_B through the back-gate can given by

$$\alpha_B = \frac{g_{mb}}{g_m} = \frac{\gamma}{2\sqrt{2\Phi_F - V_{BS}}}$$

where γ, Φ_F, and V_{BS} are the body-effect coefficient, work function, and back-gate (body) to source bias voltage, respectively. It can be seen that the coupling strength α_B is a function of V_{BS}. Therefore, in order to increase α_B, which leads to phase error reduction, the body-to-source reverse bias should be minimized. The usage of back-gates removes the

coupling transistors and therefore additional noise contributions compared to the conventional coupling transistor based topology.

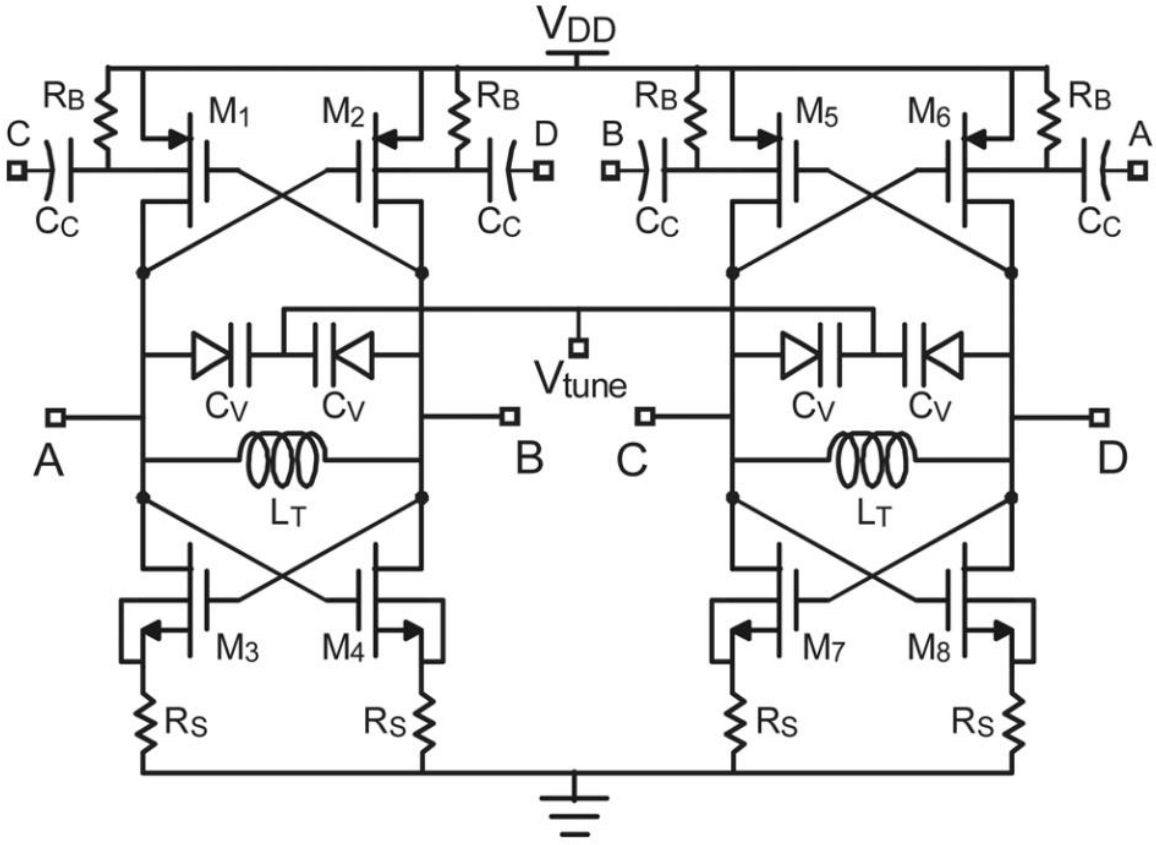

Fig. 2 - 6 Schematic of the conventional back-gate coupling QVCO

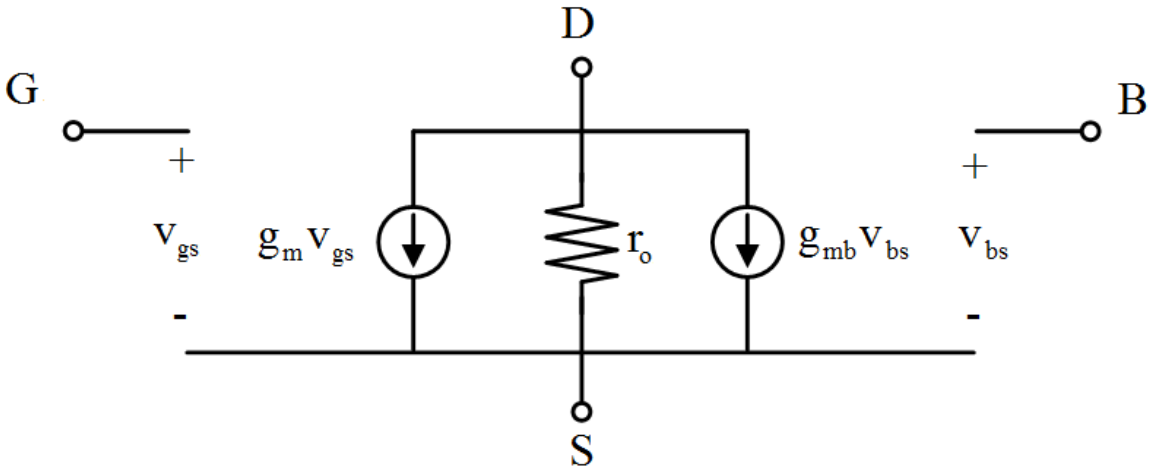

Fig. 2 - 7 Small signal equivalent circuit of the back-gate-coupling transistor

The close-in phase noise spectrum of the circuit shown in Fig. 2 - 6 results from the flicker noise up-conversion of the NMOS and back-gate modulation PMOS transistor, which is expressed as [33]

$$L(\Delta\omega) = 10\log\left[\frac{c_0^2}{q_{\max}^2}\left(\frac{\overline{\frac{i_{n,N}^2}{\Delta f}}}{2\cdot\Delta\omega^2}\cdot\frac{\omega_{1/f,N}}{\Delta\omega}+\frac{\overline{\frac{i_{n,Pb}^2}{\Delta f}}}{2\cdot\Delta\omega^2}\cdot\frac{\omega_{1/f,Pb}}{\Delta\omega}\right)\right]$$

where c_0 is the first Fourier coefficient of the impulse sensitivity function, representation the wave form symmetry of oscillating signal. The term $\overline{\frac{i_{n,N}^2}{\Delta f}}$ denotes the summed noise current spectral density from NMOS transistors with angular flicker-noise corner frequency $\omega_{1/f,N}$, while $\overline{\frac{i_{n,Pb}^2}{\Delta f}}$ denotes the one from back-gate modulated PMOS transistors with the angular corner frequency $\omega_{1/f,Pb}$. The insertion of the resistor R_S at the NMOS source node reduces the transconductance by a factor of $1/(1+g_{m,N}R_s)$, which in turn reduces $\omega_{1/f,N}$ by the same factor due to the proportionality of $\omega_{1/f,N}$ to $g_{m,N}$ for a short-channel MOS transistor [34]. The resistor R_S also linearizes the degenerated transconductance variation over an oscillating swing period. Nevertheless, this method requires an accurate resistor R_S which must be properly designed because large R_S may cease the oscillation start-up, introduce extra thermal noise and introduce an extra amount of power. As mention above, we propose the modified spontaneous transconductance match (M-STM) technique to conquer this problem.

The circuit we proposed in this chapter can achieve lower phase noise, lower amplitude imbalance ratio and lower power dissipation by combining the back-gate coupling principle, current-reused QVCO structure and modified spontaneous transconductance match (M-STM) technique. The circuit design consideration will be discussed in next section.

2.2 Circuit Design Consideration

The schematic of the proposed modified spontaneous transconductance match (M-STM) current reused quadrature VCO (CR-QVCO) is shown in Fig. 2 - 8. The CR-QVCO is mainly composed of two current reused differential VCO cores, which replaces one of the NMOS transistors of a conventional differential LC-VCO with a PMOS transistor[11]. The negative conductances are provided by the cross-connected pairs of transistors M1, M2, and M5, M6, to compensate the losses in the LC-tank. The series stacking of NMOS transistors and PMOS transistors allows the supply current to be reduced by half compared to that of the conventional LC-VCO while providing the same negative conductance.

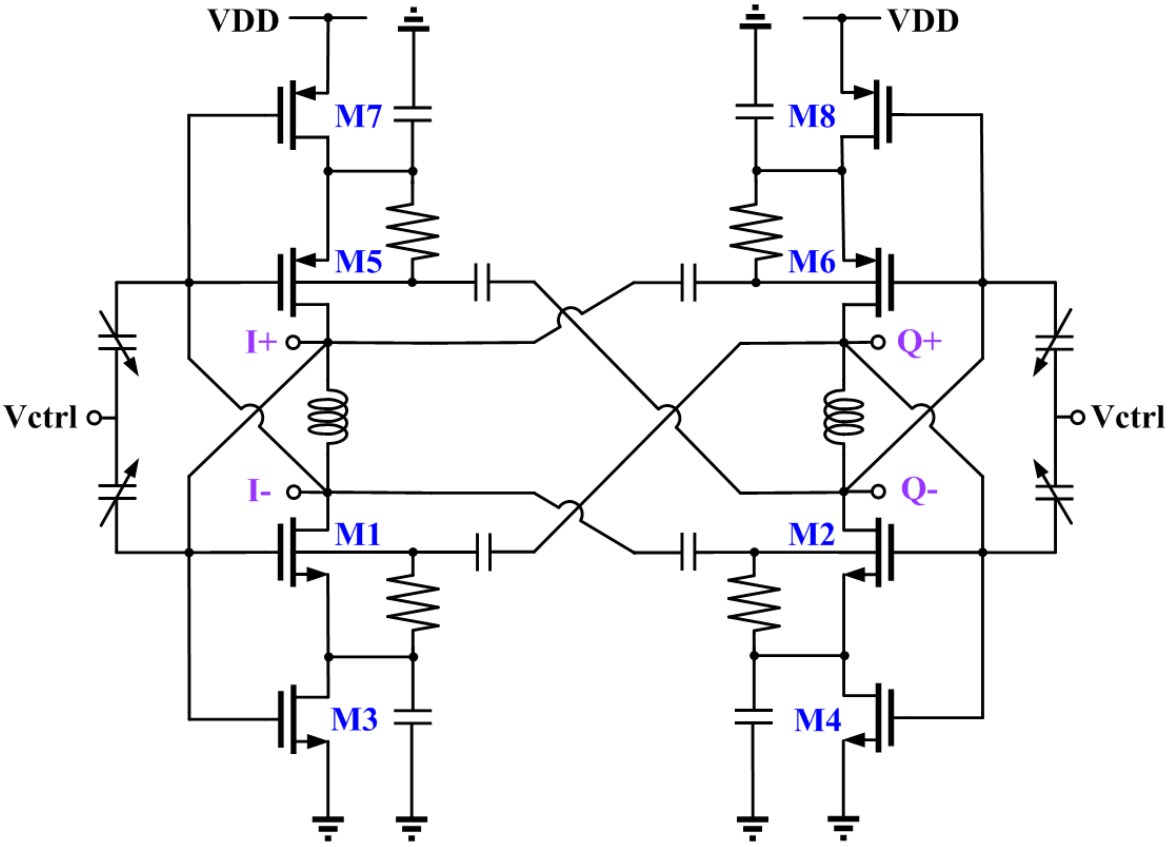

Fig. 2 - 8 Schematic of proposed current reused QVCO with modified STM

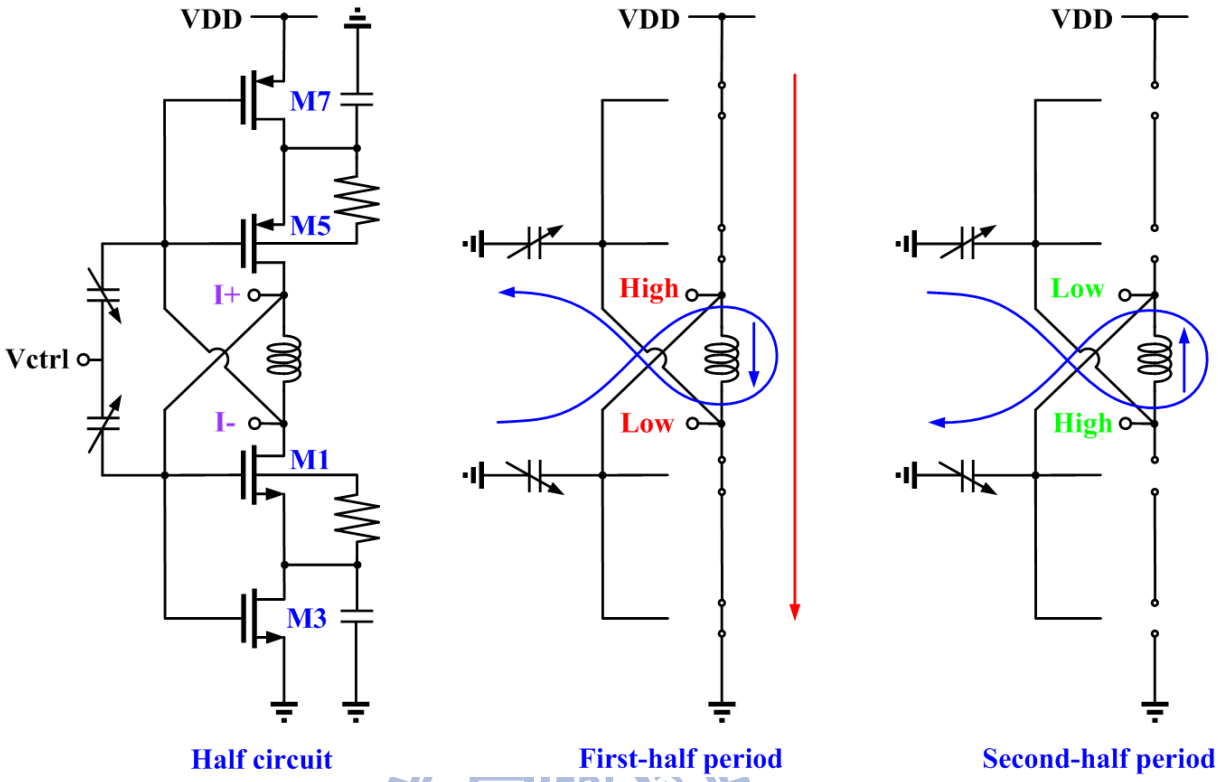

Fig. 2 - 9 Proposed CR-QVCO operation during each half period

To explain the operation of the proposed CR-QVCO, Fig. 2 - 9 shows the schematic and corresponding large-signal equivalent circuits during each half period of operation, that is, when the voltage at node I+ is high and low. As shown in Fig. 2 - 9, during the first half-period, the transistor M1, M3, M5, and M7 are on and the current flows from VDD to ground through the inductor. During the second half-period, the transistor, the transistors are off and the current flows in the opposite direction through the capacitors. Note that in the conventional differential QVCO, the cross-connected transistors switch alternatively, while in the proposed QVCO, the PMOS transistors and NMOS transistors switch at the same time.

Unlike a conventional VCO where the transistors switch alternatively, this QVCO does not have a common-source node because the transistors switch on and off at the same time. Therefore, the proposed QVCO is inherently immune to phase noise degradation caused by second-harmonic terms at the common-source node. In the conventional NMOS-based or

PMOS-based differential QVCO, the phase noise can be degraded significantly by the noise near the second harmonic[15]. Utilization of PMOS transistors in the cross-connected pair can additionally help to reduce the phase noise due to lower flicker noise and hot carrier effects[16].

Fig. 2 - 10 shows the concept of the proposed modified spontaneous match (M-STM) technique. During the first half-period, the transistor M3, M4, M7, and M8 are biased in the triode region as a variable resistor to control the gate-source voltage of M1, M2, M5, and M6,respectively, which in turn determines the transconductances of M1, M2, M5, and M6. By connecting the gate terminals to the another side of the outputs, the equivalent resistance of the variable resistor can be expressed as

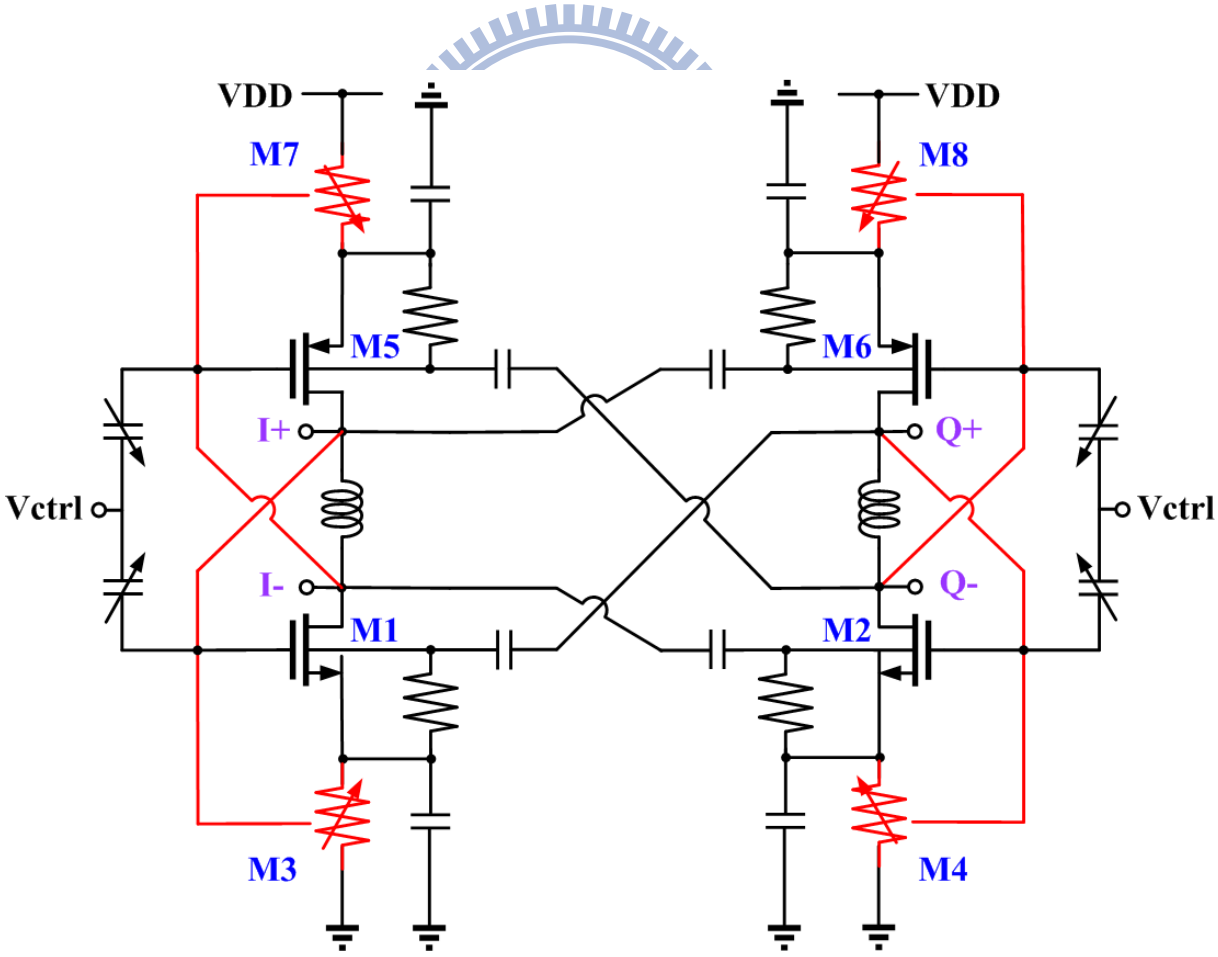

Fig. 2 - 10 Concept of the proposed modified STM technique

$$r_{ds3}=\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3\left(V_{GS3}-V_t\right)}=\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3\left(V_{I+}-V_t\right)}\propto\frac{1}{V_{OV3}}$$

$$r_{ds4}=\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4\left(V_{GS3}-V_t\right)}=\frac{1}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4\left(V_{Q+}-V_t\right)}\propto\frac{1}{V_{OV4}}$$

$$r_{ds7}=\frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_7\left(V_{SG7}-V_t\right)}=\frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_7\left(VDD-V_{I-}-V_t\right)}\propto\frac{1}{V_{OV7}}$$

$$r_{ds8}=\frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8\left(V_{SG7}-V_t\right)}=\frac{1}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8\left(VDD-V_{Q-}-V_t\right)}\propto\frac{1}{V_{OV8}}$$

where $\mu_n C_{ox}$ and $\mu_p C_{ox}$ are the MOS device parameters, W and L are the gate width and length of the transistor. The effective transconductances of M1, M2, M5, and M6 in Fig. 2 - 10 can be expressed, respectively, as

$$g_{m1}=\mu_n C_{ox}\left(\frac{W}{L}\right)_1\left[V_{OV1}-\frac{I_{DL}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_3\left(V_{I+}-V_t\right)}\right]$$

$$g_{m2}=\mu_n C_{ox}\left(\frac{W}{L}\right)_2\left[V_{OV2}-\frac{I_{DR}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_4\left(V_{Q+}-V_t\right)}\right]$$

$$g_{m5}=\mu_p C_{ox}\left(\frac{W}{L}\right)_5\left[VDD-V_{OV5}-\frac{I_{DL}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_7\left(VDD-V_{I-}-V_t\right)}\right]$$

$$g_{m6}=\mu_p C_{ox}\left(\frac{W}{L}\right)_6\left[VDD-V_{OV6}-\frac{I_{DR}}{\mu_p C_{ox}\left(\frac{W}{L}\right)_8\left(VDD-V_{Q-}-V_t\right)}\right]$$

where $\mu_n C_{ox}$ and $\mu_p C_{ox}$ are the MOS device parameters, W and L are the gate width and length of the transistor, V_{ov} is the overdrive voltage, I_{DL} and I_{DR} is the drain current of left-half VCO

and right-half VCO, respectively.

The size of M1 - M8 are selected to satisfy the symmetric oscillation waveform condition $g_{m1}Z_{I-} = g_{m5}Z_{I+}$ and $g_{m2}Z_{Q-} = g_{m6}Z_{Q+}$ where Z_{I-}, Z_{I+}, Z_{Q-}, and Z_{Q+} denote the impedance at node I-, I+, Q-, and Q+, respectively. When the output amplitude at node I- and I+ are different, the feedback mechanism will change the gate voltage of M1 and M5 in an opposite amount. Therefore, the g_{m1} and g_{m5} are complementary changed by feedback mechanism to equalize the output amplitudes. By the same token, the g_{m2} and g_{m6} are also complementary changed by feedback mechanism to equalize the output amplitudes. The comparison of amplitude ratio V3 / V1 with modified STM technique and without modified STM technique is shown in Fig. 2 - 11. Over the entire frequency tuning range, the amplitude imbalance ratio of output signals with modified STM technique is less than 0.2%, while the amplitude imbalance ratio of output signals without modified STM technique is as high as 1.7%.

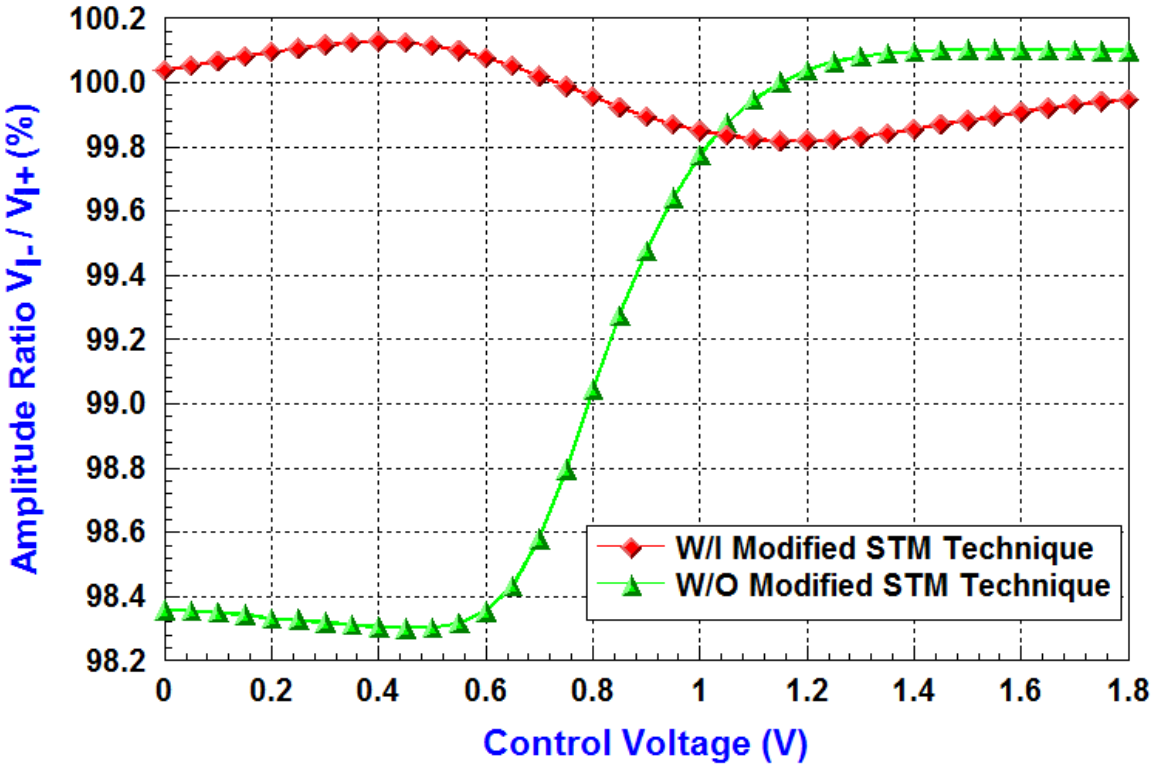

Fig. 2 - 11 Simulated output amplitude imbalance ratio of the proposed modified STM-QVCO

The mechanism of the proposed modified spontaneous transconductance match (M-STM) technique can be divided into five state, as shown from Fig. 2 - 12 to Fig. 2 - 16 :

I. Ideal Case - Equal Output Level : $V_{I+(avg)} = V_{I-(avg)} = V_{Ideal}$

As shown in Fig. 2 - 12, when the g_{mn} and g_{mp} has been properly designed, two outputs of the CR-QVCO will exhibit perfectly equal output level, i.e., $V_{I+(avg)} = V_{I-(avg)}$. We give this ideal value a name V_{Ideal} and will be used later.

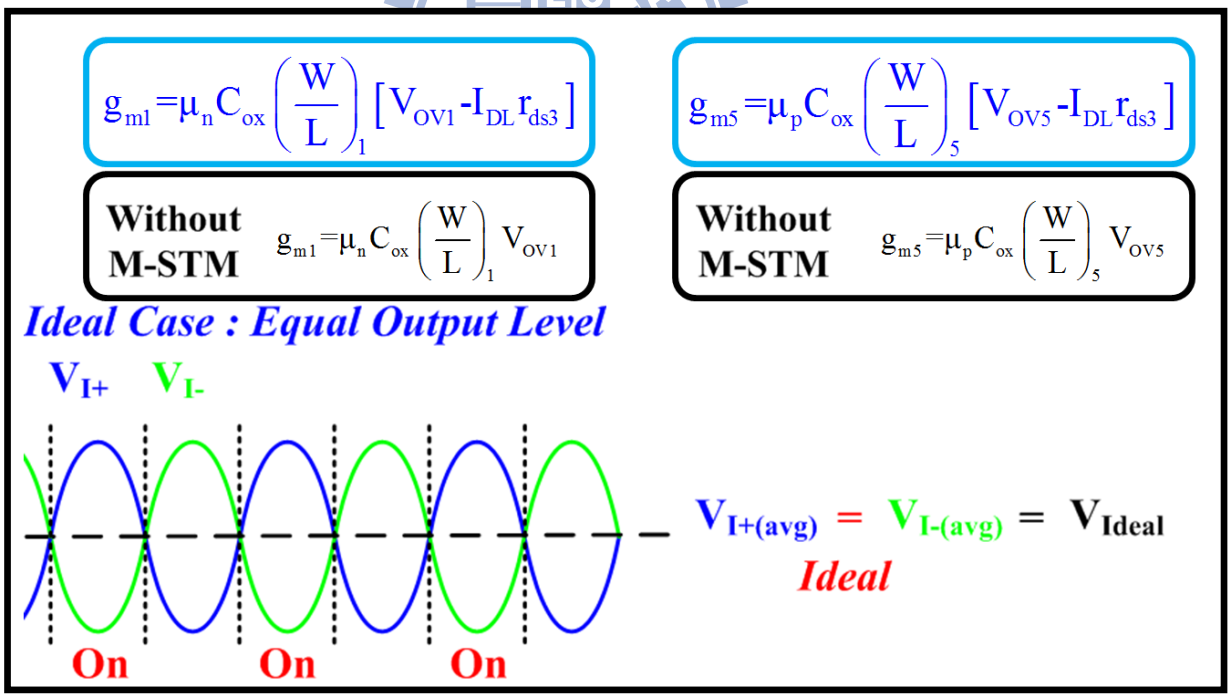

Fig. 2 - 12 The M-STM mechanism to the ideal case of the proposed CR-QVCO

II. Type 1 - Case 1 : $V_{I+(avg)} > V_{I-(avg)} = V_{Ideal}$

As shown in Fig. 2 - 13, when the NMOS process transconductance coefficient "k_n" has slightly become smaller due to process variation :

1. $V_{I+(avg)}$ will become larger than ideal value correspondingly.
2. The larger $V_{I+(avg)}$ will lead to smaller r_{ds3}, and , in turn, increase $V_{I+(avg)}$ toward the ideal value, which is the dashed line in the zoom in window.

Consequently, $V_{I+(avg)}$ will have less variation thanks to the M-STM feedback compensation.

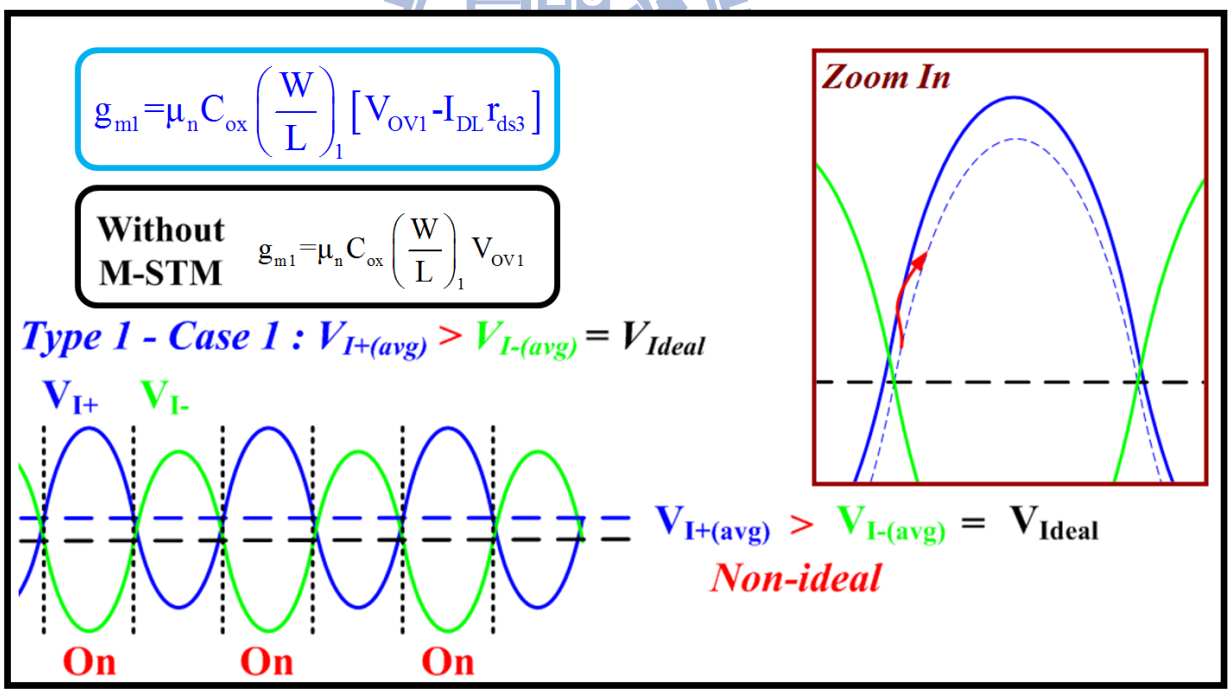

Fig. 2 - 13 The M-STM mechanism to "Type 1 - Case 1" of the proposed CR-QVCO

III. Type 1 - Case 2 : $V_{I+(avg)} < V_{I-(avg)} = V_{Ideal}$

As shown in Fig. 2 - 14, when the NMOS process transconductance coefficient "k_n" has slightly become larger due to process variation :

1. $V_{I+(avg)}$ will become smaller than ideal value correspondingly.
2. The smaller $V_{I+(avg)}$ will lead to larger r_{ds3}, and , in turn, increase $V_{I+(avg)}$ toward the ideal value.

Consequently, $V_{I+(avg)}$ will have less variation thanks to the M-STM feedback compensation.

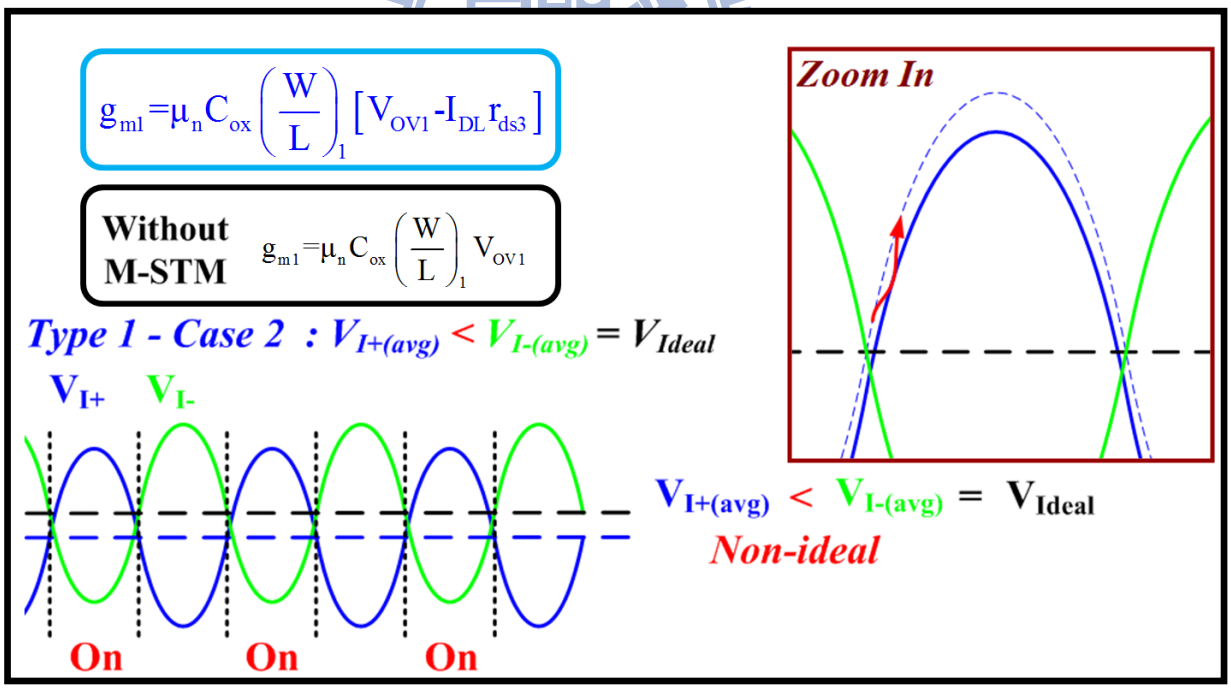

Fig. 2 - 14 The M-STM mechanism to "Type 1 - Case 2" of the proposed CR-QVCO

IV. Type 2 - Case 1 : $V_{I-(avg)} > V_{I+(avg)} = V_{Ideal}$

As shown in Fig. 2 - 15, when the PMOS process transconductance coefficient "k_p" has slightly become smaller due to process variation :

1. VI-(avg) will become smaller (but larger negative-half amplitude) than ideal value correspondingly.
2. The smaller $V_{I-(avg)}$ will lead to smaller r_{ds7}, and , in turn, increase $V_{I-(avg)}$ toward the ideal value.

Consequently, $V_{I-(avg)}$ will have less variation thanks to the M-STM feedback compensation.

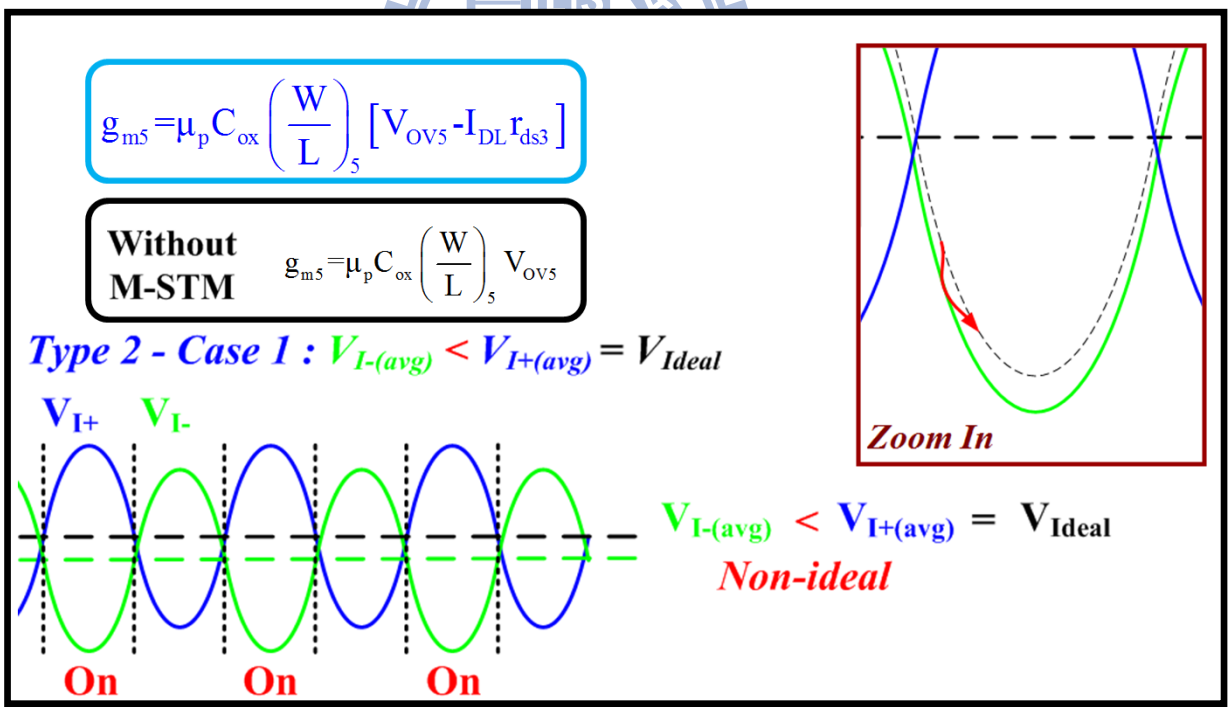

Fig. 2 - 15 The M-STM mechanism to "Type 2 - Case 1" of the proposed CR-QVCO

V. Type 2 - Case 2 : $V_{I-(avg)} < V_{I+(avg)} = V_{Ideal}$

As shown in Fig. 2 - 16, when the PMOS process transconductance coefficient "k_p" has slightly become larger due to process variation :

1. $V_{I-(avg)}$ will become larger (but smaller negative-half amplitude) than ideal value correspondingly.
2. The larger $V_{I-(avg)}$ will lead to larger r_{ds7}, and , in turn, decrease $V_{I-(avg)}$ toward the ideal value.

Consequently, $V_{I-(avg)}$ will have less variation thanks to the M-STM feedback compensation.

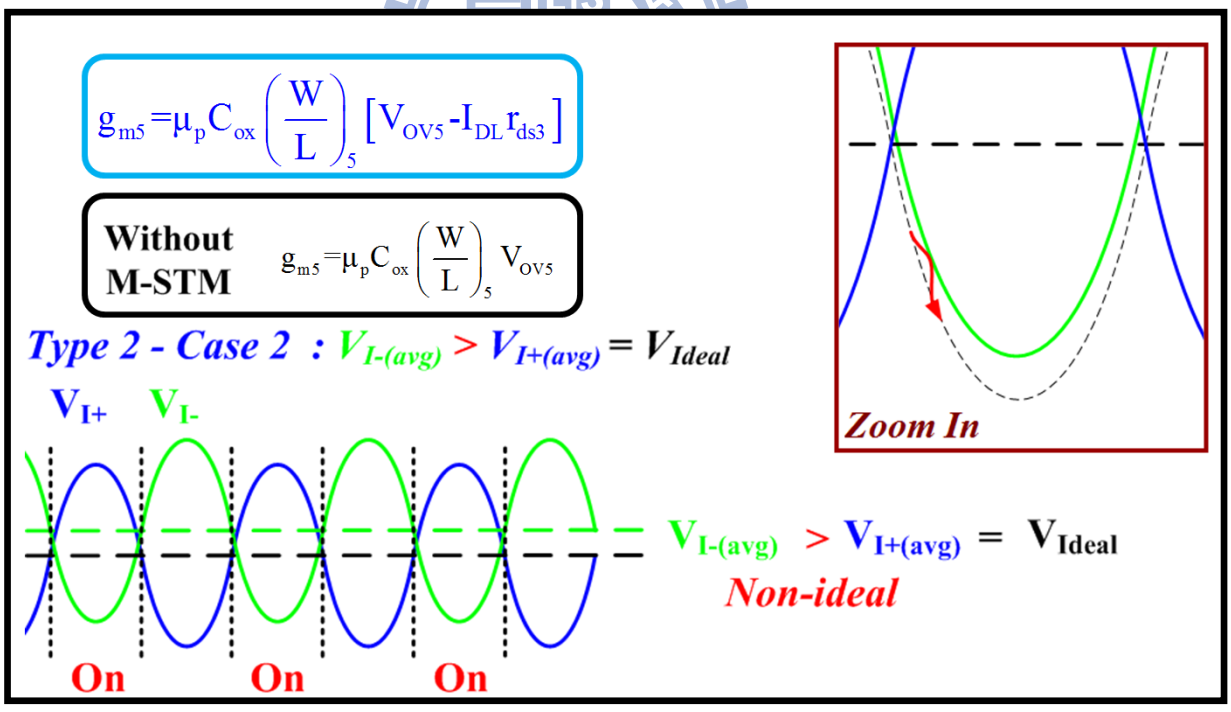

Fig. 2 - 16 The M-STM mechanism to "Type 2 - Case 2" of the proposed CR-QVCO

2.3 Chip Layout and Simulation Results

The circuit was simulated and optimized using Agilent ADS. The design procedure can be divided in two steps. First, a small signal analysis was used to optimize the feedback and the resonator elements to find the oscillation condition at the target frequency. This condition was simulated breaking the feedback path. In the second step, a large signal analysis was performed with the harmonic balance simulator to predict the exact oscillation frequency and output power of the fundamental signal as well as the harmonic signals.

Fig. 2 - 17 shows the chip layout photograph of the proposed modified STM current reused QVCO, which is designed and implemented in TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The chip size is 1.100 × 0.841 mm^2 including all pads and bypass capacitances. Each buffer of the QVCO outputs were designed as a common-source amplifier.

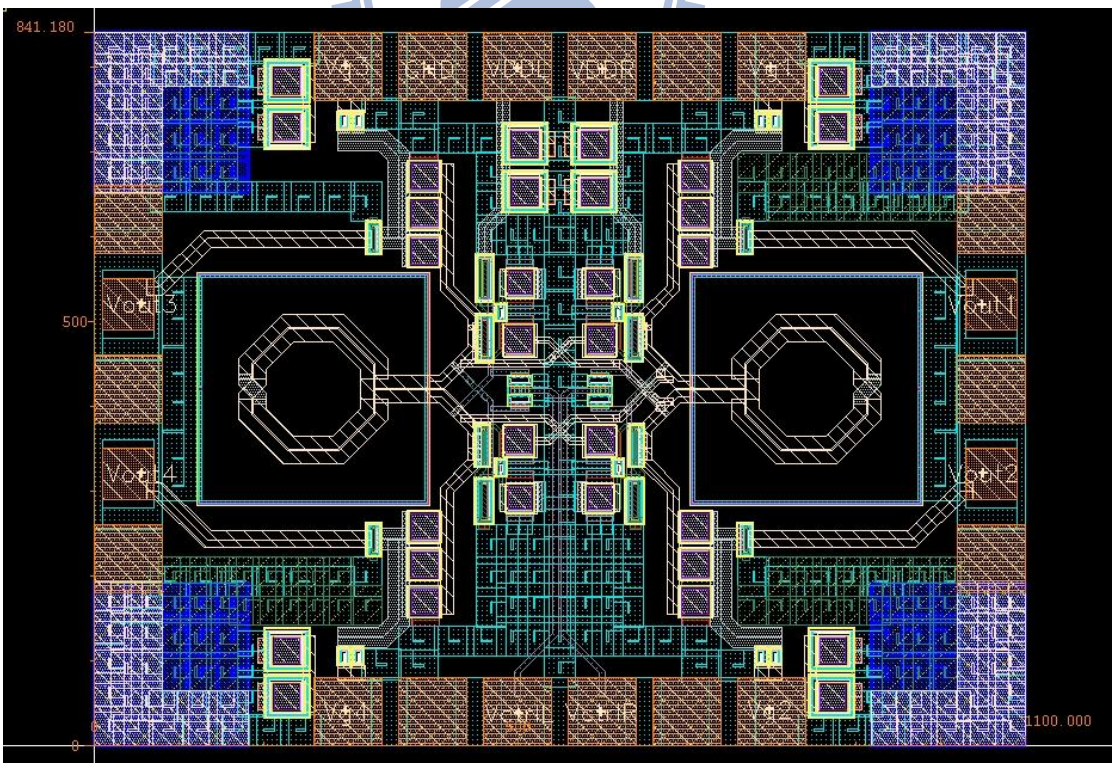

Fig. 2 - 17 Chip layout of the proposed modified STM-QVCO

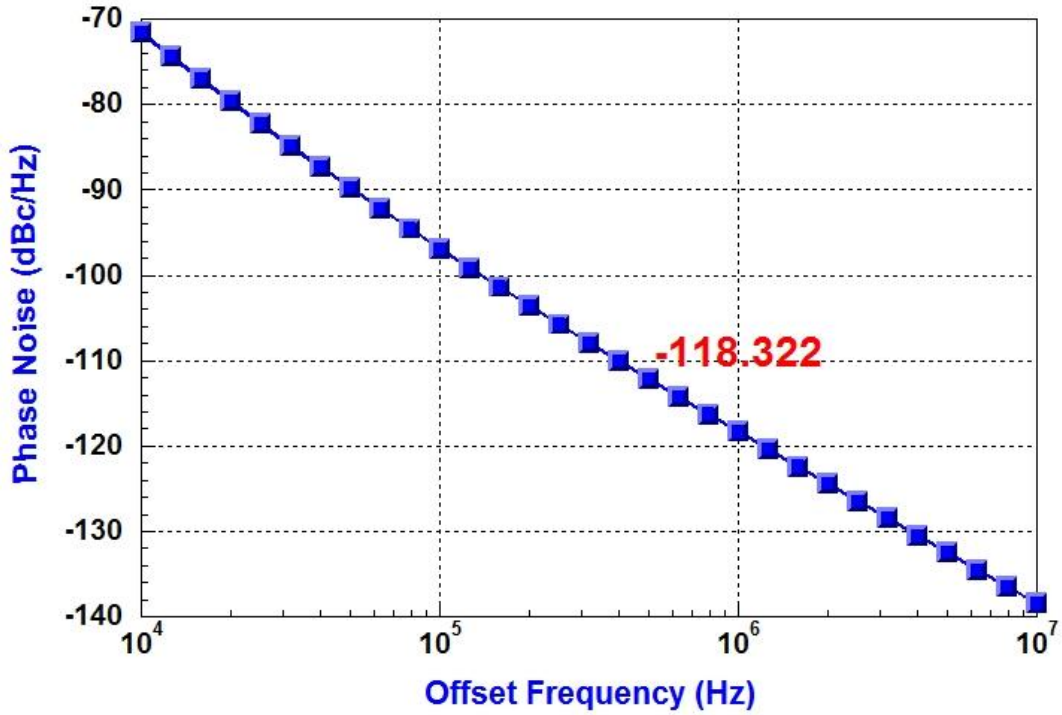

Fig. 2 - 18 Simulated phase noise of the proposed modified STM-QVCO

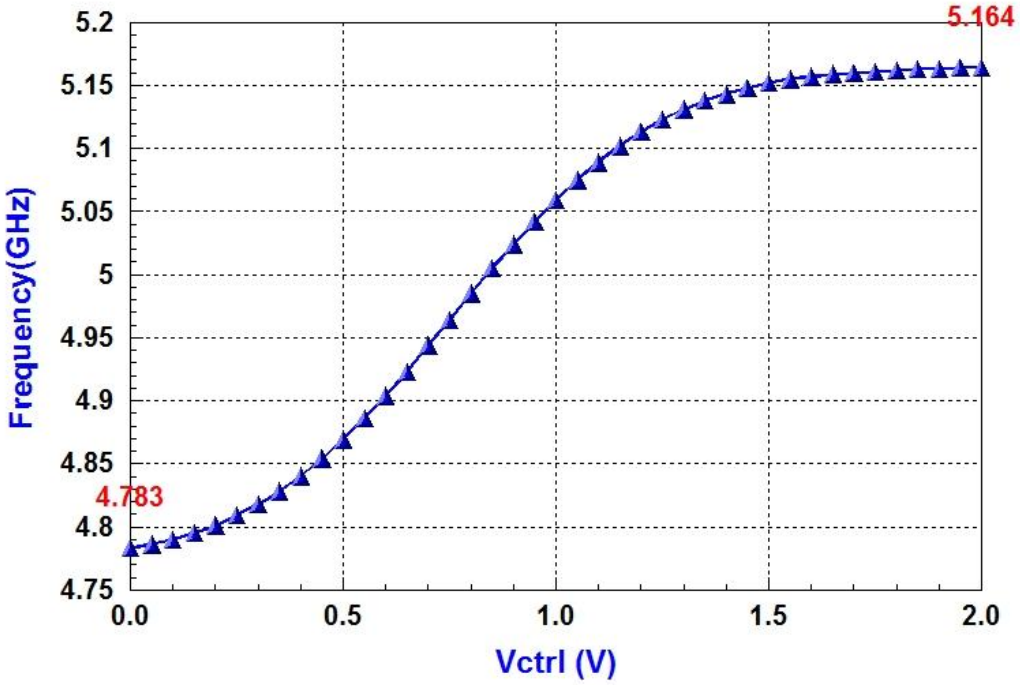

Fig. 2 - 19 Simulated tuning range of the proposed modified STM-QVCO

The simulated phase noise and tuning range of the proposed modified STM QVCO are shown in Fig. 2 - 18 and Fig. 2 - 19,respectively. Table 2 - 1 summarizes the simulated results of the proposed modified STM QVCO in each corner. The figure of merits (FOM) for oscillators summarizes the important performance parameters, i.e., phase noise and power consumption P, to make a fair comparison is defined in [40] as

$$FOM = L(\Delta\omega) + 20\log\left(\frac{\Delta\omega}{\omega_O}\right) + 10\log\left(\frac{P}{1mW}\right)$$

where the second term is to neutralize the effect of offset in L(Δω) while taking the center frequency into account. The power consumption is calculated as dBm such that the unit of FOM remains the same as that of L(Δω).

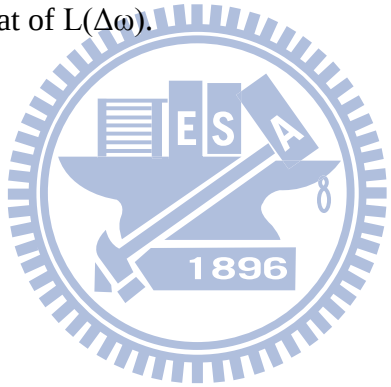

Table 2 - 1 Simulated results of the proposed modified STM-QVCO

Corner	SS	TT	FF	SF	FS
Tuning Range	4.78-5.12	4.82-5.13	4.91-5.22	4.84-5.16	4.86-5.16
Phase Noise	-118.645	-118.322	-118.102	-118.571	-118.313
Supply Voltage	1.5	1.35	1.2	1.35	1.35
ID	3.6	3.41	3.53	3.49	3.38
Core Power	4.68	4.60	4.24	4.71	4.56
FOM	-185.53	-185.35	-185.64	-185.53	-184.90

2.4 Measurement Results and Discussion

2.4.1 Measurement Consideration

The proposed QVCO are designed for on-wafer testing, and the DC voltage are supplied by two sets of six-pin probe, so that the distance between each DC pad must more than 50μm to satisfy the probe testing rules. The output buffer of each quadrature output is designed using common-source amplifier, and the drain end of each buffer is connected to the RF pad. For measurement, we connect four bias-tee terminals to the corresponding RF pads as shown in Fig. 2 - 20.

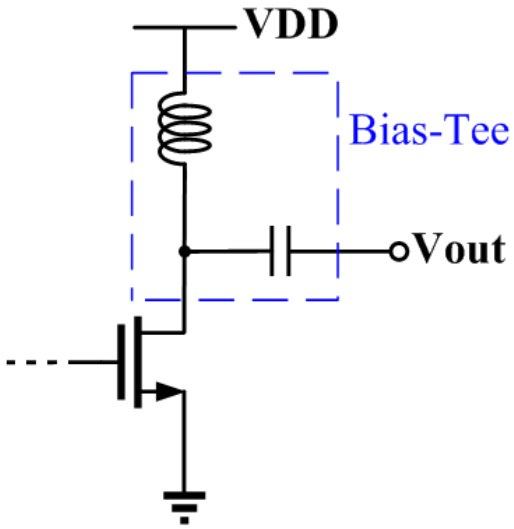

Fig. 2 - 20 Bias-Tee Model

The phase noise, tuning range, output spectrum and output waveform are measured using signal source analyzer (Agilent E5052B) and digital signal analyzer (Agilent DSA91204A) shown in Fig. 2 - 21and Fig. 2 - 22, respectively.

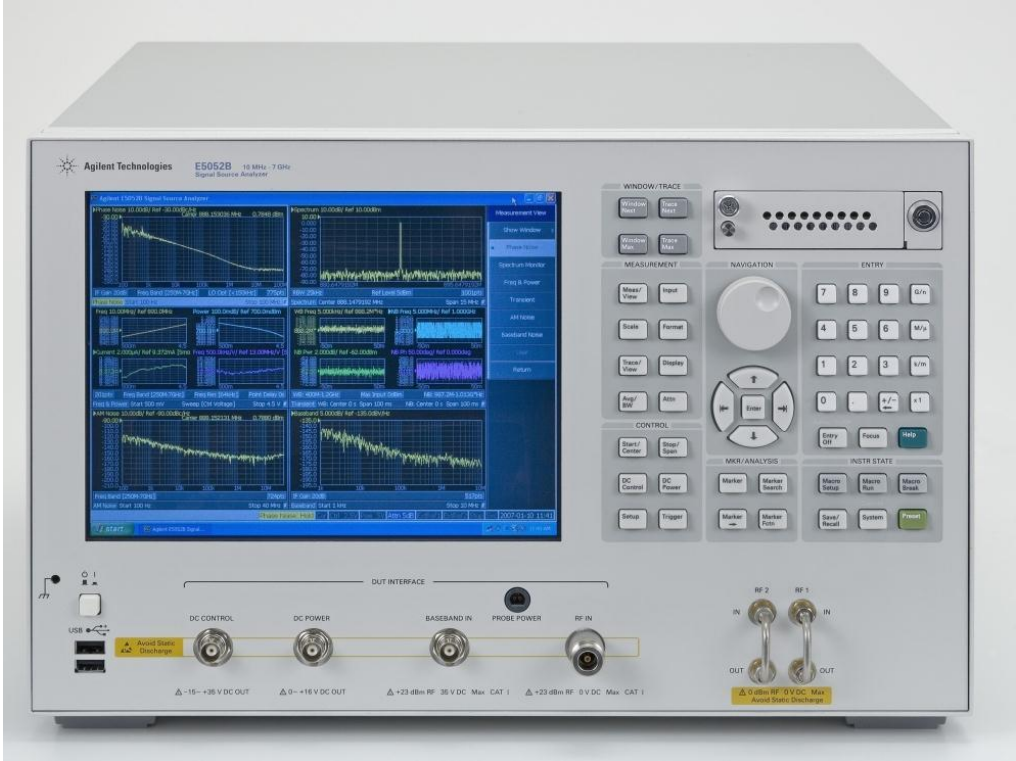

Fig. 2 - 21 Signal Source Analyzer (Agilent E5052B)

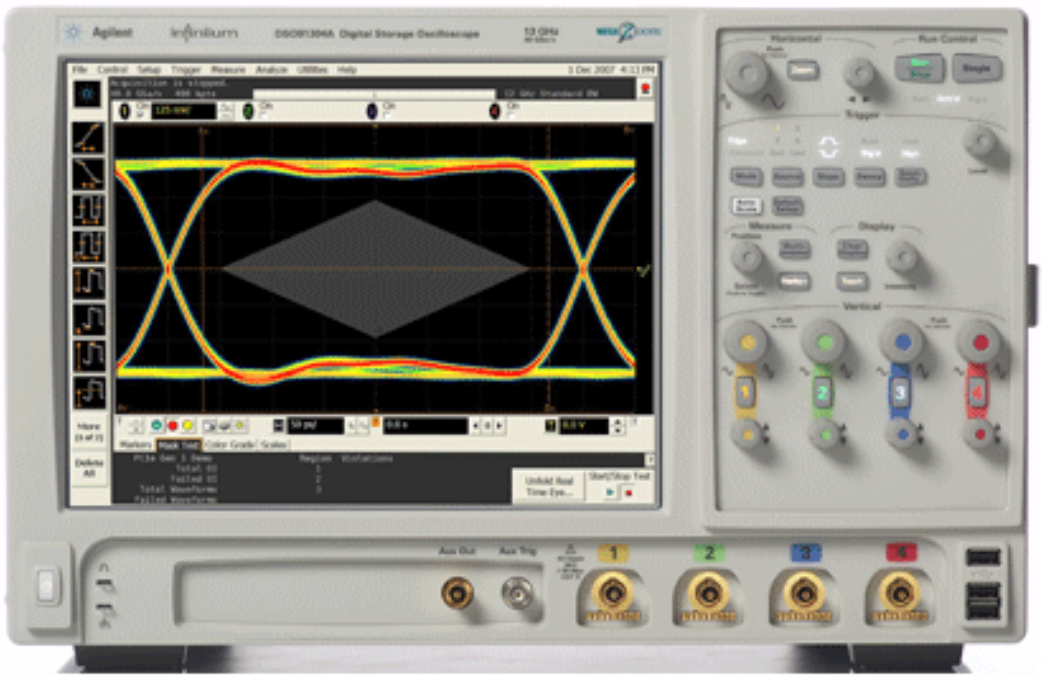

Fig. 2 - 22 Digital Signal Analyzer (Agilent DSA91204A)

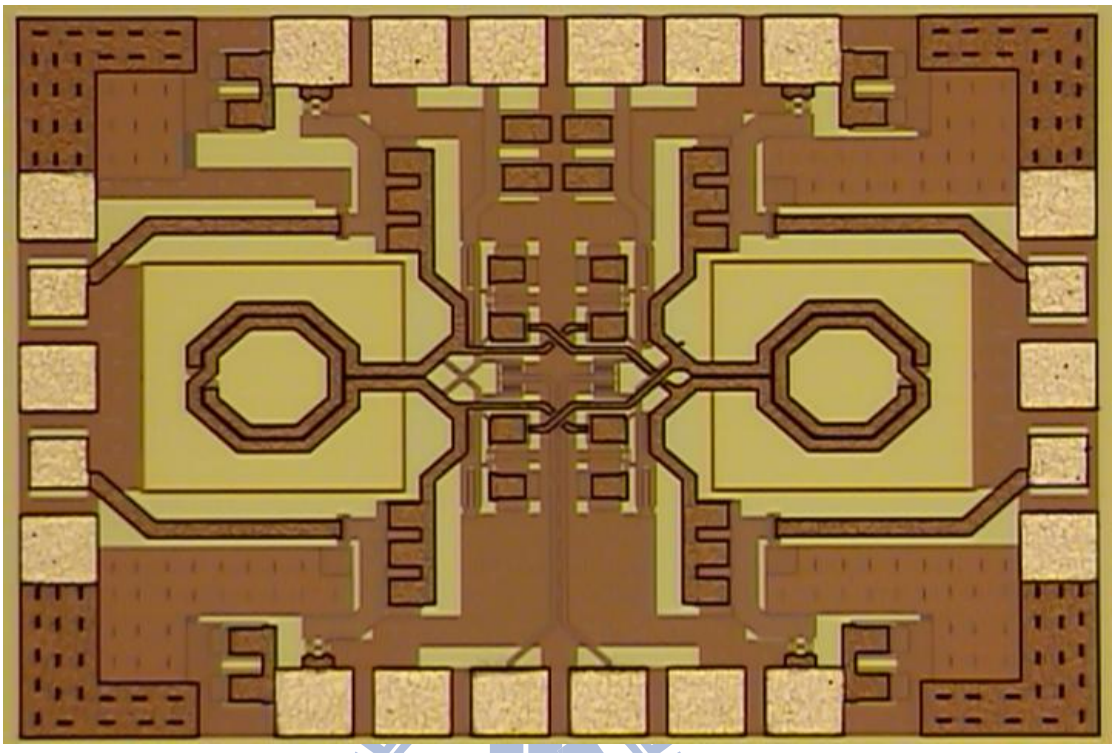

Fig. 2 - 23 Chip photo of the proposed modified STM-QVCO

The Chip photo of the proposed modified STM-QVCO is shown in Fig. 2 - 23. Fig. 2 - 24 and Fig. 2 - 25 shows the arrangement of DC and RF probes. The measured phase noise at 4.84GHz, output spectrum, tuning range, output waveform, and amplitude imbalance ratio was shown in Fig. 2 - 26 to Fig. 2 - 30, respectively. Table 2 - 2 summarizes the measured performance of the proposed modified STM-QVCO.

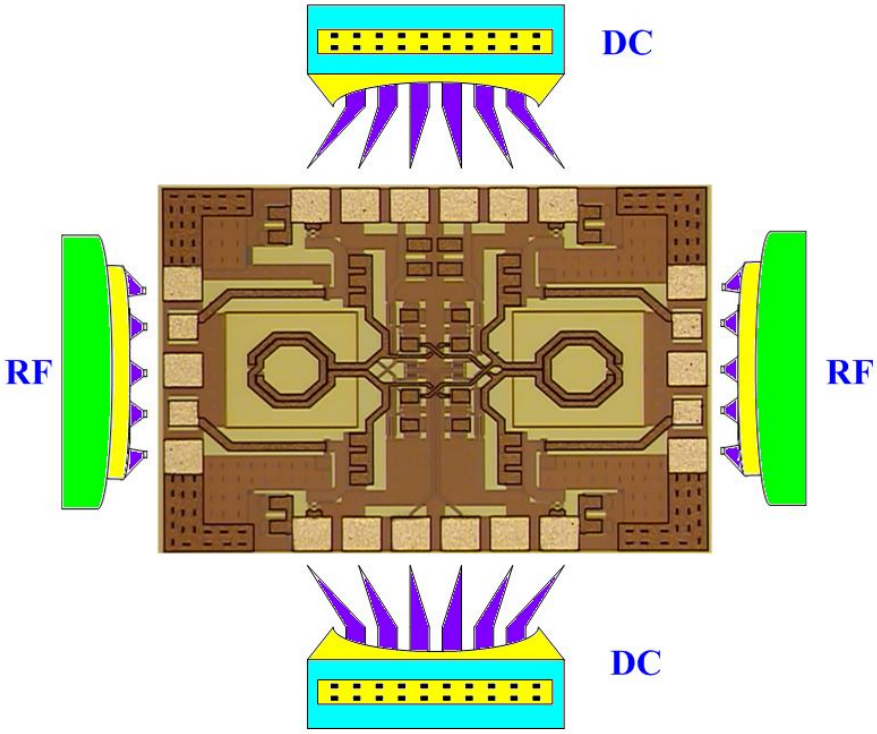

Fig. 2 - 24 Arrangement of DC and RF probes

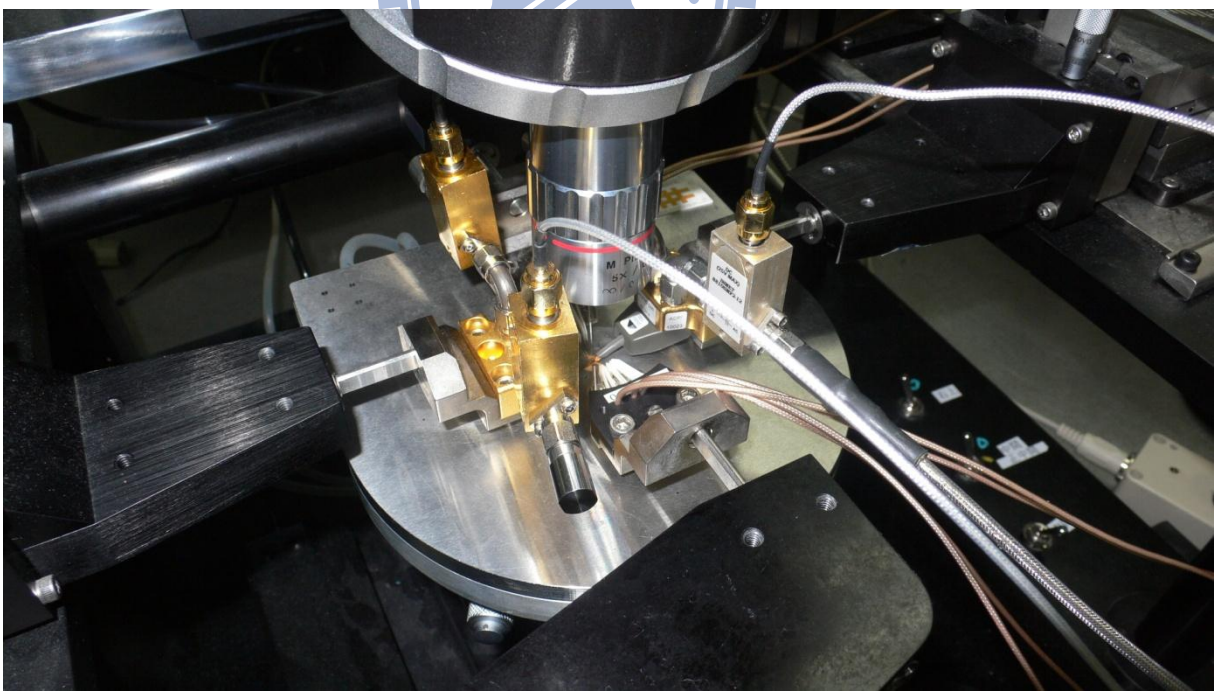

Fig. 2 - 25 Photograph of the probe station

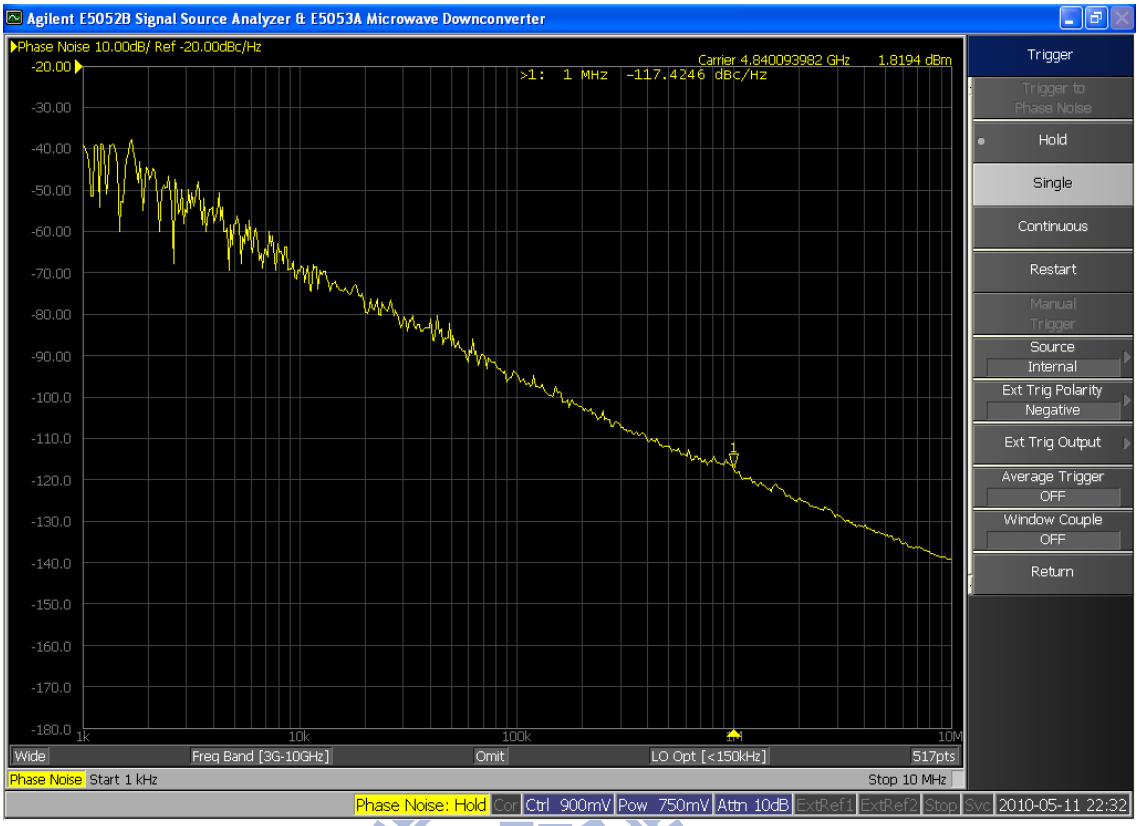

Fig. 2 - 26 Measured phase noise of the proposed modified STM-QVCO

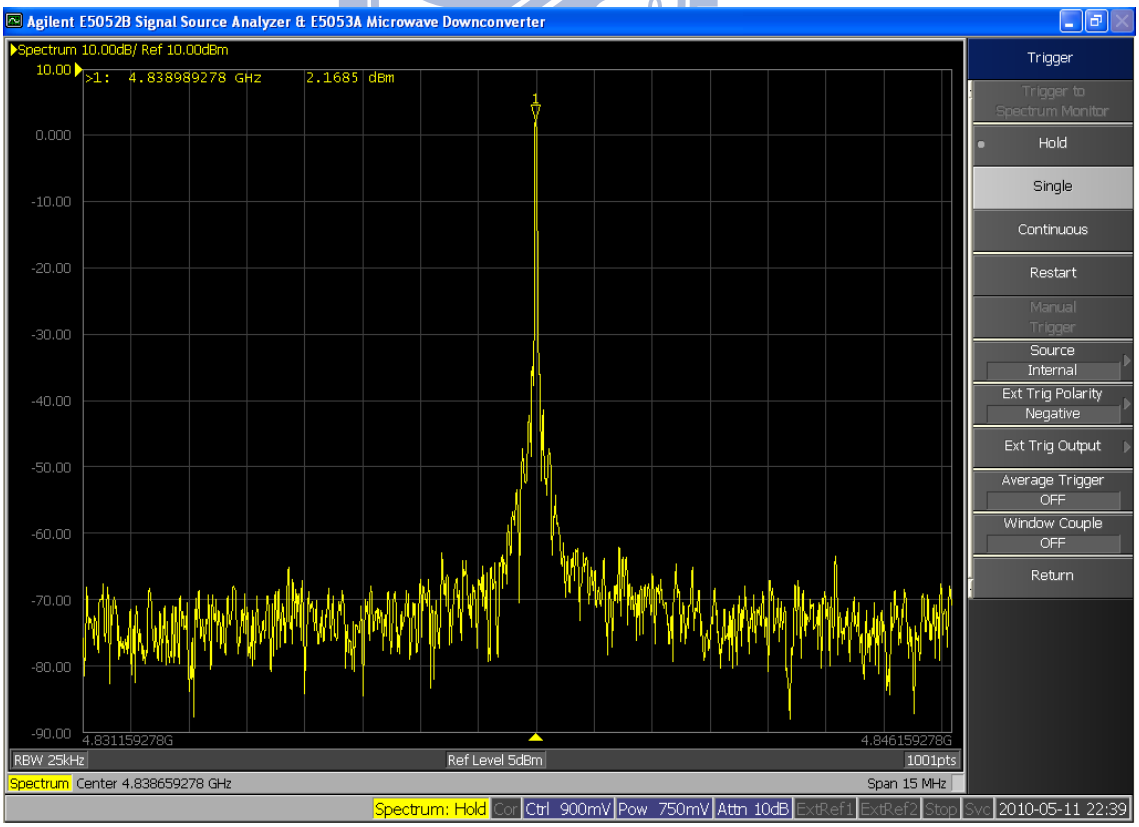

Fig. 2 - 27 Measured output spectrum of the proposed modified STM-QVCO

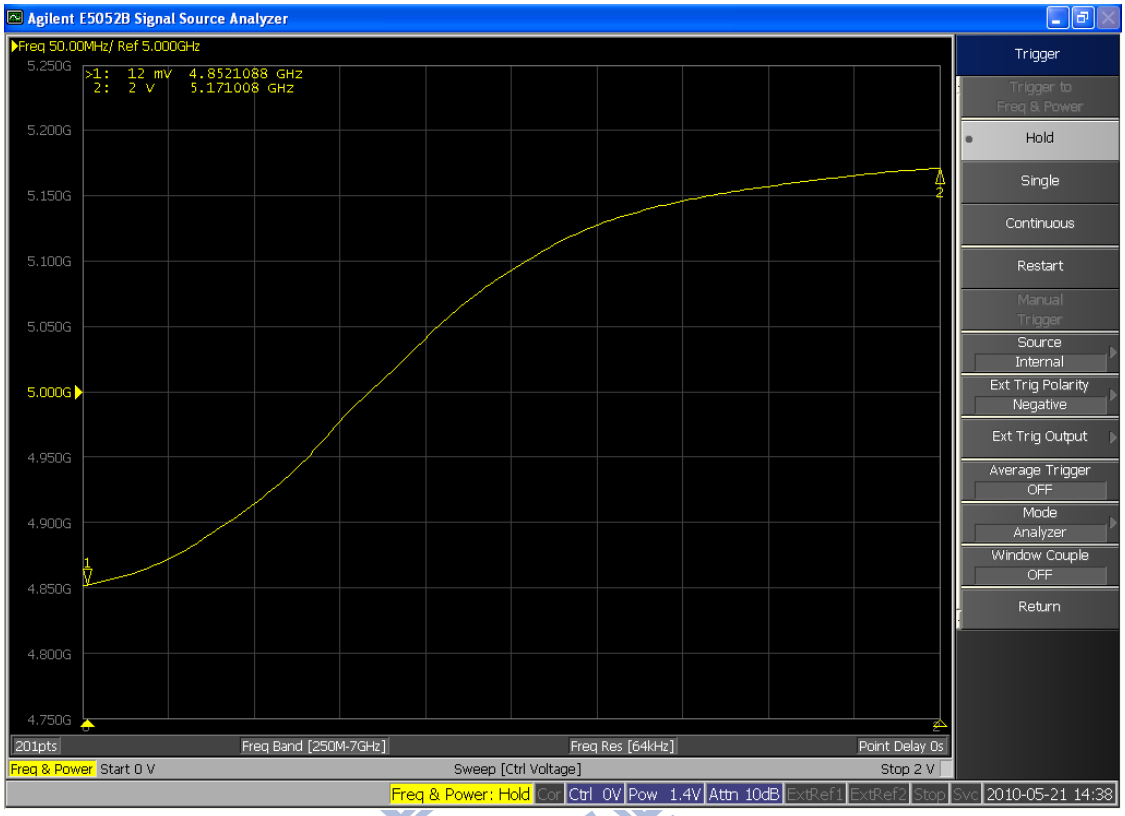

Fig. 2 - 28 Measured tuning range of the proposed modified STM-QVCO

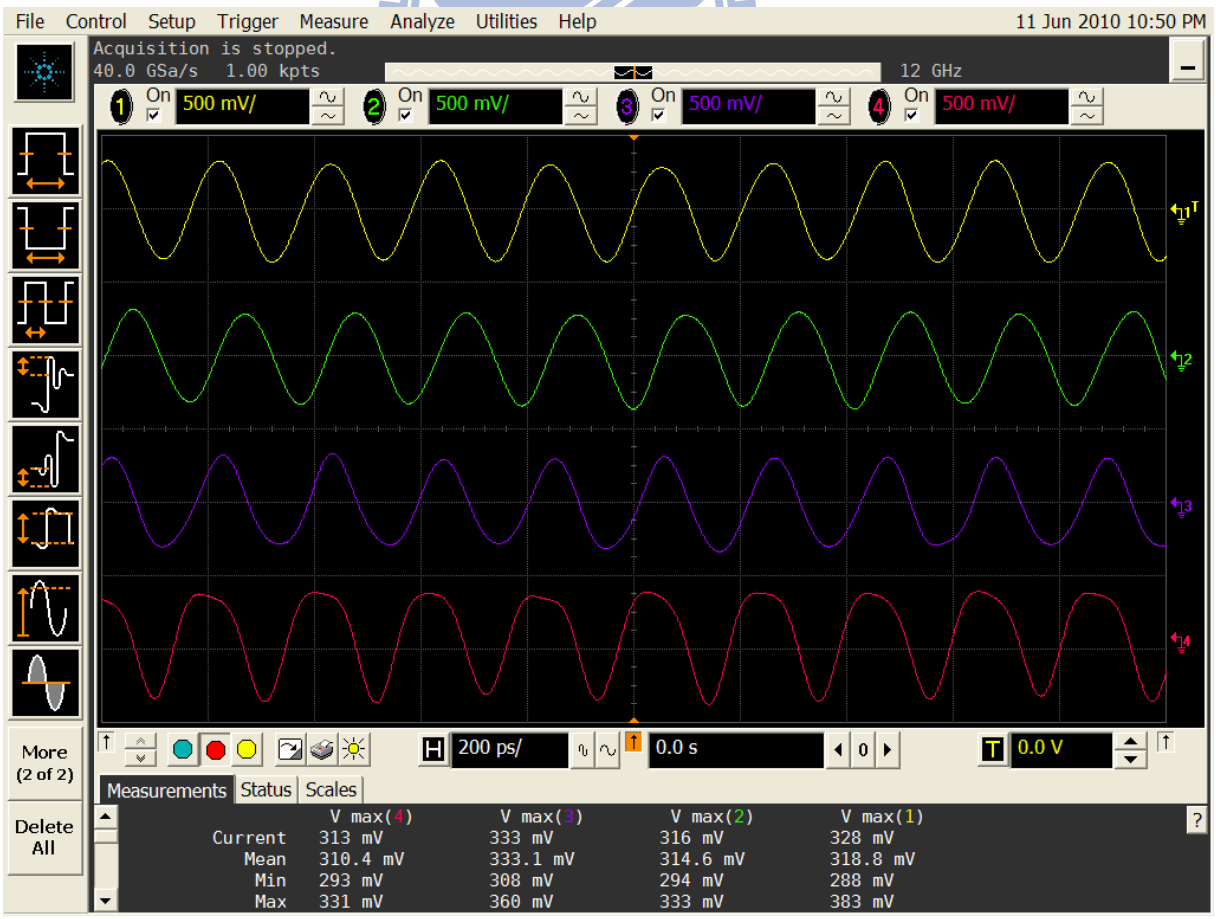

Fig. 2 - 29 Measured output waveform of the proposed modified STM-QVCO

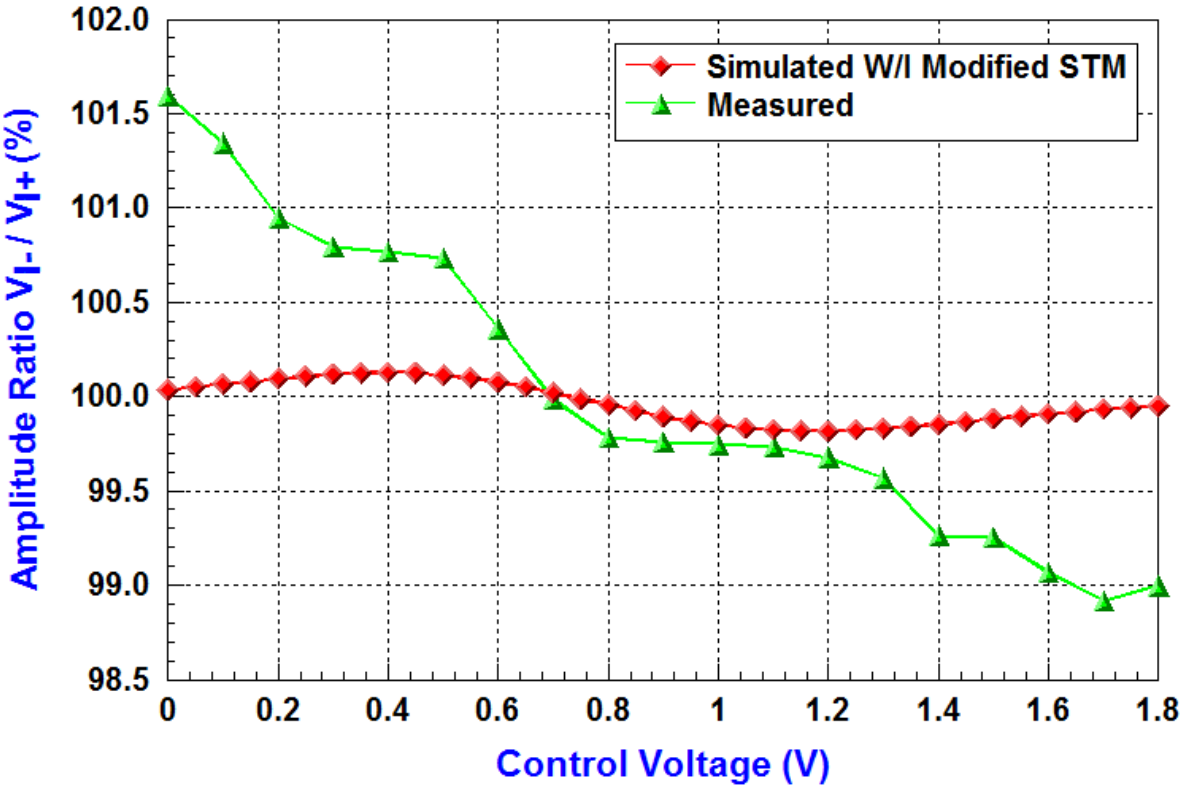

Fig. 2 - 30 Measured output amplitude imbalance ratio of the proposed modified STM-QVCO

Table 2 - 2 Comparison of QVCO Performance

	Technology	Tuning Range	Phase Noise	Supply Voltage	Core Power	FOM
This work (Chapter 2)	0.18μm CMOS	4.84-5.17 GHz	-117.4 dBc/Hz@ 1MHz	1.3V	5.04mW	-184.07
This work (Chapter 3)	0.18μm CMOS	4.83-5.30 GHz	-125.8 dBc/Hz@ 1MHz	1.3V	3.64mW	-193.87
[7] MWCL, 2009	0.18μm CMOS	4.39-5.26 GHz	-113.65 dBc/Hz@ 1MHz	1.8V	6.3mW	-180.0
[8] MWCL, 2005	0.18μm CMOS	5.50-6.10 GHz	-115 dBc/Hz@ 1MHz	1.8V	1.84mW	-182.2
[42] MWCL, 2009	0.18μm CMOS	2.05-2.47 GHz	-117 dBc/Hz@ 1MHz	1.8V	2.84mW	-184
[43] MWCL, 2009	0.18μm CMOS	4.38-4.71 GHz	-120.8 dBc/Hz@ 1MHz	1.1V	2.55mW	-189.61
[9] MWCL, 2007	0.18μm CMOS	1.83-2.02 GHz	-124 dBc/Hz@ 1MHz	1.25V	2.2mW	-186.7
[17] MWCL, 2009	0.18μm CMOS	3.01-3.49 GHz	-133 dBc/Hz@ 1MHz	1.5V	8.1mW	-193.5

Chapter 3

Current-Reused Low Phase Noise Quadrature VCO with Self-Switching Bias

3.1 Introduction

Quadrature signals finds application in many communication systems. For high speed clock and data recovery systems, quadrature signals are required for frequency detection, half-rate phase noise detection, and phase interpolation [19] - [21]. For RF front-ends, quadrature signals are necessary in the implementation of image rejection and direct conversion transceivers, where they are used for modulation or demodulation requirements.

As we mentioned in chapter 2, there are several methods to generate quadrature signal. In fact, a widely-used approach for generation the quadrature signals at high operation frequencies is to cross couple two identical LC oscillator so as to take advantage of the superior performance achievable with LC resonators. In this case two oscillators can be connected in such a way that a signal from one oscillator is injected into the second oscillator and a signal from the second oscillator is injected into the first. The result is that the two oscillators become locked in frequency with quadrature outputs. LC-VCOs have good phase noise performance due to their inherent frequency selectivity that can suppress side-band noise.

Fig. 3 - 1 shows the well-known implementation of Quadrature negative G_m Oscillator with parallel cross connections, in which two LC-VCOs are cross-coupled using addition

coupling transistor (M_5-M_8) in parallel with the core negative-resistance transistor (M_1-M_4). This technique, however, suffers from the trade-off between phase noise and accuracy. The coupling transistors connected in parallel further degrades the phase noise and the power consumption significantly. To improve the performance, the coupling transistor (M_5-M_8) can be connected in series with the negative-resistance transistors (M_1-M_4), such that the phase noise contribution from the coupling device can be reduced as a result of degeneration in cascode configuration. The trade-off between phase noise and phase accuracy can be relaxed.

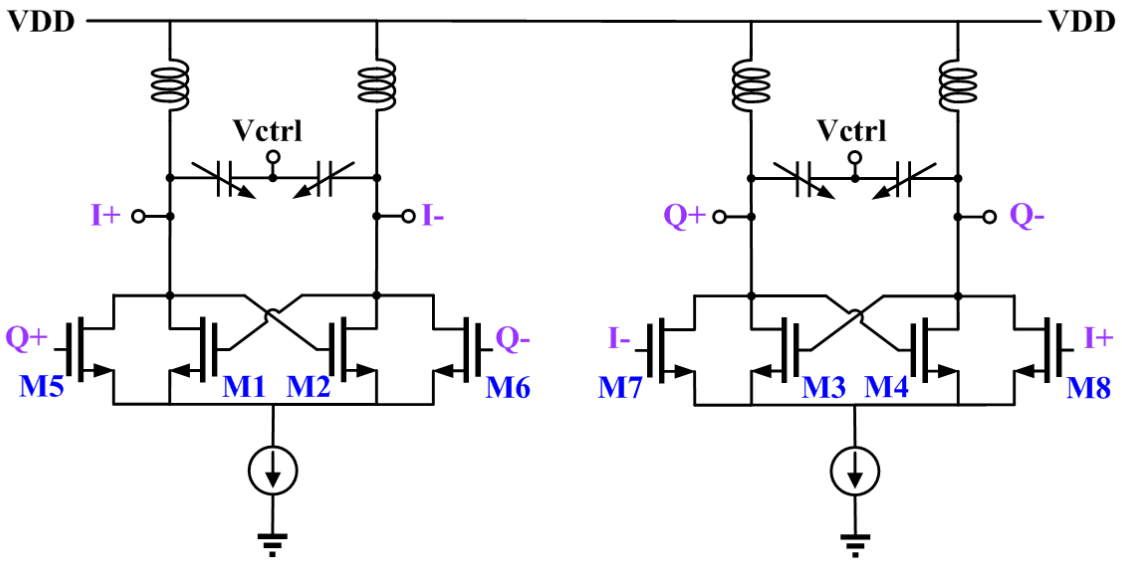

Fig. 3 - 1 Schematic of the conventional parallel-coupled QVCO (P-QVCO)

As shown in Fig. 3 - 2, one of the methods of series coupling is referred as the Top-Series (TS) QVCO [22], [23]. Since the coupling transistor does not require an additional biasing current, power consumption is reduced in this topology. The phase error is almost independent of coupling strength α_B . In fact, phase error of the TS-QVCO acts like a design constant dependent on the actual amount of mismatch between ideally identical components. When both TS-QVCO and P-QVCO are designed to have the same coupling strength, center frequency, and power consumption, it follows that the former has lower phase noise response.

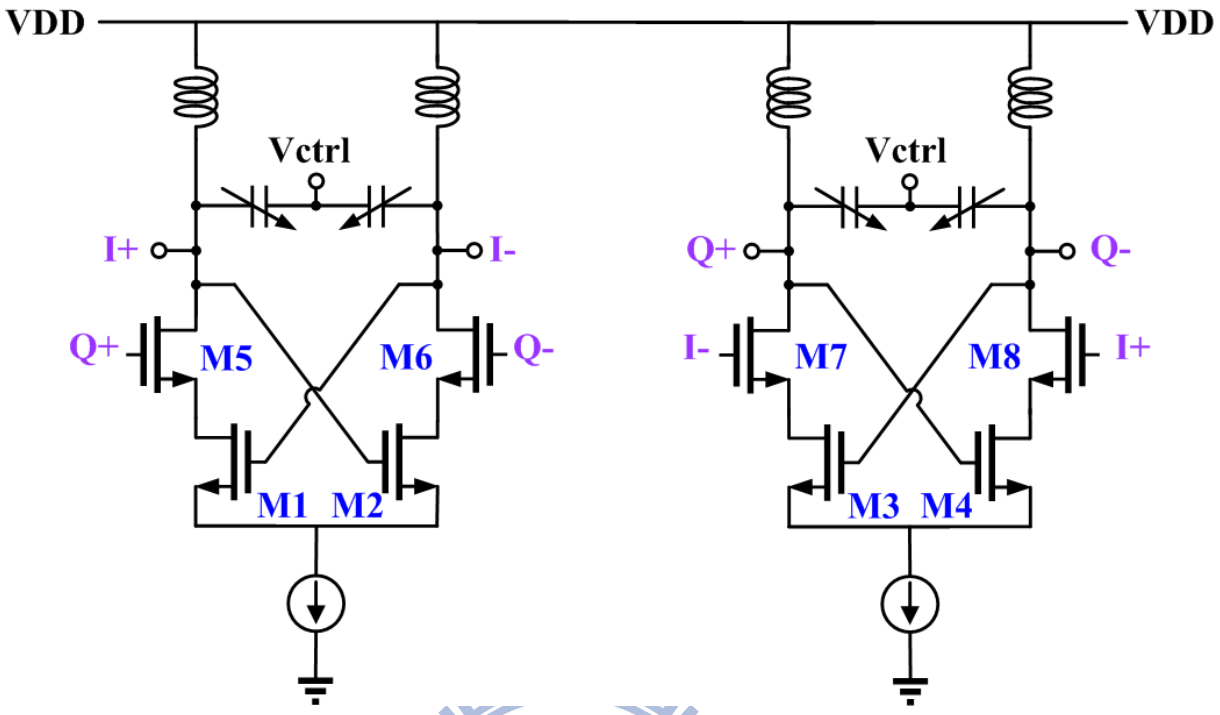

Fig. 3 - 2 Schematic of the conventional top series-coupled QVCO (TS-QVCO)

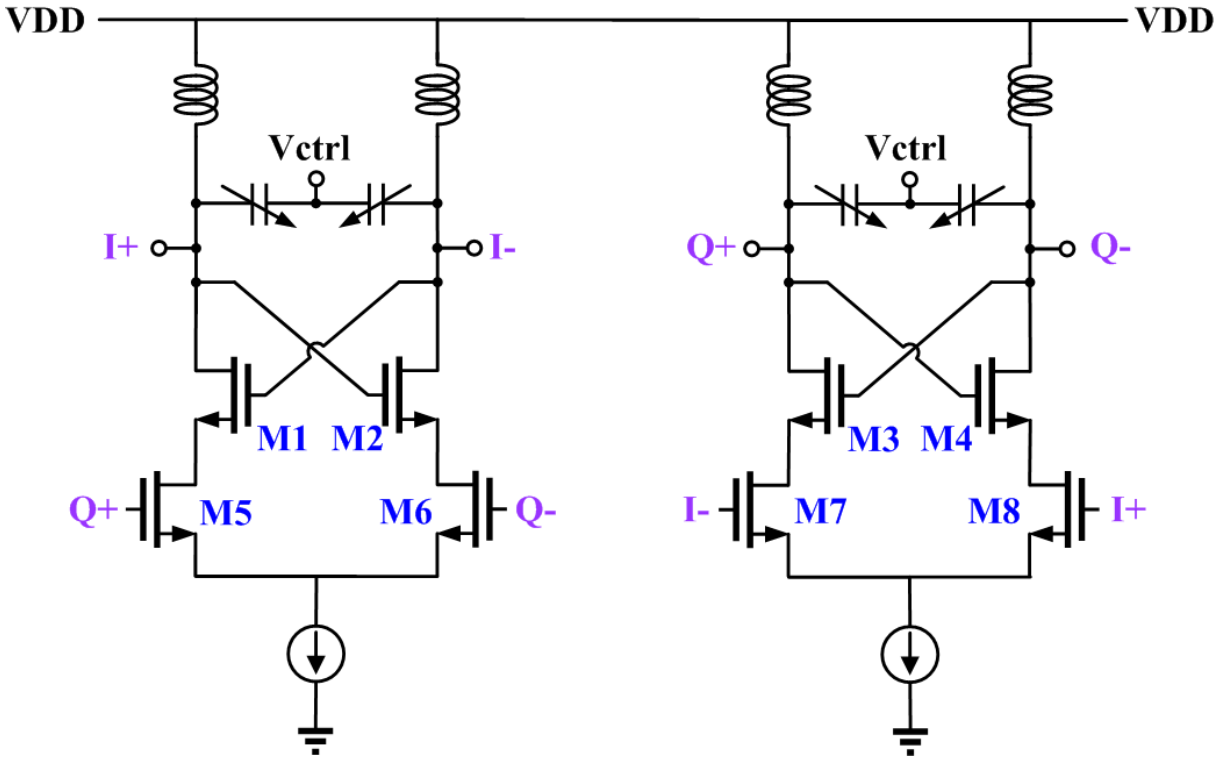

Fig. 3 - 3 Schematic of the conventional bottom series-coupled QVCO (BS-QVCO)

The major problem with this architecture is that the coupling transistors have to be about five times larger than the negative resistance transistors [24], thus loading the oscillator with large parasitic capacitances that reduce the tuning range, making this solution unsuitable for high frequency and wideband application.

There is an alternative way to achieve series coupling, as shown in Fig. 3 - 3, known as the Bottom Series (BS) QVCO [25]. In this configuration the coupling transistor is placed at the bottom of the switching transistor. As for the TS-QVCO, the phase error is almost independent of coupling strength α_B. When both BS-QVCO and P-QVCO display the same phase-error and have the same center frequency and power consumption, BS-QVCO has a higher figure of merit (FOM). However, to compare with TS-QVCO, BS-QVCO has a higher FOM but also a higher phase error than TS-QVCO.

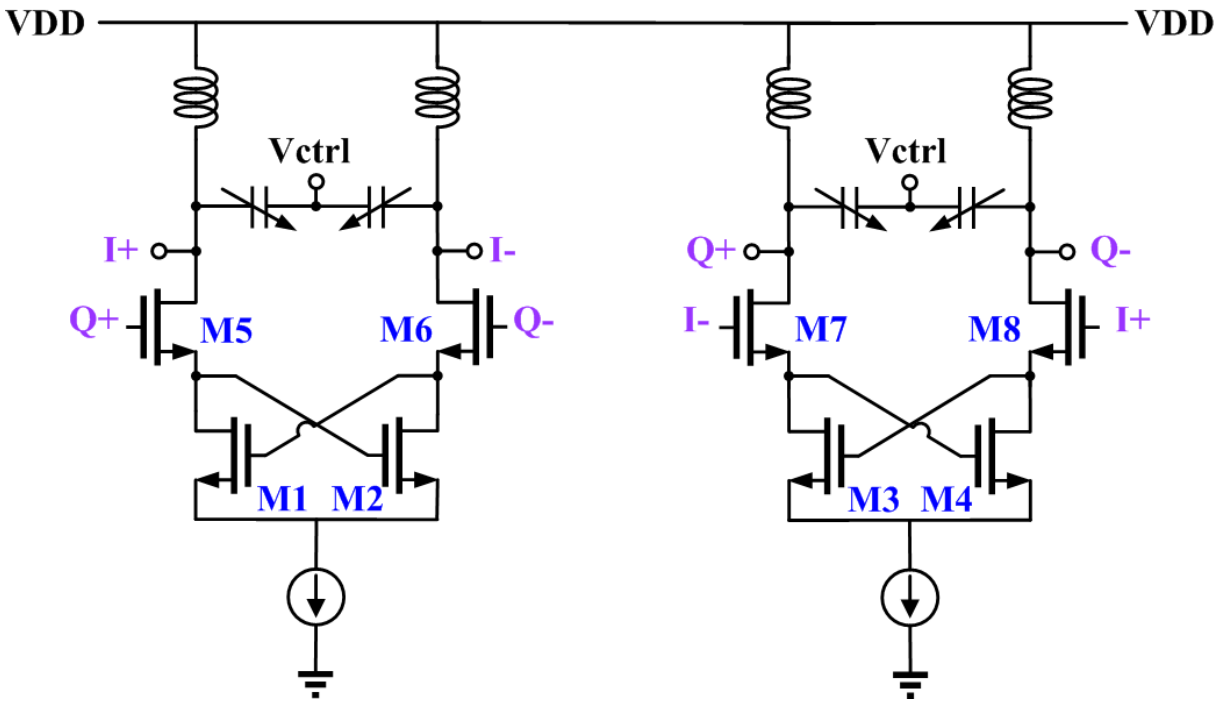

Fig. 3 - 4 Schematic of the conventional middle series-coupled QVCO (MS-QVCO)

Another alternative topology of series connection is the Middle Series (MS) QVCO [25], which is basically an improved TS-QVCO, as shown in Fig. 3 - 4. This topology has a higher Figure of Merit (FOM) than the other three topologies, but a phase error which is between that of the TS-QVCO and the BS-QVCO. It features very low phase noise especially at a low frequency offset [24].

In modern submicron CMOS processes, the flicker noise (1/f noise) is a significant noise source and is a critical issue in VCO design. As reported in [26]-[30], shown in Fig. 3 - 5, that periodically switching a MOS transistor between "on" and "off" states results in a significant reduction of the flicker noise. It was also revealed that the switching of the tail current source by applying a sine or square wave can reduce 1/f noise itself. Oscillator circuits are suitable for applying a switched biasing technique in that they can use an oscillation waveform by itself for the switching of the tail current source, as shown in Fig. 3 - 6.

Generally, it has been known that flicker noise is generated by the carrier trapping in localized oxide states [27]. Switching a MOS transistor will force the release of captured electrons or holes from a trap. The higher the frequency of a switching waveform is, the smaller the flicker noise will be. According to [27], the phase noise characteristic of an oscillator with switching bias has been reported to be reduced by 8 dB compared with a fixed bias. Furthermore, using switching bias can also reduce the power consumption.

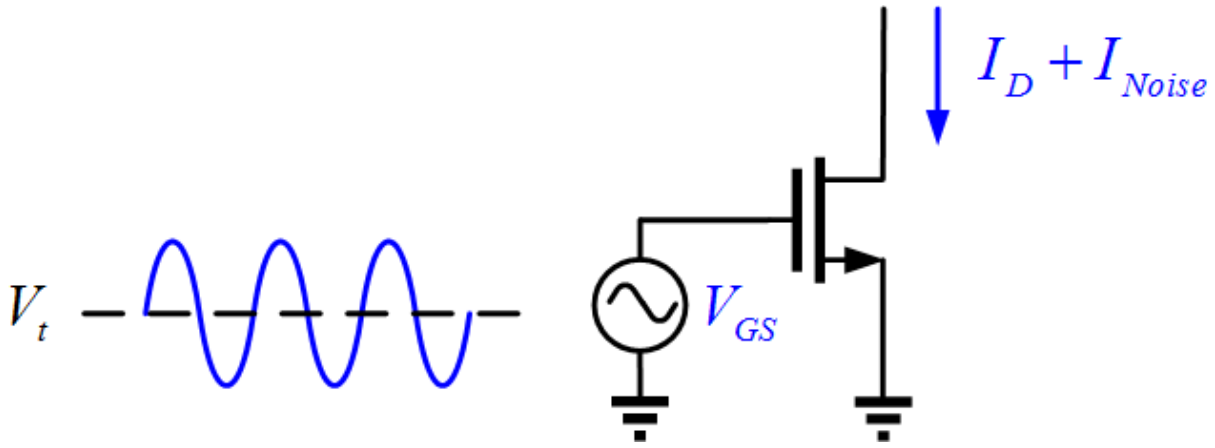

Fig. 3 - 5 Varying V_{GS} cycles a MOS transistor between "on" and "off"

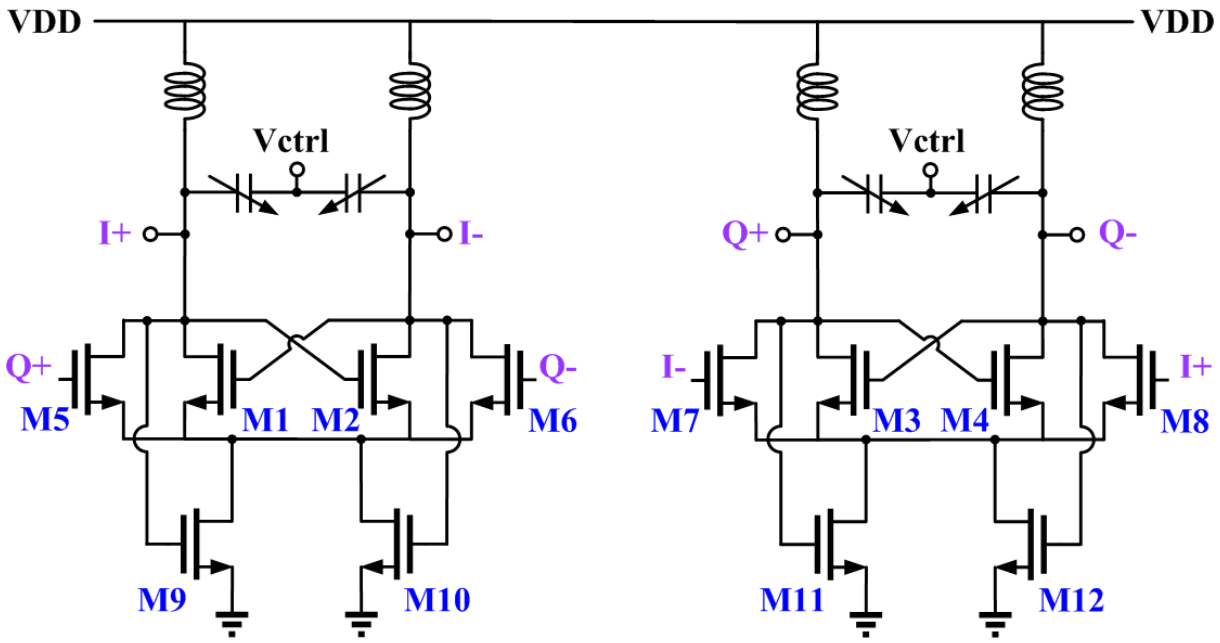

Fig. 3 - 6 Schematic of the conventional self-switching biased QVCO

The circuit we proposed in this chapter using a novel low noise capacitor-coupling method to perform injection locking, and therefore quadrature signals at the output can be obtained. Moreover, this novel low noise capacitor-coupling CR-QVCO topology adopts a self-switching bias and a tail current-shaping technique to suppress the 1/f noise from a tail current source. By using these large signal sine-wave outputs to make the tail-current transistors self-switching, the advantage of lower phase noise and lower power consumption can be simultaneously achieved. The proposed QVCO has four states of oscillating behavior, and it is a novel QVCO topology in comparison with the above-mentioned QVCOs. The circuit design consideration will be discussed in next section.

3.2 Circuit Design Consideration

The schematic of the proposed self-switching biased current reused quadrature VCO (CR-QVCO) is shown in Fig. 3 - 7. In this novel CR-QVCO topology, three mechanisms are incorporated to improve the phase noise :

I. A novel low noise capacitor-coupling technique was adopted to generate quadrature signals. As highlighted in Fig. 3 - 8, the outputs are injected to the source node of the cross coupled transistors through four noiseless components, capacitors. Consequently, there were no extra noise source incorporated in order to generate quadrature signals.

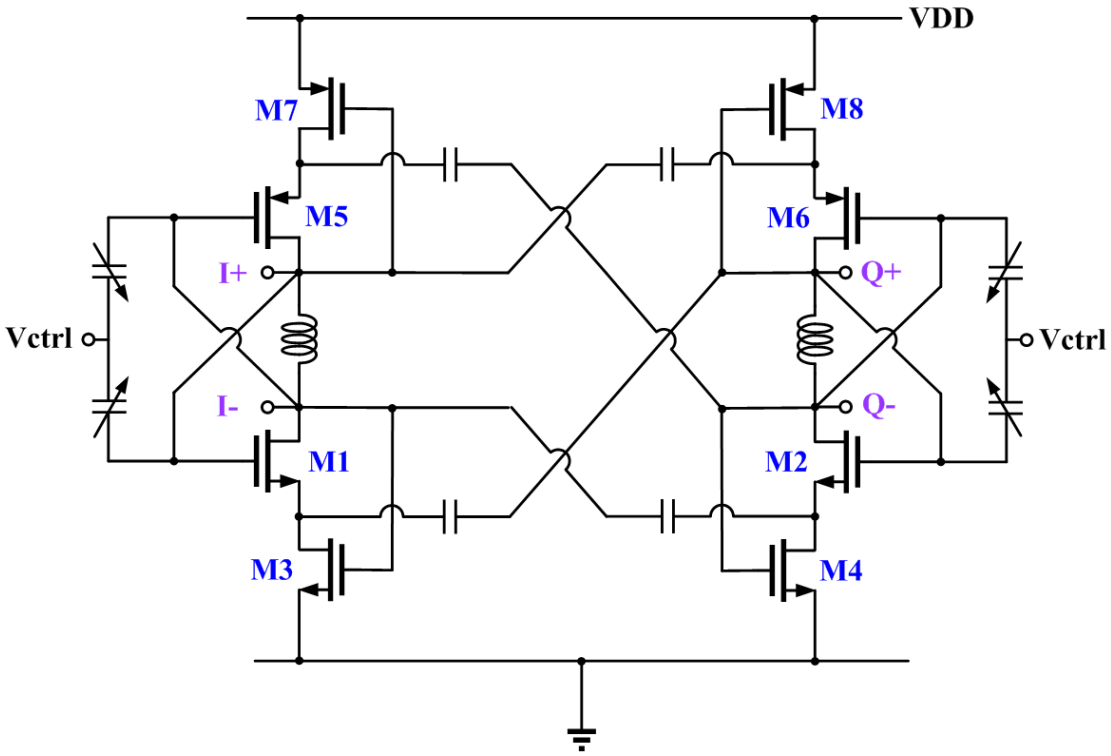

Fig. 3 - 7 Schematic of the proposed self-switching biased QVCO

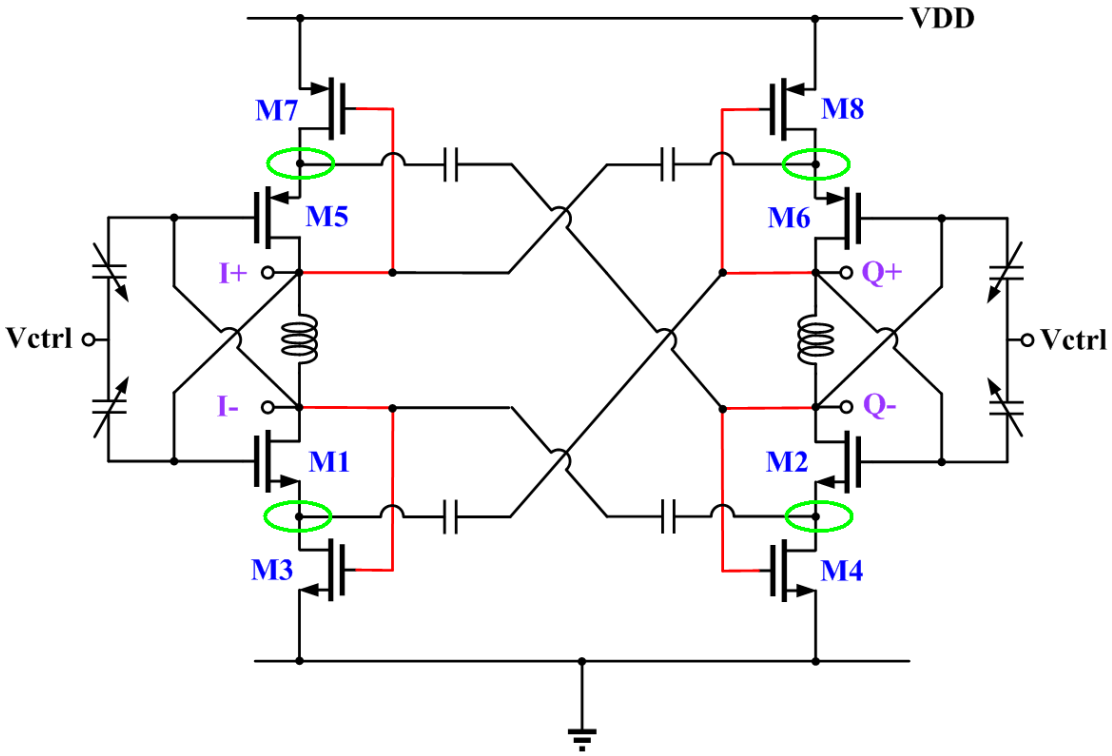

Fig. 3 - 8 Novel injection method of the proposed self-switching biased QVCO

II. By using the self-switching bias and tail current shaping technique, we can decrease the active time of the noise source, i.e., the tail current source, to reduce the oscillator phase noise. In addition, it also has benefit of saving power since each of the tail current transistors, which has about 50% on-off operation of duty cycle, needs only half of the dc power consumption as compare to the constant dc bias counterpart. Note that in the proposed self-switching biased CR-QVCO, only one switching transistor were used in each tail current source, rather than the dual-switching-transistor topology shown in Fig. 3 - 6. Consequently, the proposed self-switching biased current reused QVCO can further reduce the power consumption by combining the single switching-tail-current topology and the current-reused topology. Moreover, switching a MOS transistor will force the release of captured electrons or holes from a trap, and hence the tail current transistors with less flicker noise were obtained.

III. Using a novel CR-QVCO topology with the alternatively turn-on mechanism between tail current transistors and cross-coupled switching transistors. As shown from Fig. 3 - 9 to Fig. 3 - 12, the proposed CR-QVCO has four states during an oscillation period. In each state, the cross coupled transistor and tail current transistor, for example, M1 and M3, would never turn on simultaneously. There is no dc conducting path from VDD to ground and only the ac conducting path exists. Note that the conventional complementary CR-QVCO as we proposed in Chapter 2, shown in Fig. 2 - 9, has two half-period (In which, the first half-period is that all the transistors turn on ,and a dc conducting path from VDD to ground was established. The second half-period then becomes that all the transistors turn off) . Thanks to this alternatively turn-on mechanism, the noise current generated by the tail current transistors would be blocked, and high spectral-purity output can be obtained.

Fig. 3 - 13 and Fig. 3 - 14, in which the definitions of current-flow were marked in Fig. 3 - 15, shows the simulated currents in the current-limited regime and voltage-limited regime, respectively. Fig. 3 - 13 and Fig. 3 - 14 also give a clear illustration about the behavior of alternatively turn-on mechanism.

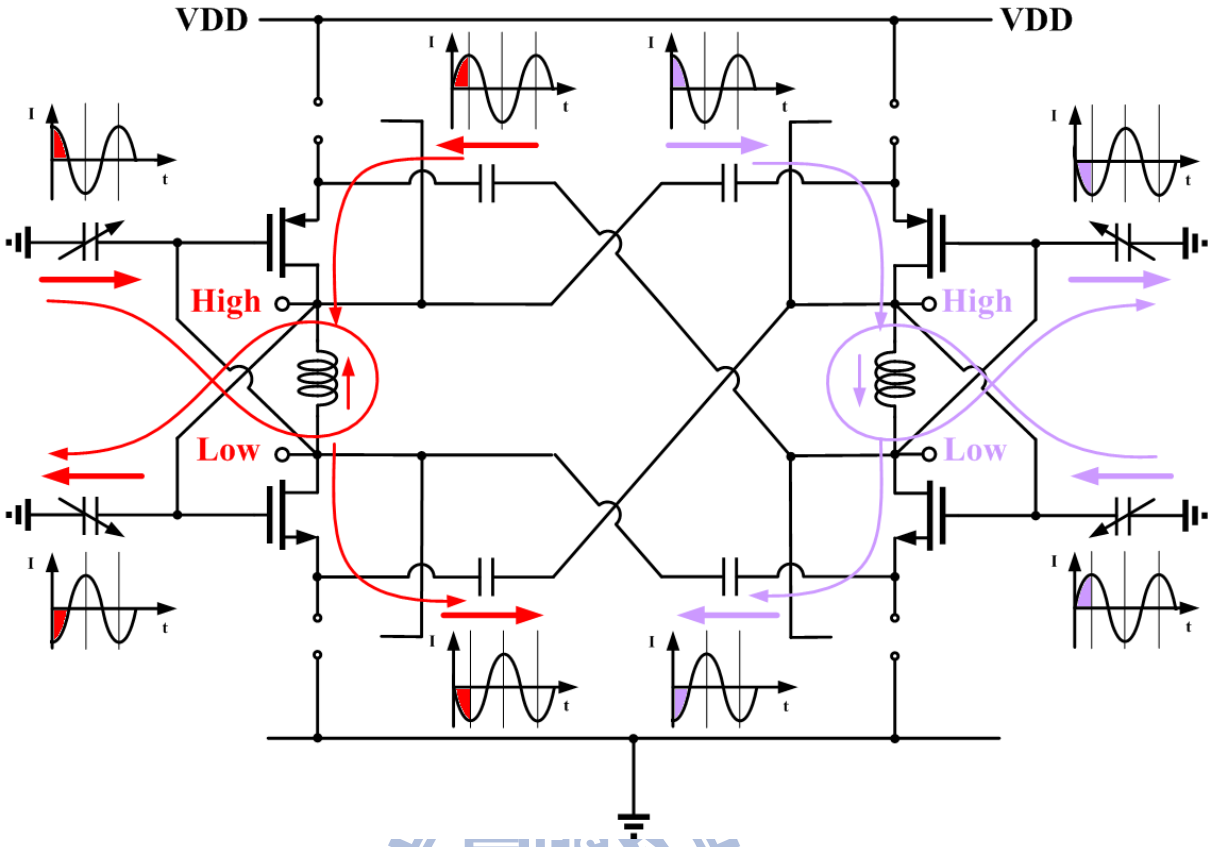

Fig. 3 - 9 State-1 of the proposed self-switching biased QVCO

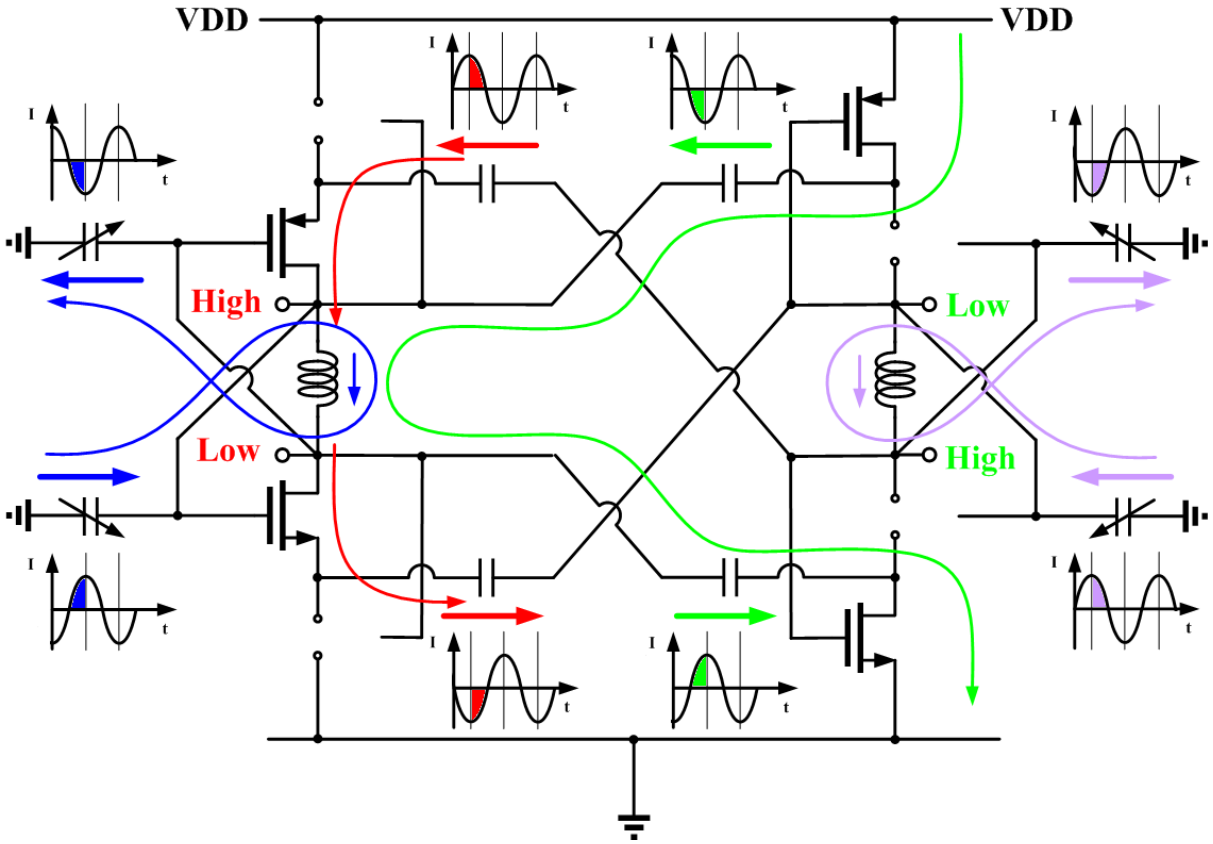

Fig. 3 - 10 State-2 of the proposed self-switching biased QVCO

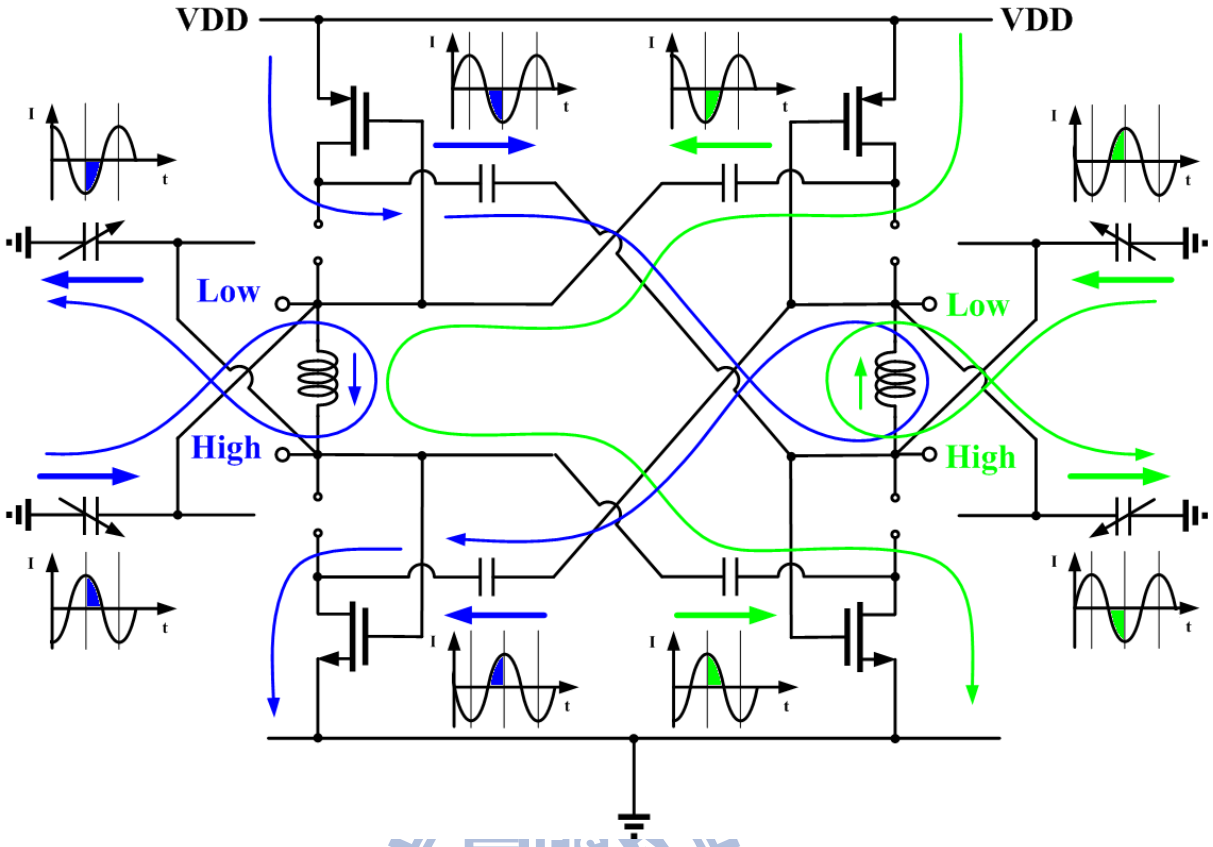

Fig. 3 - 11 State-3 of the proposed self-switching biased QVCO

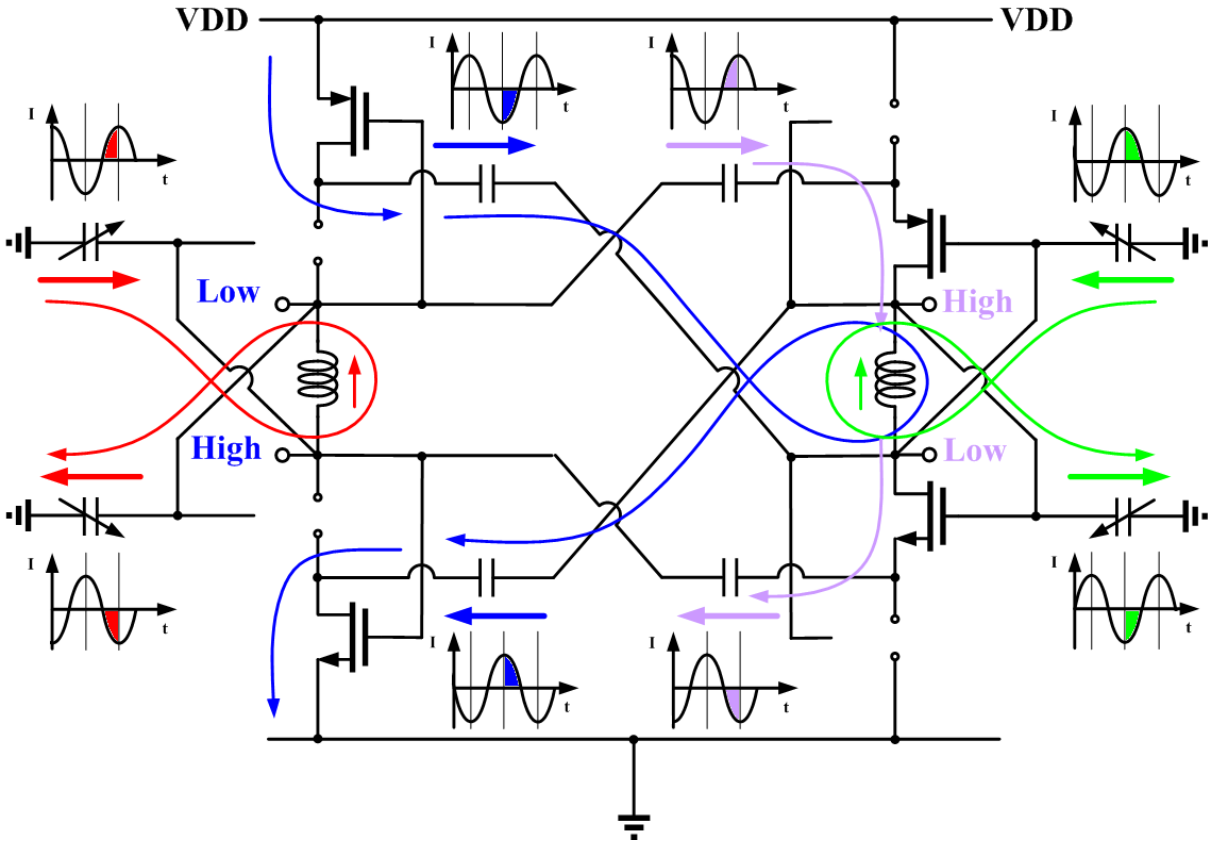

Fig. 3 - 12 State-4 of the proposed self-switching biased QVCO

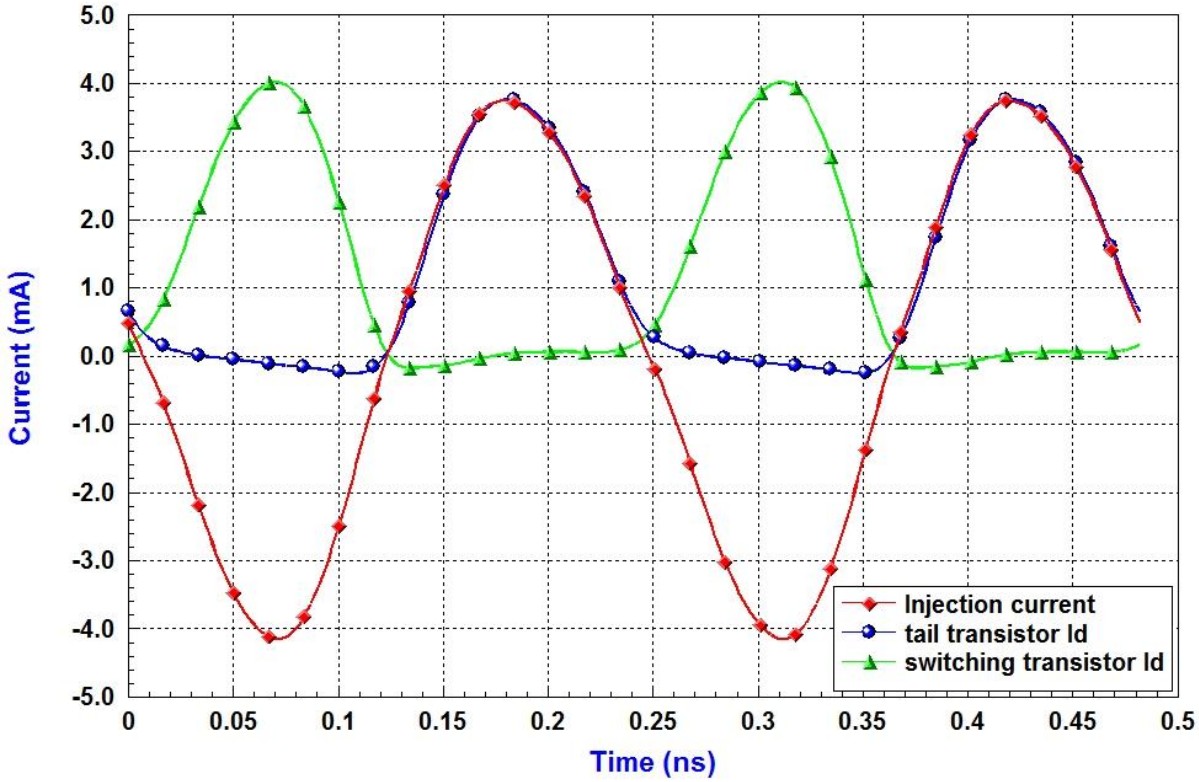

Fig. 3 - 13 Simulated currents in the current-limited regime

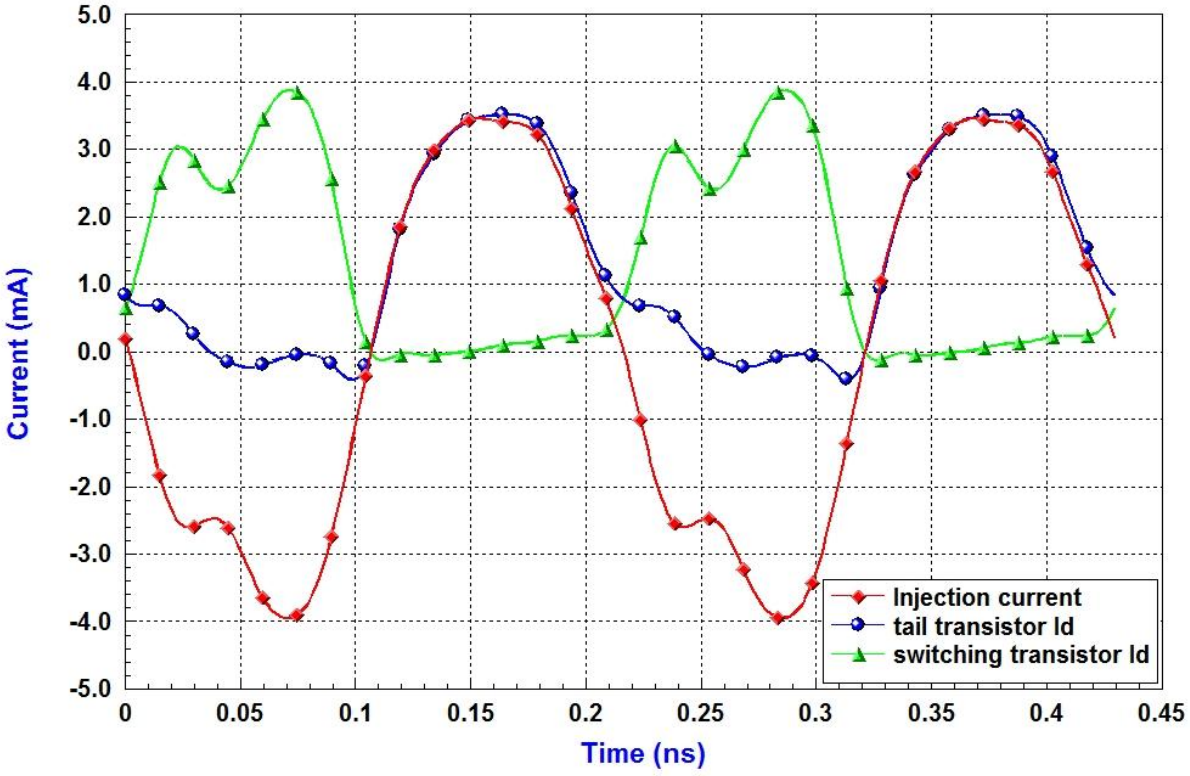

Fig. 3 - 14 Simulated currents in the voltage-limited regime

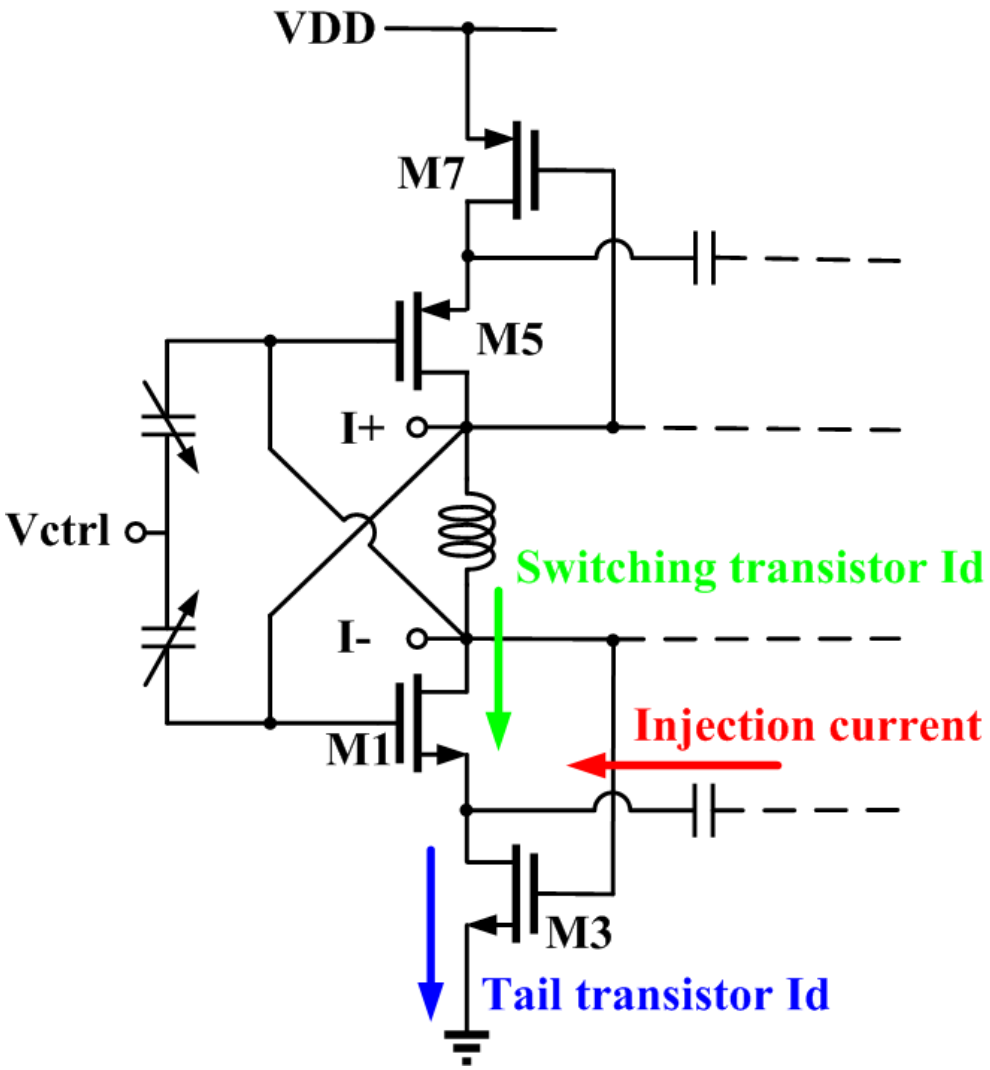

Fig. 3 - 15 The definitions of current-flow used in Fig. 3 - 13 and Fig. 3 - 14

3.3 Chip Layout and Simulation Results

The circuit was simulated and optimized using Agilent ADS. The design procedure can be divided in two steps. First, a small signal analysis was used to optimize the feedback and the resonator elements to find the oscillation condition at the target frequency. This condition was simulated breaking the feedback path. In the second step, a large signal analysis was performed with the harmonic balance simulator to predict the exact oscillation frequency and output power of the fundamental signal as well as the harmonic signals.

Fig. 3 - 16 shows the chip layout photograph of the proposed modified STM current reused QVCO, which is designed and implemented in TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The chip size is 1.100 × 0.841 mm^2 including all pads and bypass capacitances. Each buffer of the QVCO outputs were designed as a common-source amplifier.

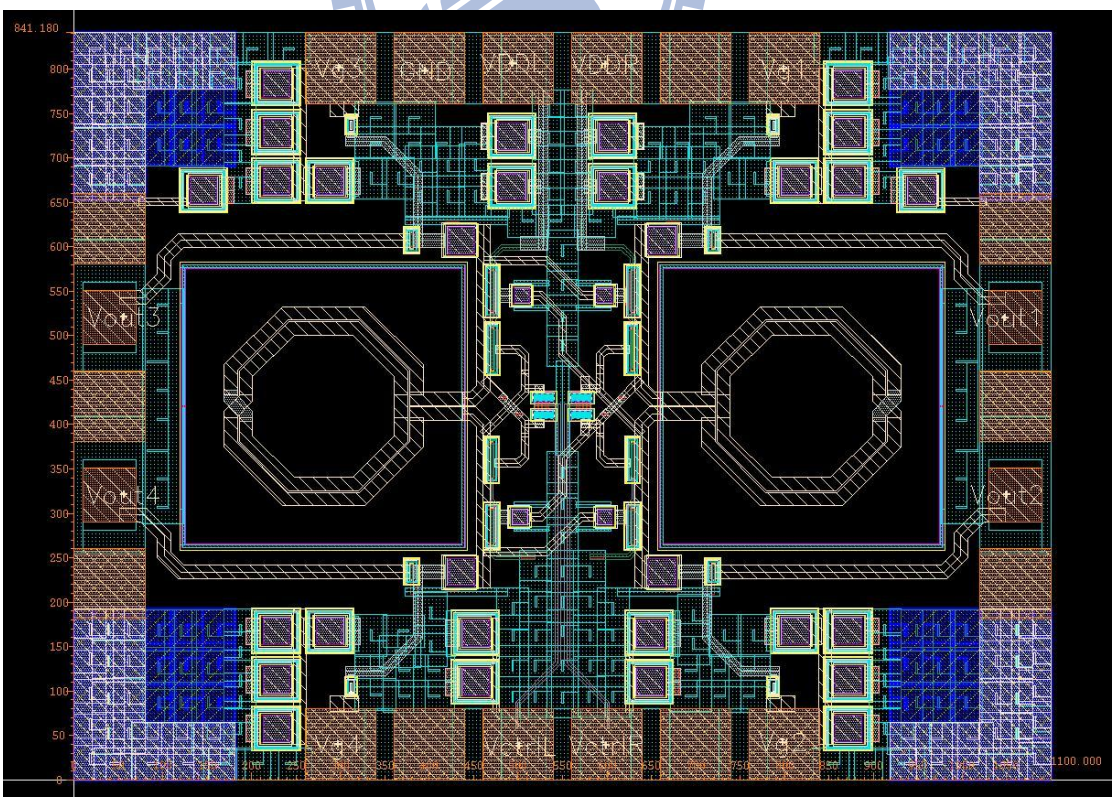

Fig. 3 - 16 Chip layout of the proposed self-switching biased QVCO

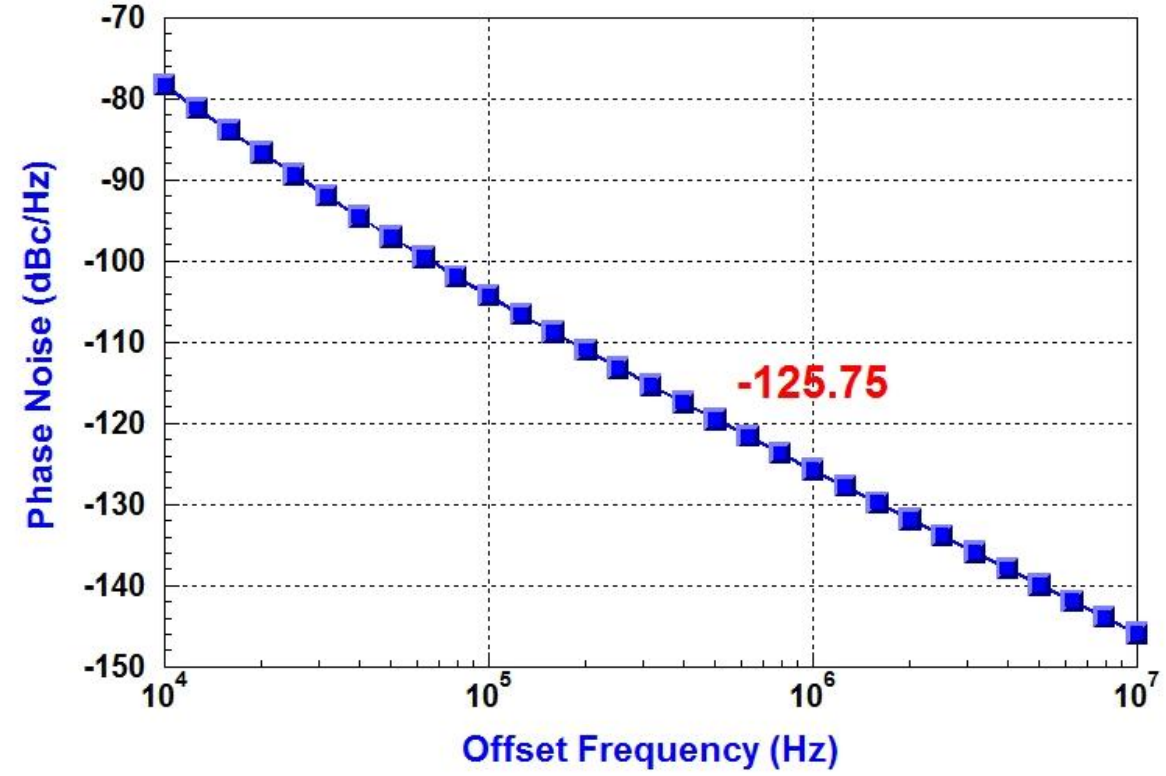

Fig. 3 - 17 Simulated phase noise of the proposed self-switching biased QVCO

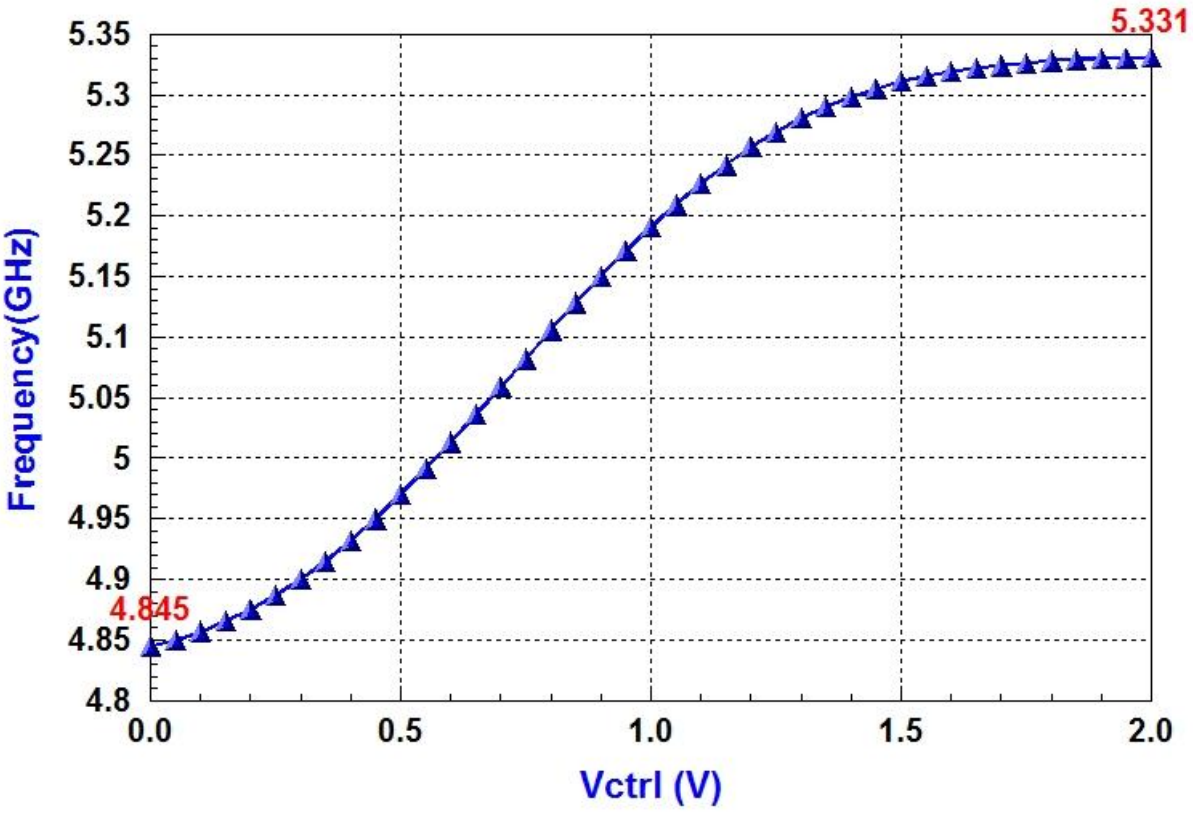

Fig. 3 - 18 Simulated tuning range of the proposed self-switching biased QVCO

The simulated phase noise and tuning range of the proposed modified STM QVCO are shown in Fig. 3 - 17and Fig. 3 - 18,respectively. Table 3 - 1 summarizes the simulated results of the proposed modified STM QVCO in each corner. The figure of merits (FOM) for oscillators summarizes the important performance parameters, i.e., phase noise and power consumption P, to make a fair comparison is defined in [40] as

$$FOM = L(\Delta\omega) + 20\log\left(\frac{\Delta\omega}{\omega_O}\right) + 10\log\left(\frac{P}{1mW}\right)$$

where the second term is to neutralize the effect of offset in L(Δω) while taking the center frequency into account. The power consumption is calculated as dBm such that the unit of FOM remains the same as that of L(Δω).

Table 3 - 1 Simulated results of the proposed modified STM-QVCO

Corner	SS	TT	FF	SF	FS
Tuning Range	4.64-5.11	4.84-5.32	5.07-5.58	4.84-5.33	4.85-5.33
Phase Noise	-126.295	-125.750	-124.371	-125.841	-125.442
Supply Voltage	1.5	1.35	1.15	1.35	1.35
ID	1.97	1.98	1.6	2.11	1.89
Core Power	2.95	2.67	1.84	2.84	2.55
FOM	-194.93	-195.18	-195.82	-195.00	-195.07

3.4 Measurement Results and Discussion

3.4.1 Measurement Consideration

The proposed QVCO are designed for on-wafer testing, and the DC voltage are supplied by two sets of six-pin probe, so that the distance between each DC pad must more than 50μm to satisfy the probe testing rules. The output buffer of each quadrature output is designed using common-source amplifier, and the drain end of each buffer is connected to the RF pad. For measurement, we connect four bias-tee terminals to the corresponding RF pads as shown in Fig. 3 - 19.

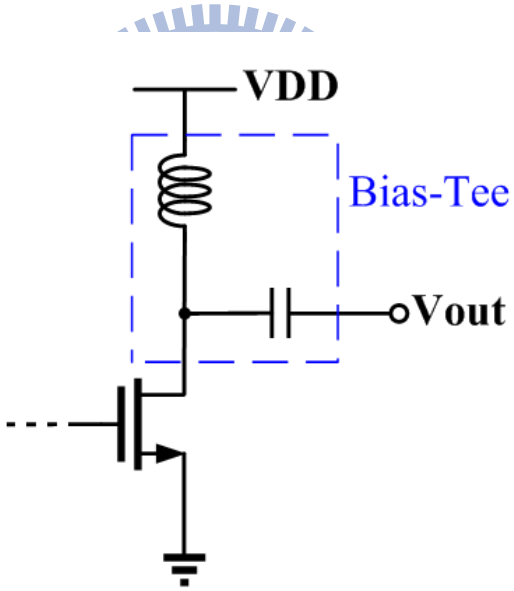

Fig. 3 - 19 Bias-Tee Model

The phase noise, tuning range, output spectrum and output waveform are measured using signal source analyzer (Agilent E5052B) and digital signal analyzer (Agilent DSA91204A) shown in Fig. 3 - 20 and Fig. 3 - 21, respectively.

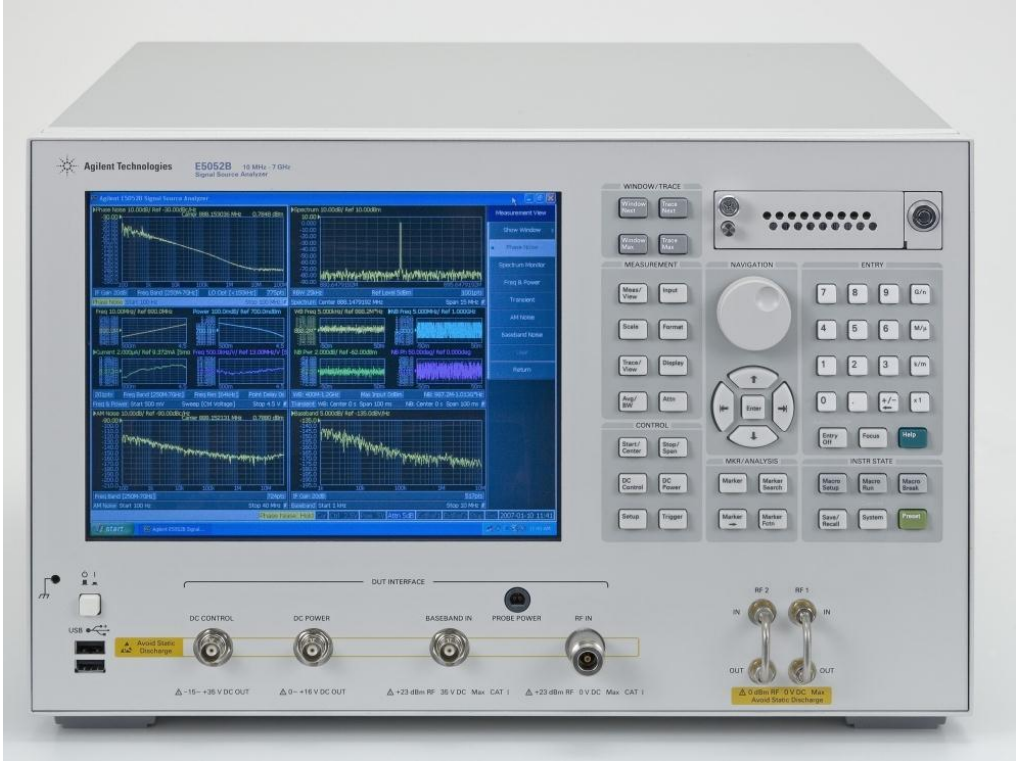

Fig. 3 - 20 Signal Source Analyzer (Agilent E5052B)

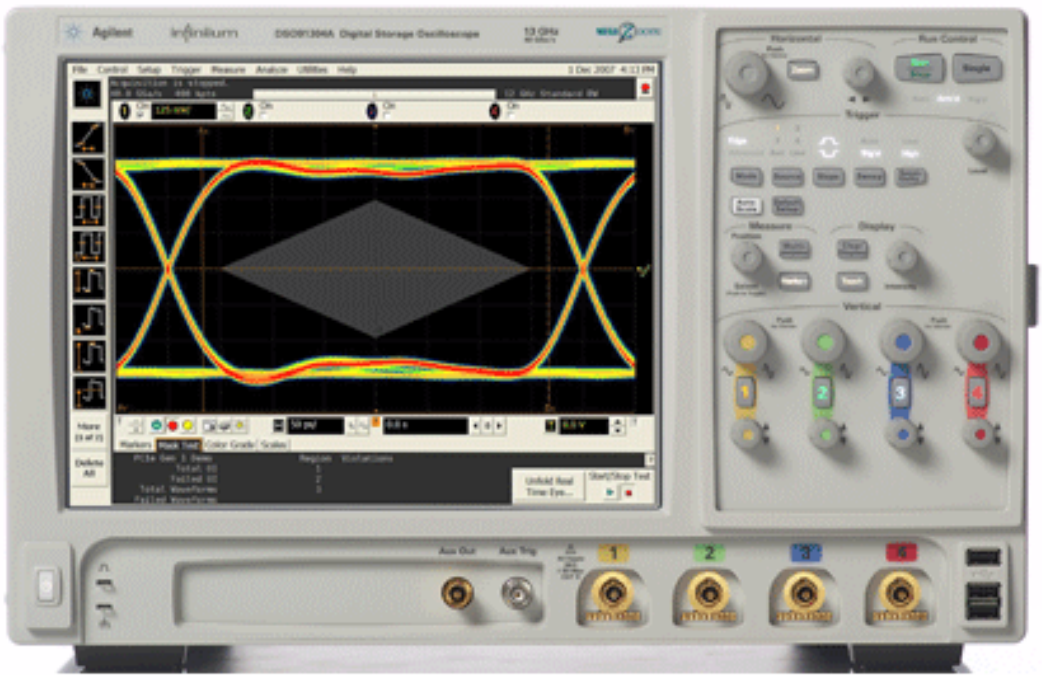

Fig. 3 - 21 Digital Signal Analyzer (Agilent DSA91204A)

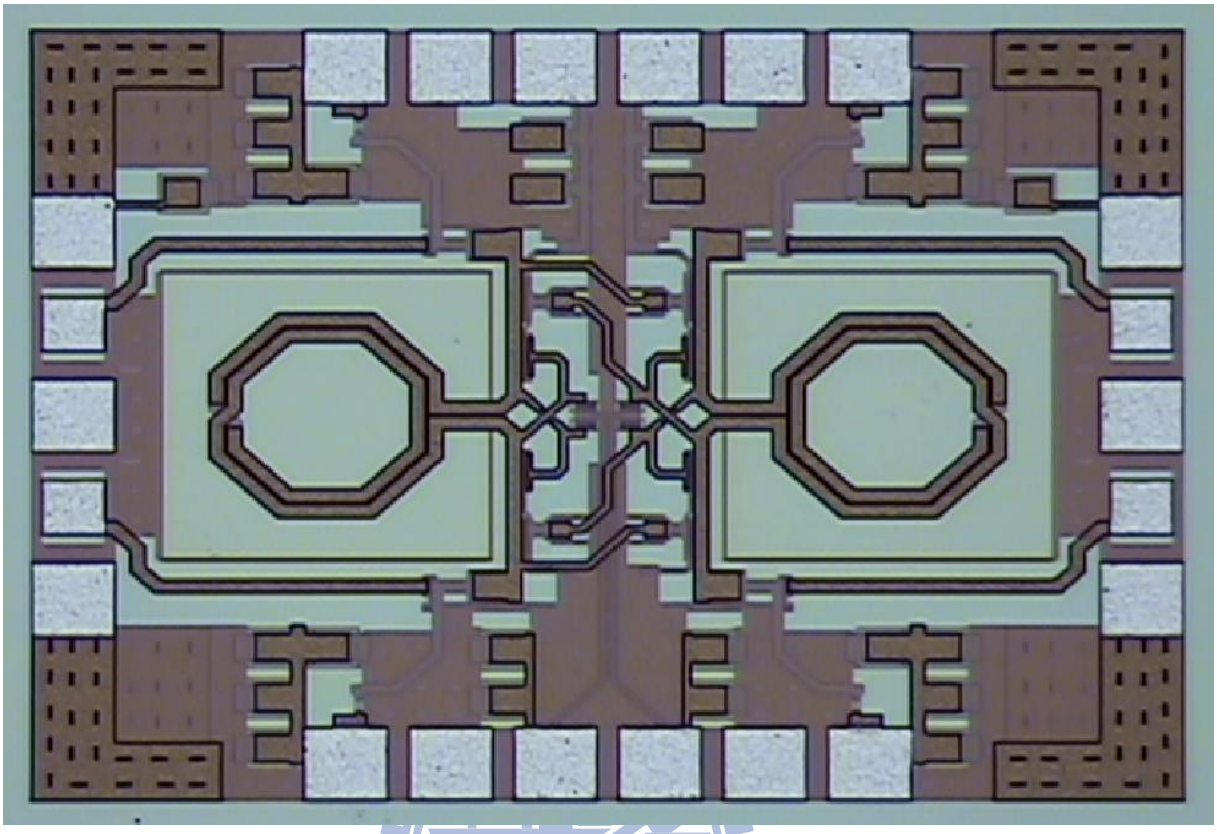

Fig. 3 - 22　Chip photo of the proposed self-switching biased CR-QVCO

The Chip photo of the proposed self-switching biased CR-QVCO is shown in Fig. 3 - 22. Fig. 3 - 23 and Fig. 3 - 24 shows the arrangement of DC and RF probes. The measured phase noise at 4.83GHz, measured phase noise at 5.3GHz, output spectrum, tuning range, and output waveform was shown in Fig. 3 - 25 to Fig. 3 - 29, respectively. Table 3 - 2 summarizes the measured performance of the proposed self-switching biased CR-QVCO.

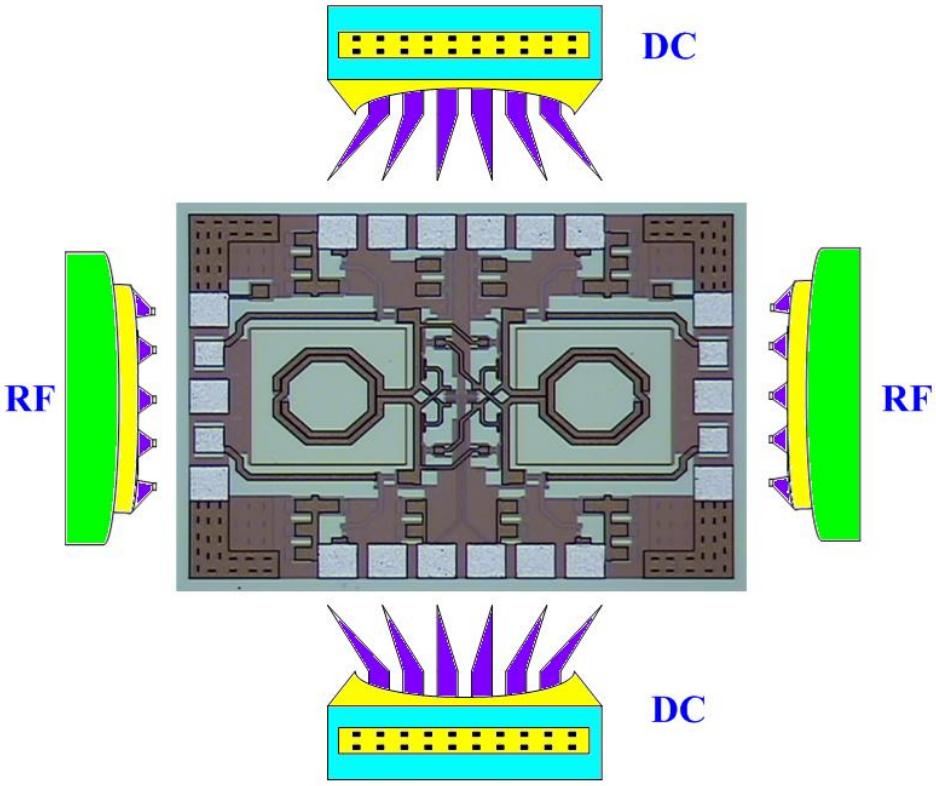

Fig. 3 - 23　Arrangement of DC and RF probes

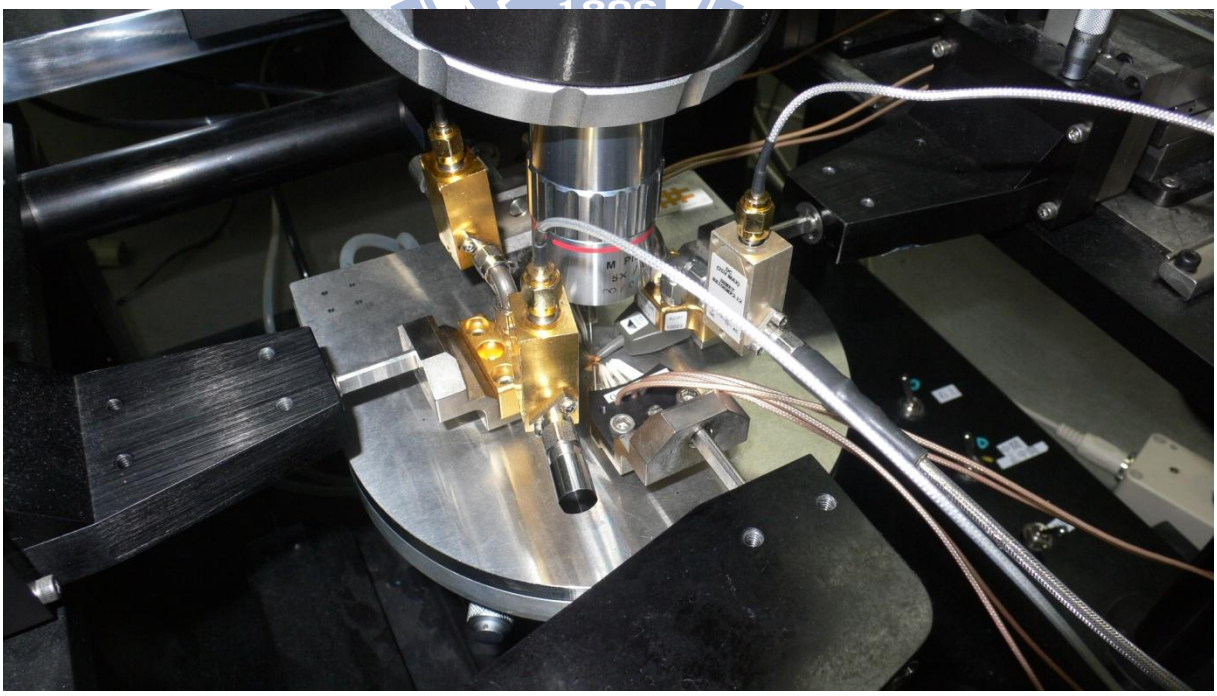

Fig. 3 - 24　Photograph of the probe station

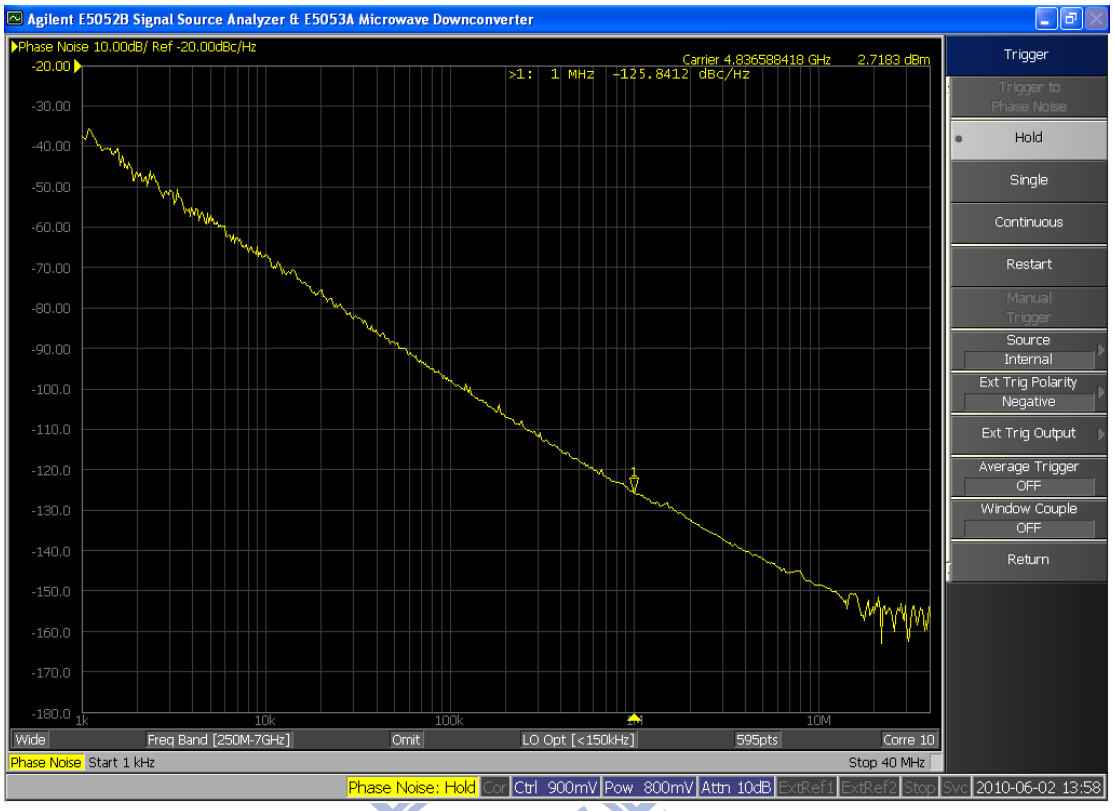

Fig. 3 - 25 Measured phase noise of the proposed self-switching biased QVCO at f_o = 4.83GHz

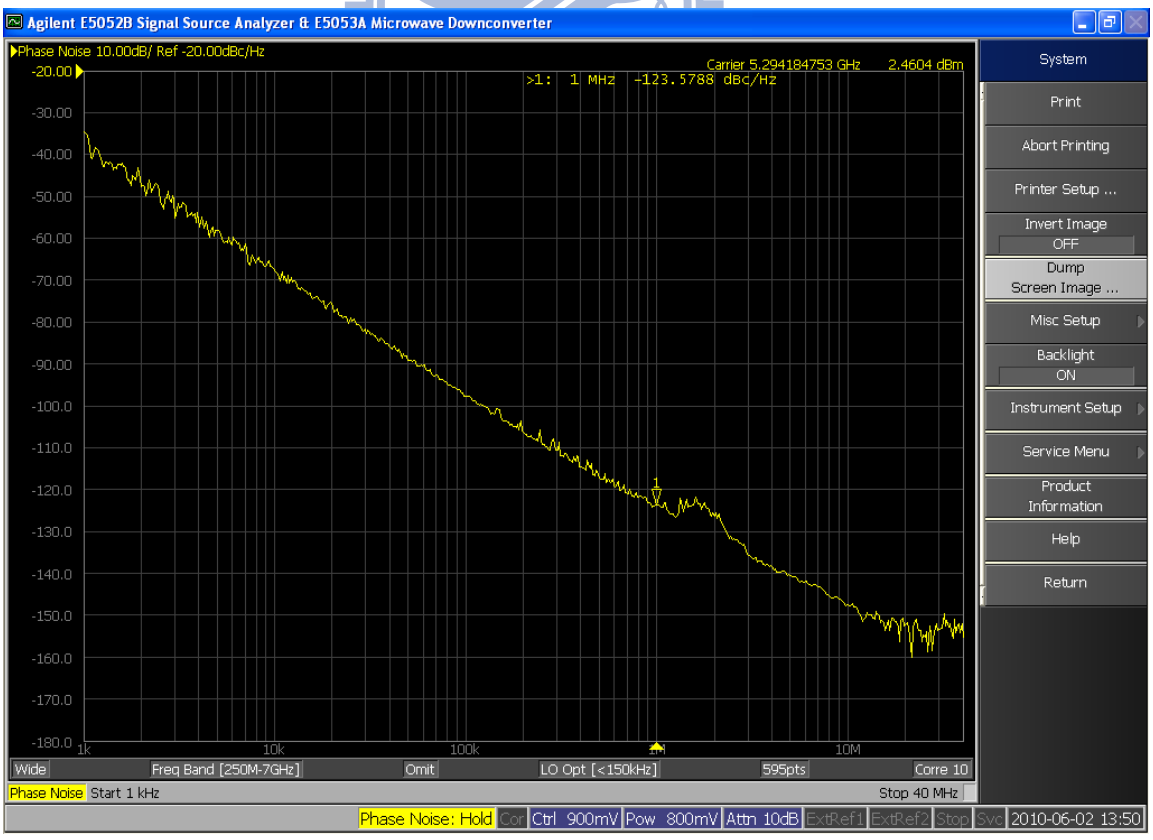

Fig. 3 - 26 Measured phase noise of the proposed self-switching biased QVCO at f_o = 5.29GHz

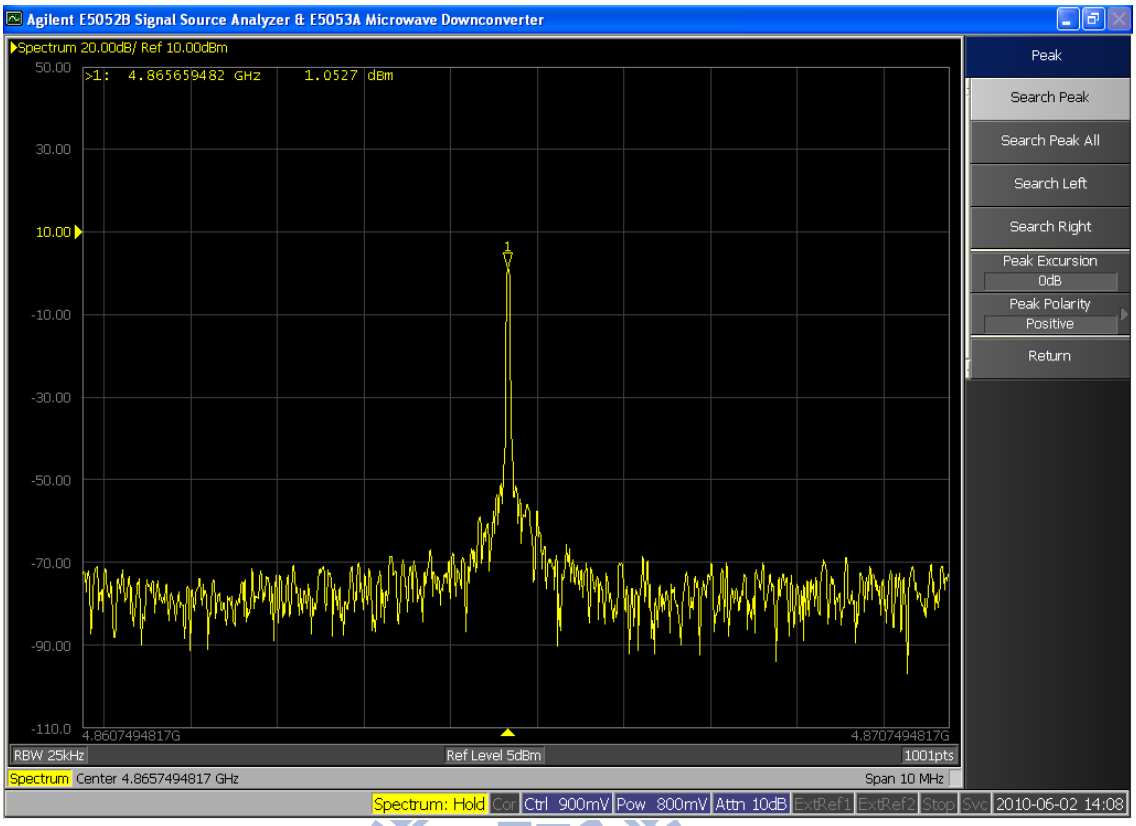

Fig. 3 - 27 Measured output spectrum of the proposed self-switching biased QVCO

Fig. 3 - 28 Measured tuning range of the proposed self-switching biased QVCO

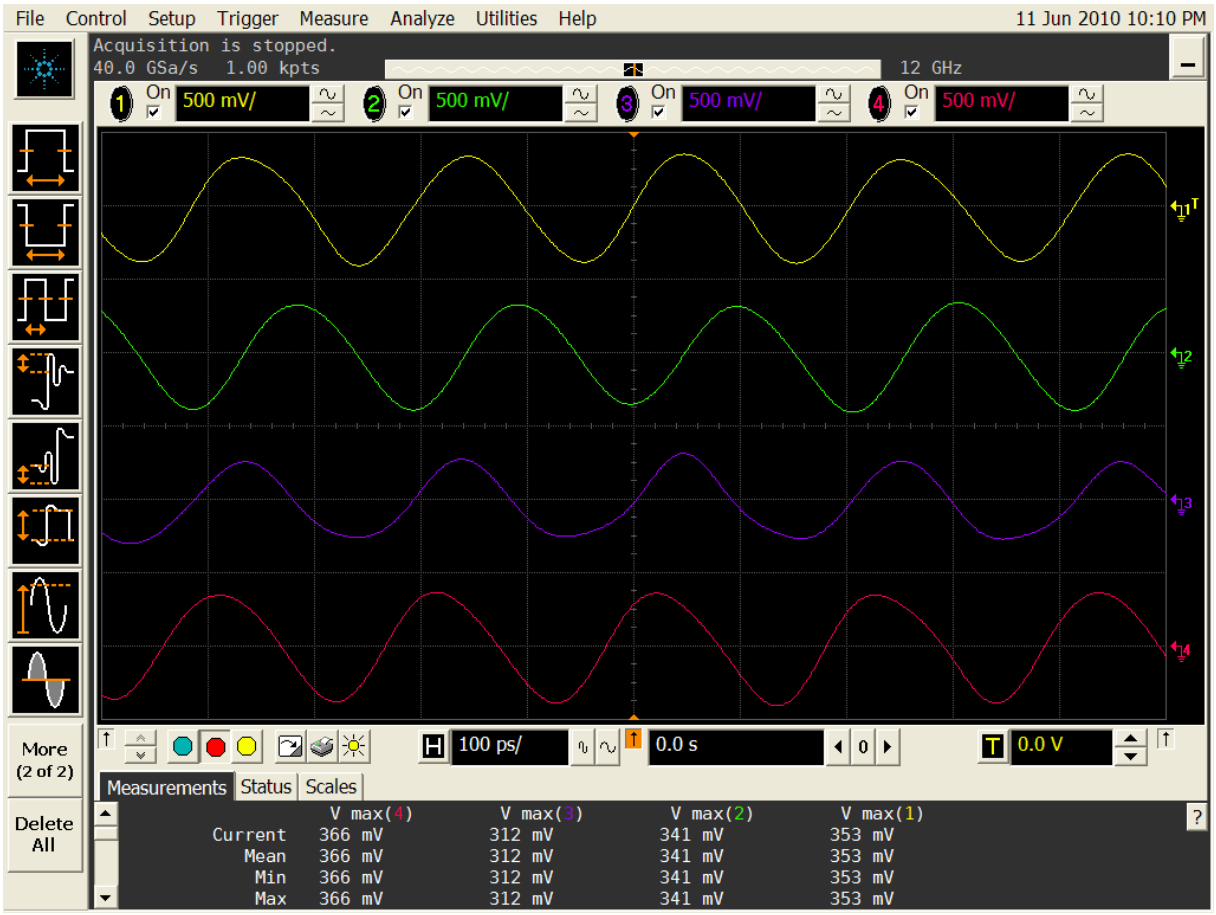

Fig. 3 - 29 Measured output waveform of the proposed self-switching biased QVCO

Table 3 - 2 Comparison of QVCO Performance

	Technology	Tuning Range	Phase Noise	Supply Voltage	Core Power	FOM
This work (Chapter 2)	0.18μm CMOS	4.84-5.17 GHz	-117.4 dBc/Hz@ 1MHz	1.3V	5.04mW	-184.07
This work (Chapter 3)	0.18μm CMOS	4.83-5.30 GHz	-125.8 dBc/Hz@ 1MHz	1.3V	3.64mW	-193.87
[7] MWCL, 2009	0.18μm CMOS	4.39-5.26 GHz	-113.65 dBc/Hz@ 1MHz	1.8V	6.3mW	-180.0
[8] MWCL, 2005	0.18μm CMOS	5.50-6.10 GHz	-115 dBc/Hz@ 1MHz	1.8V	1.84mW	-182.2
[42] MWCL, 2009	0.18μm CMOS	2.05-2.47 GHz	-117 dBc/Hz@ 1MHz	1.8V	2.84mW	-184
[43] MWCL, 2009	0.18μm CMOS	4.38-4.71 GHz	-120.8 dBc/Hz@ 1MHz	1.1V	2.55mW	-189.61
[9] MWCL, 2007	0.18μm CMOS	1.83-2.02 GHz	-124 dBc/Hz@ 1MHz	1.25V	2.2mW	-186.7
[17] MWCL, 2009	0.18μm CMOS	3.01-3.49 GHz	-133 dBc/Hz@ 1MHz	1.5V	8.1mW	-193.5

Chapter 4

Conclusion and Future Work

4.1 Conclusion

In chapter 2, we proposed a new architectures for low phase noise current-reused QVCO : current-reused quadrature VCO with modified spontaneous transconductance match (M-STM). Adopting the M-STM technique reduce the amplitude imbalanced ratio. The measured results reveal that the tuning range is between 4.84 - 5.17 GHz, the phase noise is -117.4 dBc/Hz at 1MHz offset, and the power consumption is 5.04mW under 1.3V supply voltage.

In Chapter 3, we proposed another new architecture for low phase noise current-reused QVCO : current-reused low phase noise quadrature VCO with self-switching bias. Three mechanisms are incorporated to improve the phase noise :

1. A novel low noise capacitor-coupling technique
2. By using the self-switching bias and tail current shaping technique
3. Using a novel CR-QVCO topology with the alternatively turn-on mechanism between tail current transistors and cross-coupled switching transistors.

The measured results reveal that the tuning range is between 4.83-5.30 GHz, the phase noise is -125.8 dBc/Hz at 1MHz offset, and the power consumption is 3.64 mW under 1.3V supply voltage.

Finally, we introduce a wideband CMOS down-converting mixer for W-band receiver

application in the appendix. This mixer has the RF frequency chosen to be 8.7 - 17.4GHz, LO frequency fix at 17.5GHz, and IF frequency close to 0.1 - 8.8GHz. In order to reduce the difficulty in designing the corresponding LO module, another mixer with the integrated LO frequency doubler has also been proposed in the appendix.

4.2 Future Work

Although The main purpose of this thesis focus on the study of the low phase noise current reused quadrature VCOs, I also started the study of the PLLs, frequency synthesizers, and switching power supply. All of these analog and mixed signal circuit will be my future research topics.

Appendix A

Wideband CMOS Down-Converting Mixer for W-Band Receiver

A.1 Introduction

Mixers are key components of an RF front-end, translating the IF signal to a carrier frequency for transmission and from RF carrier back down to IF for detection. Mixer essentially modulations either the transconductance of an amplifier or the resistance of a switch to produce the mixing action through time-varying mechanism. Although there are many topologies of mixers (single-balanced、double-balanced...etc.), the double-balanced

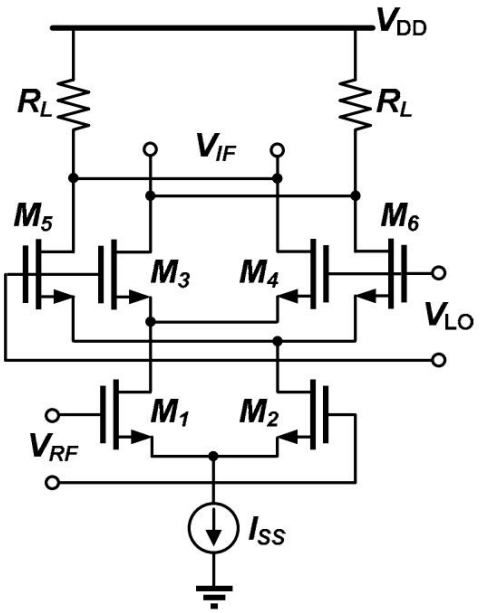

Fig. A - 1 Conventional double balanced mixer

circuit configuration have been readily appearing in microwave and millimeter wave applications for its good isolations.

For example, as indicated in Fig. A - 1, the schematic is a typical double balanced mixer. In order to enhance the conversion gain, it is perhaps to use large R_L. However, as R_L increasing, the voltage drop between R_L will also increasing, therefore minimizing the output swing. Increasing the power supply V_{DD} is a solution but it will consume more power. An alternative solution is externally injecting current by using the two current sources as indicated in Fig. A - 2, However, this solution can't be applied at tens of GHz, since the current source are usually made of p-type transistor, the output impedance of the current source tend to decrease at high frequency and thus deteriorated the mixer's performance at the high frequency.

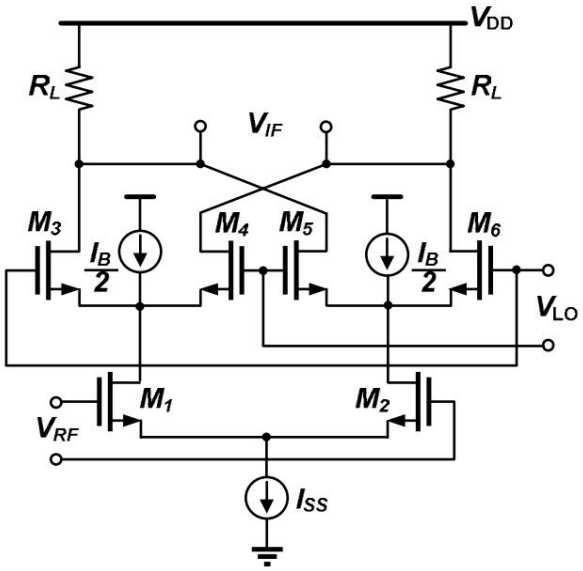

Fig. A - 2 Conventional double balanced mixer with gain-enhancement

So far, most of the mixers with normal-biased transistors, as contrast to resistors with no drain to source bias, have their wideband proclamation illustrated by shifting the LO across the intended RF bandwidth, while keeping the IF wideband comparatively small, i.e.,

wideband RF-bandwidth but narrow IF-bandwidth. With an IF bandwidth of hundreds of MHz, a large output signal voltage can be easily achieved by replacing each R_L in Fig. A - 2 with an appropriate p-type transistor as a active load, for which is capable of providing a large impedance at low frequency. However, when the IF bandwidth is extended to several GHz,

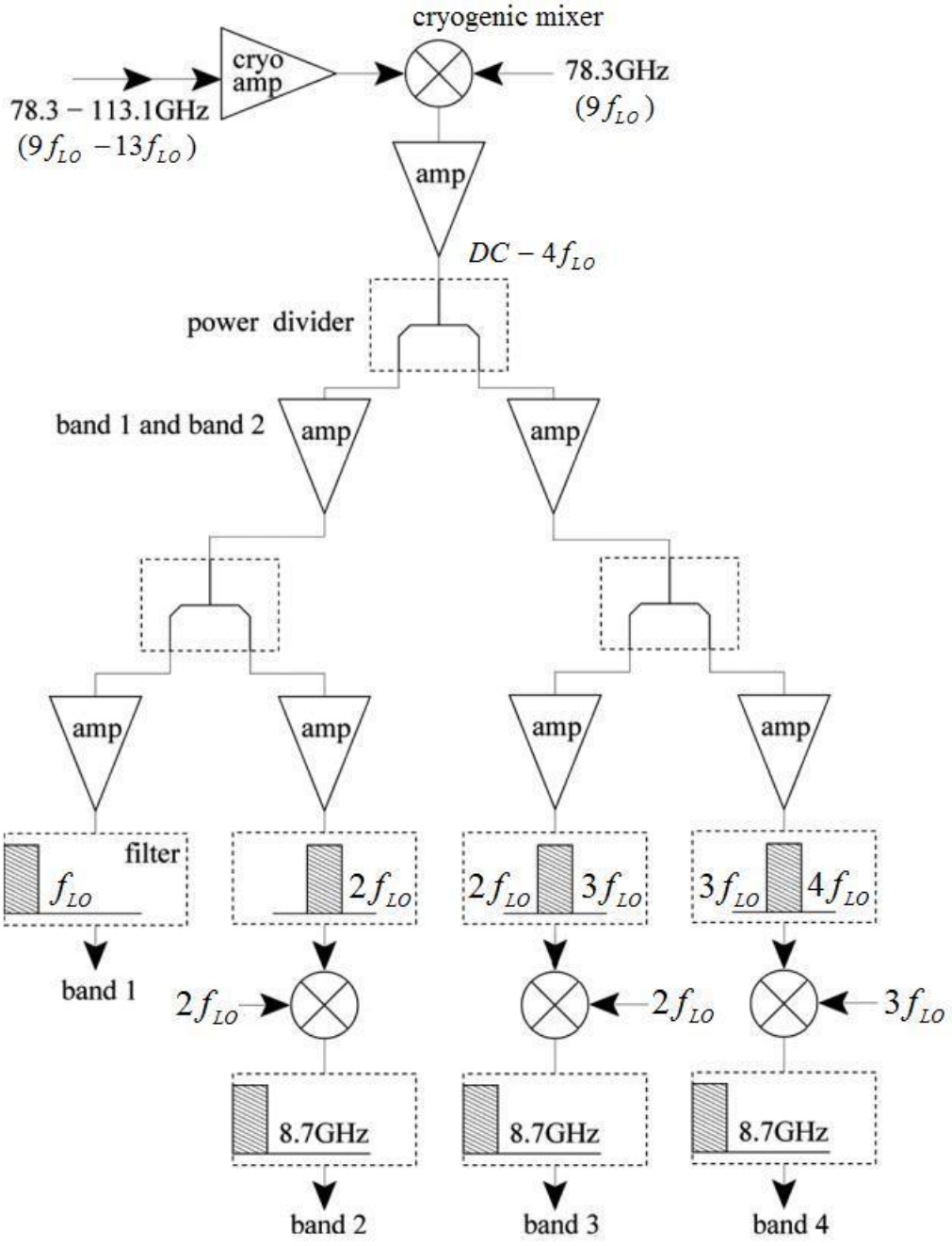

Fig. A - 3 Schematic of the wideband receiver

the rapidly decreasing impedance of this active p-type load become a liability, as it leads to a large variation of the conversion gain over the intended bandwidth: extremely high impedance at the low-end of the IF frequency range while at high-end it is mediocre or no better than that of mixers using R_L.

Fig. A - 3 is the schematic of a millimeter-wave receiver which will be used in the form of array for determination of the anisotropy of the cosmic microwave background radiation, and it demands the employment of several wide IF bandwidth mixers. The incoming signal is first fed into two cascade cryogenic amplifier modules with each has 70.90 Kelvin noise temperature and 20dB gain at 20Kelvin ambience. To ensure stability, cryogenic isolators have been incorporated into these amplifiers. The cryogenic WiseWave-FDB1001 mixer made by WiseWave Technologies (now Ducomun Technologies) is then used to down-convert, with 5.7dB conversion loss, the signal to DC - $4f_{LO}$ GHz. Of course, it is possible using a room-temperature mixer instead, but that will require the precision insertion of a hermetically-sealed millimeter-wave waveguide between the front-end cryogenic amplifier and this room-temperature mixer, and the attenuation along this long waveguide will also pronounced. Four separate bands can now be extracted by the use of amplifiers, filters, and another three mixers, each with 8.7GHz IF bandwidth and the LO frequency is fixed at 17.4GHz, 17.4GHz and 26.1GHz,respectively. The reason for not using an 8.7GHz LO for down-converting in the second band is because this LO is bordering the IF band, thus any residual LO at IF output is hard to remove; by contrast, a 17.4GHz will not have this problem.

A.2 Wide-IF-Bandwidth Mixer Design

This chapter is focus on the band 2 mixer of the proposed wideband receiver. As shown in Fig. A - 4, the proposed mixer is a fundamental mixer for lower sideband operation, and it can be divided into three parts: input RF circuit, mixing core, and output IF circuit.

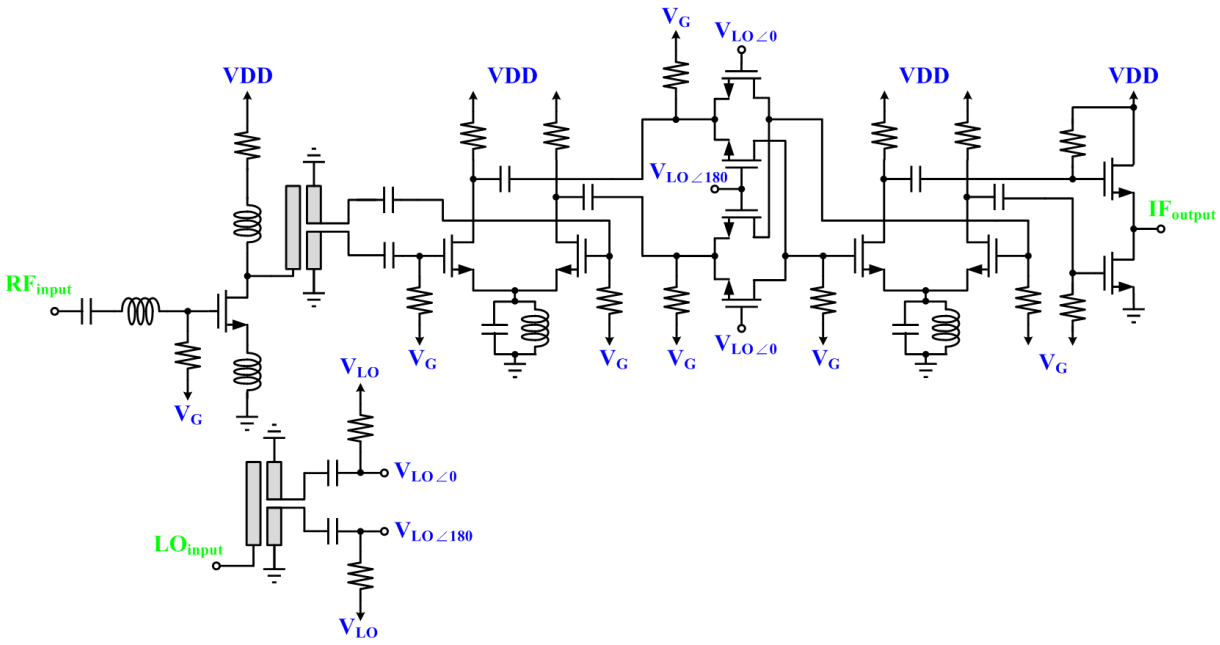

Fig. A - 4 Schematic of the wide-IF-bandwidth mixer

A.2.1 Input RF circuit

The input RF circuit starts with a inductively source-degenerated common-source amplifier, as shown in Fig. A - 5. In order to have better LO-IF isolation, the mixer will be designed in double-balanced Gilbert Cell topology, which requires differential RF signals and LO signals. While there are many circuit configurations available for converting the single-ended signal to differential signals, we adopt a distributed Marchand balun, as shown in Fig. A - 6 and Fig. A - 7, in our design [37],[38]. Distributed Marchand balun made of

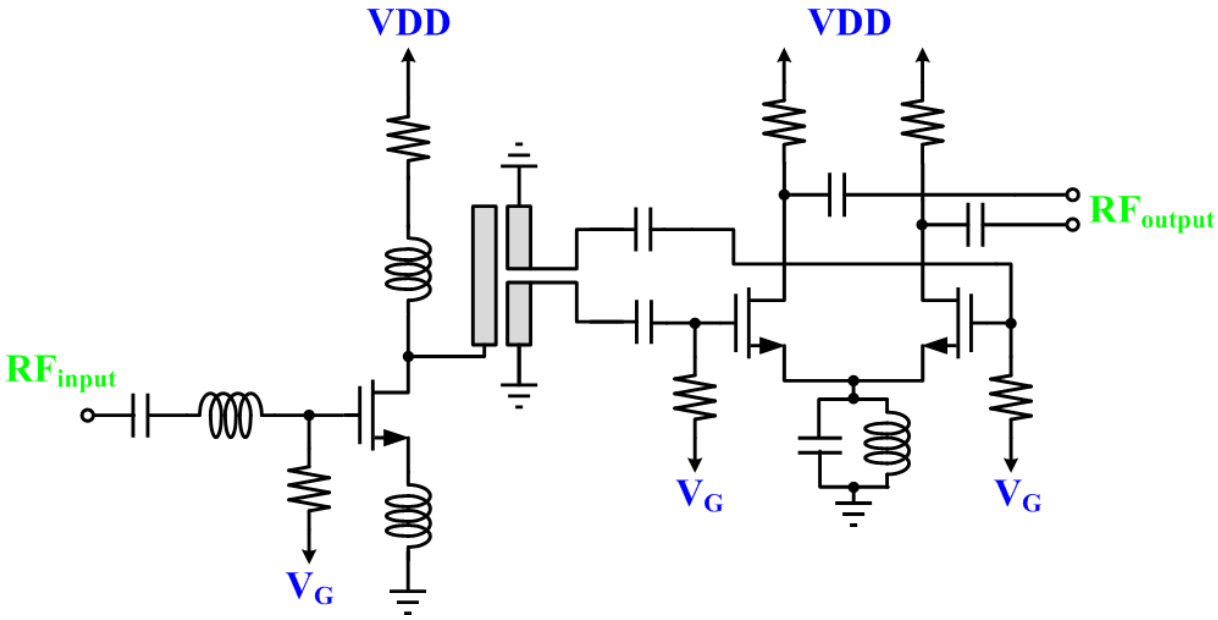

Fig. A - 5 Schematic of the input RF circuit

coupled lines has been proved application at much higher frequency [39]. Prior to the design of the Marchand balun, accuracy of electromagnetic simulation needs to be confirmed. Fig. A - 8, Fig. A - 9, Fig. A - 10 and Fig. A - 11 shows the simulated magnitude error, phase error, insertion loss and return loss of the RF Marchand balun, respectively. The proposed Marchand balun has 0.31dB of magnitude difference and 2.42 degree of phase difference.

The balanced signals out of the balun are fed to the transconductance stage. By fine-tuning the source LC of the RF differential pair, any residual common-mode signals, due to the poor out-band performance of the balun, can be suppressed while the differential-mode signal can still be amplified. That is, the transconductance stage follow by the balun has good common-mode rejection ration (CMRR) for the RF signals.

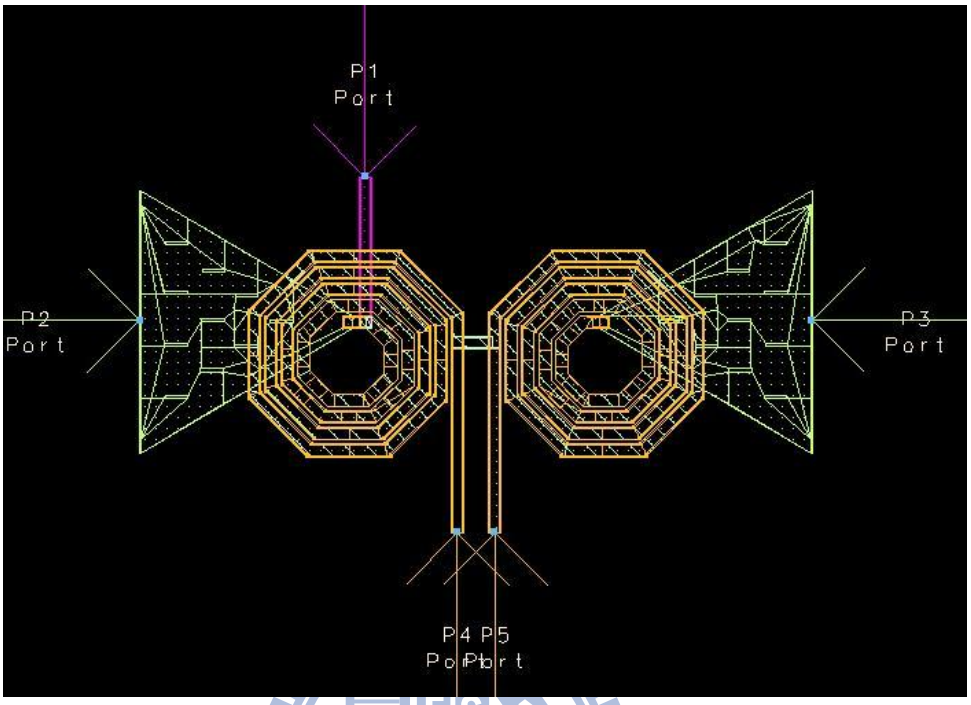

Fig. A - 6 Vertical view of the Marchand balun [37], [38]

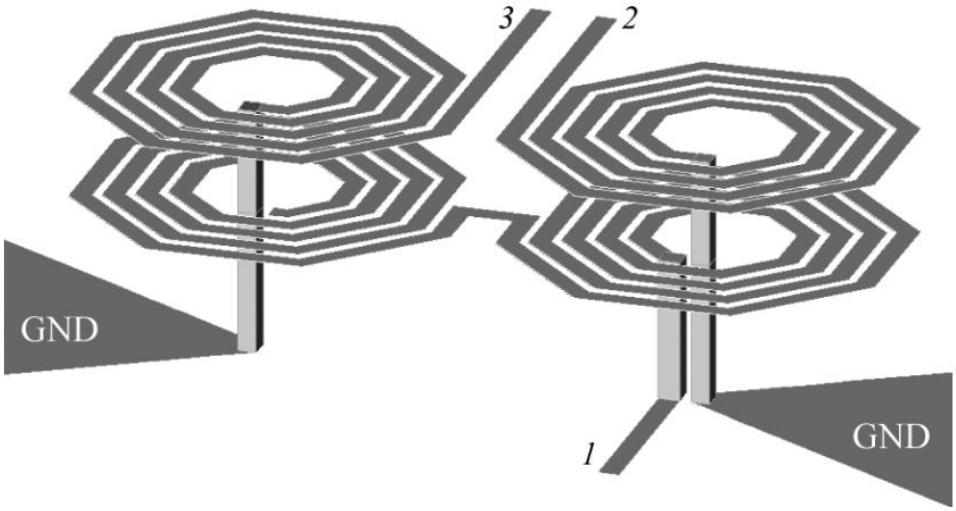

Fig. A - 7 Lateral view of the Marchand balun [37], [38]

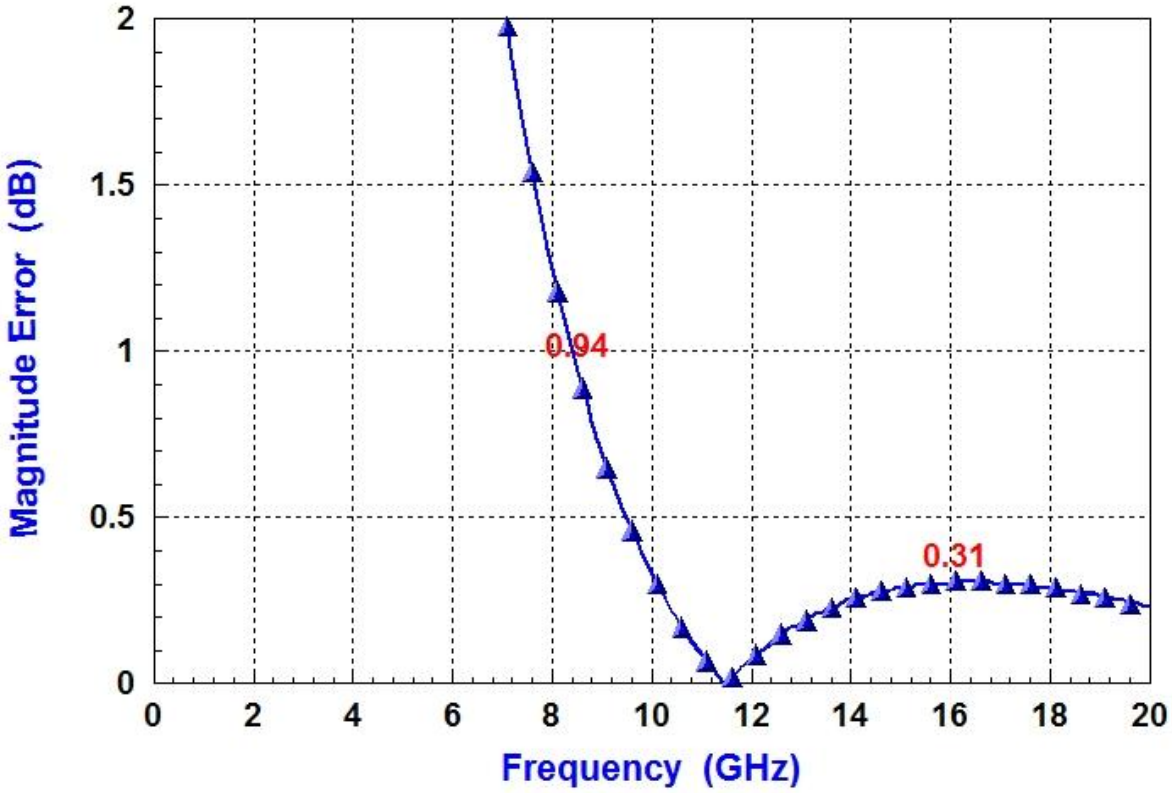

Fig. A - 8 Simulated magnitude error of the Marchand balun

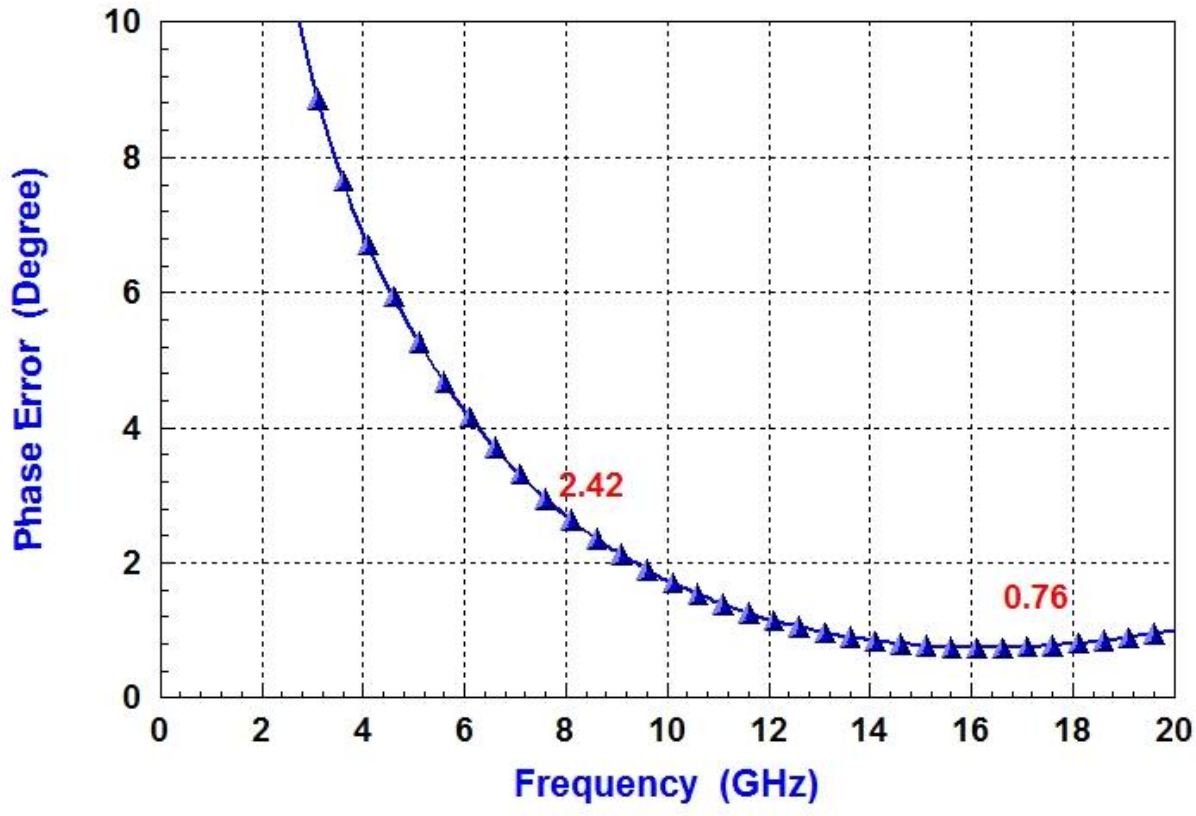

Fig. A - 9 Simulated phase error of the Marchand balun

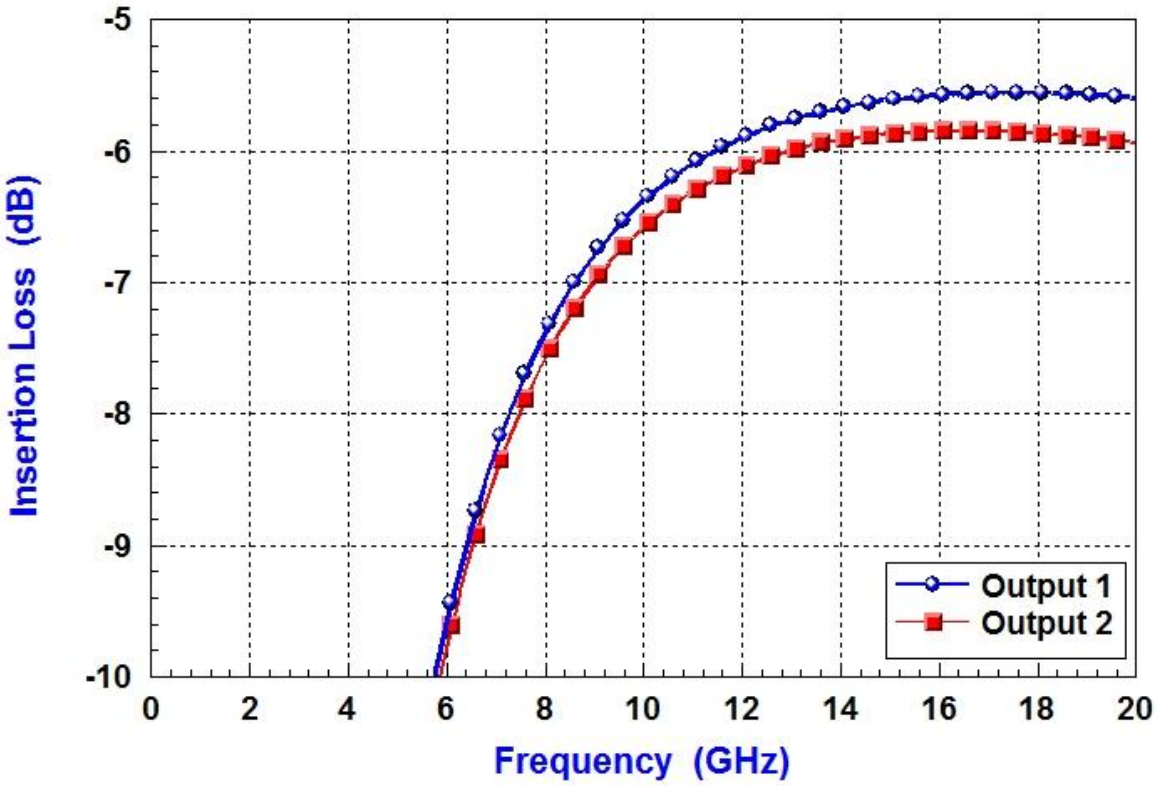

Fig. A - 10 Simulated insertion loss of the Marchand balun

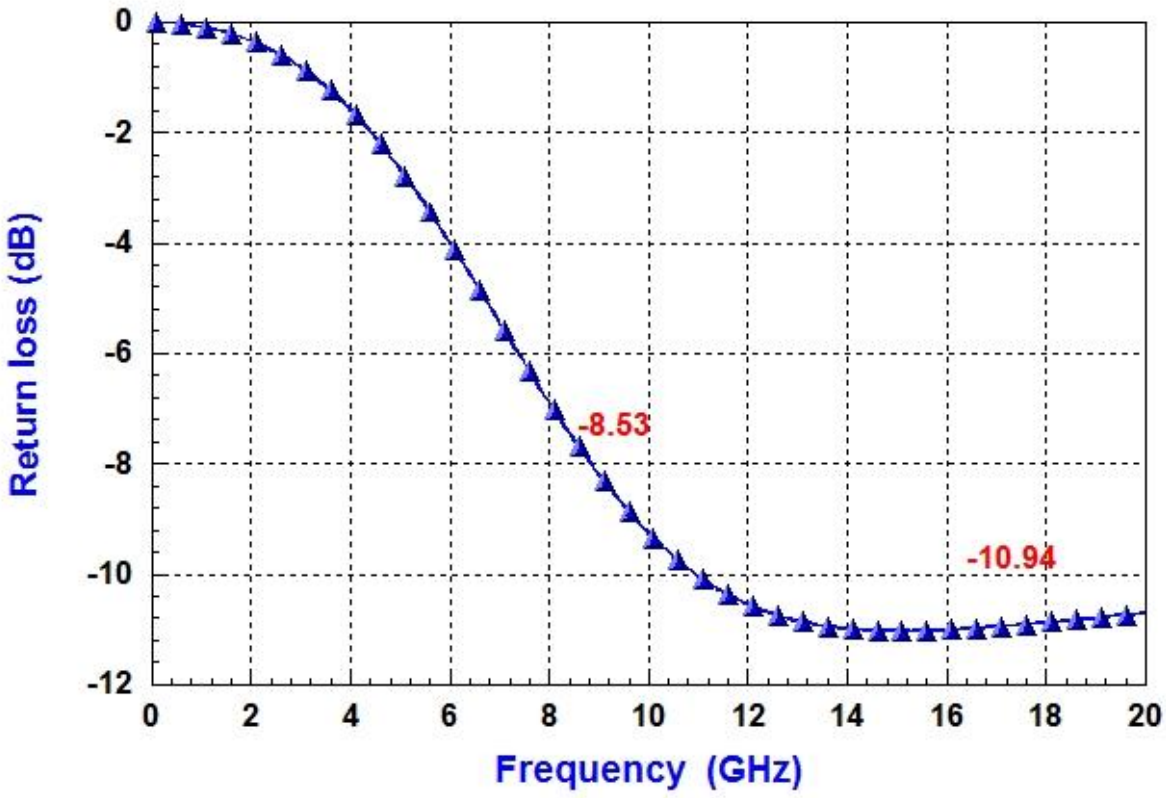

Fig. A - 11 Simulated return loss of the Marchand balun

A.2.2 Mixer core circuit

In order to achieve the high linearity purpose, the four transistors of the double-balanced Gilbert cell mixer were biased as variable resistors where the resistance is modulated by LO signal, as shown in Fig. A - 12. As a result of the less frequency-dependent property of the resistivity transistor, this mixer is expected to be wideband. Although a much larger conversion gain can be achieved by means of non-zero drain bias, it has the drawback of larger variation of conversion gain over the 8.7GHz IF bandwidth. Resistive mixer, on the other hand, tends to have more flat conversion gain.

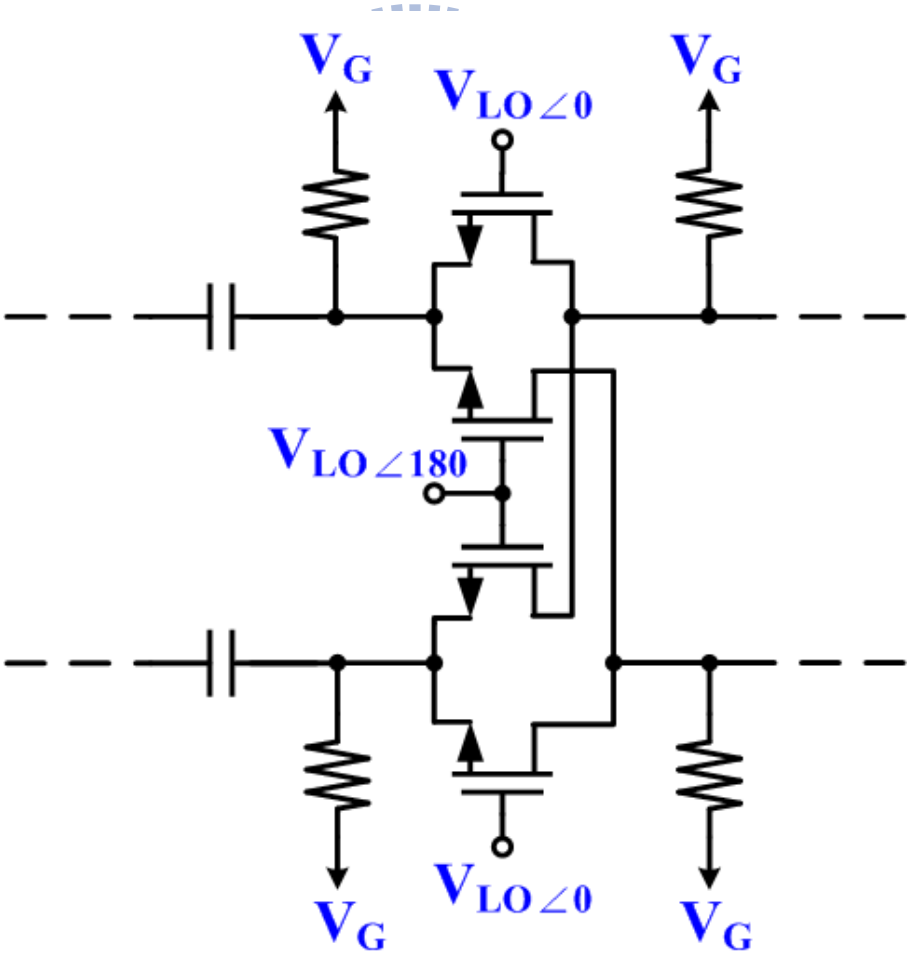

Fig. A - 12 Schematic of the mixer core

A.2.3 Output IF circuit

It goes without saying that the output IF circuit also needs to have a high common-mode rejection ratio (CMRR) over entire IF bandwidth, i.e. DC-8.7GHz. Although the distributed Marchand balun is adopted in the input RF circuit, it will occupy too much chip area for low frequency application. Consequently, we use a differential-pair followed by two n-type transistors in-cascade [35], [36], as shown in Fig. A - 13. The differential-pair with LC-tank using here not only provide the conversion gain ,but also improve the CMRR, as shown in Fig. A - 14.

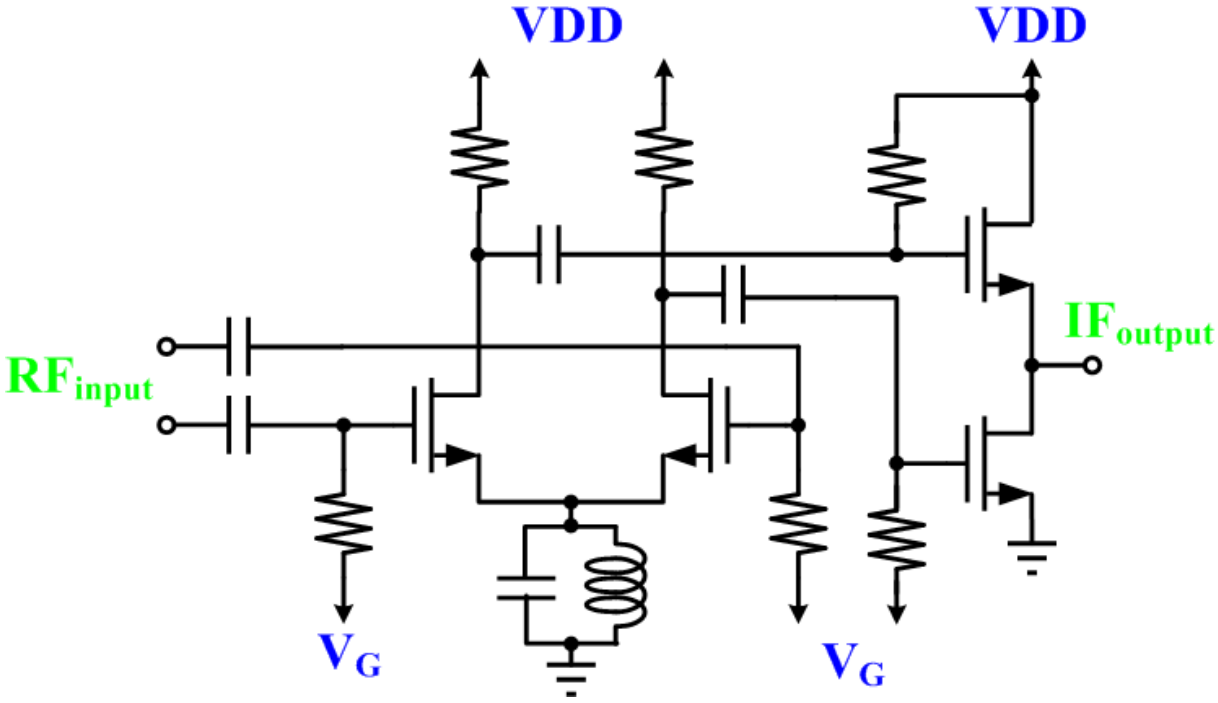

Fig. A - 13 Schematic of the output IF circuit

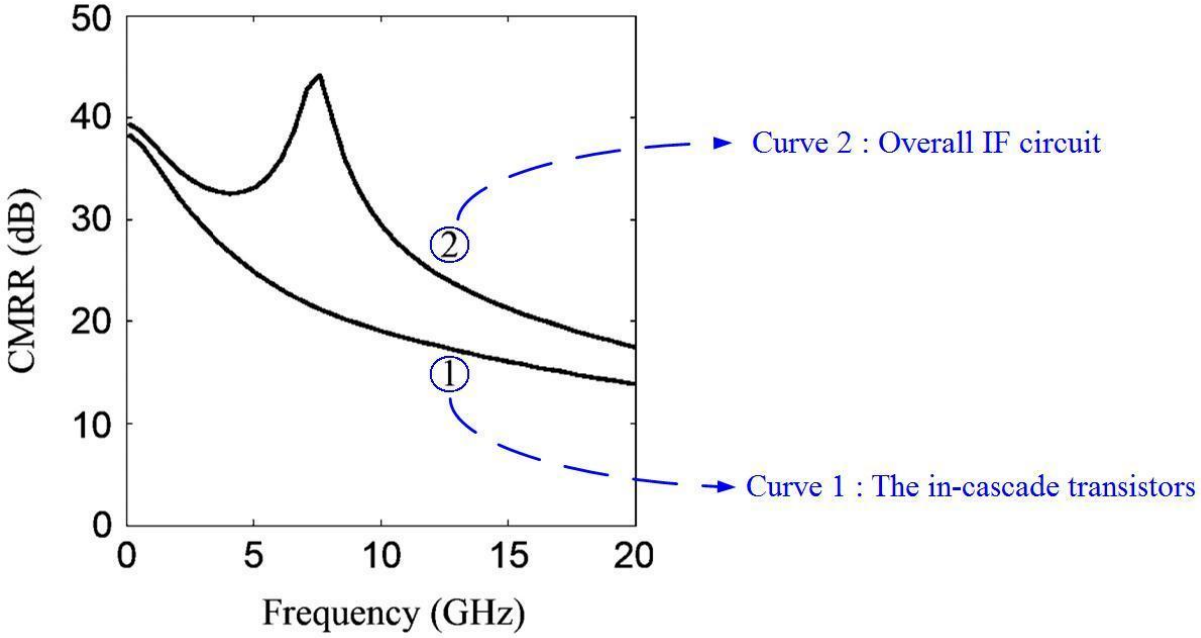

Fig. A - 14 CMRR of the output IF circuit

A.3 Simulation and Measurement Results

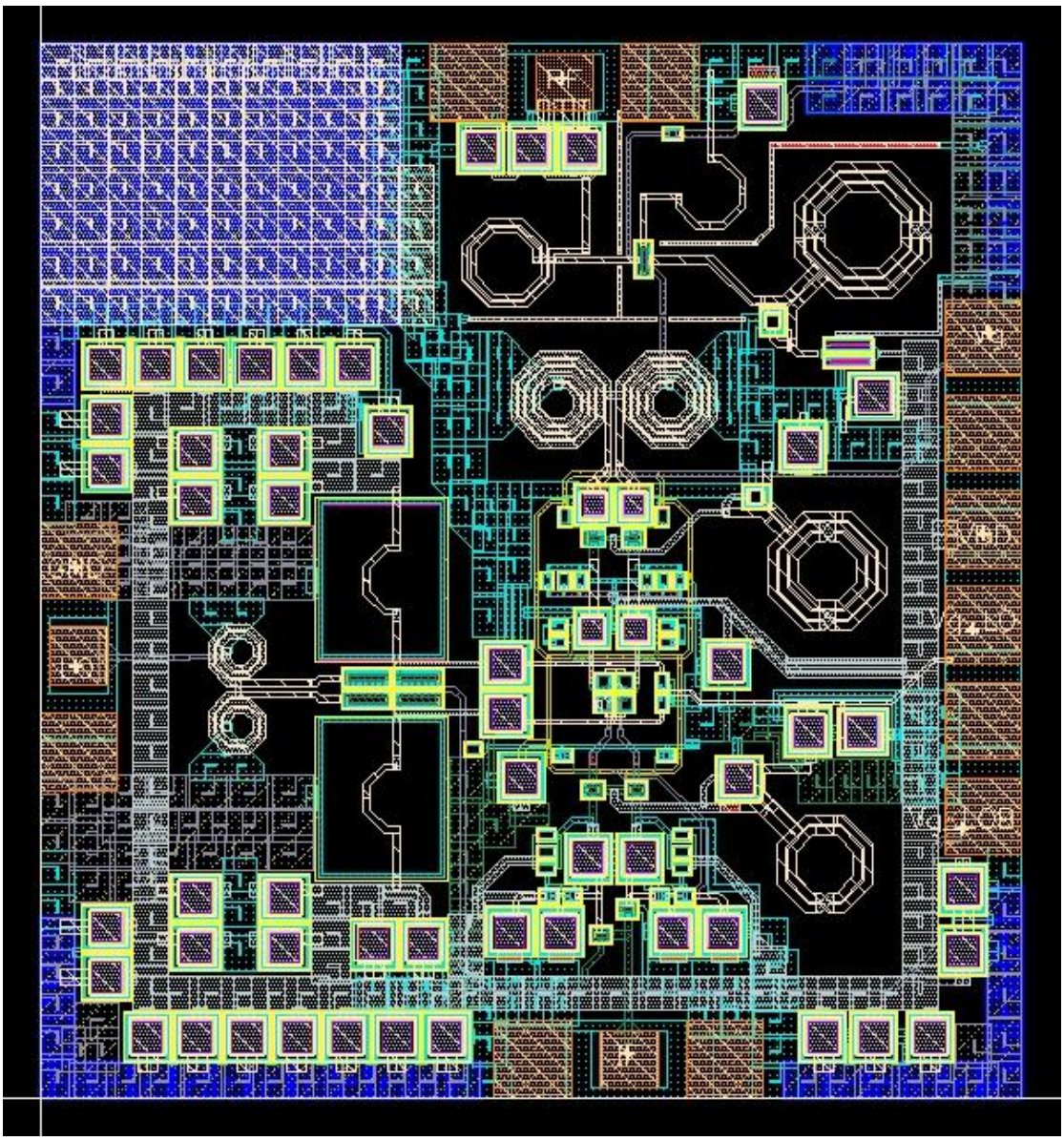

Fig. A - 15 Chip layout of the proposed wide-IF band mixer

Fig. A - 15 shows the chip layout photograph of the proposed wide-IF band mixer, which is designed and implemented in TSMC 0.18μm mixed-signal/RF CMOS 1P6M technology. The chip size is 1.023 × 1.100 mm^2 including all pads and bypass capacitances. The power consumption is 33.5mW. Fig. A - 16 is the chip photograph of the proposed wide-IF band

mixer. We deliver on-wafer measurement in National Chip Implementation Center (CIC), which provides probe stations, network analyzers (HP8510C), spectrum analyzers (Agilent E4407B), signal generators, and power supplies. Fig. A - 17 and Fig. A - 18 shows the arrangement of DC and RF probes, one 6-pin DC probe and three 3-pin RF probes with pitch 100μm.

As shown in Fig. A - 20, the simulated and measured RF port return loss are below -8 dB in 8.7-17.4 GHz. The simulated and measured IF port return loss are less than -17 dB in

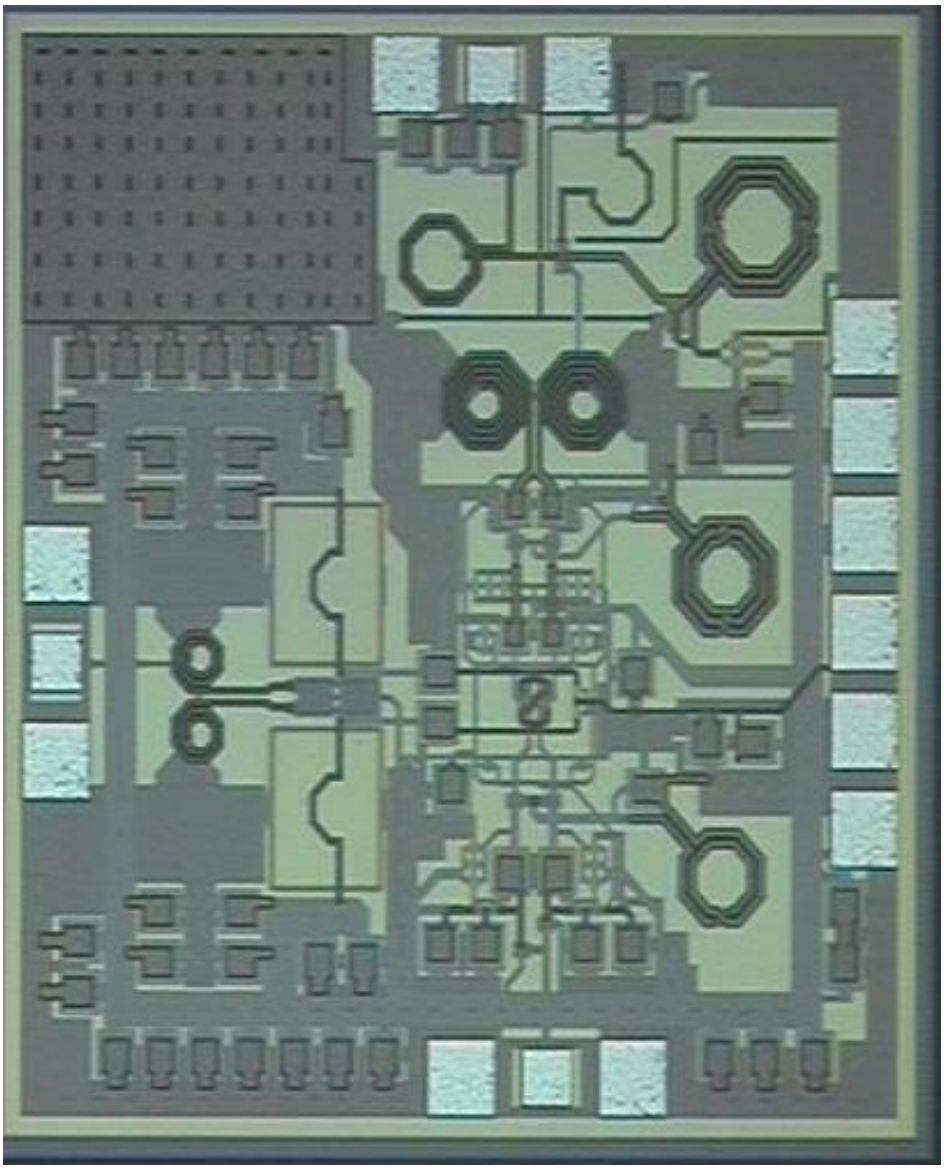

Fig. A - 16 Chip photo of the proposed wide-IF band mixer

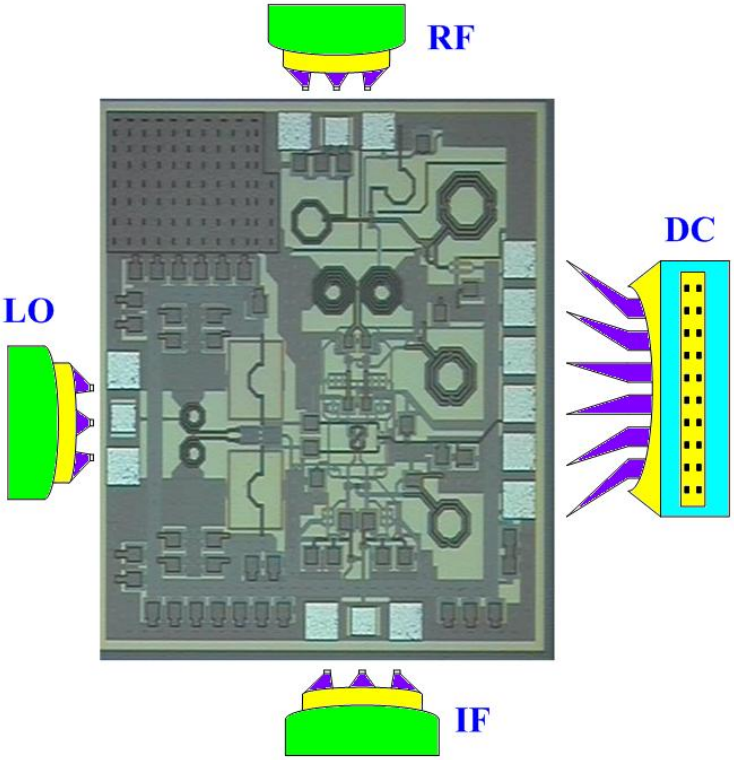

Fig. A - 17 Arrangement of DC and RF probes

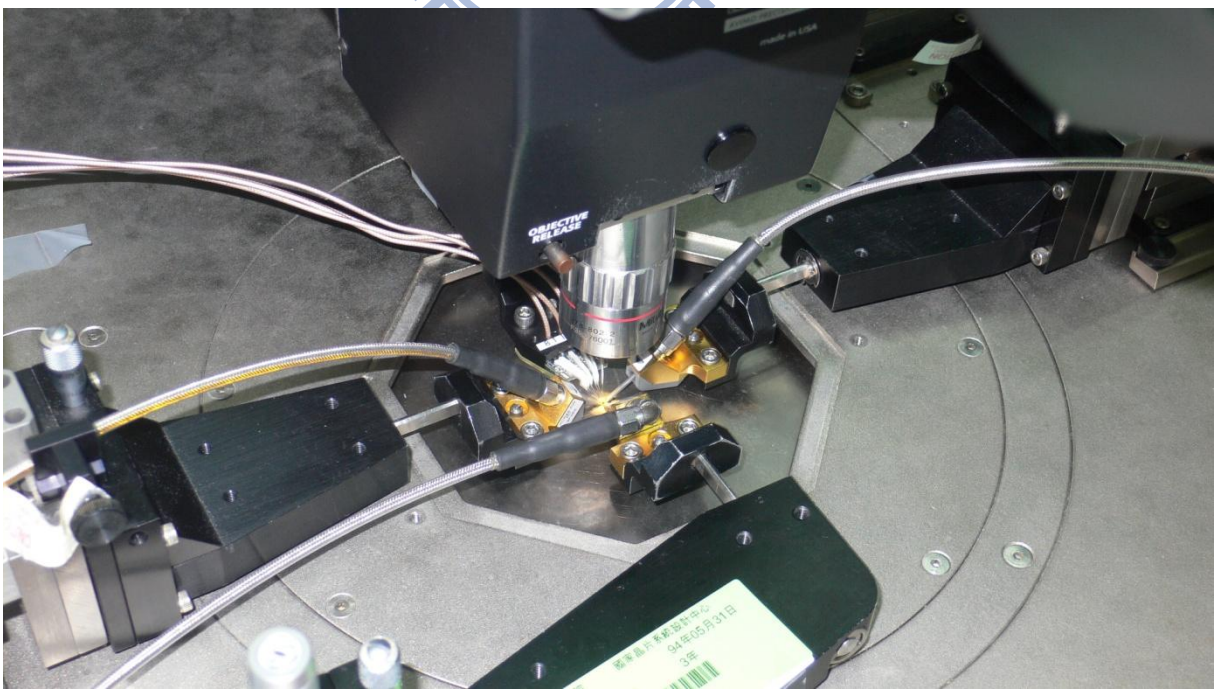

Fig. A - 18 Photograph of the probe station

DC-8.7 GHz, as shown in Fig. A - 21.

Fig. A - 22 shows the simulated and measured conversion gain. The simulated result exhibits an average 8 dB conversion gain, and gain variation less than 2 dB within the intended RF bandwidth. Due to the poor input matching, the conversion gain will degrade 2-3 dB. The measured conversion gain decrease 3 dB at the higher end and 5 dB at the lower end of RF bandwidth. The comparison of simulated and measured results is shown in Table A - 1.

The discrepancy between them appears on the conversion gain, and we consider that it is due to the performance decay of the Marchand balun mainly cause by the unsymmetric grounding path.

Fig. A - 19 Photograph of the measurement environment in Chip Implementation Center

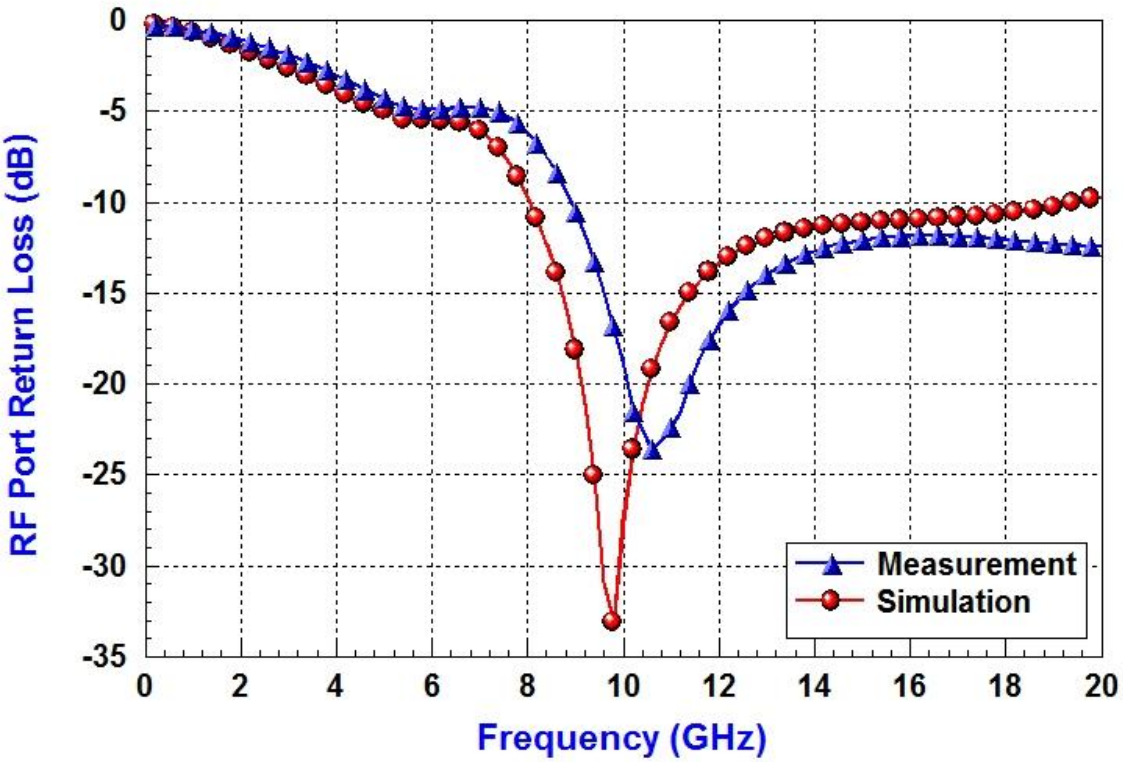

Fig. A - 20 RF port return loss for RF signal from 8.7-17.4 GHz

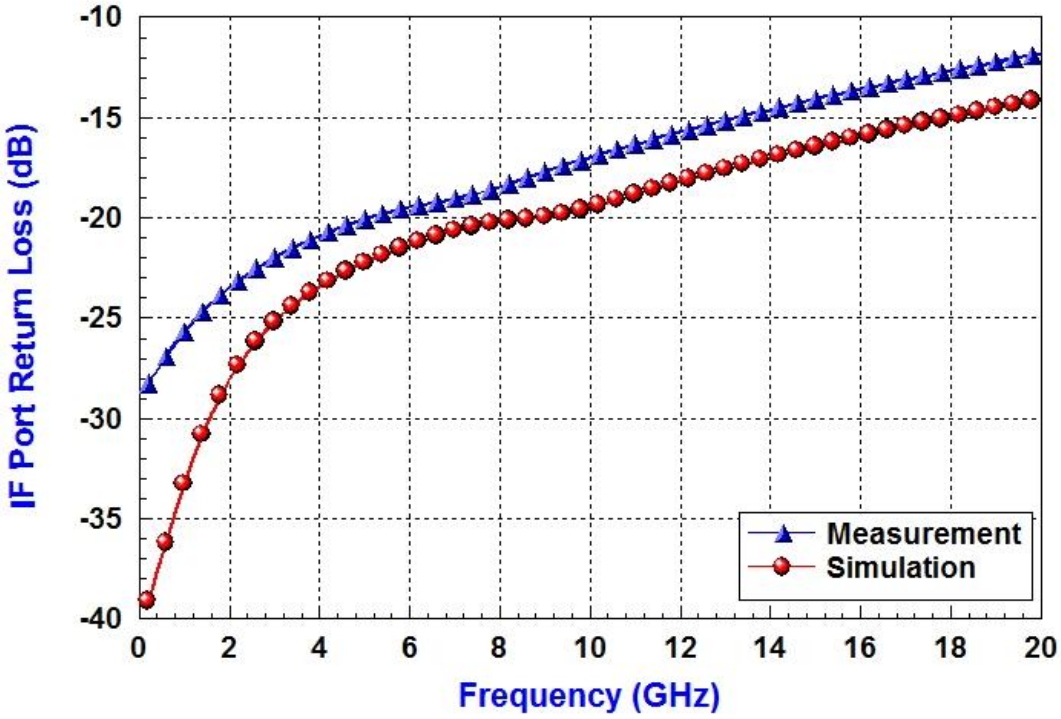

Fig. A - 21 IF port return loss for IF equals to DC-8.7 GHz

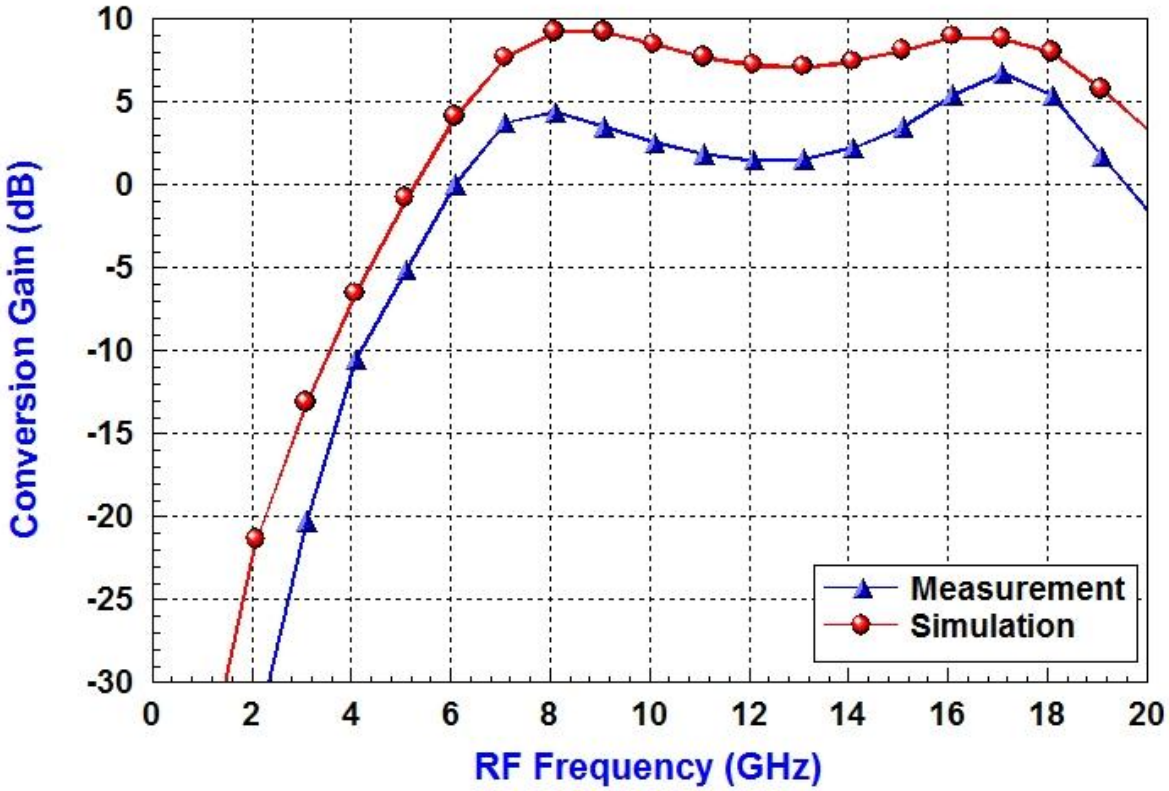

Fig. A - 22 Conversion gain versus RF frequency with LO fixed at 17.4 GHz

Table A - 1 Comparison of the simulated and measurement results

	Simulation	Measurement
Technology	0.18μm CMOS	0.18μm CMOS
RF Bandwidth	8.7 - 17.4 GHz	8.7 - 17.4 GHz
IF Bandwidth	DC - 8.7 GHz	DC - 8.7 GHz
RF input Return Loss	< -10 dB	< - 8 dB
IF input Return Loss	< -20 dB	< - 17 dB
Supply Voltage	1.8 V	1.8 V
Power Dissipation	31mW	33.5mW

A.4 Conclusion and Future Work

In order to reduce the difficulty in designing the corresponding LO module, another mixer with the integrated LO frequency doubler has also been proposed. The schematic of the frequency doubler is shown in Fig. A - 23. We also incorporate a constant-g_m bias circuit, as shown in Fig. A - 24, to generate the biasing voltage. The chip layout of the proposed wide-IF band mixer with LO-doubler is shown in Fig. A - 25. The chip size is 1.400 × 1.100 mm^2 including all pads and bypass capacitances.

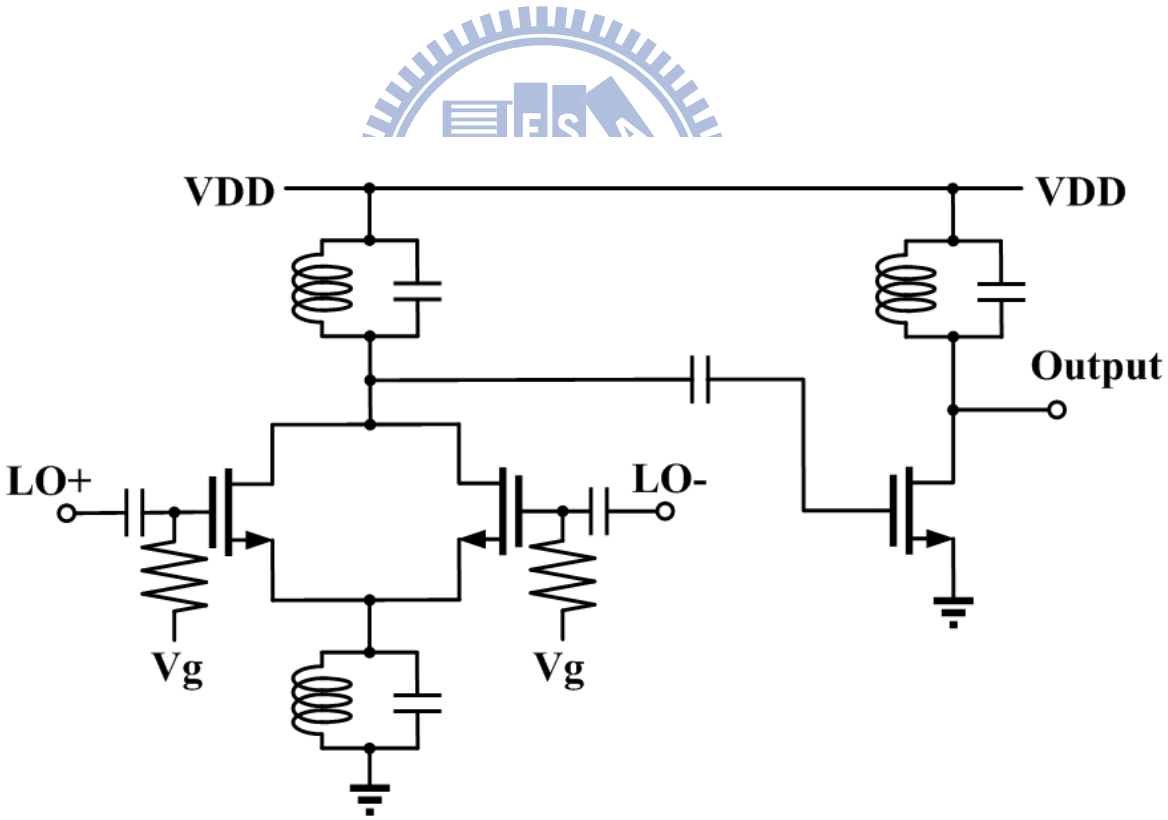

Fig. A - 23 Schematic of the frequency doubler

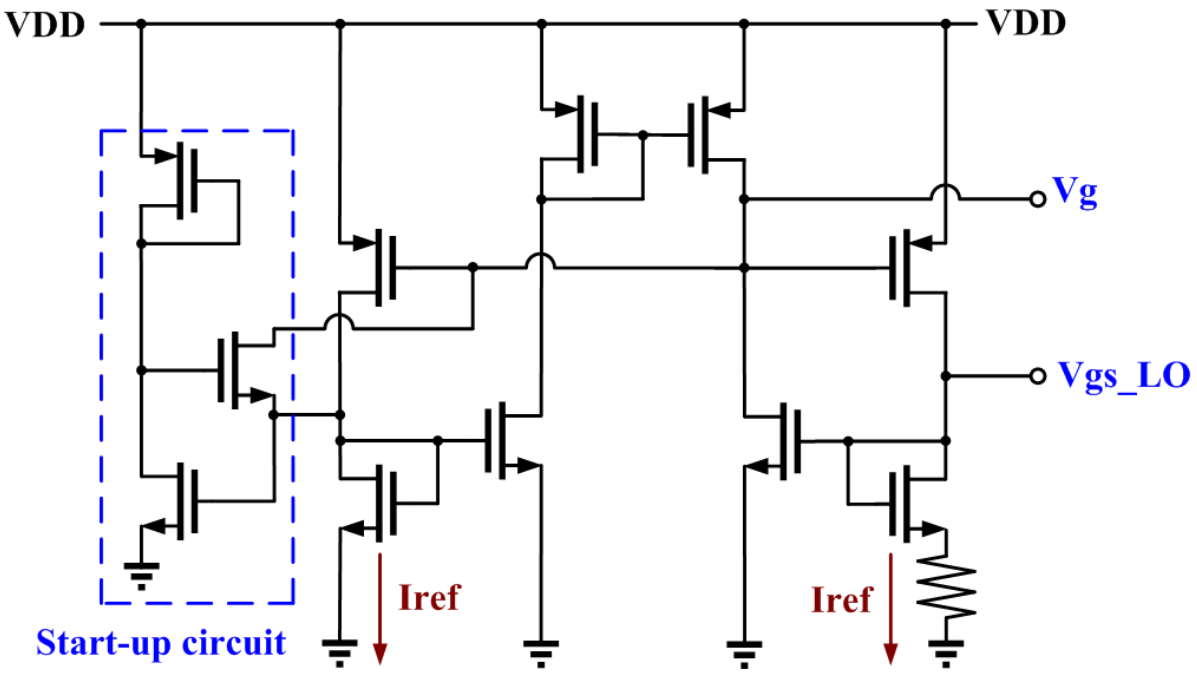

Fig. A - 24 Schematic of the constant-g_m bias circuit

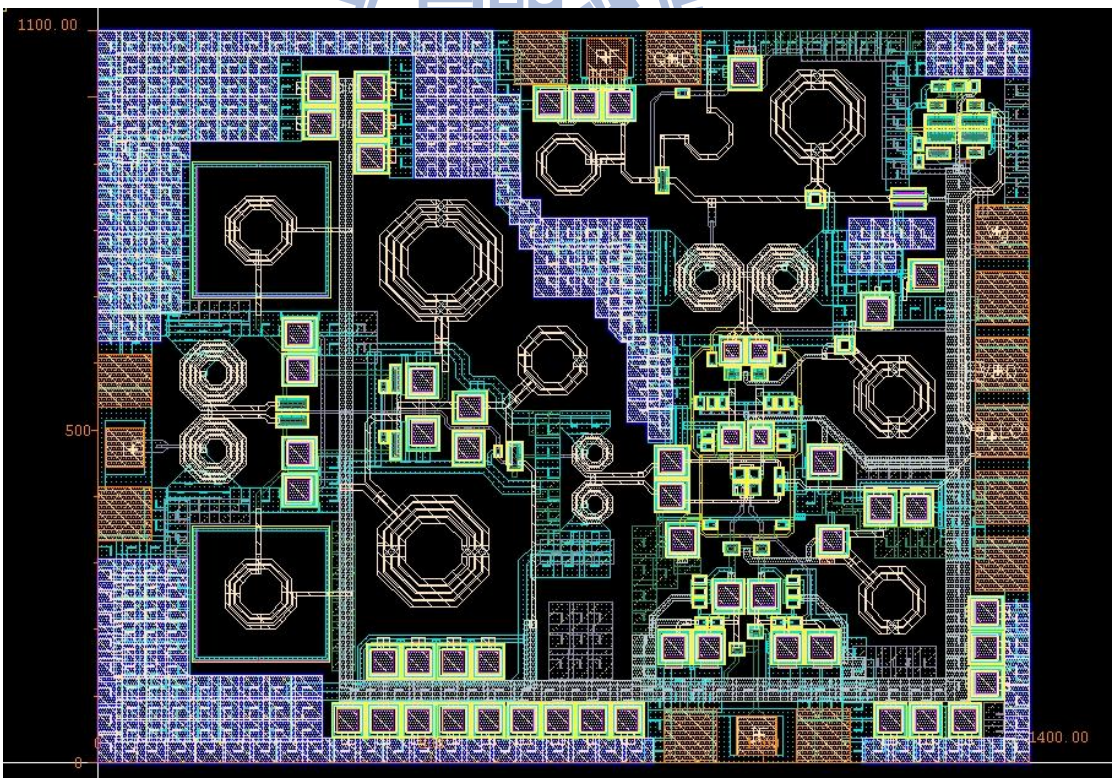

Fig. A - 25 Chip Layout of the proposed wide-IF band mixer with LO frequency doubler

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