國 立 交 通 大 學

電信工程研究所

碩 士 論 文

隨機金屬閘極功函數導致之16奈米金氧半場效應電晶體元件及電路特性擾動之研究

Random-Metal-Gate-Work-Function-Induced Electrical Characteristic Fluctuation in 16-nm-Gate CMOS Devices and Circuits

研 究 生：韓銘鴻

指導教授：李義明 教授

中 華 民 國 九十九 年 八 月


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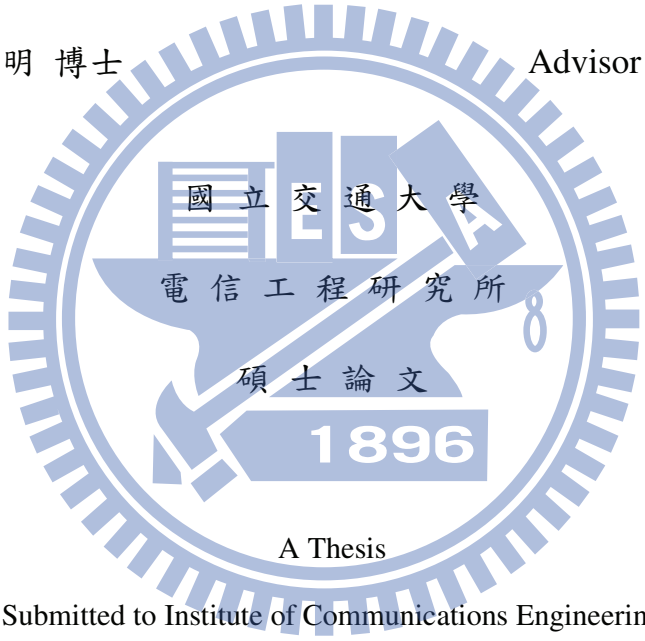

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摘　　要

金屬閘極與高介電係數閘極絕緣材料的使用使得摩爾定律能夠延續，且已成為奈米電晶體元件開發不可或缺之重要技術。然而在製程上，金屬材料在結晶的過程中，晶格顆粒的大小與方向為一個隨機的過程，又由於金屬晶格排列的不同造成金屬表面原子數量及電偶極強度的不同，造成不同的晶格排列會有不同的表面電位，進而影響金屬的功函數值，此一功函數值的不固定，將帶來新的擾動來源。為了探討此一擾動來源的重要性以及對於奈米元件與電路特性的影響，有別於文獻中提出的有效功函數擾動分析法，本論文應用蒙地卡羅方法三維度電晶體元件模擬方式，首先將閘極金屬細分成許多的小塊，再依照不同晶格出現的機率，分別隨機地給予每一小塊相對應的功函數值，藉此模擬出閘極金屬表面晶格隨機排列的現象，並藉此廣泛的分析金屬閘極功函數擾動對於 16 奈米金屬閘極金氧半場效電晶體特性暨其電路之影響。

在元件特性擾動方面，本論文分析了金屬閘極功函數擾動對於元件臨界電壓，閘極電容，以及截止頻率的特性擾動，並探討了其物理機制，模擬結果發現其對於元件臨界電壓造成不可忽略的影響，研究發現不同的金屬晶格排列的大小，數量，以及位置的不同，會造成臨界電壓值的擾動，此現象藉由通道表面的電位，電荷，以及能帶的分布得以解釋。在元件閘極電容以及截止頻率的特性分析上，研究發現金屬閘極功函數擾動只會在弱反轉區造成較大的擾動，在聚集區以及強反轉區的情形下，此一擾動將會因表面電荷集中造成的屏蔽效應而被壓抑。

在電路特性擾動方面，本論文探討了金屬閘極功函數擾動對於數位電路以及類比電路的影響，在反相器電路中，發現功函數擾動對於其延遲時間以及功率消耗均有相當的特性擾動影響，其中在功率消耗中，靜態功率消耗並不

是主要的功率消耗來源，但是其擾動卻是十分重要且需要考量的一項，另外，功函數擾動對於靜態隨機存取記憶體電路的靜態雜訊容限以及電流鏡電路的電流匹配均會造成嚴重特性擾動，但在高頻電路的應用中，因屏蔽效應的關係，功函數擾動對高頻動態特性卻不會造成明顯的影響，以上的研究對於電路設計及其最佳化，均有相當的助益。

總之，本論文已分析了金屬閘極功函數對於電晶體的影響，並探討了形成的原因及分析其背後的物理機制與影響。此論文結果對於電晶體擾動壓抑之推估以及下世代電晶體特性擾動分析極有貢獻。

Abstract (in English)

High-κ/metal gate technology has been recently recognized as the key to sub-45-nanometer transistor fabrication because of the improvement of device performance and reduction of intrinsic parameter fluctuation. However, the use of metal as the gate material introduced a new source of variation. Recently, the averaged work-function fluctuation method was reported to estimate the fluctuation; however, the effective work-function may over- or under- estimate the variability. This thesis computationally study the work-function fluctuation on emerging high-κ/metal gate devices and investigate such variation source induced characteristic fluctuation using experimental validated three-dimension device simulation. In our simulation methodology, we directly partition the device gate metal material into many sub-regions according to the measurement averaged grain size, and then we randomly generate the work-function to each sub-region according to the material properties and map them into device gate for our device simulation. Both the device and circuit characteristic fluctuation are investigated.

For device characteristics, the fluctuations of threshold voltage (V_{th}), gate capacitance (C_G), cutoff frequency (f_T) of complementary metal-oxide-semiconductor (CMOS) field effect transistor (FET) devices are comprehensively analyzed. The result show that WKF will induce significant V_{th} fluctuation (σV_{th}) which can not be neglected. However, the impacts of WKF on device AC (C_G and f_T) fluctuations are reduced at zero and high gate voltage due to the screening effect of inversion layer or accumulation layer of device.

The implications of device variability in nanoscale transistor circuits are also advanced. The digital circuit (CMOS inverter and static random access memory (SRAM)) and analog circuit (common source amplifier and current mirror) are examined. In CMOS inverter circuit, the fluctuations of rise time, fall time, and delay time fluctuations follow the trend of V_{th} fluctuation. The power fluctuations consisting of dynamic power, short circuit power, and static power are estimated. The dynamic power and short circuit power are the most important power dissipation sources. However, the static power fluctuation dominates the total power fluctuation due to the exponential relationship between the leakage current and the V_{th}. For SRAM, static noise margin fluctuations are explored and the WKF bring significant variations. For current mirror, the circuit performance variability caused by device mismatch is also clearly shown. However, in common source amplifier, the WKF shows less impact on high frequency characteristic owing to the small gate capacitance fluctuation. It is necessary to include the WKF effects in studying digital circuit reliability; however,

for high frequency applications, the influence of WKF could be neglected.

In summary, we have studied the random work-function fluctuations on nano-CMOS devices and circuits variability. The result of this study is useful for the next generation CMOS circuits and systems.


E S A
1896

誌　　謝

隨著本論文的完成，在電信工程研究所的求學生活，也即將告一個段落，心中除了高興，最重要的是能夠在這短短的兩年，學到如何的學習，解決問題的方法，以及了解學無止盡，這不是一個終點，而僅僅是人生的一個過程，而這一切都要感謝許多人的教導、支持與鼓勵。

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中華民國九十九年八月

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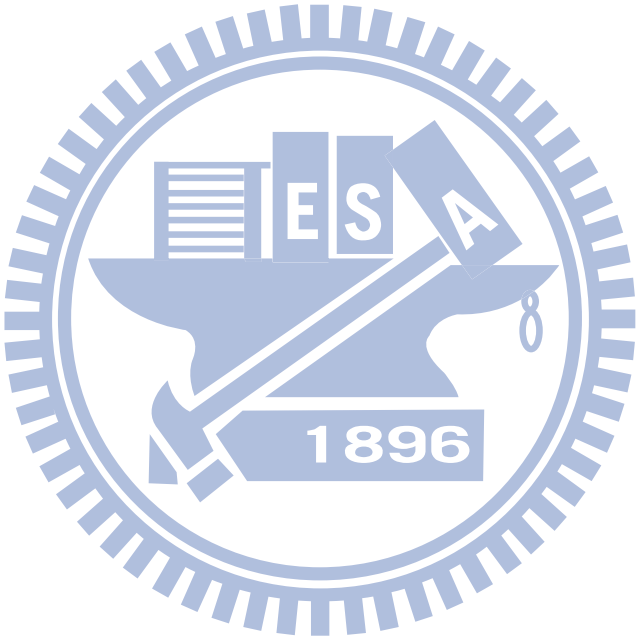
平行與科學計算實驗室


E S A
1896

Contents

List of Figures

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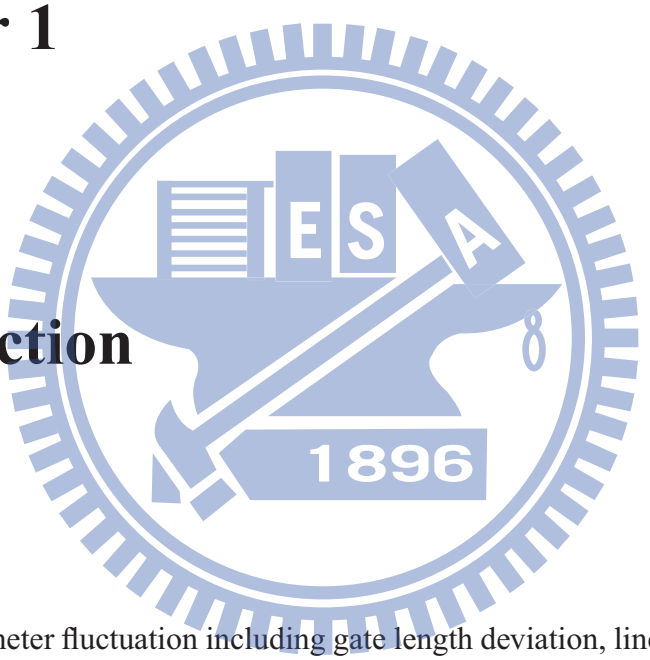
Chapter 1

Introduction



Intrinsic parameter fluctuation including gate length deviation, line edge roughness, and random dopant fluctuation is a critical issues for nanosclae device. Although the use of high-κ/metal gate is one of important device technology to deal with the aforementioned problem, the metal material introduces a new source of variation, the so-called metal work-function fluctuation (WKF). In this chapter, we first point out some interesting research topics of WKF, then present the background and review recent reports on WKF. Then, we state the purpose of this study. Finally, we outline the whole thesis.

1.1 Motivation

Evolution of complementary metal-oxide-semiconductor (CMOS) field effect transistor (FET) technology in the past 40 years has followed the path of device scaling for achieving density, speed and power improvements [1-6]. However, the fluctuation is intrinsically increased with the scaling of transistor feature size, Fig. 1.1 shows the major sources of intrinsic parameter fluctuations, including the gate length deviation [30,31,37-45], line edge roughness [30,31,37-45], and random dopant fluctuation [7-45]. High-κ/metal gate technology has been recently recognized as the key technology to nanometer transistor, Fig. 1.2 illustrates the use of high-κ/metal gate to suppress the intrinsic parameter fluctuation along the CMOS devices scaling [23]. However, the use of metal as the gate material introduced a new source of variation due to the dependency of metal work-function on the orientation of the metal grains [46-53]. It is crucial to estimated such variation induces devices and circuits characteristic fluctuations.

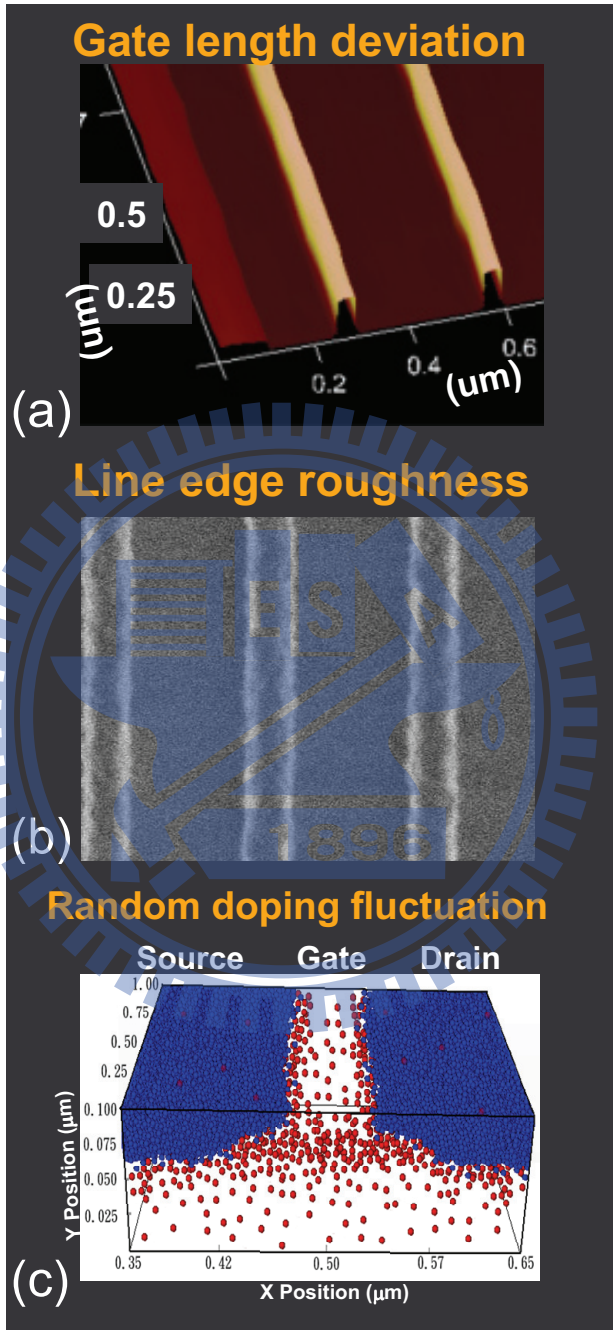


Figure 1.1: The major sources of intrinsic parameter fluctuations: (a) the gate length deviation, (b) line edge roughness, and (c) random dopant fluctuation. The gate length deviation and line edge roughness are form the variation of lithography technology [30,31,37-45]. The random dopant fluctuation comes from the ion-implantation, diffusion and thermal annealing [7-45].

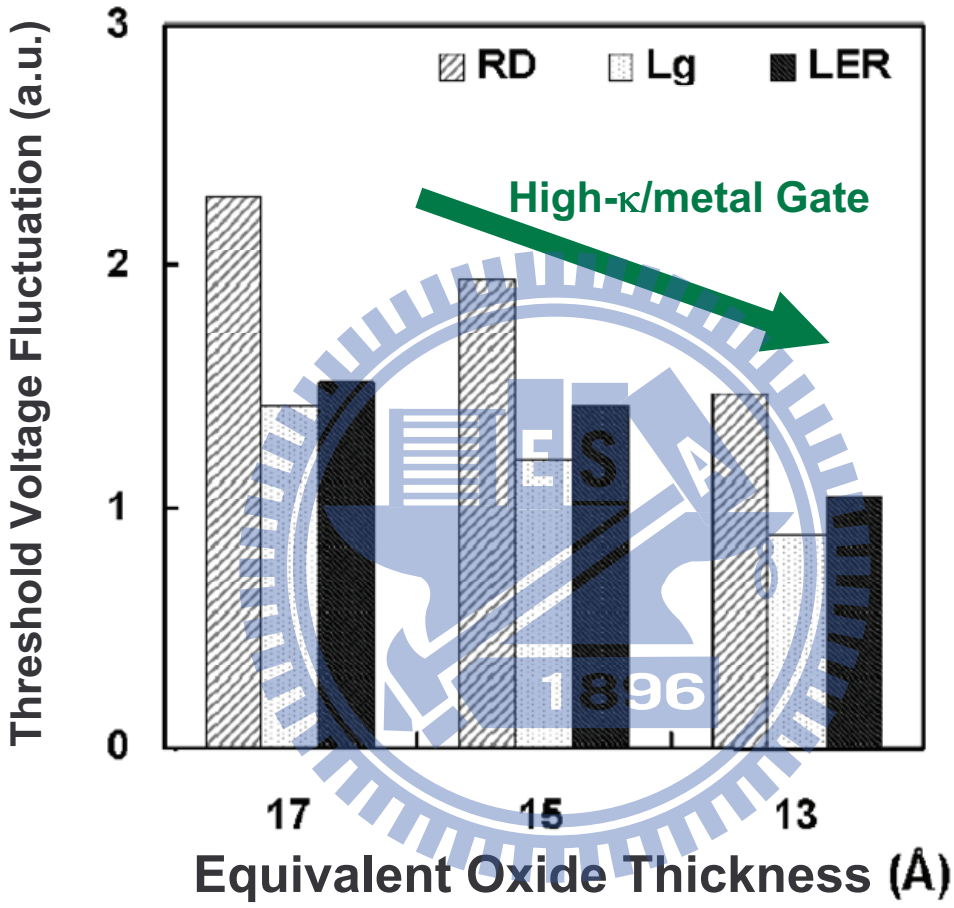


Figure 1.2: The intrinsic parameter fluctuation induced threshold voltage fluctuation versus equivalent oxide thickness, the threshold voltage fluctuation can be reduced using high-κ/metal gate technologies [23].

1.2 The Background and Literature Review

It is known that metal grains usually grow up to few nanometers in size under temperatures used in IC fabrication. The crystal orientation of nanosized metal grain is uncontrollable during growth period, the use of metal as gate material will introduce work-function fluctuation [46-53]. Figure 1.3(a) shows the scanning electron microscope (SEM) pictures of titanium nitride (TiN) [50], which containing numbers of grain with various grain orientation. TiN is a sodium chloride (NaCl) structure compound consisting of Ti atoms filled in FCC-based lattice with all octahedral sites filled with nitrogen atoms, as shown in Fig. 1.3(b). Since the different grain orientation has its own strength of dipoles, the work-function in each grain orientation is different, as shown in Fig. 1.3(c). The device's threshold voltage will become a probabilistic distribution rather than a deterministic value.

Additionally, the WKF induced characteristic fluctuations are one of major variation source in emerging high-κ/metal gate technology compare with the existance of random dopant fluctuation (RDF) and process variation effect (PVE) [46-53]. However, the simulation using a modified averaged work-function fluctuation method (the details will be examined in the next chapter), which may misestimate the WKF induced device/circuit fluctuations. Although the appearance were also found by other literature [51], they used a compact model method [54], which also could not accurately describe nanoscale grain orientation due to no well established compact model for such small transistor.

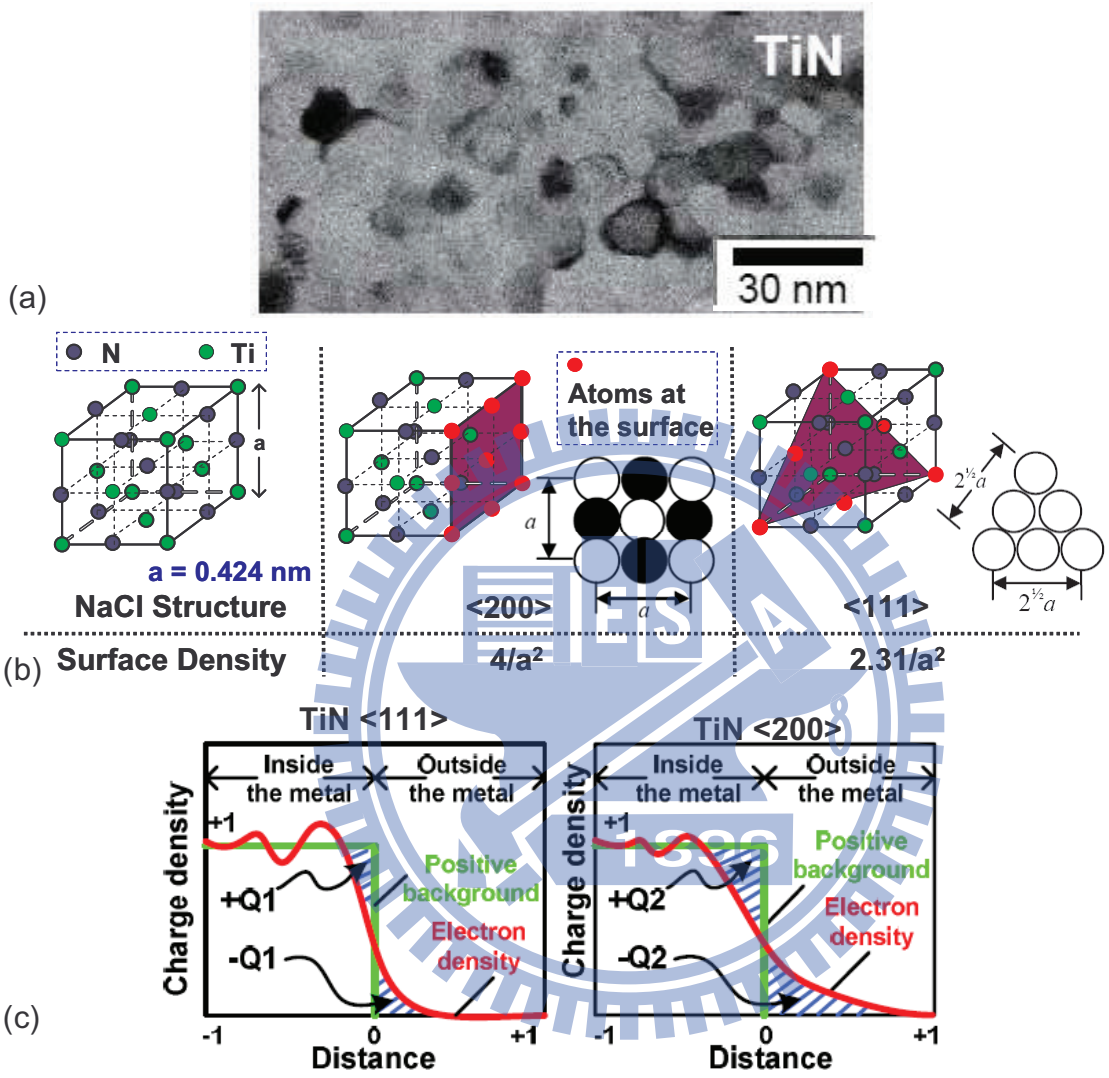


Figure 1.3: (a) The SEM pictures and illustration of TiN surface [50], which containing numbers of grain with various grain orientation. (b) An illustration of crystal structure with <200>, and <111> orientation. (c) Each grain orientation has its own strength of dipoles and therefore different work-function [48,49]. Therefore, the combination of device work-function will become a probabilistic distribution rather than a deterministic value.

1.3 The Study of this Thesis

To deal with the aforementioned problems, this work thus highlights the work-function fluctuation on emerging high-κ/metal gate technology on nano CMOS devices and circuits by experimentally calibrated three dimensional (3D) device simulation [23], called 3D localized work-function fluctuation method. The impact of work-function fluctuation on the device's DC / AC fluctuation are first investigated, and the physical mechanism are discussed. For the device characteristic fluctuations, the localized work-function fluctuation approach has its advantage to capture not only the number of different metal grain orientation but also the grain placement induced device variability. To accurately characterize the device variability in circuits, the circuit characteristic fluctuations are obtained by solving the both device transport and circuit nodal equations called coupled device-circuit simulation [55-67]. Unlike the compact model simulation approach, the coupled device-circuit simulation approaches solves the device transport characteristics in circuit simulation and therefore provide the most device physics inside circuit fluctuation. The extensive study assesses the fluctuations on circuit characteristics, which can in turn be used to optimize nanoscale MOSFET devices and circuits.

1.4 Outline

This thesis is organized as follows. Chapter 2 introduces the various simulation methods for studying the effect of metal gate work-function fluctuation. The averaged work-function fluctuation method [48,49], our modified averaged work-function fluctuation method, and experimentally calibrated 3D localized work-function fluctuation device simulation are stated. Chapter 3 compares the modified averaged work-function fluctuation and localized work-function fluctuation methods induced device DC and AC characteristic fluctuations. The physical mechanism to explain the difference of these two method are discussed. The implications of device variability in circuits are explored in Chapter 4, in which the coupled device-circuit simulation approach is used instead of compact modeling approach for pursuing best accuracy. Chapter 5 compares the work-function fluctuation with the random dopant fluctuation and the process variation effect in devices and circuits variability. Finally, conclusions are drawn including suggestions on future work.

Chapter 2

Methods for Metal Gate Work-Function Fluctuation Simulation

This chapter presents the simulation technique for work-function fluctuation. The averaged work-function fluctuation (AWKF) method which presented in the previous literature [48,49] used a probability density function to estimate the WKF induced V_{th} fluctuation. Such estimation approach is fast, but can not consider the residual blocks during the discretization procedure. We revise and call it modified AWKF (MAWKF) method to estimated the WKF. However, the AWKF and MAWKF methods use the effective work-function for each device, which may lose some physical phenomena. Therefore, the 3D localized work-function fluctuation (LWKF) approach is thus proposed to analyze WKF.

Figure 2.1(a) shows the material properties used in this work for n-type MOSFET (NMOS) and p-type MOSFET (PMOS) devices [48,49,50,53]. For PMOS device, we use aluminum (Al) incorporation to tune the work-function to the desired value [53]. Due to the work-function is tuned by the dipole formation of high-κ/SiO_x interface, the Al incorporation will give a fixed offset of work-function for different grain orientation, as shown in Fig. 2.1(b).

(a)

Device Type	NMOS		PMOS	
Material	TiN <200>	TiN <111>	TiN <200> + Al	TiN <111> + Al
Probability	60%	40%	60%	40%
Work-function (eV)	4.6	4.4	4.84	4.64
Effective WK (eV)	4.52		4.76	

(b)

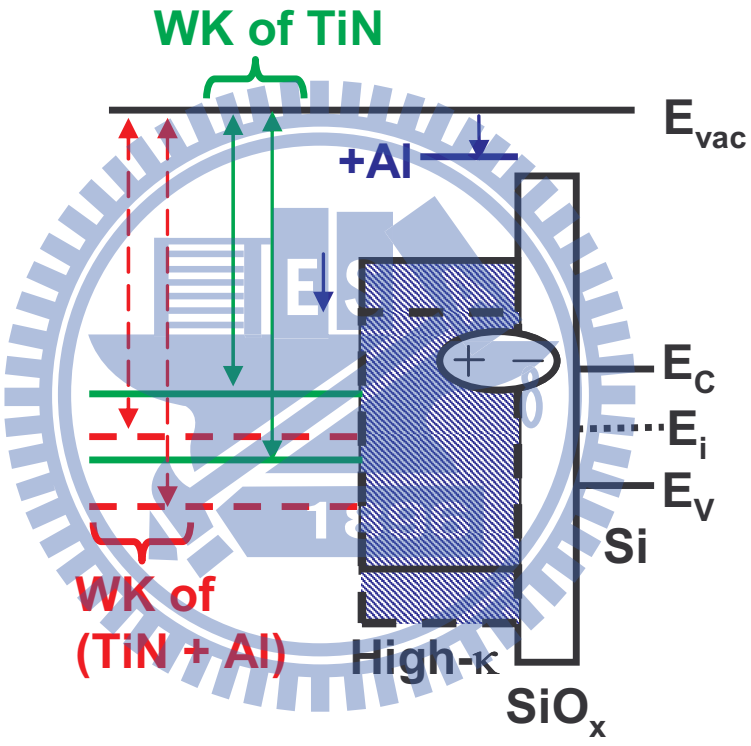


Figure 2.1: (a) The metal properties used in this work. For PMOS device, we use Al incorporation to tune the effective work-function. (b) The illustration of band diagram shows the work-function offset of TiN with adding Al is fixed for different orientation [53], where the green solid lines are original work-function of TiN, after Al incorporation, the work-function becomes larger, as the red dash lines.

2.1 The Averaged Work-Function Fluctuation Simulation Method

The AWKF method [48,49] was reported in 2008. They used an analytical formula to calculated WKF. There are several parameters that have been used in their model and should be introduced. The symbols Φ_1, Φ_2, ..., Φ_N and P_1, P_2, ..., P_N are used to identify the work-function values of grains with different orientations and their corresponding probabilities (percentage share of a particular grain orientation in the total population of grains). Assuming fixed probability values (P_i) for different devices (with identical gate metal) is reasonable because these values remain constant for each particular process conditions. It is also assumed that the grain size (G) of each type of metal film can be obtained by identifying grain boundaries on transmission electron microscope (TEM) pictures of the surface of the metal-gate. Hence, for a transistor with gate length of L and width W, the total number of grains (N) within the metal-gate area can be calculated as (L/G) $\times$ (W/G), assuming square shaped grains, for simplicity. Assuming X_1, X_2, ..., X_N to be the random variables that represent the number of grains with work-function values of Φ_1, Φ_2, ..., Φ_N, respectively, one can calculate the effective work-function of the metal-gate (Φ_M) as a weighted average of work-function of the all existing grains on the gate. Hence, the

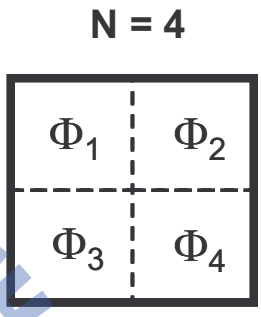
formula for Φ_M can be written as follows:

$$\Phi_M = \frac{X_1}{N}\Phi_1 + \frac{X_2}{N}\Phi_2 + ... + \frac{X_N}{N}\Phi_N, \tag{2.1}$$

where the $\frac{X_1}{N}$ is the percentage of gate area covered with grains whose work-function is Φ_1 and so forth. Given the probabilities and work-function values associated with each grain orientation, the goal is to calculate the mean and standard deviation values for the random variable Φ_M. Figure 2.2 shows the calculation formula of TiN gate for gate area contain 4 grains. Since the threshold voltage (V_{th}) is a linear function of gate work-function, the threshold voltage fluctuation (σV_{th}) is equal to the standard deviation of Φ_M.

Notably, the AWKF method in literature [48,49] did not mention how to calculate WKF if the gate area does not contain the integer value of grains. This part will be described in the next section.

Number of TiN <200>	Number of TiN <111>		
0	4	Probability (%)	$\binom{4}{0}\times(0.6)^0\times(0.4)^4=2.56\%$
		Φ_M (eV)	$\binom{0}{4}\times(4.6)+\binom{4}{4}\times(4.4)=4.4$
1	3	Probability (%)	$\binom{4}{1}\times(0.6)^1\times(0.4)^3=15.36\%$
		Φ_M (eV)	$\binom{1}{4}\times(4.6)+\binom{3}{4}\times(4.4)=4.45$
2	2	Probability (%)	$\binom{4}{2}\times(0.6)^2\times(0.4)^2=34.56\%$
		Φ_M (eV)	$\binom{2}{4}\times(4.6)+\binom{2}{4}\times(4.4)=4.5$
3	1	Probability (%)	$\binom{4}{3}\times(0.6)^1\times(0.4)^3=34.56\%$
		Φ_M (eV)	$\binom{3}{4}\times(4.6)+\binom{1}{4}\times(4.4)=4.55$
4	0	Probability (%)	$\binom{4}{4}\times(0.6)^1\times(0.4)^3=12.96\%$
		Φ_M (eV)	$\binom{4}{4}\times(4.6)+\binom{0}{4}\times(4.4)=4.6$



$$\binom{N}{k}=\frac{N!}{k!(N-k)!}$$

Figure 2.2: The formula in AWKF method to calculate the work-function fluctuation for TiN gate containing 4 grains [48,49].

2.2 The Modified Averaged Work-Function Fluctuation Simulation Method

Due to the gate area will not always fortunately include the integer value of grains, we revise the AWKF method and call the MAWKF method to examine the work-function fluctuation. The simulation flow is shown in Fig. 2.3. At first, the gate area is partitioned into several parts according to the average grain size, here we assume the grain is square for simplification. Then the grain orientation of each parts and total gate work-function are randomly generated based on properties of metal as shown in Fig. 2.1(b). The work-function of each partitioned area (WK_i) is a random value. The summation of WK_i is then averaged to obtain the effective work-function of transistor and then used for WKF induced characteristic fluctuations estimation. Figures 2.4(a)-2.4(c) show the probability distributions of work-function for devices with one and nine grains on the gate area. The distribution is similar to the normal distribution as the numbers of grain increases. In other words, in nanoscale transistor with scaled gate area, the distribution is not a normal distribution and therefore the WKF induced σV_{th} may not be a normal distribution as the gate area scales. Figure 2.4(d) examines the dependence of WKF induced σV_{th} versus the average grain length (the square root of grain size) on a 16 nm $\times$ 16 nm gate area. The WKF induced σV_{th} increases significantly as the average grain size increases, which imply

the importance of controlling metal-gate grain size in reducing WKF effect. The trend of the results is valid with experimental data [47]. Additionally, when the metal grain size is larger than devices gate area, the σV_{th} saturated due to the number of grain in a device gate area unchanged (contain only one grain). Notably, the different process of gate formulation, gate first or replacement gate, may change the thermal budget and changes the grain size of metal material.

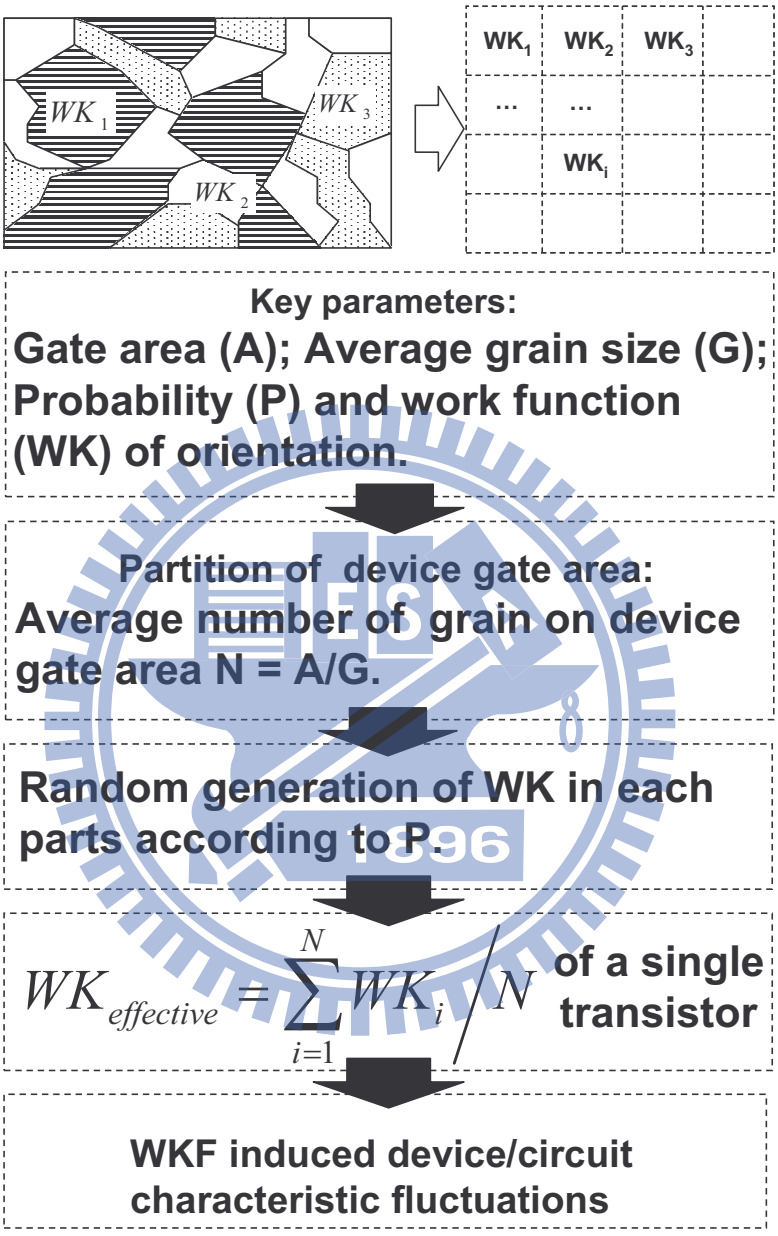


Figure 2.3: The simulation flow of MAWKF method. The gate area is partitioned into several square pieces according to the average grain size [47]. The work-function of each partitioned area WK_i is a random value. The summation of WK_i is then averaged to obtain the effective work-function of each transistor and then used for WKF induced characteristic fluctuations estimation.

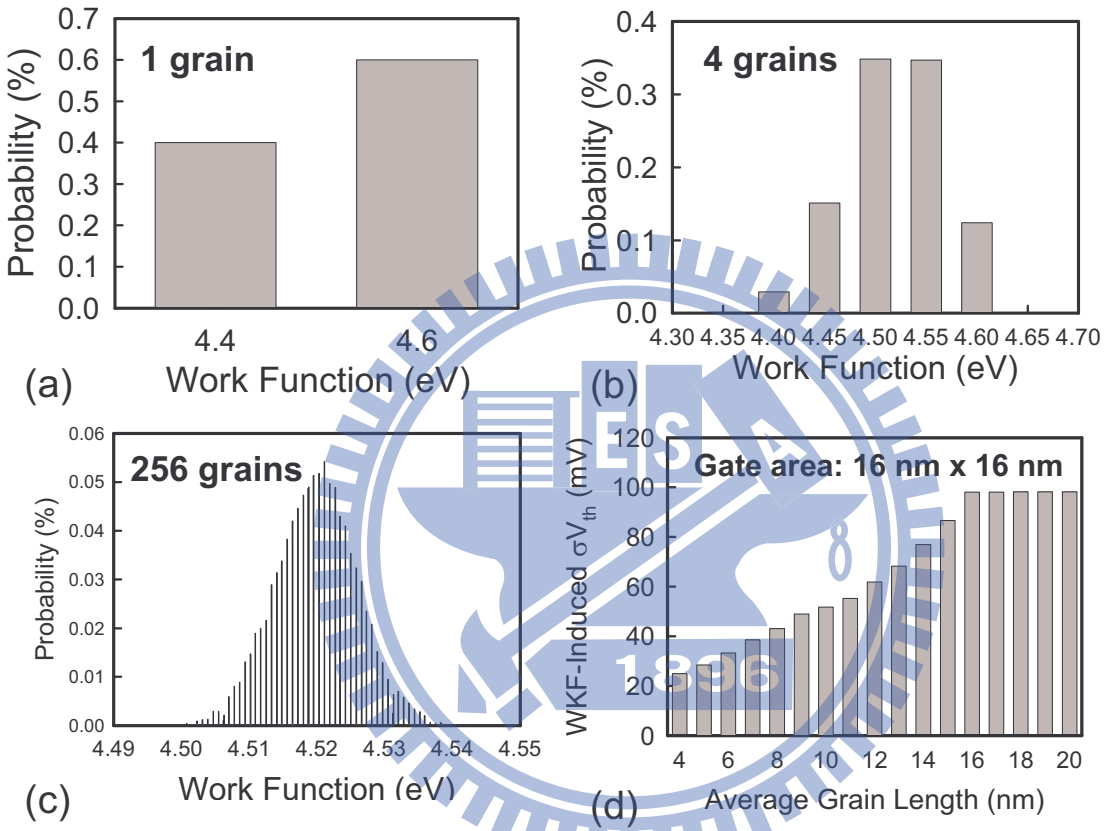


Figure 2.4: The obtained probability distributions of TiN work-function for devices with (a) 1, (b) 4, and (c) 256 grains on the gate area. (d) Dependence of TiN metal-gate induced σV_{th} versus the average grain length, where the grain length is square root of grain size. The gate area is 16 nm $\times$ 16 nm.

In the proposed MAWKF method, the results are similar to AWKF method. However, the AWKF method can not consider the residual blocks as shown in Fig. 2.5(a) due to the limitation of the used formula. In the MAWKF method, we also randomly generate the work-function for each residual grain, and consider their weight related to their area when calculating averaged work-function. Figure 2.5(b) compares the AWKF and MAWKF methods with TiN metal gate. The solid triangle and dash cross lines show the results with and without considering the residual area. The trend of σV_{th} is the same as the other; however, there are several flat area existing in the dash line, which may mislead the impact of WKF.

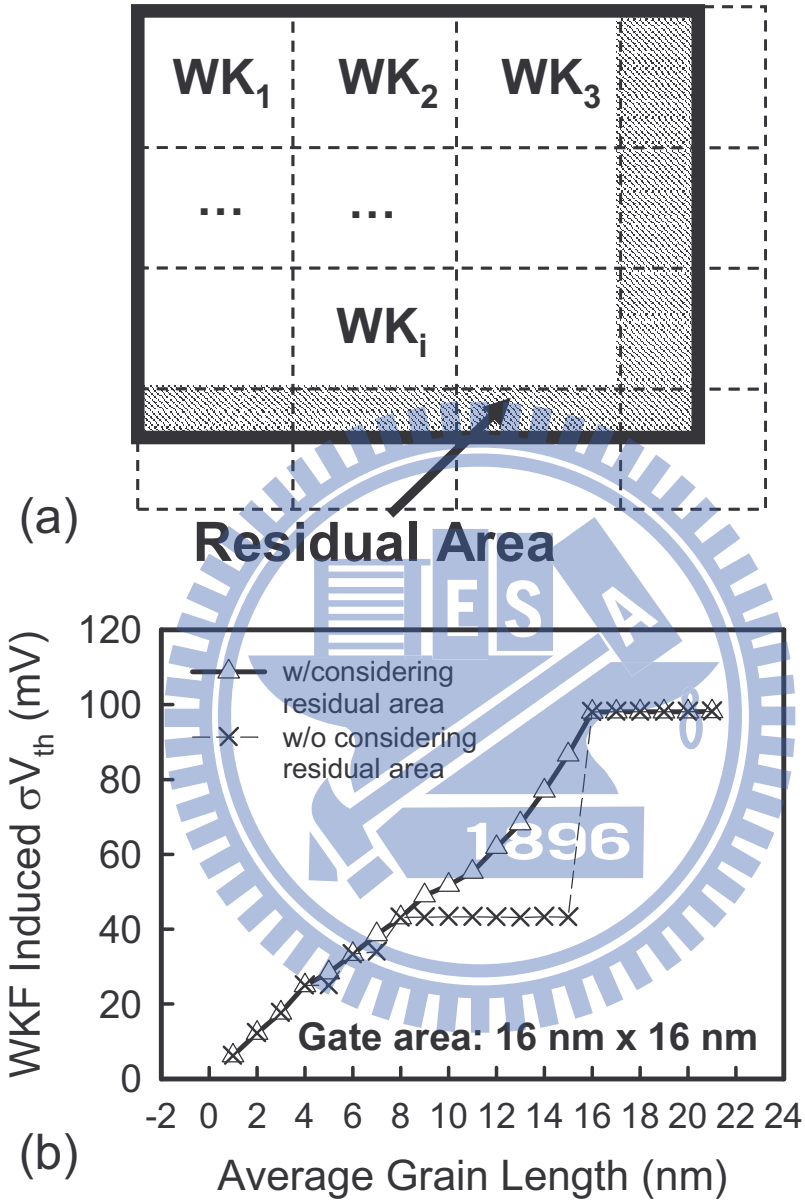


Figure 2.5: (a) The residual area which should be considered when estimating work-functions. (b) Work-function fluctuation induced threshold voltage fluctuation versus average grain length with and without taking residual gate area into consideration.

2.3 The 3D Localized Work-Function Fluctuation Simulation Method

The AWKF and MAWKF use the effective work-function, and may lack physically best accuracy [51]. This was pointed out in 2009. They assumed that devices are composed of smaller transistors both in parallel and in series over the gate area. Each small transistor with gate electrode has a metal grain with a specific work function and thus its own inversion carrier density in the channel. Using the physical model in [54] for each of the small transistor, then impose Kirchhoff's law on the resulting mesh of them, and finally numerically solve for the device behavior. However, the method may not accurately describe nanoscale grain orientation due to the model probably not work well for such small transistor. Therefore, to characterize the metal-gate induced work-function fluctuation more preciously, we use 3D device simulation to examine such phenomenon, LWKF method. Figure 2.6 illustrates the work-function fluctuation source of CMOS device and the simulation method for LWKF. The boundary condition is derived form Gauss's law:

$$\epsilon_s \frac{\partial \phi}{\partial z} - \epsilon_{ox} \frac{\partial \phi_{ox}}{\partial z} = Q_s, \tag{2.2}$$

and the relation of the metal/oxide/semiconductor [1]:

$$\phi = \chi + \frac{E_g}{2e} + \phi_{fp} - Q_s \frac{t_{ox}}{\epsilon_{ox}} - \frac{WK}{e} - \phi_{ox}, \tag{2.3}$$

where the ϕ_{ox}, t_{ox}, and ϵ_{ox} are the potential, thickness and dielectric constant of oxide, ϵ_s, χ, E_g are dielectric constant, electron affinity, and bandgap of semiconductor, ϕ_{fp} is the difference between intrinsic fermi level and fermi level, and Q_s is the fixed charge at silicon/oxide interface. In our structure, since the work-function is a grain area related step function $WK\chi_{A_i}(x,y)$, as shown in Fig. 2.7, the random grain distribution is therefore considered in LWKF method, where the total work-function on the metal gate = $\sum_{i=1}^{N} WK\chi_{A_i}(x,y)$. Figure 2.8 presents the simulation flow chart of LWKF. To describe the WKF induced characteristic fluctuations, in contrast to AWKF, MAWKF methods or compact model [38-45,48,49,51], we directly partition the device gate metal material into many sub-regions according to the grain size [47], and then we randomly generate the work-function to each sub-region according to the material properties and map them into device gate for our experimentally calibrated 3D quantum-corrected device simulation [23]. Two hundred statistically random devices are generated to examine the WKF induced characteristic fluctuations. This method can capture the different work-function of grain orientation position effect, which can not predict by previous methods.

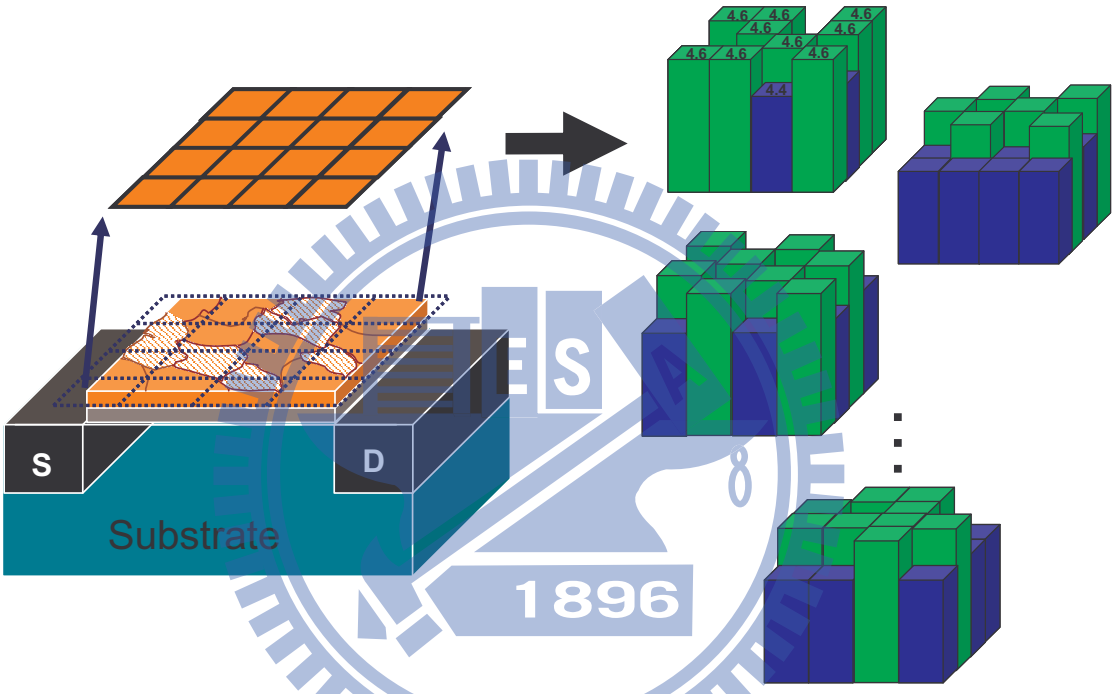


Figure 2.6: The illustration of 3D localized work-function fluctuation simulation. We directly partition the device gate metal material into many sub-regions according to the grain size [47]. The sub-regions are square or rectangle. There are total 2^{16} work-function combinations for 16 grains.

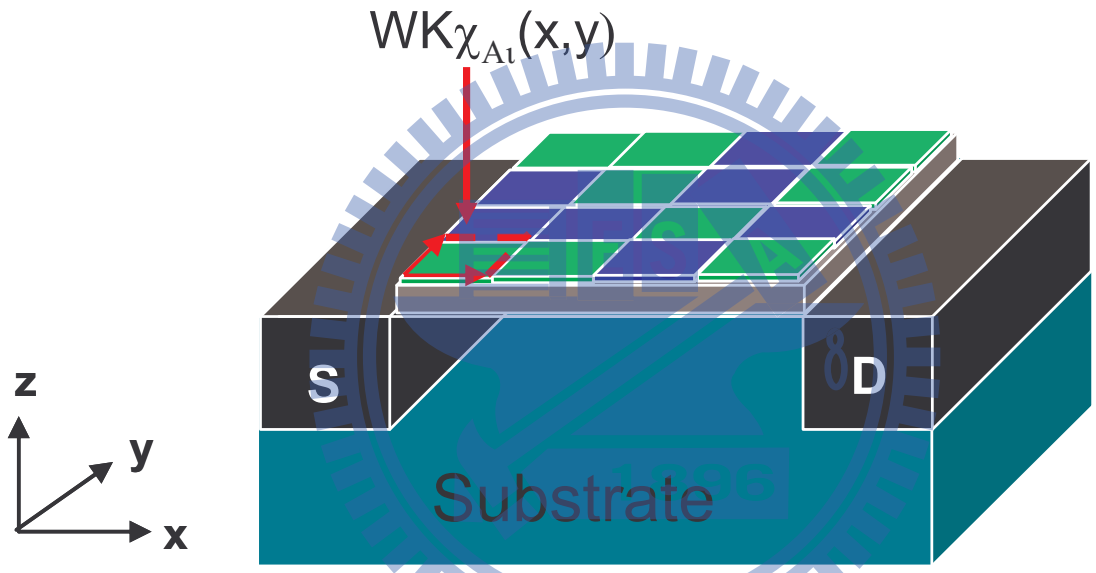


Figure 2.7: The mathematical formulation to describe the 3D localized work-function structure.

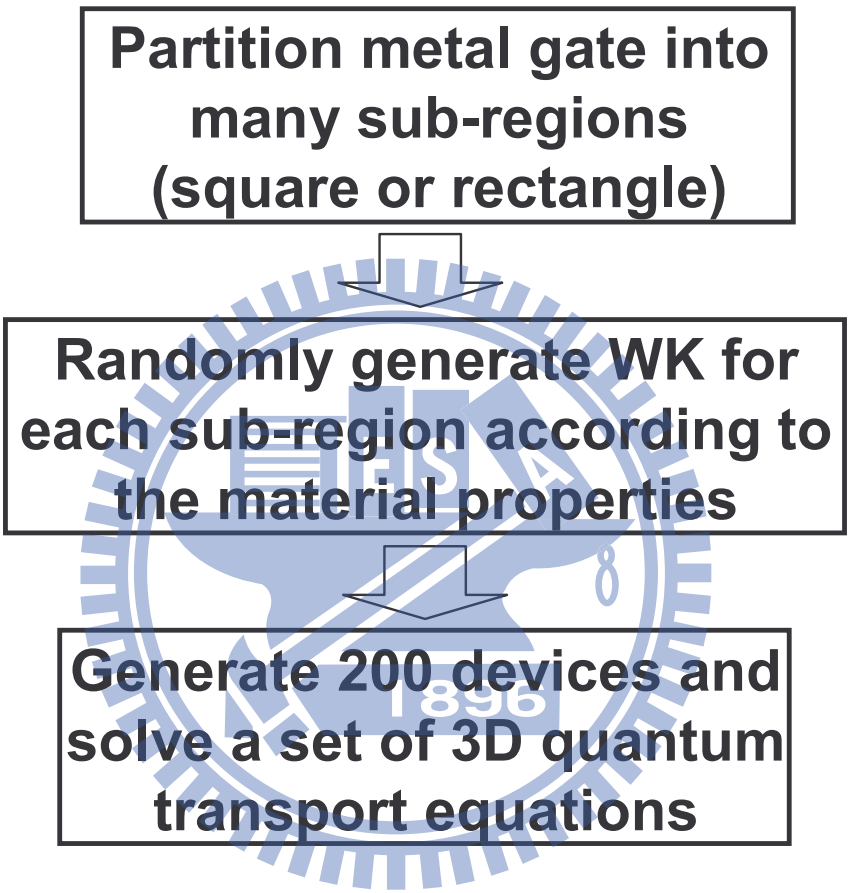


Figure 2.8: Simulation flow chart of 3D localized work-function fluctuation method. We randomly generate the work-function to each sub-region according to the material properties and map them into device gate for our experimentally calibrated 3D quantum-corrected device simulation [23].

2.4 The Coupled Device-Circuit Simulation Technique

Due to lack well-known compact model for 16-nm-gate CMOS devices, the characteristics of the devices of the circuit are first estimated by solving the device transport equations. The obtained result is then used as initial guesses in the coupled device-circuit simulation. The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations (in the form of a large matrix that contains both circuit and device equations), which are solved simultaneously to obtain the circuit characteristics. The device characteristics, such as distributions of potential and current density, obtained by device simulation are input in the circuit simulation through device contacts. The illustration of coupled device-circuit simulation is shown in Fig. 2.9, here we use an inverter circuit as example. The coupled device-circuit simulation flow chart is shown in Fig. 2.10 [38-45]. Figure 2.11 shows the inverter, static random access memory (SRAM), common source amplifier, and current mirror circuits as examples for digital/analog characteristic fluctuations exploration.

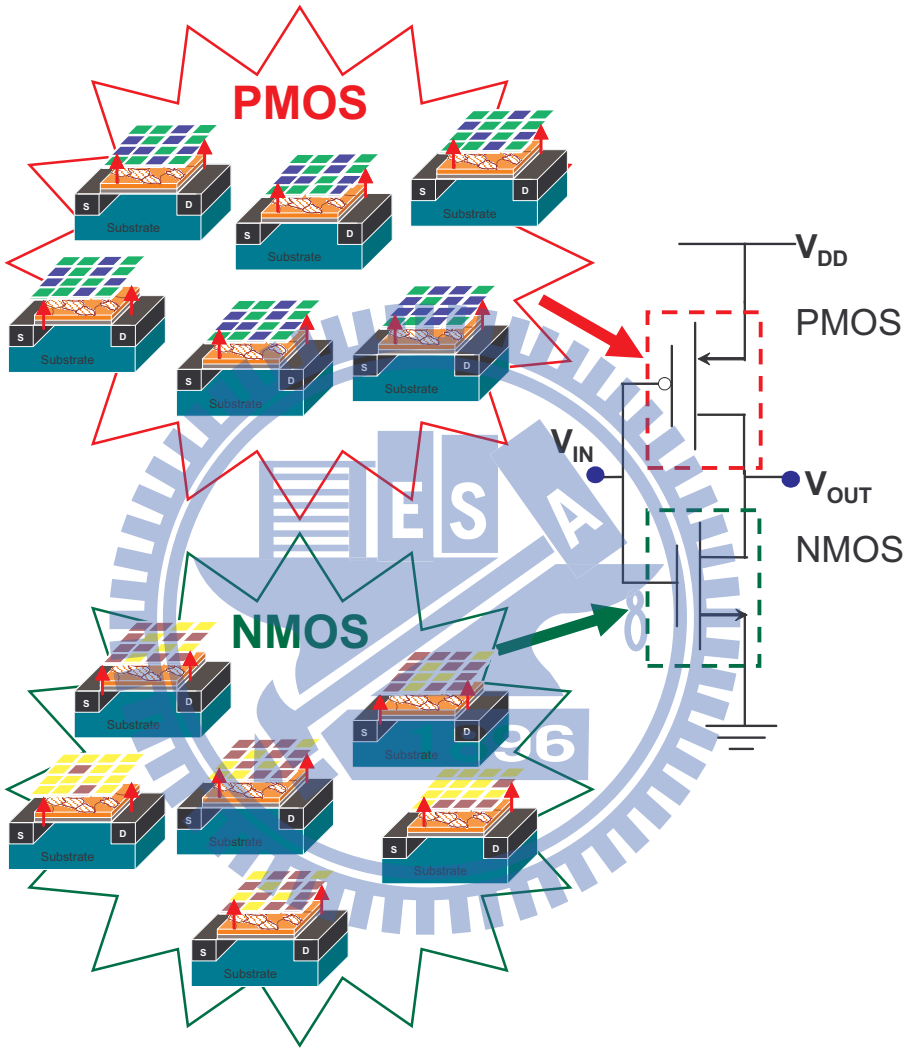


Figure 2.9: The illustration of coupled device circuit simulation with an inverter circuit as example [38-45]. The characteristics of the devices and circuit are considered simultaneously.

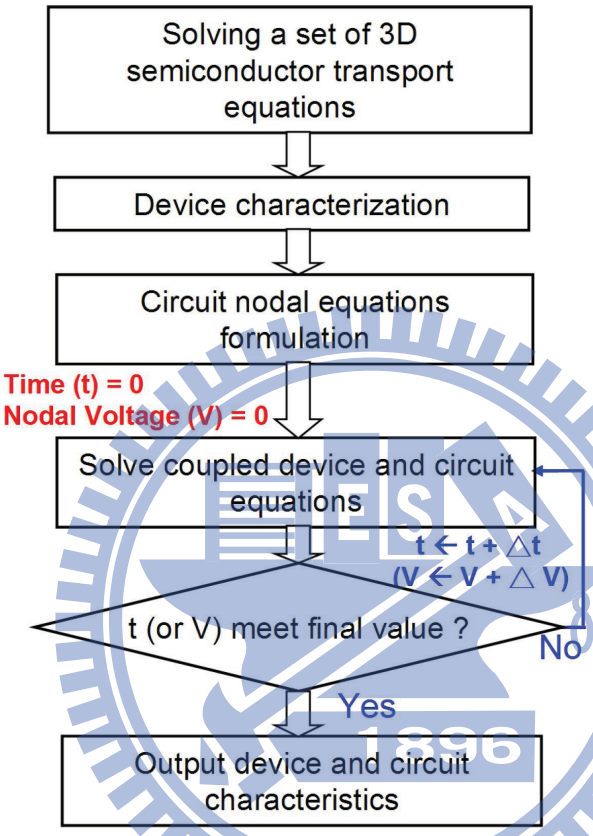


Figure 2.10: The coupled device circuit simulation flow [38-45,55-67]. The characteristics of the devices of the circuit are first estimated by solving the device transport equations. The obtained result is then used as initial guesses in the coupled device-circuit simulation. The nodal equations of the test circuit are formulated and then directly coupled to the device transport equations, which are solved simultaneously to obtain the devices and circuit characteristics.

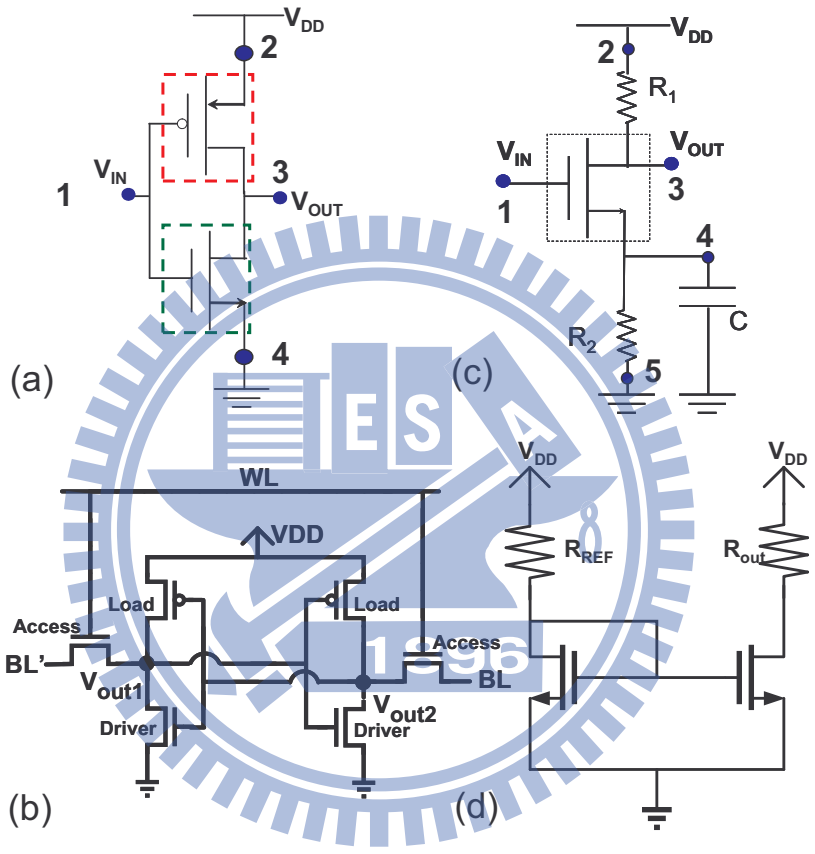
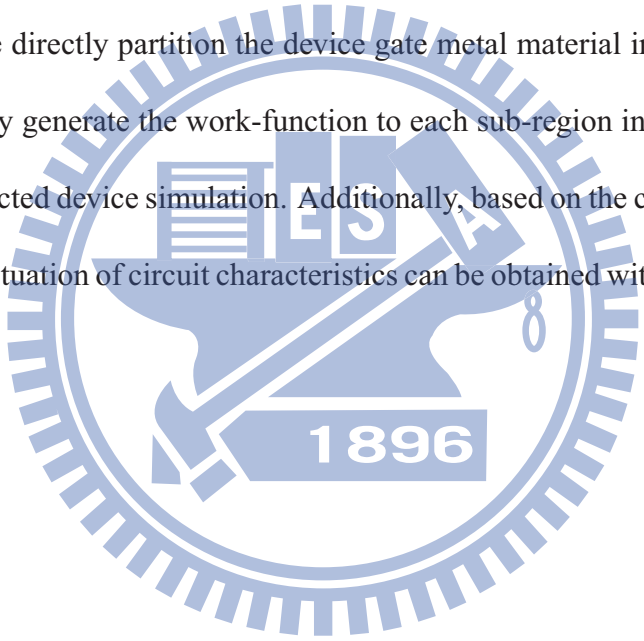


Figure 2.11: The (a) inverter, (b) static random access memory, (c) common source amplifier, and (d) current mirror circuits as examples for digital/analog characteristics fluctuation exploration.

2.5 Summary of this Chapter

This chapter has presented the AWKF, MAWKF, and 3D LWKF methods. The AWKF used an analytical formula to calculate WKF. However, the method does not consider the residual area of gate due to the limitation of the formula. The MAWKF method revised the AWKF method to improve the usage of estimating WKF induced characteristic fluctuation. In 3D LWKF method, we directly partition the device gate metal material into many sub-regions and then randomly generate the work-function to each sub-region into device gate for our 3D quantum-corrected device simulation. Additionally, based on the coupled device circuit simulation, the fluctuation of circuit characteristics can be obtained with more device physics inside.



Chapter 3

Devices Characteristic Fluctuations

This chapter estimates and compares the influences of the work-function fluctuation with MAWKF and LWKF methods on 16-nm-gate planar MOSFET devices. The DC characteristics are examined in threshold voltage, on-state current (I_{ON}) and off-state current (I_{OFF}). The AC characteristics are investigated in terms of gate capacitance (C_G) and cut-off frequency (f_T).

3.1 DC Characteristic Fluctuations Comparison

The control devices in this study are the 16-nm-gate bulk planar MOSFETs (width: 16 nm) with amorphous-based TiN/HfO_2 gate stacks with an equivalent oxide thickness of 0.8

nm and 4.52 eV and 4.76 eV work-functions for NMOS and PMOS devices, respectively. The nominal channel doping concentrations are 1.5×10^{18} cm^{-3}, the source/drain doping concentrations are 2×10^{20} cm^{-3}, and the lightly doped drain (LDD) doping concentrations are 4×10^{19} cm^{-3}. The junction depth of LDD region is 8 nm. The threshold voltages are calibrated to 250 mV following ITRS roadmap [2,23,25,27]. The details of device setting are shown in Fig. 3.1. The subthreshold slope (SS) could be improved by tuning the channel doping shape profile or metal work-function. The properties of metal are shown in Fig. 2.1(a) and the average grain size is 4 nm × 4 nm [47]. Additionally, to compare fairly the NMOS- and PMOS-induced characteristic fluctuation and eliminate the effect of transistor size on fluctuation, the dimensions of the PMOS devices are the same as those of the NMOS ones.

The mobility model used in our 3D device simulation is is given by:

$$\frac{1}{\mu} = \frac{D}{\mu_{surf\_aps}} + \frac{D}{\mu_{surf\_rs}} + \frac{1}{\mu_{bulk}}, \tag{3.1}$$

where $D = \exp(x/l_{crit})$, x is the distance from the interface and l_{crit} is a fitting parameter. The mobility consists of three parts: (1) the surface contribution due to acoustic phonon scattering, $\mu_{surf\_aps} = \frac{B}{\mathbf{E}} + \frac{C(N_i/N_0)^{\tau}}{\mathbf{E}^{1/3}(T/T_0)^K}$, where $N_i = N_A + N_D$, T_0 = 300 K, $\mathbf{E}$ is the transverse electric field normal to the interface of semiconductor and insulator, B and C are parameters which based on physically derived quantities, N_0 and τ are fitting parameters,

T is lattice temperature, and K is the temperature dependence of the probability of surface phonon scattering; (2) the contribution attributed to surface roughness scattering is $\mu_{surf\_rs} = (\frac{(\mathbf{E}/\mathbf{E_r ef})^{\Xi}}{\delta} + \frac{\mathbf{E^3}}{\eta})^{-1}$, where $\Xi = A + \frac{\alpha \cdot (n+p) N_{ref}^{v}}{(N_i + N_1)^v}$, E_{ref} = 1 V/cm is a reference electric field to ensure a unitless numerator in μ_{surf_rs}, N_{ref} = 1 cm^{-3} is a reference doping concentration to cancel the unit of the term raised to the power v in the denominator of Ξ, δ is a constant that depends on the details of the technology, such as oxide growth conditions, N_1 = 1 cm^{-3}, A, α, and η are fitting parameters; (3) and the bulk mobility is $\mu_{bulk} = \mu_L (\frac{T}{T_0})^{-\xi}$, where μ_L is the mobility due to bulk phonon scattering and ξ is a fitting parameter. The parameters of mobility were calibrated with the measurement of experimentally fabricated CMOS devices [23], as shown in Fig. 3.2.

Channel doping	$1.5x10^{18}$ cm^{-3}
S/D doping	$2x10^{20}$ cm^{-3}
LDD doping	$4x10^{19}$ cm^{-3}
Workfunction	4.52 eV (NMOS), 4.76 eV (PMOS)
Oxide thickness	0.8 nm EOT HfO_2
Junction depth	Around 1/2 L_g (8 nm) to maintain subthreshold leakage

Performance (For LOP)	V_t (mV)	I_{on} ($\mu A/\mu m$)	I_{off} ($nA/\mu m$)	SS (mV/dec)
NMOS	250	521	200	147
PMOS	-250	390	198	149

Figure 3.1: The device parameters setting and performance used in this work.

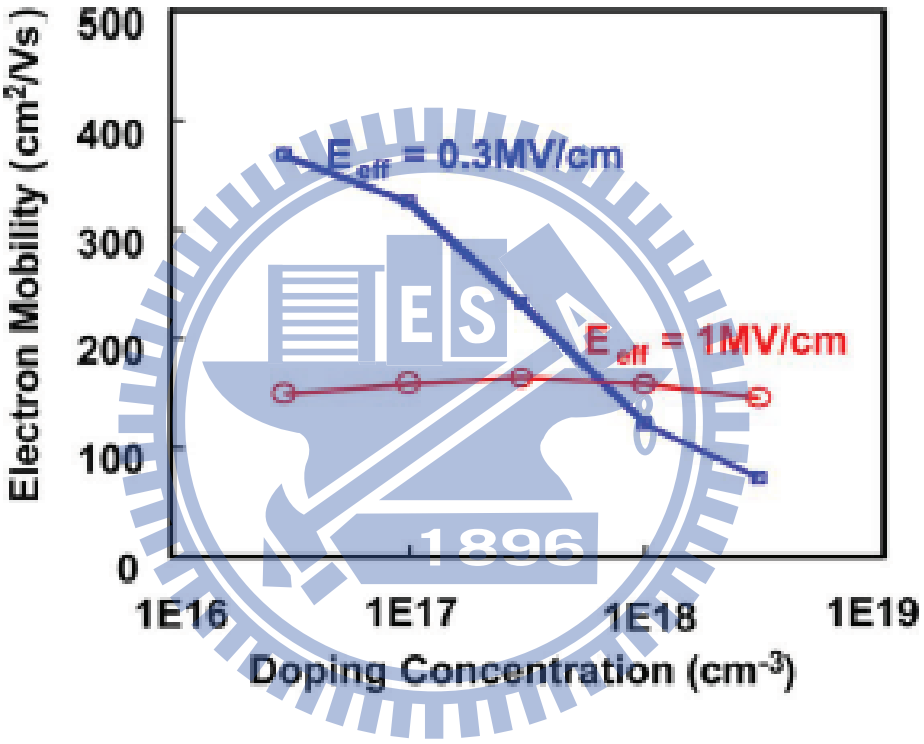


Figure 3.2: Extracted nonstrain mobility versus doping concentration at 0.3 and 1 MV/cm vertical field.

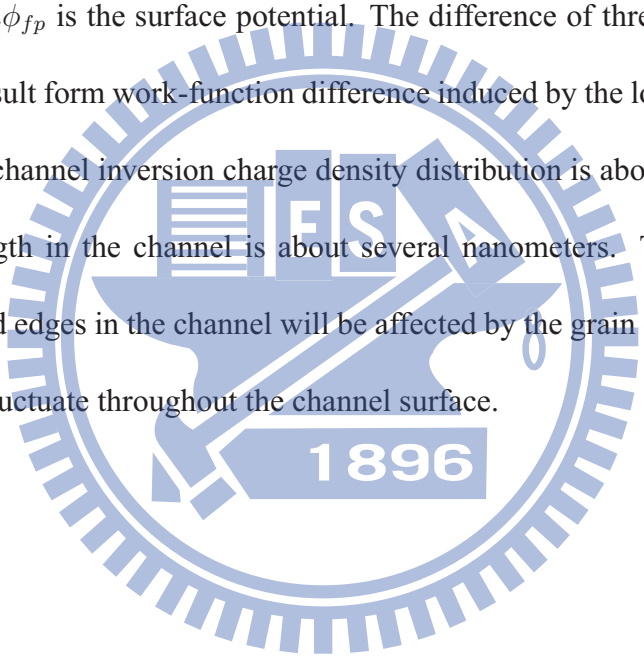
Figure 3.3 shows the threshold voltage fluctuation, the normalized on- and off-state current fluctuations (σI_{ON} and σI_{OFF}) induced by WKF of NMOS and PMOS devices with LWKF method, the values are 36.7 mV, 5%, 57%, 42.5 mV, 10%, 46%, respectively. We note that the V_{th} is determined form the current criterion when drain current is 10^{-7} A. The I_{ON} is the drain current at on-state (gate voltage (V_G) and drain voltage (V_D) are equal to 0.8 V), and the I_{OFF} is the drain current at off-state (V_G = 0 V and V_D = 0.8 V). Figure 3.4 compares σV_{th} among AWKF, MAWKF method and LWKF methods for the gate area is 16 nm $\times$ 16 nm with grain size equal to 4 nm $\times$ 4 nm (gate area contain integer number of grain), and 5 nm $\times$ 5 nm (gate area does not contain integer number of grain). The AWKF and MAWKF method significantly underestimated the WKF induced σV_{th}. To further understanding the physical mechanism of WKF induced device characteristic fluctuations; we investigate the on-state potential, charge distribution at channel surface, and band diagram. Due to the probabilistic distribution of work-function, the effective work functions of 200 devices are not a deterministic value and results in device to device performance variation. This variation can also estimated by MAWKF method. However, the position of different metal grain orientation position effect can further induce device characteristic fluctuations. Figure 3.5(a) shows the large-scale statistically computed results of V_{th} as a function of the number of TiN <200> (higher work-function) contained for NMOS device. From the number of high work-function grain orientation point of view, the effective work-function

of a single device increases as the number of TiN <200> increases, result in a higher V_{th}. Moreover, it is found that even for devices with the same numbers of TiN <200> inside the gate, the effect of nanoscale grain orientation position induces different fluctuations of characteristics in spite of there being the same number of TiN <200>. To explore the grain orientation-position-induced V_{th} fluctuation, the on-state potential distributions with containing nine TiN <200> but different position inside the gate are investigated, as shown in Figs. 3.5(b) and (c). The potential distributions are at the channel surface. For a device with TiN <200> located near the source and at the middle of channel, the corresponding potential distributions are significant decreased in these areas, which significantly changes the electron conducting path and induce larger V_{th}. The importance of grain position effect is found for the first time. Figure 3.6(a) presents the charge distribution of the channel surface extracted from Fig. 3.5(b) at V_G = 0.8 V, and V_D = 0 V; we can clearly find the charge distribution is strongly governed by different local work-function of gate metal orientation, such phenomenon can not be predicted by MAWKF method. The MAWKF model uses an effective work function for each device to calculate the performance, which assumes a uniform inversion charge density at the channel surface. The difference between these two methods can be considered in terms of the band diagram, as shown in Fig. 3.6(b) and Fig. 3.7, which leads to different substrate band bending and varying throughout the channel. Since the threshold voltage is determined by the work-function difference between metal

and semiconductor [1], as shown below:

$$V_{th} = (|Q_{SD}(max)| - Q_{ss})/C_{ox} + \phi_{ms} + 2\phi_{fp}, \tag{3.2}$$

where the $|Q_{SD}(max)|$ is the maximum charge density of depletion region, Q_{ss} is the oxide surface charge, C_{ox} is the oxide capacitance, ϕ_{ms} is work-function difference between metal and semiconductor, and $2\phi_{fp}$ is the surface potential. The difference of threshold voltage fluctuation is therefore result form work-function difference induced by the localized metal grain. Since the on-state channel inversion charge density distribution is above 10^{19} cm^{-3}, the charge screening length in the channel is about several nanometers. Therefore, for nanoscale grains, the band edges in the channel will be affected by the grain directly above a given region, and will fluctuate throughout the channel surface.



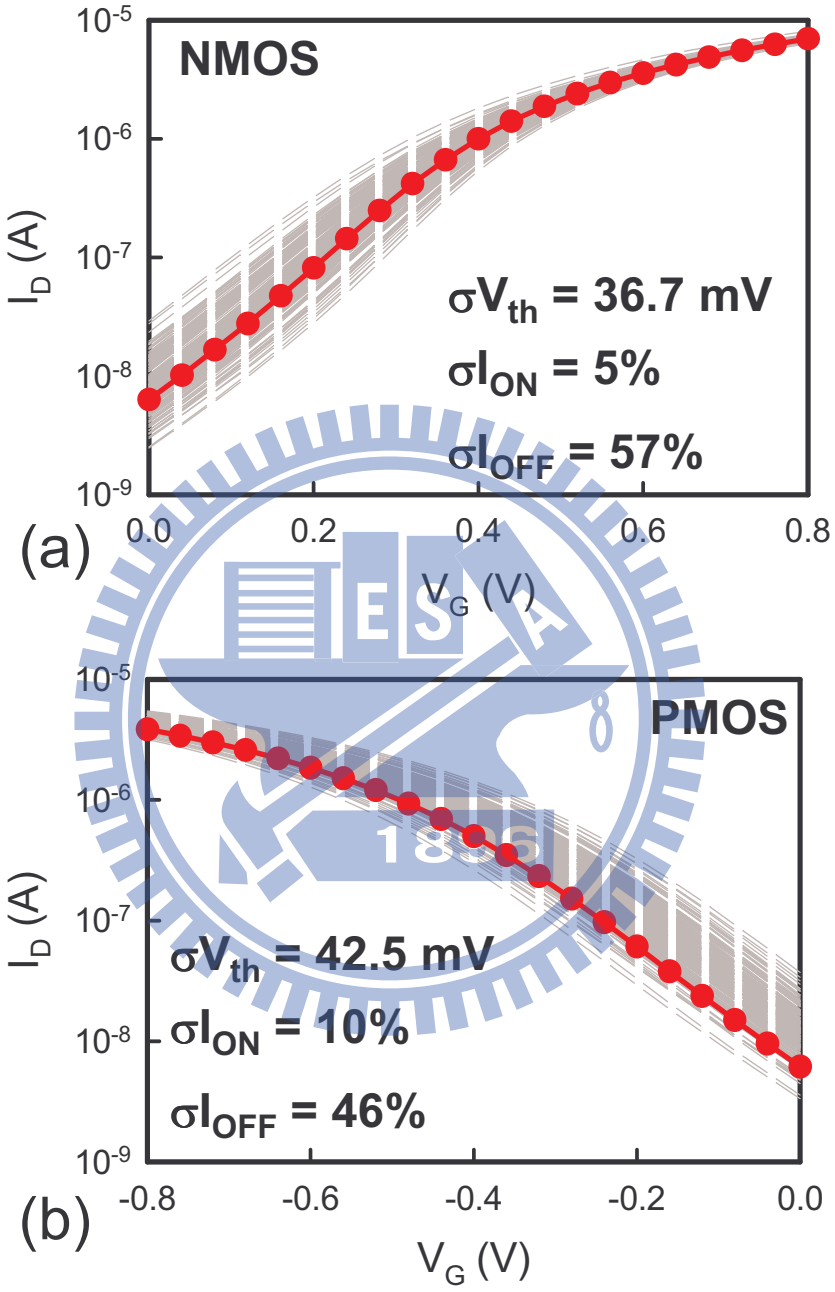


Figure 3.3: The I_D-V_G curves of localized work-function fluctuation method for (a) NMOS and (b) PMOS devices, where the nominal curve with effective work-function of 4.52 eV (NMOS) and 4.76 eV (PMOS) are the red thick symbol lines. The V_{th}, and the normalized I_{ON} and I_{OFF} fluctuations are shown in the inset.

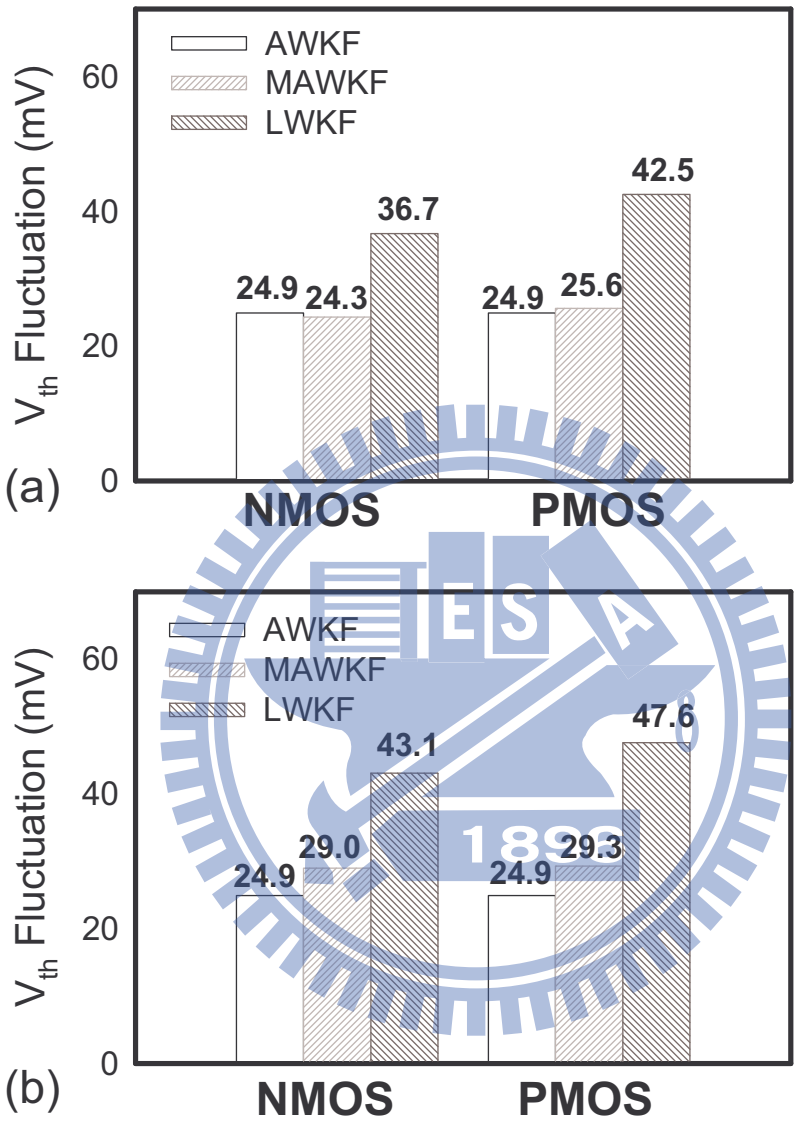


Figure 3.4: Comparison of threshold voltage fluctuation among averaged work-function fluctuation method, modified averaged work-function fluctuation method and localized work-function fluctuation method for grain size equal to (a) 4 nm $\times$ 4 nm (the gate area contain integer number of grain case) and (b) 5 nm $\times$ 5 nm (the gate area contain non-integer number of grain case).

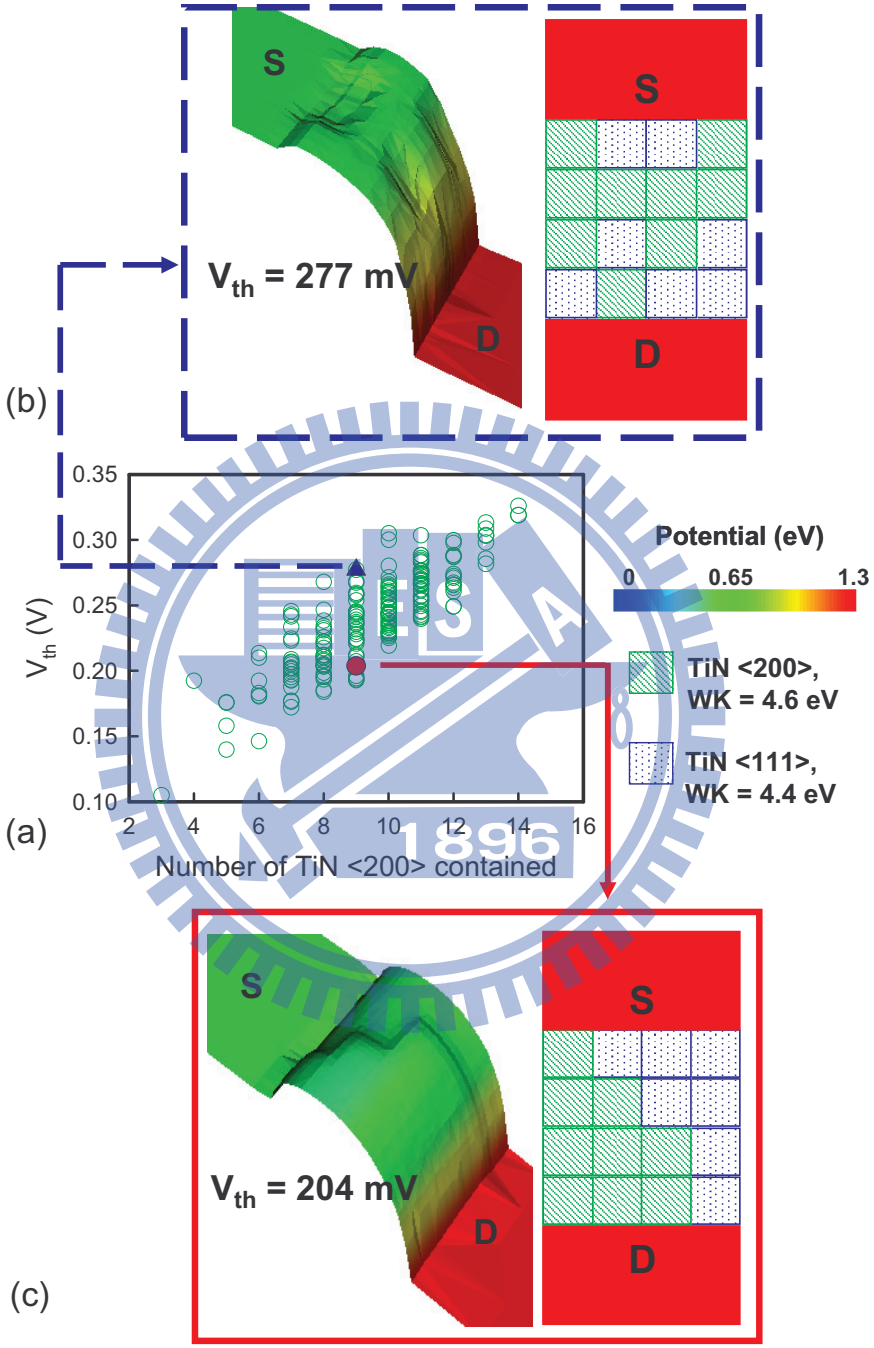


Figure 3.5: (a) Threshold voltage distribution as a function of number of TiN <200> contained. The on-state (V_G = 0.8 V and V_D = 0.8 V) potential distribution of (b) higher V_{th} and (c) lower V_{th} devices with the same number of TiN <200>.

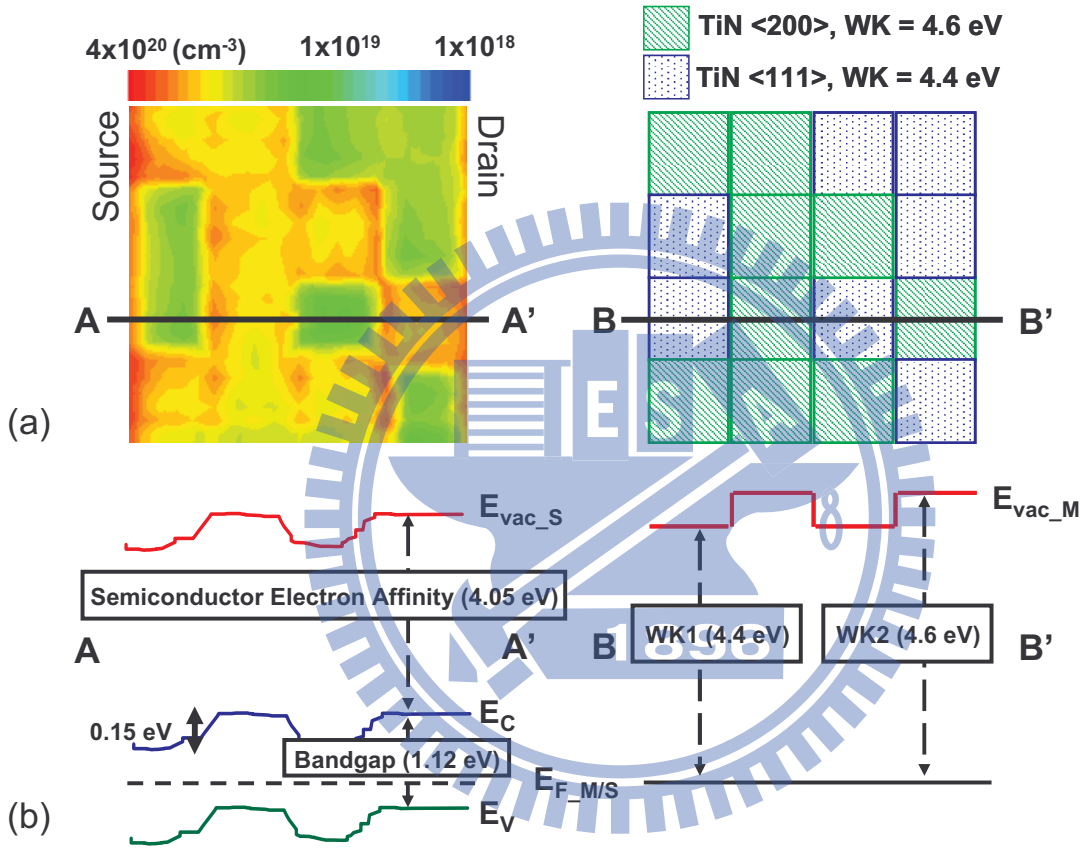


Figure 3.6: (a) The charge distribution and the metal grain distribution extracted from Fig. 3.5(b) at V_G = 0.8 V and V_D = 0 V. (b) The band diagram in the semiconductor and the metal gate.

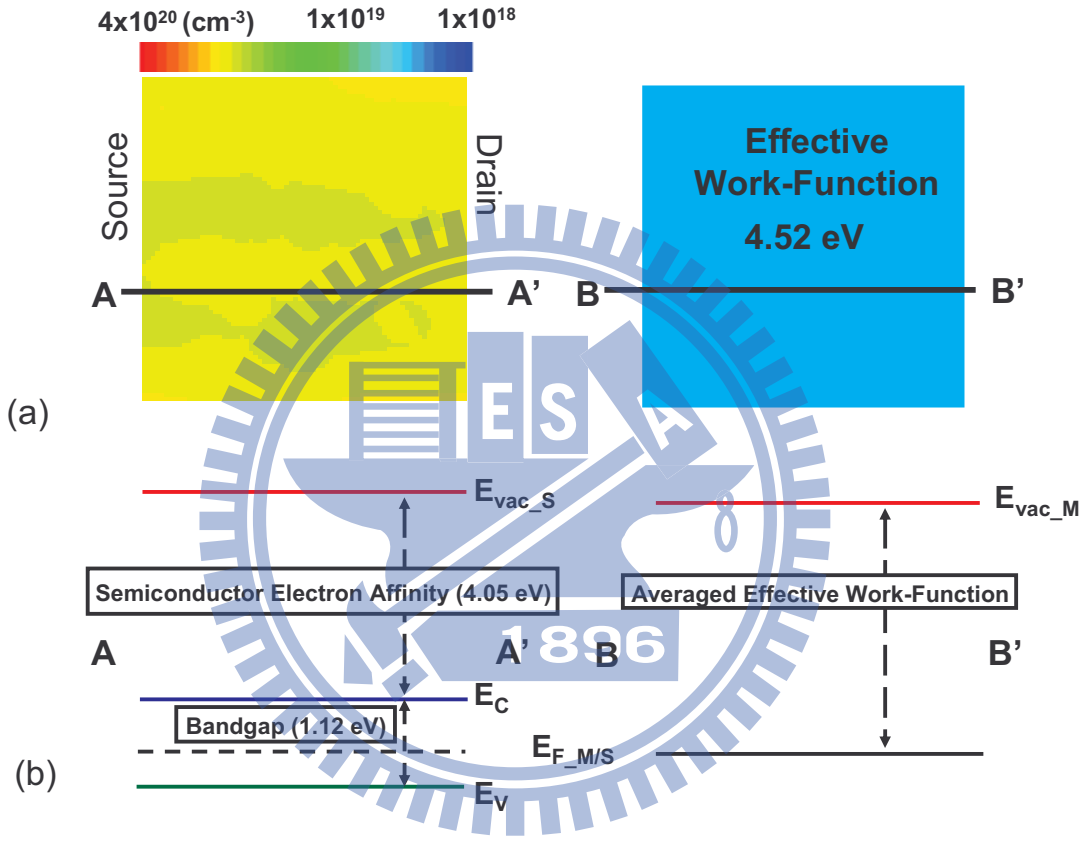


Figure 3.7: (a) The charge distribution and the metal grain distribution extracted from control device at V_G = 0.8 V and V_D = 0 V. (b) The band diagram in the semiconductor and the metal gate.

3.2 AC Characteristic Fluctuations Comparison

In this section, the device AC characteristics including C_G and f_T are investigated. The MAWKF and LWKF fluctuated C_G-V_G curves are compares in Figs 3.8(a) and (b). And the summarized gate capacitance fluctuation (σC_G) at different gate bias are shown in Figs 3.9. At zero gate bias or negative gate bias, the accumulation layer screens the impact of WKF. Additionally, at low gate bias, the total capacitance decreases because of the increased depletion region. The associated value of C_G fluctuation is small. The capacitive response is then dominated by increment of inversion in the moderate inversion. The device characteristics are then impacted by work-function fluctuated electrostatic potentials. However, if the high V_G is achieved, the result are significant different between these two methods. In MAWKF method, the capacitive response becomes dominated by the inversion layer, the impact of the work-function difference on the device electrostatics is screened by the inversion layer itself. The variation of capacitance is now again becomes the variation of gate oxide. The impact of WKF induced electrostatic potential variations is therefore bringing less impact on channel surface. In LWKF method, although the inversion layer screen effect also happened, the grain position effect still influences the charge distribution of inversion layer for different device, as shown in Figs 3.10, results in a larger σC_G. The importance of LWKF method are also shown for device AC characteristics. However, it should be notice that even in the result of LWKF method, the largest fluctuation of σC_G

is less than 3% of it's nominal value. The WKF bring less impact on gate capacitance fluctuation, it is different with device DC characteristic fluctuations.

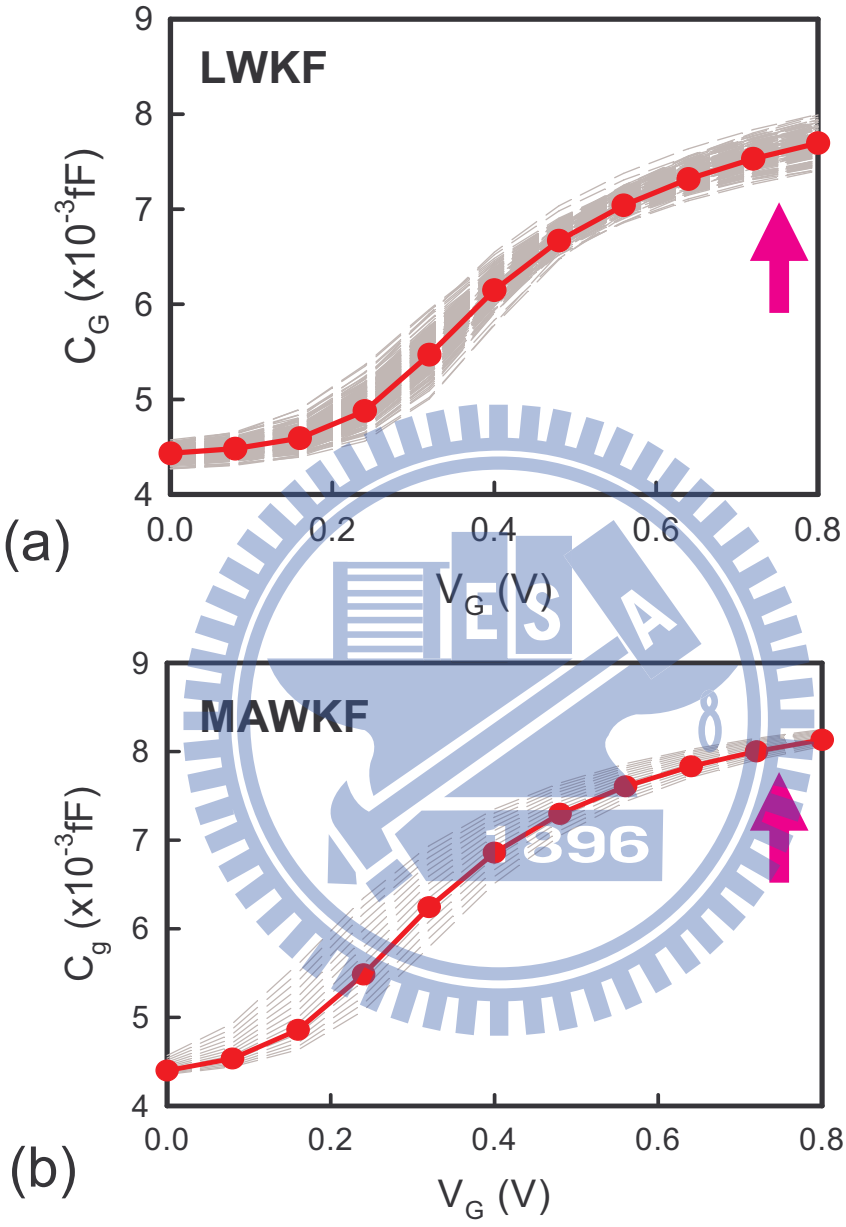


Figure 3.8: The fluctuated C_G-V_G curves with (a) localized work-function fluctuation and (b) modified averaged work-function fluctuation methods. The results are significantly different at high gate bias.

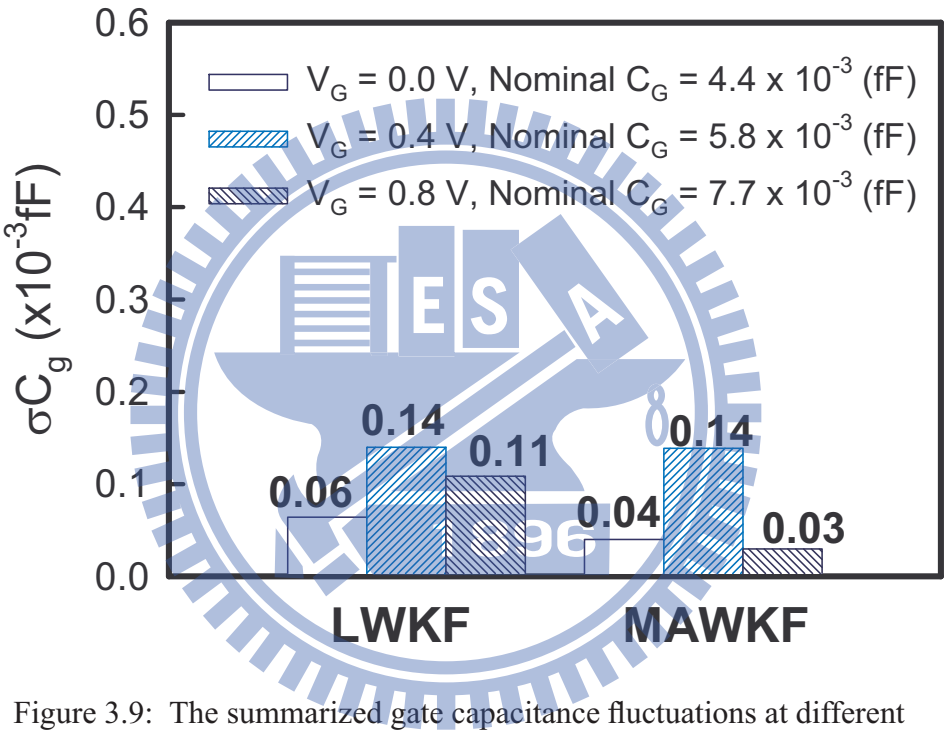


Figure 3.9: The summarized gate capacitance fluctuations at different gate bias with modified averaged work-function fluctuation and localized work-function fluctuation method.

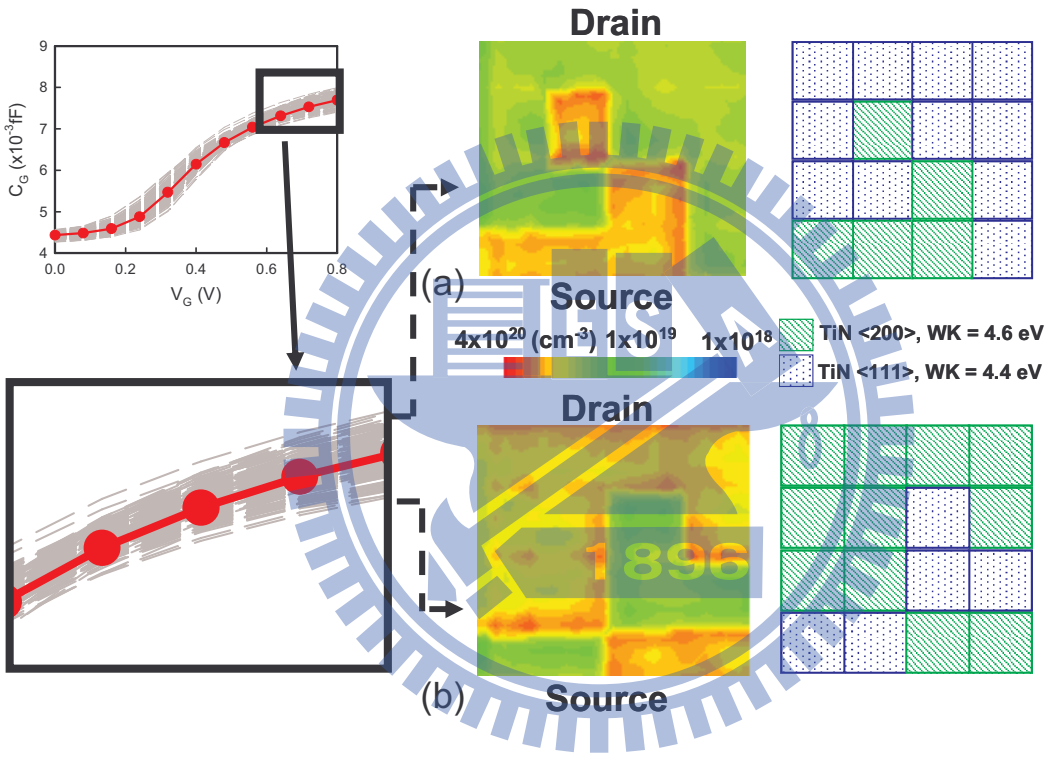


Figure 3.10: The charge distributions extract from (a) the largest and (b) the smallest gate capacitance devices.

Figure 3.11 compares the NMOS fluctuated f_T-V_G curves for MAWKF and LWKF methods, the cutoff frequency f_T is the frequency when the device short circuit current gain h_{21} is unity. Figure 3.12 shows the f_T fluctuations (σf_T) versus the gate voltage. The significant difference of two methods at high gate bias is clearly shown. To explain the results easily, we use the simplified formula $f_T = g_m / 2\pi C_G = v_{sat} / 2\pi L_g$, where the g_m and v_{sat} are the transconductance and the saturation carrier velocity of the transistors. The results show that MAWKF method significantly underestimate the σf_T, especially at strong inversion region due to the effective work-function difference between individual devices are screened. The WKF induced σf_T is reduced as the saturation carrier velocity occurs at high gate bias, the f_T is dependent on gate length only and almost the same for different work-function in MAWKF method. However, in LWKF method, the grain position effect also influence the charge distribution for different device, which alter the electrostatic potential and saturation carrier velocity as in Figs. 3.13 and 3.14, result in a larger σf_T.

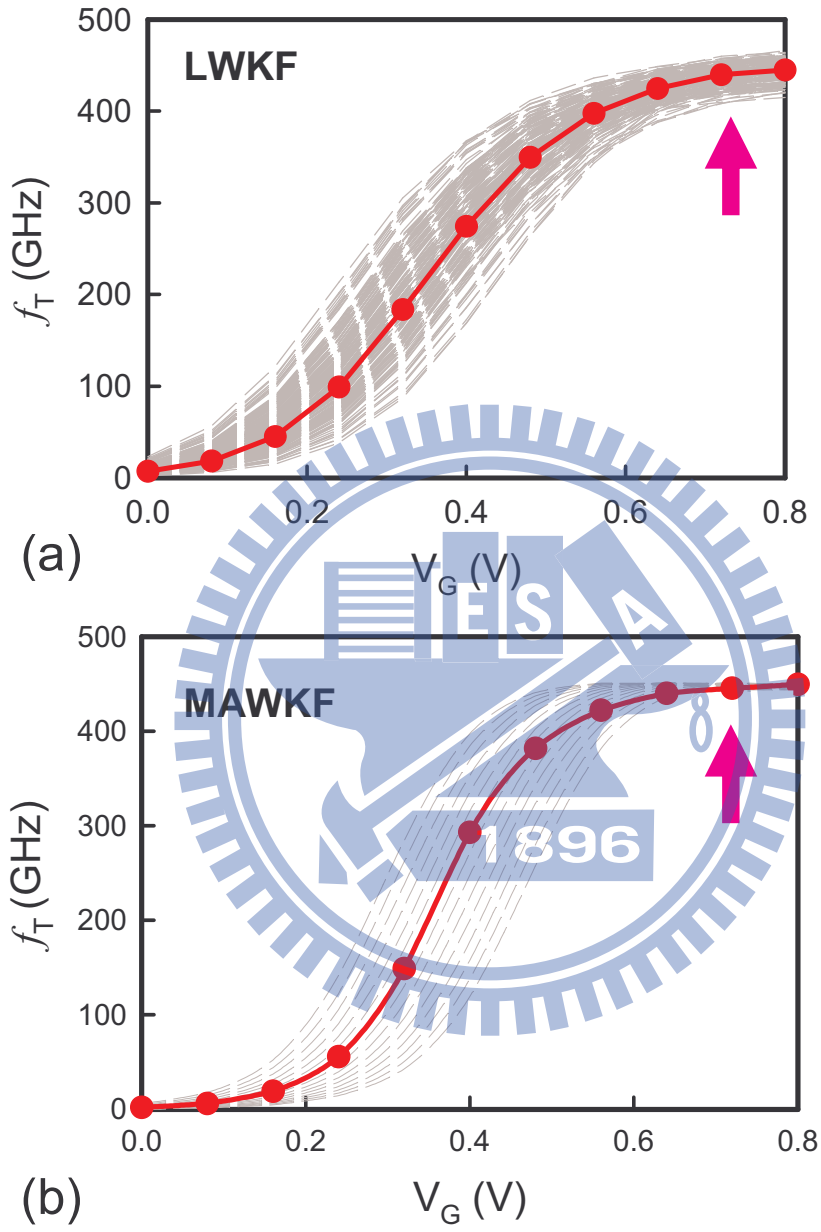


Figure 3.11: The fluctuated f_T-V_G curves with (a) localized work-function fluctuation and (b) modified averaged work-function fluctuation methods. The results are significantly different at high gate bias.

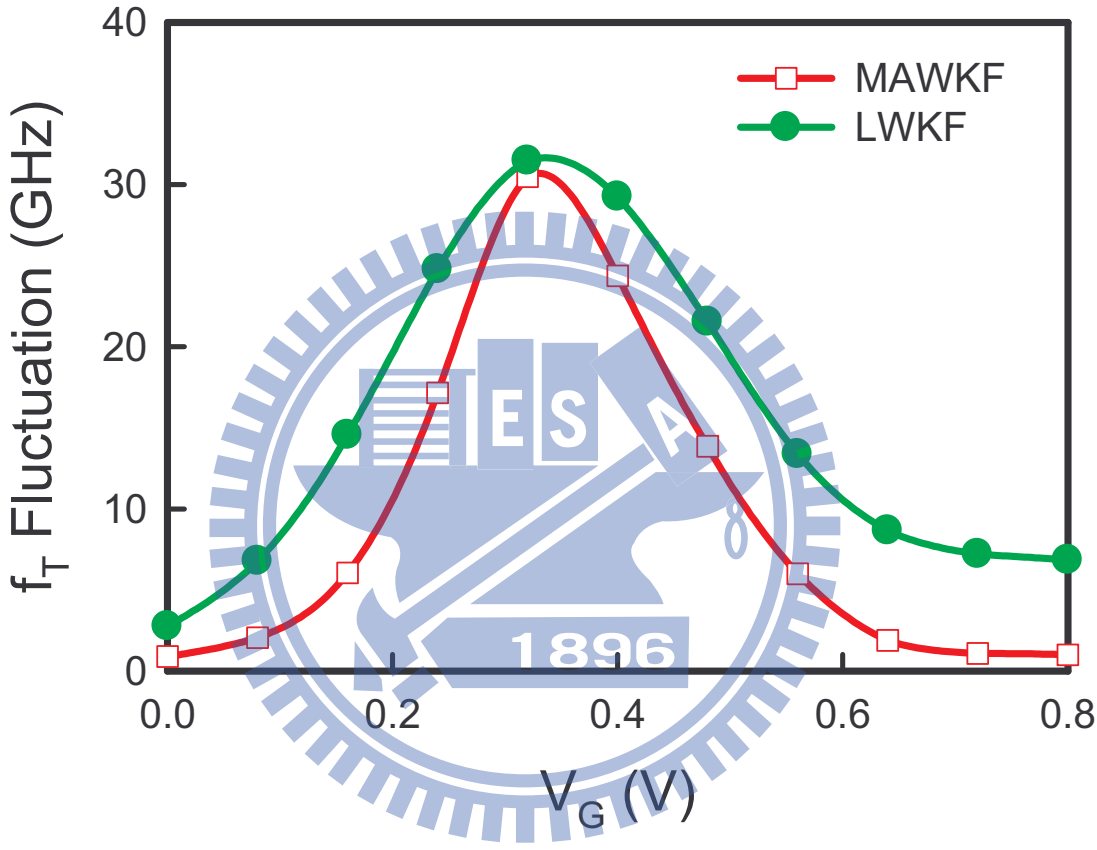


Figure 3.12: The summarized cutoff frequency fluctuations at different gate bias with modified averaged work-function fluctuation and localized work-function fluctuation method.

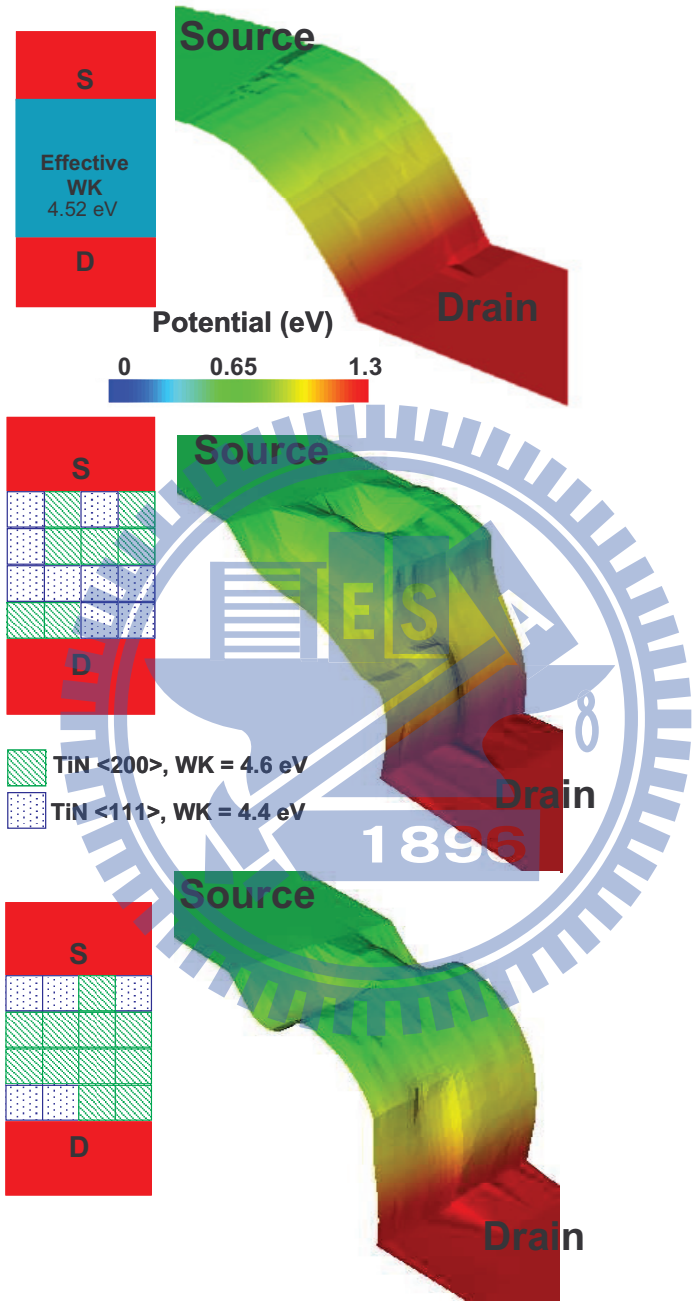


Figure 3.13: The channel surface potential distributions extracted from the devices with (a) averaged effective work-function, (b) the largest and (c) the smallest cutoff frequency in LWKF method.

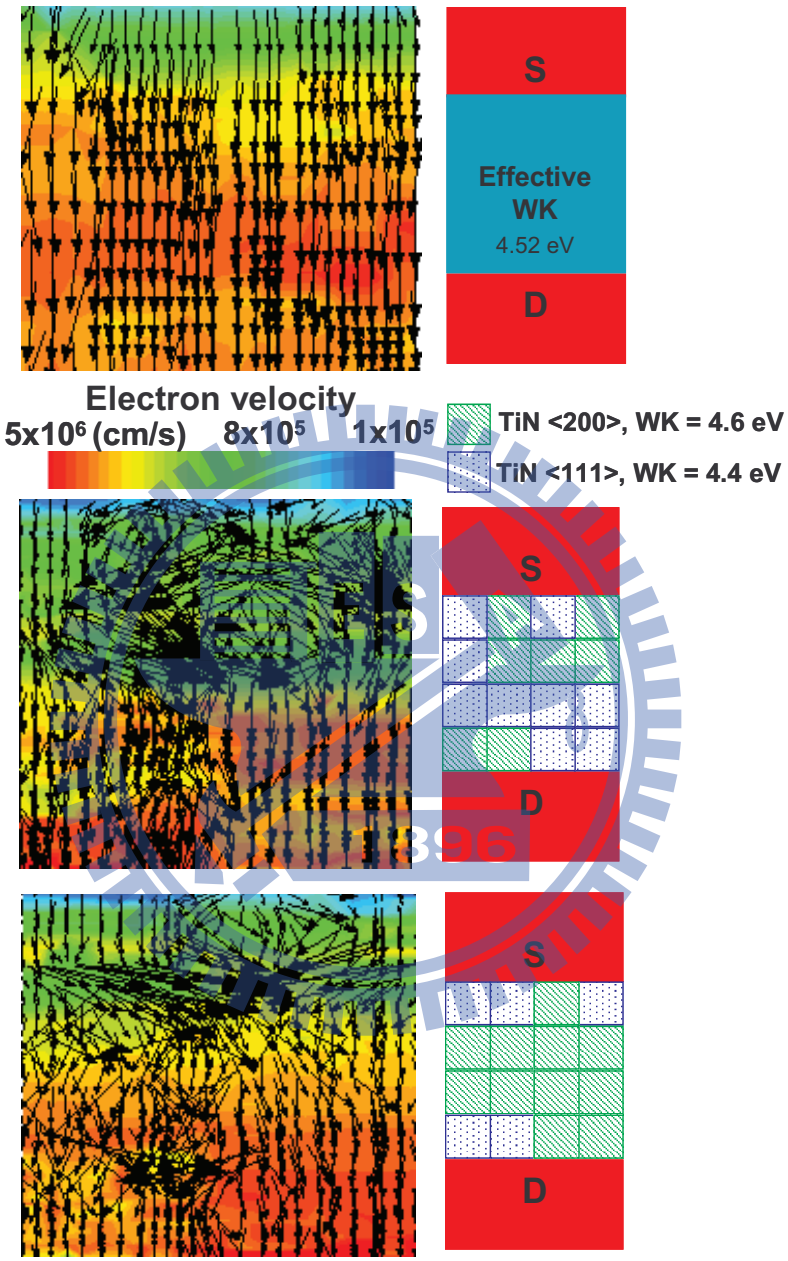


Figure 3.14: The electron velocity distributions extracted from the devices with (a) averaged effective work-function, (b) the largest and (c) the smallest cutoff frequency in LWKF method.

3.3 Summary of this Chapter

This chapter has estimated and compared the influences of the work-function fluctuations induced characteristic fluctuations in 16-nm gate planar CMOS devices with MAWKF and LWKF methods. The difference of σV_{th} with these two method are success explained by potential, charge, current, and band diagram distribution. Using the threshold voltage distribution plot, the importance of different grain position effect compare with different grain number effect is demonstrated. In device AC characteristic fluctuations, the grain position effect are also found at high gate bias. Notably, the WKF induces significantly device's DC characteristic fluctuation. However, the impact of WKF on device's AC characteristic fluctuations could be reduced at high gate voltage due to the screening effect of inversion layer of device.

Chapter 4

Circuits Characteristic Fluctuations

This chapter explores the associated device variability in the state-of-art circuits with nanoscale transistors for LWKF method. Since there are no well-established compact models for describing the behaviors of nanoscale transistors, the coupled device-circuit simulation approach which introduced in Chapter 2 is performed to ensure the best simulation accuracy. The implication of work-function fluctuation in nanoscale circuits is studied.

4.1 Digital Circuits

4.1.1 CMOS Inverter Circuit

The inverter circuit with planar MOSFETs circuit is first explored to illustrate the details of WKF in high-density integrated circuits. Figure 4.1(a) presents the input and output signal curves; the solid line represents the curve with effective metal work-function 4.52 eV and 4.76 eV for NMOS and PMOS devices, respectively. The dashed lines represent curves with fluctuations. The rising delay, falling delay, and hold time of the input signal are 2 ps, 2 ps, and 30 ps, respectively. Figures 4.1(b) and 4.1(c) display the zoom-in plots of the falling and rising transitions. The term rise time (t_r) is the time required for the output voltage (V_{out}) to rise from 10% of the logic "1" level to 90% of the logic "1", and the fall time (t_f) denotes the time required for the output voltage to fall from 90% of the logic "1" level to 10% of the logic "1" level. The low-to-high delay time (t_{LH}) and high-to-low delay time (t_{HL}) are defined as the difference between the times of the 50% points of the input and output signals during the rising and falling of the output signal, respectively. For the high-to-low transition, the NMOS device is on and starts to discharge load capacitance, causing the output signal to transit from logic "1" to logic "0". Similarly, for the low-to-high transition characteristics, the PMOS device is turned on and starts to charge the load capacitance, causing the output voltage to transit from logic "0" to logic

”1”. During the high-to-low signal transition, the output signal falls as the NMOS device is turned on. Therefore, the fluctuation of the starting points for high-to-low signal transition is determined by the V_{th} of the NMOS device. Similarly, the starting point of low to-high transition is influenced by V_{th} of PMOS device.

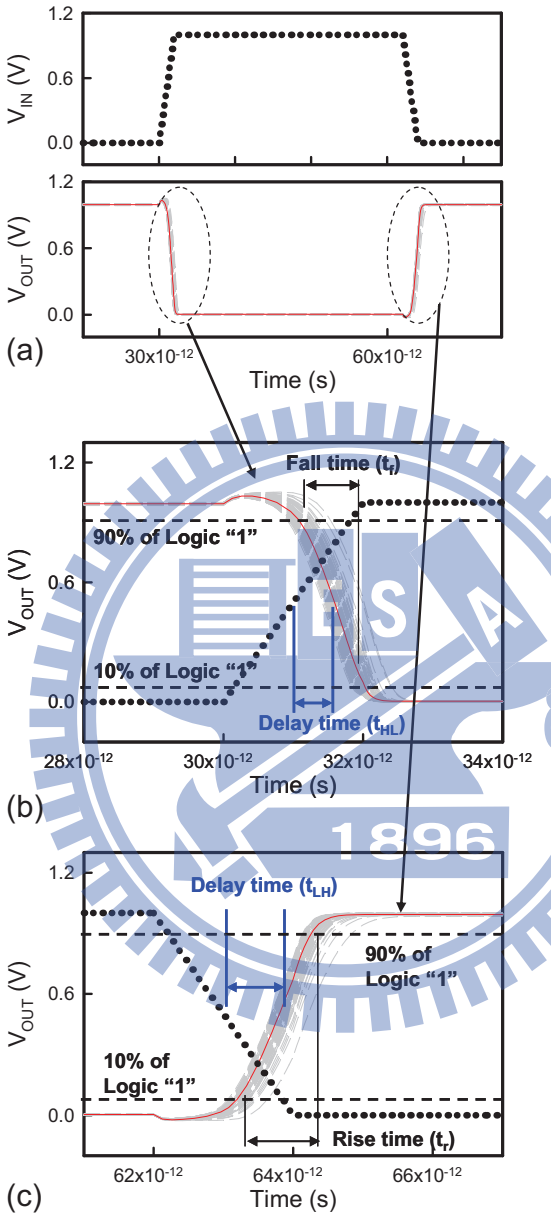
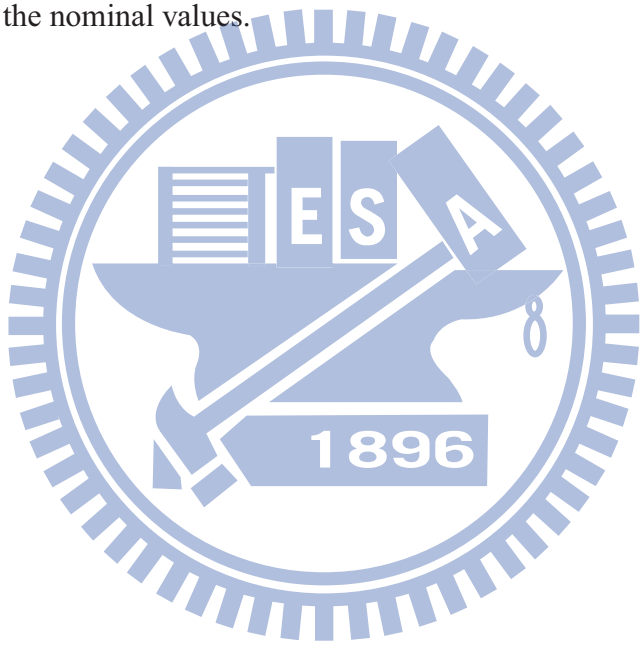


Figure 4.1: (a) The input and output signals for the fluctuated inverter. The magnified plots show (b) the falling and (c) the rising transitions, where the rise time, fall time, high-to-low delay time, and low-to-high delay time are defined.

Figure 4.2 summarizes the rise time fluctuation (σt_r), fall time fluctuation (σt_f), high-to-low delay time fluctuation (σt_{HL}) and low-to-high delay time fluctuation (σt_{LH}). The nominal values of t_f, t_{HL}, t_r, and t_{LH} are 0.8 ps, 1.25 ps, 1.04 ps, and 1.45 ps, t_f is smaller than t_r, and t_{HL} is smaller than t_{LH} due to the higher operating speed of NMOS device. The σt_f, σt_{HL}, σt_r, and σt_{LH} are 0.076 ps, 0.093 ps, 0.131 ps, and 0.165 ps, which are about 10% of the nominal values.



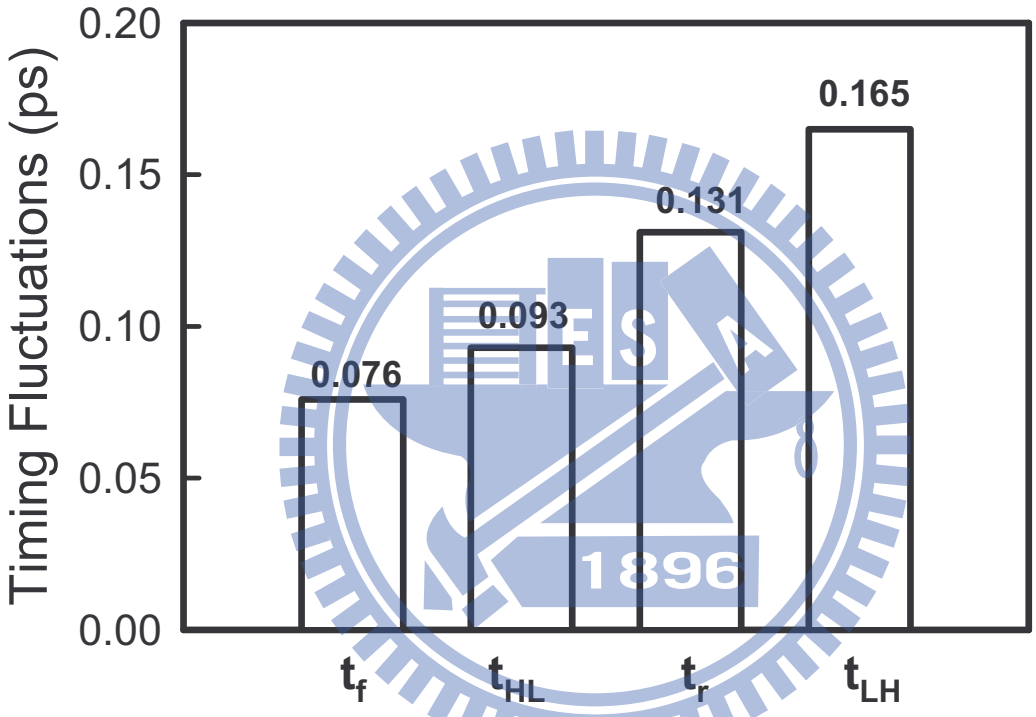


Figure 4.2: Summary of the variations of rise time, fall time, high-to-low delay time, and low-to-high delay time induced by the metal gate work-function fluctuation.

Figure 4.3 estimates the power dissipation for the studied inverter. The total power (P_{total}) is consisting of the dynamic power (P_{dyn}), the short circuit power (P_{sc}), the static power (P_{stat}). Their definitions are shown in below:

$$P_{dyn} = C_{load} V_{dd}^2 f_{0->1}, \tag{4.1}$$

$$P_{sc} = f_{0->1} V_{DD} \int_T I_{sc}(\tau) d\tau, \tag{4.2}$$

and

$$P_{stat} = V_{DD} I_{leakage}. \tag{4.3}$$

The $f_{0->1}$ is the clock rate. I_{sc} is the short circuit current, which is observed as both NMOS and PMOS devices turn on resulting a DC path between the power rails. T is the switching period. $I_{leakage}$ is the leakage current when operating at static state. The dynamic power is determined by the load capacitance, we herein use the transistors' gate capacitance as the load capacitance and focused on the device intrinsic parameter variability induced circuit variation. The short circuit power is determined by the time of existence of DC path between the power rails and the short circuit current. Since the V_{th} of devices are calibrated, the P_{sc} is then determined by the I_{sc}. The I_{sc} is dependent on the saturation current of the devices. For the static power, we determine it by the applied voltage multiply the leakage current of inverter. The P_{dyn} and P_{sc} are the dominating factors in power dissipation.

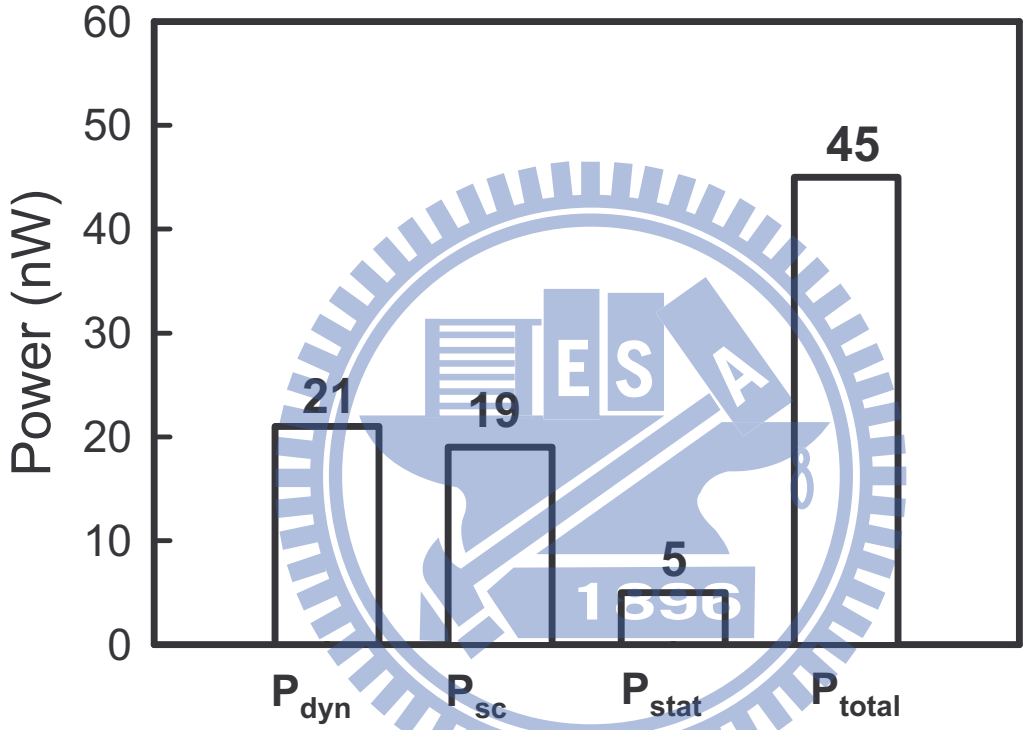


Figure 4.3: The nominal values of the inverter circuit's dynamic power, short circuit power, static power, and total power. The total power is the summation of dynamic power, short circuit power, and static power.

Figure 4.4 shows the dynamic power fluctuation (σP_{dyn}), short circuit power fluctuations (σP_{sc}), static power fluctuations (σP_{stat}), and the total power fluctuations (σP_{total} = $[(\sigma P_{dyn})^2 + (\sigma P_{sc})^2 + (\sigma P_{stat})^2]^{0.5}$) of inverter circuits with WKF. The WKF shows less impact due to the smaller gate capacitance fluctuations in σP_{dyn}. Different to the results of σP_{dyn}, the WKF start to play an important role in P_{sc} because of the significant σV_{th} induced by work-function fluctuation. Although the static power is not an important part in total power dissipation, the static power fluctuation is the largest term in the total power fluctuation due to the exponential relationship between the leakage current and V_{th}. The total power fluctuation is 5.20 nW ($0.62^2 + 3.56^2 + 3.74^2$), which is about 12% (σP_{total} / $P_{total} \times 100\%$ = 5.2 / 45 $\times$ 100%) of power consumption.

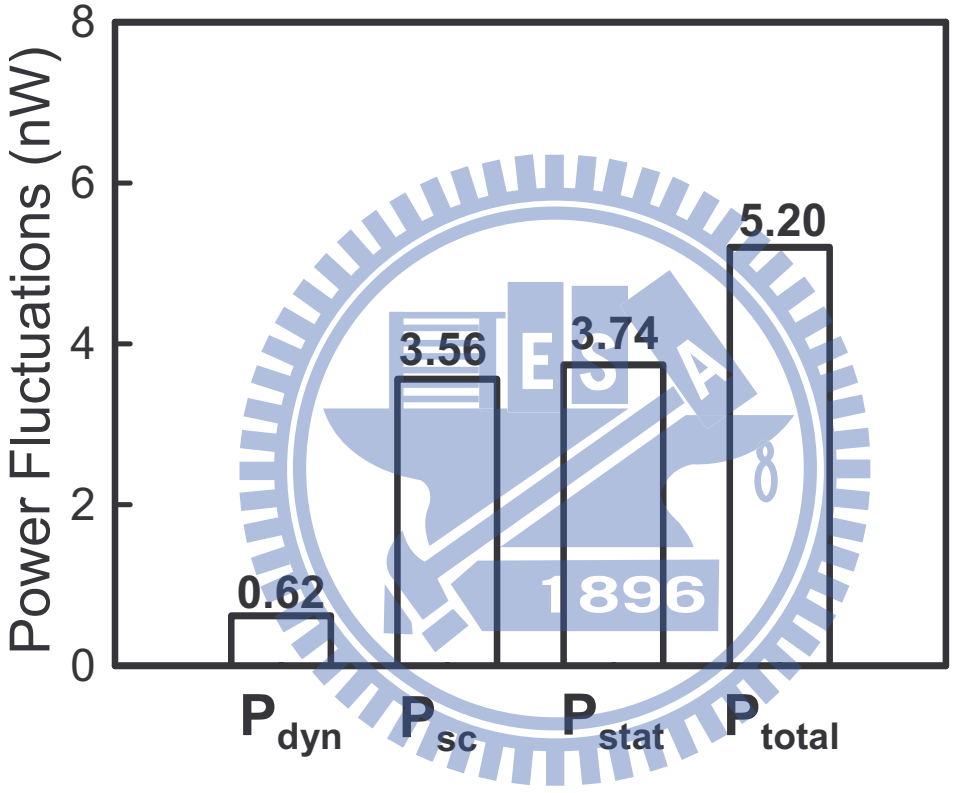


Figure 4.4: The dynamic power, short circuit power, static power, and total power fluctuations for the explored inverter with work-function fluctuation.

4.1.2 6T SRAM Circuit

The performance estimation of SRAM cell as shown in Fig. 4.5(a) is often related to the static noise margin (SNM), due to the cell is most vulnerable to noise during a read access since the ”0” storage node rises to a voltage higher than ground due to a voltage division along the access and inverter pull-down NMOS devices between the precharged bitline and the ground terminal of the cell [28-30,68-72]. There are several definitions of the static noise margin, one of the common used approach of estimating SNM is first proposed by Hill [72] and been used in this thesis. In this approach, an SRAM cell is seen as two equivalent inverters with the noise sources insert between the corresponding inputs and outputs as shown in Fig. 4.5(b). Both series voltage noise sources (V_n) have the same value and act together to upset the state of the cell. Applying the adverse noise sources polarity represents the worst-case equal noise margins [69-71]. This method is only applicable to circuits with $R_{in} >> R_{out}$, and CMOS inverters of an SRAM cell comply with this condition [70-71]. Graphically, this may be seen as moving the static characteristics vertically or horizontally along the side of the maximum nested square until the curves intersect at only one point as shown in Fig. 4.5(c) [72].

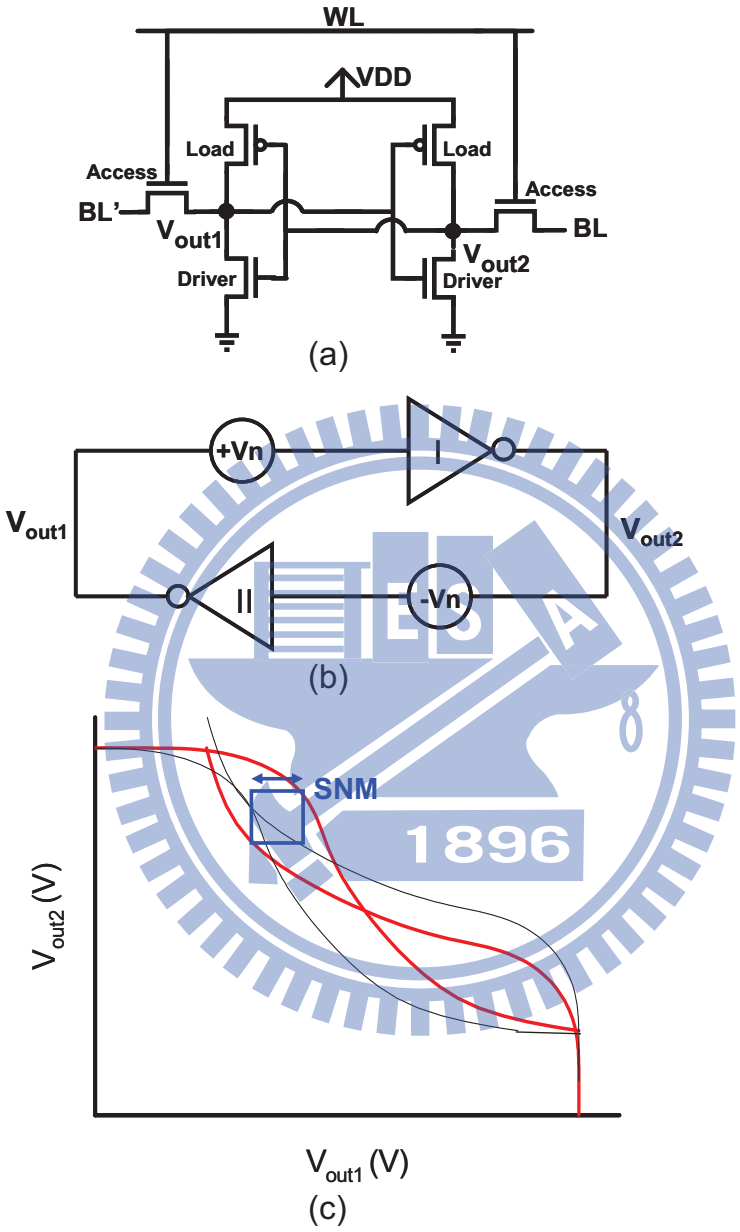
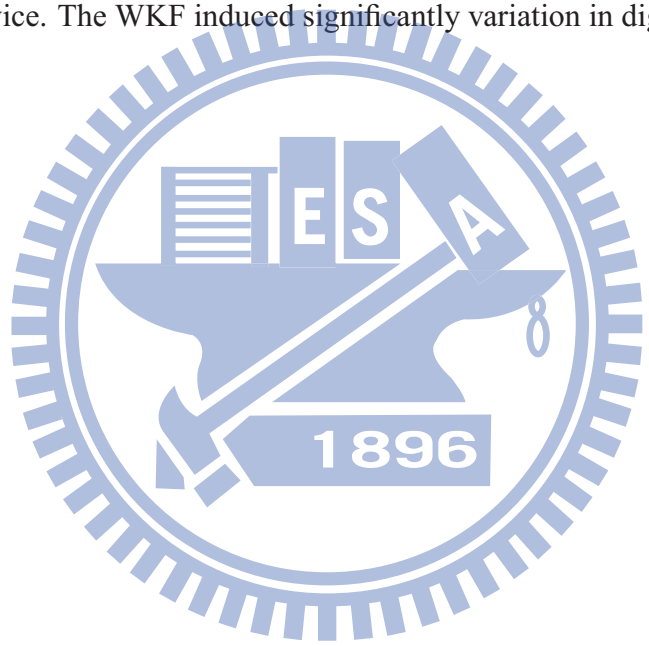


Figure 4.5: (b) The static noise margin is defined as the minimum noise voltage present at each of the cell storage nodes necessary to flip the state of the cell. (c) Graphically, this may be seen as moving the static characteristics vertically or horizontally along the side of the maximum nested square until the curves intersect at only one point [72].

Figure 4.6 shows the butterfly curves with work-function fluctuation for 16-nm-gate SRAM. The nominal butterfly curve is red symbol line and the nominal SNM is only 86 mV. The SNM fluctuation of SRAM is 25.3 mV, which is about 29% of nominal SNM value. Although the shrinking of the device size can increase the density of memory, the decreased SNM and increased SNM fluctuation are crucial issues and may limit the usage of such small device. The WKF induced significantly variation in digital circuits.



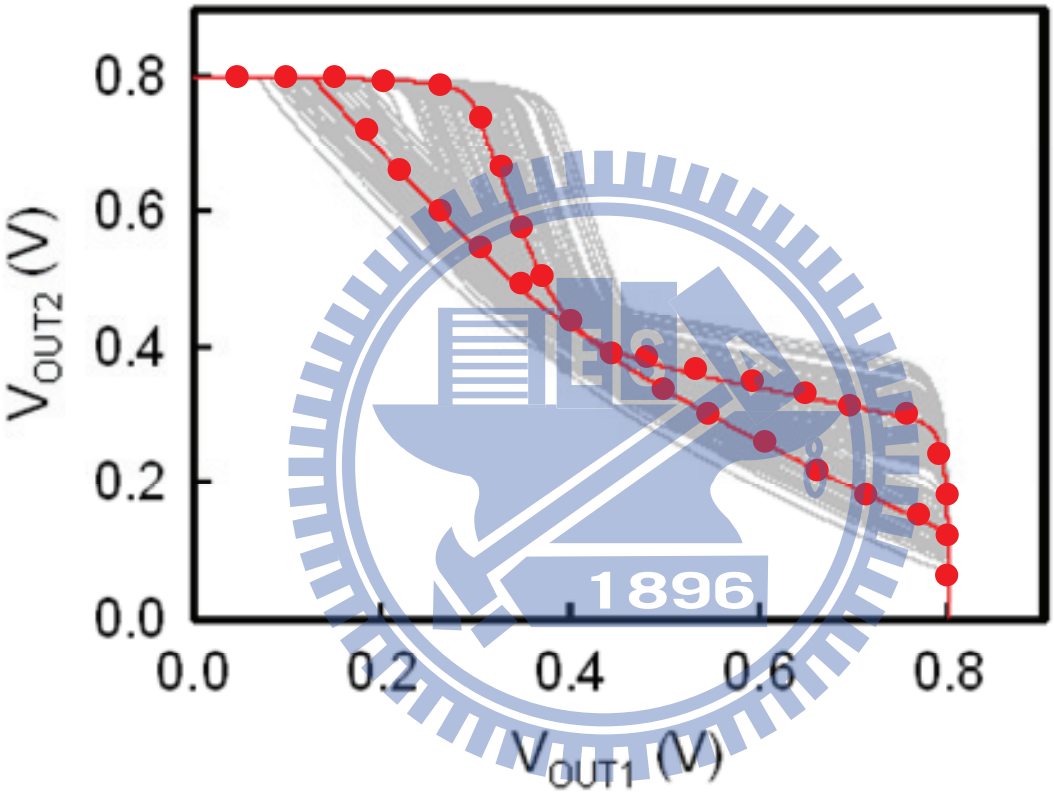


Figure 4.6: The butterfly curves of SRAM circuit with work-function fluctuation.

4.2 Analog Circuits

4.2.1 Common Source Amplifier Circuit

The common source amplifier circuit with sinusoid input wave (offset is equal to 0.5 V), as shown in Fig. 4.7, is used as a tested circuit to explore the fluctuation of high-frequency characteristics. The time-domain simulation results are simultaneously used for the calculation of the property of the frequency response, where the frequency is sweep from 1×10^{8} Hz to 1×10^{12} Hz. The common-source amplifier circuit is first explored to illustrate the details of work-function fluctuation in high-frequency circuits.

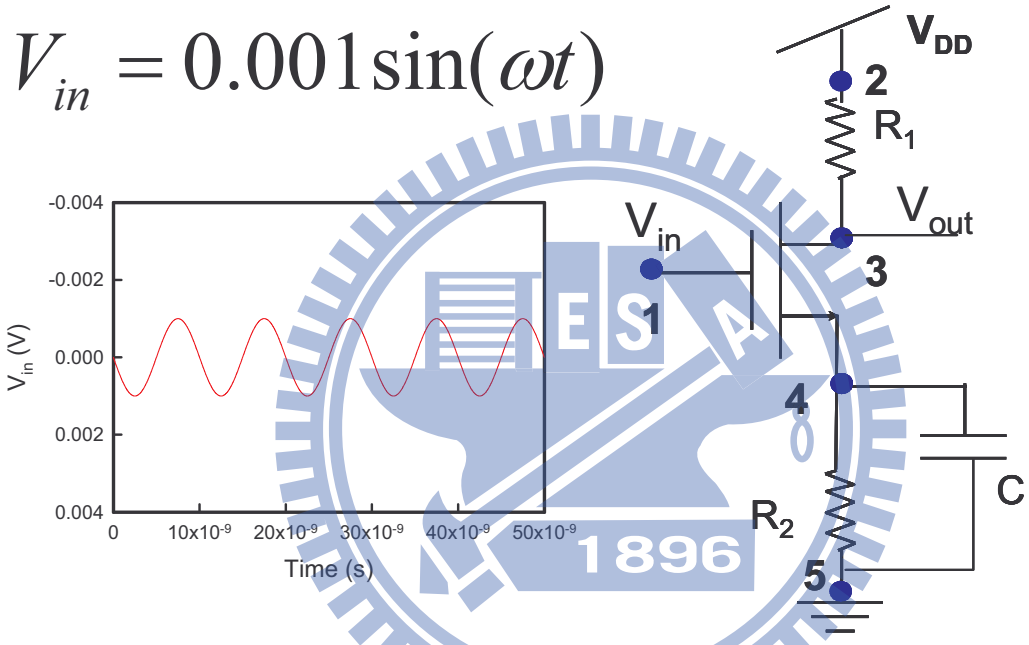


Figure 4.7: The common-source circuit is used to explore the fluctuation of high-frequency characteristics. The input signal is a sinusoid input wave with 0.5 V offset. The frequency is sweep from 1×10^{8} Hz to 1×10^{12} Hz.

Figure 4.8(a) shows the circuit gain versus operation frequency with WKF curves, where the red solid line shows the nominal device. The circuit gain, 3dB bandwidth, and unity-gain bandwidth of the nominal device are 9.3 db, 76 GHz, and 291 GHz, respectively. The corresponding high-frequency characteristic fluctuations are explored, as shown in Figs. 4.8(b). The gain of the studied circuit is proportional to g_m multiplied by output resistance of circuit. The circuit output resistance, R_{out}, is given by

$$R_{out} = \left(\frac{1}{R_1} + \frac{1}{r_o}\right)^{-1}. \tag{4.4}$$

The 3dB bandwidth and the unity-gain bandwidth fluctuations indicate the variations of switching speed resulted from work-function fluctuation. The main sources of 3dB bandwidth and the unity-gain bandwidth fluctuations contributed from device characteristics fluctuations, g_m, r_o, and C_g as shown in the inset of Figs. 4.8(b), where the g_m and r_o are calculated below:

$$g_m = \frac{\partial I_D}{\partial V_{gs}} \propto V_{GS} - V_{th}, \tag{4.5}$$

and

$$r_o = \frac{\partial V_{ds}}{\partial I_D} \propto \frac{1}{(V_{GS} - V_{th})^2}. \tag{4.6}$$

The high-frequency characteristic fluctuation of the common source amplifier circuit is less than 4%, which become less important in this analyzing skeleton. The results are similar to the device AC characteristic fluctuations.

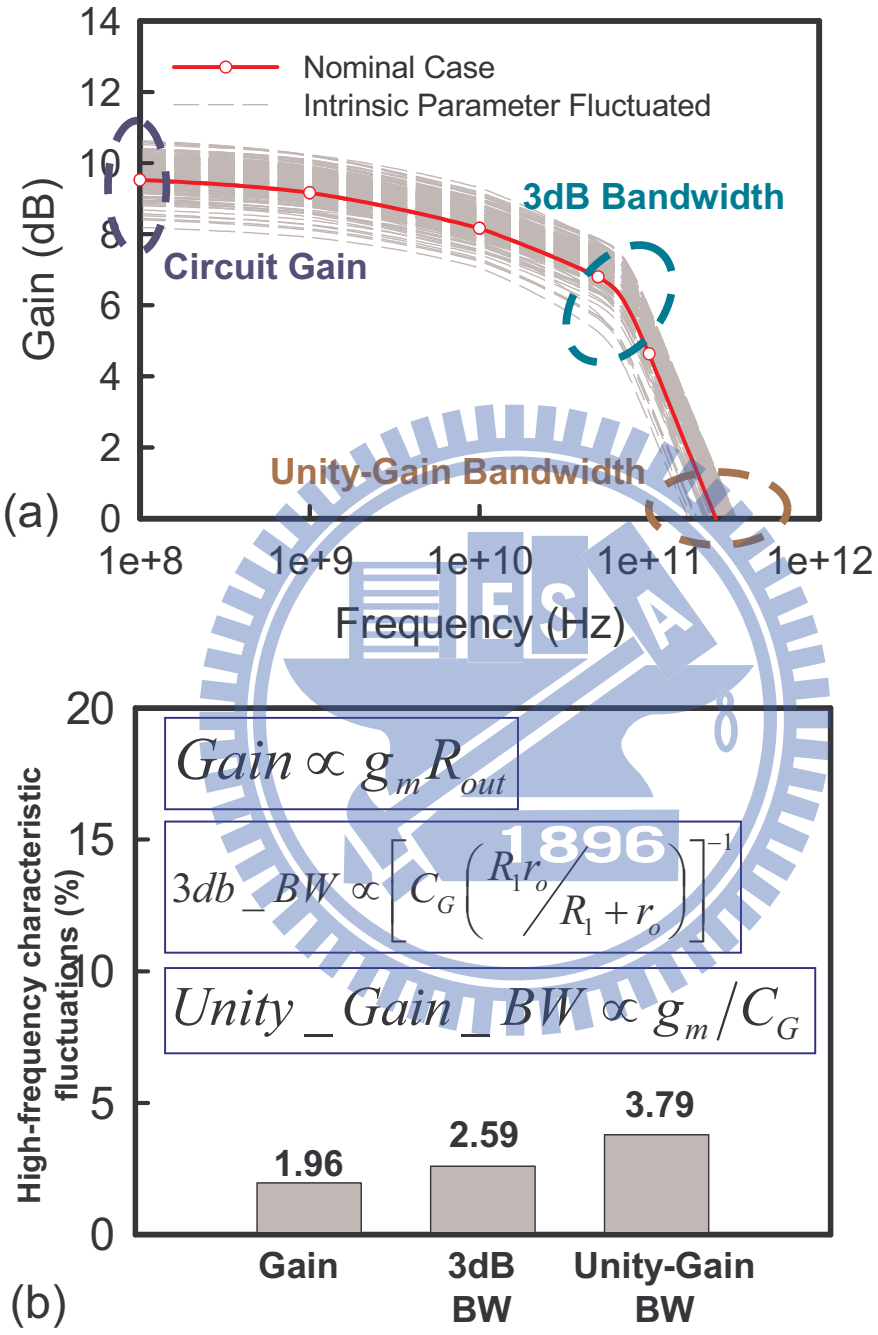


Figure 4.8: The (a) frequency response and (b) summarized high-frequency circuit gain, 3dB bandwidth, and unity-gain bandwidth fluctuations induced by work-function fluctuation. The relation between device and circuit characteristics are shown in the inset.

4.2.2 Current Mirror Circuit

The current mirrors which shown in Fig. 4.9 are basic and critical circuit in analog integrate circuit. For current mirror design, the match of transistor pair is important. The mismatch of device influence the reference current and output current value and result in the variation of circuit operation. The analytical formula for the ratio of reference current and output current is expressed as below:

$$(\frac{I_{REF}}{I_{OUT}}) = \frac{\frac{1}{2}\mu_{n,M1}C_{ox,M1}\frac{W_{M1}}{L_{M1}}[V_{GS1}-(V_{th,M1})]^2}{\frac{1}{2}\mu_{n,M2}C_{ox,M2}\frac{W_{M2}}{L_{M2}}[V_{GS2}-(V_{th,M2})]^2}, \tag{4.7}$$

where the $\mu'_{n,M1}$, $C'_{ox,M1}$, W_{M1}, L_{M1}, V_{GS1}, $V_{th,M2}$, and $\mu'_{n,M2}$, $C'_{ox,M1}$, W_{M2}, L_{M2}, V_{GS2}, $V_{th,M2}$ are the parameters of transistors M1 and M2. If M1 and M2 is matched, the corresponding values are the same, the current ratio is 1. However, these parameters will be different for each device if considering device intrinsic parameter fluctuation. Here we assume μ'_n, C'_{ox}, W, L, and V_{GS} are constant with respect to work-function fluctuation, the only term which affects the current mismatch is the threshold voltage fluctuation. To investigate the current mismatch, we define the normalized I_{OUT} fluctuation:

$$Normalized \quad I_{OUT} \quad fluctuation(\%) = \frac{\sigma(I_{REF}-I_{OUT})}{I_{REF}} \times 100\%, \tag{4.8}$$

where the I_{REF} and I_{OUT} are the reference and output currents, as shown in Fig. 4.9. In Fig. 4.10, the WKF induces about 8% normalized I_{OUT} fluctuation due to the drain current of transistor is strongly relative to threshold voltage.

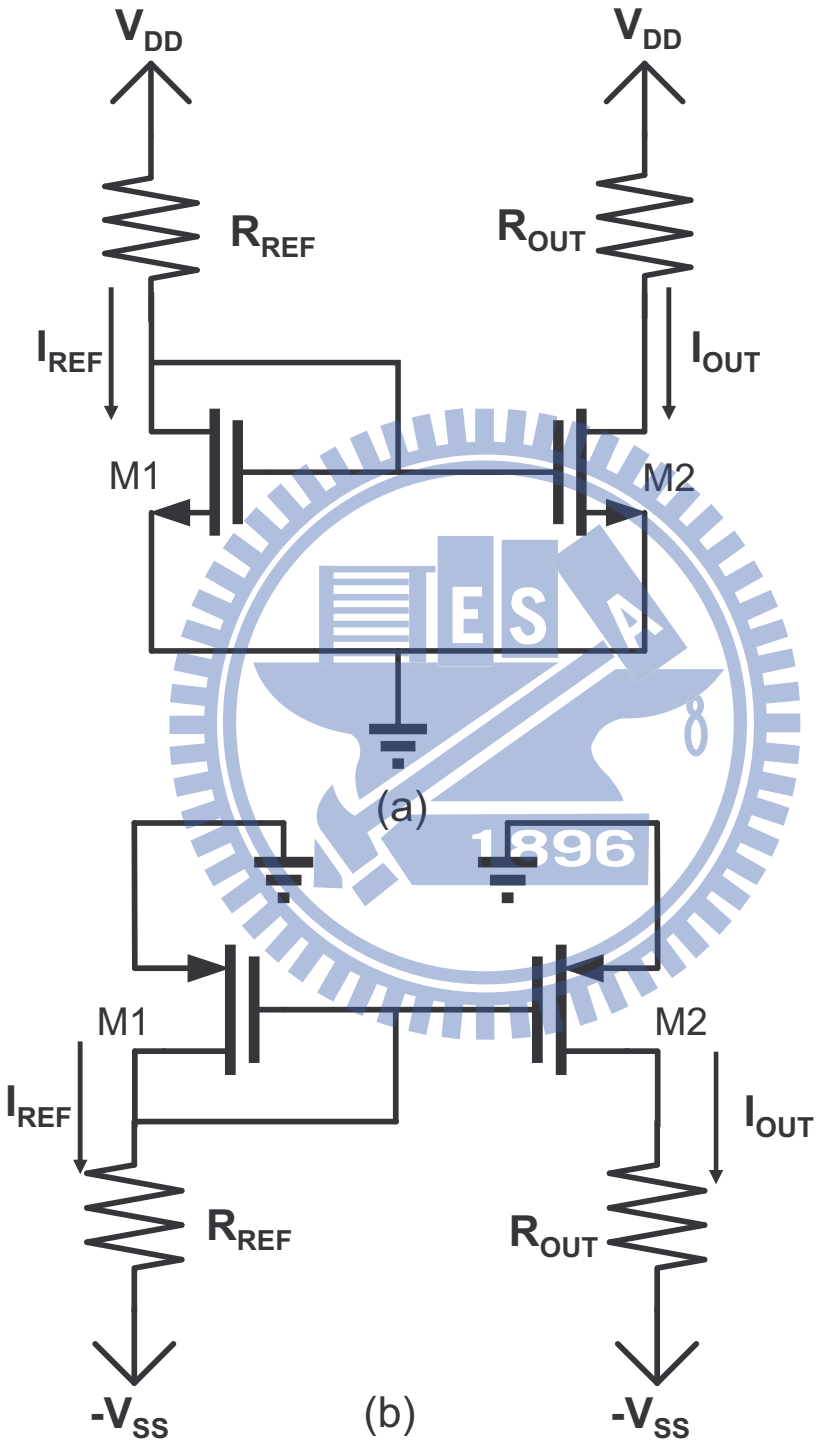


Figure 4.9: The (a) NMOS and (b)PMOS current mirror circuits used in this work.

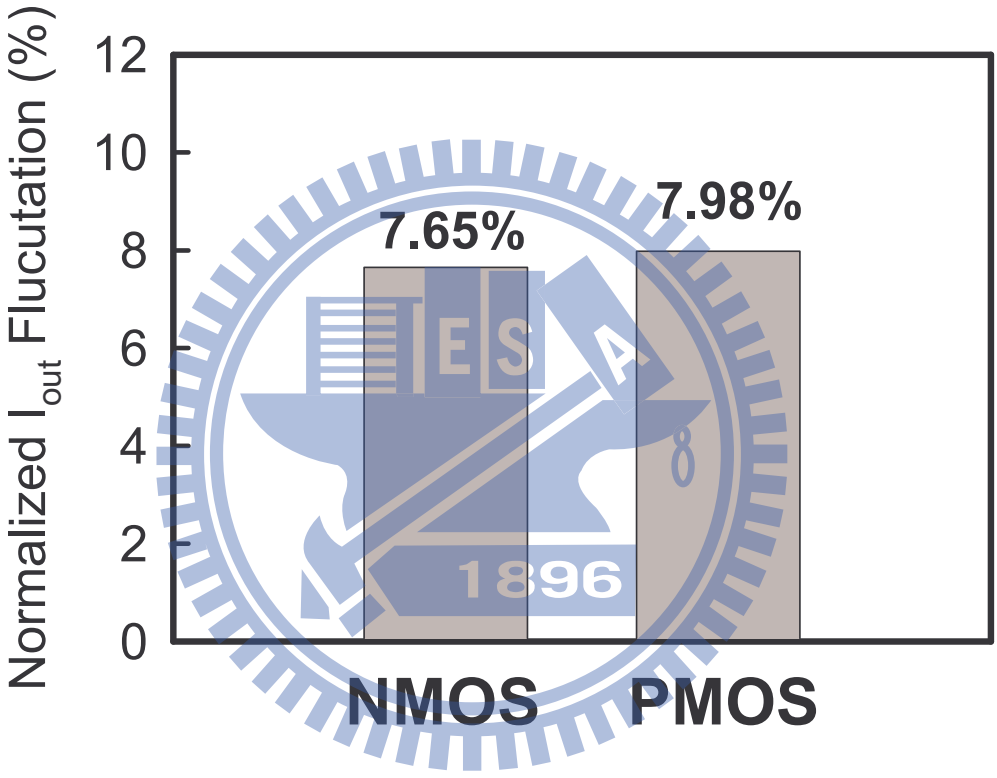


Figure 4.10: The summarized normalized I_{OUT} fluctuations induced by work-function fluctuation for NMOS and PMOS current mirrors.

4.3 Summary of this Chapter

This chapter has estimated the influences of the work-function fluctuation in 16-nm nanoscale circuits. The WKF significantly affect the device threshold voltage fluctuation; and therefore impact the timing of inverter circuit, static noise margin of SRAM circuit, and current mismatch of current mirror circuit. The fluctuations of rise time, fall time, and delay time fluctuations follow the trend of V_{th} fluctuation. The power fluctuations consisting of dynamic power, short circuit power, and static power have been estimated. The dynamic power and short circuit power are the most important power dissipation sources. However, the static power fluctuation dominates the total power fluctuation due to the exponential relationship between the leakage current and the V_{th}. For current mirror, the circuit performance variability caused by device mismatch is also clearly shown. For SRAM, static noise margin fluctuations have been explored and the WKF brings significant variations. For the high frequency characteristics of common source amplifier, the circuit gain, 3dB bandwidth, and unity-gain bandwidth have been explored. Similar to the trend of the device AC characteristics, the WKF shows less impact on high frequency characteristic owing to the small gate capacitance fluctuation. It is necessary to include the WKF effects in studying digital circuit reliability; however, for high frequency applications, the influence of WKF may neglect.

Chapter 5

The Total Effects of All Fluctuations

The random dopant fluctuation (RDF) and process variation effect (PVE) are important variation sources of state-of-art CMOS device [7-45]. It is necessary to compare the WKF with RDF and PVE. This chapter investigates and compares the characteristic fluctuations induced by RDF, PVE, and WKF for CMOS devices and circuits, then the dominant fluctuation sources are identified.

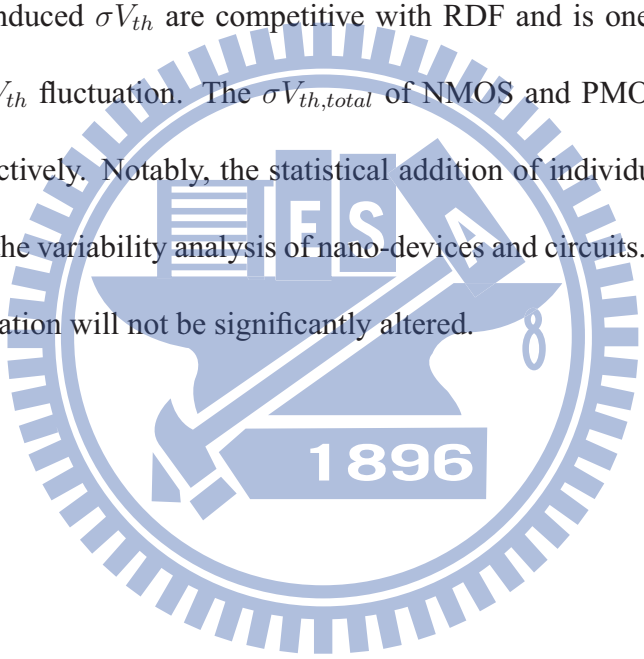
5.1 Device Characteristics

The RDF-, PVE-, and WKF-fluctuated V_{th} of CMOS devices are first explored. Figure 5.1 shows the σV_{th} induced by RDF, PVE, and WKF. The total V_{th} fluctuation ($\sigma V_{th,total}$)

is given by according to the independency of the fluctuation components:

$$(\sigma V_{th,total})^2 \approx (\sigma V_{th,RDF})^2 + (\sigma V_{th,PVE})^2 + (\sigma V_{th,WKF})^2 , \tag{5.1}$$

where the $\sigma V_{th,RDF}$, $\sigma V_{th,PVE}$, and $\sigma V_{th,WKF}$, are the random-dopant-induced, process-variation-induced, and work-function-fluctuation-induced V_{th} fluctuation, respectively. The results show that WKF induced σV_{th} are competitive with RDF and is one of the major variation sources of the V_{th} fluctuation. The $\sigma V_{th,total}$ of NMOS and PMOS devices are 63 mV and 66 mV, respectively. Notably, the statistical addition of individual fluctuation sources herein simplifies the variability analysis of nano-devices and circuits. However, the dominant source of fluctuation will not be significantly altered.



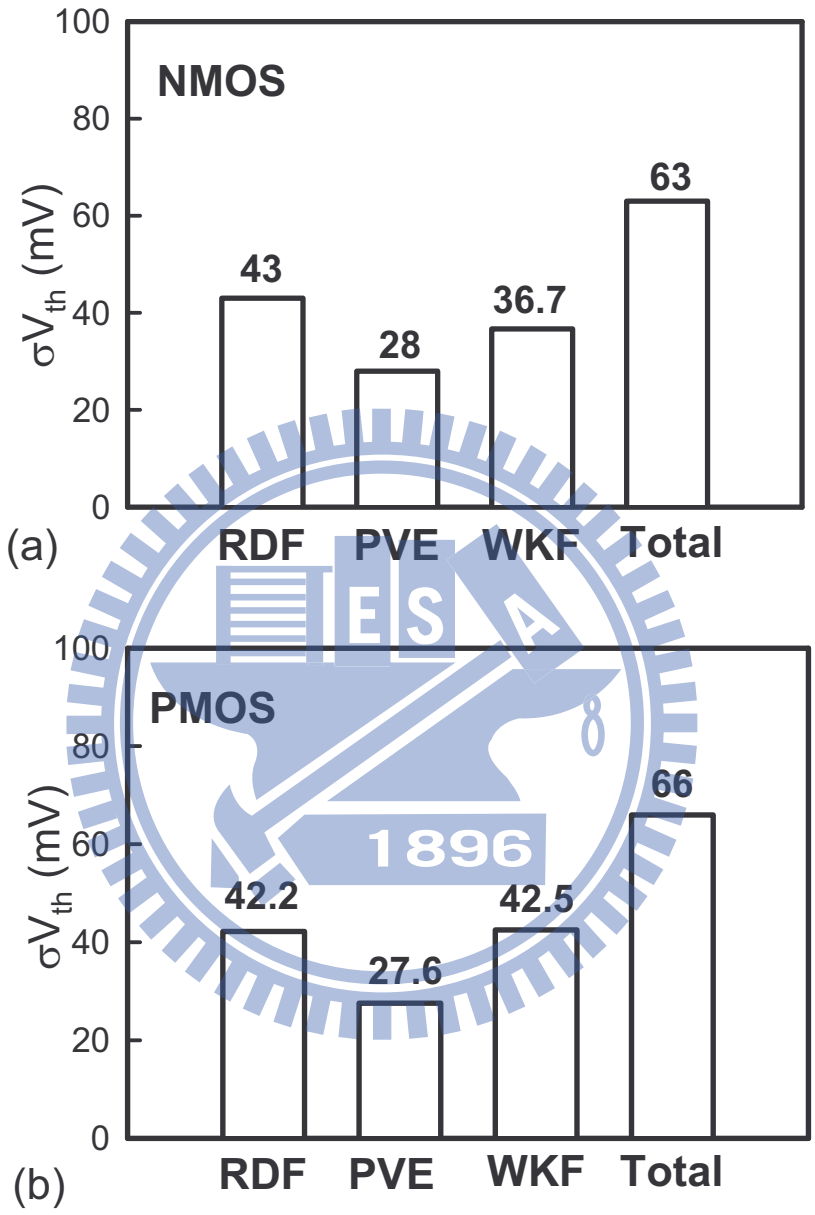


Figure 5.1: The summarized threshold voltage fluctuations for (a) NMOS and (b) PMOS devices, respectively.

The RDF-, PVE-, and WKF-fluctuated C_G with different gate bias are compares in Fig 5.2 for NMOS and PMOS devices. The different intrinsic parameter variability induced rather different C-V characteristics. Different to the results of V_{th} fluctuation, the WKF brought less impact on gate capacitance fluctuation. At low gate bias or negative gate bias, the accumulation layer screens the impact of RDF and WKF. The capacitive response is then dominated by increment of inversion in the moderate inversion. The device characteristics are then impacted by intrinsic parameter fluctuated electrostatic potentials. The RDF is the largest variation source at this bias condition. If the high V_G is achieved, the capacitive response becomes dominated by the inversion layer, the impact of the individual dopant or metal grain on the device electrostatics is screened by the inversion layer itself. The impact of RDF- and WKF-induced electrostatic potential variations is therefore bringing less impact on channel surface. The PVE dominates the gate capacitance fluctuations at all gate bias conditions due to PVE brings direct impact on gate length and therefore influences the gate capacitance. The PVE induced gate capacitance fluctuation is independent of screening effect and should be noticed when the transistor operated in high gate bias.

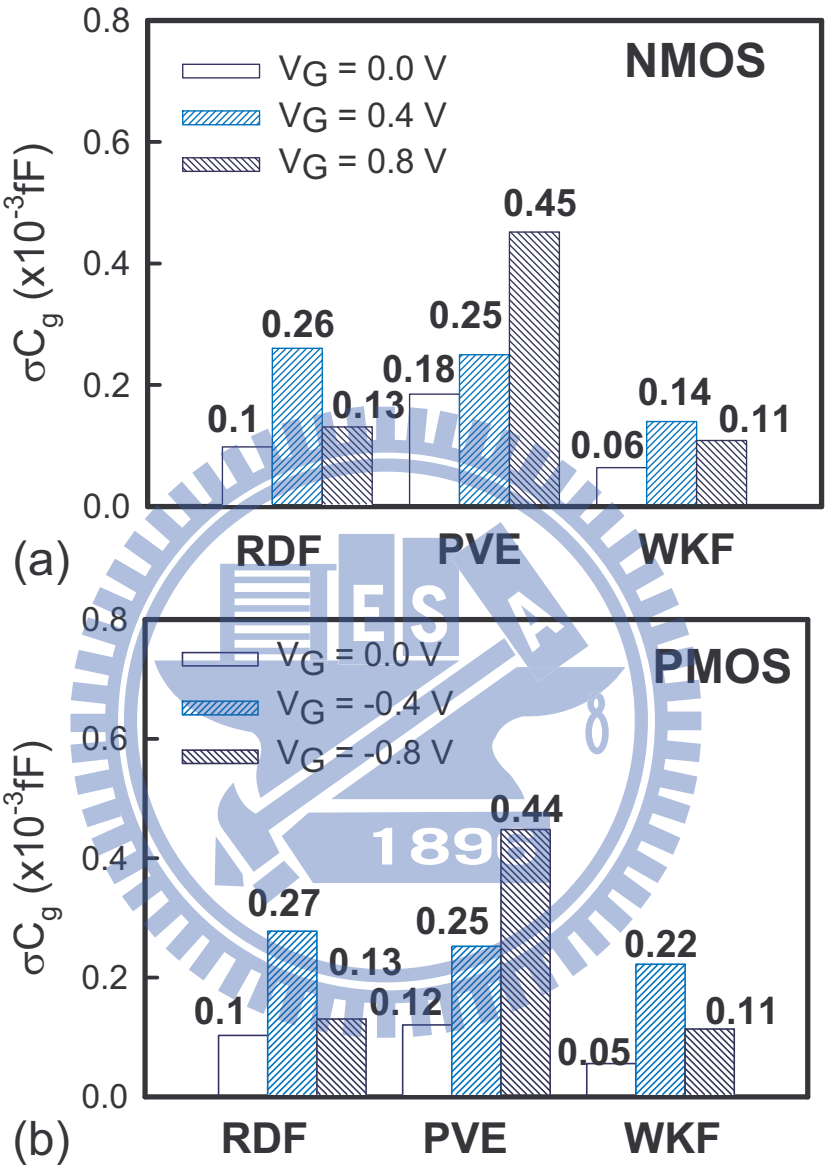


Figure 5.2: The summarized gate capacitance fluctuations at different gate bias for (a) NMOS and (b) PMOS devices, respectively.

Figures 5.3(a) and 5.3(b) show the cutoff frequency ($f_T = v_{sat} / 2\pi L_g = g_m / 2\pi C_G$) fluctuations versus the gate voltage for NMOS and PMOS devices, respectively. The results show that RDF play the dominating factor in the σf_T at low gate bias, and PVE become the most important parameter when the transistors operate at high gate bias. For RDF, similar to the threshold voltage and gate capacitance fluctuations, it is reduced at high gate bias; however, the carrier-impurity scattering alters the saturation velocity at high gate bias (high-field); therefore σf_T does not diminish in high-field region. The trend of WKF induced σf_T is similar to the RDF, it is larger at low gate bias and reduced at high gate bias; however, the impact of WKF on σf_T is insignificant. The PVE-induced σf_T is increase with gate bias increased owing to the direct influence of gate length on gate capacitance and PVE become dominates σf_T as V_G larger than 0.6V due to the screening effect in RDF and WKF fluctuations.

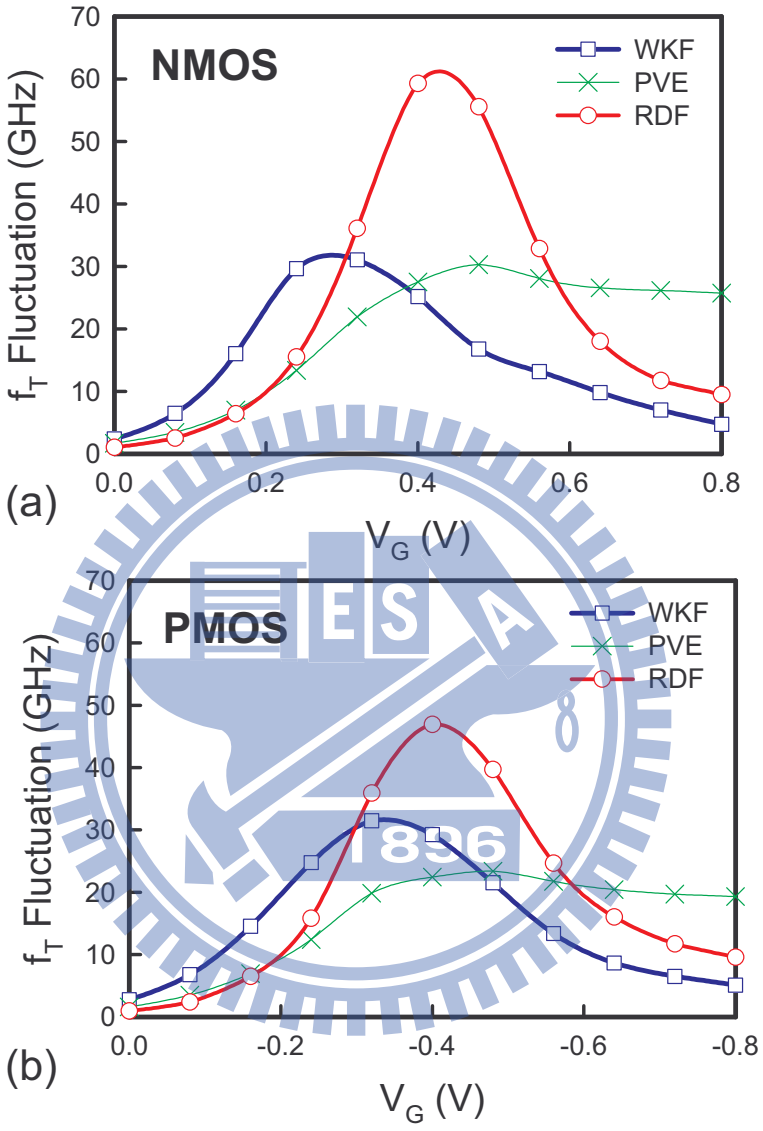


Figure 5.3: The summarized cutoff frequency fluctuations as a function of gate bias for (a) NMOS and (b) PMOS devices, respectively.

5.2 Circuits Characteristics

The impact of emerging metal gate work-function fluctuation compare with random dopant fluctuation and process variation effect on device reliability has been discovered and discussed in the previous section. This section then explores the associated device variability in the state-of-art circuits. The dominant fluctuation sources in each circuit characteristics are found and discussed.

5.2.1 CMOS Inverter Circuit

Figures 5.4(a) - 5.4(d) compare the t_r, t_f, t_{HL} and t_{LH} fluctuations. The t_f and t_{HL} are dependent on the V_{th} fluctuations of NMOS device, and t_r and t_{LH} are dependent on the V_{th} fluctuations of PMOS device. According to the results of Fig. 5.1, the RDF and WKF are the dominating factors in digital timing fluctuations.

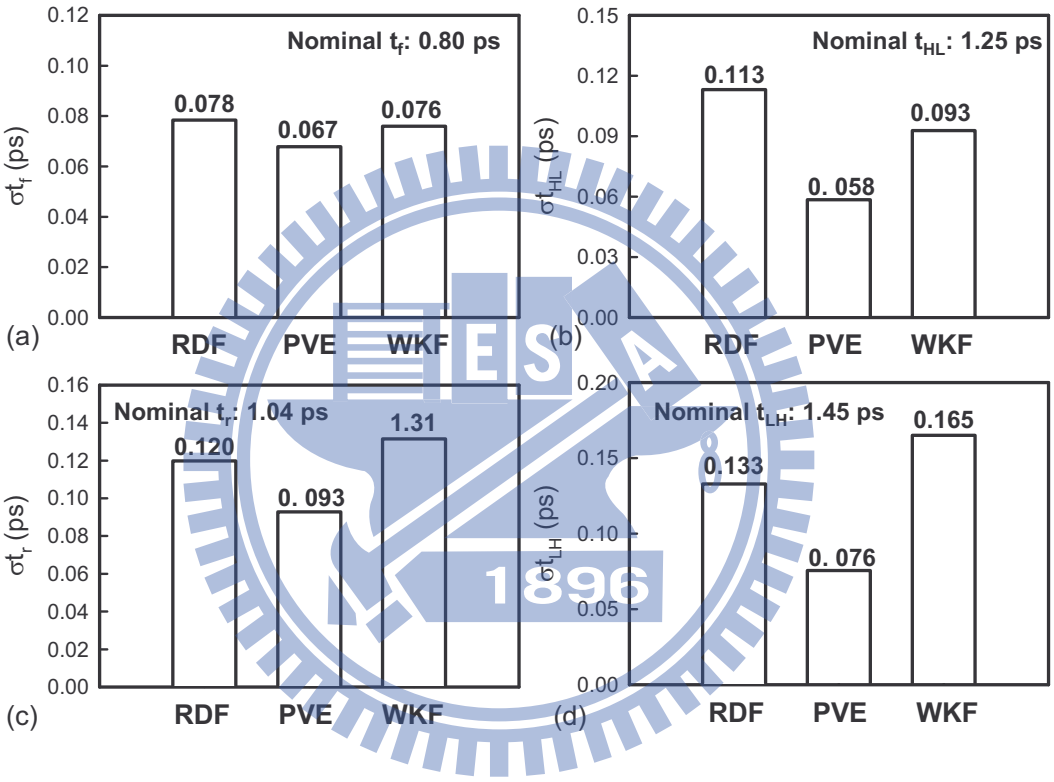


Figure 5.4: Comparison of the variations of (a) fall time, (b) high-to-low delay time, (c) rise time, and (d) low-to-high delay time with respect to RDF, PVE, and WKF.

Figure 5.5(a) shows the σP_{dyn} of inverter circuits with RDF, PVE, and WKF. The RDF and PVE dominate the dynamic power fluctuation; additionally, the WKF shows less impact due to the smaller gate capacitance fluctuations. Figure 5.5(b) displays σP_{sc} for the studied inverter circuits. Different to the results of σP_{dyn}, the WKF start to play an important role in σP_{sc} because of the significant σV_{th} induced by work-function fluctuation. Figure 5.5(c) summarizes the σP_{stat}. Since the σP_{stat} is related to the device leakage current fluctuation, the RDF and WKF dominant the σP_{stat} due to the induced larger σV_{th}. The inverter power fluctuations ($\sigma P_{inverter} = [(\sigma P_{PVE})^2 + (\sigma P_{WKF})^2 + (\sigma P_{RDF})^2]^{0.5}$) are summarized in Fig 5.5(d). The P_{stat} is one of the major sources of the power fluctuation and the RDF and WKF are the dominating factors in power fluctuation of CMOS inverter. The inverter power fluctuation is 8.09 nW ($5.23^2 + 3.32^2 + 5.20^2$), which is about 18% ($\sigma P_{inverter}$ / P_{total} $\times$ 100% = 8.09 / 45 $\times$ 100%) of power consumption and may bring significant impacts on the reliability of circuits, such as temperature and timing.

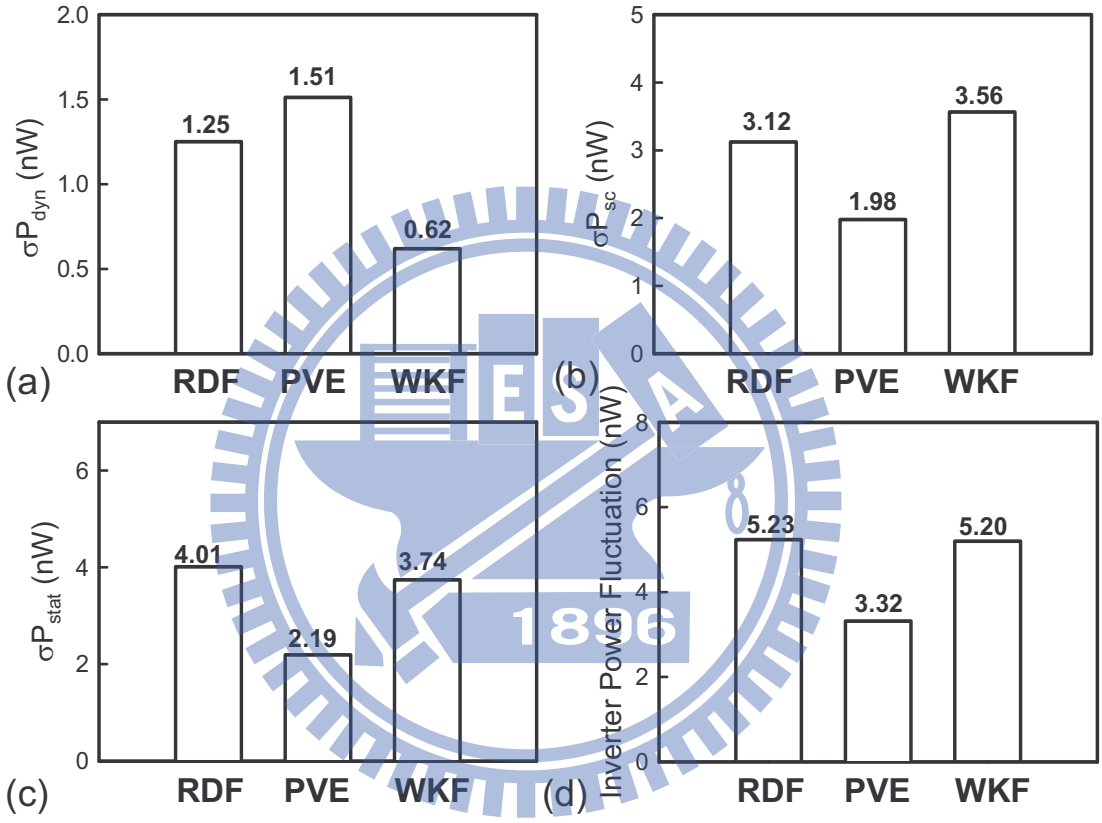


Figure 5.5: The (a) dynamic power, (b) short circuit power, (c) static power, and (d) inverter power fluctuations for the explored inverter with RDF, PVE, and WKF.

5.2.2 6T SRAM Circuit

Figure 5.6 summarizes the SNM fluctuations for 16-nm-gate SRAM, in which the nominal SNM is only 86 mV. Since the RDF and WKF induce larger device variability in threshold voltage, the SNM fluctuations of SRAM are thus dominated by RDF and WKF, which are 32% and 29%, respectively. The results are also similar to the results of device σV_{th}, the RDF and WKF are dominating sources.

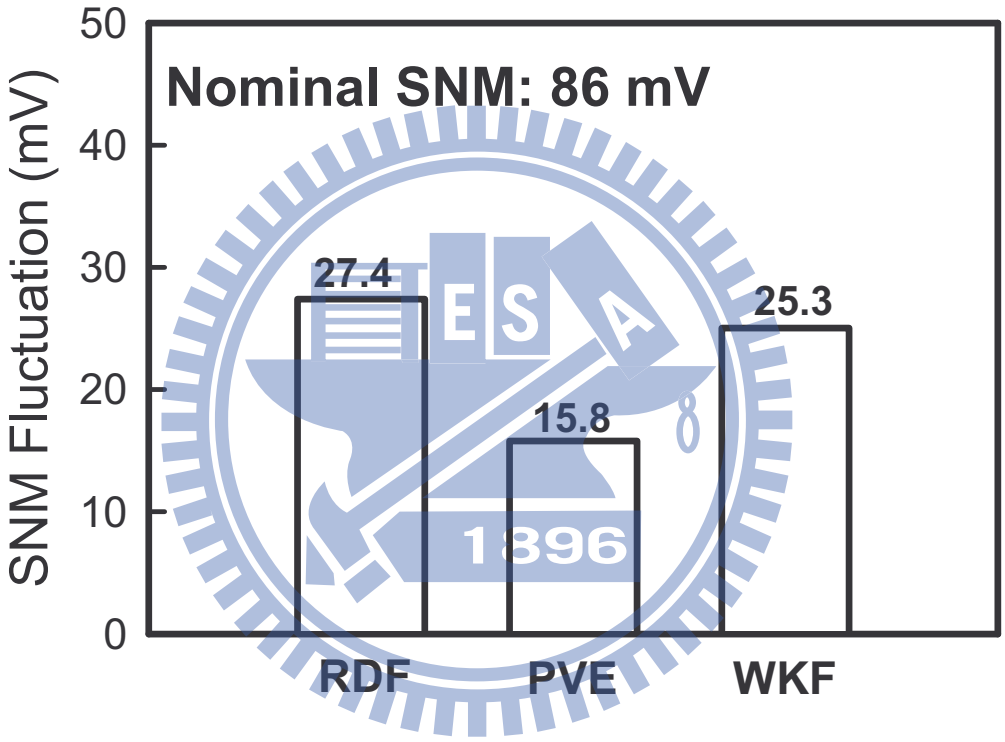


Figure 5.6: The summarized static noise margin fluctuation induced by RDF, PVE, and WKF.

5.2.3 Common Source Amplifier Circuit

Figure 5.7(a) shows the circuit gain versus operation frequency, where the solid line shows the nominal device. The circuit gain, 3dB bandwidth, and unity-gain bandwidth fluctuations are explored, as shown in Figs. 5.7(b) -(d), where the insets show the trend of circuit gain, 3dB bandwidth, and unity-gain bandwidth as a function of device characteristic and circuit element. The gain of the studied circuit is proportional to g_m multiplied by output resistance of circuit. The 3dB bandwidth and the unity-gain bandwidth of the common source amplifier circuit indicate the variations of switching speed. The insets of Figs. 5.7(c) and (d) show the main sources of variations contributed from device characteristics fluctuations, g_m, r_o, and C_G. Similar to the cutoff frequency fluctuation of NMOS device at the same gate bias, the high-frequency characteristic fluctuation of the common source amplifier circuit is dominated by RDF and PVE, and WKF become less important in this analyzing skeleton.

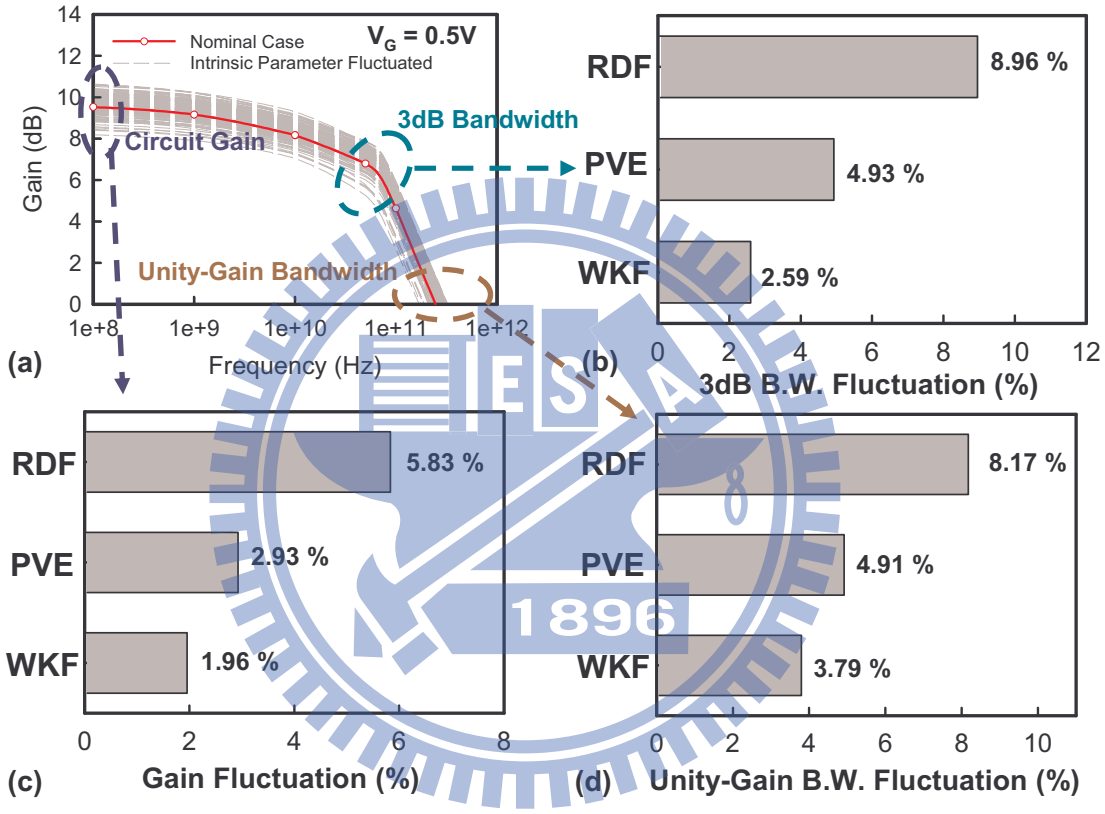
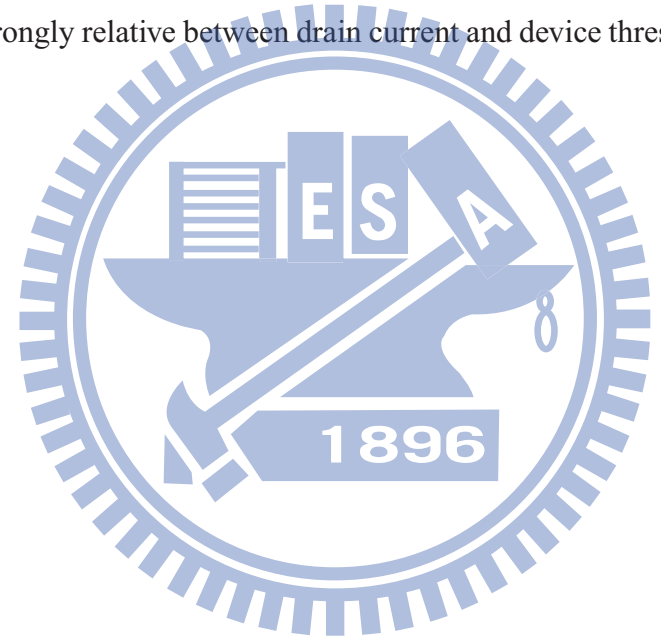


Figure 5.7: The (a) frequency response, (b) 3dB bandwidth, (c) high-frequency circuit gain, and (d) unity-gain bandwidth fluctuations induced by RDF, PVE, and WKF.

5.2.4 Current Mirror Circuit

The mismatch of device influence the reference current and output current value and result in the variations of circuit operation of current mirror circuits. We compare WKF with RDF and PVE induced normalized I_{OUT} fluctuation. The RDF and WKF are the major variation sources of current mismatch, and the results are similar to the results of device σV_{th} due to the strongly relative between drain current and device threshold voltage.



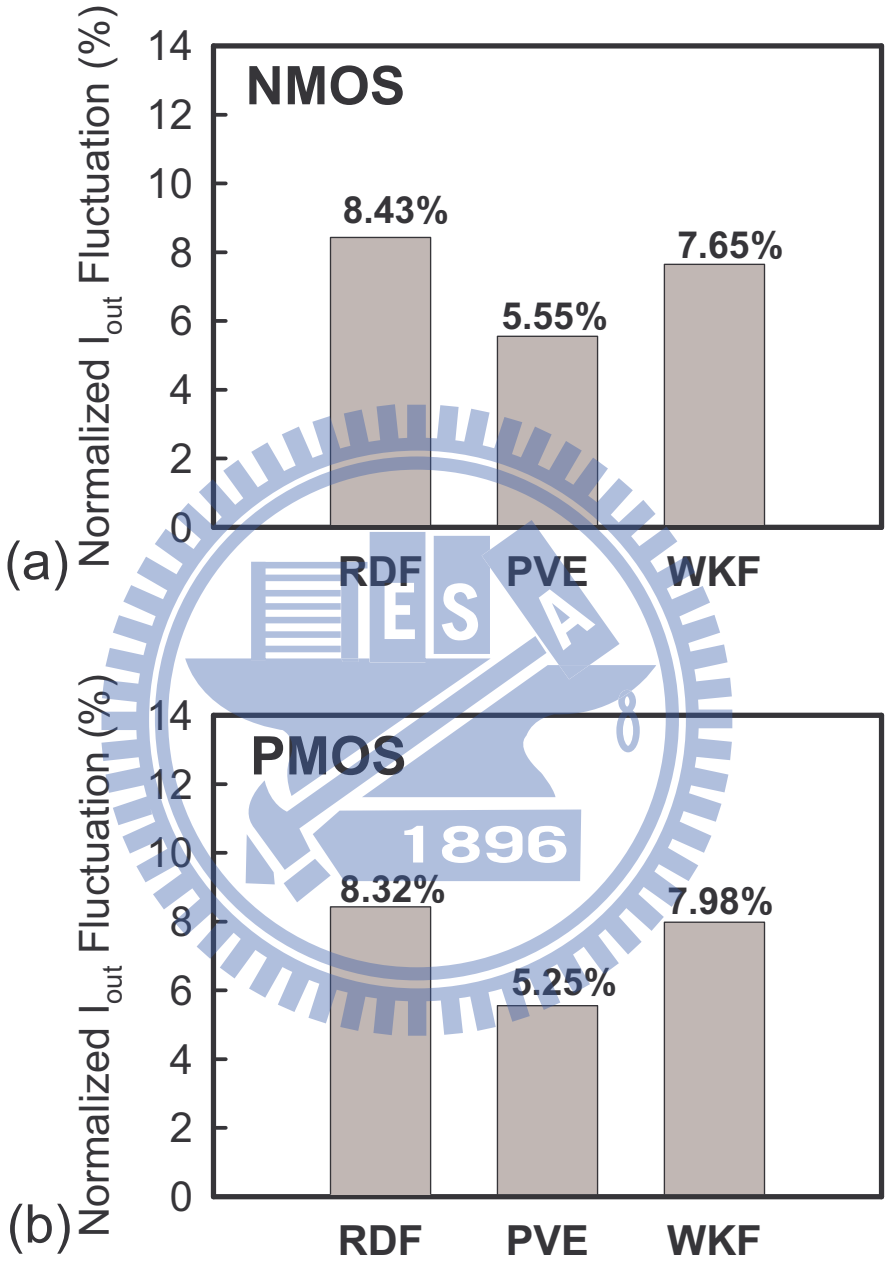


Figure 5.8: The summarized normalized I_{OUT} fluctuations induced by RDF, PVE, and WKF for (a) NMOS and (b) PMOS current mirror circuits.

5.3 Summary of this Chapter

This chapter has compared the influences of the work-function fluctuation with random dopant fluctuation and process variation effect in 16-nm nanoscale devices and circuits. The dominating factors of devices and circuits characteristic fluctuations were found and discussed. The WKF induced σV_{th} are competitive with RDF and is one of the dominating factors of the V_{th} fluctuation; however, the impact of WKF is small, especially at high gate bias. On the other hand, the PVE brings direct impact on gate length and therefore the PVE induced AC characteristic fluctuations are independent of screening effect and should be noticed when the transistor operated in high gate bias. In the timing and power fluctuations of inverter circuit, the SNM of SRAM, and the normalized I_{OUT} fluctuation of current mirror, the WKF is also a dominating factor due to significantly influence of device σV_{th}. For the high frequency characteristics including circuit gain, 3dB bandwidth, and unity-gain bandwidth, the major fluctuation sources are RDF and PVE, and WKF become less important in this analyzing skeleton.

Chapter 6

Conclusions and Future Work

6.1 Conclusion of this Study

The metal gate work-function fluctuation has been highlighted and investigated. The 3D device simulation proposed in this thesis can capture the work-function position effect which can not predict by the previous method. We have successfully examined it by the potential, charge, and band diagram distributions, and then compared with random dopant fluctuation and process variation effect. Our results have shown that the WKF and RDF dominate the device threshold voltage fluctuation; and therefore rule the power and delay time of the explored inverter circuit, SNM of SRAM circuit, and current mismatch of NMOS and PMOS current mirror circuits. The delay time, current mismatch, and static noise margin depend on the device V_{th}; therefore, their fluctuations follow the trend of

σV_{th}. The total power fluctuation including fluctuation of the dynamic power, the short circuit power, and the static power have been investigated. The RDF and WKF are the dominating factors. For the high-frequency characteristics, the circuit gain, the 3dB bandwidth, and the unity-gain bandwidth were also explored. Similar to the trend of the device cutoff frequency, the PVE and RDF dominate the device and circuits characteristic fluctuations and the WKF shows less impact on high-frequency characteristic owing to the small gate capacitance fluctuation. The sensitivities of circuit performance with respect to device parameter fluctuation have been reported. It is necessary to include both the WKF and RDF effects in studying digital circuit reliability; however, for the high frequency applications, the PVE and RDF effect are dominating factors. Consequently, the links should be established between circuit design and fundamental device technology to allow circuits and systems to accommodate the individual behavior of every transistor on a silicon chip.

6.2 Suggestions on Future Work

The nanoscale technology in now facing great challenge and provide abundant chances in new semiconductor application. For more realistic partitions on the shape of metal grains, we can generate them with voronoi diagram as shown in Fig. 6.1. The characterization and measurement of metal-gate work-function on high-κ dielectrics are required. The multi-layer structure in high-κ/metal gate should be further considered. The future work is suggested from device and circuit viewpoints. From the device viewpoint, study more fluctuation source, such as oxide thickness variation, interface trap variability as shown in Fig. 6.2 [73] and so on are necessary. The simulation of multi variation sources at the same time and find their correlation may be required. Another important issue is the suppression of intrinsic parameter fluctuations. The suppression may result in some drawbacks, which should be addressed properly. From the circuit viewpoint, it is imperative to derive a well-established compact model consisting of the randomness effect to realize the nanoscale device and circuit design. The coupled device-circuit simulation may provide an effective way to obtain circuit characteristics without use of compact model. However, there is still a lot of room to improve the numerical stability and numerical method in the coupled device-circuit simulation. To improve the reliability of VLSI circuits and systems, the development of fluctuation suppression approach from circuit topology is necessary.

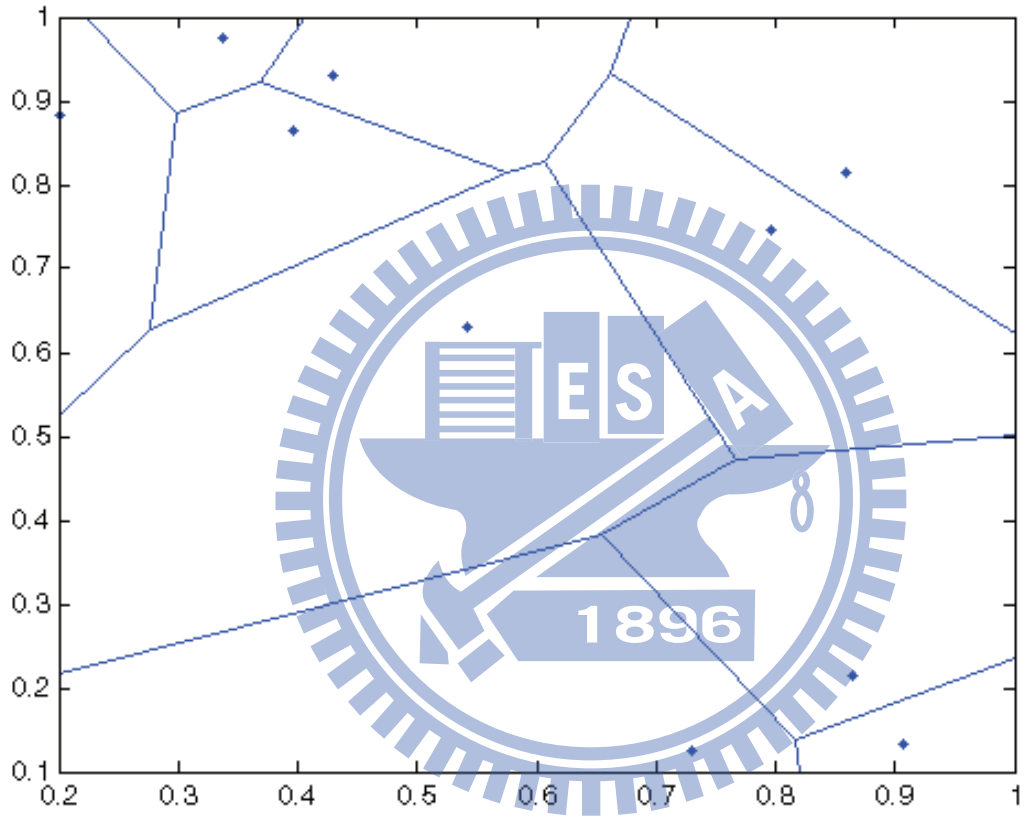


Figure 6.1: The voronoi diagram generated by MATLAB® could be considered to describe the random shape of metal grains in the LWKF simulation method.

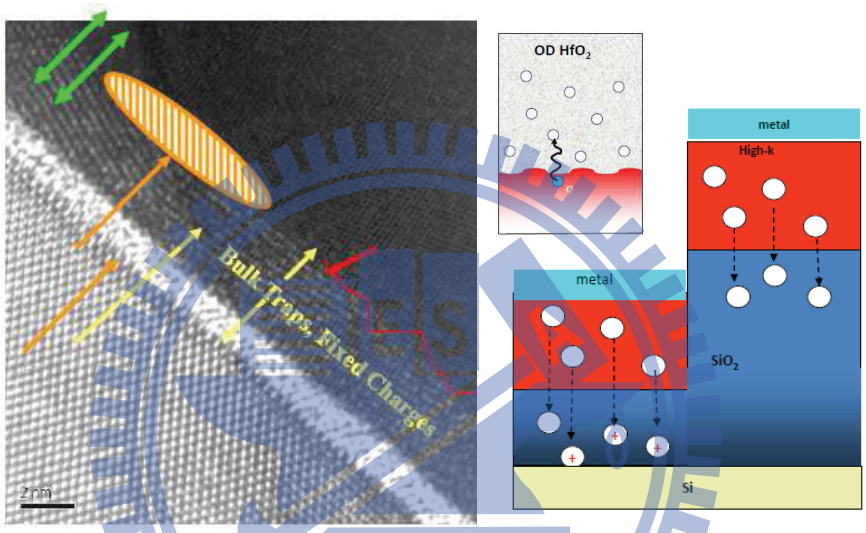


Figure 6.2: The illustration of interface trap at oxide/Si interface. Oxygen up-diffuse from SiO_2 interfacial layer to passivate the O-vacancies in high-κ and generation of positive charges associated with the oxygen vacancies near SiO_2/Si interface. The generated positive charge causes V_{th} reduction, thinner the SiO_2 more efficient to generate O-vacancy near the SiO_2/Si interface [73].

Bibliography

[1] S. M. Sze, and K. K. Ng, "Physics of Semiconductor Devices, 3rd ED," *WILEY-INTERSCIENCE*, 2007.

[2] http://www.itrs.net

[3] F.-L. Yang, J.-R. Hwang, and Y. Li, "Electrical Characteristic Fluctuations in Sub-45nm CMOS Devices," *IEEE Custom Integrated Circuits Conference*, pp. 691-694, 2006.

[4] Y. Li and H.-M. Chou, "A comparative Study of Electrical Characteristic on Sub-10 nm Double Gate MOSFETs," *IEEE Transactions on Nanotechnology*, vol. 4, no. 5, pp. 645-647, September 2005.

[5] F.-L. Yang, D.-H. Lee, H.-Y. Chen, C.-Y. Chang, S.-D. Liu, C.-C. Huang, T.-X. Chung, H.-W. Chen, C.-C. Huang, Y.-H. Liu, C.-C. Wu, C.-C. Chen, S.-C. Chen, Y.-T. Chen, Y.-H. Chen, C.-J. Chen, B.-W. Chan, P.-F. Hsu, J.-H. Shieh, H.-J. Tao,

Y.-C. Yeo, Y.-Li, J.-W. Lee, P.-Chen, M.-S. Liang and C. Hu, "5nm-Gate Nanowire FinFET," *Symposium on VLSI Technology*, pp. 196-197, June 2004.

[6] F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, and C. Hu, "25 nm CMOS Omega FETs," *International Electron Devices Meeting*, pp. 255-258, December 2002.

[7] R. W. Keyes, "Effect of Randomness in Distribution of Impurity Atoms on FET Thresholds," *Applied Physics*, vol. 8, pp. 251-259, November 1975.

[8] R. P. Joshi and D. K. Ferry, "Effect of Multi-ion Screening on the Electronic Transport in Doped Semiconductors: A Molecular-Dynamics Analysis," *Physics Review B*, vol. 43, pp. 9734-9739, April 1991.

[9] J.-R. Zhou and D.K. Ferry, "3D Simulation of Deep-Submicron Devices. How Impurity Atoms Affect Conductance," *IEEE Computational Science Engineering*, vol. 2, no. 2, pp. 30-37, June 1995.

[10] X.-H. Tang, V.K. De, and J.D. Meindl, "Intrinsic MOSFET Parameter Fluctuations Due to Random Dopant Placement," *IEEE Transactions VLSI Systems*, vol. 5, no. 4, pp. 369-376, December 1997.

[11] K. Noda, T. Tatsumi, T. Uchida, K. Nakajima, H. Miyamoto, and C. Hu, "A 0.1-μm Delta Doped MOSFET Fabricated with Post-low-energy Implanting Selective Epitaxy," *IEEE Transactions on Electron Devices*, vol. 45, no. 4, pp. 809-813, April 1998.

[12] P.A. Stolk, F.P. Widdershoven, and D.B.M. Klaassen, "Modeling Statistical Dopant Fluctuations in MOS Transistors," *IEEE Transactions on Electron Devices*, vol. 45, no. 9, pp. 1960-1971, September 1998.

[13] D. Vasileska, W.J. Gross, and D.K. Ferry, "Modeling of Ddeep-Submicrometer MOSFETs: Random Impurity Effects, Threshold Voltage Shifts and Gate Capacitance Attenuation," *Extended Abstracts of International Workshop on Computational Electronics*, pp. 259-262, October 1998.

[14] W. J. Gross, D. Vasileska, and D. K. Ferry, "A Novel Approach for Introducing the Electron-Electron And Eectron-Impurity Interactions in Particle-based Simulations," *IEEE Electron Device Letter*, vol. 20, no. 9, pp. 463-465, September 1999.

[15] H.-S. Wong, Y. Taur, and D. J. Frank, "Discrete Random Dopant Distribution Effects in Nanometer-Scale MOSFETs," *Microelectronics Reliability*, vol. 38, no. 9, pp. 1447-1456, September 1999.

[16] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, "Role of Long-range and Short-range Coulomb Potentials in Threshold Characteristics under Discrete Dopants in Sub-0.1μm Si-MOSFETs," *International Electron Devices Meeting*, pp. 275-278, December 2000.

[17] P. Dollfus, A. Bournel, S. Galdin, S. Barraud, and P. Hesto, "Effect of Discrete Impurities on Electron Transport in Ultrashort MOSFET Using 3D MC Simulation," *IEEE Transactions on Electron Devices*, vol. 51, no. 5, pp. 749- 756, May 2004.

[18] T. Ohtou, N. Sugii, T. Hiramoto, "Impact of Parameter Variations and Random Dopant Fluctuations on Short-Channel Fully Depleted SOI MOSFETs With Extremely Thin BOX," *IEEE Electron Device Letter*, vol. 28, no. 8, pp. 740-742, August 2007.

[19] T. Tsunomura, A. Nishida, and T. Hiramoto, "Analysis of NMOS and PMOS Difference in VT Variation with Large-Scale DMA-TEG," *IEEE Transactions on Electron Devices*, vol. 56, no. 9, pp. 2073-2080, September 2009.

[20] Y. Li, and C.-H. Hwang, "Discrete-Dopant-Induced Characteristic Fluctuations in 16 nm Multiple-Gate Silicon-on-Insulator Devices," *Journal of Applied Physics*, vol. 102, no. 8, 084509, October 2007.

[21] Y. Li and S.-M. Yu, "A Coupled-Simulation-and-Optimization Approach to Nanodevice Fabrication with Minimization of Electrical Characteristics Fluctuation," *IEEE Transactions on Semiconductor Manufacturing*, vol. 20, no. 4, pp.432-438, November 2007.

[22] N. Sano and M. Tomizawa, "Random Dopant Model for Three-Dimensional Drift-Diffusion Simulations in Metal-Oxide-Semiconductor Field-Effect-Transistors," *Applied Physics Letter*, vol. 79, pp. 2267, 2007.

[23] Y. Li, S.-M. Yu, J.-R. Hwang and F.-L. Yang, "Discrete Dopant Fluctuated 20nm/15nm-Gate Planar CMOS," *IEEE Transactions on Electron Devices*, vol. 55, no. 6, pp. 1449-1455, June 2008.

[24] Y. Li, C.-H. Hwang, and H.-M. Huang, "Large-Scale Atomistic Approach to Discrete-Dopant-Induced Characteristic Fluctuations in Silicon Nanowire Transistors," *Physics State Solution (a)*, vol. 205, no. 6, pp. 1505-1510, May 2008.

[25] A. Asenov, A. Cathignol, B. Cheng, K. P. McKenna, A. R. Brown, A. L. Shluger, D. Chanemougame, K. Rochereau, and G. Ghibaudo, "Origin of the Asymmetry in the Magnitude of the Statistical Variability of n- and p-Channel Poly-Si Gate Bulk MOSFETs," *IEEE Electron Device Letter*, vol. 29, no. 8, pp. 913-915, August 2008.

[26] Y. Li, and S.-M. Yu, "A Study of Threshold Voltage Fluctuations of Nanoscale Double Gate Metal-Oxide-Ssemiconductor Field Effect Transistors Using Quantum Correction Simulation," *Journal Computational Electronics*, vol. 5, no. 2-3, pp. 125-129, July 2006.

[27] C.L. Alexander, G. Roy, and A. Asenov, "Random Impurity Scattering Induced Variability in Conventional Nano-Scaled MOSFETs: Ab initio Impurity Scattering Monte Carlo Simulation Study," *International Electron Devices Meeting*, pp. 949-952, November 2006.

[28] A. Balasubramanian, P.R. Fleming, B.L. Bhuva, A.L. Sternberg, L.W. Massengill, "Implications of Dopant-Fluctuation-Induced Vt Variations on the Radiation Hardness of Deep Submicrometer CMOS SRAMs," *IEEE Transactions on Device and Materials Realiability*, vol.8, no.1, pp. 135-144, March 2003.

[29] R. Tanabe, Y. Ashizawa, H. Oka, "Investigation of SNM with Random Dopant Fluctuations for FD SGSOI and FinFET 6T SOI SRAM Cell by Three-dimensional Device Simulation," *Simulation of Semiconductor Processes and Devices Conference*, pp. 103-106, September 2006.

[30] B. Cheng, S. Roy, G. Roy, and A. Asenov, "Impact of Intrinsic Parameter Fluctuations on SRAM Cell Design," *Intional Solid-State and Integrated Circuit Technology*

Conference, pp. 1290-1292, October 2006.

[31] S. K. Springer, S. Lee, N. Lu, E. J. Nowak, J.-O. Plouchart, J. S. Watts, R. Q. Williams, and N. Zamdmer, "Modeling of Variation in Submicrometer CMOS ULSI Technologies," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 2168-2178, September 2006.

[32] Y. Li and C.-H. Hwang, "Discrete-Dopant-Fluctuated Tthreshold Voltage Roll-Off in Sub-16nm Bulk FinFETs," *Japanese Journal of Applied Physics*, vol. 47, no. 4B, pp. 2580-2584, April 2008.

[33] X. Tang, K. A. Bowman, J. C. Eble, V. K. De, and J. D. Meindl, "Impact of Random Dopant Placement on CMOS Delay and Power Dissipation," *European Solid-State Device Research Conference*, pp. 184-187, September 1999.

[34] H. Mahmoodi, S. Mukhopadhyay, and K. Roy, "Estimation of Delay Variations due to Random-Dopant Fluctuations in Nanoscale CMOS Circuits," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 9, pp. 1787-1796, September 2005.

[35] Y. Li, and C.-H. Hwang, "High-Frequency Characteristic Fluctuations of Nano-MOSFET Circuit Induced by Random Dopants," *IEEE Transactions on Microwave Theory and Technology*, vol. 56, no. 12, pp. 2726-2733, December 2008.

[36] J. Jaffari and M. Anis, "Variability-Aware Bulk-MOS Device Design," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System*, vol. 27, No. 2, pp. 205-216, February 2008.

[37] L. Brusamarello, R. da Silva, G. I. Wirth, and R. A. L. Reis, "Probabilistic Approach for Yield Analysis of Dynamic Logic Circuits," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 55, no. 8, pp. 2238-2248, September 2008.

[38] Y. Li, C.-H. Hwang, T.-C. Yeh, and M.-H. Han, "Simulation of Electrical Characteristic Fluctuation in 16-nm FinFETs and Circuits," *Device Research Conference*, pp. 54-55, June 2009.

[39] T.-Y. Li, C.-H. Hwang, M.-H. Han, and Y. Li, "Effects of Intrinsic Parameter Fluctuations in Emerging CMOS Technologies," *Silicon Nanoelectronics Workshop*, pp. 139-140, June 2009.

[40] C.-H. Hwang, T.-Y. Li, M.-H. Han, K.-F. Lee, H.-W. Cheng, and Y. Li, "Statistical 3D Simulation of Metal Gate Workfunction Variability, Process Variation, and Random Dopant Fluctuation in Nano-CMOS Circuits," *Simulation of Semiconductor Processes and Devices Conference*, pp. 99-102, September 2009.

[41] M.-H. Han, C.-H. Hwang, and Y. Li, "Intrinsic-Parameter-Fluctuated Power-Delay

Characteristics in 16nm-Metal-Gate CMOS Devices and Circuits," *Solid State Devices and Materials Conference*, pp. 404-405, October 2009.

[42] Y. Li, C.-H. Hwang, T.-Y. Li, and M.-H. Han, "Process Variation Effect, Metal-Gate Workfunction and Random Dopant Fluctuations in Emerging CMOS Technologies," *IEEE Transactions on Electron Devices*, vol. 57, no. 2, pp. 437-447, February 2010.

[43] M.-H. Han, Y. Li, and C.-H. Hwang, "Discrete-Dopant-Induced Power-Delay Characteristic Fluctuation in 16 nm Complementary Metal-Oxide-Semiconductor with High Dielectric Constant Material," *Japanese Journal of Applied Physics*, vol. 49, no. 4, pp. 04DC02, 2010.

[44] Y. Li, C.-H. Hwang, and M.-H. Han, "Intrinsic Parameter Fluctuations in 16-nm-Gate FinFET Devices," *Nanotechnology*, vol. 21, pp. 095203, 2010.

[45] M.-H. Han, C.-H. Hwang, and Y. Li, "The Impact of High Frequency Characteristics Induced by Intrinsic Parameter Fluctuations in Nano-MOSFET Device and Circuit," *Microelectronics Reliability*, vol. 50, no. 5, pp. 657-661, May 2010.

[46] O. Weber, O. Faynot, F. Andrieu, C. Buj-Dufournet, F. Allain, P. Scheiblin, J. Foucher, N. Daval, D. Lafond, L. Brevard, O. Rozeau, C. Fenouillet-Beranger, M. Marin, F. Boeuf, D. Delprat, K. Bourdelee, B.-Y. Nguyen, and S. Deleonibus, "High

Immunity to Threshold Voltage Variability in Undoped Ultra-Thin FDSOI MOSFET and its Physical Understanding," *International Electron Devices Meeting*, pp. 245-248, December 2008.

[47] K. Ohmori, T. Matsuki, D. Ishikawa, T. Morooka, T. Aminaka, Y. Sugita, T. Chikyow, K. Shiraishi, Y. Nara, and K. Yamada, "Impact of Additional Factors in Threshold Voltage Variability of Metal/High-k Gate Stacks and its Reduction by Controlling Crystalline Structure and Grain Size in the Metal Gates," *International Electron Devices Meeting*, pp. 409-412, December 2008.

[48] H. Dadgour, De Vivek, K. Banerjee, "Statistical Modeling of Metal-Gate Work-Function Variability in Emerging Device Technologies and Implications for Circuit Design," *International Conference on Computer-Aided Design*, pp. 270-277, November 2008.

[49] H. Dadgour, K. Endo, V. De, and K. Banerjee, "Modeling and Analysis of Grain-Orientation Effects in Emerging Metal-Gate Devices and Implications for SRAM Reliability," *International Electron Devices Meeting*, pp. 705-708, December 2008.

[50] T. Matsukawa, S. O'uchi, K. Endo, Y. Ishikawa, H. Yamauhci, Y.X. Liu, J. Tsukada, K. Sakamoto, and M. Masahara, "Comprehensive Analysis of Variability Sources of FinFET Characteristics," *Symposium on VLSI Technology*, pp. 118-119, June 2009.

[51] X. Zhang, J. Li, M. Grubbs, M. Deal, B. Magyari-Kope, B. M. Clemens, and Y.Nishi, "Physical Model of the Impact of Metal Grain Work Function Variability on Emerging Dual Metal Gate MOSFETs and its Implication for SRAM Reliability," *International Electron Devices Meeting*, pp. 57-60, December 2009.

[52] L. Brunet, X. Garros, M. Casse, O. Weber, F. Andrieu, C. Fenouillet-Beranger, P. Perreau, F. Martin, M. Charbonnier, D. Lafond, C. Gaumer, S. Lhostis, V. Vidal, L. Brevard, L. Tosti, S. Denorme, S. Barnola, J.F. Damlencourt, V. Loup, G. Reimbold, F. Boulanger, O. Faynot, and A. Bravaix, "New Insight on VT stability of HK/MG Stacks with Scaling in 30nm FDSOI Technology," *Symposium on VLSI Technology*, pp. 29-30, June 2010.

[53] H. -C. Wen, S. C. Song, C. S. Park, C. Burham, G. Bersuker, K. Choi, M. A. Quevedo-Lopez, B. S. Ju, H. N. Alshareef, H. Niimi, H. B. Park, P. S. Lysaght, P. Majhi, B. H. Lee, and R. Jammy, "Gate First Metal-Aluminum-Nitride PMOS Electrodes for 32nm Low Standby Power Applications," *Symposium on VLSI Technology*, pp. 160-161, June 2007.

[54] C. Canali, G. Majni, R. Minder, and G. Ottaviani "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature," *IEEE Transactions on Electron Devices*, vol. 22, no. 11, pp. 1045-1047, November 1975.

[55] T. Grasser and S. Selberherr, "Mixed-Mode Device Simulation," *Microelectronics Journal*, vol. 31, no. 11-12, pp.873-881, December 2000.

[56] G.J. Iafrate, H.L. Grubin and D.K. Ferry, "Utilization of Quantum Distribution Functions for Ultra-Submicron Device Transport," *Le Journal de Physique Colloques*, vol. 42, no. C7, pp. C7-307, 1981.

[57] M. G. Ancona and H. F. Tiersten, "Macroscopic Physics of the Silicon Inversion Layer," *Physics Review B*, vol. 35, no. 15, pp. 7959-7965, May 1987.

[58] J.-R. Zhou and D.K. Ferry, "Simulation of Ultra-Small GaAs MESFET Using Quantum Moment Equations," *IEEE Transactions on Electron Devices*, vol. 39, no. 3, pp. 473-478, March 1992.

[59] J.-R. Zhou and D.K. Ferry, "Simulation of Ultra-Small GaAs MESFET Using Quantum Moment Equations II. Velocity Overshoot," *IEEE Transactions on Electron Devices*, vol. 39, no. 8, pp. 1793-1796, August 1992.

[60] A. Hafid Zaabab, Qi-Jun Zhang, and Michel Nakhla, "A Neural Network Modeling Approach to Circuit Optimization and Statistical Design," *IEEE Transactions on Microwave Theory and Technology*, vol. 43, no. 6, pp. 1349-1358, June 1995.

[61] J.-R. Zhou and D.K. Ferry, "Modeling of quantum effects in ultrasmall HEMT devices," *IEEE Transactions on Electron Devices*, vol. 40, no. 2, pp. 421-427, February 1993.

[62] T.-W. Tang, X. Wang, and Y. Li, "Discretization Scheme for the Density-Gradient Equation and Effect of Boundary Conditions," *Journal Computational Electronics*, vol. 1, no. 3, pp. 389-393, October 2002.

[63] P. Crippa, C. Turchetti, and M. Conti, "A Statistical Methodology for the Design of High-Performance CMOS Current-Steering Digital-to-Analog Converters," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System*, vol. 21, No. 4, pp. 377-394, April 2002.

[64] S. Odanaka, "Multidimensional Discretization of the Stationary Quantum Drift-Diffusion Model for Ultrasmall MOSFET Structures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System*, vol. 23, no. 6, pp.837-842, June 2004.

[65] S. Berge, P. O. Gartland, and B. J. Slagsvold, "Photoelectric Work-Ffunction of a Molybdenum Single Crystal for the (100), (110), (111), (112), (114), and (332) Faces," *Surface Science*, vol. 43, pp. 275-292, 1974.

[66] A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, K. Matsuo, T. Shibata, Y. Tsunashima, K. Suguro, and T. Arikado, "Improvement of Threshold Voltage Deviation in Damascene Metal-Gate Transistors," *IEEE Transactions on Electron Devices*, vol. 48, pp. 1604-1611, 2001.

[67] G. Jie, S.S. Sapatnekar, and C. Kim, "Width-dependent Statistical Leakage Modeling for Random Dopant Induced Threshold Voltage Shift," *Conference on Design Automation Conference*, pp. 87-92, 2007.

[68] T.-S. Park, H. J. Cho, J. D. Choe, S. Y. Han, D. Park, K. Kim, E. Yoon, and J.-H. Lee, "Characteristics of the Full CMOS SRAM Cell Using Body-Tied TG MOSFETs (Bulk FinFETs)," *IEEE Transactions on Electron Devices*, vol. 53, no. 3, pp. 481-487, March 2006.

[69] Z. Liu and V. Kursun, "Characterization of a Novel Nine-Transistor SRAM Cell," *IEEE Transactions on VLSI Systems*, vol. 16, no. 4, pp. 488-492, April 2008.

[70] C. Fenouillet-Beranger, S. Denorme, P. Perreau, C. Buj, O. Faynot, F. Andrieu, L. Tosti, S. Barnola, T. Salvetat, X. Garros, M. Casse, F. Allain, N. Loubet, L. Pham-NGuyen, E. Deloffre, M. Gros-Jean, R. Beneyton, C. Laviron, M. Marin, C. Leyris, S. Haendler, F. Leverd, P. Gouraud, P. Scheiblin, L. Clement, R.Pantel, S. Deleonibus, and T. Skotnicki, "FDSOI Devices with Thin BOX and Ground Plane

Integration for 32nm Node and Below," *European Solid-State Device Research Conference*, pp. 206-209, September 2008.

[71] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, "Stable SRAM Cell Design for the 32 nm Node and Beyond," *Symposium on VLSI Technology*, pp. 128-129, June 2005.

[72] C. Hill, "Definitions of Noise Margin in Logic Systems," *Mullard Technical Communications*, vol. 89, pp. 239V245, 1967.

[73] G. Bersuker, C. S. Park, H. C. Wen, K. Choi, O. Sharia, and A. Demkov, "Origin of the Flat-Band Voltage (V_{fb}) Roll-Off Phenomenon in Metal/High-k Gate Stacks ," *European Solid-State Device Research Conference*, pp. 134-137, September 2008.

Appendix A

VITA

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Institute of Communications Engineering, National Chiao Tung University, Hsinchu, Taiwan	MS	August, 2010

Master thesis title:

Random-Metal-Gate-Work-Function-Induced Electrical Characteristic Fluctuation in 16-nm-Gate CMOS Devices and Circuits

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98年度研究生書卷獎(Academic Achievement Award)與獎學金

Selected Publication List:

Journal papers

1. Ming-Hung Han, Yiming Li, and Chih-Hong Hwang, "Discrete-Dopant-Induced Power-Delay Characteristic Fluctuation in 16 nm Complementary Metal-Oxide-Semiconductor with High Dielectric Constant Material," *Japanese Journal of Applied Physics*, vol. 49, no.4, pp. 04DC02, 2010.
2. Ming-Hung Han, Yiming Li, and Chih-Hong Hwang, "The Impact of High Frequency Characteristics Induced by Intrinsic Parameter Fluctuations in Nano-MOSFET Device and Circuit," *Microelectronics Reliability*, 2010. vol. 50, no. 5, pp. 657-661, May 2010.

3. Yiming Li, Chih-Hong Hwang, Tien-Yeh Li, and **Ming-Hung Han**, "Process Variation Effect, Metal-Gate Workfunction and Random Dopant Fluctuations in Emerging CMOS Technologies," *IEEE Transactions on Electron Devices*, vol. 57, no. 2, pp. 437-447, Feb. 2010.
4. Yiming Li, Chih-Hong Hwang, and **Ming-Hung Han**, "Intrinsic Parameter Fluctuations in 16-nm-Gate FinFET Devices," *Nanotechnology*, vol. 21, pp. 095203, 2010.
5. Chih-Hong Hwang, Yiming Li, and **Ming-Hung Han**, "Statistical Reliability in FinFET Devices with Intrinsic Parameter Fluctuations," *Microelectronics Reliability*, vol. 50, no. 5, pp. 635-638, May 2010.

Conference papers

1. **Ming-Hung Han**, Chih-Hong Hwang, and Yiming Li, "Intrinsic-Parameter-Fluctuated Power-Delay Characteristics in 16nm-Metal-Gate CMOS Devices and Circuits," *The 2009 International Conference on Solid State Devices and Materials* (*SSDM* 2009), Sendai Kokusai Hotel, Miyagi, Japan, pp. 404-405, Oct. 7-9, 2009.
2. **Ming-Hung Han**, Yiming Li, Kuo-Fu Lee, Hui-Wen Cheng, and Zhong-Cheng Su "Comprehensive Examination of Intrinsic-Parameter-Induced Characteristic Fluctuations in 16-nm-Gate CMOS Devices," *2010 International Conference on Nanofabrication Technologies, Devices and Applications* (*Nanotech* 2010), Anaheim Convention Center Anaheim, California, U.S.A, June 21- 25, 2010.
3. Hui-Wen Cheng, **Ming-Hung Han**, Kuo-Fu Lee, Chun-Yen Yiu, Thet Thet Khaing, and Yiming Li, "Electrical Characteristics Fluctuation and Suppression in Emerging CMOS Device and Circuit," *Workshop Abstracts of The 2010 IEEE Silicon Nanoelectronics Workshop* (*IEEE SNW* 2010), Hilton Hawaiian Village, Honolulu, HI, USA, June 13-14, 2010.
4. Chia-Hui Yu, **Ming-Hung Han**, Hui-Wen Cheng, Zhong-Cheng Su, Yiming Li, and Hiroshi Watanabe, "Statistical Simulation of Metal-Gate Work-function Fluctuation in Emerging High-κ/Metal-Gate CMOS Devices," *Proceedings of The 2010 IEEE International Conference on Simulation of Semiconductor Processes and Devices* (*IEEE SISPAD* 2010), Royal Carlton Hotel, Bologna, Italy, Sep. 6-8, 2010.
5. Hui-Wen Cheng, Kuo-Fu Lee, **Ming-Hung Han**, and Yiming Li, "Metal-Gate Work-Function Fluctuation in 16-nm Single- and Multi-fin Field Effect Transistors with Different Aspect Ratio," *2010 IEEE International Conference on Semiconductor Electronics* (*ICSE* 2010),Holiday Inn Melaka Hotel, Melaka, Malaysia, June 28-30, 2010.
6. Chih-Hong Hwang, Tien-Yeh Li, **Ming-Hung Han**, Kuo-Fu Lee, Hui-Wen Cheng, and Yiming Li, "Statistical 3D Simulation of Metal Gate Workfunction Variability, Process Variation, and Random Dopant Fluctuation in Nano-CMOS Circuits," *Proceedings of The 2009 IEEE International Conference on Simulation of Semiconductor Processes and Devices* (*IEEE SISPAD* 2009), Hotel Del Coronado, San Diego, California, USA, pp. 99-102, Sept. 9-11, 2009.
7. Tien-Yeh Li, Chih-Hong Hwang, **Ming-Hung Han**, and Yiming Li, "Effects of Intrinsic Parameter Fluctuations in Emerging CMOS Technologies," *Workshop Abstracts of The 2009 IEEE Silicon Nanoelectronics Workshop* (*IEEE SNW* 2009), Kyoto, Japan, pp. 139-140, June 13-14, 2009.
8. Yiming Li, Chih-Hong Hwang, Ta-Ching Yeh, and **Ming-Hung Han**, "Simulation of Electrical Characteristic Fluctuation in 16-nm FinFETs and Circuits," *Device Research Conference* (*IEEE DRC* 2009), Penn State University, PA, USA, pp. 54-55, June 22-24, 2009.

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榮獲大學院校奈米元件 電腦輔助模擬與設計軟體製作競賽

特優

指導老師 國立交通大學 李義明 教授

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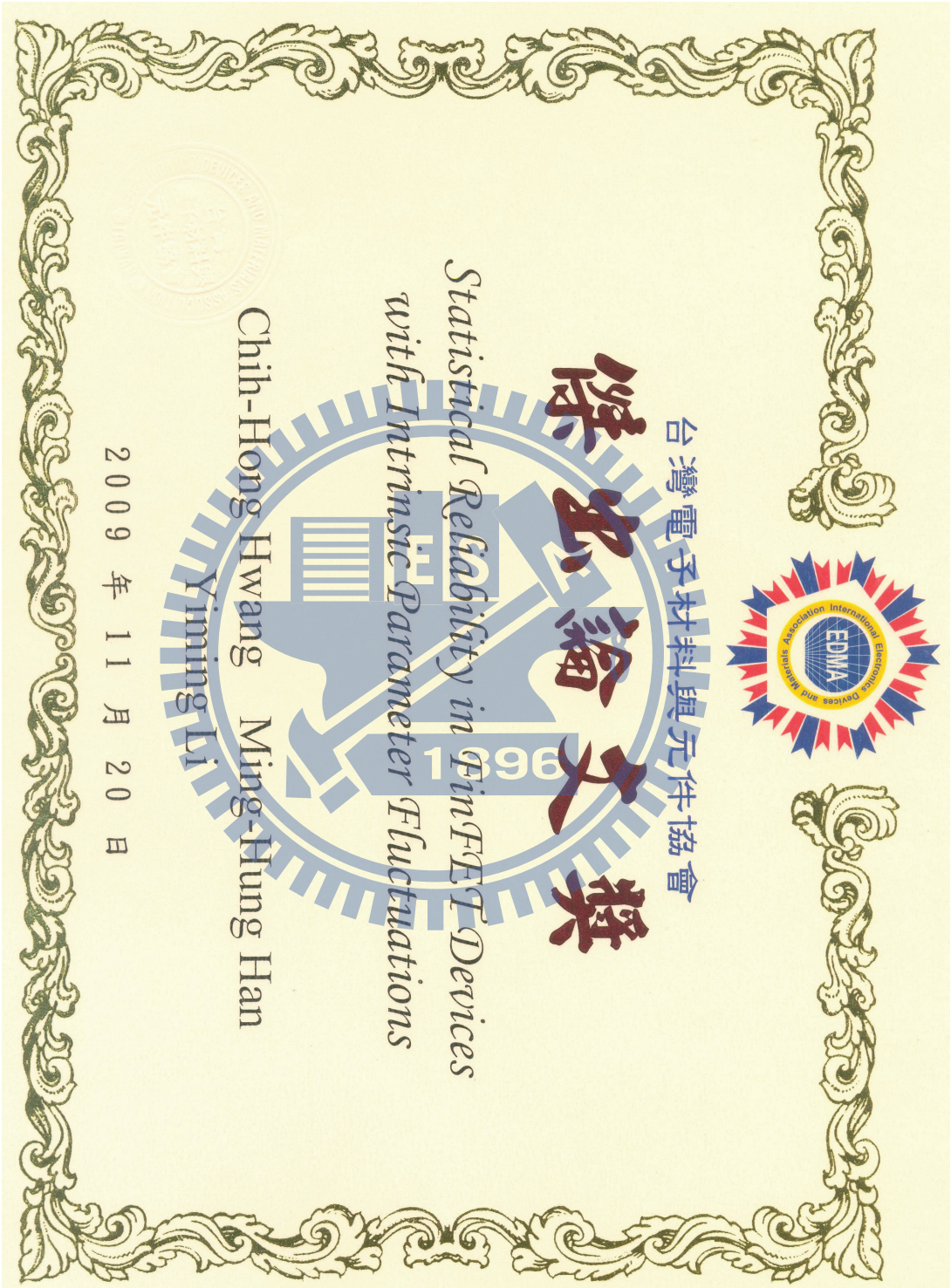
台灣電子材料與元件協會
傑出論文獎
Statistical Reliability in FinFET Devices
with Intrinsic Parameter Fluctuations
Chih-Hong Hwang Ming-Hung Han
Yiming Li
2009 年 11 月 20 日
EDMA
Electronics Devices and Materials Association International

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在本校九十七學年度第二學期學業成績優異，殊堪嘉許。特頒此狀，用示獎勉。

國立交通大學校長 吳重雨

中華民國 九十八 年 十 月 二十六 日