國立交通大學

顯示科技研究所

碩士論文

具氧化物之電阻式隨機存取記憶體

Oxide-Based Resistive Random Access Memory

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摘　　要

本篇論文中，我們使用磁控濺鍍的二氧化矽薄膜來實現無機的電阻式記憶體，以及探討後退火製程對元件電性的影響。結果發現經過後退火處理的元件可以展現較好的電性，由其在可靠性量測得到大幅的改善。此外，我們也分析元件在高導電態的載子傳輸行為，探討了記憶體元件在不同退火條件下的載子傳輸機制。

為了朝向更低成本以及大量生產的目標發展，我們製作了兩種結構的有機電阻式記憶體元件，分別是 AlO_x/Alq_3 雙層和 $Alq_3/MoO_3/Alq_3$ 三層結構。實驗結果顯示：雙層結構的 AlO_x/Alq_3 之介面缺陷態主導元件的記憶體特性，使得元件在電性上展現近 6 個數量級的高開關電流比；三層結構的記憶體特性源自具奈米結構的 MoO_3 與 Alq_3 的能帶差所形成的載子捕捉中心，並且該元件展現了 4 個數量級的高開關電流比，以及可以多次的抹除寫入。

Oxide-Based Resistive Random Access Memory

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Abstract

In this thesis, we demonstrate inorganic resistive random access memory (RRAM) using sputtered SiO_2 thin films, and investigate the influences of electrical characteristics of the devices with various post-annealing conditions. The results show that devices with RTA treatment can exhibit better electrical characteristics, especially in the significant improvement of endurance. We also analyze carrier transport behaviors in the high conductance state of devices and propose carrier transport mechanisms under different RTA treatments.

In addition, we fabricate two different structures of organic RRAM: AlO_x/Alq_3 bi-layer and $Alq_3/MoO_3/Alq_3$ tri-layer structures. It is found that interface defects at the AlO_x/Alq_3 interface dominate the resistive switching of organic RRAM using the bi-layer structure, and the high ON/OFF current ratio near 10^6 is obtained; the switching behavior of organic RRAM using the tri-layer structure originate from carrier confinement barriers produced by the difference of energy bands between the nano-structure MoO_3 and Alq_3 layers, and this devices exhibit a high ON/OFF current ratio about 10^4 and provide many write-read-erase-read cycles.

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2010/07/05 于新竹 國立交通大學 交映樓 401 室

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Chapter 1. Introduction

1.1. Introduction

Nonvolatile storage device of flash memory is one of the most famous memories in recent years due to the advantages of fast read access time, robust, portable, and high density of data storage. However, a tremendous demand for large amount of data and information storage is necessary, because we are in the information explosion and a rapid development of computer and electronic devices of times. Therefore, the nonvolatile memory (NVM) for next generation has attracts extensive attention due to the conventional flash memory approaching its scaling limits. The memories with capacity of three-dimension (3-D) stacking have most potential for high density data storage.

Fig. 1.1 depicts the schematic structure of a conventional flash memory, and this transistor-based structure is complicated and unsuitable for 3-D stacking. Moreover, when the tunneling oxide thickness is below 10nm, the charge stored in the floating gate will be lost.

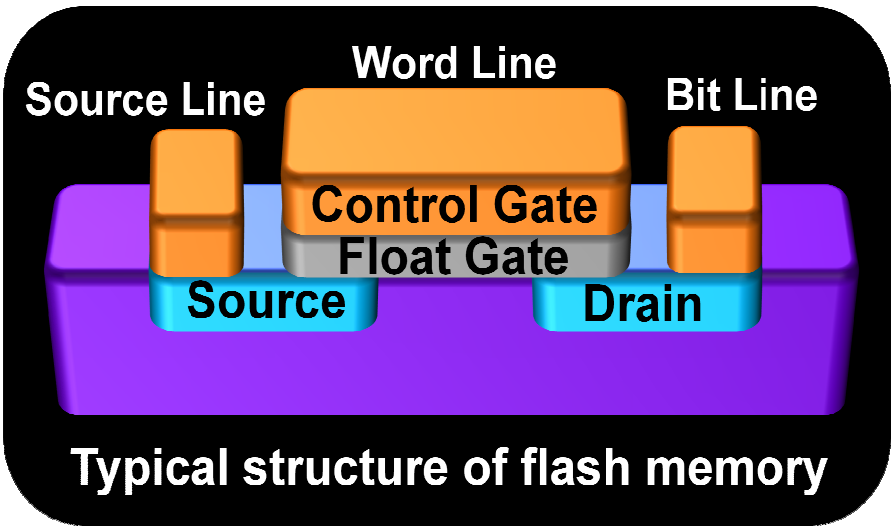


Fig. 1.1: Schematic structure of a conventional flash memory

The potential next-generation memory such as phase-changed memory, ferroelectrical random access memory, magnetic random access memory, and resistive random access memory has been widely studied. Among those, resistive random access memory is more promising due to the simple structure, simple fabrication process, fast read access time, low operation voltage, and especially the capability of 3-D stacking.

1.2. Resistive Random Access Memory (RRAM)

1.2.1. Inorganic RRAM

The change of resistivity in insulator has been discovered in the early 1962 years by T.W. Hickmoot [1]. After that, various insulators such as Al_2O_3 [2-4], NiO [5-6], TiO_2 [7], Nb_2O_5 [8], and ZrO_2 [9-11] have been extensively investigated due to the simple compositions which are easy to control during the fabrication process.

However, the mechanism of resistive switching property is not clearly understood until now. So far, the formation and fracture of filamentary paths are most acceptable to elucidate the resistivity switching occurring in oxide films.

It has been proposed that filamentary paths consist of oxygen vacancies and oxygen-related defects in nonstoichiometry oxide [2], and penetrated metal particles [3], metal ions in solid electrolyte [12]. For example, Tseung-Yuen Tseng et al propose a structure of Pt/Ti/Al_2O_3/Pt/Ti/SiO_2/Si, where resistive switching is dominated by filamentary paths formation in Al_2O_3 layer. Because of the strong oxygen-gettering ability of Ti, the oxygen ions will escape from Al_2O_3 and getter with Ti under a suitable applied voltage, called forming voltage. Therefore, the oxygen vacancies and oxygen-related defects are generated and modified to form conducting paths in Al_2O_3 thin film.

Fig. 1.2 displays the typical electrical characteristics of Pt/Ti/Al_2O_3/Pt structure, and its mechanism is dominated by filamentary paths. Compliance current is set in the writing process during the electrical measurement. Because the joule heat of a large current in erasing process (where arrow points in Fig. 1.2) may burn the conducting filamentary paths, the devise will be changed from high conductance state (ON state) to low conductance state (OFF state). In their work, they also discover the forming voltage decreases with increasing post-annealing temperature, and the device with

600°C post-annealing treatment do not need a forming process due to the penetration of Ti into Al_2O_3 thin film which connect two electrodes.

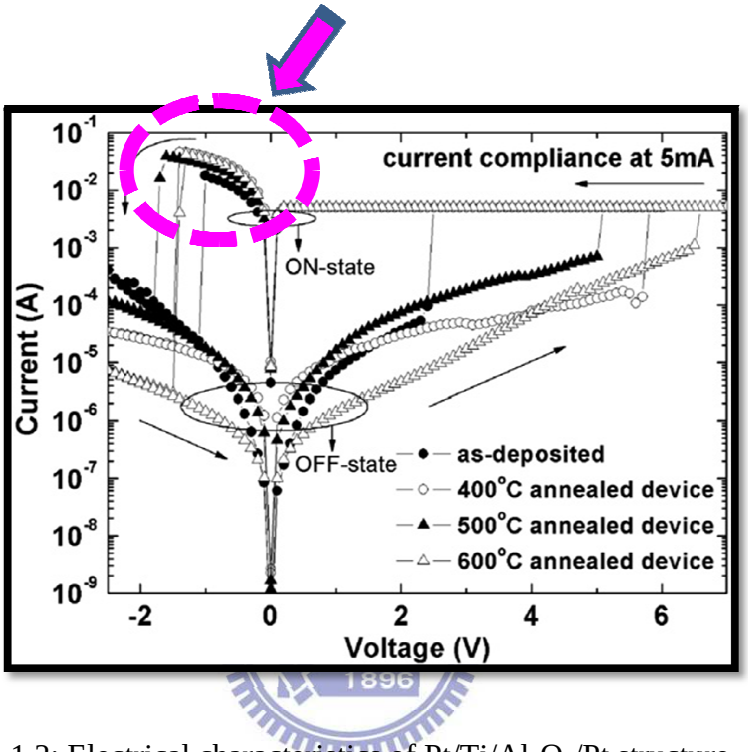


Fig. 1.2: Electrical characteristics of Pt/Ti/Al_2O_3/Pt structure.

In the other hand, some researches of metal doped oxide as the insulator layer in MIM structure of RRAM have been manifested. For example, W. Guan et al propose an RRAM with Cu doped ZrO_2. As shown in a linear-linear plot of Fig. 1.3, the electrical characteristics exhibit a linear relation between current and voltage in ON-state. This ohmic conduction is ascribed to the formation of conducting filamentary paths, which originate from Cu ions diffusion. Moreover, other studies such as Cu doped MoO_3 [13] and Cu doped SiO_2 [14] are also proposed due to the

great diffusion ability of Cu ions in oxide films. This kind RRAM with metal doped oxide can provide better memory performance.

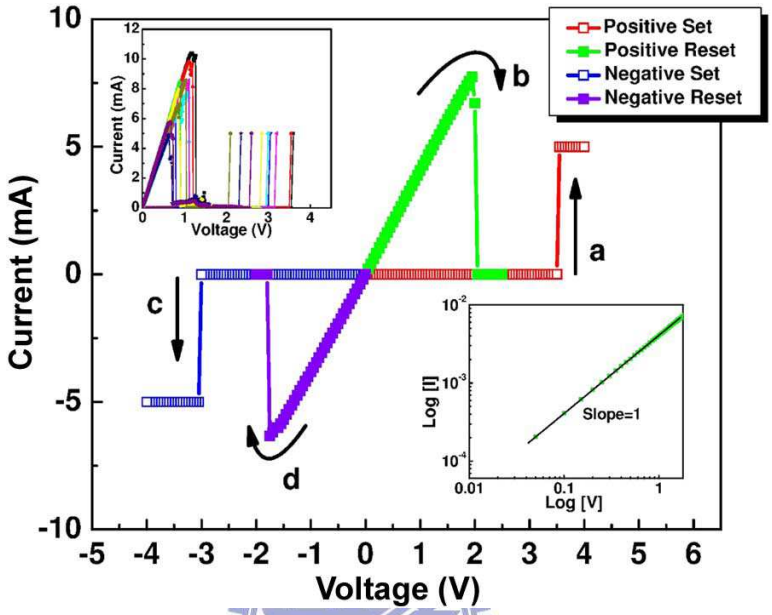


Fig. 1.3: Electrical characteristics of Cu/ZrO_2:Cu/Pt memory devices.

1.2.2. Organic RRAM

In recent years, there has been an increasing interest in organic electronic devices such as OTFT [15], OPV [16], OLED [17]…etc, owing to low cost, simple fabrication process, massive production, low power driving, and flexibility. Therefore, many researchers in nonvolatile memory field have widely developed RRAM devices using organic materials, for instances, nano-structure based devices, donor-acceptor type, and charge-transfer complexes based devices have been proposed to demonstrate the organic RRAM.

The nano-structure based devices can be classified according to the organic materials. One is organic small molecular materials blended with core-shell nano-particles/nano-clusters [18], and the other one is polymeric material blended with metal nano-particle [19-20]. Yang Yang et al proposes a more promising device with sandwich structure of organic/ core-shell nano-clusters/ organic [21]. In their study, they use AIDCN as matrix and interpose a thin Al layer which is oxidized during thermal evaporation and formed Al nano-clusters. The device structure and resistive switching characteristics are shown in Fig 1.4. According to measurements of electrical characteristics and AFM image of Al nano-clusters as shown in Fig 1.5, they evaluate that the mechanism of resistive switching is ascribed to charging and decharging of carriers in Al nano-clusters. Due to the charging of carriers in Al nano-cluster, the organic thin films will be polarized and then a built-in electrical filed is formed. This built-in electrical filed induced large amount of carrier pass through thin films, and this device is switched to high conductance state (ON state) from initial low conductance state (OFF state). In addition, this device with sandwich structure can exhibit high on/off current ratio about six orders in magnitude (10^6) which can avoid reading error between ON and OFF states.

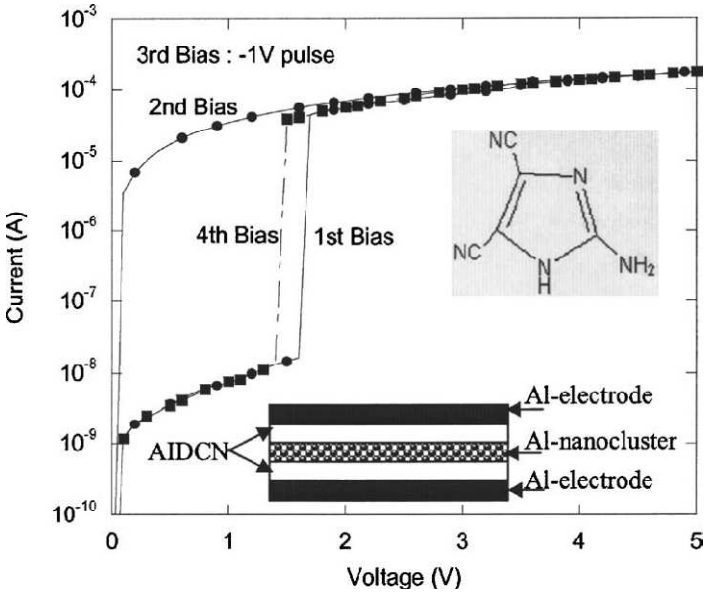


Fig. 1.4: Current-voltage characteristics of AIDCN/Al nano-clusters/AIDCN sandwich structure.

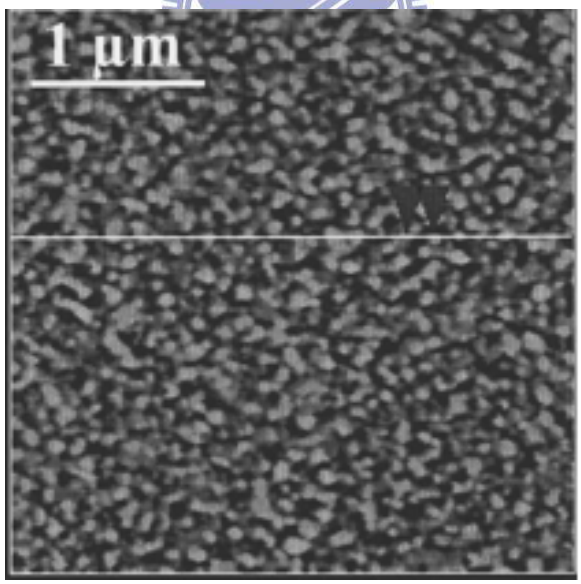


Fig. 1.5: AFM image of Al nano-cluster

In the other hand, some research groups have proposed that organic RRAM with nano-structure can also be fabricated by chemical synthesis of polymeric

material with Au nano-particles. H. T. Lin et al. synthesized PCm (4-Cyano-2,4,4-trimethyl-2-methylsulfanylthio- carbonylsulfanyl-poly (butyric acid 1-adamantan-1-yl-1-methyl-ethyl ester) with Au nano-particles as the active layer of the organic RRAM [22]. The current-voltage characteristics with/without Au nano-particles and the TEM image with Au nano-particles in PCm are shown in Fig. 1.6 and 1.7, respectively. Au nano-particles synthesized with parylene-C by B. Park et al. [23] and Au nano-particles are blended in PVK by P.Y. Lai et al. are also be demonstrated successfully as memory devices [24]. However, these materials need specific techniques to synthesize and are more expensive.

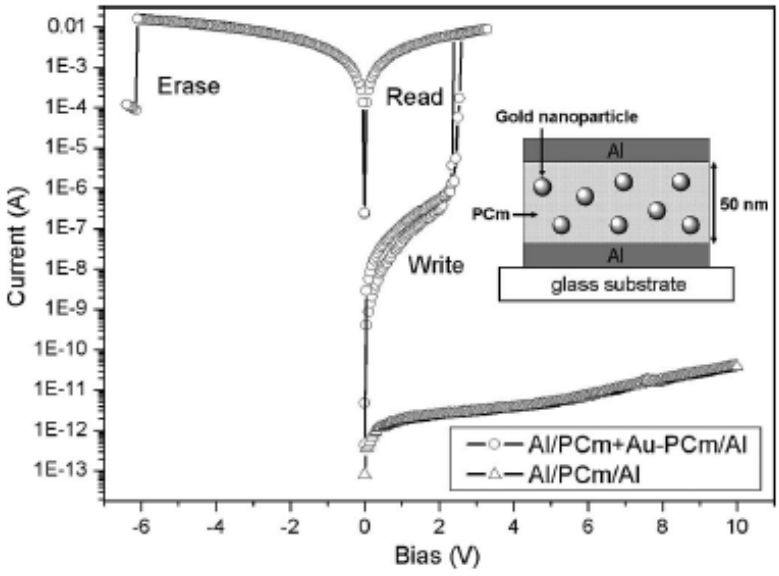


Fig. 1.6: Current-voltage characteristics of Al/PCm: Au nano-particles/Al sandwich structure.

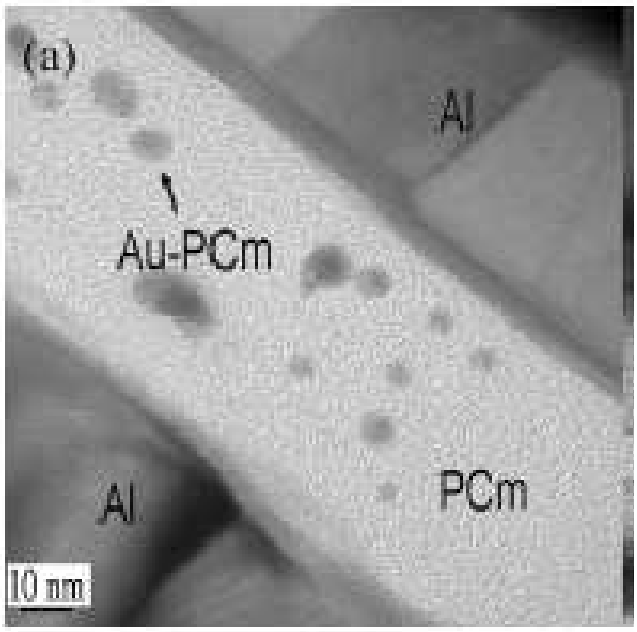


Fig. 1.7: Cross session TFM image of Au nano-particles in PCm matrix.

Some proposed that memory effect and resistive switching of organic RRAM come from its organic materials. Donor-Acceptor typed materials such as m-NBMN/DAB, DC-BDCP complex…etc have been demonstrated as the active layers of the organic RRAM. Y. Ma et al. investigated the arrangement of the donor and the acceptor unit in molecular structure affected the device performance [25]. They classify that the devices based on the D–π–A–π–D molecule exhibit better write–read–erase characteristics with a high ON/OFF ratio than devices based on the A–π–D–π–A molecules.

Charge transfer complexes such as copper 7, 7_, 8, 8_-tetracyanoquinodimethane (Cu-TCNQ) are used as the active layer of the organic

RRAM. According to the current research results, Cu-TCNQ acts as solid ionic conductor (SIC) providing mobile Cu cations, indicates that the mechanism originates from growth and dissolution of conductive Cu filamentary paths [26]. In order to improve the electrical properties of Cu-TCNQ-based device, a porous oxide layer need to add in the device architecture. R. Muller et al. report an inverted device structure which improves the possible damage of Cu-TCNQ layer during the oxide deposition, and they also investigate the device performance with various porous oxides such as SiO_2, Al_2O_3, HfO_2, and ZrO_2. The mechanism of Cu-TCNQ-based organic RRAM is interpreted by growth and dissolution of conducting filamentary paths, and it provides another choice for next generation memory device. However, it needs complicated device architecture and/or expensive process equipments such as atomic layer deposition (ALD) to grow the dedicated layer.

1.3. Models of Carrier Transport

1.3.1. Fowler-Nordheim Tunneling

As depiction in Fig. 1.8, when applied a bias on device, the barrier potential will drop. If we increase the applied bias, the barrier potential will reduce dramatically that cause carrier tunnel through the triangle barrier. The current through the device in case of F-N tunneling is given by [27]:

$$I=C\ V^2 \exp\{[-4d(q\Phi)3/2(2m^*)1/2]/3qhV\} \qquad \text{(Eq. 1.1)}$$

where Φ is the energy barrier height, q is electronic charge, V is applied bias, d is the tunneling distance, m* is the reduced mass of the charge carrier, and C is a constant.

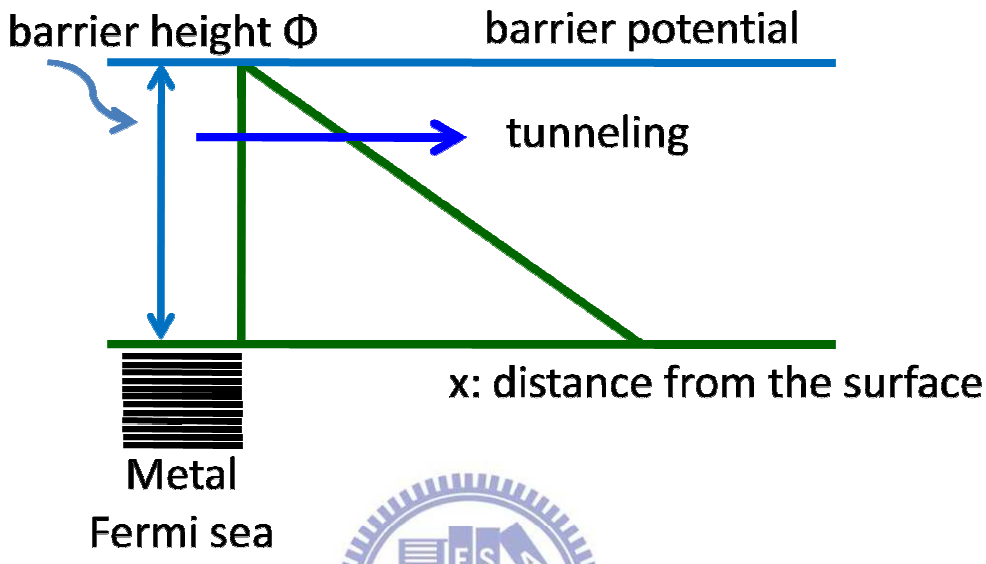


Fig. 1.8: Depiction of F-N tunneling

1.3.2. Poole-Frenkel Emission

If the dielectrical layer contains lots of defects, carrier transport is hopping between defects under a bias as shown in Fig. 1.9. The current through the device in case of P-F emission is given by [27]:

$$I=C\ V \exp[-q/kT(\Phi-(qV/\pi\varepsilon l)^{1/2})] \qquad \text{(Eq. 1.2)}$$

where Φ is the energy barrier height, q is electronic charge, k is Boltzmann constant, V is applied bias, ε is the tpermittivity, T is the temperature, and C is a constant.

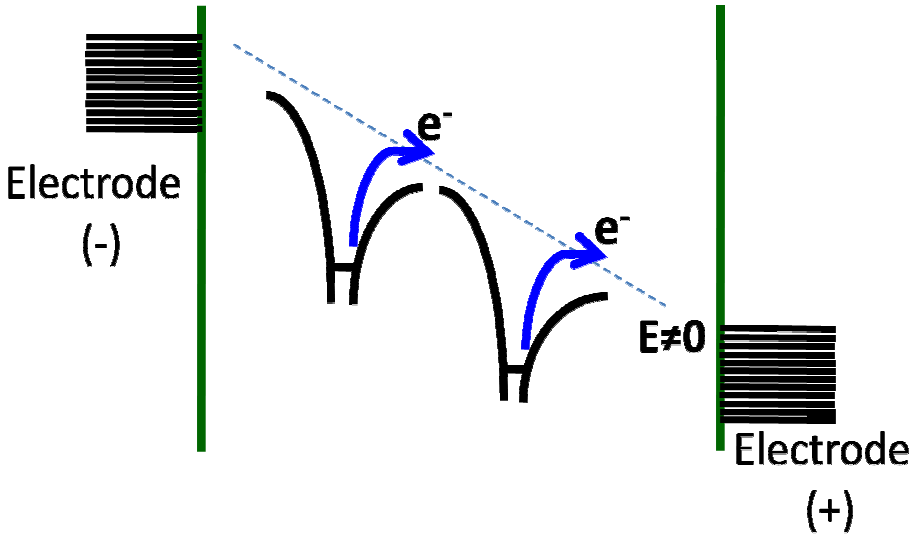


Fig. 1.9: Depiction of P-F emission

1.3.3. Schottky Emission

Schottky emission is also called thermionic emission. The kinetic energy of carrier increases due to the absorption of thermal energy which causes carriers inject across the barrier as shown in Fig. 1.10. The device in case of Schottky emission is given by:

$$I=A^* T^2 \exp[-q(\Phi_B-\beta V^{1/2})/kT] \qquad \text{(Eq. 1.3)}$$

where Φ is the energy barrier height, q is electronic charge, k is Boltzmann constant, V is applied bias, ε is the permittivity, T is the temperature, and A* is effective Richard son constant.

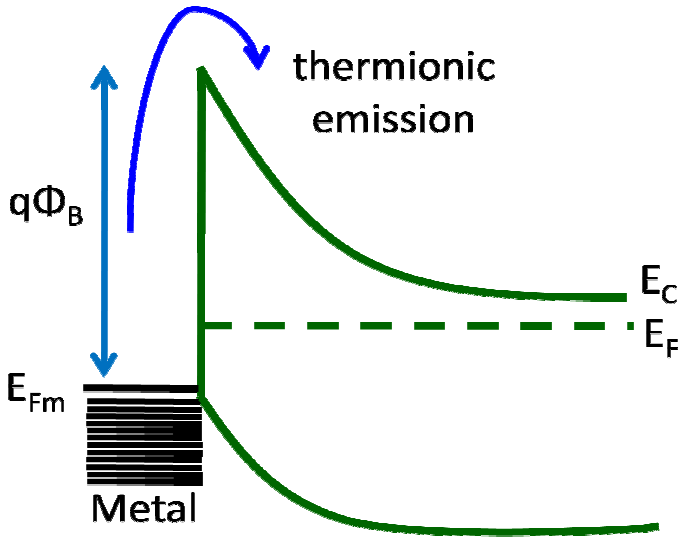


Fig. 1.10: Depiction of Schottky emission

1.3.4. Space Charge Limited Current (SCLC)

Following are some assumptions:

1. The distribution of the electric is uniform

2. Neglect the diffusion of charge carriers

3. No recombination of holes and electrons (monopolar injection)

4. Neglect the thermal equilibrium charge carriers

The current through the device in case of trap-free is given by [28]:

$$I_{spc}=(9/8)\ \varepsilon\ \varepsilon_o\ \mu V^2/L^3 \qquad \text{(Eq. 1.4)}$$

, and for the trap case is given by [28]:

$$I_{spc}=(9/8)\ (n_f/n_f+n_t)\varepsilon\ \varepsilon_o\ \mu V^2/L^3 \qquad \text{(Eq. 1.5)}$$

where μ is mobility, L is thickness, V is applied bias, $\varepsilon\varepsilon_o$ is the dielectrical constant, n_f is the density of free carrier, and n_t is density of trapped carrier.

1.4. Motivation

In recent years, the demands of cost down in production lines and products are becoming most important for device production. The selection of materials and design of device structure are two of the key points to reduce cost. Therefore, we want to demonstrate a potential resistive random access memory (RRAM) with cheap materials and simple fabrication process which can integrates with the well developing process in semiconductor industry nowadays. Moreover, we expect the RRAM can apply to organic electronic products and even manifest the flexible property.

In this work, we demonstrate an inorganic RRAM with low cost materials and simple MIM structure of Ag/SiO_2/p^+-Si. Furthermore, we improve the endurance of device by post-annealing treatment on SiO_2 thin film. The performance and mechanisms of devices are also investigated. Later, we fabricate organic RRAM with bi-layer and tri-layer structure, respectively and both devices exhibit high ON/OFF current ratio. Moreover, we observe the endurance improvement by substituting the metal electrode for the tri-layer structure.

Chapter 2. Inorganic RRAM Using Sputtered SiO_2 films

In this chapter, we focus on the research on $Ag/SiO_2/p^+$-Si structure with different post-annealing SiO_2 conditions. We observe that the device with RTA 800^oC exhibits the best performance of a memory device. Furthermore, we observe a transition of mechanism for the high conductance states which are different from the filamentary mechanism dominated RRAM with MIM structure.

2.1. Fabrication of the RRAM with $Ag/SiO_2/p^+$-Si Structure

The metal-insulator-metal (MIM) device structure of the inorganic RRAM in this study is shown in Fig. 2.1. First, p^+-type silicon substrate is cleaned according to a standard RCA clean process. Then, silicon dioxide (SiO_2) is deposited onto cleaned p^+-type silicon substrate at $5x10^{-3}$ torr using sputter at room temperature. The sputtering power is at 100W, and the thickness is fixed at 100nm. After deposition, two samples are treated as post-annealing using rapid thermal annealing (RTA) with 600^oC and 800^oC, respectively. Finally, an Ag electrode, 100nm thick is evaporated through metal mask with 2mm x 2mm square pattern onto as-deposited, 600^oC and 800^oC RTA treated samples. The parameters of fabrication process are shown in Table 2.1.

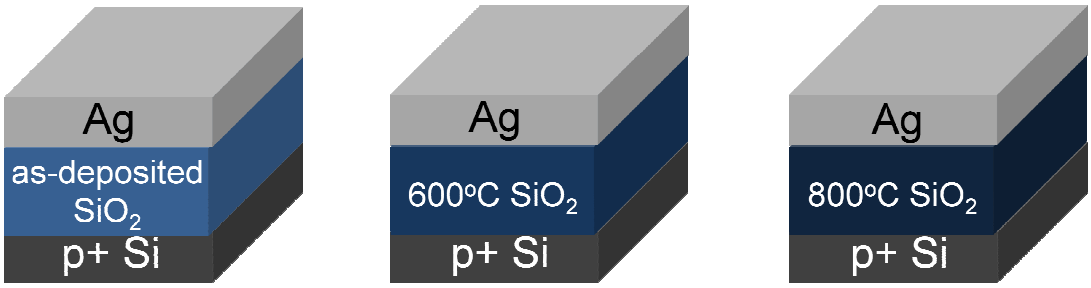


Fig. 2.1: Schematic diagram of Al/SiO_2/p^+-Si structure with different RTA conditions on SiO_2 thin film: (a) as-deposited, (b) RTA 600°C, (c) RTA 800°C.

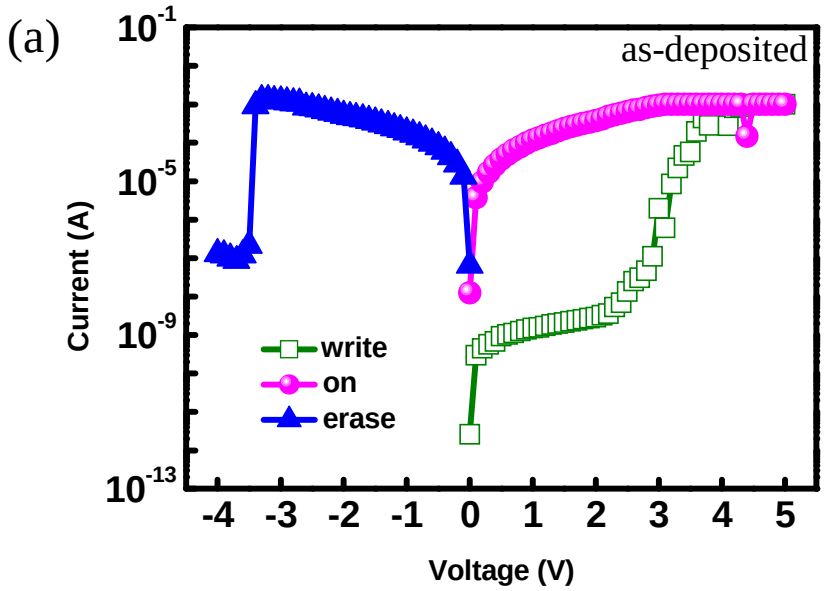
Table 2.1: The parameters of fabrication process of Al/SiO_2/p^+-Si devices

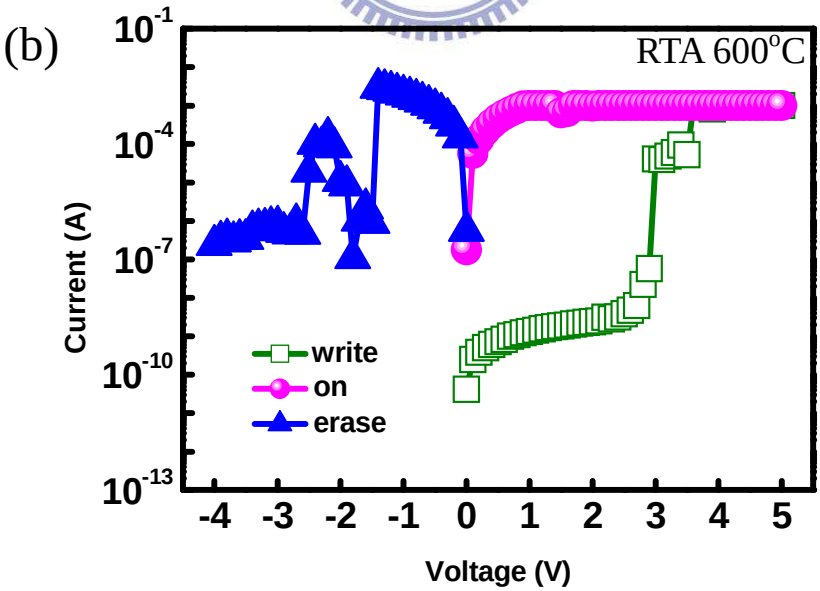
Device	Sample A	Sample B	Sample C
SiO_2 thin film	100nm		
RTA temp.	as deposited	600°C	800°C
Electrode (Ag)	100nm		

2.2. Electrical Characteristics of Ag/SiO_2/p^+-Si RRAM Devices

In our experiment, the electrical characteristics of devices are measured using a Hewlett Packard 4156A (HP 4156A) semiconductor analyzer in ambient environment. The p^+-silicon substrate is grounded, and all bias conditions are applied on the silver electrode. In addition, the scanning interval of voltage is set to 100mV per step in sweeping mode. Fig. 2.2 shows the electrical characteristics of as-deposited, 600°C and 800°C RTA treated samples, respectively. Initially, this device keeps at low

conductance state with low current level. However, when sweeping voltage exceed to threshold voltage, 4V, 4V and 4.5V, which are individually corresponding to as-deposited, RTA 600^{o}C and 800^{o}C treated samples, an abruptly increase of current is observed. Then, devices keep at high conductance state with a high current level. The sweeping process switches the device form low conductance state (OFF state) to high conductance state (ON state), which is called writing process (green squares line). When the sweeping voltage from 0V to 5V is applied again, these devices still hold at high conductance state with high current level, which is called reading process (magenta circles line). At third sweeping process, the reverse voltage from 0V to -4V is applied. A noticeable drop of current from high conductance state to low conductance state is observed. After the reducing of current, all devices are turn back and kept at low conductance state with a low current level, which is called erasing process. The parameters of performance of as-deposited, RTA 600^{o}C and 800^{o}C treated samples are listed in Table 2.2. The V_t, V_{th}, and ON/OFF current ratio increase with increasing RTA temperature.


(a)
as-deposited
Current (A)
Voltage (V)
write
on
erase


(b)
RTA 600°C
Current (A)
Voltage (V)
write
on
erase

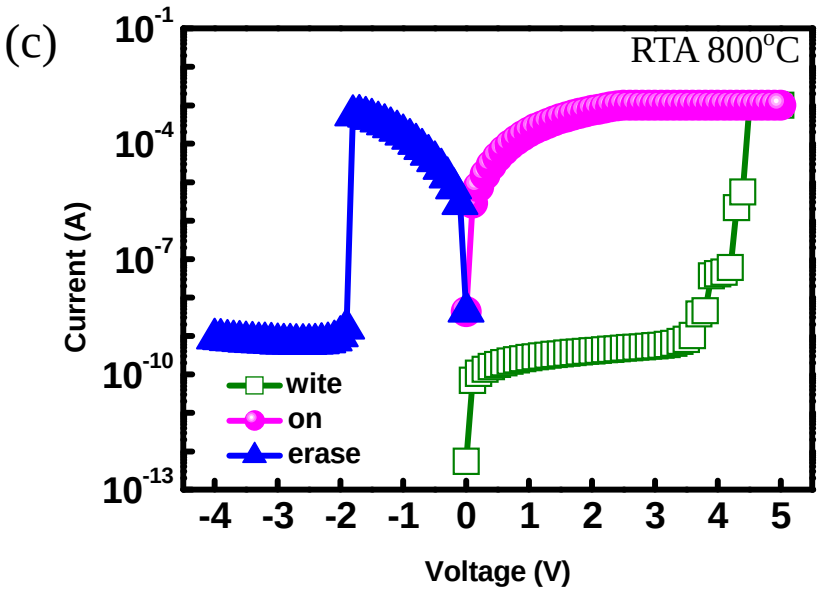


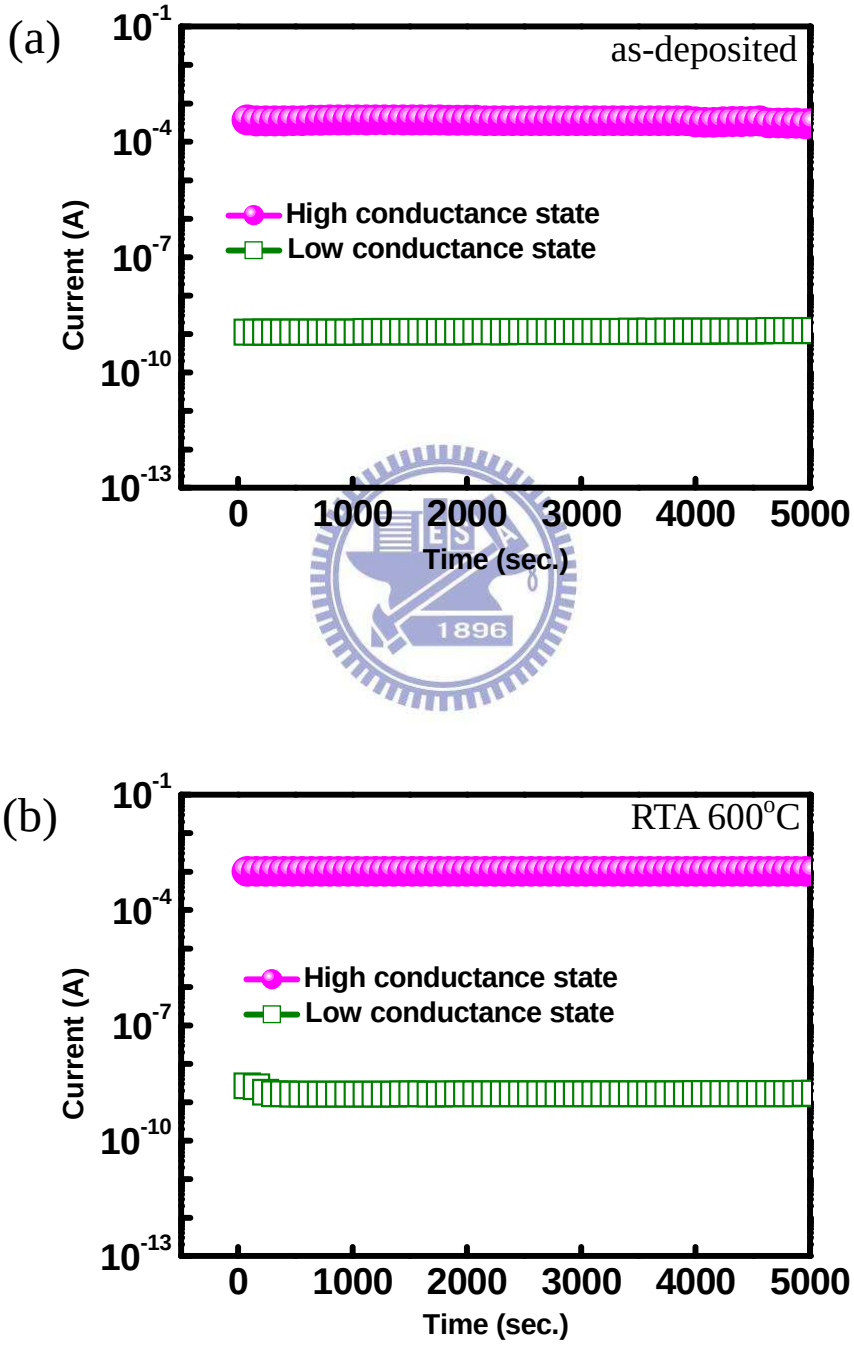
Fig 2.2: The current-voltage characteristics of Al/SiO_2/p^+-Si structure with different RTA conditions on SiO_2 thin film: (a) as-deposited, (b) RTA 600°C, (c) RTA 800°C.

Table 2.2: The parameters of electrical measurements of Al/SiO_2/p^+-Si devices

Condition	ON/OFF ratio	Transition Voltage	Threshold Voltage
as-deposited	10^5	~2.5V	4V
600°C RTA	10^5	~3V	4V
800°C RTA	10^6	~4V	4.5V

Fig. 2.3 shows the long retention time over 5000 seconds of samples with different RTA conditions, and exhibited quite stable ON/OFF current ratio without any degradation during the retention time measurement. The current level of ON and

OFF states for samples with different RTA conditions in retention time measurement are shown in Table 2.3.



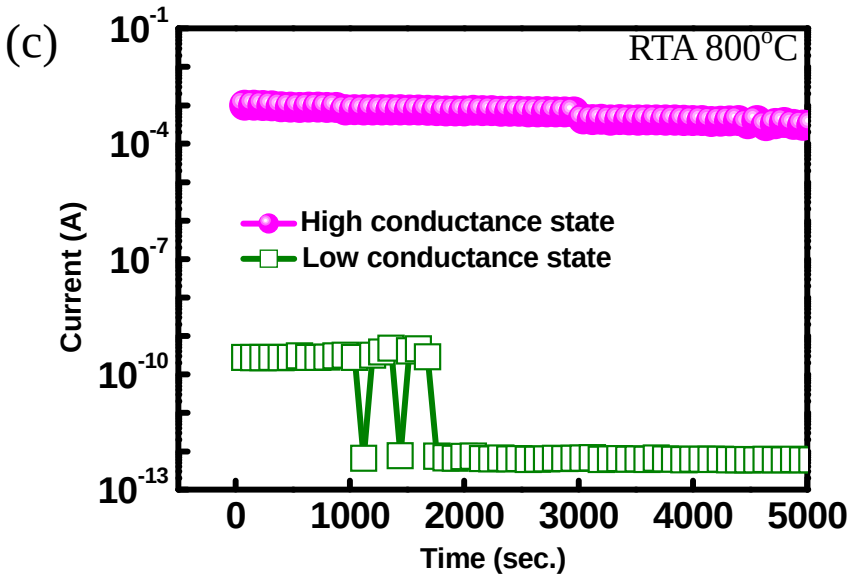


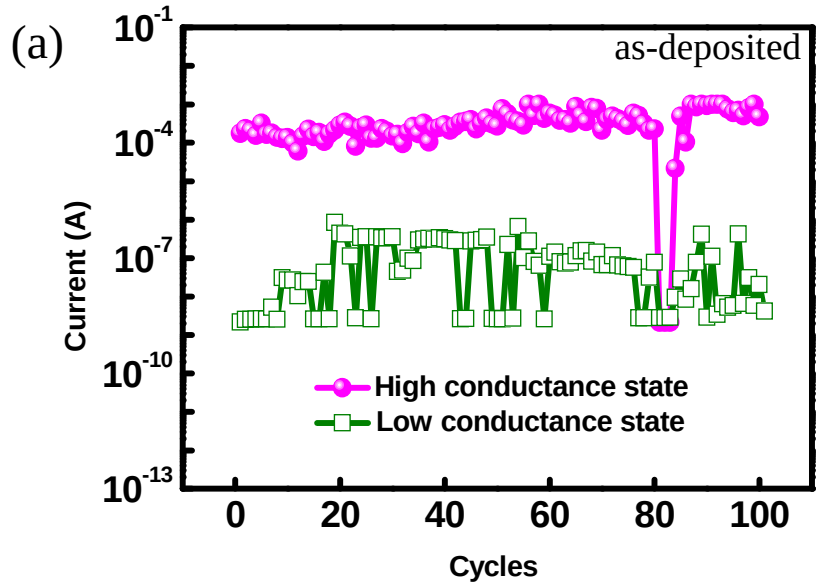
Fig 2.3: The retention times of $Al/SiO_2/p^+$-Si structure with different RTA conditions on SiO_2 thin film: (a) as-deposited, (b) RTA 600°C, (c) RTA 800°C.

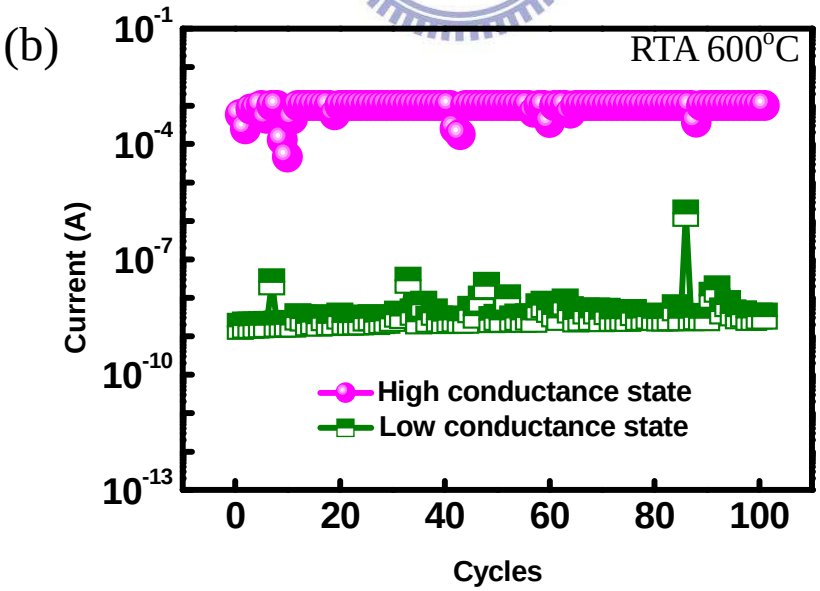
Table 2.3: The measurements of retention time of $Al/SiO_2/p^+$-Si structure with different RTA conditions

Condition	ON current	OFF Current	Retention time
as-deposited	10^{-4}	10^{-9}	over 5000s
600°C RTA	10^{-3}	10^{-9}	over 5000s
800°C RTA	10^{-3}~10^{-4}	10^{-10}~10^{-13}	over 5000s

The cycle times of (operation), also called endurance test, is one of the most important properties about the performance of a memory device. For investigation,

the writing, reading, erasing and reading processes are executed in sequence by 5V, 1V, -4V, and 1V AC pulse for devices with different RTA conditions. To ensure the consistence of measurement, here we apply the same writing, erasing, and reading voltages on all devices. As shown in Fig. 2.4, the cycles of as-deposited, RTA 600^{o}C and 800^{o}C treated samples are 80, 90, and 280 times, respectively. We observe that the cycles increase with increasing RTA temperature, and the high and low conductance currents are becoming more stable with increasing RTA temperature, especially at 800^{o}C. Obviously, the as-deposited device shows a large perturbation between the high and low conductance current, and device with RTA 800^{o}C treatment shows the most cycle times and best performance. In short, the endurance of Ag/SiO_2/p^+-Si structure is improved by increasing RTA temperature on SiO_2 thin film. The current levels of ON and OFF states with different RTA conditions in endurance measurement are shown in Table 2.4.


(a)
as-deposited
Current (A)
10-1
10-4
10-7
10-10
10-13
0
20
40
60
80
100
Cycles
High conductance state
Low conductance state


(b)
RTA 600°C
Current (A)
10-1
10-4
10-7
10-10
10-13
0
20
40
60
80
100
Cycles
High conductance state
Low conductance state

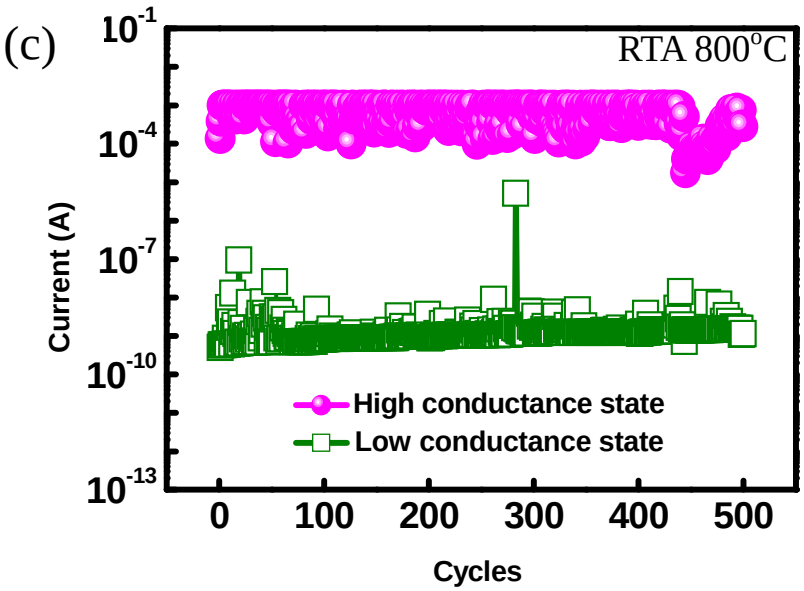


Fig 2.4: The write-read-erase-read cycles of Al/SiO_2/p^+-Si structure with different RTA conditions on SiO_2 thin films: (a) as-deposited, (b) RTA 600°C, (c) RTA 800°C.

Table 2.4: The measurements of endurance of Al/SiO_2/p^+-Si structure with different RTA conditions

Condition	ON current	OFF Current	Cycles
as-deposited	10^{-4}	10^{-6}~10^{-9}	80
600°C RTA	10^{-3}~10^{-5}	10^{-7}~10^{-9}	90
800°C RTA	10^{-3}~10^{-4}	10^{-7}~10^{-10}	280

2.3. Mechanism and Discussion

2.3.1. Mechanism

At first, we investigate the optical properties of SiO_2 thin film using Raman scattering measurements. As shown in Fig. 2.5, the intensity of the peak at 610nm increases with increasing RTA temperature, and it indicates the 3-fold ring defects are produced by thermal compressive stress [29]. Therefore, we know that the properties of SiO_2 thin films are varied after RTA treatment, and this result may affect the carrier transportation and mechanism of resistive switching in the SiO_2 thin films.

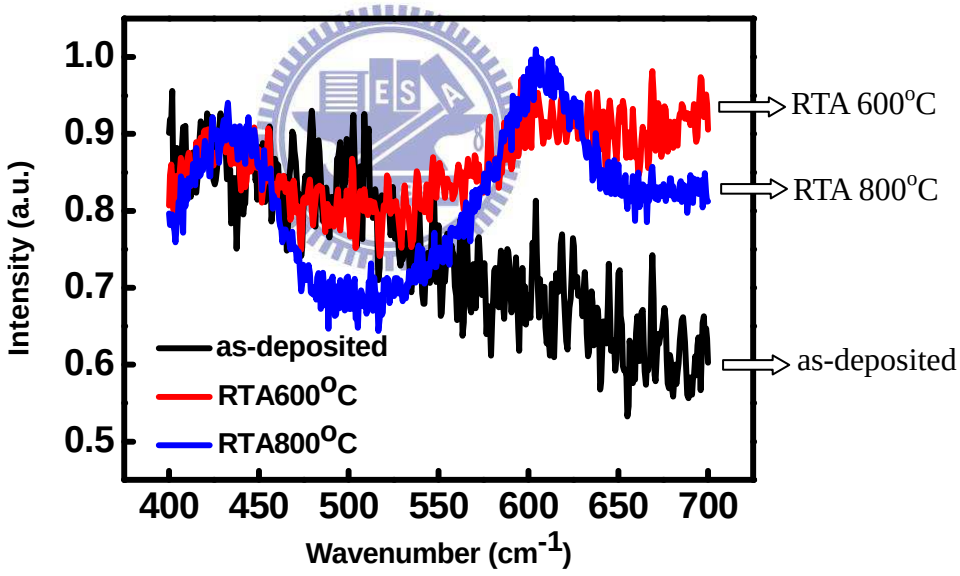
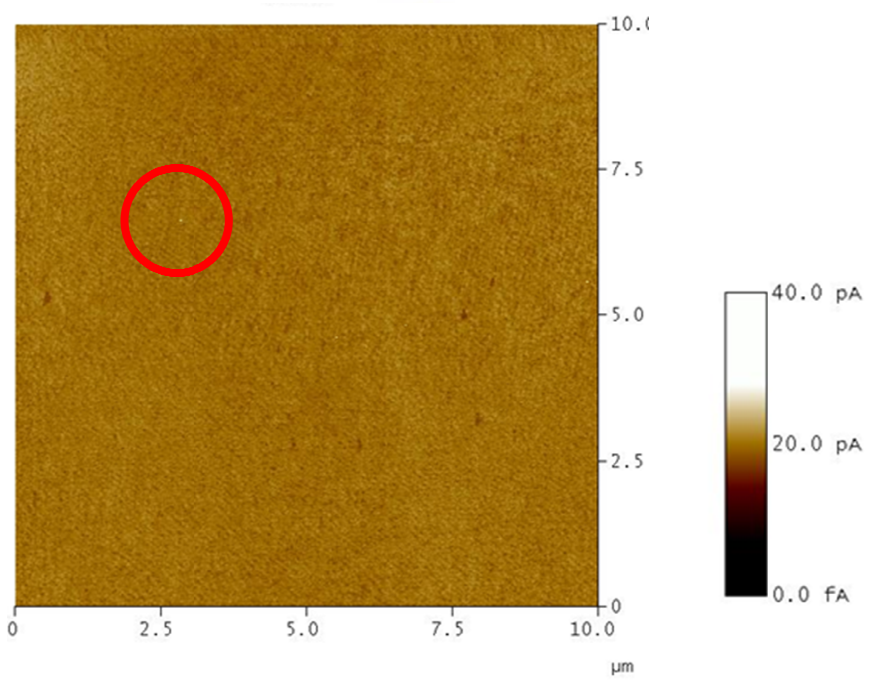


Fig. 2.5: Raman spectrum of SiO_2/p^+-Si structure with as-deposited, RTA 600°C, and RTA 800°C treatments on SiO_2 thin films.

The formation of conductive filamentary paths in oxide films dominates the resistive switching has been widely discussed and proposed. To verify the mechanism

of resistive switching of the as-deposited SiO_2 thin film, we use the conductive atomic force microscope (c-AFM) to scan the SiO_2 thin film, which keeps at ON state. Fig. 2.6 shows the c-AFM image of the as-deposited SiO_2 thin film, a few conductive channels are observed. This result indicates the as-deposited SiO_2 thin film may have similar conductive filamentary property in the high conductance state. However, such few conductive channels are probably not the only source, which is dominating the resistive switching.



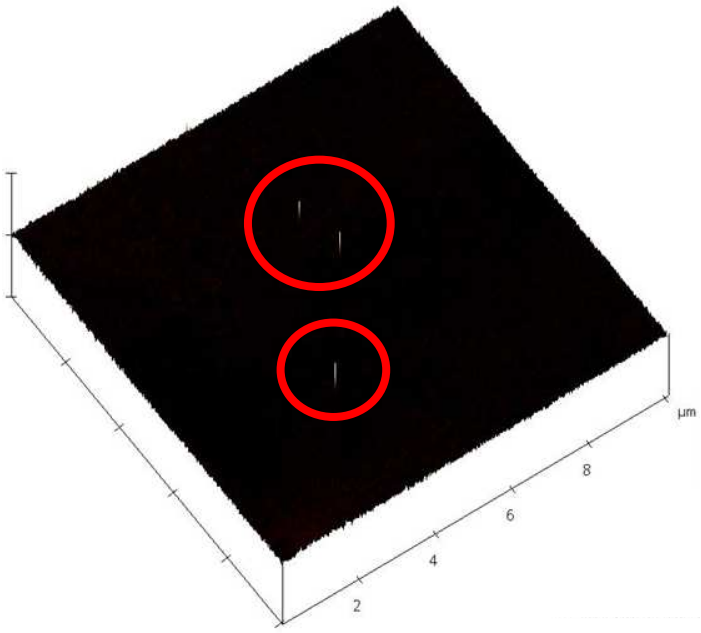


Fig. 2.6: The c-AFM images of SiO_2/p^+-Si structure: (a) 2-D, and (b) 3-D.

If the conductive filamentary property originates from silver cations, we can expect the current in high conductance state will decrease with increasing temperature due to the metallic property. To verify the point above mentioned, the current-voltage measurements of as-deposited, RTA 600^{o}C, and 800^{o}C treated samples under different temperature are investigated. As shown in Fig. 2.7, the current-voltage relation versus temperature shows a clear independence, it suggests the carrier transport in high conductance state isn't dominated by metallic filamentary path. In addition, the temperature-independent property also implies the high conductance current, in the as-deposited sample, isn't dominated by Poole-Frenkel emission.

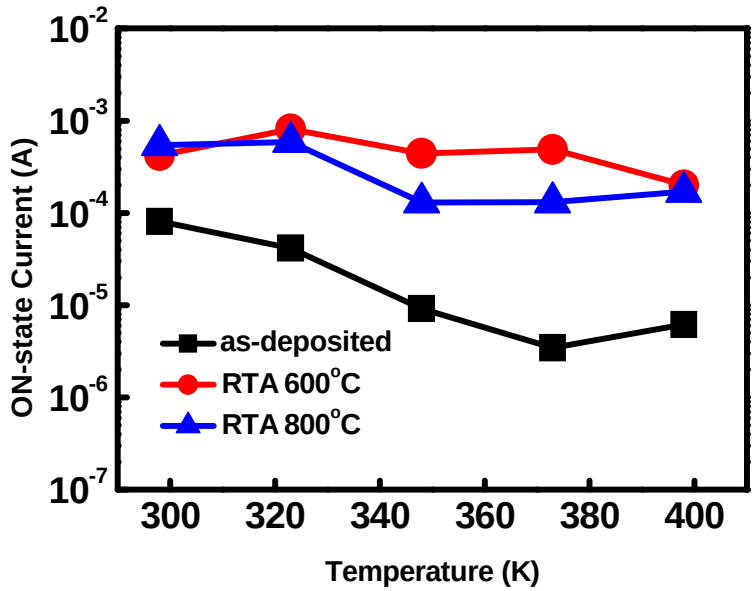
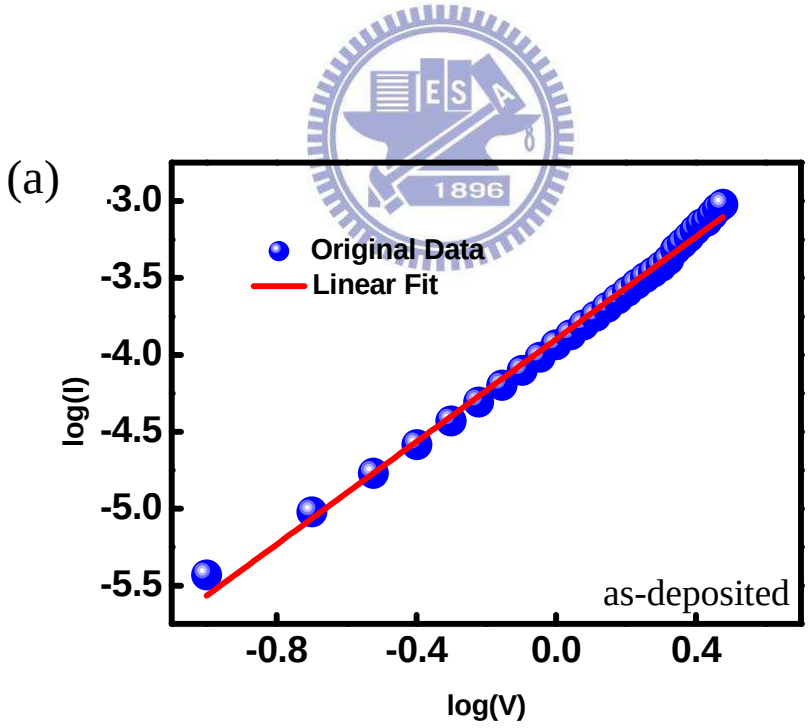


Fig. 2.7: The current-voltage measurements of as-deposited, RTA 600°C, RTA 800°C treated samples under various temperatures from 298K to 398K.

2.3.2. Curve Fitting of I-V Currents

Mechanism of filamentary path formation and rupture has been proposed to explain the resistive switching. According to the filamentary model, the high conductance current exhibits an ohmic conduction property, it also means that current (I) will proportion to biased voltage (V^1). Therefore, we investigate the transport characteristics by analyzing the I-V relationship. Fig. 2.8 illustrates the I-V relationship of the high conductance state in a log-log scale for the various treated samples. As can be seen, all of the curves are well fitted with the linear form, meaning that, space charge limited current (SCLC) in the presence of traps is responsible for

carrier transport at the high conductance state. However, the slopes of the fitting curve are about 1.6 and 1.8 for as-deposited, and RTA 600^{o}C treated samples, respectively, suggesting not only SCLC properties but also resistive properties in both samples. In addition, the slope of the fitting curve for RTA 800^{o}C treated sample is close to 2. Due to the results of the curve fitting about the high conductance state, we observe a transition of carrier transport mechanism from SCLC combined with resistive property to pure SCLC property with different RTA conditions. The results of curving fitting are sorted out and displayed in Table 2.5.



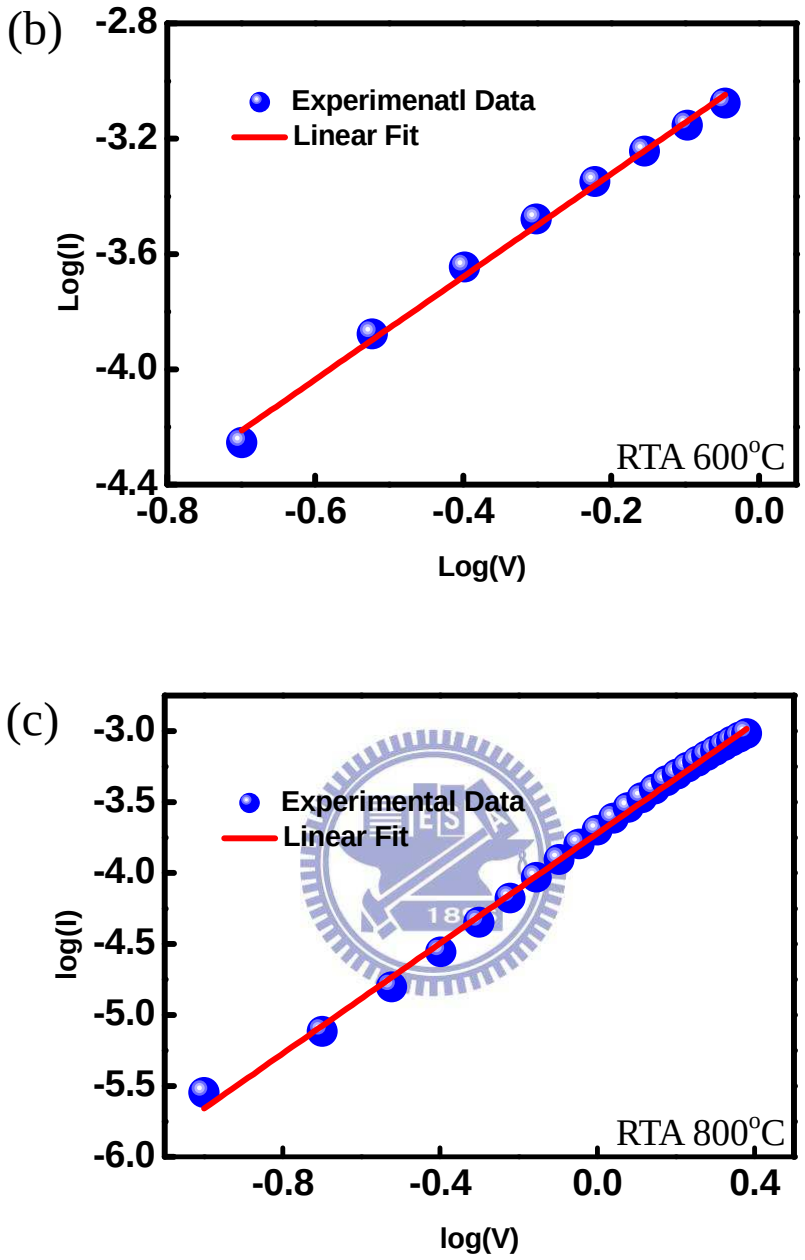


Fig. 2.8: Curve fitting of the I-V curves of the high conductance state of Al/SiO_2/p^+-Si structure in a log-log plot: (a) as-deposited, (b) RTA 600°C, (c) RTA 800°C.

Table 2.5: Fitting results of the high conductance states of Al/SiO_2/p^+-Si structure with different RTA conditions

Condition	Slope (S)	Indicated Mechanism
as deposited	1<S<2	SCLC and ohmic property
600°C RTA	1<S<2	SCLC and ohmic property
800°C RTA	S~2	SCLC

In order to confirm the probable mechanism for carrier transport in the high conductance state, the device with RTA at 800°C is compared with the as-deposited and RTA at 600°C ones. Since a large amount of defects exist in SiO_2 thin films, the defects should be very close to each other. When we applied a suitable bias on device, the defects will form some localized filamentary paths, providing carrier transport through the device, since that, an ohmic conduction will be observed, as shown in Fig. 2.9 (a). On the other hand, some carriers are trapped by defects but through the filamentary paths, and the other carriers can transport through SiO_2 thin film without any influence by defects, as a result, it shows a transport property of SCLC. According to the previous analyses, we suggest the devices with as-deposited and RTA at 600°C exhibit a mixing property by SCLC and ohmic conduction. However,

the device with RTA at 800°C is more condensed and contains a fewer defects, it causes a significant increase on the average distance of defects. Hence, the carriers trapped in defects couldn't tunnel through defects, and then, it exhibits a pure SCLC property, as shown in Fig. 2.10.

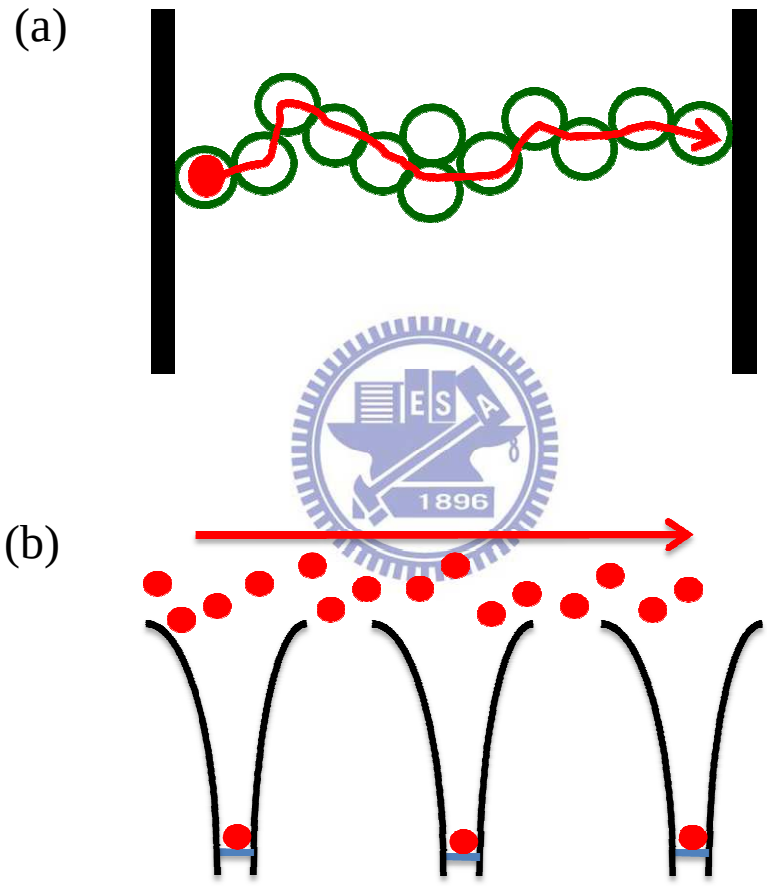


Fig. 2.9: Paths of carrier transport for as-deposited and RTA 600°C treated samples: (a) path1: conductive filaments, and (b) path2: SCLC

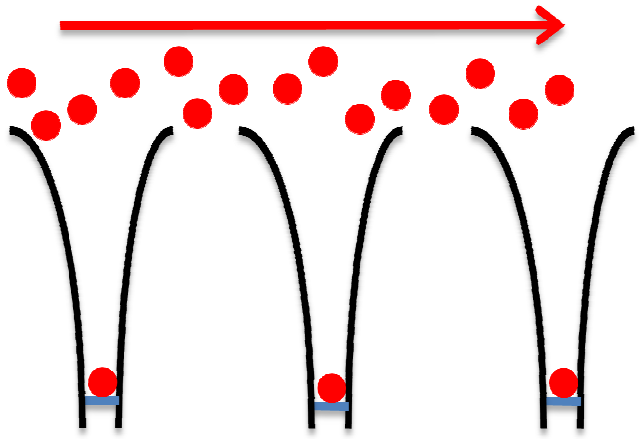


Fig. 2.10: Depiction of Mechanisms of carrier transport in the high conductance state for RTA 800^{o}C treated sample.

To elucidate the results of curve fitting of the high conductance states in different samples and the proposed mechanisms, the C-V characteristics are shown in Fig. 2.11. It depicts that the flat band voltage (V_{FB}) shifts from about -7V to -1V with increasing RTA temperature, meaning that, the total defects in SiO_2 thin film decrease with increasing RTA temperature and the quality of SiO_2 thin film is improved by RTA treatment. Such results are well corresponding to the previous suggestion about the carrier transport mechanisms under various RTA conditions.

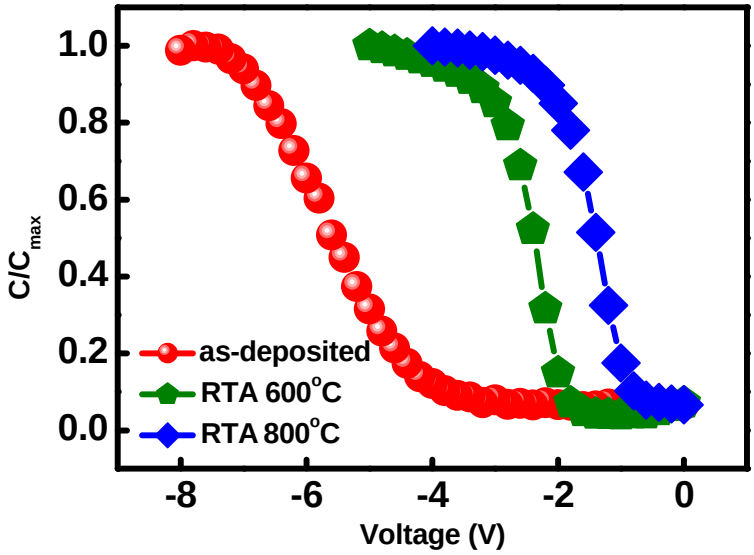
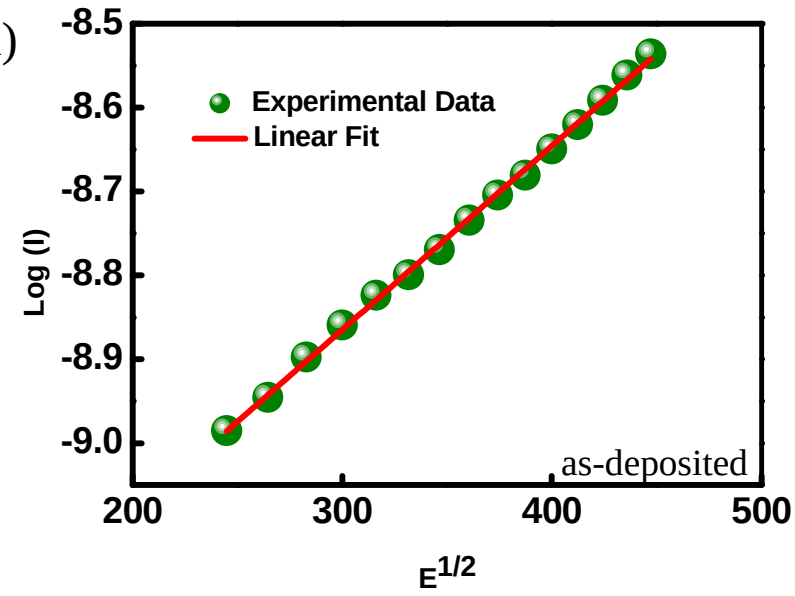


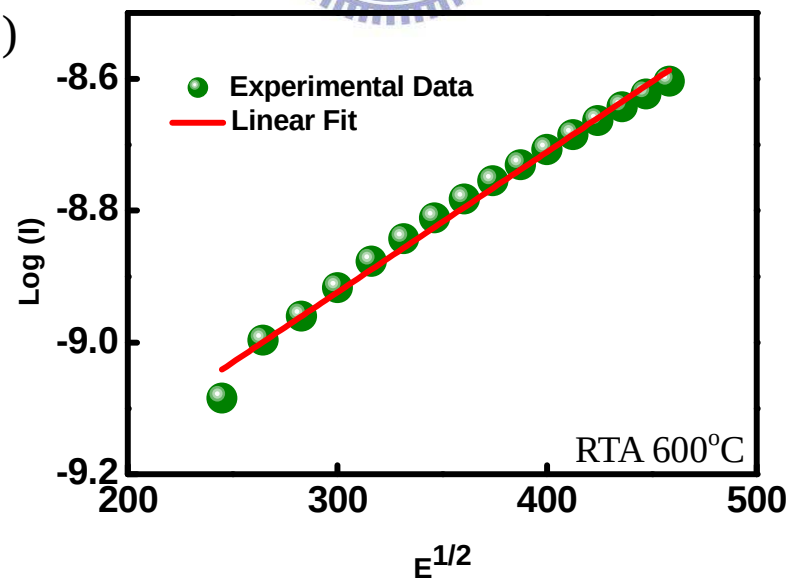
Fig. 2.11: C-V characteristics of Ag/SiO_2/p-Si/Au structure of the as-deposited, RTA 600°C, and RTA 800°C treatments.

Furthermore, the low conductance currents of devices with various RTA cinditions are fitted with Shottky emission model in log (I) versus $E^{1/2}$ plots, respectively. As shown in Fig. 2.12, a linear relationship is observed, meaning that, the carrier injection of the low conductance currents is limited. Unsurprising fitting results of low conductance currents are obtained due to the existence of a large barrier height between silver and SiO_2 thin film.

(a)


-8.5
-8.6
-8.7
-8.8
-8.9
-9.0
Log (I)
Experimental Data
Linear Fit
as-deposited
200
300
400
500
E1/2

(b)


-8.6
-8.8
-9.0
-9.2
Log (I)
Experimental Data
Linear Fit
RTA 600°C
200
300
400
500
E1/2

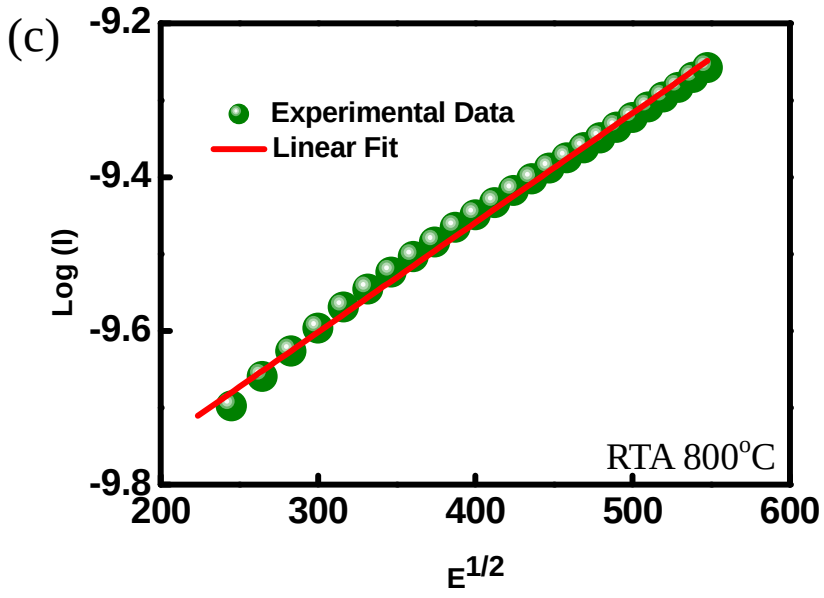


Fig. 2.12: Fitting of the I-V curve of the low conductance state of $Al/SiO_2/p^+$-Si structure under different RTA conditions in a log (I) - $E^{1/2}$ plot: (a) as-deposited, (b) RTA 600°C, and (c) RTA 800°C.

2.4. Summary

The RRAM device performances are list in Table 2.6. The memory properties of $Ag/SiO_2/p^+$-Si structure with different RTA conditions are investigated and the RTA 800^oC device shows the better performance. Moreover, the transition of mechanism in the high conductance state is also proposed and discussed in this study.

Table 2.6: The performance of $Ag/SiO_2/p^+$-Si structure under different RTA conditions

SiO_2 (100nm)	**ON/OFF Ratio**	**Retention Time**	**Cycles**	**Transition Voltage**	**Threshold Voltage**
As-deposited	10^5	Over 5000s	80	~2.5V	4V
RTA (600^OC)	10^5	Over 5000s	90	~3V	4V
RTA (800^oC)	10^6	Over 5000s	280	~4V	4.5V

Chapter 3. Organic RRAM Using Metal Oxide

3.1. Introduction

In this chapter, we fabricate two different structures of organic RRAM. One of them is $Al/AlO_x/Alq_3/n^+$-Si bi-layer structure, and the other one is $Al/Alq_3/MoO_3/Alq_3/p^+$-Si tri-layer structure (sandwich structure). Both devices of bi-layer and tri-layer structure can achieve high on/off current ratio about six orders and four orders in magnitude, respectively. At first, we propose a simpler device structure exhibiting the high on/off current ratio than tri-layer structure. Therefore, the $Al/AlO_x/Alq_3/n^+$-Si bi-layer structure is fabricated. However, the deposition of AlO_x needs a high temperature process, and we deposit AlO_x by e-gun system in this work. In addition, this bi-layer structure is subjected to cycling problem which is that device can't be written and erased for many times. Therefore, to demonstrate an organic RRAM with low temperature process fabrication for application of electronic products, we fabricate $Al/Alq_3/MoO_3/Alq_3/p^+$-Si tri-layer structure to manifest this ideal. Moreover, we investigate the electrical properties and the electrode effect on $Al/Alq_3/MoO_3/Alq_3/p^+$-Si device.

3.2. Fabrication of the Organic RRAM

3.2.1. Al/AlO_x/Alq_3/n^+-Si bi-layer structure

The device structure of the organic RRAM consisting of organic/metal-oxide bi-layer structure interposed between anode and cathode in this study is shown in Fig. 3.1 (a). First, n^+-type silicon substrate is cleaned according to standard RCA clean process. Then, tris-(8-hydroxyquinoline) aluminum (Alq_3), whose structural formula is given in Fig. 3.1 (b), is evaporated onto cleaned n^+-type silicon substrate in a vacuum below $3x10^{-6}$ torr at room temperature. The deposition rate and thickness of the Alq_3 thin film are about 0.1nm/s and 45nm, respectively. Afterwards, 10nm thick aluminum oxide (AlO_x) with deposition rate of 0.01nm/s is deposited by e-beam evaporation at pressure below $4x10^{-6}$ torr at room temperature. Finally, 100nm thick Al thin film is evaporated through metal mask with 2mm x 2mm square pattern onto devices as top electrode. The parameters of fabrication process are shown in Table 3.1.

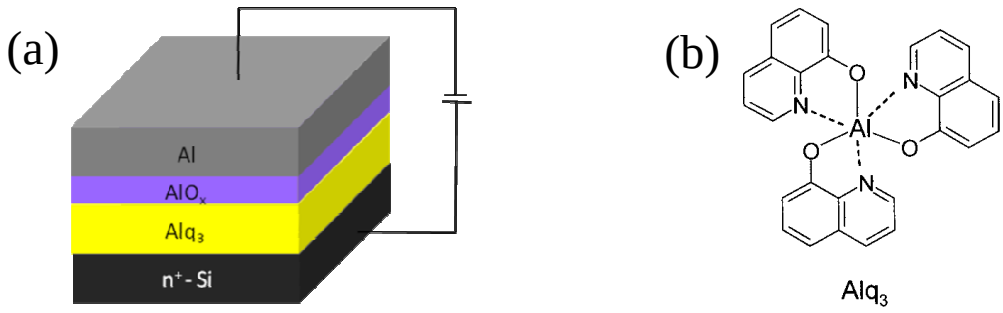


Fig. 3.1: (a) Schematic diagram of Al/AlO_x/Alq_3/n^+-Si structure. (b) Structural formula of Alq_3.

Table 3.1: The parameters of fabrication process of $Al/AlO_x/Alq_3/n^+$-Si device

Bi-layer structure	**AlO_x**	**Alq_3**	**Al electrode**
Vacuum Value	$4x10^{-6}$ Torr	$3x10^{-6}$ Torr	$6x10^{-6}$ Torr
Thickness	10nm	45nm	100nm
Evaporation Rate	0.01nm/s	0.1nm/s	0.2nm/s

3.2.2. $Al/Alq_3/MoO_3/Alq_3/p^+$-Si tri-layer structure

The organic RRAM consisted of an Alq_3/ MoO_3 nano-clusters/Alq_3 tri-layer structure interposed between anode and cathode is shown in Fig. 3.2 (a). First, a p^+-type silicon substrate is cleaned according to a standard RCA clean process. A 50 nm thick Alq_3 thin film is evaporated onto the cleaned p^+-type silicon substrate at pressure below $3x10^{-6}$ torr at room temperature. Then, 5 nm thick MoO_3, and 50 nm thick Alq_3 thin films are evaporated in sequence onto the Alq_3/p^+-Si. The average deposition rate of the Alq_3 thin film and that of the MoO_3 layer are about 0.1nm/s and 0.01nm/s, respectively. Finally, 100nm thick Al thin film is evaporated through metal mask with 2mm x 2mm square pattern onto Alq_3/ MoO_3 nano-clusters/Alq_3/p^+-Si as top electrode. Furthermore, Standard device of 100nm thick Alq_3 layer is also fabricated, and device structure is shown in Fig. 3.2 (b). The parameters of fabrication process are shown in Table 3.2.

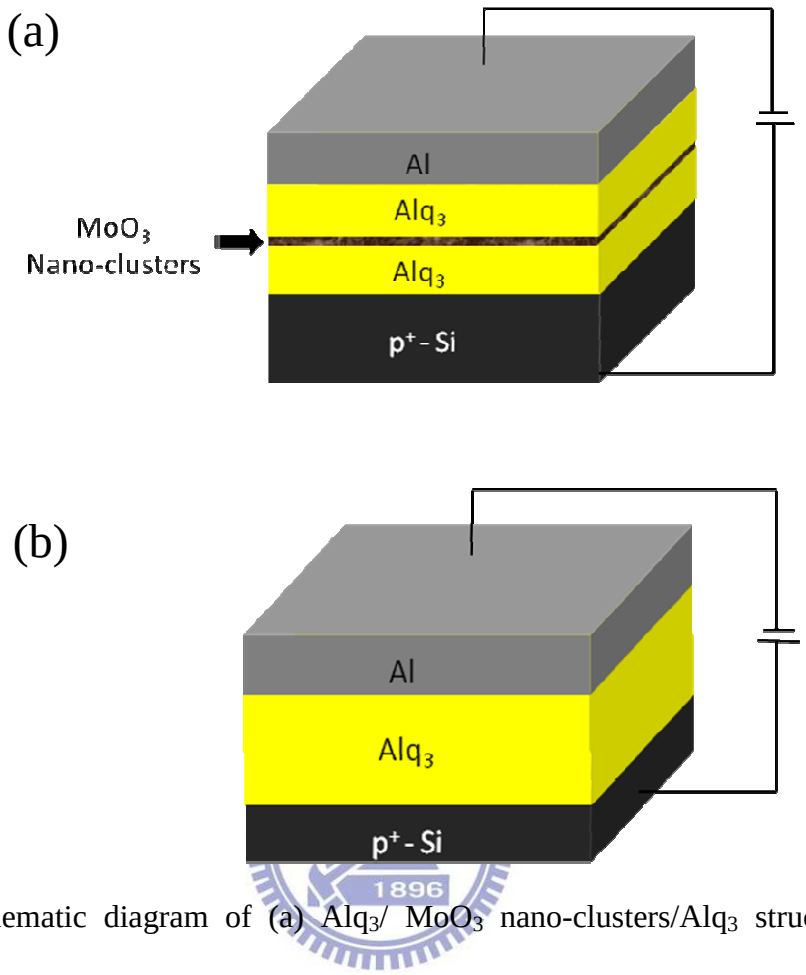


Fig. 3.2: Schematic diagram of (a) Alq_3/ MoO_3 nano-clusters/Alq_3 structure. (b) Standard devices of Alq_3 single layer.

Table 3.2: The parameters of fabrication process of Al/Alq_3/MoO_3/Alq_3/p^+-Si device

Tri-layer structure	**Alq_3**	**MoO_3**	**Alq_3**	**Al electrode**
Vacuum Value	$3x10^{-6}$ torr	$3x10^{-6}$ torr	$3x10^{-6}$ torr	$6x10^{-6}$ torr
Thickness	50nm	5nm	50nm	100nm
Evaporation Rate	0.1nm/s	0.01nm/s	0.1nm/s	0.2nm/s

3.3. Organic RRAM with AlO_X/Alq_3 Bi-layer Structure

3.3.1. Electrical Characteristics

In our experiment, the electrical characteristics of devices are measured using a Hewlett Packard 4156A (HP 4156A) semiconductor analyzer in ambient environment. The n^+-silicon substrate is grounded, and all bias conditions are applied to the aluminum electrode. In addition, the scanning interval of voltage is set to 100mV per step in sweeping mode. Fig. 3.3 shows the current-voltage (*I-V*) characteristics of the fabricated device with $Al/AlO_x/Alq_3/n^+$-Si Structure. First, when a negative bias from 0V to -5V is applied on the Al electrode with 100mA current compliance, the current is in the low conductance state with a current level of 10^{-13}~10^{-6}A (red solid sphere curve). As the bias is applied at about -5V, there is an abruptly increase in current. Then the current of the device keeps at high conductance state with a current compliance (100mA) for the applied voltage above -5V (red solid sphere curve). This device undergoes a resistive switching from low conductance state to high conductance state which is called writing process. Furthermore, the device always maintains at a high conductance state no matter the voltage sweep from -10V back to 0V or from 0V to -10V. As can be see, this device exhibits two different conductance states with an ON/OFF current ratio close to 10^6. Nevertheless, when applied a reverse bias from 0V to 10V, this device is in the low conductance state. Then the

device undergoes a resistive switching. This similar electrical transition is called erasing process (blue open square curve). In addition, this device can be turned to high conductance state again when a sweeping bias from 0V to -10V is applied on device again (green open circle curve). Due to the observed electrical characteristics, this device exhibits memory properties which are bistability and re-writability.

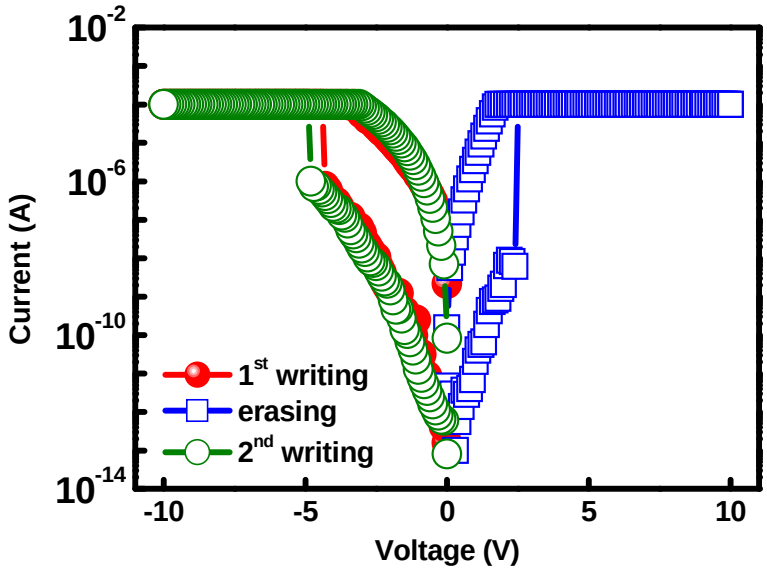


Fig. 3.3: Typical I-V curves of the Al/AlO_x/Alq_3/n^+-Si structure. The red (-●-) and green (-○-) curves are 1st and 3rd voltage sweepings from 0V to -10V, respectively. The blue (-□-) curve is reversed bias sweeping from 0V to 10V.

Retention time is the important property of the organic RRAM. The retention time of Al/AlO_x/Alq_3/n^+-Si structure is measured at -0.5V in a period of 80 seconds in ambient environment. As shown in Fig. 3.4, an average current level of high

conductance state is 10^{-7}A at -0.5V, while the average current level of low conductance state is 10^{-12}A at -0.5V. In spite of a fluctuation in high conductance state, there is no significantly degradation for both states over 1500 seconds. This reveals that the Al/AlO_x/Alq_3/n^+-Si structure can maintain quite stable ON/OFF current ratio. Such large ON/OFF current ratio can reduce reading errors and increase the device reliability.

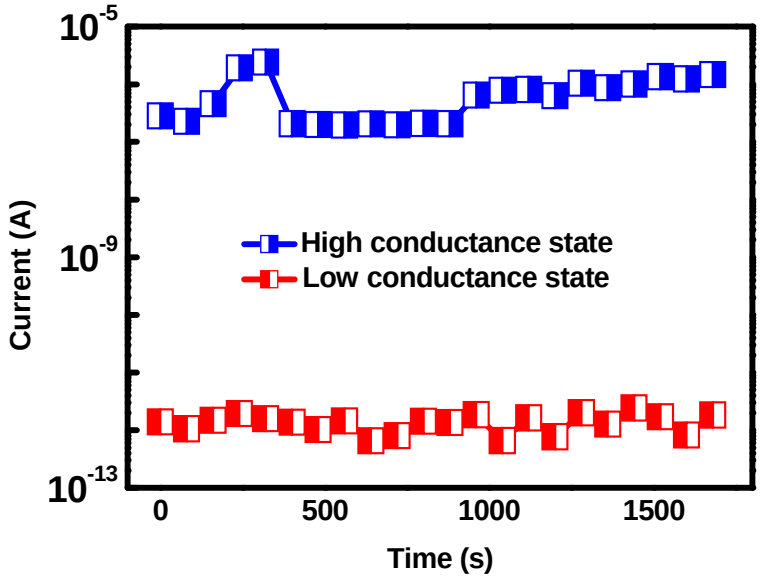


Fig. 3.4: Retention measurement of the reported Al/AlO_x/Alq_3/n^+-Si structure.

3.3.2. Mechanism

The mechanisms of organic RRAM has been widely investigated and proposed. Charging and decharging of carriers in charge trapping centers, formation and fracture of metallic filamentary paths and oxygen vacancies in insulator films, and oxidation

and reduction of solid electrolyte…etc are addressed to interpret for their work. However, the exact mechanisms are still not clearly understood and under debate yet.

According to the electrical characteristics observed in this work, it's totally different from electrical characteristics of filamentary paths dominated. The mechanism of filamentary paths formation is described in section 1.2.2.

To further investigate the mechanism of electrical characteristics of the Al/AlO_x/Alq_3/n^+-Si structure, we also fabricate two kinds of samples with single layer AlO_x or Alq_3 as shown in Fig 3.5. The fabrication parameters are described in section 3.2.1.

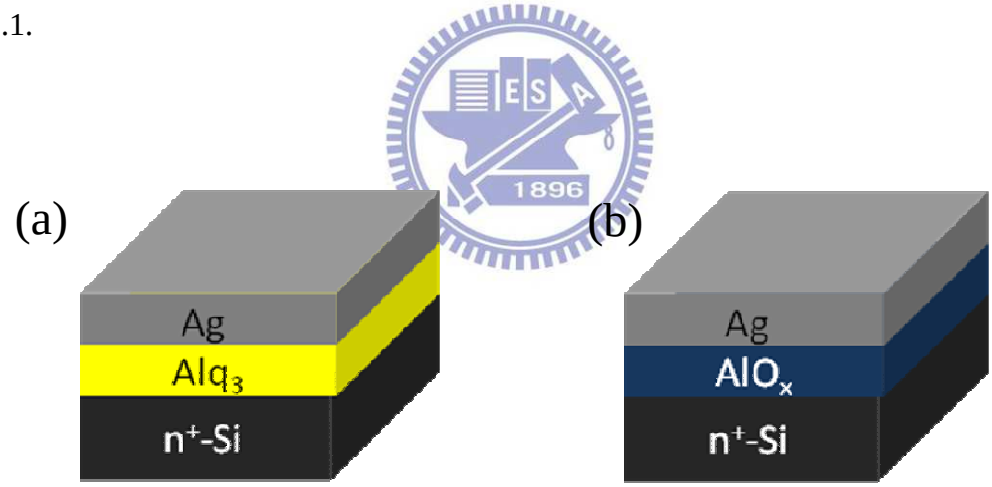


Fig. 3.5: (a) Schematic diagram of the Ag/Alq_3/n^+-Si structure, (b) the Ag/AlO_x /n^+-Si structure.

The electrical characteristics of Ag/Alq_3/n^+-Si structure and Ag/AlO_x/n^+-Si structure are shown in Fig. 3.6 and Fig. 3.7, respectively. As can be seen, there are no resistive switching properties observed in both of the Ag/Alq_3/n^+-Si structure and the

Ag/AlO_x /n^+-Si structure. These results indicate that neither filaments in AlO_x layer nor Alq_3 single layer is the origin of resistive switching. Therefore, we suggest that the resistive switching is attributed to charge trapping and detrapping in the interface defects between the Alq_3 and AlO_x thin films.

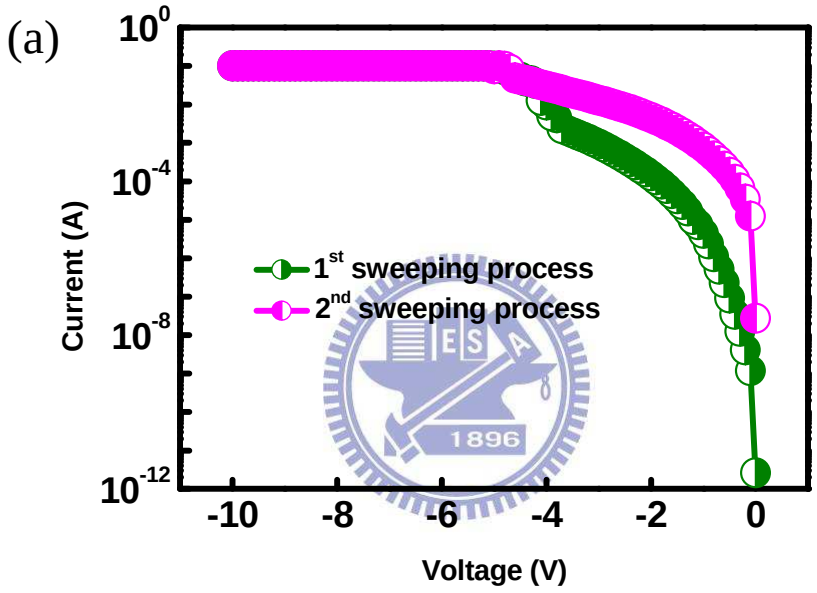


Fig. 3.6: Current-voltage (I-V) curves of the Ag/AlO_x/n^+-Si structure.

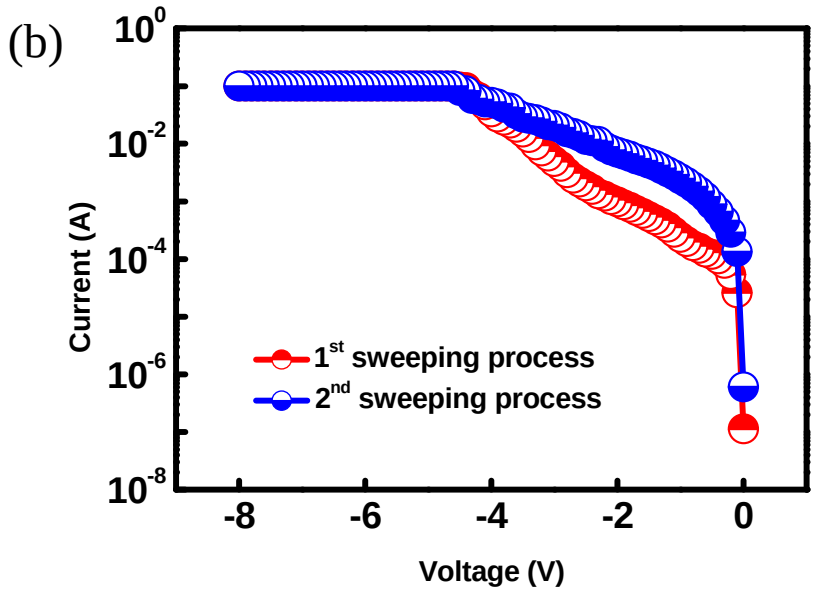


Fig. 3.7: Current-voltage (I-V) curves of the Ag/Alq_3/n^+-Si structure.

Fig. 3.8 depicts the energy band diagram of the Al/AlO_x/Alq_3/n^+-Si structure and the corresponding defect states. Fig. 3.9 shows that how resistive switching happens. As sweeping bias is applied from 0V to -5V, at OFF state, transportation of charge carriers is limited by shallow defect states in AlO_x thin film [4], localized trap states in Alq_3 thin film, and interface defects between Alq_3 and AlO_x. At low voltage bias less than -5V, electrons are injected into AlO_x thin film, and then hopped through shallow defect states in AlO_x thin film (see Fig. 3.9 (a)). Most of them are further trapped by the interface defects between Alq_3 thin film and AlO_x thin film, and the remains hops through localized trap states in Alq_3 thin film. As a result, the device stayed at high resistance. By applying a voltage above -5V, numerous electrons are

injected into the device and the interface defects can be filled (see Fig. 3.9 (b)). Accordingly, electrons can transport easily into Alq_3 thin film by the dipoles induced internal electrical field (see Fig. 3.9 (c)).

However, when a reversed polarity bias is applied, a large amount of carriers can be released from the interface defects (see Fig. 3.9 (d)), and then most of injected electrons from n^+-Si substrate are trapped by the interface defects again, while others hopped through AlO_x thin film. Therefore, the device is at high resistance. As soon as the reversed polarity sweeping voltage is larger than 2.5V, interface defects will be filled with numerous electrons and other electrons can again transport easily through the device without being blocked by the interface defects (see Fig. 3.9 (e) (f)). This means that the Al/AlO_x/Alq_3/n^+-Si structure is a bipolar switching memory device.

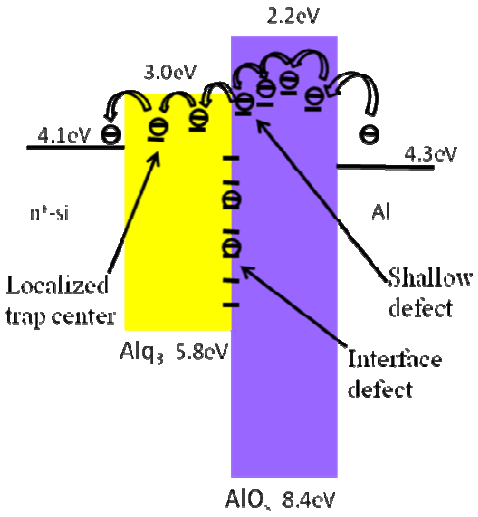


Fig. 3.8: Schematic band diagram of the Al/AlO_x/Alq_3/n^+-Si structure.

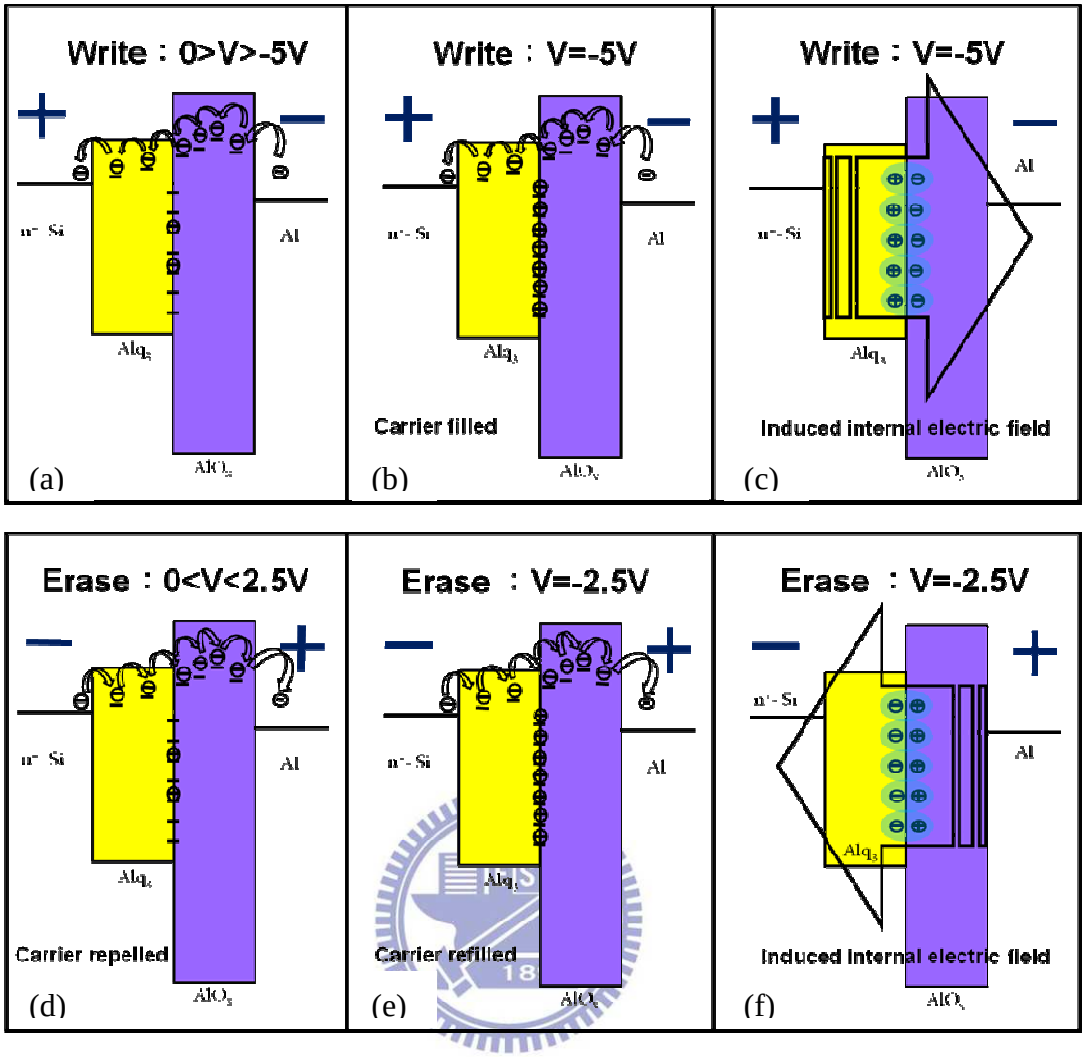


Fig. 3.9: Depictions of proposed mechanisms for the $Al/AlO_x/Alq_3/n^+$-Si structure.

Furthermore, to support the proposed mechanisms, we investigate the transport characteristics by analyzing the I-V relationship. Fig. 3.10 illustrates the I-V relationship in a log (I/V)-$V^{1/2}$ scale for the high conductance state. It can be seen here that the high conductance current follow a linear relationship, meaning that, Poole-Frenkel emission dominates the carrier transport.

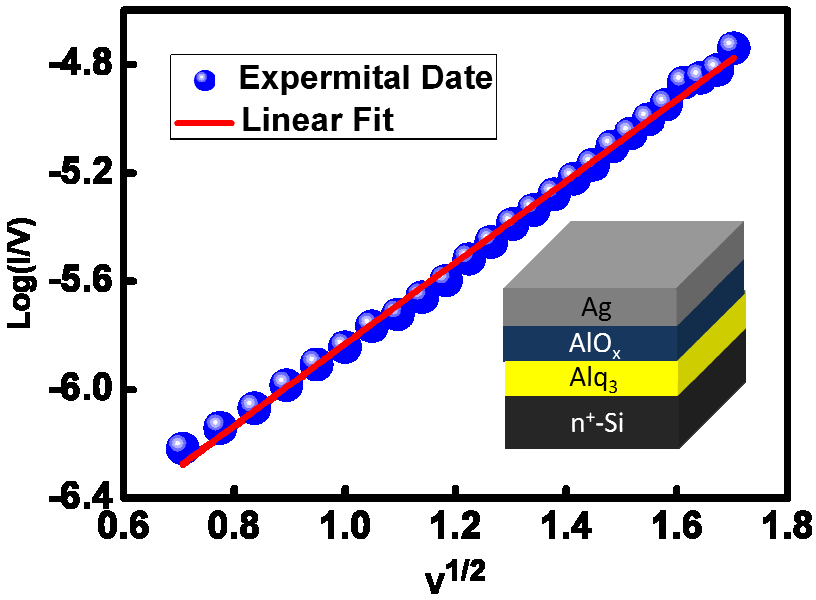


Fig. 3.10: Fitting of the I-V curve of the high conductance state of $Al/AlO_x/Alq_3/n^+$-Si structure in a $log(I/V)-V^{1/2}$ plot.

3.3.4. Summary

In this section, we investigate the I-V characteristics of the $Al/AlO_x/Alq_3/n^+$-Si structure, and propose the possible mechanism of resistive switching. The resistive switching of the $Al/AlO_x/Alq_3/n^+$-Si structure can be attributed to the interface defects between Alq_3 and AlO_x thin films. Bipolar switching behavior is also observed in this structure. Furthermore, the stable high ON/OFF current ratio ~10^6 is obtained.

3.4. Organic RRAM with $Alq_3/MoO_3/Alq_3$ Tri-layer Structure

3.4.1. Introduction

In order to demonstrate a low cost organic RRAM with a low temperature fabrication process, we propose a new structure of $Al/Alq_3/MoO_3/Alq_3/p^+$-Si. In this structure, MoO_3 providing many advantages is utilized as the interposed layer between Alq_3 layers. The advantages of MoO_3 are listed below.

a) High transparency

b) MoO_3 is insensitive to moisture and oxygen.

c) Low melting point of MoO_3

d) Charge trapping property (when MoO_3 is interposed between Alq_3 layers)

e) The nano-structure can be grew by very low evaporation rate

First of all, even though the most Al nanostructure is utilized as the charge trapping center in organic RRAM, Al is sensitive to moisture and oxygen which make device hard to guarantee its performance. MoO_3 do not meet the oxidation problem. Moreover, due to the low melting point of MoO_3, it can be evaporated by heating crucible in thermal coater. Therefore, we don't vent the vacuum necessary for this new structure of $Alq_3/MoO_3/Alq_3/p^+$-Si in our fabrication process. The device yield can improve significantly.

As shown in Fig 3.11, Valance band (E_v) of MoO_3 is about 5.3eV, and the highest occupied molecular orbital (HOMO) level of Alq_3 is about 5.8eV. Hence, there exists an energy difference between E_v of MoO_3 and HOMO of Alq_3, which can capture charge carriers. In addition, it is very important to grow a three-dimension (3-D) structure to provide a better confinement of charge carriers. Fortunately, MoO_3 can form a nano-cluster structure with a low evaporation rate during thin film deposition.

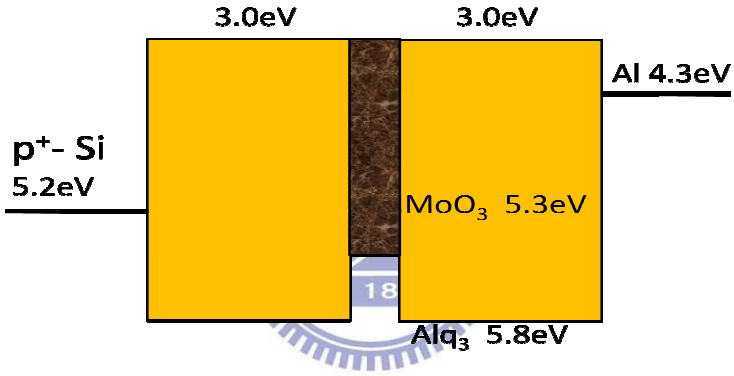


Fig. 3.11: Schematic band diagram of the $Al/Alq_3/MoO_3/Alq_3/p^+$-Si structure.

3.4.2. Electrical Characteristics

Different to the electron-only device of $Al/AlO_x/Alq_3/n^+$-Si structure, the $Al/Alq_3/MoO_3/Alq_3/p^+$-Si structure is a bipolar device, which means that holes and electrons can inject into the device from different electrodes at the same time. Therefore, we can expect that the electrical characteristics of $Al/Alq_3/MoO_3/Alq_3/p^+$-Si structure are dissimilar to $Al/AlO_x/Alq_3/n^+$-Si structure.

The aluminum electrode is grounded, and all bias conditions are applied on the p^+-silicon substrate. Fig. 3.12 shows the electrical characteristics of Al/Alq_3/MoO_3 (5nm)/Alq_3/p^+-Si. The 5nm-thick thin film of MoO_3 layer is the optimized thickness. At first sweeping process, the sweeping voltage from 0V to 10V is applied. Initially, this device is kept at low conductance state with low current level. However, when sweeping voltage exceeds to threshold voltage, a remarkably increase of current is observed. Then, this device is kept at high conductance state with high current level. This sweeping process switched the device form low conductance state (OFF state) to high conductance state (ON state), which called writing process (red circles line). When the sweeping voltage from 0V to 10V is applied again, this device is still hold at high conductance state with high current level, which called reading process (blue triangles line). At third sweeping process, the reverse voltage from 10V to -10V is applied. A noticeably drop of current from high conductance state to low conductance state at -5V is observed. After the decreasing of current, this device is turn back and kept at low conductance state with low current level, which called erasing process.

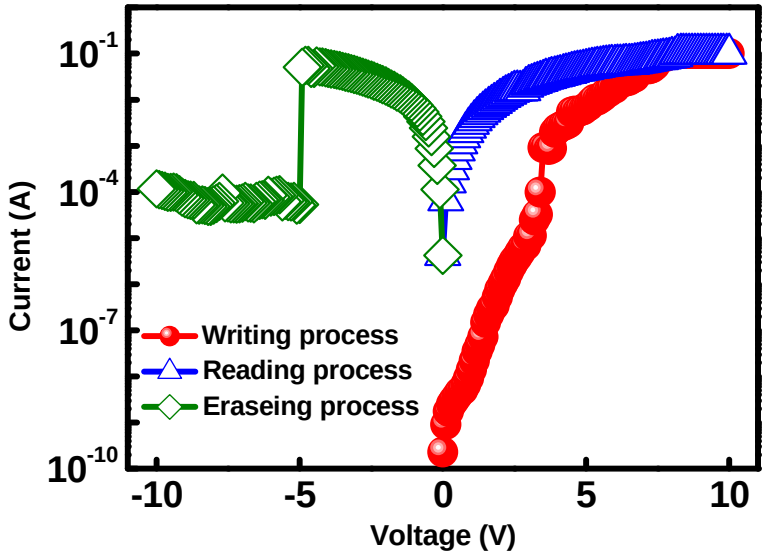


Fig. 3.12: I-V characteristics of an organic RRAM with an Al/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure. The red circles, the blue triangles, and the green diamonds represent the writing, reading, and erasing sweeping biases, respectively.

Fig. 3.13 shows the measurement of retention time of the device, and the long retention time is over 4000 seconds. Despite the fluctuation is observed in the initial 2000s at low conductance state, the current of the low conductance state is getting smaller and more stable with time, and the ON/OFF current ratio becomes larger with time. This large ON/OFF current ratio can reduce reading errors and increase the reliability of the device.

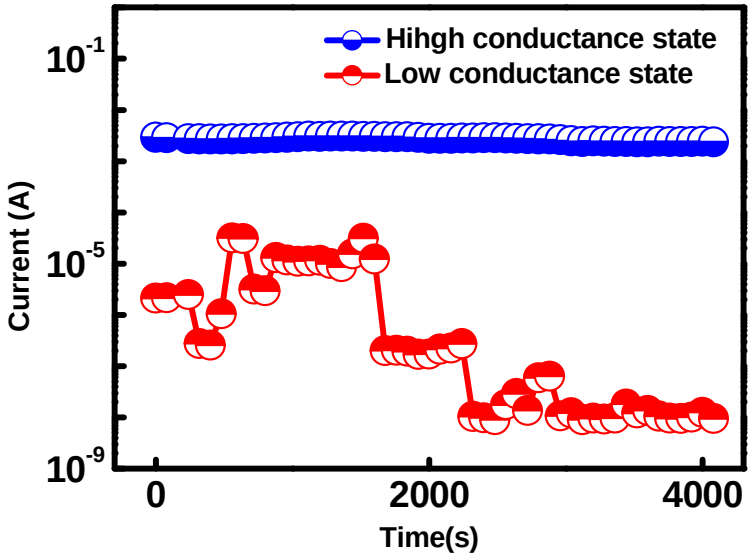


Fig 3.13: Retention time measurement of the organic RRAM. The blue and red circles represent the high and low conductance states, respectively.

To investigate the endurance of the Al/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure, the writing, reading, erasing, and reading processes are executed in sequence. Fig 3.14 shows eight write-read-erase-read cycles. Although the current level of low conductance state varies widely than high conductance state, it still exhibits an interval without overlapping between both states.

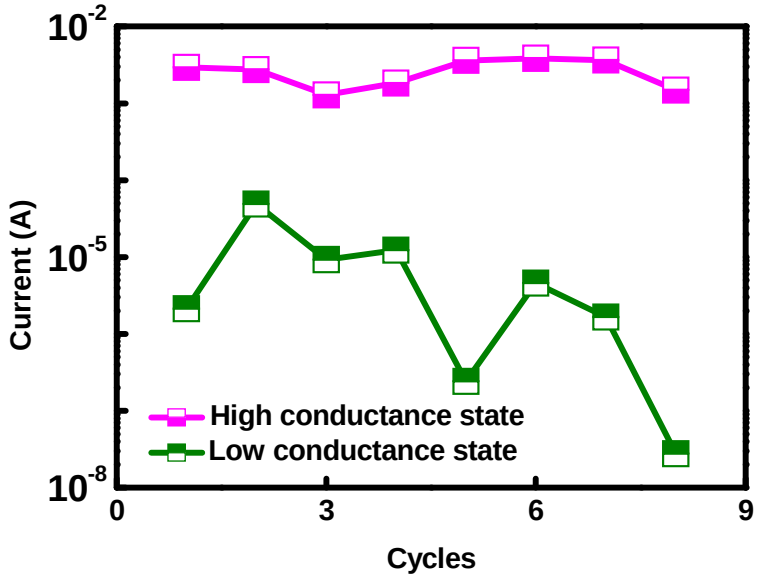


Fig 3.14: Write-read-erase-read cycles measurement for Al/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure.

3.4.3. Mechanism

The mechanism of resistive switching from low conductance state to high conductance state is ascribed to holes trapped in MoO_3 nano-clusters, owing to the confinement of energy level difference between Alq_3 and MoO_3 nano-clusters. As shown in Fig. 3.15 (a), when holes are trapped in the MoO_3 nano-clusters, it acted as space charges and induced an internal electrical filed, which enhanced a large amount of carriers to transport through the device. On the other hand, as a reverse polarity voltage is applied, more electrons inject from p^+-Si than holes inject from Al due to the lower injection barrier of electrons (1.2eV) than holes (1.5eV). In addition, Alq_3 is

well known as electron transporting material with a higher mobility for electrons. Accordingly, the trapped holes will be neutralized by electrons during the erasing process as shown in Fig. 3.15 (b).

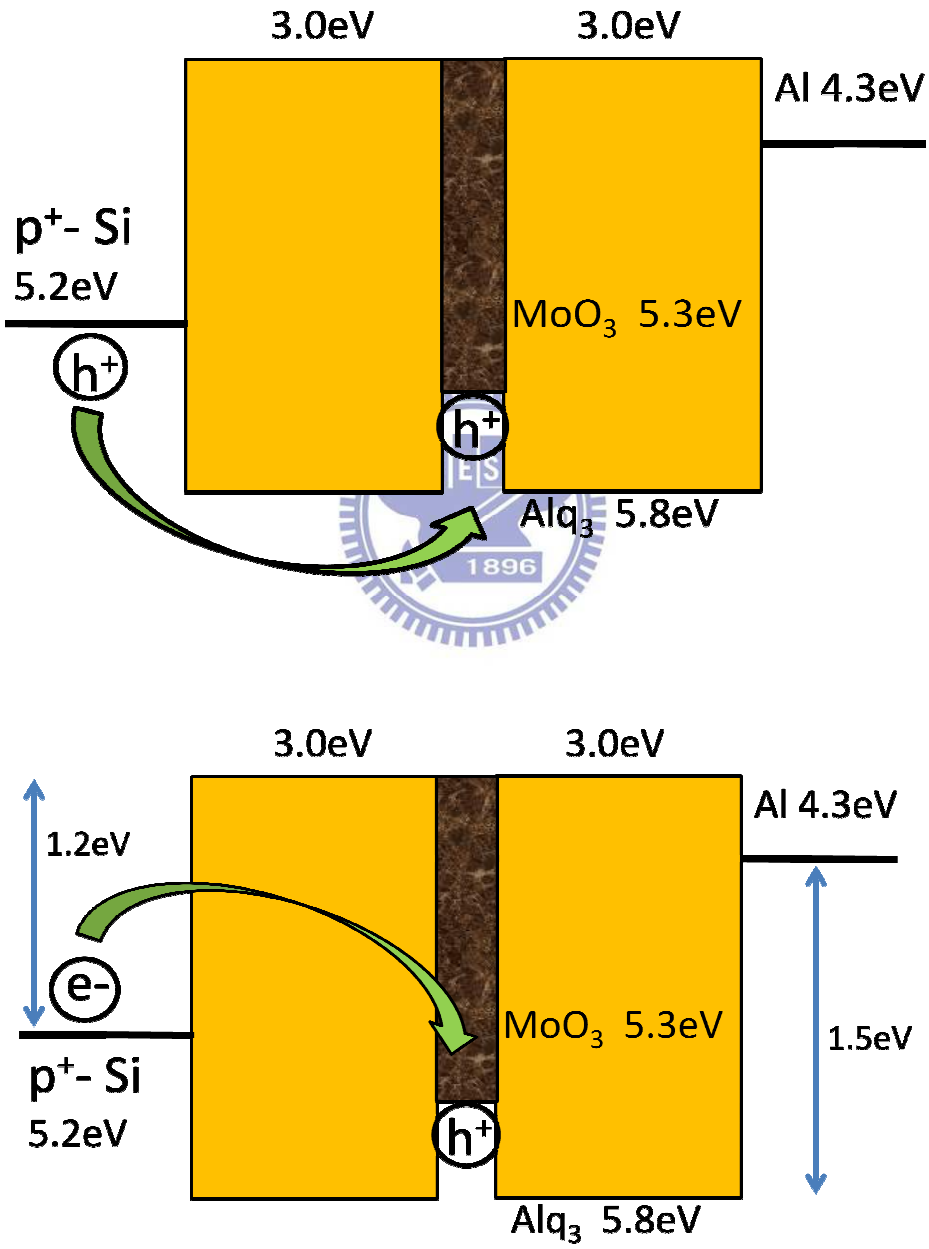


Fig 3.15: (a) The depiction of the writing process for the organic RRAM (b) The depiction of the erasing process for the organic RRAM.

To verify the importance of the nano-clusters MoO_3, standard device without MoO_3 and samples with 3nm, 5nm and 8nm of MoO_3 in Al/Alq_3/MoO_3/Alq_3/p^+-Si structure are fabricated.

As the I-V curves shows in Fig. 3.16, no resistive switching is observed for standard device. The Al/Alq_3/MoO_3/Alq_3/p^+-Si structures with 3nm-thick and 8nm-thick MoO_3 exhibit resistive switching property as shown in Fig. 3.17 and Fig. 3.18, respectively. However, 3nm is too thin to form a continuous film, which caused a large current in low conductance state and an unapparent resistive switching property. On the other hand, 8nm MoO_3 is too thick, hence both the ON state and OFF state currents are suppressed with a low current level. To further investigate the structure of MoO_3, we utilize atomic force microscope (AFM) to measure the morphology of 3nm and 5nm MoO_3 which grown at Alq_3 (50nm)/p^+-Si structure, respectively. As shown in Fig. 3.19 and Fig. 3.20, whatever the MoO_3 is 3nm or 5nm, the nano-clusters MoO_3 are clearly observed in the AFM images. The nano-clusters of MoO_3 can provide a 3-D confinement of charge carriers. Moreover, the most height difference of morphology in 3nm MoO_3 is 1nm and for the 5nm MoO_3 is about 4nm which correspond with the electrical characteristics observed.

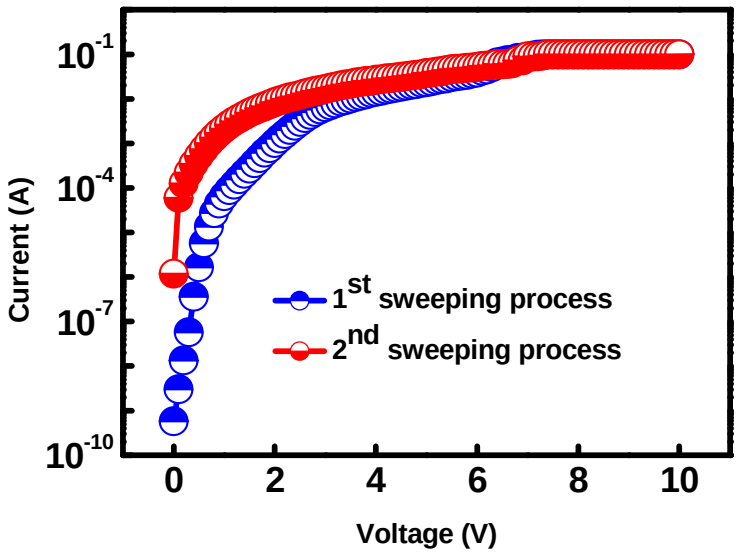


Fig. 3.16: I-V characteristics of the standard device with an Al/Alq_3 (100nm)/p^+-Si structure. The blue circles, and the red circles represent the first and second sweeping processes, respectively.

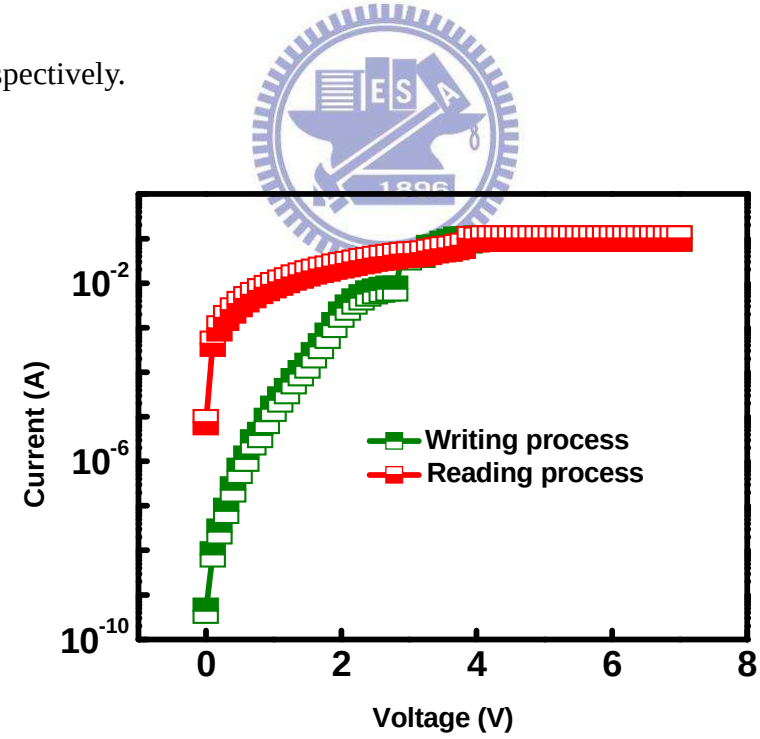


Fig. 3.17: I-V characteristics of the sample with the Al/Alq_3/ MoO_3 nano-clusters (3nm)/Alq_3/p^+-Si structure. The green squares and the red squares represent the writing and reading sweeping processes, respectively.

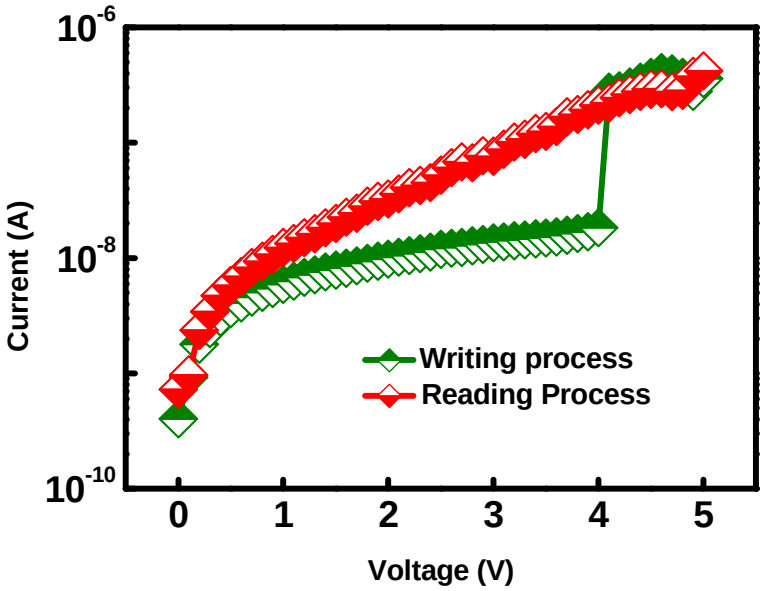


Fig. 3.18: I-V characteristics of the sample with the Al/Alq_3/ MoO_3 nano-clusters (8nm)/Alq_3/p^+-Si structure. The green triangles and the red triangles represent the writing and reading sweeping processes, respectively

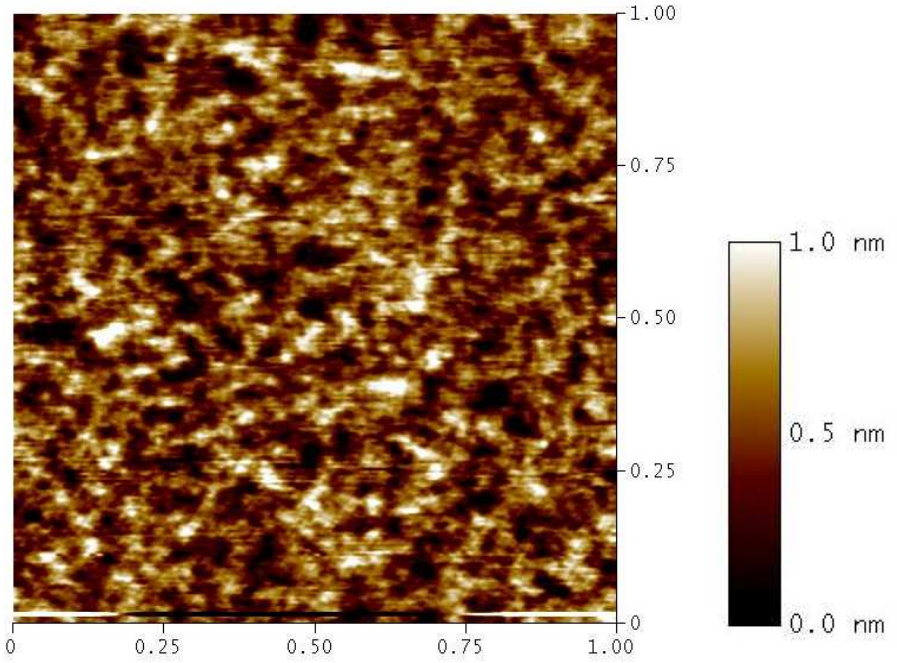


Fig. 3.19: Surface morphology of the 3 nm-thick MoO_3 layer deposited on the Alq_3 /p^+-Si.

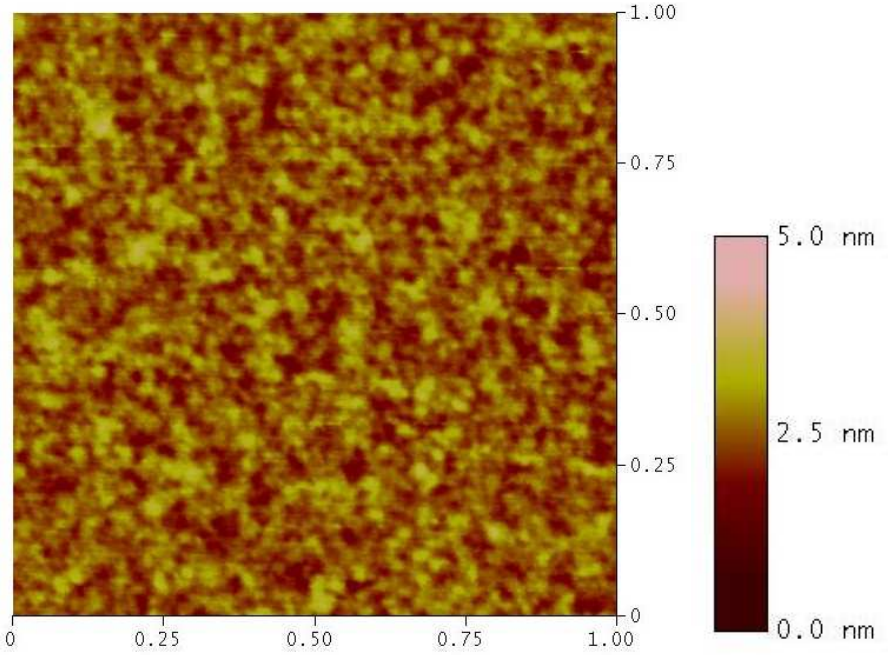


Fig. 3.20: Surface morphology of the 5 nm-thick MoO_3 layer deposited on the Alq_3 /p^+-Si.

3.4.4. Electrode Effect on Re-writing Characteristic

The resistive switching of the Al/Alq_3/MoO_3/Alq_3/p^+-Si structure is ascribed to holes trapped in MoO_3 nano-clusters, due to the confinement of energy level difference between Alq_3 and MoO_3 nano-clusters in this study. However, some studies report that the Al-O compound is probably related to the resistive switching property [30-32]. Unfortunately, the Al-O compound is hard to guarantee reproducibility of device performance. As the XPS results shown in Fig. 3.21, the Al-O compound is generated in the interface between Al and Alq_3 layers.

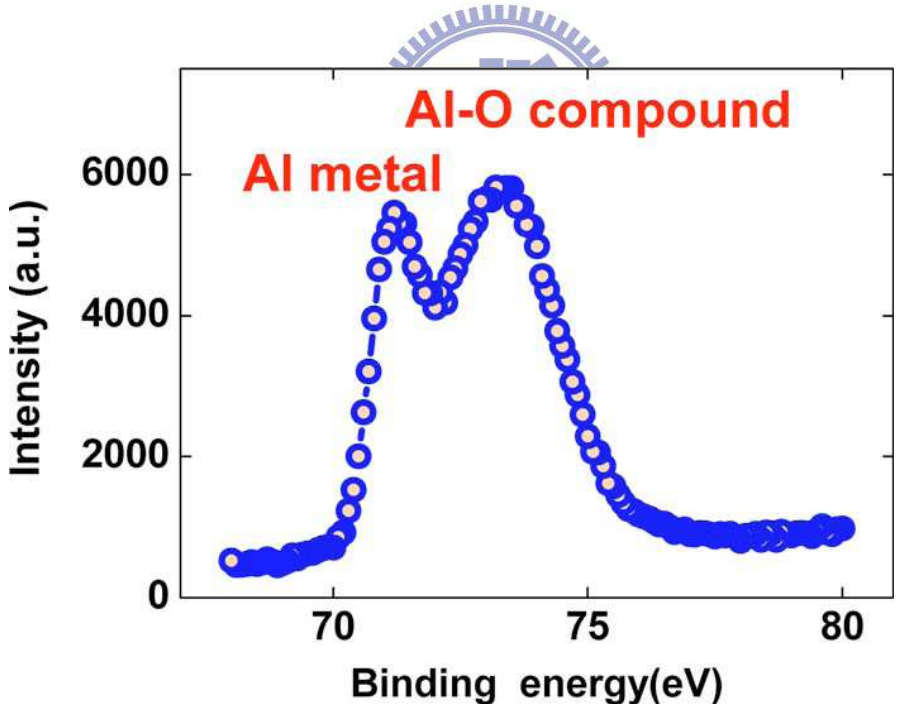


Fig. 3.21: Al (2p) XPS curve of the Al/Alq_3 interface of the Al/Alq_3/MoO_3/Alq_3/p^+-Si structure.

To avoid the extra element, Al-O compound to worsen the performance of the device, the Al electrode is substituted for Ag electrode in $Alq_3/MoO_3/Alq_3/p^+$-Si structure. As shown in Fig. 3.22, the resistive switching is observed in $Ag/Alq_3/MoO_3/Alq_3/p^+$-Si structure. Moreover, the cycling process of this device by pulse is demonstrated. Fig. 3.23 shows the five write-read-erase-read cycles. A 4V pulse is applied to switch the device from OFF to ON state, and 1V pulse is applied to read the ON state current (about 10^{-4}A); a -7V pulse is applied to switch the device from ON to OFF state, and then 1V pulse is applied again to read the OFF state current (about 10^{-10}A). The resistive switching of device can be precisely controlled by applying an appropriate voltage pulse and write-read-erase-read cycles can be repeated more than 35 times as shown in Fig. 3.24.

In conclusion, it is worth to mention again that Al-O compound may relate to the resistive switching property but not definitely. By comparison the electrical characteristics between $Ag/Alq_3/MoO_3/Alq_3/p^+$-Si structure and $Ag/Alq_3/p^+$-Si structure in section 3.4.2, it suggested that the resistive switching is originated from nano-clusters MoO_3. Furthermore, after replacing the Al electrode with Ag electrode in $Alq_3/MoO_3/Alq_3/p^+$-Si structure, the resistive switching behaviors are observed obviously, and the reproducibility of device is improved significantly.

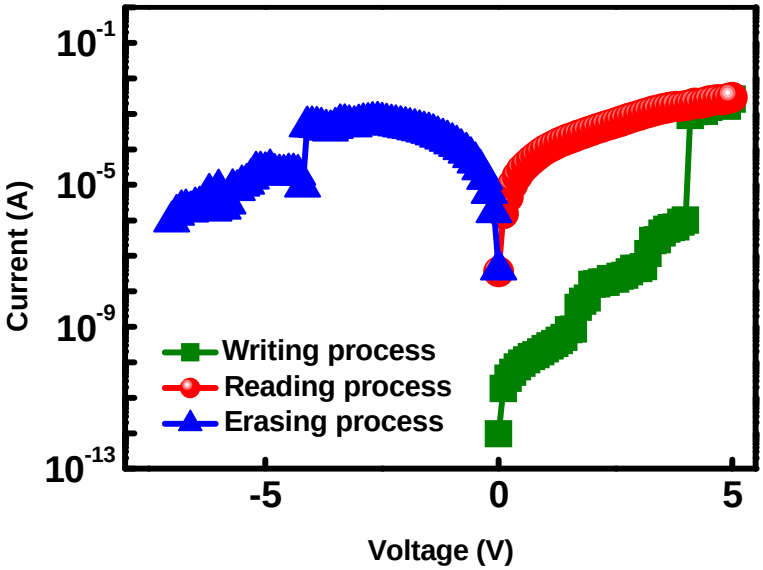


Fig. 3.22: I-V characteristics of an organic RRAM with an Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure.

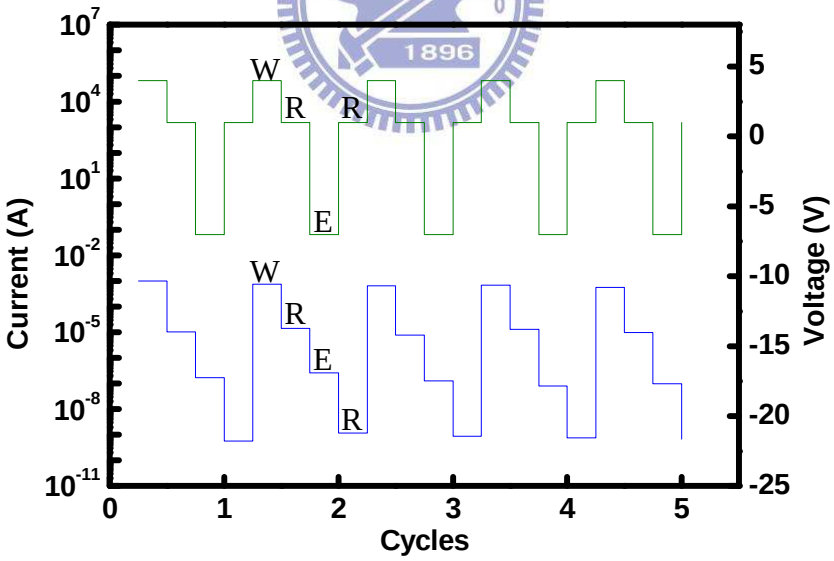


Fig 3.23: Write-read-erase-read cycles measurement for Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure. The 4V, 1V, -7V, and 1V pulses correspond to write, read, erase, and read AC processing voltages.

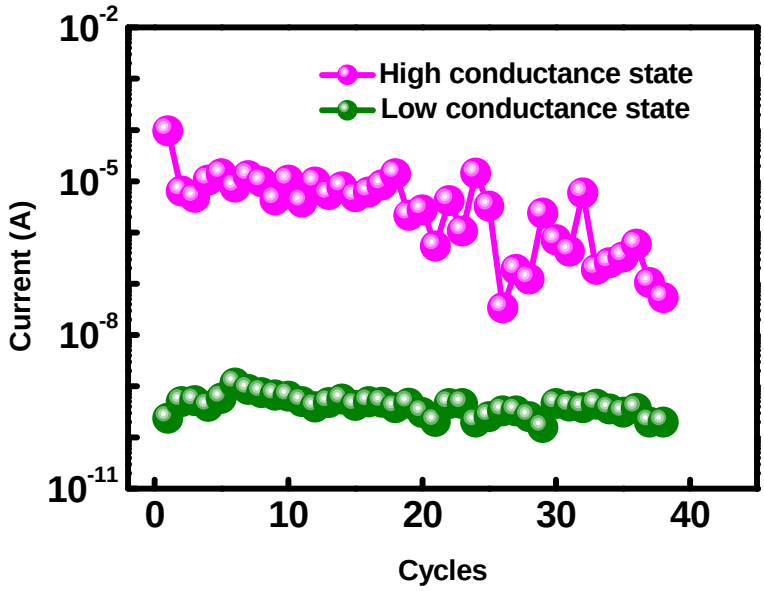


Fig 3.24: More than 35 cycles of write-read-erase-read measurement for Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure.

3.4.5. Summary

The electrical characteristics of an organic RRAM using a MoO_3 nano-clusters layer are reported. The bistability of the Al/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure is a consequence of the charge trapping effect of the MoO_3 nano-clusters layer interposed between Alq_3 thin films. The surface morphology of a nano-structure MoO_3 layer makes a great influence on the electrical characteristics of organic RRAM. Furthermore, the electrode effect on device is also investigated. The Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure exhibits a capability of

re-writing characteristic by programming with pulse. This Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure has great potential for low cost and high-density data storage in the near future.

Chapter 4. Conclusion and Future Work

4.1. Conclusion

We introduce the scaling down problem of the memory currently and the advantages of resistive random access memory (RRAM), which is one of the potential memory devices for next generation. Also, some promising RRAM structure and mechanisms of resistive switching and carrier transport are also mentioned in the first chapter.

In the second chapter, we propose a RRAM with Ag/SiO_2/p^+-Si simple structure, and investigate the electrical characteristics of devices with different post-annealing temperature by RTA. The device with RTA 800^oC treated SiO_2 thin film exhibits the best memory performance. In addition, we discuss and propose the possible mechanisms of the devices with as-deposited, RTA 600^oC treated, and RTA 800^oC treated SiO_2 thin film, respectively. The cost of SiO_2 is more economic compared to metal-oxide. Therefore, this Ag/SiO_2/p^+-Si structure provides a great potential for low cost and mass production.

To reduce the cost, to improve the mass production of memory devices, and even to integrate with organic electronic devices with flexibility, we propose the organic RRAM structure of Al/AlO_x/Alq_3/n^+-Si and Al/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si. The electrical characteristics, mechanisms and role of

nano-structure MoO_3 layer are also discussed. Furthermore, we demonstrate the re-writing characteristic of Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure successfully by substituting the Ag electrode for Al electrode. The more than 35 write-read-erase-read cycles are manifested. From the above results, this Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/p^+-Si structure provides a great potential for low cost and mass production with capability of applying to plastic substrate.

4.2. Future Work

We demonstrate a flexible organic RRAM with Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/Au/PET structure as shown in Fig. 4.1. The electrical characteristics exhibit resistive switching as shown in Fig. 4.2. However, after bending the device for ten times, the V_t and V_{th} decrease, and it is easy to breakdown during the erasing process as shown in Fig. 4.3. We use AFM to investigate the morphology of PET substrate as shown in Fig. 4.4. The surface of the PET substrate is very rough that may degrade the electrical characteristics. It is even worse after bending stress. Therefore, a future work with deposing an additional layer is necessary to reduce surface roughness of PET substrate.

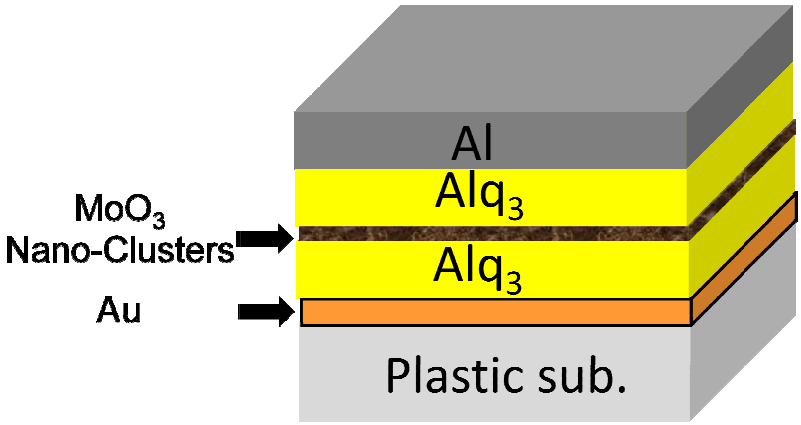


Fig. 4.1: Schematic diagram of Ag/Alq_3/ MoO_3 nano-clusters (5nm) /Alq_3/Au/PET structure.

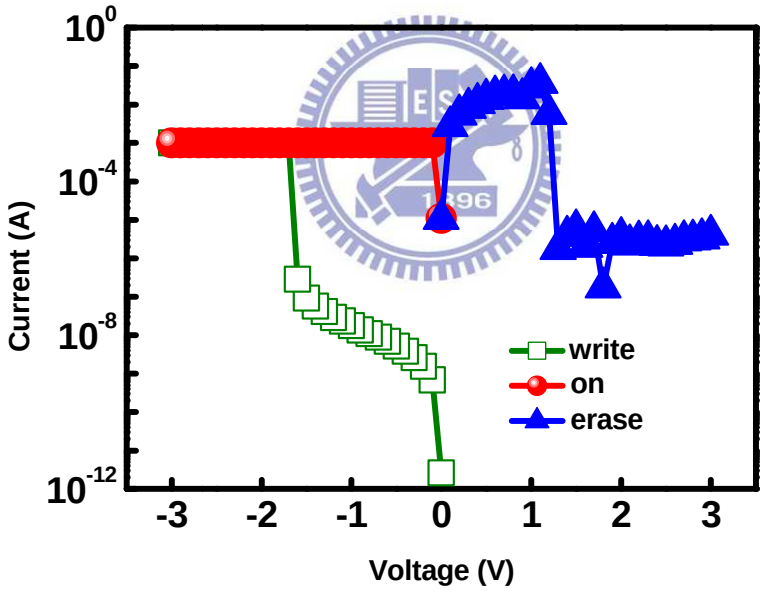


Fig. 4.2: Typical I-V curves of the Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/Au/PET structure before bending.

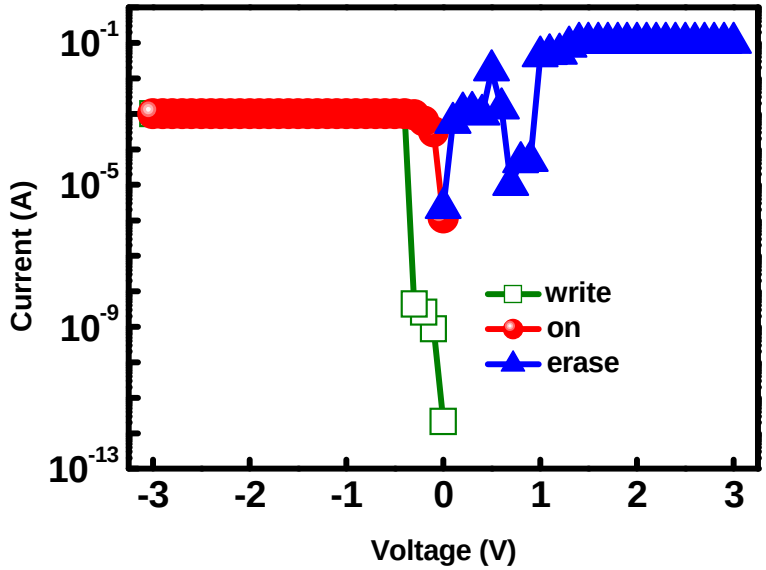


Fig. 4.3: Typical I-V curves of the Ag/Alq_3/ MoO_3 nano-clusters (5nm)/Alq_3/Au/PET structure after bending ten times.

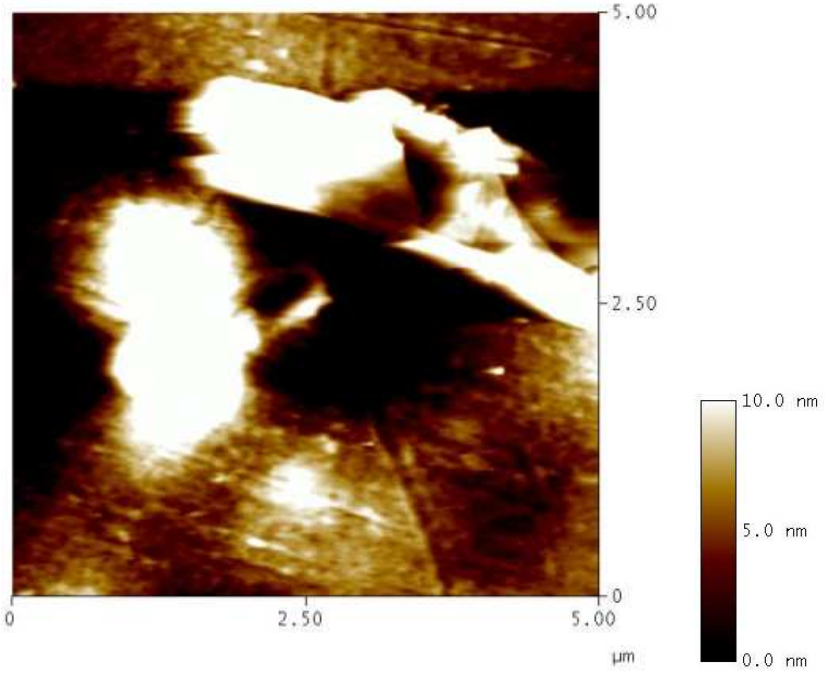


Fig. 4.4: Surface morphology of the PET substrate

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