Chapter 1

Introduction

1.1. General Background

Display technologies have become an important Hi-Tech industry in recent years. Nowadays, the a-Si:H TFTs, which is used widely as drivers of Active Matrix Liquid-Crystal Display (AMLCD), has encroached on the territory of the cathode ray tubes. But the deadly issue to the material based on a-Si:H in channel layer in TFTs is low field effect mobility (~0.5$cm^{2} \cdot V^{-1} \cdot S^{-1}$), photo sensitivity (low band gap about 1.7eV) and rather high deposition temperature (~400℃) [1]. Since the band gap of a-Si is in visible regime, the photo excited carriers (photo current effect) might make the array of AMLCD out of control. For this reason, the opaque metals to keep a-Si based channel blind from visible light are integrated necessarily. This causes lower opening of AMLCD pixels and more complicated device fabrication. In terms of power consumption, a large part of the energy of the display is cost from the backlight instruments, such as Cold Cathode Fluorescent Lamps (CCFL). We need to maximize brightness and efficiency, but the opaque TFTs based on a-Si:H restricts the

amount of light that can be transmitted to the observers. Then, fabricating high-performance devices is challenging of owing to a trade-off between the brightness and power consumption. For the purpose of enhancing power efficiency, display technology based on organic light emitting diodes (OLED), including polymers light emitting diode (PLED) are demonstrated for promising for providing lightweight, power efficient, and high brightness performance at reasonable voltage and current levels. But the challenging facing the OLED and PLED is the need of high driving voltage and high driving current for the controlling circuit [2]. However, the driving circuit seems difficult for us to use the a-Si based material for the low mobility limited.

1.2. Amorphous Oxide Semiconductors

1.2.1. Introduction to Amorphous Oxide Semiconductors

Amorphous oxide semiconductors (AOS) are materials for high performance, low processing temperature electronic devices such as flexible devices due to their high electron mobility >> 10 $cm^2(Vs)^{-1}$ 、high transmission about 75％ in visible light portion of the electromagnetic spectrum and even when their films are deposited at room temperature (RT)

[3][4].

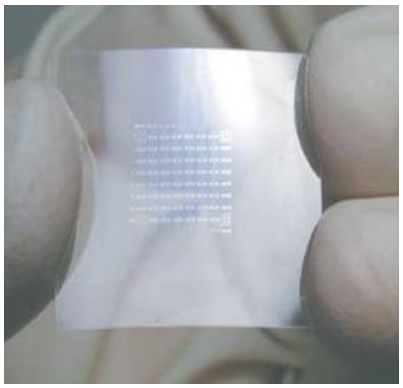

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Fig. 1-1 A photograph of the flexible TIFT sheet. The transparent TFT devices are made visible by adjusting the angle of the illumination.

However, some AOS materials have uncontrollable carriers generated from oxygen vacancy. Therefore, it is important to design and explore a suitable material having both properties of large mobility and stable controllability of carrier concentration for practical applications.

1.2.2. The Carrier Transport Mechanism of AOSs

The mobility of a-Si:H (~1 $cm^2(Vs)^{-1}$) is much smaller than that of single crystalline Si (~200 $cm^2(Vs)^{-1}$) due to the intrinsic chemical bonding nature. The average carrier transportation paths in covalent semiconductors,

such as a-Si:H, consist of strongly directive sp^3 orbitals. The bond angle fluctuation significantly alters the electronic levels, causing high density of deep tail-states, as shown in Fig. 1-3 [5].

In contrast, transparent oxides constituting of heavy post transition metal cations with the $(n-1)d^{10}ns^0$ electron configuration, where $n \geq 5$, are the transparent AOS (TAOS) candidates having large mobilities comparable to those of the corresponding crystals. The electron pathway in oxide semiconductor is primarily composed of spatially spread ns orbitals with an isotropic shape, as shown in Fig. 1-2 [5]. The direct overlap among the neighboring ns orbitals is possible. The degree of overlap of the ns orbitals is insensitive to the distorted metal-oxygen-metal bonding. This feature shows why the Hall mobility of AOSs is similar to the corresponding crystalline phase, even under the room temperature deposition of thin-films.

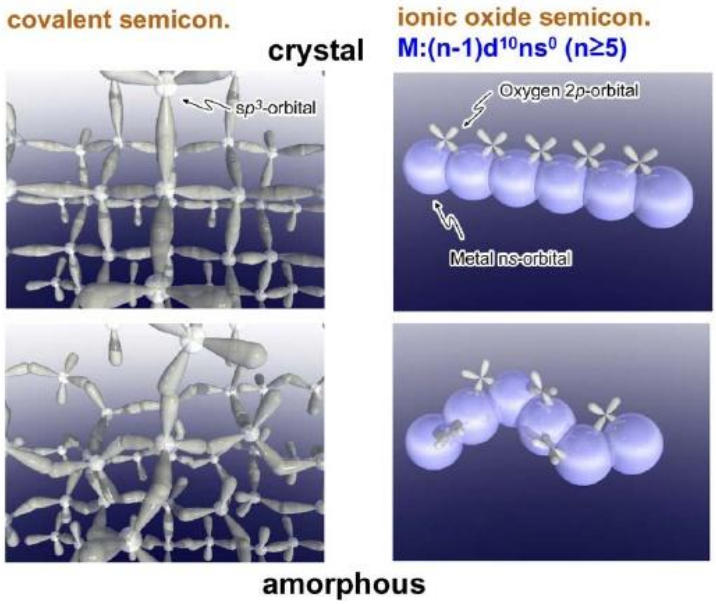

Fig. 1-2 The schematic orbital drawing of electron pathway (conduction band bottom) in conventional silicon-base semiconductor and ionic oxide semiconductor.

1.2.3. amorphous In-Ga-Zn-O

The popular material of TCO was Zinc Oxide (ZnO) which deposited at room temperature reveals polycrystalline with a hexagonal wurtize structure [6]. Because of this characteristic it has many issues in fabrication of TFTs such as uniformity、leakage current and the it's sensitive to the quantity of defects in itself. To solve the above issues, the new material amorphous $InGaZnO_4$ have been developed today.

Transparent AOSs have attracted keen attention since the high performance thin-film transistors can by obtained by using the amorphous In-Ga-Zn-O (a-IGZO) thin films for the semiconductor layers deposited by pulse-laser deposition (PLD) at room temperature []. The TFT performance is also confirmed by using the sputter deposition, which demonstrates the possibility of the large-area applications without the issue of uniformity and

the film composition can be controlled easier. Besides, amorphous In-Ga-Zn-O (a-IGZO) is transparent throughout the visible spectrum; the transmittance is greater than 80 percent from 400 nm to 850 nm as shown in Fig. 1-3 [5].

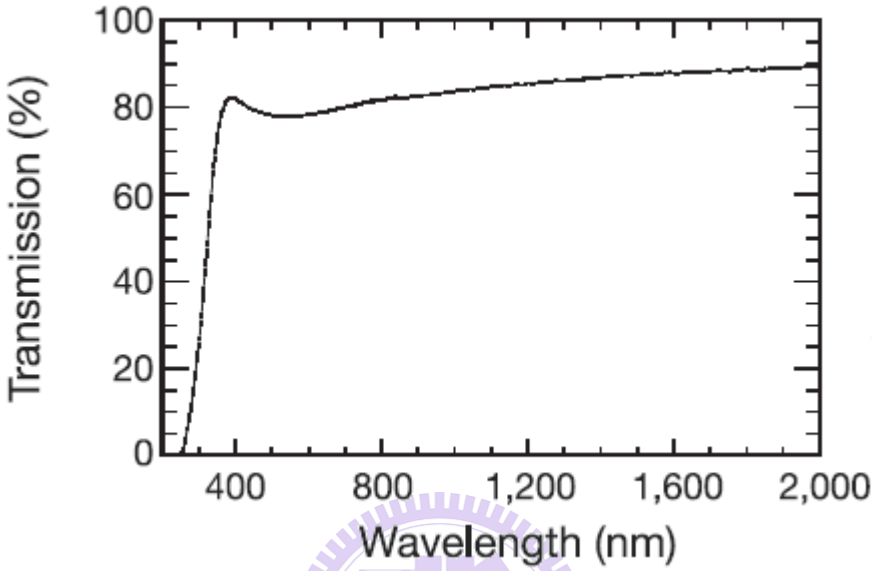

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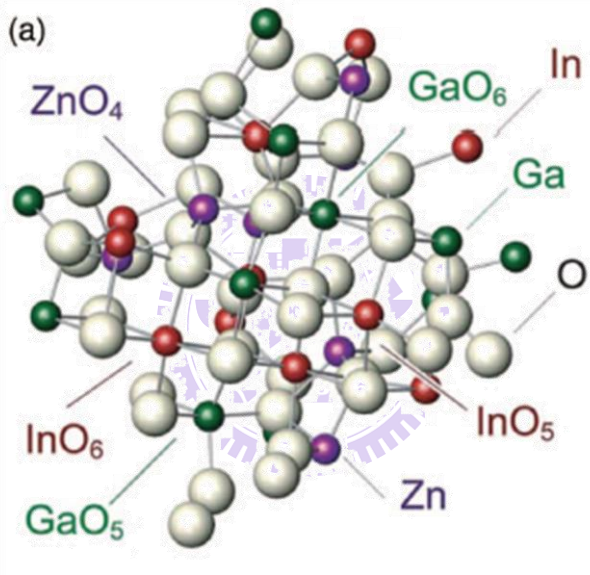
Fig. 1-3. The optical transmission spectrum of the amorphous InGaZnO film.

For the In_2O_3-Ga_2O_3-ZnO ternary system in Fig. 1-4, the incorporation of cations with large ionic valance such as Ga^{3+} and Al^{3+} to high conductive oxides such as In_2O_3 and ZnO is effective to control the carrier concentration due to their strong metal-oxygen bonds [6]. The mobility of $InGaZnO_4$ is primary determined by the In_2O_3 content fraction because only In^{3+} meets the electron configuration criterion $(n-1)d^{10}ns^0$ ($n \geq 5$) of heavy post transition metal cation for ionic AOS (IAOS) among the three cations. The large ionic

valence ions such as Ga^{3+} and Al^{3+} combine with high conductive oxides such as In_2O_3 and ZnO to control the carrier concentration effectively because of the strong metal-oxygen bonds. In other words, Ga^{3+} suppresses carrier generation via oxygen vacancy formation because Ga ion forms stronger bond with oxygen than Zn and In ions. Therefore, the $InGaZnO_4$ composition was chosen as the AOS for channel layer of the transparent TFT.



PHYSICAL REVIEW B 75, 035212 2007

Fig. 1-4. LDA-relaxed a-IGZO structure containing.

1.3. Motivations

The display backplane for large scale and fast switching display is needed. Recently, there are a large number of teams announced the reports on the fabrication method on InGaZnO based TFTs by using RF Magnetron Sputtering

[8], chemical solution deposition [9], pulsed laser deposition (PLD) [7], and Atomic Layer Deposition (ALD) instruments [10]. However the methods above are not suitable for Mass Production. We need a better method and condition to fabricate InGaZnO films to achieve a higher output.

Many papers have claimed that the electrical performance of a-IGZO TFTs is good enough for display application. However, some fundamental transport mechanisms are still unclear which seriously limits its development for realistic application. In addition to that, as the previous studies reported, the annealing process critically dominated the electrical performance of a-IGZO TFTs but each factor during annealing processes still needed to be specified.

In this study, we studied the device properties of TFTs with InGaZnO film as channel layer deposited by using DC plasma of an argon and oxygen mixture atmosphere with a IGZO disc target. And then we annealed our samples in vacuum, pure oxygen, and pure nitrogen environment. Sequentially, an electrical analysis and reliability analysis (gate bias stress measurement) was implemented in ambient air and vacuum environment. Finally we want to establish a transmission model though the results given by above experiments.

1.4. Thesis Organization

This thesis is divided into five chapters. In **Chapter 2**, the operation principle of the TFTs is introduced. The measurement and extraction of electrical parameters are also described. The experiments and equipments for a-IGZO TFTs is described in **Chapter 3**. In **Chapter 4,** the electrical properties of a-IGZO films are presented. First, the effects of inlet gas flow ratio and annealing conditions are discussed. Second, the reliability analysis about a-IGZO TFTs are also presented. Finally, conclusions and future works are summarized in **Chapter 5.**

Chapter 2

Experimental Procedures

2.1 Experimental Procedures

Table. 2-1. is the experimental flow path in my experiment. We did both material and electric analysis to analyze our a-InGaZnO TFT. Fig. 2-1. shows my experimental conception. There were seldom papers about this deposition method for depositing InGaZnO film for TFTs utility. Because of the innovation of DC sputter, we can easily adjust atom ratio especially for oxygen in our InGaZnO film. Besides, we can also control the oxygen content slightly by using different annealing parameter such as temperature and the kind of gas condition. Finally we defined a suitable film for helping us to figure out the transportation model in a-InGaZnO TFT.

Table. 2-1. The experimental flow path

Fig. 2-1. Experimental conception.

2.2. a-InGaZnO TFT Device Fabrication

In our present work, the fabrication both staggered and coplanar thin-film transistors using an n-type InGaZnO film as channel layers will be described. Our InGaZnO-based TFTs, as shown schematically illustrated cross-sectional and planed views in Fig. 2-2.(a) and Fig. 2-2.(b), were fabricated on SiO_2/n-Si substrates. Thermal oxide was chosen as the gate insulator. The channel layer based on InGaZnO was realized by using shadow mask. The width and length range from 200 um to 1000 um, and the width/Length ratio of our TFTs was about 1 to 5.

Prior to the deposition of InGaZnO films, 100-nm-thick SiO_2 layers were thermally grown by 650℃ in Horizontal Furnace on n-type Si (100) substrates. This process was done in Class 10 in National Nano Device Laboratories. The 50-nm-thick InGaZnO films were subsequently deposited by sputtering IGZO target (In:Ga:Zn:O = 1:1:1:4) in a DC power sputtering system at room temperature. The film thickness was measured by AFM. The InGaZnO films were patterned by shadow mask. Then, a shadow mask was subsequently used to pattern ITO source/drain electrode pads deposited upside of the InGaZnO channel by RF sputtering system, and the thickness of the electrons were about

50 nm.

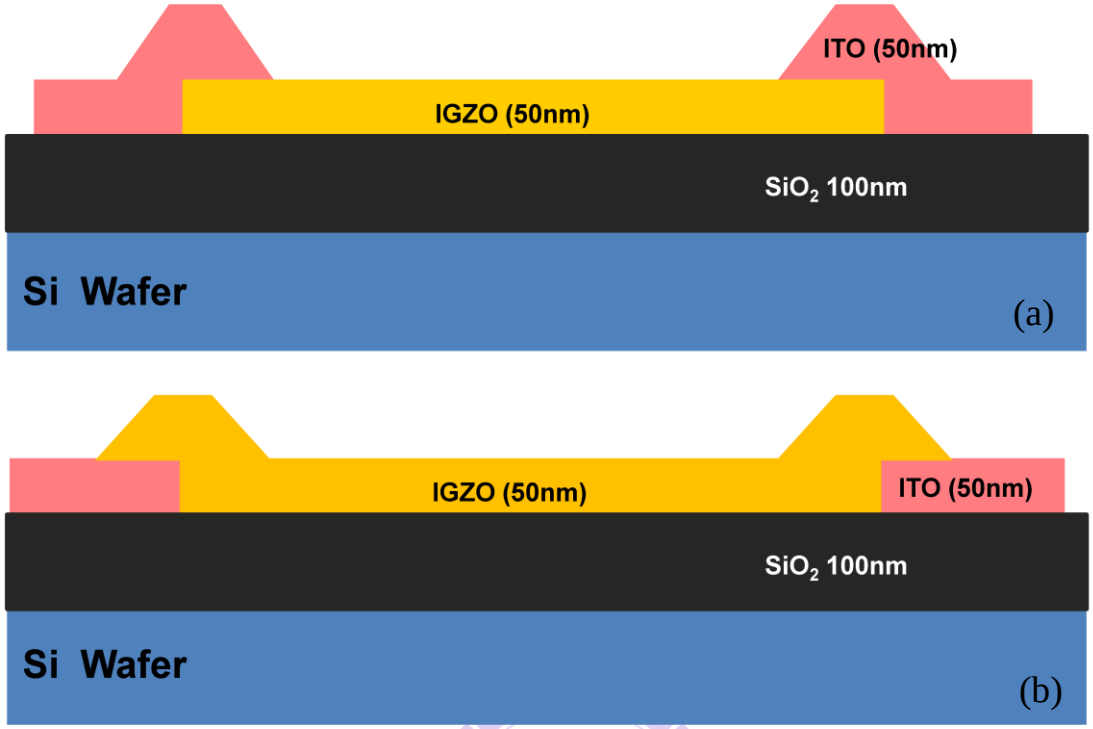


Fig. 2-2.(a)The staggered structure of a-InGaZnO TFT (b)The coplanar structure of a-InGaZnO TFT

2.3. Sputtering Systems

The experimental methods of the fabrication of the a-IGZO TFT are described. Besides, the principle of sputtering system including the RF sputtering and the DC sputtering is described. Fig. 2-3. shows a sputtering system.

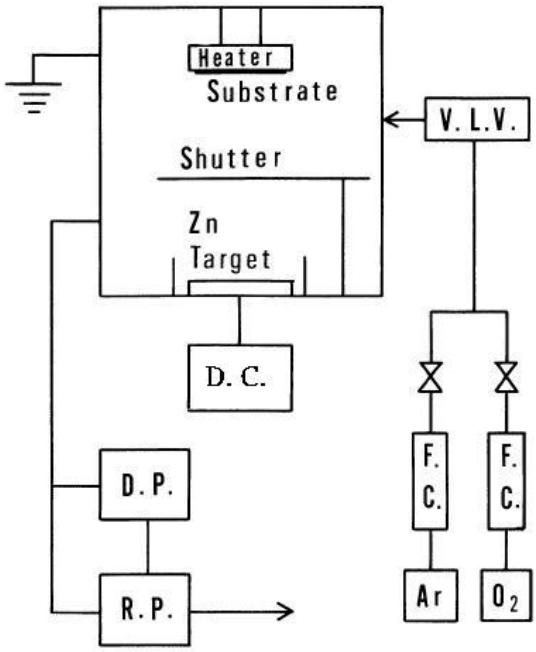


Fig. 2-3. Schematic sputtering system.

2.3.1. RF Sputtering

RF sputtering can be applied to the deposition of both insulating and conducting materials. Fig. 2-4. shows a RF sputtering system, the substrate is located above the target so that the sputtered atoms can be deposited on to the substrate. A RF power supply generates plasma at the frequency of 13.56 MHz. The plasma creates ions which are accelerated towards the target by a negative DC bias on the target. The ions bombard the target surface and dislodge the target atoms, which then deposit onto the substrate. The sputtering is performed in vacuum, typically between 1 mTorr and 50 mTorr. A lower chamber pressure

increases the mean free path, which is the distance between collisions, so that the sputtered target atoms can reach the substrate without scattering away.

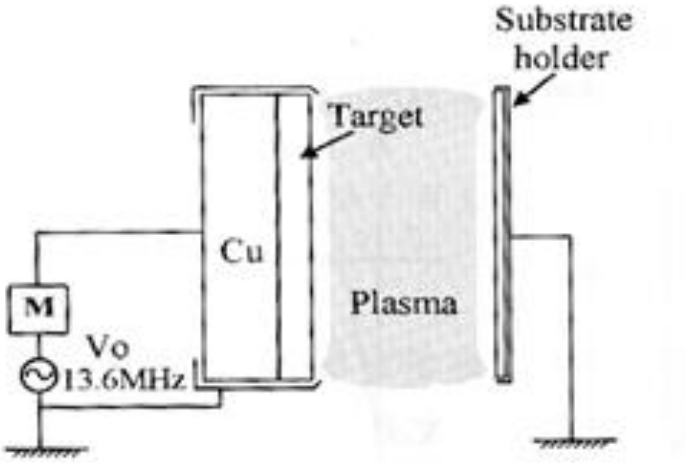


Fig. 2-4 Schematic RF sputtering system.

2.3.2. DC Sputtering

DC sputtering has the advantage of higher deposition rate and is less expensive than RF sputtering. A DC sputtering system is shown in Fig. 2-5., the substrate is located above the target and acts as the anode. DC sputtering is commonly applied to deposit conductive materials.

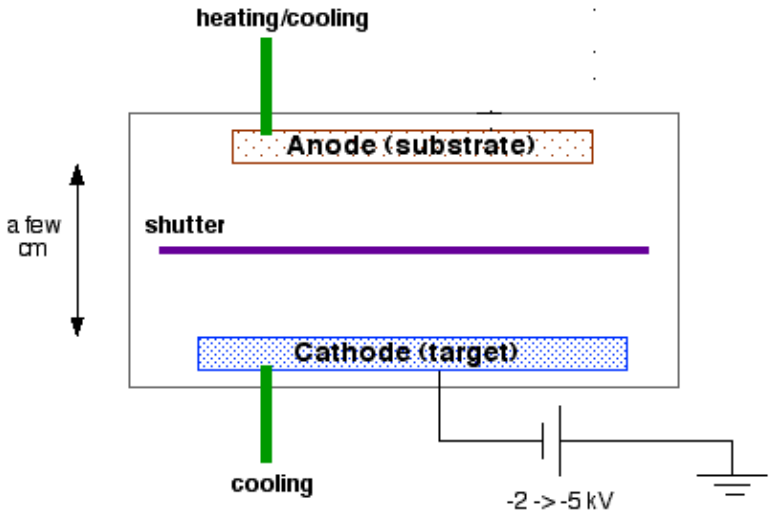


Fig. 2-5 Schematic DC sputtering system.

2.4. Electrical Measurement

The device electrical properties were measured by a Keithley 4200 IV analyzer in a light-isolated probe station at room temperature. In I_{DS}-V_{GS} measurement, the typical drain-to-source bias was swept from V_{GS} = -10 V to V_{GS} = 20 V. In I_{DS}-V_{DS} measurement, the typical drain-to-source bias was swept from VD_S = 0 V to V_{DS} = 30 V.

2.5. Parameter Extraction Method

In this session, we describe the methods of typical parameters extraction such as threshold voltage (V_{th}), subthreshold swing (SS), On/Off current ratio

(I_{on}/I_{off}) and field effect mobility (μ_{FE}) from device characteristics.

2.5.1. Determination of the V_{th}

Threshold voltage (V_{th}) was defined from the gate to source voltage at which carrier conduction happens in TFT channel. V_{th} is related to the gate insulator thickness and the flat band voltage.

Plenty of methods are available to determine V_{th} which is one of the most important parameters of semiconductor devices. This thesis adopts the constant drain current method, which is, the voltage at a specific drain current NI_D is taken as V_{th}, that is, $V_{th} = V_G (NI_D)$ where V_{th} is threshold voltage and NI_D stands for normalized drain current. Constant current method is adopted in most studies of TFTs. It provides a V_{th} close to that obtained by the complex linear extrapolation method. Generally, the threshold current $NI_D = I_D/(W/L)$ is specified at 1 nA in linear region and at 10 nA in saturation region; W and L represent for TFT channel length and width, respectively.

2.5.2. Determination of the Subthreshold Swing

Subthreshold swing (SS, V / dec.) is a typical parameter to describe the control ability of gate toward channel which is the speed of turning the device on and off. It is defined as the amount of gate voltage required to increase and decrease drain current by one order of magnitude.

$$SS = \frac{\partial V_g}{\partial(\log I_d)} \qquad (2\text{-}1)$$

SS can be lessened by substrate bias since it is affected by the total trap density including interfacial trap density and bulk density. In this study, SS was defined as one-half of the gate voltage required to decrease the threshold current by two orders of magnitude (from 10^{-8} A to 10^{-10} A). The threshold current was specified to be the drain current when the gate voltage is equal to V_{th}.

2.5.3. Determination of the Field-Effect Mobility

Typically, the field-effect mobility (μ_{FE}) is determined from the transconductance (g_m) at low drain bias (V_D = 0.1 V). The TFT transfer I-V characteristics can be expressed as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}[(V_G - V_{th})V_D - \frac{1}{2}V_D{}^2] \qquad (2\text{-}2)$$

Where

C_{OX} is the gate oxide capacitance per unit area,

W is channel width,

L is channel length,

V_{th} is the threshold voltage.

If V_D is much smaller than $V_G - V_{TH}$ (i.e. $V_D << V_G - V_{th}$) and $V_G > V_{th}$, the drain current can be approximated as:

$$I_D = \mu_{FE} C_{ox} \frac{W}{L}(V_G - V_{th})V_D \qquad (2\text{-}3)$$

The transconductance is defined as:

$$g_m = \mu_{FE} C_{ox} \frac{W}{L} V_D \qquad (2\text{-}4)$$

Thus,

$$\mu_{FE} = \frac{L}{C_{OX} W V_D} g_m \qquad (2\text{-}5)$$

Similarly, we get mobility in the saturation region as

$$\mu = \frac{L}{W C_{ox}} \left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2 \qquad (2\text{-}6)$$

2.5.4. Determination of On/Off Current Ratio

Drain on/off current ratio is another important factor of TFTs. High on/off current ratio represents not only the large turn-on current but also the small off current (leakage current). It affects AMLCD gray levels (the bright to dark state number) directly.

There are many methods to specify the on and off current. The easiest one is to define the maximum current as on current and the minimum leakage current as off current while drain voltage equal to 0.1V.

$$\text{on/off ratio} = \left.\frac{I_{DS\,Max\,on}}{I_{DS\,Min\,off}}\right|_{V_{DS}=0.1V} \qquad (2\text{-}7)$$

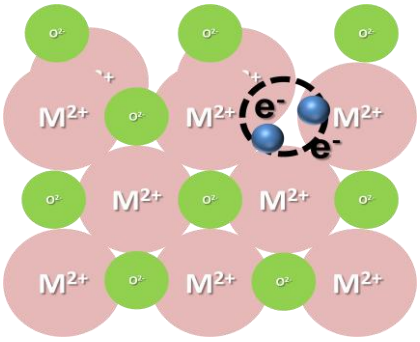
Chapter 3

Experimental Results and Discussion

3.1. The Effects of Oxygen Flow Rate and Post-Annealing on a-IGZO TFTs

3.1.1. Introduction

For metal oxide, the carrier concentration is related to the oxygen vacancy; one oxygen vacancy provides two electrons, as shown in Fig. 3-1 [4].



Appl. Phys. Lett., **89**, 112123 (2006)

Fig. 3-1. The carrier source of Metal oxide.

Hideo Hosono, the most famous researcher in metal oxide semiconductor,

have claimed in APL 2009 that the available condition of oxygen in the film could truly effect the electrical characteristics in IGZO film such as oxygen vacancy(V_o)、interstitial oxygen(O_i). Fig. 3-2.、Fig. 3-3.shows the oxygen vacancy(V_o) 、interstitial oxygen(O_i) in the film [5]. The V_O does not produce mobile electrons, V_O is inactive for electrons and does not affect operation of the *n*-channel TFTs because the V_O level is fully occupied by electrons and cannot trap an electron anymore. Because of the oxygen in the a-IGZO film, a-IGZO TFT characteristics are strongly associated with this channel layer. In addition to that, the electrical characteristics of IGZO film can be controlled by varying the deposition conditions (Ar flow rate and O_2 flow rate) and this can be easily reached by using sputtering system. In this work, several oxygen flow rates (0 sccm, 0.2 sccm, 0.4 sccm, 0.6 sccm, 0.8 sccm, 1 sccm) and annealing condition(temperature、different kinds of gas) were given so as to prepare the a-IGZO TFTs with various electrical characteristics.

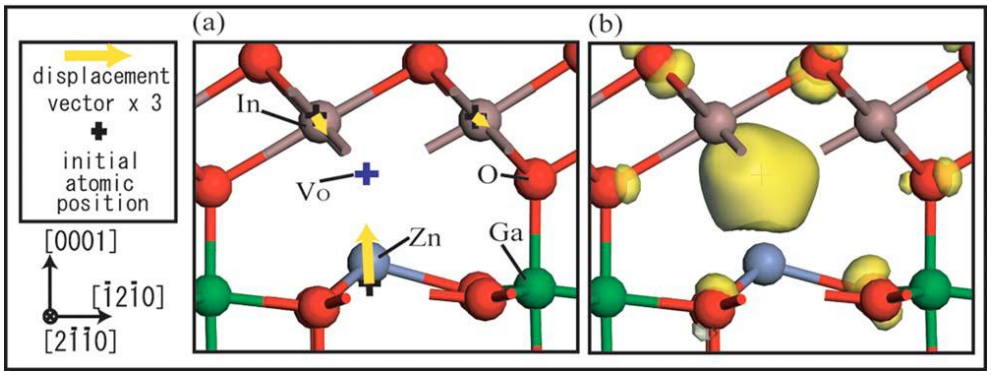


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Fig. 3-2 The oxygen vacancy(V_o) in IGZO film.

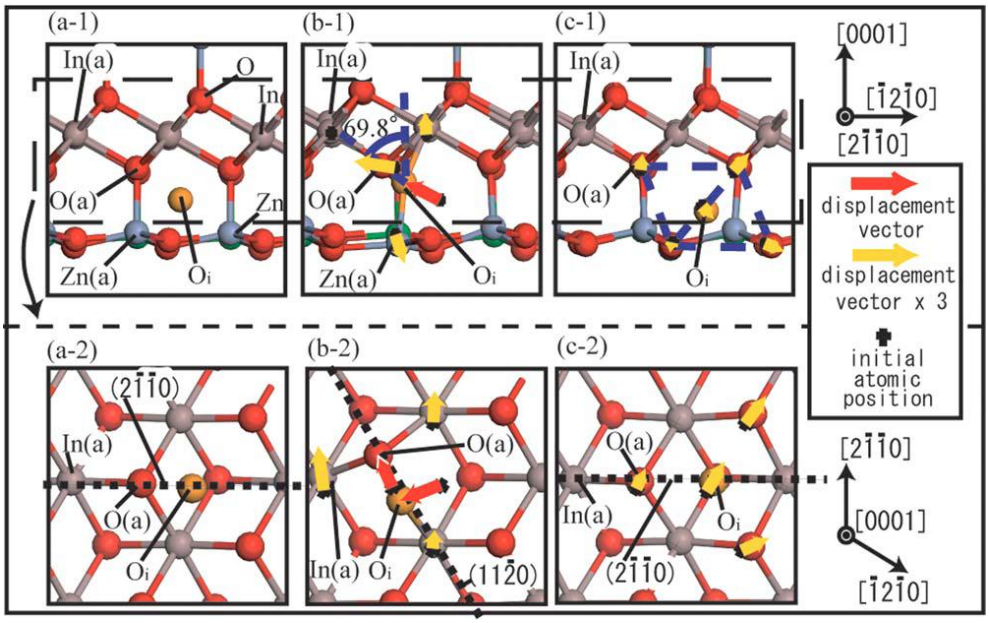

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Fig. 3-3 Different kinds of interstitial oxygen(O_i) in the IGZO film.

As the previous studies reported, the annealing process critically dominated the electrical performance of a-IGZO TFTs but each factor during annealing processes still needed to be specified [5]. In this study, we annealed our samples in vacuum, pure oxygen, and pure nitrogen environment at 450℃. Sequentially, an electrical analysis and gate bias stress measurement was implemented in ambient air and vacuum environment.

3.1.2. Results and Discussion

3.1.2.1. The Effects of Oxygen Flow Rate in a-IGZO TFTs

First, the deposition rate of IGZO was determined by measuring the film

thickness with the AFM. The thickness of a-IGZO film was fixed at 50nm using 100W dc sputtering power and the deposition rate are shown in Table. 3-1. Generally the deposition rate decreased from 2.542 A/sec to 1.969 A/sec when the oxygen increased from 0 to 10% of the Argon flow rate. And the Fig. 3-4 shows a apparent trend of the deposition rate.

DC Power	Ar (sccm)	O_2 (sccm)	Time (h/m/s)	Thickness (nm)	Deposition rate(A/sec)
100W	10	0	00:03:15	49.587	2.542923
100W	10	0.2	00:03:30	51.981	2.475286
100W	10	0.4	00:04:19	53.08	2.049421
100W	10	0.6	00:04:10	49.386	1.97544
100W	10	0.8	00:04:45	50.975	1.788596
100W	10	1	00:04:20	51.199	1.969192

Table. 3-1. The deposition rate with different O_2 flow rate.

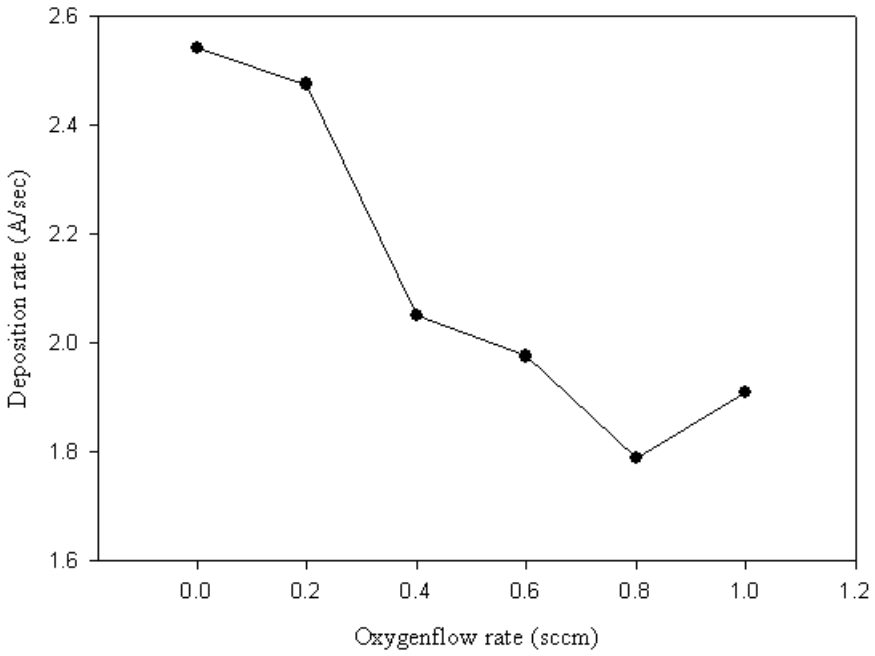


Fig. 3-4. The deposition rate with oxygen flow rate.

Then a-IGZO TFT using coplanar structure was fabricated with different oxygen flow rate and post-annealed 1hour in 250℃、350℃、450℃. Fig. 3-5 shows the a-IGZO TFT I_D-V_G curve with different oxygen flow rates. From the I_D-V_G, the oxygen flow rate indeed affected the electrical characteristics on a-IGZO TFT in different annealing temperature. That's mean the amount of oxygen actually control the film quality. The most obvious one is the sample annealed in 250℃.

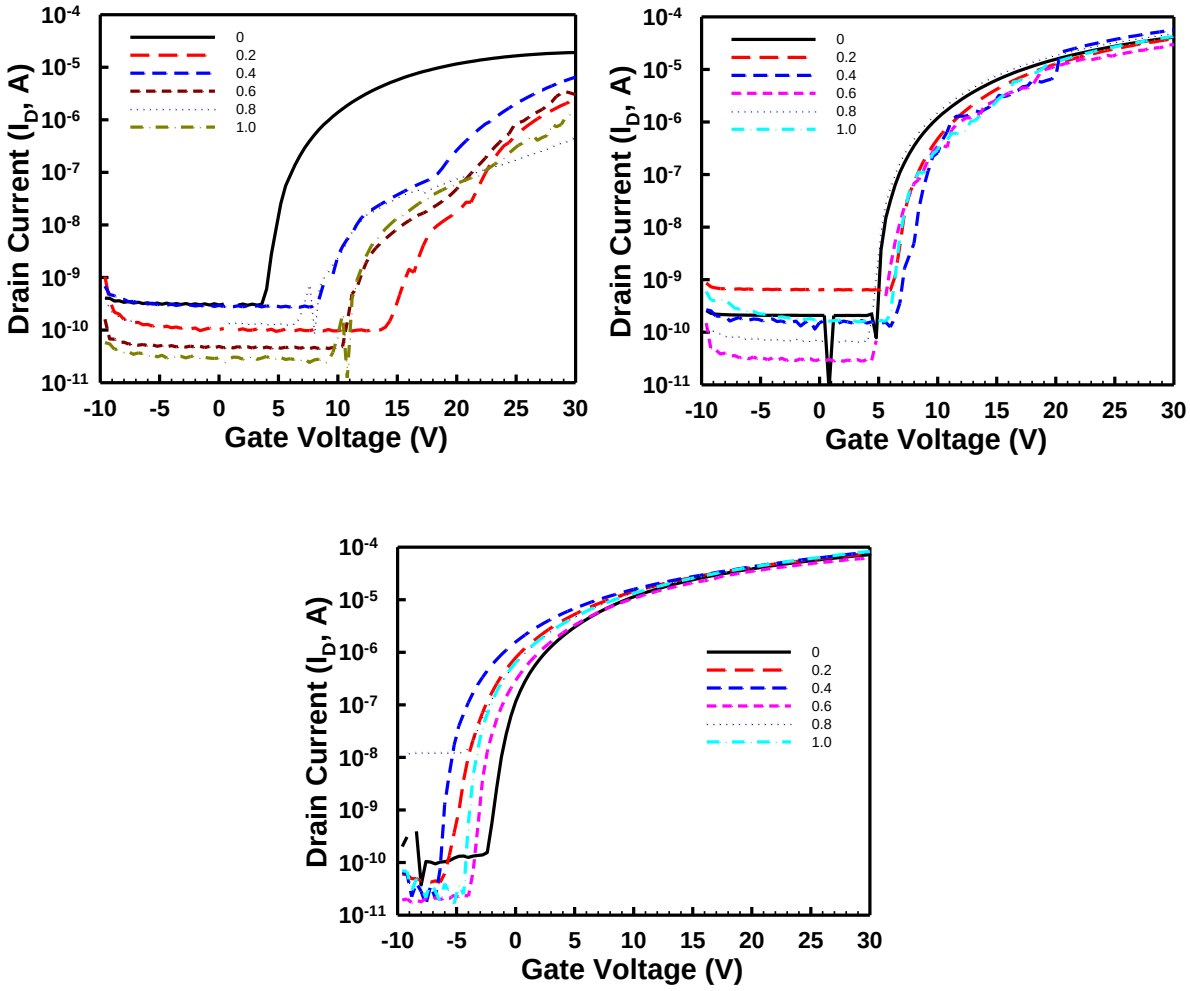
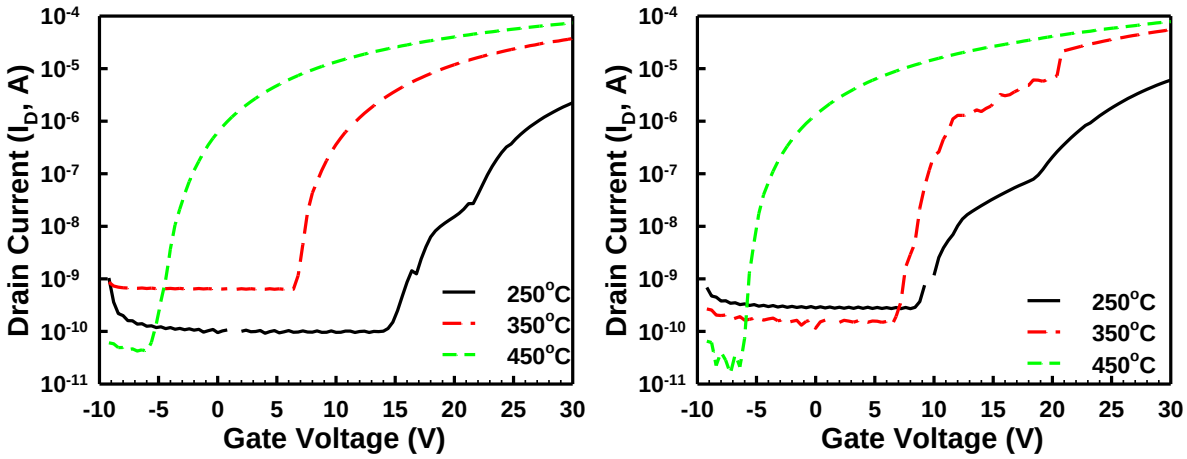


Fig.3-5. The a-IGZO TFT I_D-V_G curve with different oxygen flow rates in (a)

250℃、(b) 350℃、(c) 450℃.

However there didn't have an obvious tendency about the curve shift with oxygen flow rate and we can only find out a little change on the others sample annealed in higher temperature. Because of this, each comparison of oxygen flow at different temperatures are showed in figure. 3-6 and the threshold voltage and subthreshold swing were extracted in fig. 3-7. No matter the oxygen flow was high or low, there had a similar phenomenon that the electrical characteristic improved at higher annealing temperature. The a-IGZO TFT with smallest threshold voltage and subthreshold swing had been found with 0 sccm oxygen flow rate and it was accepted as our standard recipe for the following study.



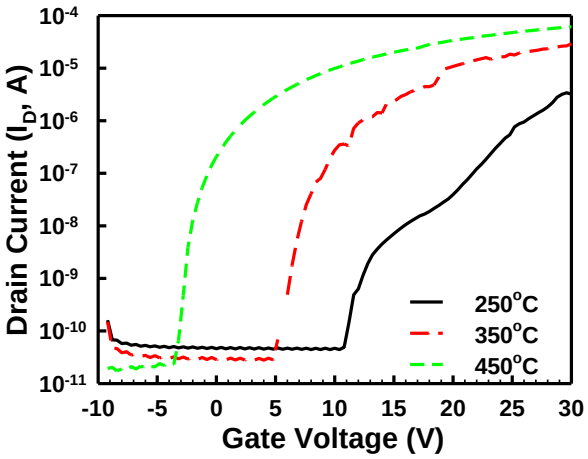


Fig. 3-6. Different oxygen flow rate (a) 0.2 sccm、(b) 0.6sccm、(c) 0.8sccm at different annealing temperature

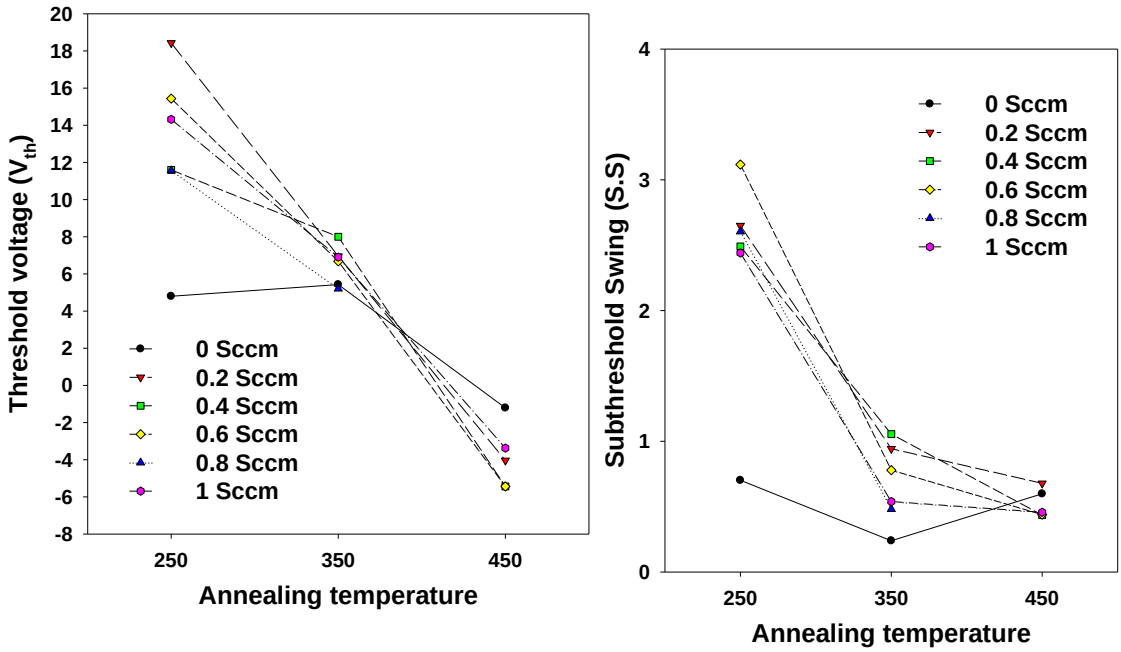


Fig. 3-7. The (a)threshold voltage and (b) subthreshold swing at different annealing temperature.

3.1.2.2. The temperature effects of Post-Annealing on a-IGZO TFTs

The a-IGZO TFT using staggered structure was fabricated with more detail post-annealing temperature at 250℃、300℃、350℃、400℃、450℃. The electrical performance shows in fig.3-8 and fig3-9. The error bar in fig.3-9 present the difference between different device in the same process conditions. Threshold voltage shifts negatively as the annealing temperature increase and the uninformative of devices also improved. Because of the temperature leads to the lattice structure rearrangement, structural relaxation, and the improved a-IGZO bonding. In short, the film quality improved by higher annealing temperature.

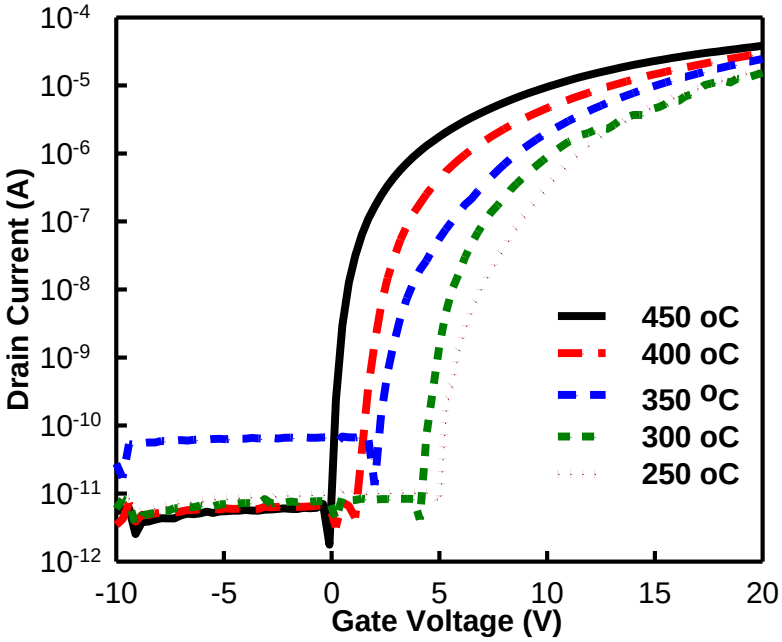


Fig. 3-8. The I_D-V_G curve of a-IGZO TFT with annealing temperature from 250℃to 450℃

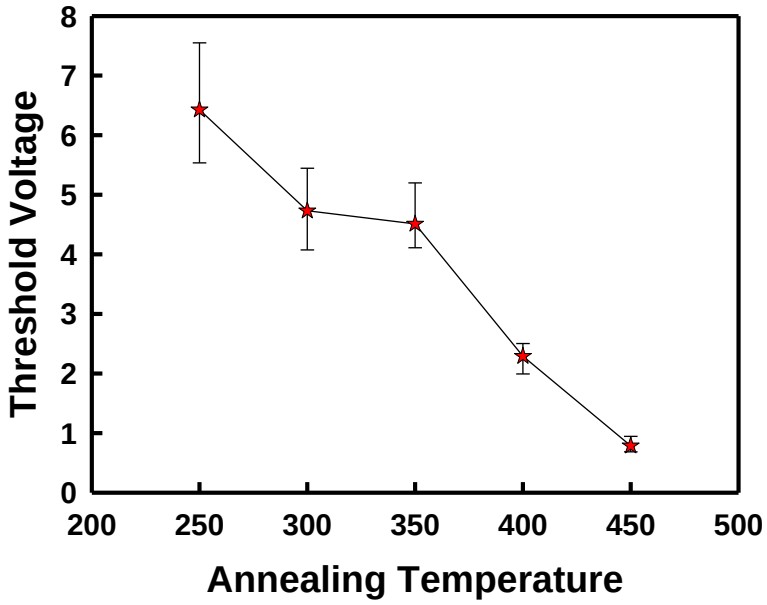


Fig. 3-9. The threshold voltage of a-IGZO TFT with annealing different temperature

Fig.3-10. reveal V_{th} variation of a-IGZO TFTs after being gate bias stressed with a electrical field of 1 MV/cm for 180 min in atmosphere. In fig.3-10(a), V_{th} shifted in the direction of positive voltages under positive gate bias stress (PGBS). The shift values decrease with higher post-annealing temperaure and that mean the improvement of film quality were actually better in 450℃. In fig.3-10(b), V_{th} shifted in the direction of negative voltages under negative gate bias stress (NGBS) but the shift value were almost about -2V no matter the post-annealing temperature increased.

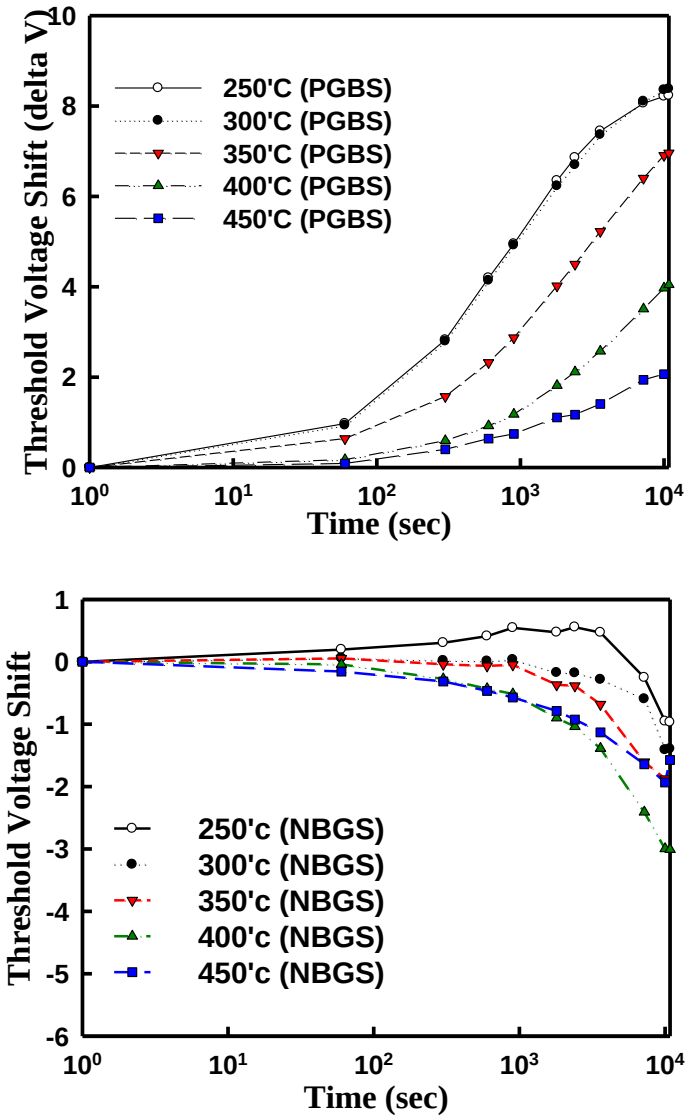


Fig.3-10. The V_{th} variation of a-IGZO TFTs after (a) positive gate bias stress (PGBS) and (b) negative gate bias stress (NGBS) with a electrical field of 1 MV/cm for 180 min.

3.1.2.3. The gas condition of post-annealing on a-IGZO TFTs

Figure.3-11 shows the I_D-V_G curves of the staggered a-IGZO TFT before

and after annealing in nitrogen, oxygen, and vacuum environment in 450℃. It was obviously observed that the I_D-V_G curve left shifted. After annealing, all samples revealed similar on current (I_{on}), while samples annealed in vacuum environment had larger off current (I_{off}) than the other samples. For the seldom I_{on} variation, it can be attributed to the gate-voltage-induced accumulated electrons carriers near the semiconductor and dielectric interface. From the previous studies, the thickness of this region is presumably about 10 nm. That indicated the thermal factor during annealing process can effectively affect the front channel region and result threshold voltage (V_{th}) left shifted. Concerning the I_{off} increased samples annealed in vacuum environment; it surely was related with the increasing of oxygen vacancy at back channel region, leading to a higher leakage current path there. Also, we can expect to have a higher number of free carriers in the back channel region. On the other hand, the desorption of oxygen were inhibited and oxygen or nitrogen in the environment could fill into a-IGZO film again. In addition to that, the a-IGZO TFT could turn off with normal operating.

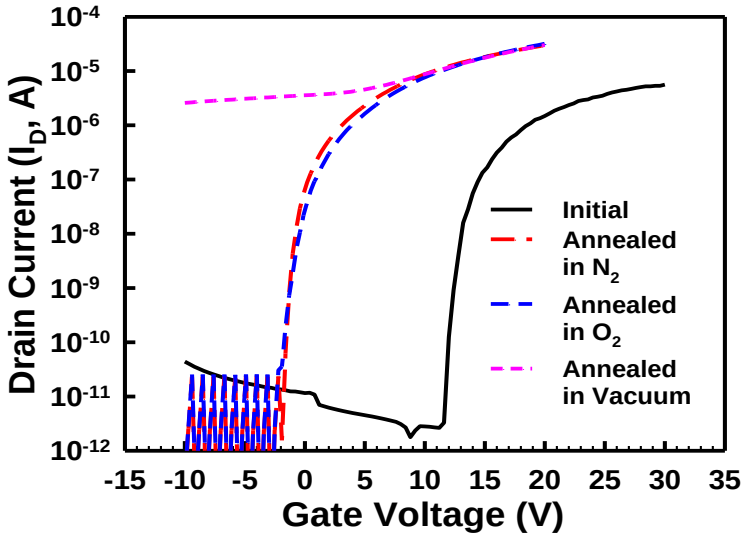


Fig. 3-11. The I_D-V_G of a-IGZO TFT before and after being annealed in vacuum, oxygen and nitrogen environment at 450℃.

3.1.3. Conclusions

The a-IGZO TFT was actually affected by different oxygen flow rate but didn't have an apparent tendency about electrical characteristic change. We fabricated our TFT with oxygen flow rate = 0 sccm to get the best performance of a-IGZO TFT in this thesis.

Post-annealing improved the quality of a-IGZO TFT and the effect were increase with higher temperature 450℃. Because of this, the reliability also improved with lowest threshold voltage shift value 2V after gate bias stress (GBS).

The thermal factor could be specified to improve the front channel characteristics while the annealing environment was specified to affect the amount of oxygen vacancy at back channel. The sample annealed in atmosphere could avoid the oxygen desorption at the back channel and got a great performance a-IGZO TFT.

3.2. The reliability analysis for a-IGZO TFTs and establish the transport model

3.2.1. Introduction

Research for a-IGZO TFT was focused on the electrical performance. However some fundamental transport mechanisms are still unclear which seriously limits its development for realistic application [11][12]. By generalizing the results in last section, the transport model will be derived in this section.

A large V_{th} after stress is still an issue for a-IGZO TFT. It is important to know the mechanism of reliability for applied this material to the display industry. In 2009Applied Physics Letter, the reliability about IZO TFT have claimed that the mechanism of PGBS is affected by oxygen and the mechanism

of NGBS is affected by H_2O in the air [13][14]. Figure.3-12 shows the sketch about mechanism. Under application of +30 V gate bias stress. Oxygen species absorbed from ambient air and a-IZO film can capture electrons in conducting channel, forming the negatively charged species [$O_{2(s)}^-$], positively shifting V_{th}. Schematic reaction of water molecules on a-IZO TFT backchannel under -30 V gate bias stress. Resultant buildup of positive space charges [$H_2O_{(s)}^+$] negatively shifts V_{th}.

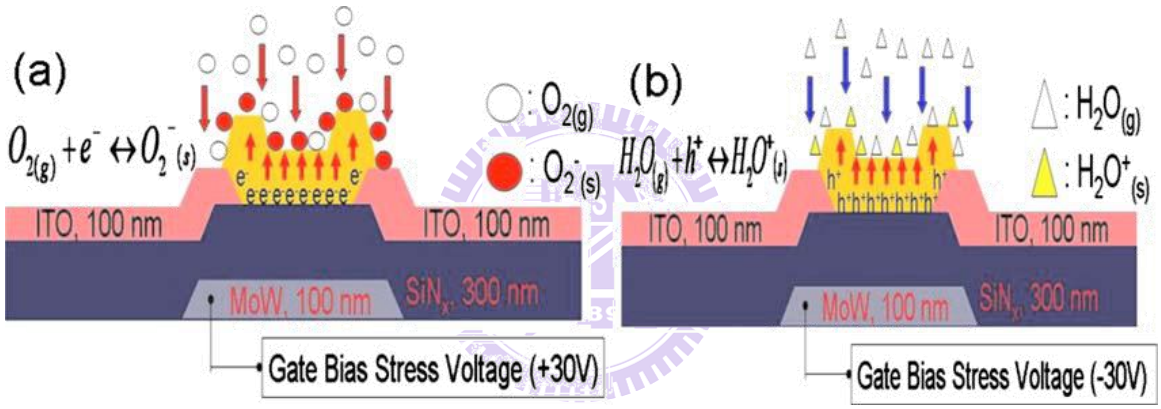


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Fig.3-12.(a) Schematic of adsorption of oxygen molecules on a-IZO TFT backchannel under application of +30 V gate bias stress. (b) Schematic reaction of water molecules on a-IZO TFT backchannel under -30 V gate bias stress.

In this session, the a-IGZO TFT with the staggered structure, as shown in Fig.2-2(b), was implemented in ambient air and vacuum environment given a gate bias stress measurement. We want to figure out the effect about oxygen and

water steam.

3.2.2. Result and Discussion

3.2.2.1. Establish transport model on a-IGZO TFTs

From I_D-V_G curve in figure.3-13, the electrical characteristic can divide into two parts: front channel (turn-on region) and back channel (turn-off region). The I_{on} region can be attributed to the gate-voltage-induced accumulated electrons carriers near the semiconductor and dielectric interface. From the previous studies, the thickness of this region is presumably about 10 nm [11]. That indicated the thermal factor during annealing process can effectively affect the front channel region and result threshold voltage (V_{th}) left shifted. The I_{off} region can be attributed to the oxygen vacancy near the surface of the back channel. The formation of vacancy can attribute to the oxygen desorption when annealing in the vacuum chamber. Although the TFT operate in off region, it still provided a channel for electron transmission. But this phenomenon can be improve by filling oxygen or nitrogen in appropriate annealing environment and the off current could be suppressed to 10^{-11} A from 10^{-6} A.

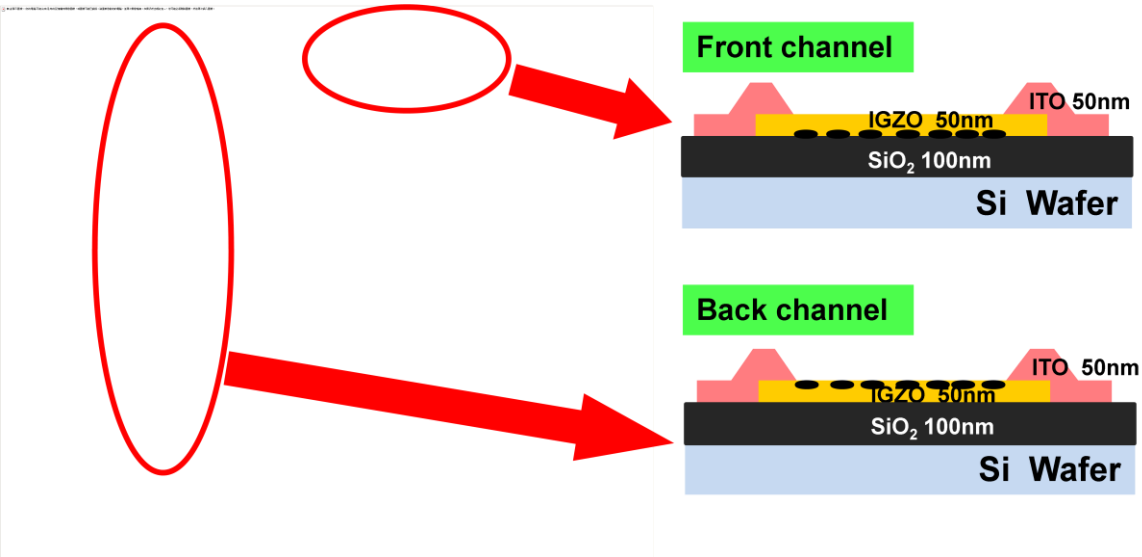


Fig.3-13. The transportation model of a-IGZO TFT.

3.2.2.2. The reliability analysis for a-IGZO TFTs

Figure.3-14 reveal V_{th} variation of a-IGZO TFTs after being gate bias stressed with a electrical field of 1 MV/cm for 180 min in atmosphere and vacuum. For both samples annealed in oxygen and nitrogen environment, V_{th} shifted in the direction of positive voltages under positive gate bias stress (PGBS). The shift values were even the same to samples stressed in atmosphere and vacuum environment. As for the bias-stress-induced instability of TCO-based TFTs, it was reported that the adsorption/desorption reaction of ambient gases, especially for oxygen and moisture, on back-channel can play important role in the device electrical characteristics. These reaction followed the chemical reaction as dercribed below:

$$O_{2(g)} + e^{-} \leftrightarrow O_2^{-}(s) \quad (1)$$

$$H_2O_{(g)} + h^{+} \leftrightarrow H_2O^{+}(s) \quad (2)$$

where e^- and h^+ was referred to electrons and holes. The resultant buildup of negative space charges $O_2^-{}_{(s)}$ easily repelled conduction electrons in the a-IGZO TFT channel, leading to positively V_{th} shifts [13]. With the increase of bias durations, the V_{th} increased progressively due to the continuous accumulation of electron (PGBS) showing up in the conducting channel. The H_2O played the reversed role to oxygen, and formed H_2O^+ to lead V_{th} negatively shifted as Eqn. 2 shown. It also could be progressively increased by the continue accumulation of holes (negative gate bias stress (NGBS)).

However for Eqn. 1, oxygen reaction should occupy the vacancy at back channel of a-IGZO TFT and charges exchanged with a-IGZO, while H_2O would stand on the film surface and charges exchanged with a-IGZO. That explained the similar V_{th} variation after PGBS independent on the ambient $O_{2(g)}$.

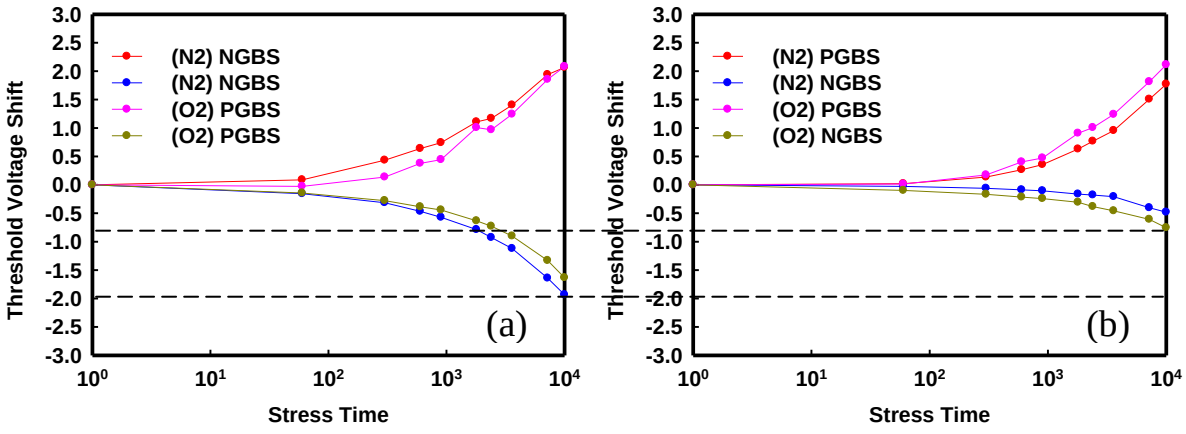


Fig. 3-14. The V_{th} variation of a-IGZO TFTs after positive gate bias stress (PGBS) and negative gate bias stress (NGBS) with a electrical field of 1 MV/cm for 180 min in atmosphere and vacuum.

But as for the Eqn. 2, H_2O could stay on the surface of a-IGZO films, and charge exchanged with it, leading Eqn. 2 keep working even there are seldom vacany existed on the a-IGZO TFTs which were annealed in oxygen and nitrogen at 450℃. That resulted the different V_{th} variation happened in atmosphere and vacuum. The O_2 and H_2O acting behaviors were schematically sketched in Figure.3-15.

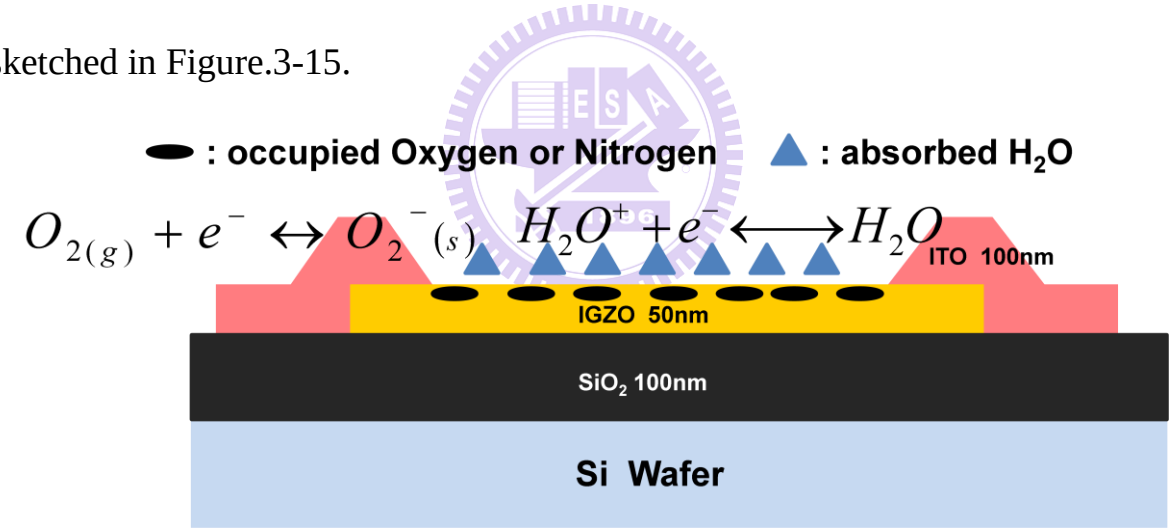


Fig. 3-15. Schematic of adsorption position of O_2 and H_2O molecules on a-IGZO TFT backchannel.

In summary, experimental results indicated annealing environment influence and electrical metastability of the a-IGZO TFT under gate bias stresses of different voltage polarities. Annealing temperature would improved the front

channel characteristics and annealing forming gas would fill up the back channel vacancy. For the PGBS and NGBS experiments, the magnitude of the V_{th} variation was similar after PGBS in atmosphere and vacuum because of the lack of oxygen vacancy in back channel of samples annealed in oxygen and nitrogen environment. However, H_2O would stay on the surface of a-IGZO and resulted the different Vth variation happened under NGBS in atmosphere and vacuum.

3.2.3. Conclusion

The annealing environment influence for a-IGZO TFT has been investigated in this study. The thermal factor could be specified to improve the front channel characteristics while the annealing environment was specified to affect the amount of oxygen vacancy at back channel. By discussing V_{th} variation after PGBS and NGBS in sufficient (atmosphere) and un-sufficient (vacuum) air environment, an annealing influence related electrons transportation model for a-IGZO TFT was obtained. Following this model, as we could well control the annealing condition, high reliability a-IGZO TFT device could be achieved easily.

3.3. The Effects of IGZO film's thickness on a-IGZO TFTs

3.3.1. Introduction

Because of the high interest of application in the future of these 'new' materials, it's more important to research the influence of active layer on electrical properties. In the last chapter, the transport mechanism of a-IGZO TFT can be separated to front channel and back channel. The oxygen、water absorbing at the back channel actually degrade the electrical performance and reliability. In this chapter, three different of IGZO thicknesses were obtained to fabricate the thin film transistors and also given gate bias stress to analyze the reliability.

3.3.2. Result and Discussion

3.3.2.1. The Effects of IGZO film thickness in a-IGZO TFTs

The figure.3-15 shows the I_D-V_G curve of a-IGZO TFT with different thickness 10、20、50、100 nm using staggered structure. The transfer curves are systematically shifted in the negative direction as t_{active} is increase from 10 to

50nm [15][16]. Then the threshold voltage fixed at 0V and didn't shift more negatively with increasing the layer to 100nm. The electrical parameters are shown in figure.3-16. The subthreshold swing is 0.3V/decade and would be not significantly affected by the t_{active}. This is because the threshold swing is dominated by the interface condition between gate insulator and active layer [17]. In my research the same thermal SiO_2 was adopted for gate insulator so the swing seems similar for all different IGZO thickness.

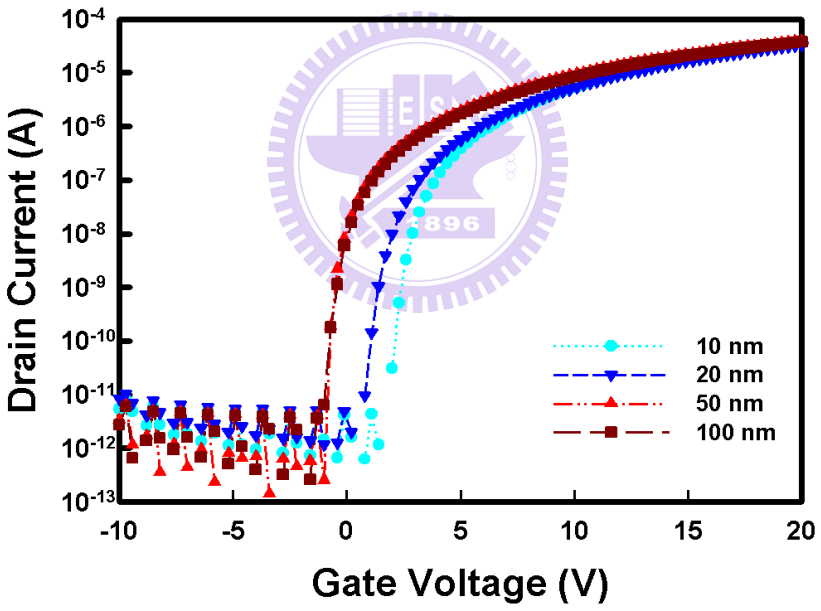


Fig.3-15 The I_D-V_G curve with different IGZO thickness.

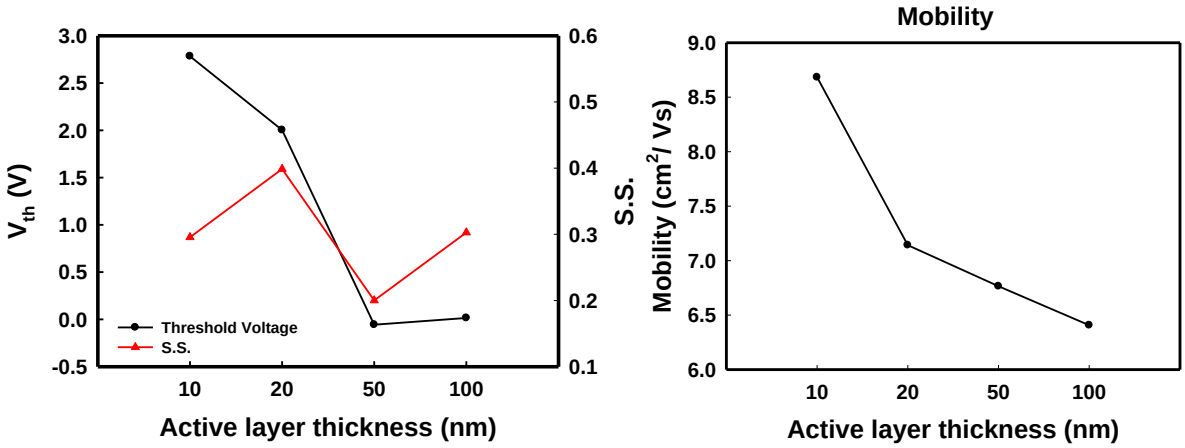


Fig.3-16 The electrical parameters with different IGZO thickness.

3.3.2.2. The reliability of a-IGZO TFTs with different active layer thickness

The reliability of different thicknesses is claimed in this section. The stress conditions are the same in section 3.1.2.2. The figure.3-17 shows the reliability analysis result. For the PGBS, figure.3-17(a), the V_{th} shifted in the positive direction and the amount of V_{th} shift increases with thinner t_{active}. With thicker IGZO layer, the unstable $O_{2(s)}^-$ can be separate from the front channel and decrease the interference with carriers in the front channel. From figure.3-17(b), the phenomenon in NGBS has the same mechanism with t_{active}. The V_{th} shifted to left under NGBS and increase with thinner t_{active} too. With thinner IGZO layer, the H_2O^+ are more closer with front channel and affect more seriously under NGBS.

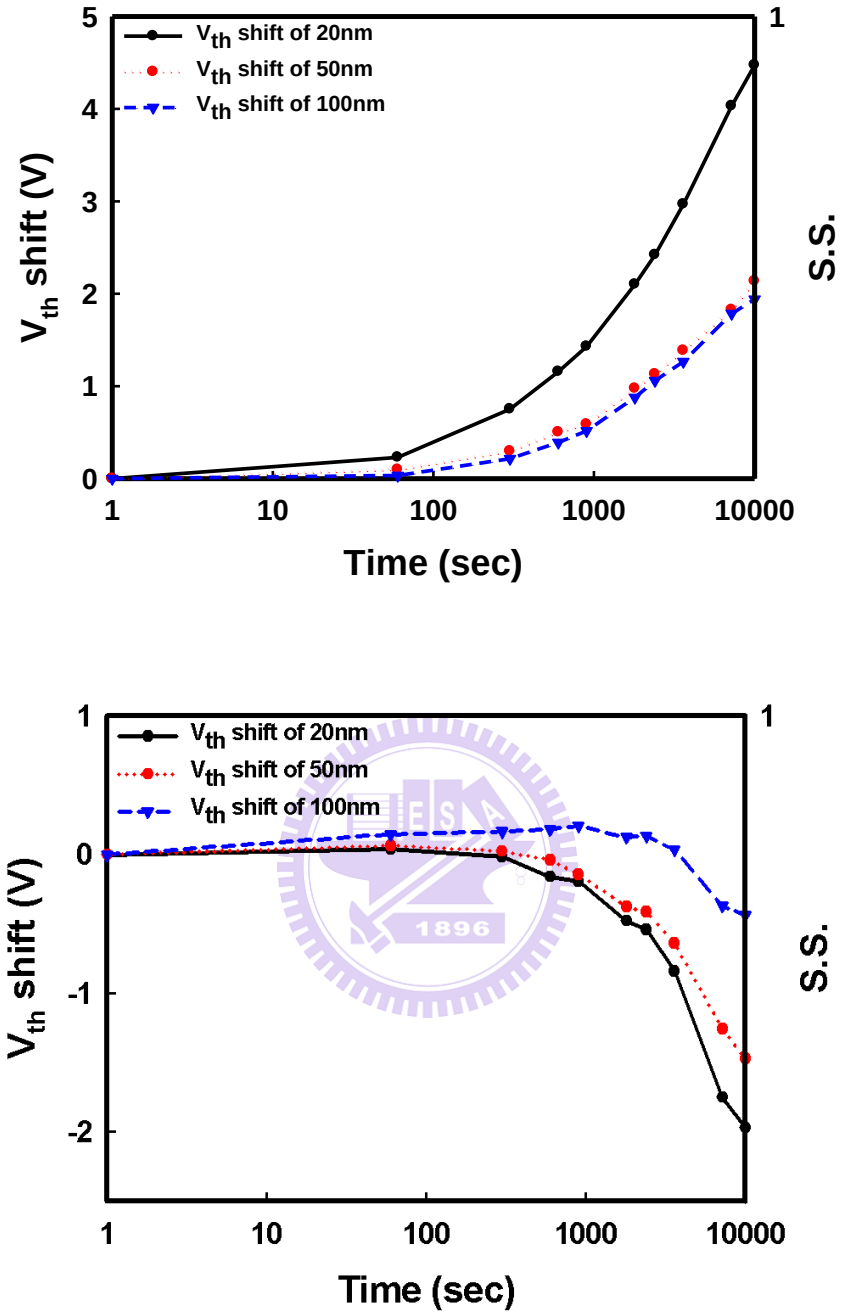


Fig.3-17 The (a) PGBS and (b) NGBS with different IGZO thickness.

3.3.3. Conclusion

In this chapter, a test experiment to check the correction of transport mechanism claimed in last chapter by changing the thickness of t_{active}. As

increasing IGZO active layer, the reliability improve apparently by separating the unstable $O_{2(s)}^{-}$、H_2O^{+} from front channel. Besides, the fundamental electrical characteristic also has a great dependent on IGZO thickness.

Chapter 4

Conclusion

4.1. Conclusions

We successfully report on the properties of a-IGZO TFTs fabricated on Si substrate at room temperature using sputtering process.

In the first part, the oxygen flow rate was varied to examine oxygen content effect in the a-IGZO thin film. The different oxygen flow rate actually influences electrical performance in I_D-V_G curve and there is no tendency about curve shift with different oxygen content. Because of it, we choose the oxygen flow rate 0sccm for our standard recipe to get the best performance of others.

We find the post-annealing improves the quality of a-IGZO film. Although there don't have an obvious change with increasing annealing temperature, the electrical performance shows a great improvement in all electrical characteristic such as V_{th}、S.S and the reliability also improve in 450℃ annealing. Besides, the post-annealing environment also influences a-IGZO TFT. The oxygen vacancy can be filled up in the back channel by annealing with oxygen or nitrogen gas in atmosphere and the leakage current can be pulled down too.

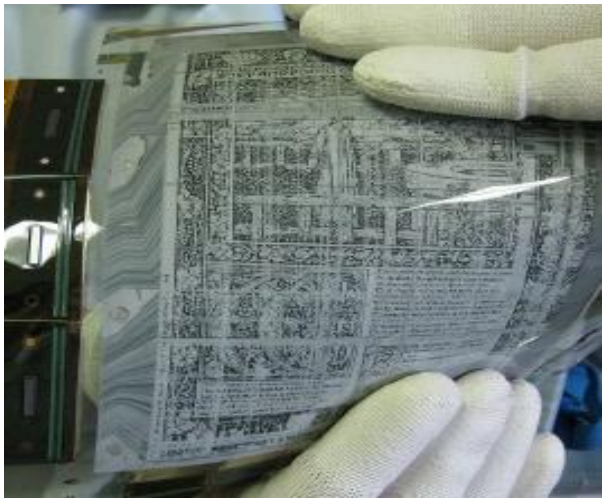
In the second part, the transport model of a-IGZO TFT have be claimed.

Channel for electron to transport can specific into front channel and back channel in a-IGZO layer. The annealing temperature effect the front channel leading to turn-on region and the annealing environment influence the back channel leading to turn-off region.

For the PGBS and NGBS experiments, the magnitude of the V_{th} variation was similar after PGBS in atmosphere and vacuum because of the lack of oxygen vacancy in back channel of samples annealed in oxygen and nitrogen environment. However, H_2O would stay on the surface of a-IGZO and resulted the different V_{th} variation happened under NGBS in atmosphere and vacuum.

4.2. Future Work

The a-IGZO TFT fabricated on Si substrate still have many problems such as large leakage current and this is not a standard structure for panel application. Because of it, in our future work, the a-IGZO TFT fabricate on glass substrate or even flexible substrate will adopted to simulate the real cause in industry. Then the same research will imitate to discuss device performance. The figure.4-1 and figure.4-2 show the oxide TFT fabricated on flexible substrate such as PEN、metal foil and also have a great quality for display [18][19].



2008 IDW Conference

Fig.4-1. The e-paper using oxide semiconductor TFT fabricated on flexible substrate.

2008 IDW Conference

Fig.4-2. Toppan Printing 5.35 inch E-Ink e-paper

Most of the paper research discuss about the D.C stress influence in a-IGZO TFT and don’t mention about the reliability under A.C. gate bias stress. So the next scheme is to figure out the influence about A.C. stress and figure out

the degradation mechanism.

Uses the correlation transistor parameter model, completes the critical electric circuit as well as the application product, for example: Ring-like oscillator(O-ringcircuits), electric charge pump unit (charge pumping), COS-like inverter(ambipolar) and so on the electric circuit characteristic designs. The simulation analyze and manufacture to achieves the concurrently energy conservation and the system conformity demonstration using indium oxide gallium zinc thin film transistor in the same time.

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