國立交通大學

顯示科技研究所

碩 士 論 文

具功能性的有機薄膜封裝保護層在非晶態銦鎵鋅氧化物半導體薄膜電晶體之探討

Study in Functional Organic Passivation on amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors

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摘　　要

雖然非晶態銦鎵鋅氧化物半導體薄膜電晶體具有非常高的載子遷移率，但銦鎵鋅氧化物在大氣環境中不穩定，因此需要封裝保護層來隔絕與大氣中的接觸以達元件長時間操作的穩定性。相較其他有機材料 PTFMA 和 PMMA 具有較高的材料密度和較高的介面疏水性，在本文中被提出用來做為封裝保護層，當元件沉積 PTFMA 後，臨界電壓偏移了 2.3 伏特;沉積 PMMA 後偏移了 6.4 伏特，兩者都展現了非常好的環境穩定性，諸如次臨界區飄移、臨界電壓、載子遷移率都只有些許的改變。最後具彩色濾光片功能性的有機封裝保護層被提出，元件達到 49%的 NTSC 標準。整體來說有機封裝保護層具有非常高的潛力在低沉積損傷、顏色功能性、噴塗，結合這些優勢不論是製程機台或是材料的成本都可以被大幅度的降低。

Study in Functional Organic Passivation on amorphous-Indium-Gallium-Zinc-Oxide Thin-Film Transistors

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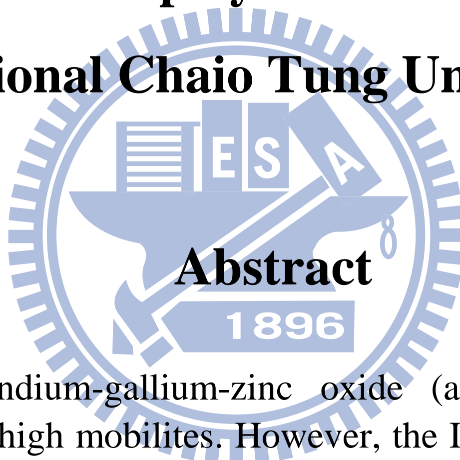

Abstract

The amorphous indium-gallium-zinc oxide (a-IGZO) channel thin-film transistor (TFTs) has high mobilites. However, the IGZO is not chemical stable in ambience; hence the passivation layer is essential for the devices long term stability. Thus the organic passivation PTFMA and PMMA were proposed, due to their high material density (compare with other organic polymer) and hydrophobic feature. An a-IGZO with PTFMA shows a 2.3V threshold voltage (V_{Th}) shift, another with PMMA shows V_{Th}=6.4V shift, both devices revealed good stability in ambience; The sub-threshold swing (s.s.), V_{Th}, and mobilities (μ_{sat}) changed only slightly. Finally, the functional color filter passivation layers were demonstrated, the colored passivation showed 49% National Television Systems Committee (NTSC) standard. In general, organic passivations provided a high potential passivation process for lowering deposition damage, functional color filter, printable, easy process, and lowering cost. These merits in organic passivation can also reduce the equipment and material costs.

Acknowledgement

時光匆匆又到了鳳凰花開的時節,轉眼間兩年已過,在這段求學期間的點點滴滴,如今回想起來真的有種說不出的奇妙滋味,很慶幸的,在人生中最精華的兩年我能夠在交大渡過, 在這裡我真正學到了團隊合作的重要性,有別於以往團隊合作只是一個口號,交大真正落實了團隊合作這個名詞的實際意義,不論在校內或是實驗室內大家彼此學習與合作,又或者與清大進行的梅竹賽,處處都讓我感覺到交大那份團結合作的可貴。

兩年期間我最感謝的莫過於謝漢萍老師與黃乙白老師,在這段時間中,不論是英文口語報告的能力或者是工程與科學研究的精神與邏輯中,我都從謝老師與黃老師身上學到了許多非常寶貴的經驗,雖然謝老師平常忙於公務,和我們見面的時間不多,但從很多小地方都可以看出謝老師對我們的關心與照顧,實驗室也提供相當充足的經費與優質的環境讓我們在研究上面可以盡情的發揮。

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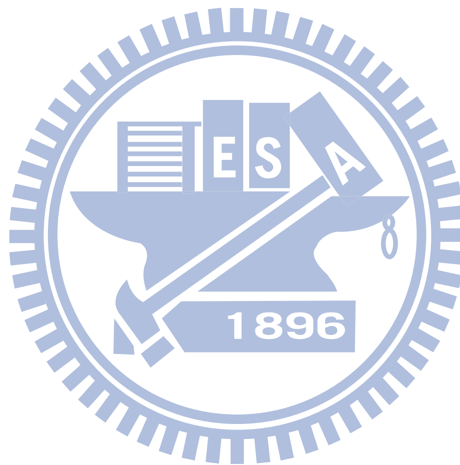

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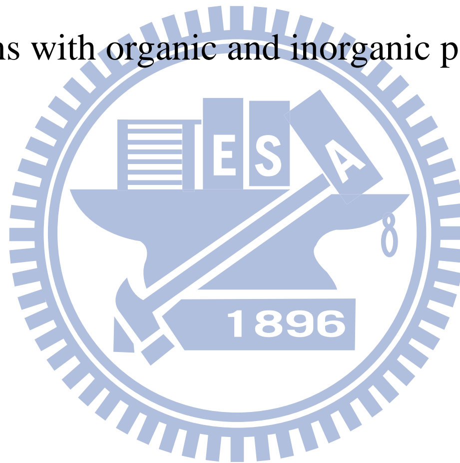

Chapter 1

Introduction

1.1.Background of amorphous-Oxide Semiconductor

Thin-film transistors (TFTs) are critical components for active matrix arrays applied in the flat panel displays (AM-FPDs). Nowadays, conventional AM-FPDs are either based on amorphous or polycrystalline silicon TFT technologies. However, several limitations and drawbacks were observed in hydrogenated amorphous silicon (a-Si:H) TFT arrays, such as visible light sensitivity [1] and low field-effect mobilities. The low field-effect mobility becomes a limiting factor for display performance, especially when the current trend of AM-FPDs development are toward high frame rate (120-240 Hz) [2] and ''all solid-state'' devices, such as active-matrix organic light-emitting displays (AM-OLEDs) [3]. Although polycrystalline silicon (poly-Si) TFTs have high field-effect mobilities, their uniformity on large scale sized panels might not be very applicable. Over the past several years, there has been great interest in TFTs made of transparent oxide semiconductors [4]. This is mainly due to the metal oxide semiconductor TFTs unique advantages, such as visible light transparency, larger-area uniformity at low temperatures, and high carrier mobilities. However, the conventional metal oxide semiconductors such as zinc oxide

(ZnO) are polycrystalline in nature even at room temperature. The grain boundaries of such metal oxides affect the device properties, uniformity and stability over large area which is similar to polycrystalline Si. To overcome this issue, a new ternary amorphous oxide semiconductor (AOS) material composed of indium (In), gallium (Ga), zinc (Zn), and oxygen (O) has been proposed for use as the active layer in TFTs [5]. The amorphous In-Ga-Zn-O (a-IGZO) can more easily form uniform amorphous phase while still having high carrier mobility and flexibility when they are fabricated at room temperature as shown in Fig. 1-1. Nomura groups have demonstrated the a-IGZO devices exhibit the field-effect mobility of 8.3 $cm^2/(V \cdot s)$ in the virgin state (without bending) such a property can be maintained after bending tests at a radii of 30 mm.

Fig. 1-1 The first amorphous oxide semiconductor TFT using a-IGZO channel fabricated at RT on a PET substrate using ITO electrodes [5].

1.2. Development of IGZO

IGZO is an n-type semiconductor with wide band gap (~3.5 eV); its stoichiometry can be usually described as $In_{2x}Ga_{2-2x}$ $(ZnO)_k$, where $0 < x < 1$ and k is an integer that is greater than 0 [6-9]. The single crystal IGZO is composed of alternating layers of InO^{2-} and $GaZnO^{4+}$; the In^{3+} ion has an octahedral coordination, the Ga^{3+} ion has pentagonal coordination, and the Zn^{2+} has tetragonal coordination[6], the figure as shown in Fig. 1-2. Many groups have synthesized bulk samples with varying stoichiometry (both x and k) to evaluate the solubility limits of the oxide. The intriguing result is that, regardless of k, when $x = 0.5$ (equal proportions of In and Ga) the structure is preserved. In other words, $x = 0.5$ form the base compound where all the In^{3+} ions are in the InO^{2-} and all the Ga^{3+} ions are in the $GaZnO^{4+}$ layer.

For $k \leqq 3$, the conductivity decreases as k is increased. This trend is observed in both bulk samples [6] and thin films [7], indicating that the conductivity of IGZO is mainly associated with the In 5*s* states. However, for $k \geqq 4$, the fraction of Zn becomes increasingly large and Zn begins to contribute to conduction. [7] Considering orbital overlap interaction and comparing the ionic radii of cations in the IGZO system is useful for understanding the shift in the conduction path. The ionic radii of Ga, In, and Zn are 1.27, 1.49, and 1.54 A, respectively. As the ionic radii of In and Zn are quite similar, it is not surprising that Zn contributes to conduction as the fraction of Zn increases large [7].

The structure of single crystal and amorphous $InGaZnO_4$ thin films (~250

nm) are examined using extended x-ray absorption fine structure (EXAFS), which is commonly employed to evaluate short range order [10, 11]. The nearest-neighbor distances for In-O, Ga-O and Zn-O in the amorphous film are 0.211, 0.200, and 0.195 nm, respectively. This short range ordering is similar to that of the single crystal structure (0.218, 0.193, and 0.193 nm, respectively). However, it appears that medium range ordering (second 13 nearest-neighbor distances) near the Ga and Zn ions is lost in the amorphous films. *Ab initio* calculations were performed and are in good agreement with the EXAFS results [11].

Additional calculations show that the In-In second nearest-neighbor coordination number in the amorphous state varies with distance (i.e., ~ 1 to ~ 4 for distances of 0.32 to ~ 0.4 nm) and is significantly lower than in the crystalline structure, which has a coordination number of ~ 6. This indicates that the selective (medium range) coordination of In-In is lost in the amorphous structure. From the experimental and calculated results, the coordination numbers of In-O, Ga-O, and Zn-O are thought to be 5, 5, and 4, respectively (Fig. 1-3).

Finally, pseudo-band calculations show that the conduction band minimum is composed of In 5*s* (consistent with the experimental results discussed in the previous paragraph) and that that amorphous IGZO has an isotropic effective mass of ~ 0.2 m_e.

Amorphous IGZO has been employed in a light-emitting *pn* heterojunction [12]. The IGZO layer is deposited by pulsed laser deposition (PLD) at room temperature. The carrier concentration and mobility of this layer is 1×10^{19} cm^{-3} and 5 $cm^2V^{-1}s^{-1}$, respectively. IGZO is chosen here for its reasonable

conductivity at low processing temperatures and its large band gap (~3.5 eV). Blue emission (~430 nm peak) is observed from this *pn* heterojunction and is due to intrinsic exciton recombination in the single crystal *p*-LaCuOSe layer (which has a band gap, carrier concentration, and mobility of ~2.8 eV, 1×10^{19} cm^{-3}, and 8 $cm^2V^{-1}s^{-1}$, respectively).

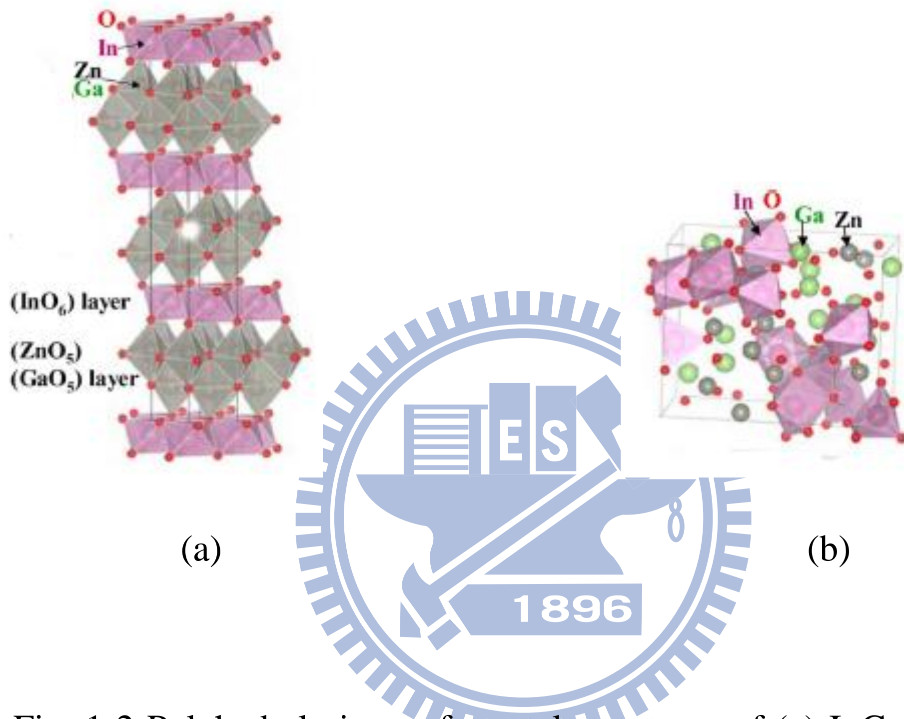

Fig. 1-2 Polyhedral views of crystal structures of (a) $InGaZnO_4$ determined by diffractometery crystal structure. (b) Structure of amorphous $InGaZnO_4$

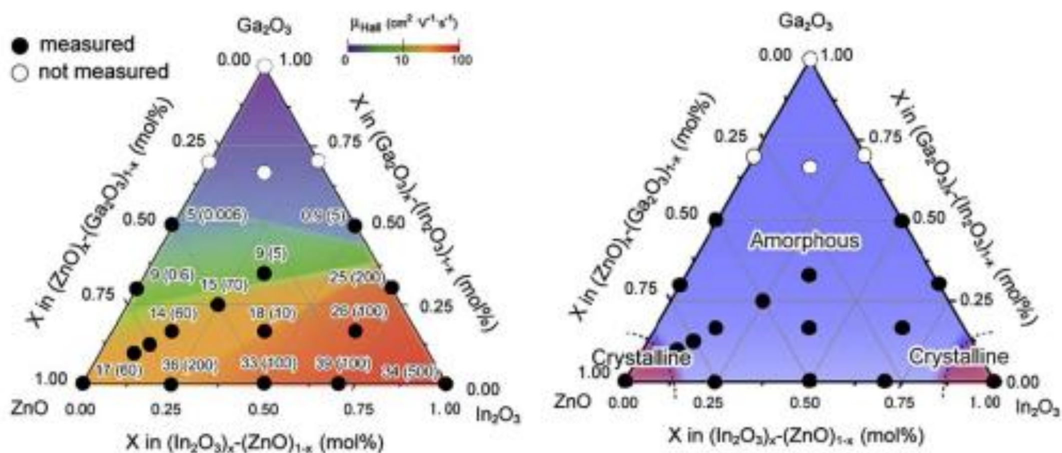

Fig. 1-3 The amorphous formation region (right) and the electron mobilities and concentrations evaluated from the Hall effects for the amorphous thin films (left) in the In_2O_3- Ga_2O_3-ZnO system. The thin films were deposited on a glass substrate by PLD under deposition atmosphere of P_{O2} = 1 Pa. Number in the parenthesis denotes carrier electron concentration.

1.3. The carrier transport mechanism of amorphous $InGaZnO_4$

The mobility of a-Si:H (~1 $cm^2V^{-1}s^{-1}$) is much smaller than that of single crystalline Si (~200 $cm^2V^{-1}s^{-1}$) due to the intrinsic chemical bonding nature. The average carrier transportation paths in covalent-type semiconductors, such as a-Si:H, consist of strongly directive sp^3 orbitals. The bond angle fluctuation significantly alters the electronic levels, causing high density of deep tail-states, as shown in Fig. 1-4.

In contrast, transparent oxides constituting of heavy post transition metal cations with the (n-1) $d^{10}ns^0$ electron configuration, where n $\geq$ 5, are the transparent AOS (TAOS) candidates having large mobilities comparable to those of the corresponding crystals. The electron pathway in oxide semiconductor is primarily composed of spatially spread ns orbitals with an isotropic shape, as shown in Fig. 1-4. The direct overlap among the neighboring n*s* orbital is possible. The degree of overlap of the ns orbital is

insensitive to the distorted metal-oxygen-metal bonding. This feature shows why the Hall mobility of AOSs is similar to the corresponding crystalline phase, even under the room temperature deposition of thin-films.

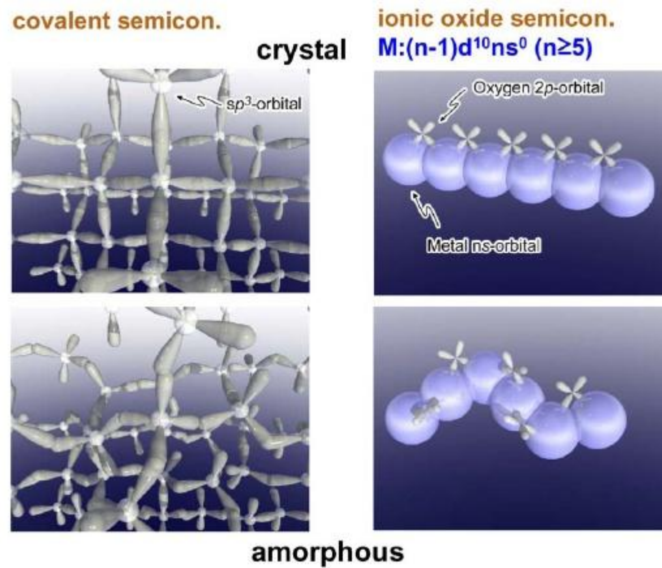

Fig. 1-4 Schematic of orbital drawing of electron pathway (conduction band bottom) in conventional silicon-base semiconductor and ionic oxide semiconductor.

1.4. Motivations and Objectives of Thesis

a-IGZO is not chemically stable in the ambience that the electrical properties of the TFT based on a-IGZO channel are seriously degraded during the operation. Therefore the passivation is essentially required in a-IGZO TFTs because the oxygen and moisture in ambience are thought to trap electrons on the interface of the a-IGZO active layer and lead the instability

and performance degradation of a-IGZO TFTs [13], as shown in Fig. 1-5. Consequently, the passivation is needed as a barrier of oxygen and moisture. Many researches for passivation pay attention to this issue, such as SiO_2, Al_2O_3, and TiO_x inorganic materials [14-16]. However, the inorganic passivation was processed by either PECVD or sputtering at high energy conditions. The interface of the active layer in a-IGZO back-channel region is thought damaged by the plasma or high energy operational conditions during the process. As a result, the electric performance of TFT device, including the V_{Th}, μ_{sat}, and *s.s.* is unstable.

The passivation based on solution processes, such as spin-coating, ink-jet printing, and screen printing with organic materials are also been considered. Among these fabrication processes, the organic polymer passivation not only provides the cost-effective manufacturing process but also lowers the processing temperature. As a result, the damage on the back-channel region can be minimized.

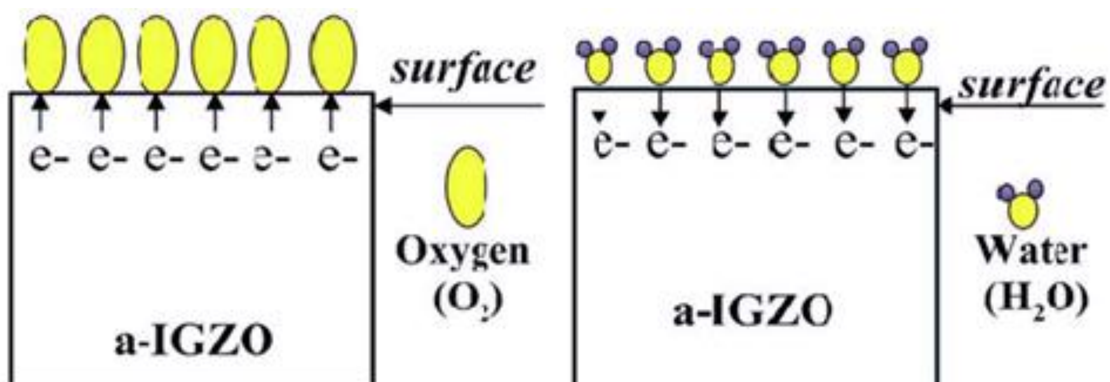

Fig. 1-5 (a) Schematic shows the electric–field-induced adsorption of oxygen molecules from the ambience. (b) Schematic showing the electric-field-induced desorption of moisture molecules at ambience

1.5. Organization of this thesis

This thesis is organized as follows: The basic knowledge of thin-film transistor and the measurement of TFT device parameters are described in **Chapter 2**. The experimental details are presented in **Chapter 3**, and the a-IGZO TFTs stability in ambience or under constant DC voltage stress are illustrated in **Chapter 4**. The performance of a-IGZO TFT before and after passivation is also investigated. Finally, the conclusions and future works will be given in **Chapter 5**.

Chapter 2

Principles and Characterization

The principle of thin-film transistor will be introduced firstly. The basic TFT parameter such as V_{Th}, *s.s.*, On/Off current ratio (I_{on}/I_{off}), and μ_{sat} will be defined. Finally, the morphology of passviation film and the relative structure will be examined by using an atomic force microscope (AFM) and a scanning electron microscope (SEM), respectively.

2.1. Operation principle of TFT

The concept of TFT can be traced back to patent applications filed at 1925 and 1926. While the technically correct name for these devices is “thin-film insulated-gate field-effect transistors” the simplest term “thin-film transistors” was proposed by Weimer to describe the first successful vacuum-deposited field-effect device fabricated in 1961 [16].

TFT are similar in operation and structure to metal-oxide-semiconductor field-effect transistors (MOSFEFs) which are widely used in single crystal Si applications such as dynamic random access memory (DRAM) or digital integrated circuit (DIC). Like MOSFETs, TFTs are three terminal devices with a source terminal (injecting carriers), a drain terminal (extracting carriers) and a gate terminal (for controlling the concentration of carriers in channel region). They are fabricated by sequential deposition of the conductor,

insulator and semiconductor thin-film onto an insulating substrate. The ability to use an insulating substrate, such as glass or plastic, has several advantages compared to using a semiconductor substrate, e.g., (1) substantially low material cost and (2) elimination of the problems such as parasitic capacitances and latch-up which are either unavoidable or additional isolation requirement when using a semiconductor substrate.

To realize the operational mechanism, a bottom-gate-top-contact TFT configuration is plotted in Fig. 2-1. An n-type semiconductor was considered, the three modes of operational energy band diagrams are shown in Fig. 2-1.2 The equilibrium energy band diagram, shown in Fig. 2-2a, means no gate bias is applied to the gate terminal. As a negative bias is applied to the gate, delocalized electrons in the channel are repelled from the semiconductor/gate interface and create a depletion region, as indicated by the positive curvature in the conduction and valence bands in Fig. 2-2b near the insulator. When a positive voltage is applied to the gate terminal, delocalized electrons in the channel region are attracted to the semiconductor/insulator interface, creating electron accumulation at the interface, as indicated by the negative curvature in the conduction and valence bands in Fig. 2-2c close to insulator.

Theoretically, the delocalized electrons are accumulated near the semiconductor/insulator interface during operation. At this moment, a pathway for current conduction is provided when positive voltage is applied to the gate terminal. It is also called the channel region. When the channel was applied a positive voltage, these electrons delocalized in the accumulation layer are extracted from the channel, and given rise to drain current through the TFT. In the similar operational mode, the drain current

conduction can be derived and expressed as a linear relationship in eq. 2.1 when the $V_{DS} << V_{GS}-V_{Th}$ is applied.

$$I_D=(1/2)\ \mu_{sat} C_{ox}(W/L)[(V_{GS}-V_{Th})V_{DS}-V_{DS}^2], \quad (2.1)$$

where the C_{ox} is the gate capacitance, the turn on voltage V_{th} is denoted as the smallest applied gate voltage that causes a non-negligible increase in drain current for a given drain voltage. W and L denoted the TFT's channel width and length, respectively. A more thorough description of the electrical parameters relative to V_{Th} and μ_{sat} is provided in next section. As the drain voltage increases and exceeds $V_{DS} \equiv V_{GS}-V_{Th}$, the drain current ($I_D$) is ideally independent of the drain voltage and this condition is called the saturation regime. The formula for describing I_D is given by equation 2.2.

$$I_D=(1/2)\mu_{sat} C_{ox}(W/L)(V_{GS}-V_{Th})^2, \quad (2.2)$$

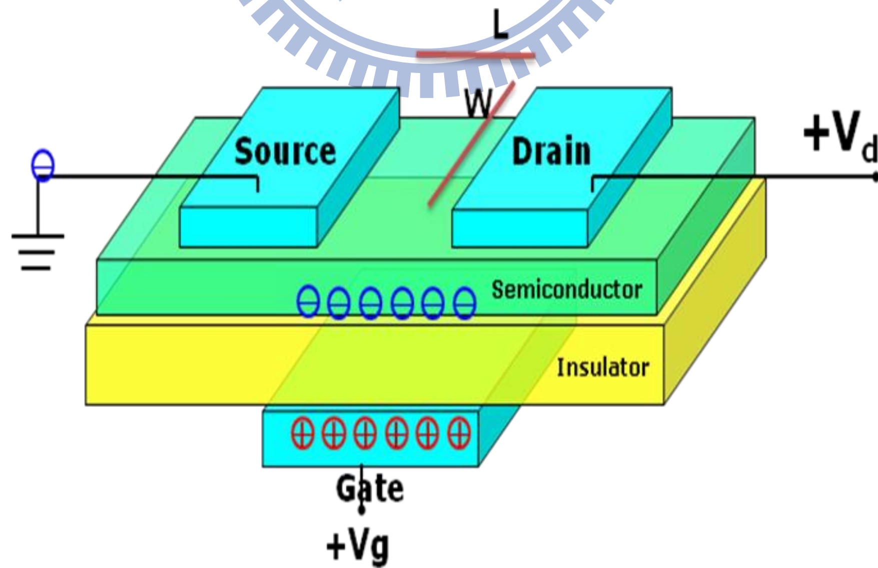

Fig. 2-1 a bottom-gate-top-contact TFT structure

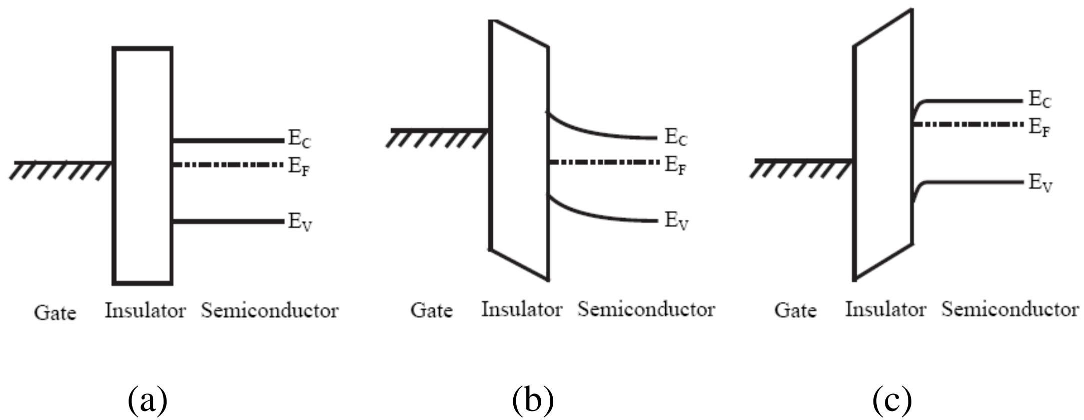

Fig. 2-2 several energy band diagrams as viewed through the gate of the TFT. (a) Energy band diagram when the gate without applied voltage. (b) Energy band diagram when a negative voltage is applied to the gate. (c) Energy band diagram when a positive voltage is applied to the gate contact.

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2.2. Method of Device Parameter Extraction

In this section, the method of typical parameter extraction will be introduced such as V_{Th}, *s.s.*, and μ_{sat}.

2.2.1 Determination of the V_{Th}

Various methods are used to determinate the V_{Th} which is the most important parameter of TFTs. The method to determinate the V_{Th} in this thesis is the constant drain current method that the voltage at a specific drain current

I_N is taken as the V_{Th}. This technique is adopted in most studies of TFTs. It can give a V_{Th} close to that obtained by the complex linear extrapolation method. Typically, the threshold current $I_N=I_D/(W_{eff}/L_{eff})$ is specified at 10nA for V_D=-0.1V and 100nA for V_D=-15V in most papers to extract the V_{Th} of TFTs.

2.2.2 Determination of the sub-threshold swing

s.s., (V/dec.) is a typical parameter to describe the control ability of gate toward channel which is the speed of turning the device on and off. It is defined as the amount of V_G required to increase and decrease I_D by one order of magnitude. s.s. is related to the process, and is irrelevant to device dimensions. s.s. can be lessened by substrate bias since it is affected by the total trap density including interfacial trap density and bulk density. In this study, s.s. is defined as one-half of the V_G required to decrease the threshold current by two orders of magnitude (from 10^{-8}A to 10^{-10}A). The threshold current was specified to be the I_D when the V_G is equal to V_{Th}.

2.2.3 Determination of the μ_{sat}

μ_{sat} is determined from the transconductance g_m at low V_D. The transfer characteristics of TFTs are similar to those of conventional MOSFETs, therefore the I-V relation in the bulk Si MOSFETs can be applied to the TFTs, which can be expressed as Eq. (2.1).

If V_D is much smaller than $V_G - V_{Th}$ and $V_G > V_{Th}$, the I_D can be approximated as (2.2).

The transonductance is defined as

$$g_m = \mu_{FE} C_{ox} \frac{W}{L} V_D \tag{2.3}$$

Thus, μ_{sat} can be obtained by Eq. 2.4.

$$\mu_{FE} = \frac{L}{C_{OX} W V_D} g_m \tag{2.4}$$

The mobility was estimated from Eq. (2.4) with the maximum μ_{sat}

2.2.4. Determination of I_{on}/I_{off}

I_{on}/I_{off} is another important factor of TFTs. The high I_{on}/I_{off} represents not only the large turn-on current but also the small off current (leakage current). The I_{on}/I_{off} affects AMLCD gray levels (the bright to dark state number) directly.

There are many methods to determine I_{on}/I_{off}. The practical one is to define the maximum leakage current as off current when drain voltage is applied at 4.5 V.

2.3. AFM Measurement

The Digital Instruments Dimension 300 atomic force microscope (AFM) was used to characterize the surface morphology of the passivation layer.

The tapping-mode scanning prevents the probe from damaging the sample

surface and can get more precise surface topographic information. In the tapping-mode, the probe oscillates up and down regularly. The cantilever vibrates at various frequencies depending on the magnitude of the van der Waals force between the cantilever tip and the sample surface. A laser beam reflected by the cantilever detects the tiny vibration of the cantilever, as shown in Fig. 2-3. The feedback amplitude and the phase signals of the cantilever were recorded by the computer. The amplitude signals and the phase signals reveal the morphology and the material information, respectively such as roughness and surface morphology.

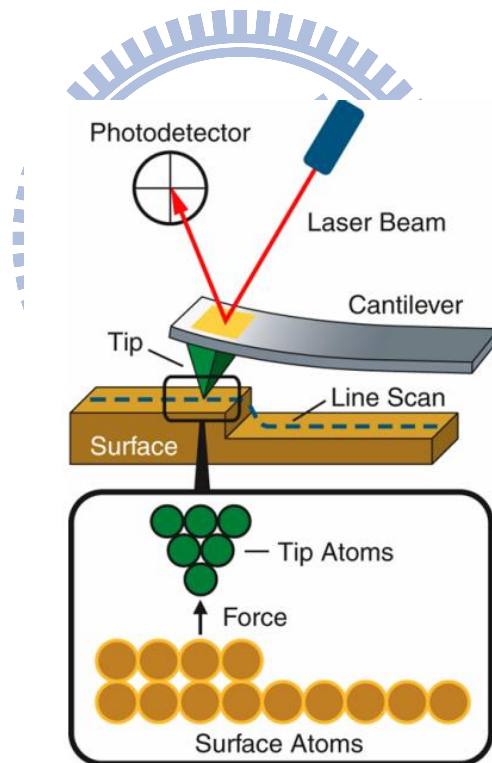


Fig. 2-3 A schematic model of AFM

2.4. Contact angle measurement

The contact angle, formed between the liquid/solid interface and the liquid/vapor interface, is defined by the edge of a liquid droplet on the surface of flat sample, which is illustrated in Fig. 2-5 indices s and l stand respectively for “solid” and “liquid”; the symbols σ_s and σ_l denote the surface tension components of the two phases; symbol γ_{sl} represents the interfacial tension between the two phases, and θ stands for the contact angle corresponding to the angle between vectors σ and γ_{sl}.

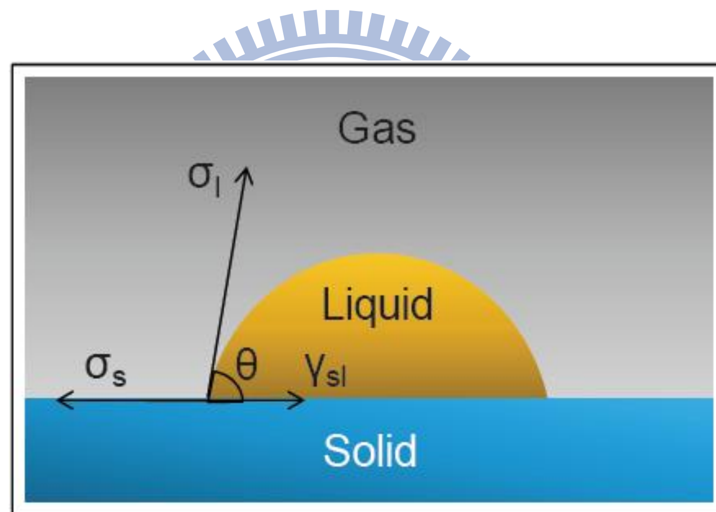


Fig 2-4 The contact angle formation of liquid on solid surface

The contact angle is specific for any given system and is determined by the interaction across the thress. The dropped respectively diode-methane, water on the glass surface with various modification to measure the contact angle in each case. Furthermore, use Young’s equation [17] to calculate the surface energy of different modified passivation. The contact angle measurement and surface

energy calculation were finished by Kruss Universal Surface Tester, GH100

Chapter 3

Experiment Methods

Even a-IGZO TFTs can provide very good performance, the stability is also a concern for practical applications. Several parameters must be considered to evaluate the a-IGZO devices stability, such as the device performance before/after passivation, stability in ambience, and under constant DC bias. In this chapter, the analysis of stability will be depicted, and the fabrication flow of a-IGZO TFTs which including the passivation film will also be described.

3.1 Experimental Section

The purpose of present experiment is to investigate the devices stability in ambience after passivation, and thus to provide fundamental information for deuce stability.

The schematic diagram of experimental flow is shown in Fig. 3-1. It consists of substrate preparation, the flowchart of devices fabrication process, and evaluation of device performance with and without passivation layer.

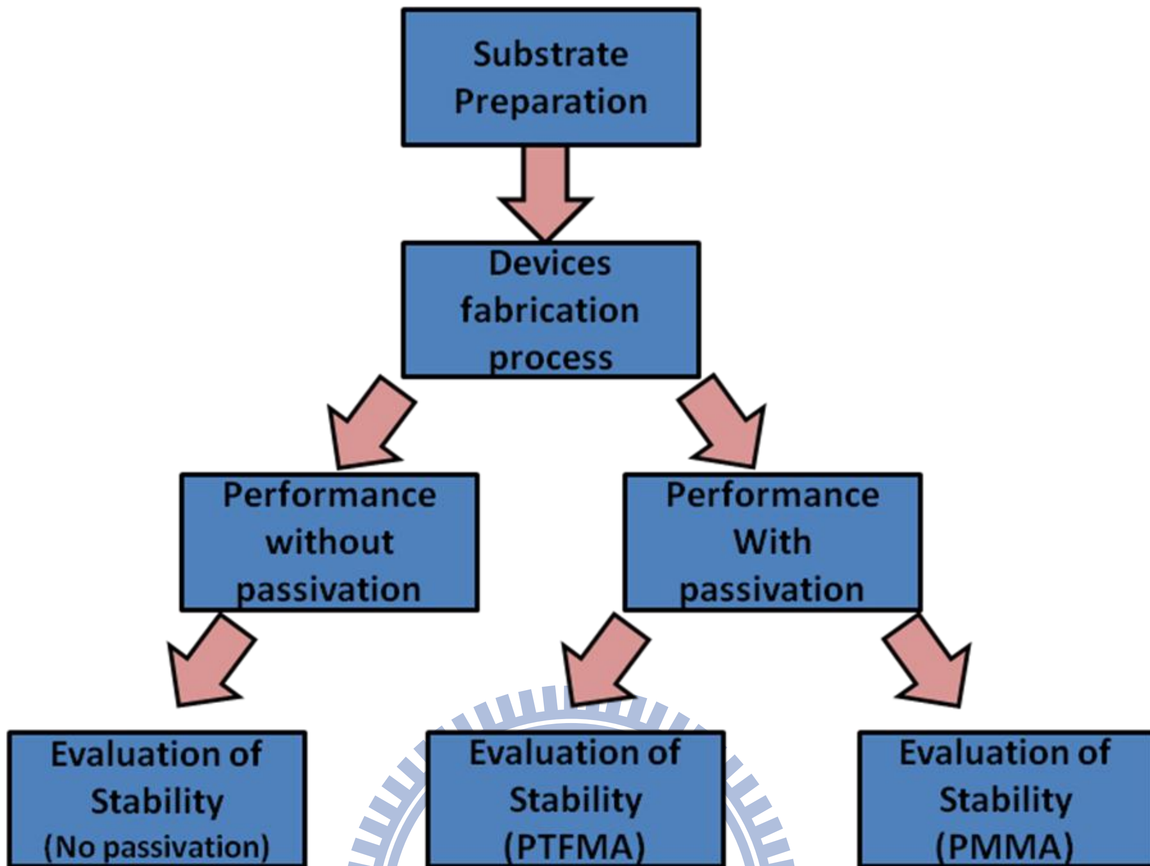


Fig. 3-1 Schematic diagram of experimental setup

3.2 a-IGZO TFT Devices Fabrication process

3.2.1 Substrate preparation

The detail follows:

Step 1: Clean wafer which has thermally SiO_2 by detergent

Step 2: Clean wafer by DI water

Step 3: Place the wafer on the Teflon carrier, and put them into a container with acetone. Ultrasonic vibration for 30 minutes to remove organic contamination.

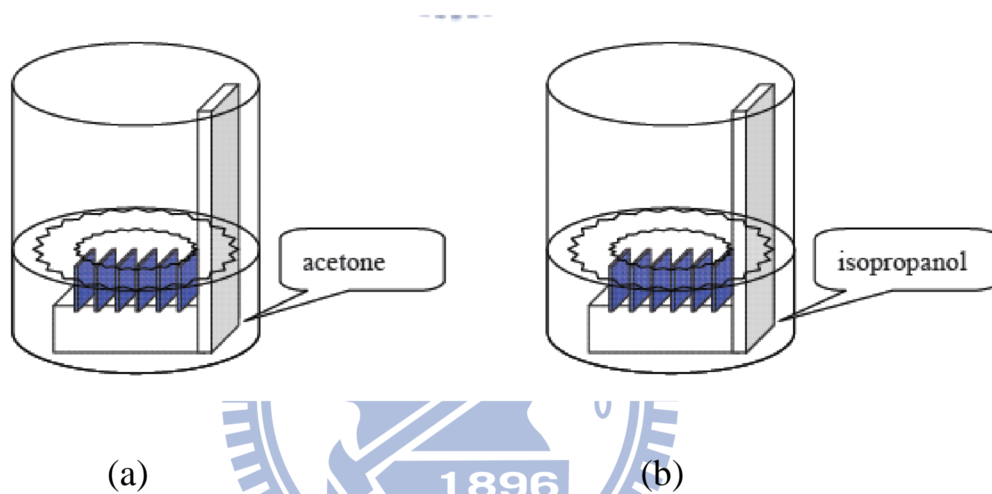
Step 4: Place the wafer into another container with isopropanol (IPA).

Ultrasonic vibration for 30 minutes to remove acetone.

Step 5: Use N_2 jet to purge to dry the wafer; place them into a glass container with a cover.

Step6: Put the wafer container into an oven of 120℃

Step 3 and Step 4 are shown schematically in Fig. 3-2



(a) (b)

Fig. 3-2 Schematic of (a) step 3 and (b) 4

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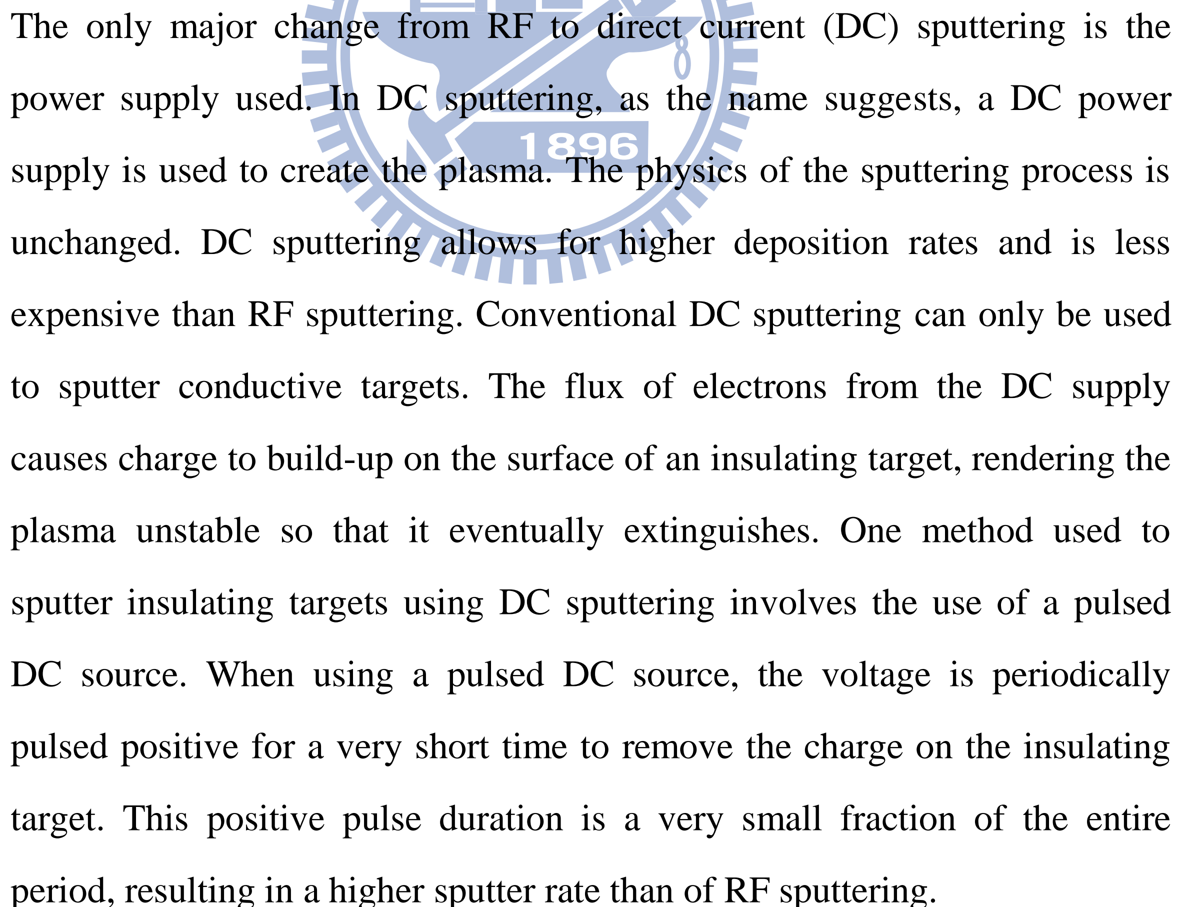
3.2.2 Growth of IGZO and Electrodes

(1) RF sputtering

RF sputtering uses a radio frequency power supply, operating at 13.56 MHz, to generate plasma, which creates ions are used to sputter the target. The ions are accelerated towards the target by a negative DC bias on the target due to the flux of electrons. The ions hit the target with enough energy to dislodge

the target atoms, which are then deposited onto the substrate. RF is performed under vacuum, typically between 1 mTorr and 50 mTorr, to improve the quality and the deposition rate of the deposited film. A lower pressure increases the mean free path, the distance between collisions, and results in the deposited species having more energy to diffuse along the substrate surface in order to find the lowest energy state possible. RF sputtering can be used to sputter both insulator and conducting targets, since charge does not build up on the surface of the target. The major disadvantages of RF sputtering are cost and deposition rate

(2) DC sputtering



The only major change from RF to direct current (DC) sputtering is the power supply used. In DC sputtering, as the name suggests, a DC power supply is used to create the plasma. The physics of the sputtering process is unchanged. DC sputtering allows for higher deposition rates and is less expensive than RF sputtering. Conventional DC sputtering can only be used to sputter conductive targets. The flux of electrons from the DC supply causes charge to build-up on the surface of an insulating target, rendering the plasma unstable so that it eventually extinguishes. One method used to sputter insulating targets using DC sputtering involves the use of a pulsed DC source. When using a pulsed DC source, the voltage is periodically pulsed positive for a very short time to remove the charge on the insulating target. This positive pulse duration is a very small fraction of the entire period, resulting in a higher sputter rate than of RF sputtering.

(3) Sputter system in NCTU

The NCTU sputtering system was placed in class 10K clean room schematic outline is shown in Fig 3-3. Vacuum system composes of rotation pump and cryo pump, which work for different pressure range. Power system consists of several DC and RF power modules with 6 sputtering guns. Purified gas sources are Ar, N, and O. There is also a rotation system to get high uniformity by rotating sample disk and sample holders.

The sputter system with a background pressure was less than 8×10^{-6} torr, shown in Fig 3-4, was employed to deposit a-IGZO thin films. The deposition was at RF power = 80W, and oxygen and argon flow rate at 0.6 sccm and 10 sccm under 6×10^{-6} torr ambient, respectively. The total thickness was controlled at 40nm.

The thermal evaporation system shown in Fig. 3-4 was employed to deposit the Al source and drain electrodes. The evaporation rate was controlled at 3 Å /sec at a pressure of 5×10^{-6} torr and the total thickness was at 1000 Å .

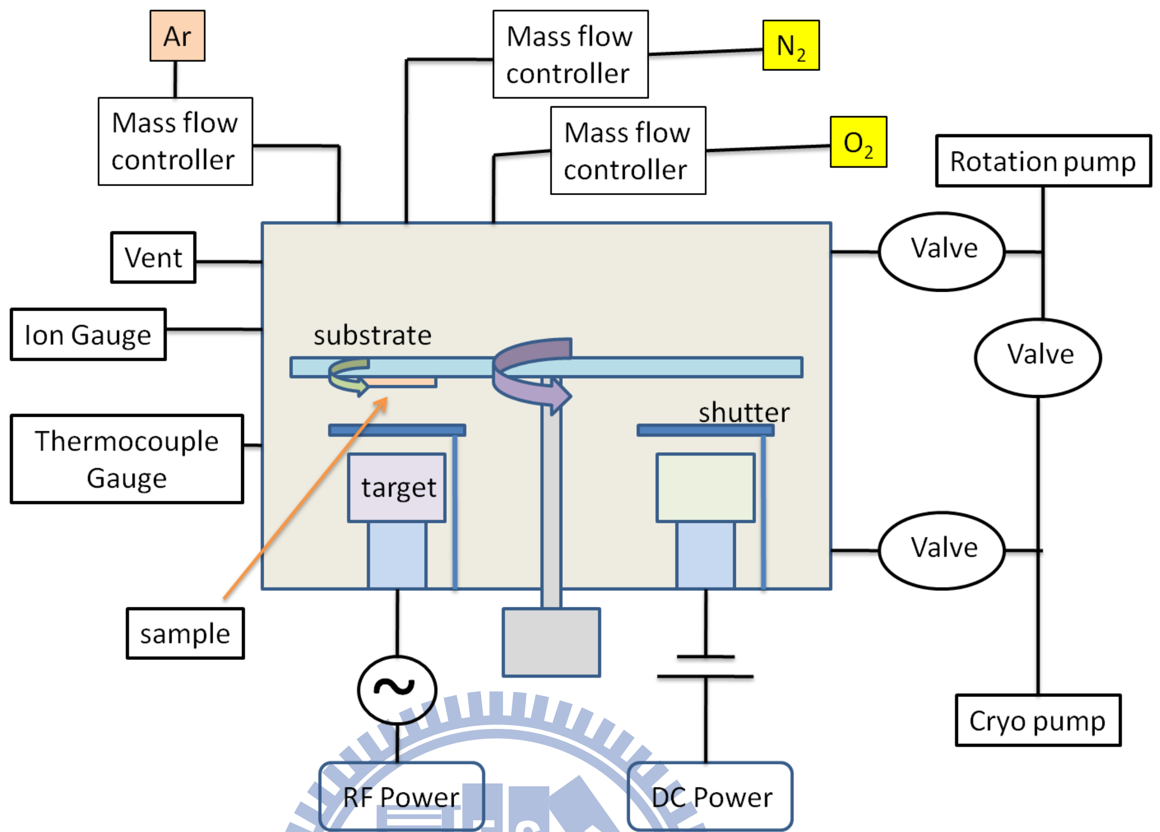


Fig. 3-3 Schematic sputtering system in NCTU

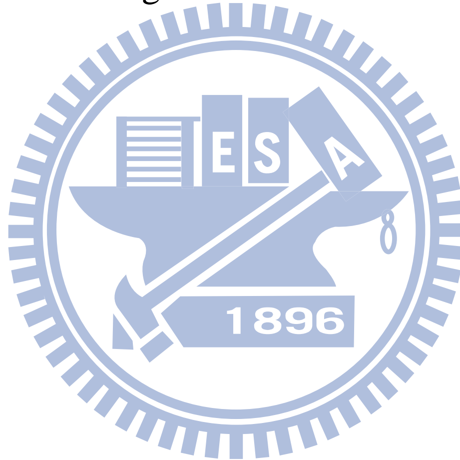
Fig. 3-4 NCTU's sputter system

Fig. 3-5 NCTU's thermal evaporator system

3.2.3 Annealing process

Using to be furnace in nitrogen ambience to anneal a-IGZO. After annealing, the electrical characteristics of the device are better than that of the devices without annealing. The photo of atmospheric anneal furnace is shown in Fig. 3-6. The experiment conditions was controlled at 350℃ and N_2 atmospheric environment, the total annealing time was set in 1 hr.

Fig. 3-6 Tube furnace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3.2.4 Flowchart of Devices fabrication process

A typical a-IGZO TFTs processing flow chart is shown below.

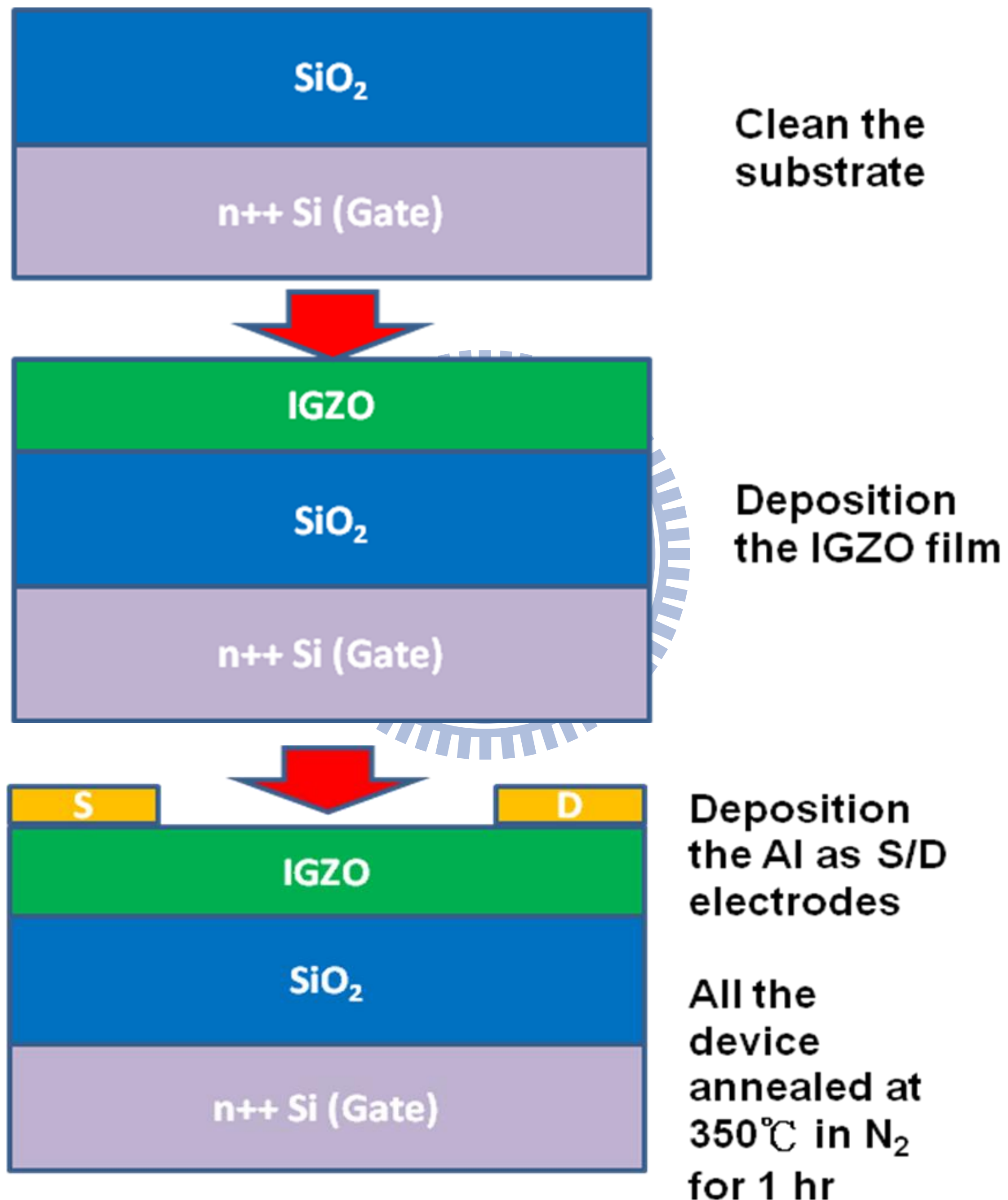


Fig. 3-7 Flowchart of a-IGZO devices fabrication

3.2.5 Organic passivation deposition

Finally, PTFMA and PMMA were separately dissolved in 1,2-dichloroethane with 15 wt% concentration and filtered by a 0.45-μm pore size membrane filter. Thereafter, PTFMA and PMMA solutions were separately spin-coated onto IGZO TFTs at a spin speed of 1000 rpm. The passivated IGZO TFTs were cured at 100℃ for 30 min, and then were stored in ambience for measurements. The chemical structure and relative parameters for PTFMA and PMMA are shown in Fig. 3-7 and Table 3-1, respectively.

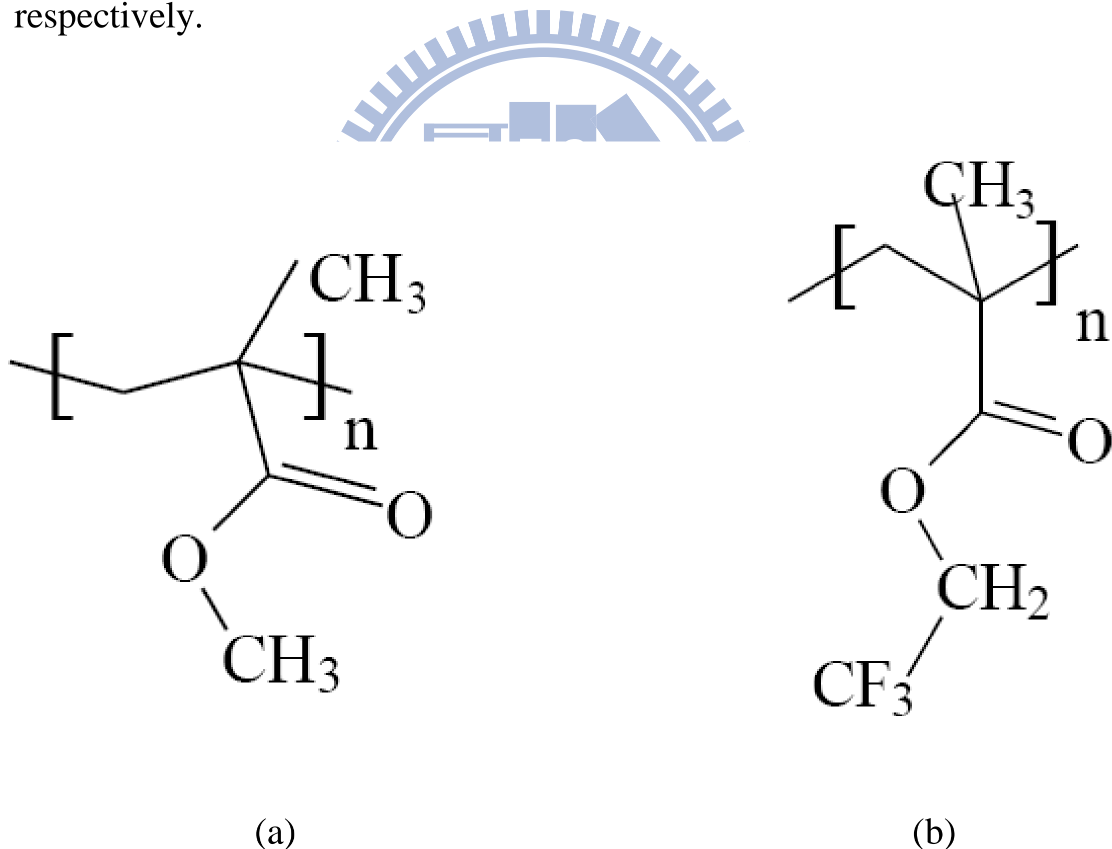


Fig. 3-7 The chemical structure of (a) PMMA and (b) PTFMA

Table 3-1 Organic passivation materials

Material	Abbriviation	Density (g/cm^3)	Molecule Weight (Mw; g/mol)	Water contact angle (°)
2,2,2-trifluoroethylmethlyacrylate	PTFMA	1.2	30000	95
methylmethacrylate	PMMA	1.14	15000	75

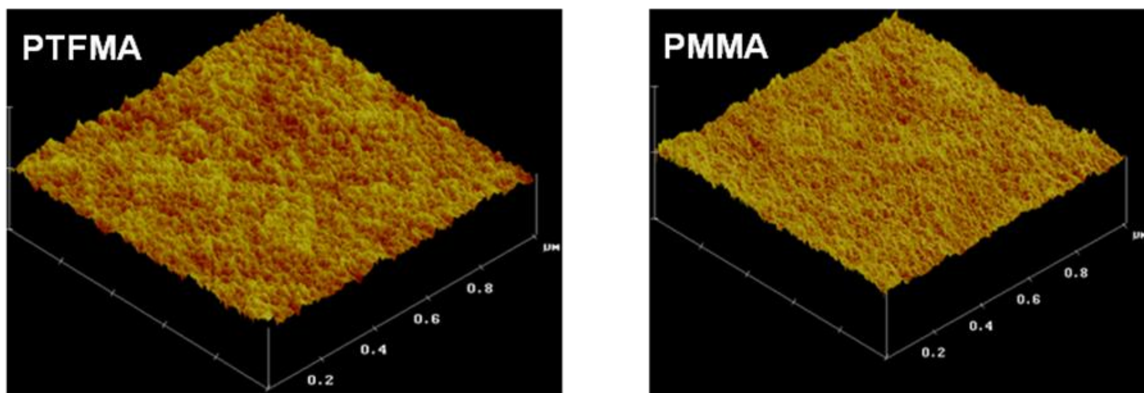
Chapter 4

Results and Discussion

4.1 Thin-film morphology of passivation layer

The topography of passivation layers is a critical issue for the TFT performance, because the subsequent processes are constructed on the top of the passivation layer when preparing an active matrix array black plane.

The thin-film morphology of spin-coated PTFMA and PMMA organic passivations were measured by an atomic force microscope (AFM) and the images are shown in Fig. 4-1 The surface roughness for PTFMA and PMMA are 0.46 nm and 0.41 nm, respectively. The results reveal that the dielectric layer with a quite smooth surface and is suitable for following pixel electrodes process.



(a) (b)

Fig.4-1 AFM (5μm×5μm) images of the thin-film surface morphology on passivation layers (a) PTFMA and (b) PMMA

4.2 Output and transfer characteristics of devices

High energy process such as PECVD or sputtering may damage the back channel, hence, a low energy process by spin-coating the organic passivation PTFMA and PMMA were proposed. The electrical properties of device without and with passivation film are discussed first. The electrical properties of device including I_D-V_G and I_D-V_D, are shown in Figs. 4-2 and 4-3, respectively.

The result in Fig. 4-2 shows a-IGZO devices electrical property without and with PTFMA passivation film. The dark line indicates devices without passivation layers and red line indicate devices with passivation layers. The a-IGZO devices show a 2.3V V_{Th} shift, s.s., μ_{sat}, and I_{on}/I_{off} change only slightly. General PMMA devices exhibited similar results to those of PTFMA-coated device, expect the PMMA devices shows larger V_{Th} shift of about 6.4V. The electrical characteristics also are summarized in Tab. 4-1.

Transfer characteristics of both PTFMA and PMMA exhibited very small change due to the low deposition damage. Interestingly, both devices show negative V_{Th} shift, 2.3V and 6.4V, respectively. In previous study in PMMA process, the side chain group of alkyl group (-OCH_3) as possesses shown in Fig. 4-4a. The -OCH_3 chain can be classified into an electron donor-like [18]. In the semiconductor/passviation interface, -OCH_3 may release electrons into a-IGZO

active layer. This increases the carrier concentrations, and then leads to negative V_{Th} shift. Similarly, PTFMA possesses, the side chain group of fluoroalkyl group ($-OCH_2CF_3$) as shown in Fig. 4-4b. The $-OCH_2CF_3$ group is also an electron donor-like group. The results suggest that the $-OCH_3$ has a stronger electron donor-like effect than $-OCH_2CF_3$. In comparison with $-OCH_2CF_3$ chain, $-OCH_3$ chain affects the a-IGZO film carrier concentrations dramatically. Accordingly, the devices with PMMA passivation layer show a larger V_{Th} shift.

From the viewpoint of device designer, the device performance after passivation layer should be maintained. The device performances passivated by various inorganic layers are summarized in Table 4-2. Obviously, the IGZO devices passivated by either PECVD or sputtering showed serve degradation. Organic passivation PTFMA and PMMA can efficiently suppress the back channel damages. PTFMA revealed better performance than PMMA, because the PTFMA could preserve the devices properties such as V_{TH}, .s.s., and μ_{sat}. In next chapter, the devices stability in ambience will be further discussed.

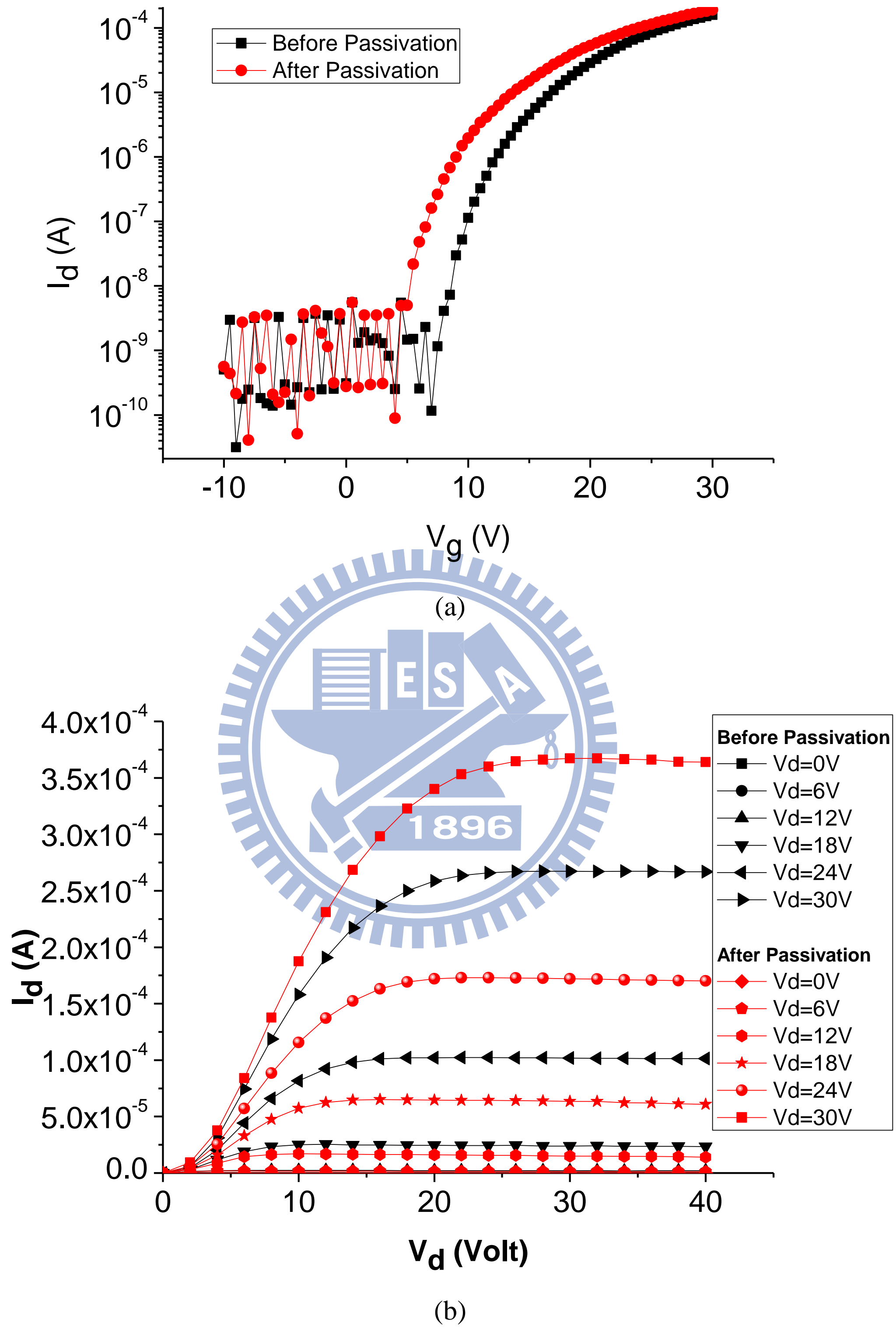
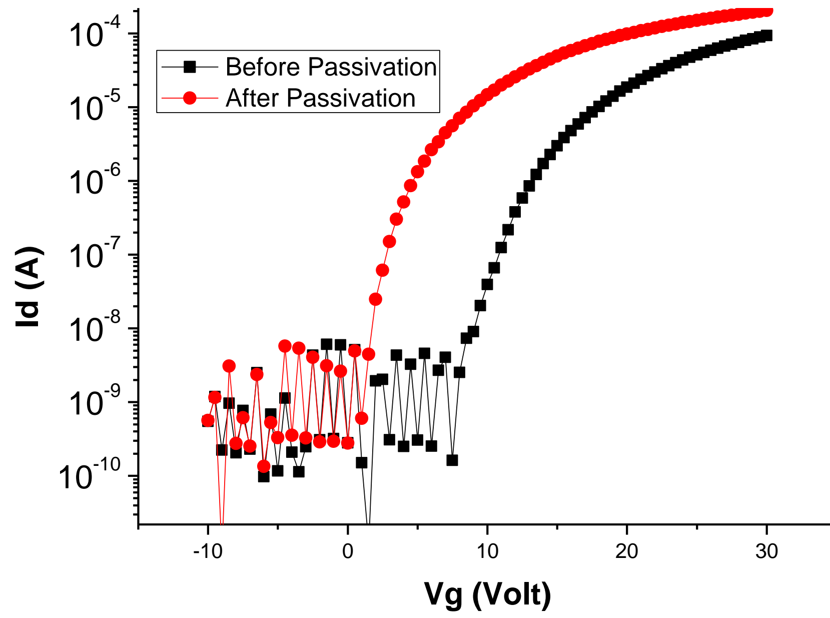
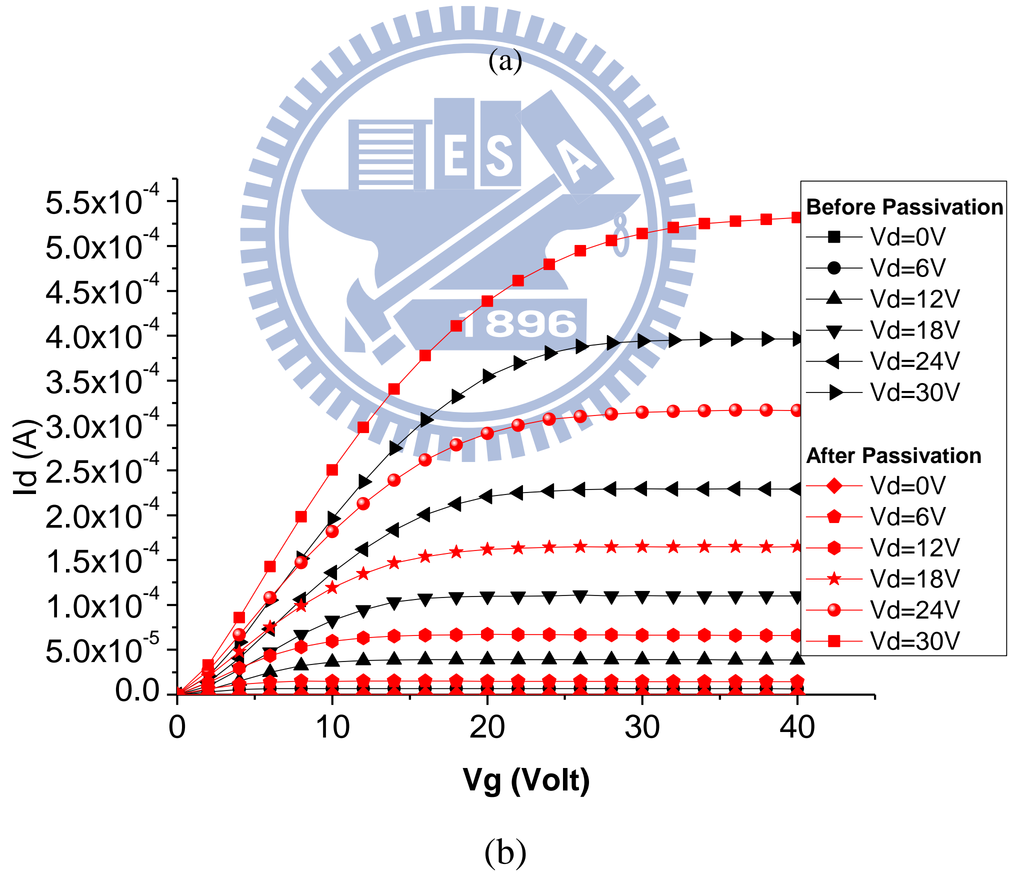


Fig 4-2 Transfer characteristics of a-IGZO TFTs with and without PTFMA passivation layer drain current versus (a) gate voltage, and (b) drain voltage.



(a)



(b)

Fig 4-3 Transfer characteristics of a-IGZO TFTs with and without PMMA passivation layer drain current versus (a) gate voltage and (b) drain voltage.

Table 4-1 the electrical characteristics of a-IGZO devices with and without organic passivation layer

	Mobility ($cm^2V^{-1}s^{-1}$)	I_{on}/I_{off}	Subthreshol swing (V/dec)	Threshold voltage (V)	Dielectric constant	Drain current (A)
Before PTFMA passivation	8.07±0.12	6.0*10^5	1.75±0.08	6.50±0.30		2.75*10^{-4}
After PTFMA passivation	8.30±0.11	6.0*10^5	1.69±0.08	4.22±0.20	6	3.50*10^{-4}
Before PMMA passivation	7.71±0.26	5.0*10^5	1.45±0.08	7.38±0.77		4*10^{-4}
After PMMA passivation	7.86±0.23	4.7*10^5	1.52±0.09	1.00±0.10	3.2	5.3*10^{-4}

Table 4-2 The a-IGZO device performance by various inorganic passivations

Passivation	Mobility degradation	V_{th} shift (V)	S.S. degradation (V/dec)	Process	Ref.
SiO_2	- 31.28%	5.54	0.99 1.09	PECVD	J. H. Cho et al., SID 08, DIGEST 625
Al_2O_3	- 24.86%	22.90	Increase greatly	ALD	D. H. Cho et al., SID 08, DIGEST 1243
Ga_2O_3	- 44.44%	15.00	Increase greatly	Sputter	D. H. Cho et al., Journal of The Korea Physical Society Vol. 54 NO. 1 (2009)

4.3 a-IGZO TFT device stability in ambience

For long term operation, the device stability in ambience is important. Several experiments were set up to evaluate the device stability in ambience, including the devices without passivation layer, with PTFMA, and with PMMA.

In first experiment, the devices without passivation was exposed in ambience for 24 days, the environment conditions are 26℃ and 78% RH. After exposure in ambience, the device transfer characteristic showed severe degradation, as shown in Fig. 4-5. Obviously, the interactions between the active back-channel and ambient played a critical role in the performance degradation. It is well known that adsorbed oxygen can capture an electron from the conduction band and the resulted oxygen species can exist in various forms such as O^{2-}, or O^{-}, as described by Eq. (4-1). As a result of charge transfer, a depletion layer is formed in beneath the Zn-based oxide surface, leading to an increase in the V_{Th} of the transistor [19]

$$O_2\,(gas) + e^- = 2O^-\,(solid) \qquad (4\text{-}1)$$

The equilibrium constant K is given by $[O^-]_{solid}/P_{O2}[n]$, where $[O^-]_{solid}$, P_{O2}, and $[n]$ are the adsorbed oxygen concentration on the IGZO surface, the partial oxygen pressure, and the electron density in the channel, respectively. As pointed out in previous study [20], an increase in P_{O2} results in a positive V_{Th} shift in the resulted oxide transistor because the equilibrium constant K should be invariant at a fixed temperature. As a result, the concentration of O^-_{solid} increases. Hence, the oxygen would dominate a positive V_{Th}.

However, the result in first experiment shows a negative V_{Th} shift, which is

attributed to moisture in ambience [21]. When a-IGZO film adsorbs moisture, the trap density will increase. It is speculated that the traps created due to H_2O adsorption in deep-level state. The deep-level state can be classified into acceptor-like trap which causes a negative V_{Th} shift. The schematics including adsorption of oxygen and moisture are depicted in Fig. 4-6.

To evaluate the ability of ambience barrier, PTFMA and PMMA were chosen as passivation layer, due to their high material density (PTFMA=1.2 g/cm^3, PMMA= 1.14 g/cm^3), and high water contact angle (PTFMA=95°, PMMA=75°). The following experiment would focus on the devices with passivation layer. The results are shown in Figs. 4-7 and 4-8, respectively. When the PTFMA and PMMA devices are exposed in ambience, both devices show almost the same performance after 24 days. The devices parameters are summarized in Table 4-3. The devices without a passivation layer showed a significant increase of S.S. (increase of 1.6), and V_{Th} (shift to 3.4V) with time. The a-IGZO devices with PTFMA and PMMA passivation layer showed good stability in ambience. Two devices have similar results, the reasons can be attributed to that PTFMA (1.2 g/cm^3) and PMMA (1.14 g/cm^3) have similar material density, which directly affects the ability of barrier to gas. To confirm the data, five passivated a-IGZO devices separately with PTFMA and PMMA passivaiton layer were prepared and almost similar changes in all passivated device were obtained.

When the devices were passivated, the devices stability was improved, essentially. However, organic dielectric materials are thought to be poor in water resistance because it may absorb water in ambience. Therefore, the devices stability in high humidity environment also will be discussed in next chapter.

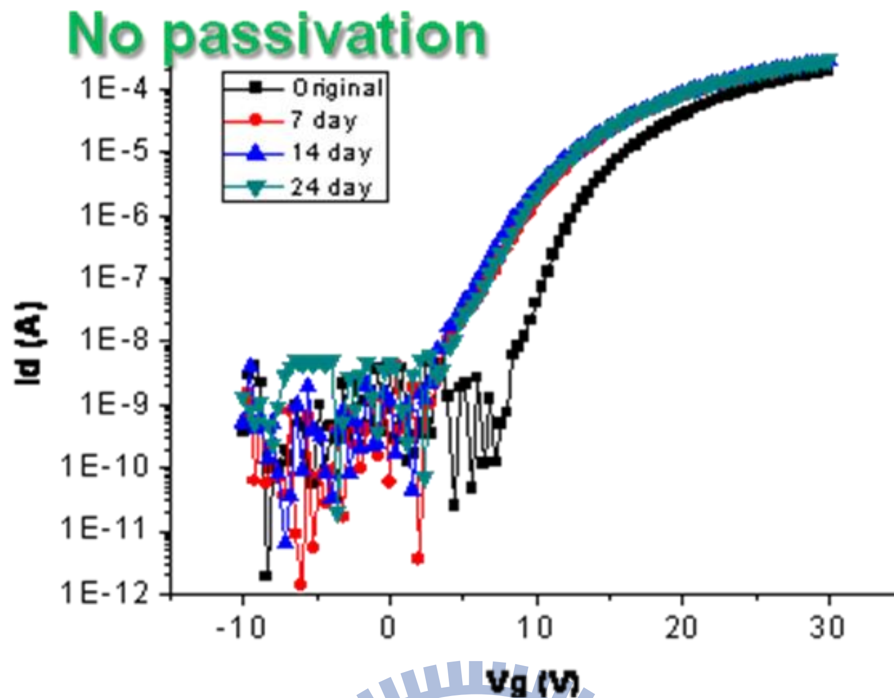
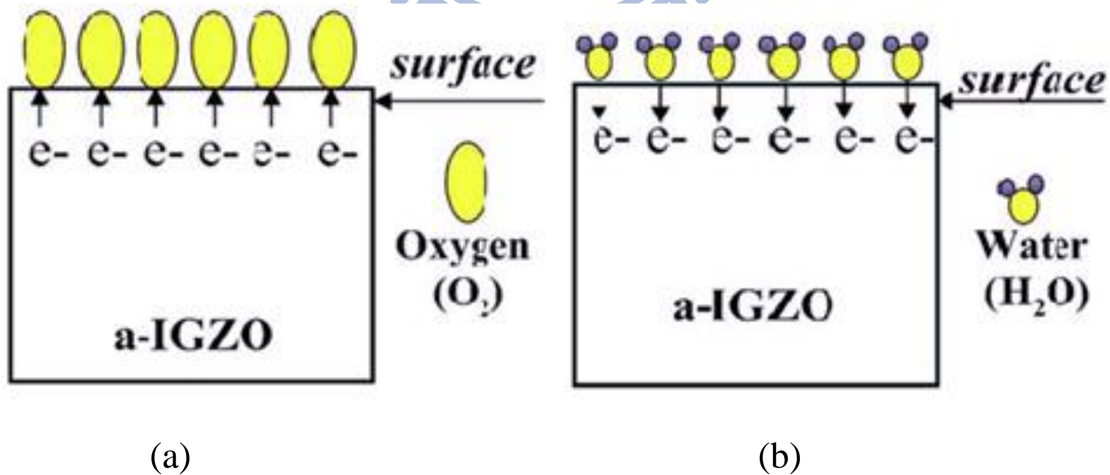


Fig 4-4 Transfer characteristics of a-IGZO TFTs without passivation stored in ambience for 24 day



(a) (b)

Fig. 4-5 (a) Schematic of the electric–field-induced adsorption of oxygen molecules from the ambience. (b) Schematic of the electric-field-induced desorption of moisture molecules at the ambience.

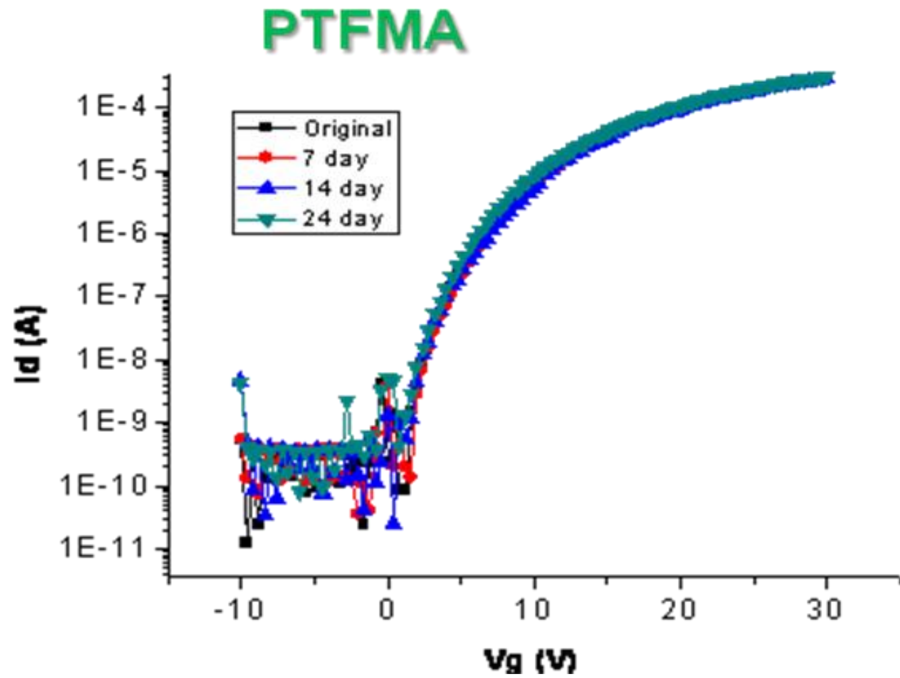


Fig. 4-6 Transfer characteristics of a-IGZO TFTs with PTFMA passivation layer stored in ambience for 24 days.

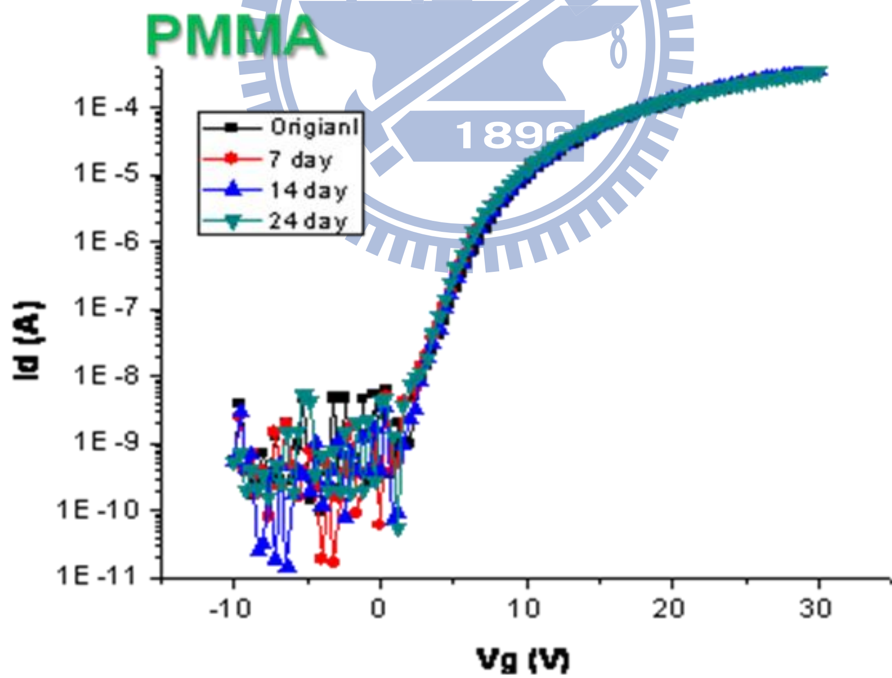


Fig. 4-7 Transfer characteristics of a-IGZO TFTs with PMMA passivation layer stored in ambience for 24 days

Table 4-3 The a-IGZO device electrical characteristics exposed in ambience for 24 days without and with organic passivations

	Storage Time (Day)	Mobility (cm^2/V-s)	S.S. (V/dec)	V_{th} (V)
No passivaiton	1	8.02±1.21	1.14±0.17	4.7±1.1
	24	9.01±0.81	2.73±0.23	1.3±0.4
PTFMA	1	8.13±0.70	1.50±0.14	1.2±0.3
	24	8.15±0.54	1.52±0.19	1.1±0.3
PMMA	1	8.10±0.65	1.79±0.11	1.3±0.3
	24	8.07±0.62	1.82±0.13	1.2±0.3

4.4 a-IGZO TFT devices stability in high humidity environment

To ensure that the device with PTFMA and PMMA still can function in severe environment, both devices were stored in a high humidity conditions, 60 ℃, 95% HR for 5 days

After exposure in high humidity conditions, both PTFMA and PMMA devices revealed a negative V_{TH} shift, the results as shown in Figs. 4-9, and 4-10, respectively. A negative V_{TH} shift can be ascribed to the moisture catch electron in back channel. To confirm the data, five devices were measured and the results shown in Fig. 11. The PTFMA devices revealed about 3V shift and the PMMA devices revealed about 4V shift. In comparison, PTFMA has larger water contact angle (PTFMA=95°, PMMA=75° as shown in Fig. 4-12) which directly

affect the ability of water resistance. Base on the property of high water contact angle PTFMA possess better passivation characteristics.

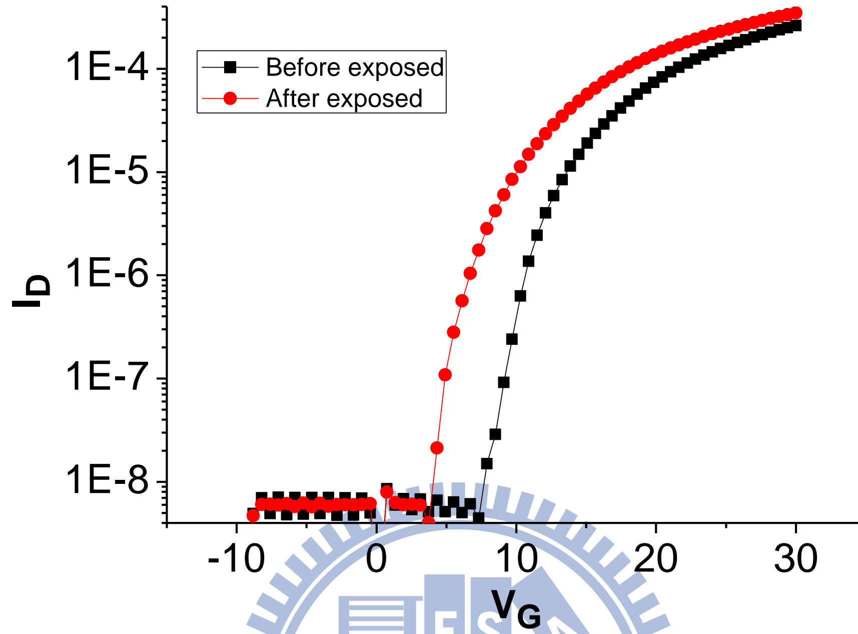


Fig. 4-8 Transfer characteristics of a-IGZO TFTs with PMMA passivation layer stored in high humidity condition for 1 day.

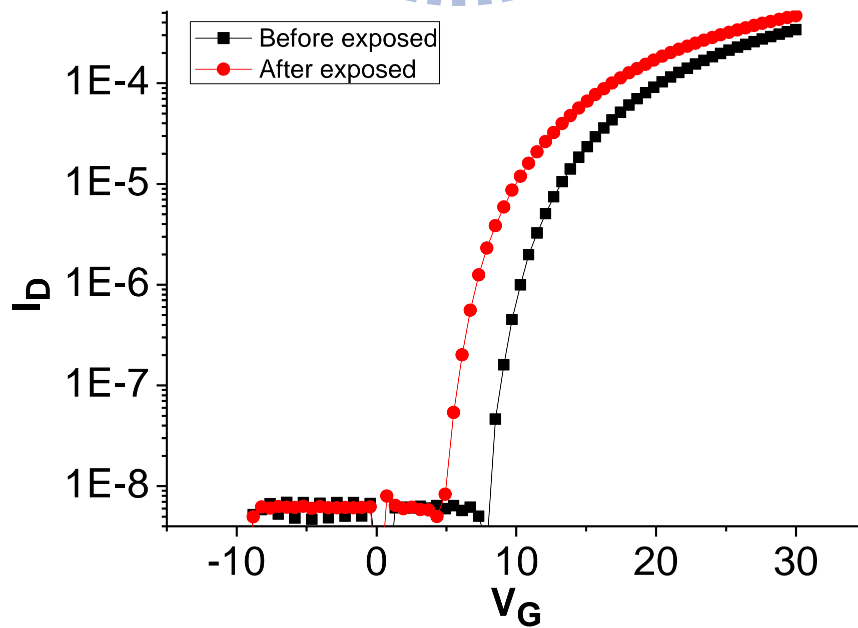


Fig. 4-9 Transfer characteristics of a-IGZO TFTs with PTFMA passivation layer stored in high humidity condition for 5 day.

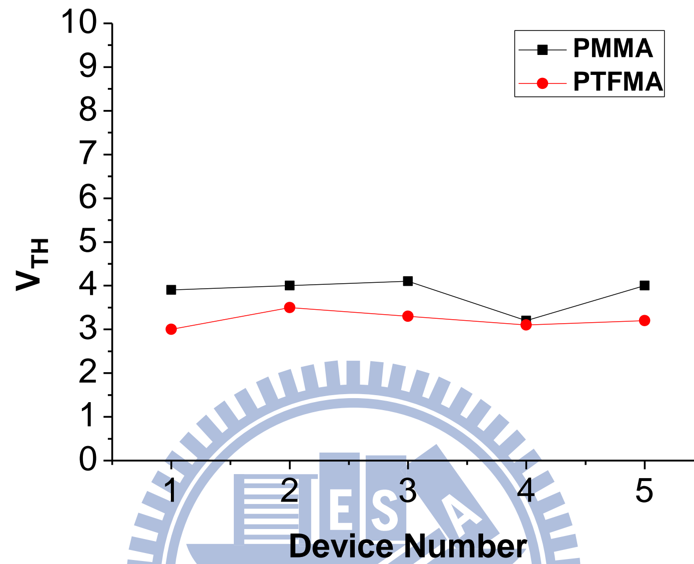
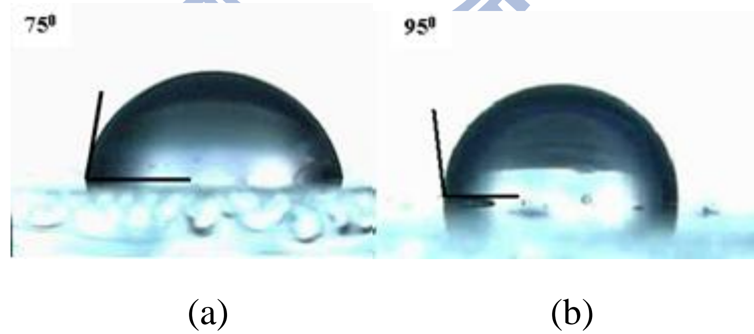


Fig. 4-10 a-IGZO devices V_{Th} shift including the with PTFMA, and with PMMA passivation layer



(a) (b)

Fig. 4-11 The water contact angle for (a) PMMA and (b) PTFMA

4.5 a-IGZO TFT devices stability under DC stress

In AMLCD's, the TFT is used as a digital switch driven with duty cycles for only ~0.1%, making the circuit fairly insensitive to the conventionally large V_{Th} shifts of a-IGZO devices. In contrast, the TFT driver in an AMOLED pixel operates in DC, the OLED current depends directly and continuously on the TFT V_{Th}. An increase in the V_{Th} of the driver TFT's over time reduce the OLED drive current and therefore decreases the brightness of the pixel, as shown schematically in Fig. 4-13. Hence, the devices stability under DC bias stress also is very important to evaluate the device stability.

Measurement at high gate stress fields (V_G=20V) were performed by grounding the TFT drain and source (V_D=V_S=0 V) and applying a voltage to the gate. The V_{Th} shift was found by the difference of the V_{Th} shift extracted from the TFT characteristics before and after applying the stress.

When the devices without passviation layer, the V_{Th} revealed a significantly shift to positive as shown in Fig. 4-14. The mechanisms responsible for the V_{Th} shift in a-IGZO TFT's were (i) the trapping of electrons in the gate insulator and (ii) creation of defects in a-IGZO at or near the a-IGZO/insulation interface, and (iii) electron trapping within the IGZO channel layer [22]. In the first mechanism, channel electrons tunnel into the empty trap states in the insulator, resulting in shift of the threshold voltage. In the second mechanism, the creation of deep electronic states produced within the IGZO layer and concomitant trapping of accumulation layer electrons during operation of a-IGZO TFT. In the third mechanism, the conduction band electron traps distributed throughout the IGZO layer. The three mechanisms were summarized in Fig. 4-15.

However, the first mechanism is unlikely for the insulator/a-IGZO TFTs tested herein, considering the high electric fields required and the small capture cross section of thermal SiO_2 [23]. Thus, this mechanism is eliminated for further consideration. Actually, the oxygen and moisture in ambience might affect the second and third mechanisms. During DC stress, oxygen or moisture may attach to the back channel, and capture the carrier, the concept as shown in Fig. 4-16. Hence, the V_{Th} of a-IGZO devices will shift to positive. In the case of devices with passviation, the V_{Th} was greatly suppressed, the result shown in Fig. 4-17. For comparison, the V_{Th} versus stress time for the sample without, with PTFMA, and with PMMA passivation layer were summarized in Fig. 4-18. The results clearly indicate that for the passivated devices, the V_{Th} was suppressed to 3V. The two devices have similar results. The results also can be attributed to both PTFMA and PMMA with similar material density.

The positive V_{Th} shift during positive V_G stress comes not only from the charge trapping, but also from the dynamic interaction between the exposed back channel and the ambience. Compared with other inorganic passivation layer such as SiO_2, the V_{Th} shift is 0.75V [24]. It is much lower than organic passivation layer. Hence, single organic passivation layer still difficult to achieve long term stability for AMOLED. However, organic passivation layer provides a method of low deposition damage to the device back channel. To maintain the devices stability and performance, the double passivation layer inorganic/organic may be a solution.

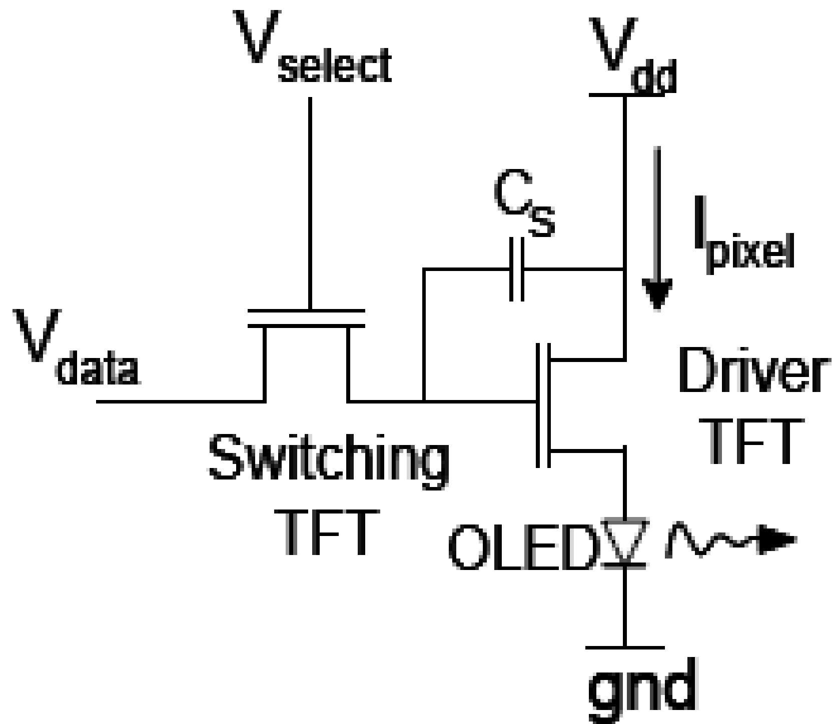


Fig. 4-12 Schematic of the AMOLED driver and switching TFT

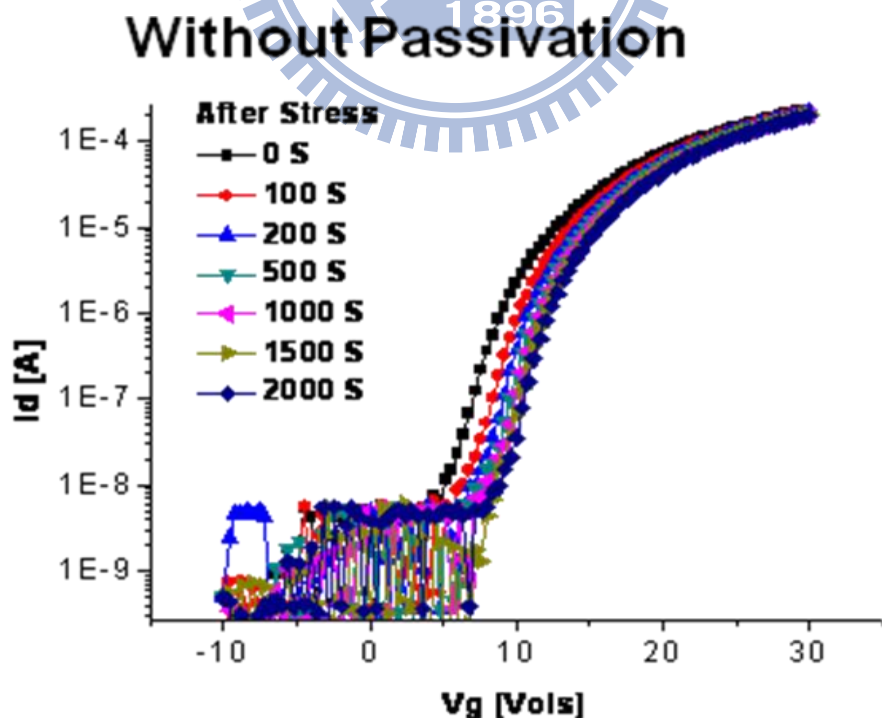


Fig. 4-13 The a-IGZO device without passivation layer after stress for 2000 s

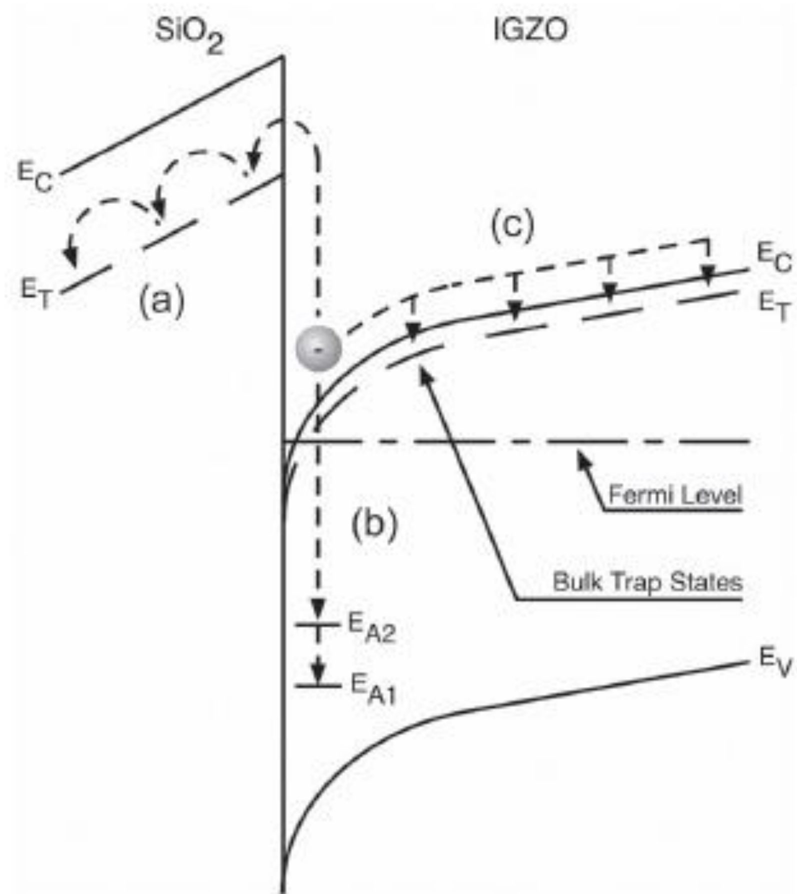


Fig. 4-14 Energy band diagram of a-IGZO devices, illustrating three instability mechanisms: (a) Electron injection and trapping within the gate insulator, (b) deep state creation for the explicit case of a zinc vacancy, and (c) electron trapping within the a-IGZO channel layer.

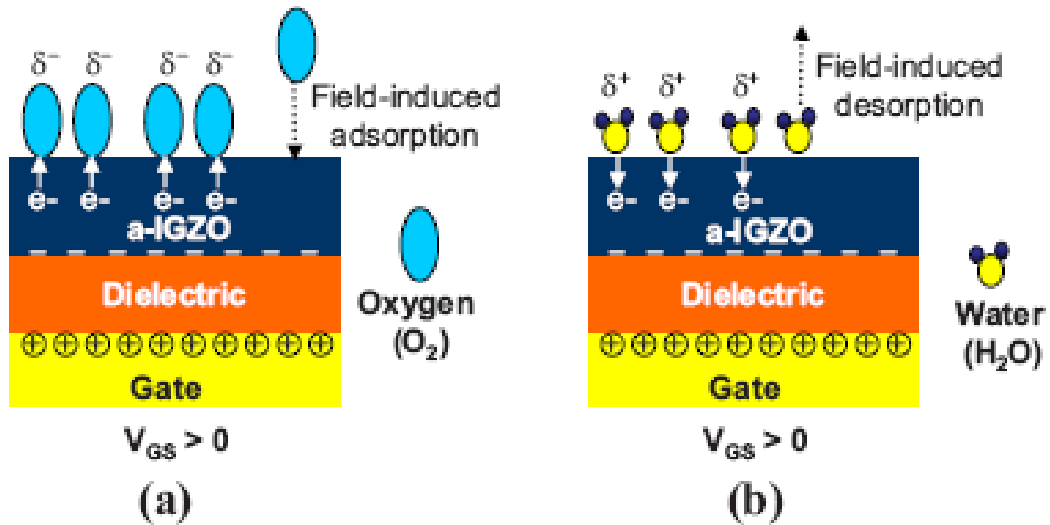


Fig. 4-15 (a) Schematic of adsorption of oxygen molecules from the ambience under the application of positive gate voltage stress. (b) Schematic of adsorption of moisture into the ambience under positive V_{GS} stress [19].

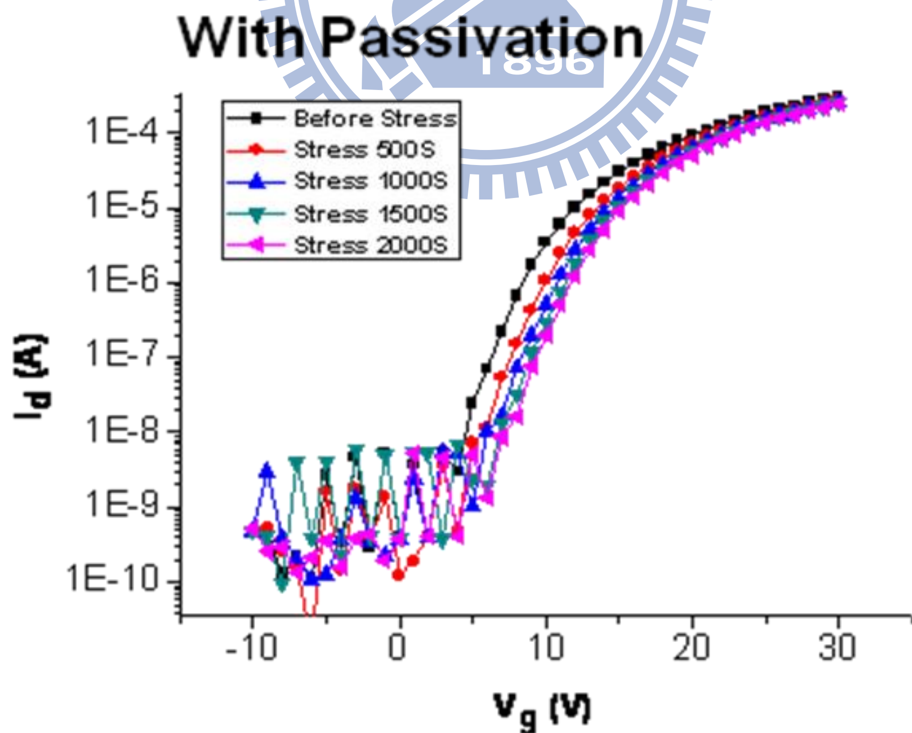


Fig. 4-16 a-IGZO device with passivation layer after stress for 2000 s

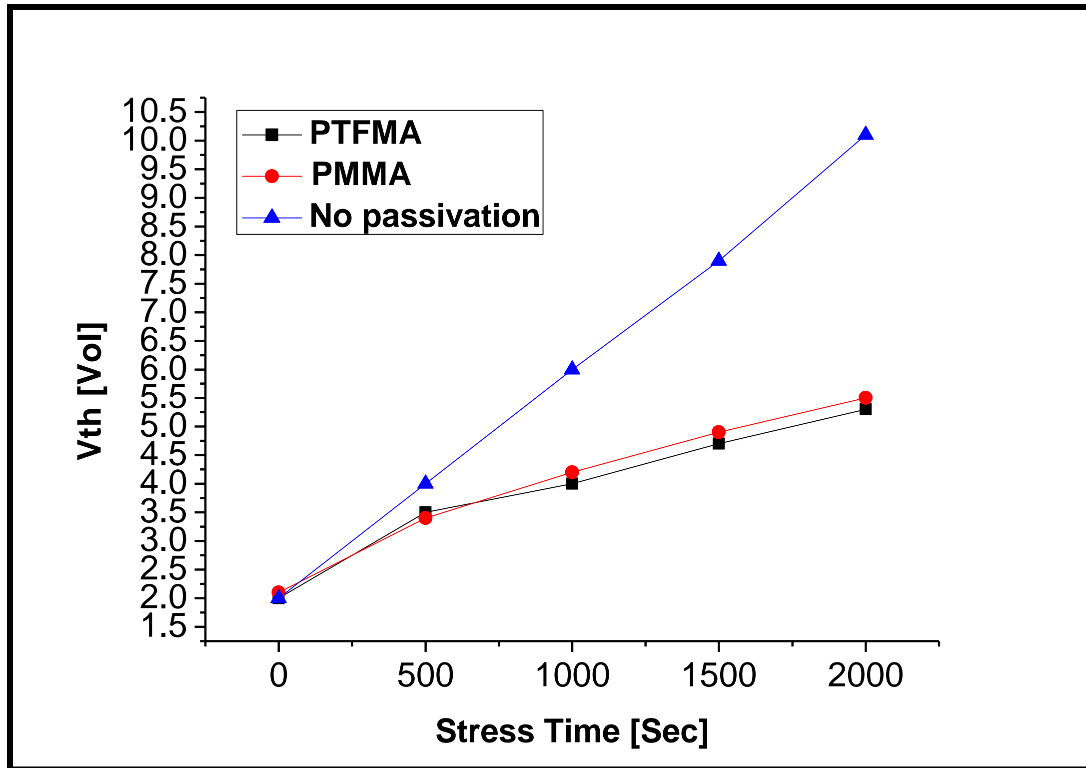


Fig. 4-17 a-IGZO devices V_{Th} versus stress time including the without, with PTFMA, and with PMMA passivation layer

4.6 Color filters functional organic passivation layer

The polymer dielectric materials served not only as insulator for TFTs, but also as color filters for LCDs [25] or colorful electrophoresis paper (E-paper) [26], schematically shown in Figs. 4-19, and 4-20, respectively. This work represents one potential example for multifunctional passivation layer. Further, since color filters significantly contribute to the bulk of material cost, integrating color filters and passivation layer is also an effective method for reducing the

overall cost of LCDs or colorful E-paper. Therefore, colored PMMA was utilized [25]; the photo of colored passivation was shown in Fig. 4-21. The corresponding 1931 CIE coordinates was shown in Fig. 4-22, which were (0.64, 0.34), (0.36, 0.54), and (0.14, 0.15) for red, green, and blue devices, respectively, covering 49% National Television Systems Committee (NTSC) standard. Conventional color filter is about 72% NTCS, 49% is not enough for LCD applications. However, the color gamut can be improved by increasing the thickness of passivation or purify the material. Our work provides a possibility for multifunctional colored passivation layer.

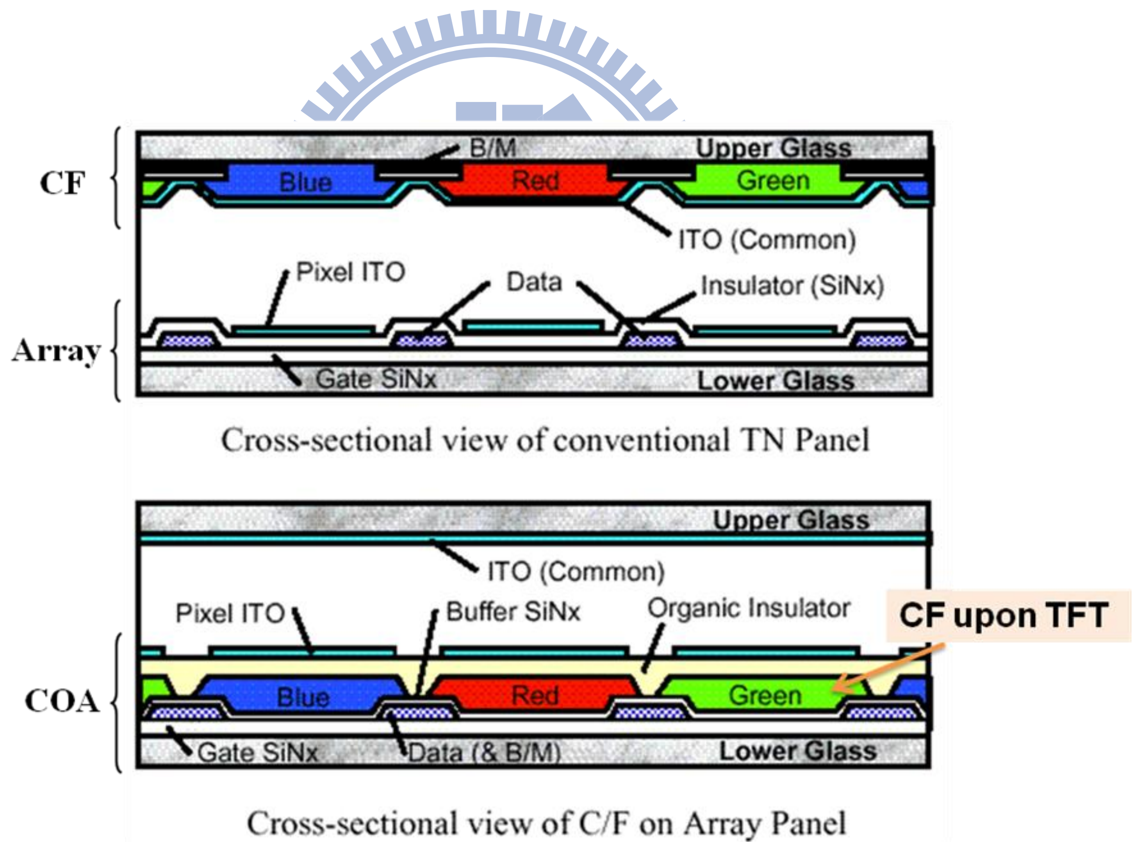


Fig. 4-18 Schematic color filters on active matrix arrays

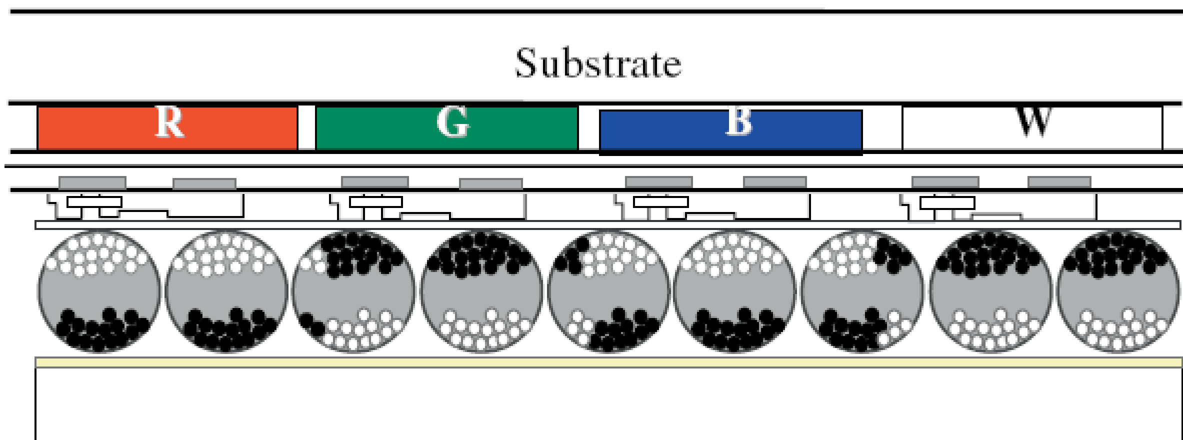


Fig. 4-19 Schematic cross-sectional view of colorful E-paper

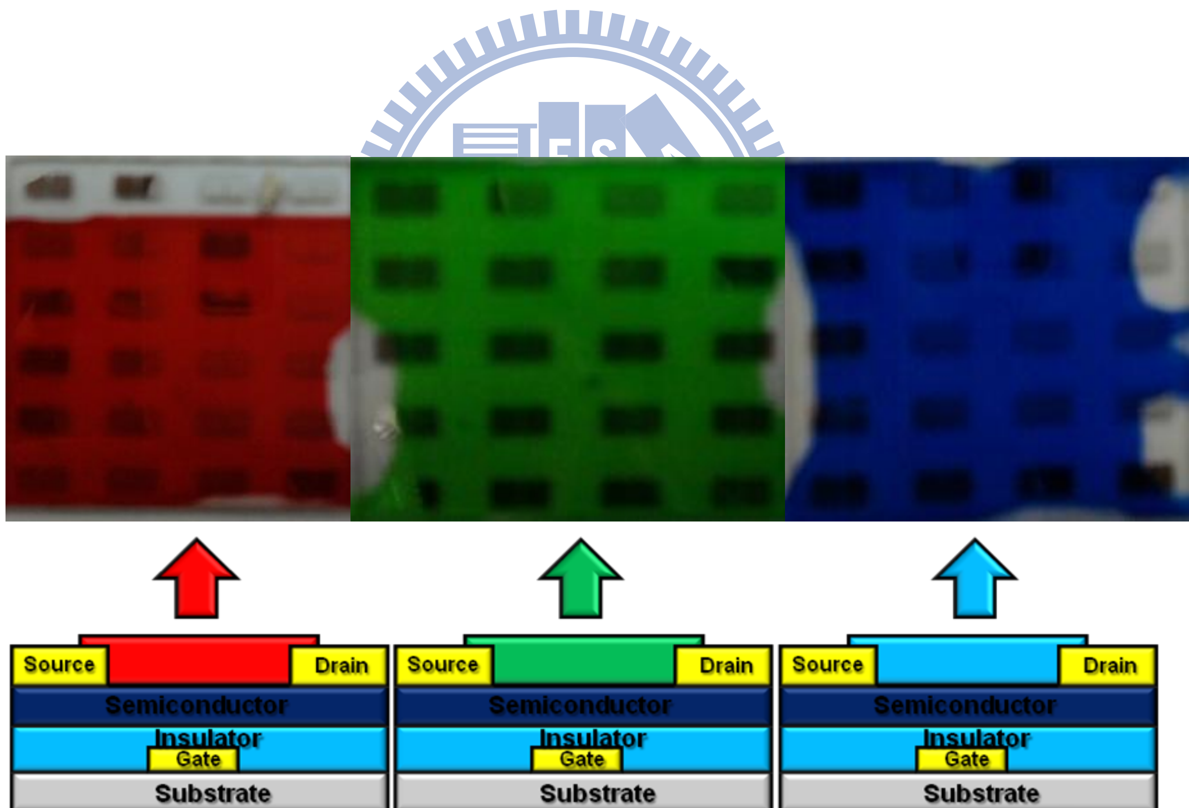


Fig. 4-20 A real picture in full-colored colorful organic passivation layer

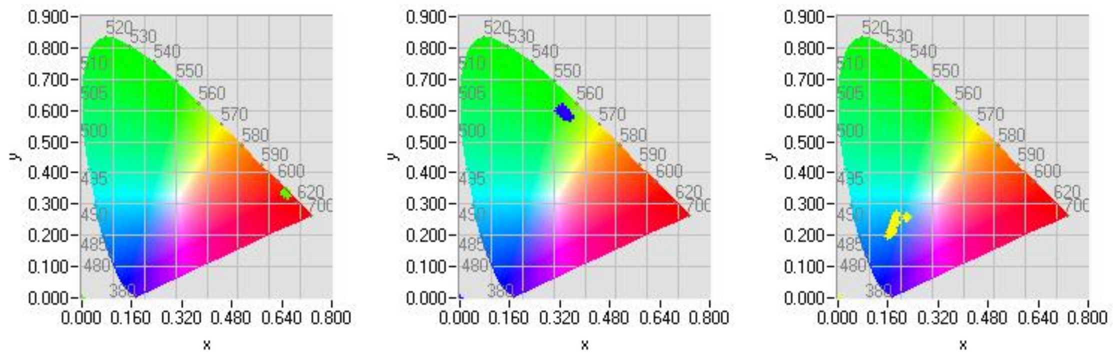


Fig. 4-21 Chromaticities of red, green, and blue 1931 CIE coordinates

4.7 Summary

The a-IGZO deposition damage in back channel can be suppressed by using the organic passivation layer. Because PTFMA has a weaker electron donor-like effect, the device reveals a 2.3V V_{Th} shift (The PMMA device shows 6.4V shift). Hence, PTMA shows better passivation characteristics. Furthermore, organic passivation can also protect the a-IGZO devices from oxygen and moisture in ambience, s.s., μ_{sat}, and I_{on}/I_{off} change only slightly even storage in ambience for 24 days.

For AMOLED applications, the a-IGZO devices stability under DC stress was evaluated. The stress condition is V_{GS}=20V and stress time = 2000 s. The devices after stress, shows 3V V_{Th} shift. Actually, it was poor than inorganic passivation. Therefore, single organic passivation may not suit to AMOLED display, but organic passivation still provides a possibility of low back channel damage. Finally, for the reason of cost and higher aperture ratio, colorful

organic material was integrated into the passivation layer. The devices show about 49% NTSC standard.

Chapter 5

Conclusions and Future works

5.1 Conclusions

In this study, we reduced a-IGZO device back channel damage by using PTFMA and PMMA. PTFMA is suitable for passivation layer material, because it has weaker electron donor-like effect, high material density, and high water contact angle. For long term stability, PTFMA is very stable in ambience after 24 days, with slight change in μ_{sat}, s.s., and I_{on}/I_{of}. Although an organic passivation layer revealed poor DC bias voltage stress stability, it still provides potential for lowering deposition damage. Finally, the organic passivation layer provides an alternative approach to integrate passviation layer and color filters in LCDs. Overall organic passivation revealed high potential for producing a printable, low process energy, and functional color filter. Combining these merits, organic passivation layer can further reduce the equipment and material cost. Comparisons in organic and inorganic passivation layer are shown in Table. 5-1

Table 5-1 Comparisons with organic and inorganic passivation layer

Passivation	Sputtering SiO_2	PECVD SiO_2	Spin PTFMA
Ref.	J.D.T., Vol. 5, NO. 12, (2009)	Thin Solid Films, 517 6341-6344, (2009)	NCTU'10
Process	Complicated	Complicated	Easy
Deposition damage	△	△	◎
Ambient Stability	◎	◎	○
Stress stability	◎	◎	△
Integration of color filter	×	×	○

◎: Excellent ; ○: Good; △:Acceptable; ×: Poor

5.2 Future work

The a-IGZO was found to be a highly visible light transparent [26], however, the photosensitivity will cause the a-IGZO device unstable. Because the wavelength dependent a-IGZO TFTs photosensitivity under broad-band illumination (365~660nm) and found that the a-IGZO TFT is stable under visible light (460~660nm) (Fig. 5-1). Under UV illumination (<400nm), TFT off state drain current increases and the change is consistent with the Tauc gap of the a-IGZO [27], shown in Fig. 5-2.

Therefore, we proposed a color filter passviation layer to solve the photosensitivity issue. Because the color filter only allowed specific wavelength to pass, the optical properties of red, green, and blue color filter passivation layer were shown in Fig. 5-3. The 400nm transmittances in red, green, and blue colored passivaiton are 30, 5, and 40%, respectively. Colored passivation can filter the light in UV range (<400nm), it can be expected to suppress the phenomenon of photosensitivity.

However, the UV light transmittance is totally different in red, green, and blue colored passivation that might cause the different photosensitivity phenomenon. Hence we have to further consider that the relationship between the thickness of colored passivation layer and photosensitivity, because thickness will directly affect the optical spectrum of colored passivation. Ideally, the UV light region transmittance in red, green, and blue should be as same as possible (considering the uniformity of photosensitivity); it will produce the different off current state and V_{Th} in red, green, and blue pixel respectively. Overall the colored passivation is a good topic in photosensitivity.

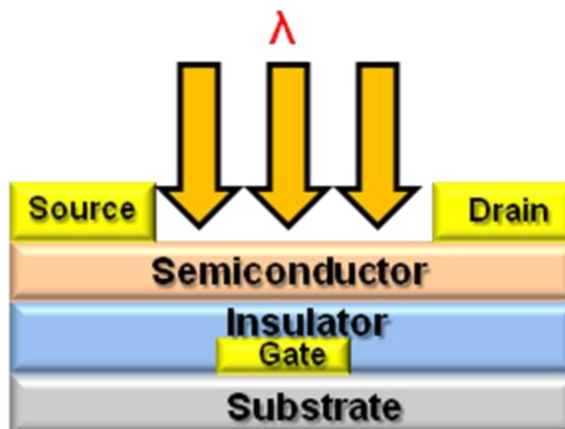


Fig. 5-1 Schematic of the a-IGZO device under illumination

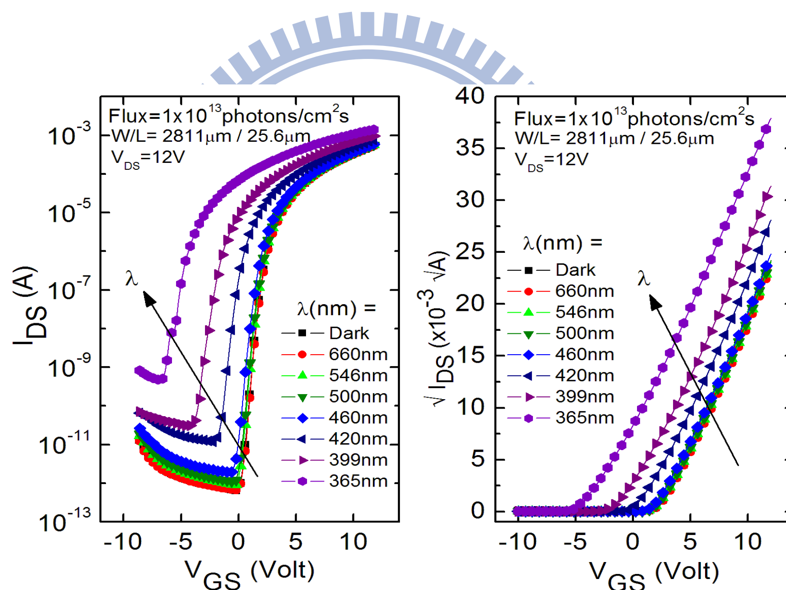


Fig. 5-2 I_D-V_{GS} curves for constant photo flux with the varying light wavelength

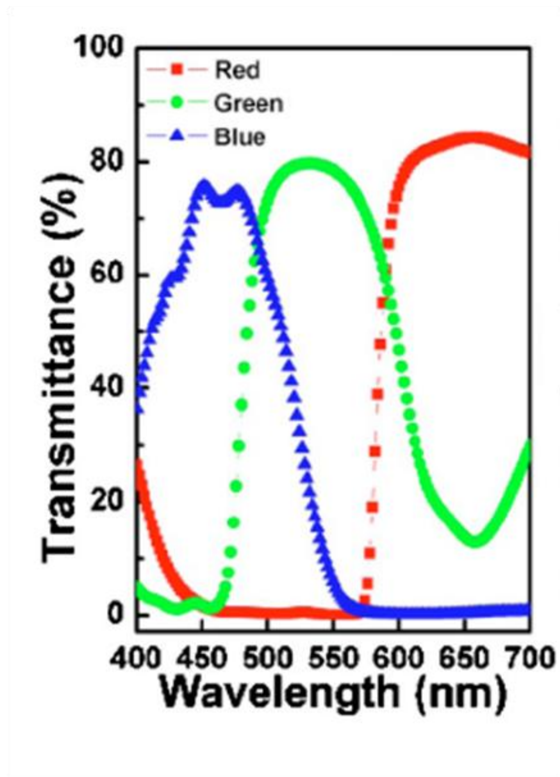


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Fig. 5-3 Color filter passivation optical properties of red, green, and blue

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