國立交通大學

顯示科技研究所

碩士論文

矽光伏特材料於低溫薄膜電晶體之應用

Application of photovoltaic silicon materials in low temperature thin film transistor

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中 華 民 國 九 十 九 年 七 月

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碩士論文

A Thesis
Submitted to the Display Institute
Collage of Electrical Engineering and Computer Science
National Chiao Tung University
in Partial Fulfillment of the Requirements
for the Degree of Master
in
Electro-Optical Engineering

July 2010
Hsinchu, Taiwan

中華民國九十九年七月

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摘要

大面積軟性電路展現新型態的電子裝置，快速的崛起在顯示、感應裝置、生醫及其他領域。除此之外軟性電子元件更具備許多優點，輕量化、可饒式、耐用、可以因應更多自由的設計。因爲氫化非晶矽薄膜電晶體的成熟的低溫製程，現階段是最常被使用在液晶顯示器以及軟性電子，然而最大的缺點便是較低的電子遷移率、不穩定性以及較高的驅動電壓。近來研究發展顯示奈米或稱微晶矽的材料是具有取代氫化非晶矽成爲新一代軟性電子及大面積電子元件潛力

本篇論文中，利用高密度電漿化學氣相沉積系統及熱燈絲化學氣相沉積系統在低溫 200℃ 下沉積出高結晶性的氫化微晶矽薄膜以及低電阻率的 n 型氫化微晶矽薄膜，並且藉由 XRD 及 SEM 確認氫化微晶矽薄膜，確認晶粒大小約 100nm 等同於一般非晶矽藉由固相結晶法(Solid Phase Crystallization) 600℃退火 24 小時的結晶性。使用簡單的自我對準式薄膜電晶體，藉由場效傳導法(Field Effect Conductance)取出缺陷密度(Density of states)從中了解不同結晶度對於缺陷密度分布之影響。最後將低缺陷密度之氫化微晶矽及 n 型氫化微晶矽薄膜整合成功的製作出不需離子佈植、低成本、低溫、高結晶性的薄膜電晶體，開與關的電流差距超過 10^5、開關速度達到 S=100 mV/decade，並且電子遷移率達到 50 cm^2/V-s 展現出極高的潛力應用於軟性電子元件。

Application of photovoltaic silicon materials in low temperature thin film transistor

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Abstract

Flexible, large area circuits exhibit a new form of electronics which have led to rapidly rising and promising applications in displays, sensors, medical devices and other areas. Besides flexible electronics on plastic substrates possess advantageous characteristics, being lightweight, flexible, and have the capacity to be manufactured in a variety of shapes, which leads to freedom of design. Currently, a-Si:H TFTs are used in AMLCD and compatible with flexible substrate due to low temperature process. However, low device mobility, higher drive voltage and electrical instability are the main disadvantages of a-Si TFT. Recent developments reveal that micro- or nanocrystalline silicon is a promising alternative for flexible display and large area electronic applications. The charge carrier mobility exceeds the mobility of amorphous silicon significantly and compatible with flexible substrate.

In this thesis, a high quality and low resistivity of intrinsic and n-type microcrystalline silicon films were developed at low temperature 200^{o}C by High Density Plasma chemical vapor deposition system and Hot-Wire chemical vapor deposition system. First μc-Si:H film was analyzed by XRD and SEM. And the μc-Si:H with a grain sizes of ~50-100 nm was recognized.

The grain size is the same with conventional SPC(600℃ annealing 24hours) method. A self-aligned TFTs was demonstrated. After that, the density of state distribution was extracted from TFTs by FEC method. With these results we can understand the different crystallinity on the effect of defect density distribution. Finally a top-gate microcrystalline TFTs without S/D implantation was demonstrated. A high electron mobility exceeding 50 $cm^2/V\text{-}s$, low subthreshold swing 0.1-0.3 V/decade and high current ON/OFF ratios more than 10^5 was obtained. It shows highly potential in flexible electronics application.

誌謝

本論文能夠順利完成，首先要感謝我的指導老師黃中垚教授及謝嘉民教授，使我在兩年的研究所學習生涯中，得以培養出獨立研究的能力。特別感謝國家奈米元件實驗室謝嘉民博士給予我細心的指導與鼓勵，讓我知道實驗的方向及效率是影響成果優劣的最重要因素。其次，也要謝謝郭浩中教授及沈昌宏博士及戴寶通博士擔任我的口試委員，提供我不少的寶貴意見。

感謝奈米元件實驗室工程師游文謙、王昭凱、黃文賢大哥們以及彥佑、耿正在實驗上對我的指導及實驗儀器上的幫助，你們的經驗與指教幫助我度過不少難關。感謝博士班學長們，宥浦學長在機台以及材料上提供許多的寶貴經驗與意見、建華學長的機台使用經驗、小閩學長、尚融學長的討論與指教，你們的指點幫忙讓我的研究更加順利。感謝和我共同奮鬥的同學們:泓瑜、育新、智維、國欽、舒純真的很慶幸能遇見你們這群可愛的朋友，有你們的陪伴，兩年的生活更加多采多姿。也謝謝所有學弟妹默默地付出，使我能順利的完成研究。祝福你們未來的實驗順利。

最後，謹將本論文獻給我的父母。謝謝他們辛苦的支持與不斷的鼓勵，使我能順利完成學位。

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Chapter 1 Introduction

1.1 The general background and motivation

Thin-film transistors (TFT), which use a thin semiconductor film on an insulating substrate as the active channel, was first demonstrated in 1961 by Dr. P. K. Weimer. However the first TFT used CdSe as the active device channel, not now commonly used amorphous Si(a-Si). Until 1979 the first amorphous Si TFT was demonstrated by P. G. le Comber , W. E. Spear. With its simplicity in structure and fabrication, applications of thin-film transistors in image sensors and displays become more and more popular. But for now the great demand information and desire high resolution displays has stimulated higher interest in poly-Si TFT. This is due to a much higher mobility and drive current of poly-Si TFTs, compared to amorphous Si counterparts, which enables the integration of peripheral circuits on the same panel in active matrix liquid crystal displays (AMLCD) manufacturing [1][2].

Generally, AMLCDs used a-Si TFTs as a switching element to control the gray level in liquid crystal display(LCD) [5] In AMLCDs, TFTs play as switching device to turn ON/OFF the current path for charging/discharging the liquid crystal capacitor. However, a-Si TFTs has poor effect field mobility (0.5-1 cm2/V-s) and higher turned on voltage. In order to improve the TFTs performance, the poly-Si TFT was developed in 1980 by S.W. Depp and A. Juliana. The undoped poly-Si was deposited by low-pressure CVD at 625 ^{O}C, and the films were approximately 0.75 m thick.[3] The major advantage of polycrystalline silicon poly-Si TFT technology is its suitability for multifunctional active-matrix displays, because it enables the integration of driver electronics, sensors, memories, and peripheral circuits on the glass substrate to produce system-on-glass SOG displays. But the temperature in the

process is too high to use on glass. Therefore in 1991 T.W. Little and K. Takahara developed low-temperature ($T \leqq 600\ ^{o}C$) polycrystalline silicon thin film transistor (poly-Si TFTs) which was fabricated by solid phase crystallization (SPC) of amorphous silicon(a-Si).[4]

Over the years, amorphous, polycrystalline, and recently, nano/microcrystalline forms of silicon have gained prominence as low temperature alternatives to crystalline silicon for large-area applications. Amorphous silicon is the current material for most of the thin film transistors used in liquid crystal displays, and a host of other applications. It is a versatile material for limited mobility applications, and can be reliably grown at very low temperatures, but suffers from bias stress and light induced degradation. Polycrystalline silicon on the other hand has much higher mobilities, and hence suitable for high-speed CMOS applications. But it requires processing at much higher temperatures, which is out of scope of inexpensive plastic substrates. Although methods of converting amorphous silicon to polycrystalline silicon exist by laser induced crystallization, it suffers from problems of device uniformity besides being expensive.

For this reason we have been pursuing thin-film transistor technology based on nano/microcrystalline silicon, nc-Si:H/μc-Si:H as an inexpensive alternative. This semiconductor can provide sufficient electron mobility [5–7].Moreover, it can be fabricated at low temperatures which are compatible with the plastic substrates [7]. The table 1. summarizes the low-temperature silicon processes prevalent at present. Although amorphous silicon-based TFTs are currently used in addressing the pixels of AMLCD. The material is deposited at low temperature compatible with the use of plastics. However, the low field effect mobility in these TFTs limits the panel size.[8] Then, TFTs with higher mobility are needed. Nano/Microcrystalline silicon (nc-Si) is now the main candidate to reach this goal. It can be deposited by different techniques

at low temperature compatible with the use of plastics substrates. In this thesis, a-Si:H TFTs and nc-Si:H/μc-Si:H TFTs were demonstrated under low temperature(T≦200 ^{o}C) by HWCVD and HDPCVD.

Table 1. Status of silicon materials for TFTs [10]

Attribute	a-Si:H	nc-Si:H	μc-Si
Standard deposition T (°C)	250	250	150 (precursor)
Highest T process/material (°C)	350 SiN_x	280 n^+, p^+	Laser μc-Si
Lowest reported process T (°C)	110	150	Laser
Electron mobility ($cm^2 V^{-1} s^{-1}$)	0.5–1	40	300
Hole μ ($cm^2 V^{-1} s^{-1}$)	~0.01	0.2	50
Conductivity ($S cm^{-1}$)	10^{-11}	10^{-7}–10^{-2}	10^{-6}
Growth rate ($nm s^{-1}$)	0.1–1	0.1	0.1–1
Gate and source/drain geometry	Bottom Staggered	Top Coplanar or staggered	Top Coplanar
Gate insulator	SiN_x	SiO_2	SiO_2

1.2 TFT Structures

The thin-film transistor usually refers to MOSFET as opposed to other kinds of transistors. The structure is similar to MOSFET. It can be roughly classified into top-gate and bottom-gate types depending upon the placement of the gate dielectric relative to the channel material. In bottom-gate (inverted) devices, the gate dielectric is below the active layer, while in top-gate devices the gate dielectric layer is above the active layer similar to conventional MOSFETS. These can be further classified into coplanar and staggered types depending upon the location of the source and drain contacts relative to the gate. In coplanar TFTs, the source and drain contacts are on the same side of the active region as the gate contact, whereas in staggered structures, the source and drain contacts are on the opposite side of the active region as compared to the gate contact. These device geometries are schematically described in the **Fig. 1.** The inverted staggered in currently industry is most commonly used structure for a-Si:H TFT. One of the most important reasons for this is that silicon nitride forms an excellent gate dielectric with amorphous silicon which is currently the material of choice owing to low cost and low temperature fabrication. In this thesis a top-gate

structure was used to take advantage of the highly crystalline top surface of the film.[11-14].

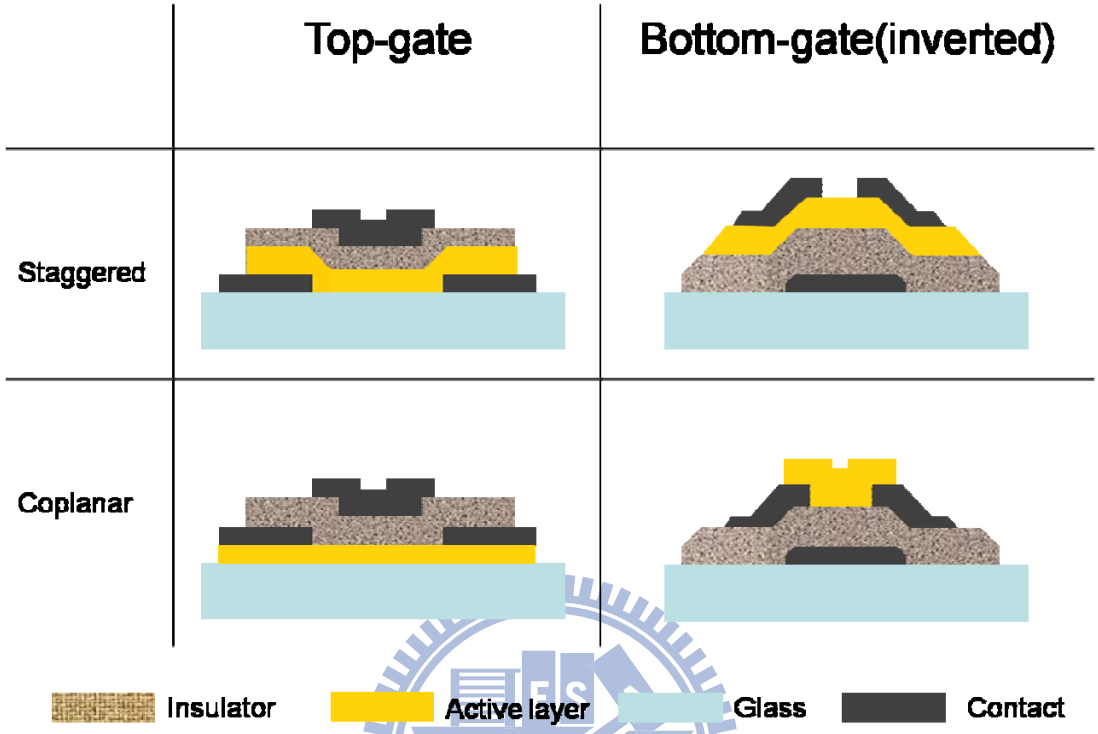


Fig. 1 Schematic of commonly used TFT structures

Chapter 2 Material Characterization

2.1 Introduction of amorphous and microcrystalline silicon

In crystalline silicon, the silicon atoms are covalently bonded with four neighbors in tetrahedral directions. The bond of bonding states (valance band) is completely occupied with electrons, and the antibonding bond (conduction band) is empty. Electrons can cross the energy gap by thermal or optical excitation. Impurity introduced states within the gap, such as boron or phosphorous, govern the electronic properties.

In amorphous silicon the conduction and valance bands have tails of states due to fluctuations of the bond lengths and bond angles in the silicon matrix. These states are modified band states. They can be divided into localized and extended states. Charge carriers in localized states have near zero mobility. Extended states provide a finite mobility to carriers, and they are separated from localized states by a conceptual mobility edge, which defines a mobility gap. In brief, the amorphous semiconductors are noncrystalline, and they lack long-range periodic ordering of their constituent atoms. But they do have a local order on the atomic scale. This short-range order is directly responsible for observable semiconductor properties such as optical absorption edges and activated electrical conductivities.

Polycrystalline semiconductors are composed of grains, with each grain containing a periodic array of atoms surrounded by a layer of interconnective or boundary atoms. For progressively smaller grains, such as microcrystallites, the surface layer of each grain contains progressively larger numbers of interconnective randomly distributed atoms relative to the periodically arrayed interior atoms. Consequently, a semiconductor containing a larger number of very small grains

embedded in the amorphous phase of the material is called the microcrystalline (or noncrystalline) semiconductor. The microcrystalline semiconductors lie on the borderline between the amorphous and polycrystalline phases, and the difference between polycrystalline and microcrystalline semiconductors is the content of the amorphous phase. The relative amount of crystalline phase contained in the film is described by the crystalline volume fraction, which can vary from a few percent up to 80 or 90% in fully crystallized samples. In general, in polycrystalline semiconductors, the content of the amorphous phase is negligible and is mainly located at the grain boundaries, and in microcrystalline semiconductors the content of the amorphous phase is variable. If the volume fraction of the amorphous phase is not negligible, the device electronic properties can still be dominated by the amorphous phase [1].

2.2 Growth mechanisms of microcrystalline silicon thin films

Microcrystalline silicon μc-Si:H consists of silicon crystallites, amorphous phases, and voids.[2] The microstructure of microcrystalline silicon can be controlled from highly crystalline to a material where amorphous growth prevails **Fig. 2**[3]

It is well known that high hydrogen (H_2) dilution in a silane (SiH_4) plasma can induce a microstructural change from amorphous to ordered structures even at low temperatures,300 °C,[4],[5] This behavior can be also observed in Hot-wire chemical-vapor deposition system.[6] There are three primary model to understand the formation of uc-Si:H films at low temperatures (100-350 ℃) for PECVD.

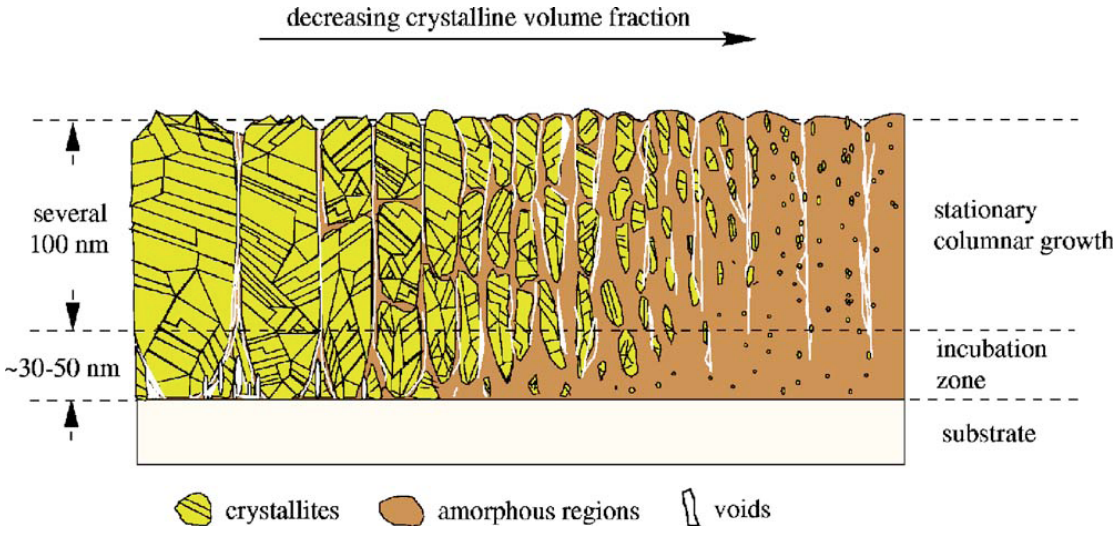


Fig. 2 Microstructure of microcrystalline silicon as a function of the crystalline volume fraction.

I. **Surface diffusion model:**

This model was proposal to explain the relationship between crystalline volume fraction in the resulting uc-Si:H films and substrate temperature during growth of the films. Sufficient flux density of atomic hydrogen from hydrogen diluted silane plasma realizes a full surface coverage by bonded hydrogen and also produces local heating through hydrogen-recombination reactions on the growth surface of the film. These two events occurring on the surface enhance the surface diffusion length of film

precursor (SiH3). As a consequence, film precursors adsorbed on the surface can find energetically stable sites, leading to a formation of atomically flat surface. At first, uc nucleus is formed. After the formation of nucleus, epitaxial like crystal growth takes place with a similarly enhanced diffusion of film precursors [7, 8].

II. **Etching model:**

This model was proposed based on the experimental fact that film growth rate is reduced by an increase of hydrogen dilution. An atomic hydrogen provided on the film-growing surface breaks Si-Si bonds, preferentially the weak bond, involved in the amorphous network structure, leading to a removal of a Si atom bonded more weakly to another Si. This site is replaced by a new film precursor, forming a rigid and strong Si-Si bond [9, 10].

III. **Chemical annealing model:**

The model was proposed for explaining the experimental fact that crystalline formation is observed during hydrogen plasma treatment in a layer-by layer growth by an alternating sequence of amorphous film growth and hydrogen plasma treatment. During the hydrogen plasma treatment, many hydrogen atoms are permeating in the sub-surface region, giving rise to a crystallization of amorphous network through the formation of a flexible network with a sufficient amount of atomic hydrogen in the sub-surface region without any removal process of Si atoms [11].

2.3 Electronic properties of amorphous silicon (a-Si:H) and microcrystalline silicon (uc-Si:H)

The electronic properties of the amorphous silicon(a-Si:H) and microcrystalline silicon (uc-Si:H) depend sensitively on the density and energy distribution N(E) of the localized gap states. And these states determine the doping efficiency, transport, and recombination, as well as the width and the potential profile of space charge layers in devices. **Fig. 3** shows a model of this density of states distribution including both intrinsic and extrinsic defect states. Tails of localized states extend from both bands deep into the gap. And these states are believed to arise from potential fluctuation due to the disorder. In addition to these tail states, one excepts to discover states in the gap from specific defects. Such defects will be formed in random network structure in order to release internal tension, but they may also arise from unfavorable deposition conditions. The simplest intrinsic defect is an unsaturated bond-the so-called "dangling" bond-the neutral state of which is located around midgap in undoped material; however, in principle, there can also be more complicated defects that act as deep centers. Both the concentration and energy distribution of these states are determined by the position of the Fermi level. In undoped a-Si:H, the concentration of these defects can be as lower as $10^{15}cm^{-3}$. Due to the low density of gap states, the Fermi level in such films can easily be moved by doping, illumination, or external bias to a space charge layer.

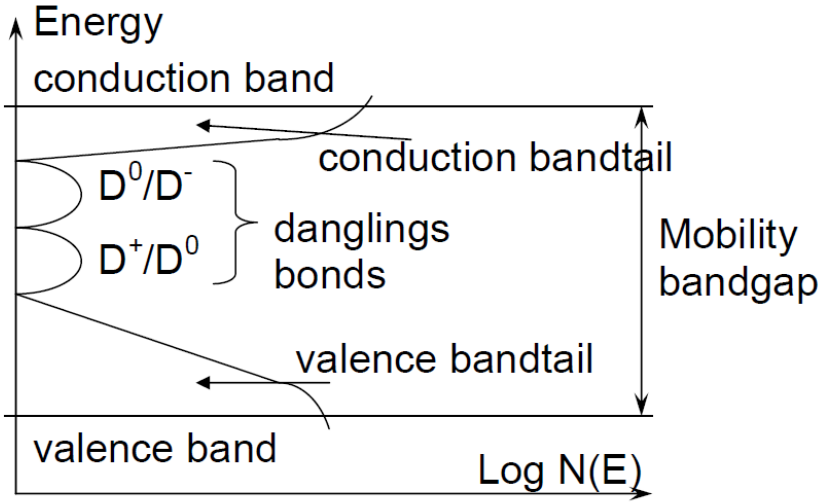


Fig. 3 The standard model for density of states in a-Si:H.

2.4 Density of states extraction using FEC method

As mentioned in section **2.3** , the electronic properties is strongly affected by density and energy distribution N(E) of the localized gap states. So the defects in the active channel plays an important role on the performance of TFTs. In this section, we will introduce the field effect conductance(FEC) method to extract density of states distribution from TFTs.

Fortunato et al. had been proposed that poly-Si can be modeled using the "effective-medium" approach, in which the effects of grain boundary defects and intragranular defects are assumed to be uniformly distributed throughout the material [12].This indicates that a model based on a spatially uniform distribution of gap states, such as those developed for amorphous-Si, constitutes a good and reasonable approximation[13]-[14].

2.4.1Determination of flat-band voltage

The temperature method that is based on the temperature dependence of $\partial G/\partial V_G$ is used to calculate flat-band voltage. The equation is expressed by Weisfield and Anderson [15]:

$$\frac{\partial \log G}{\partial V_G} \cong \frac{\varepsilon_{ox}}{t_{ox}} \cdot \frac{1}{qkTN_0}\left[1+\frac{1}{2}\left(\frac{q\psi_S}{KT}\right)+O\left(\frac{q\psi_S}{KT}\right)^2 \cdots\right]$$

The flat-band voltage (V_{FB}) can be determined as the gate voltage where

$T\cdot(\partial \log G/\partial V_G)$ is temperature independent.

2.4.2Current-voltage and surface band-bending

The incremental method [16] is utilized to establish the relationship between surface band-bending and current-voltage (I_d-V_g) characteristics. The field conductance is defined as [17]:

$$G = G_0 - \frac{G_0}{d}\int_0^{\psi_s}\frac{\exp(q\psi/KT)-1}{\partial\psi/\partial x}\partial\psi \qquad \text{Eq.2-1}$$

Where G_0 stands for the conductance for the flat band condition and d is the thickness of poly-Si film. The electric field of the semiconductor surface can be given from the voltage drop at the surface:

$$\left.\frac{\partial\psi_S}{\partial x}\right|_{x=0} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{d}{t_{ox}} = -\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_G - V_{FB} - \psi_S}{t_{ox}} \qquad \text{Eq.2-2}$$

Differentiating Eq. 3-6 and immediately substituting the Eq.2-2 into the result, the followingequation can be expressed:

$$\left.\frac{\partial\psi}{\partial G}\right| = \frac{1}{G_0}\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{d}{t_{ox}}\cdot\frac{V_G - V_{FB} - \psi_S}{\exp(q\psi_s/KT)-1} \qquad \text{Eq.2-3}$$

Substituting the field conductance into the drain current in Eq. 2-4 and the relationship between surface band-bending and current-voltage shows in Eq. 3-9 can be obtained by rewriting Eq. 2-3:

$$\frac{G_{i+1} - G_i}{G_0} = \frac{I_{D,i+1} - I_{D.i}}{I_{D,0}} \qquad \text{Eq.2-4}$$

$$\psi_{s,i+1} = \psi_{s,i} + \frac{I_{D,i+1} - I_{D,i}}{I_{D,\,flatband}}\cdot\frac{d}{t_{ox}}\cdot\frac{\varepsilon_{ox}}{\varepsilon_{Si}}\cdot\frac{V_{G,i} - V_{FB} - \psi_{s,i}}{\exp(q\psi_s/KT)-1} \qquad \text{Eq.2-5}$$

Placing the initial condition that $\psi_{s,i} = 0$, we can calculate $\psi_{s,i}...\psi_{s,N}$ for $V_{G,1}...V_{G,N}$.

2.4.3Density of states (DOS) extracted from the band bending

The band bending is a solution of the one-dimensional Poisson's equation:

$$\frac{\partial^2 \psi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_{Si}} \qquad \text{Eq.2-6}$$

Where ε_{Si} is the poly-Si dielectric constant and ρ(x) is the local space-charge density. For gate voltage below threshold, the free-carrier concentration can be neglected and sufficiently low temperatures:

$$\rho(x) = -q\int_{E_F}^{E_F+q\psi} N_g(E)\partial E \qquad \text{Eq.2-7}$$

where $N_g(E)$ is the average gap state density. After multiplying by $2\partial\phi/\partial x$ and integrating from x=0 to x=d (oxide-semiconductor interface to bottom of channel),

$$\left(\left.\frac{\partial \psi}{\partial x}\right|_{x=0}\right)^2 = \frac{2q}{\varepsilon_{Si}}\int_0^{\psi_S} \partial\psi_s' \int_{E_F}^{E_F+q\psi} N_g(E)\partial E \qquad \text{Eq.2-8}$$

Where is the band bending at x=0. The density of state is expressed by

$$N_g(E_F+\psi_S) = \frac{\varepsilon_{Si}}{2q}\frac{\partial^2}{\partial \psi_s^2}\left(\left.\frac{\partial \psi}{\partial x}\right|_{x=0}\right)^2 \qquad \text{Eq.2-9}$$

where E_F, ϕ_S, ε_{Si} are Fermi energy, surface band bending at poly-Si film/gate-oxide interface, and dielectric constant of silicon, respectively.

Chapter 3 Experimental Details

In this chapter, there are two difference processes to demonstrate TFTs. The main purpose of the first process is to verify material properties of microcrystalline silicon active layer. Then the high performance TFTs was demonstrated by the second process with source and drain in-situ dopant.

3.1 Measurement system setup

The system we used to measure the high ferquence capacitance is **Bias Temperature Stress measurement system (BTS):** Keithley 590 CV analyzer 、Keithley 595 Quasistatic CV meter、Keithley 230 programmable voltage source、Keithley 5951 remote input coupler and computer with ICS software installed and the I-V measurement we used HP 4156A. **Fig. 4** shows the schematic diagram of C-V measurement system.

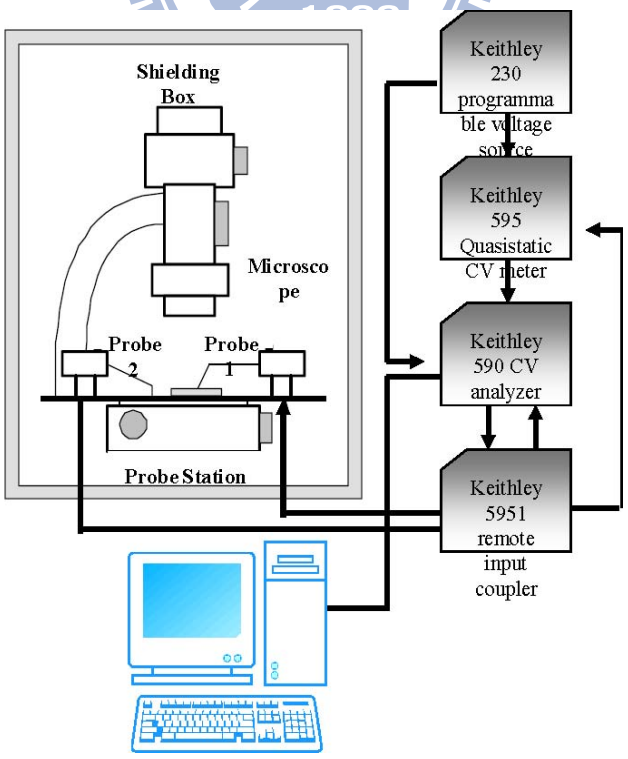


Fig. 4 Schematic diagram of C-V measurement system.

3.2 Capacitance fabrication

Current-voltage (I-V), capacitance-voltage (C-V) characteristics of SiO2 films were studied using a metal-oxide-semiconductor (MOS) capacitor structure. First the RCA clean was using for the removal of organic, metallic, and particulate contamination on the wafer surfaces. Then metal-oxide-semiconductor (MOS) structure with a Al/SiO2 stack on a p-type silicon substrate. The SiO2 was deposited using a mixture of N_2O 75sccm , SiH_4 5sccm ,Argon 75sccm at low substrate temperature of 200℃. The top and bottom electrodes of MOS capacitor was evaporated by E-gun evaporator.

3.3 Laser-activatied amorphous silicon (a-Si:H) and microcrystalline silicon (uc-Si:H) self-aligned TFTs

- **Device fabrication flow**

The device structure and fabrication flow chart show in **Fig. 5**

Step 1 . Active region formation. (1st Mask)

Using the HWCVD or HDPCVD to deposit amorphous silicon or microcrystalline silicon as 100nm on glass substrate. Then active region were defined by lithography process , that is first Mask. After lithography process, the patterned active region by RIE etching. After active region forming, acetone solution in supersonic oscillator was used to remove photoresist.

Step 2 . Gate dielectric and Metal gate defined. (2rd Mask)

As source-drain had been formed , using the high density plasma chemical-vapor deposition system (HDPCVD) to deposited SiO_2 100nm as gate dielectric. The SiO_2 layer was deposited using mixture of SiH_4 of 5 sccm, N_2O of 75 sccm, and Argon of 25 sccm at pressure of 10mtorr and power of 300 watt, and substrate temperature 200^{O}C was used. And then aluminum 250nm was evaporated by E-gun evaporator. After aluminum evaporated, gate region was defined by lithography process named

third Mask. Next, using RIE etcher to form gate structure ,then removed photoresist by acetone solution in supersonic oscillator. And it was known as self-aligned structure.

Step 3 . S/D Implantation and Laser activation

After gate structure was formed, S/D regions were implanted with phosphorus dose of 5×10^{15} cm^{-2} at an energy 35 keV for n-type TFT and activated by laser annealing(LA) at laser power of 3.3W. S/D regions must make sure the interface between silicon and metal as ohmic contact.

Step 4 . Passivation and Contact hole defined. (3^{th} Mask)

Passivation is a process that using a certain thickness dielectric capping on the device to protect components from damage to the external environment. After gate structure was defined, SiO_2 was used as passivation layer which was deposited 500nm by HDPCVD. The third Mask was used to define contact hole in lithography process. Then contact hole structure was formed by RIE etcher. After contact hole region forming, acetone solution in supersonic oscillator was used to remove photoresist.

Step 5. Metal pads defined. (4^{th} Mask)

After contact hole was defined, evaporating aluminum 500nm to contact gate, source and drain. And the final step, metal pads was patterned by fourth mask in in lithography process. Then gate, source and drain was isolated by RIE etcher. Finally, a top gate thin film transistor was compeleted.

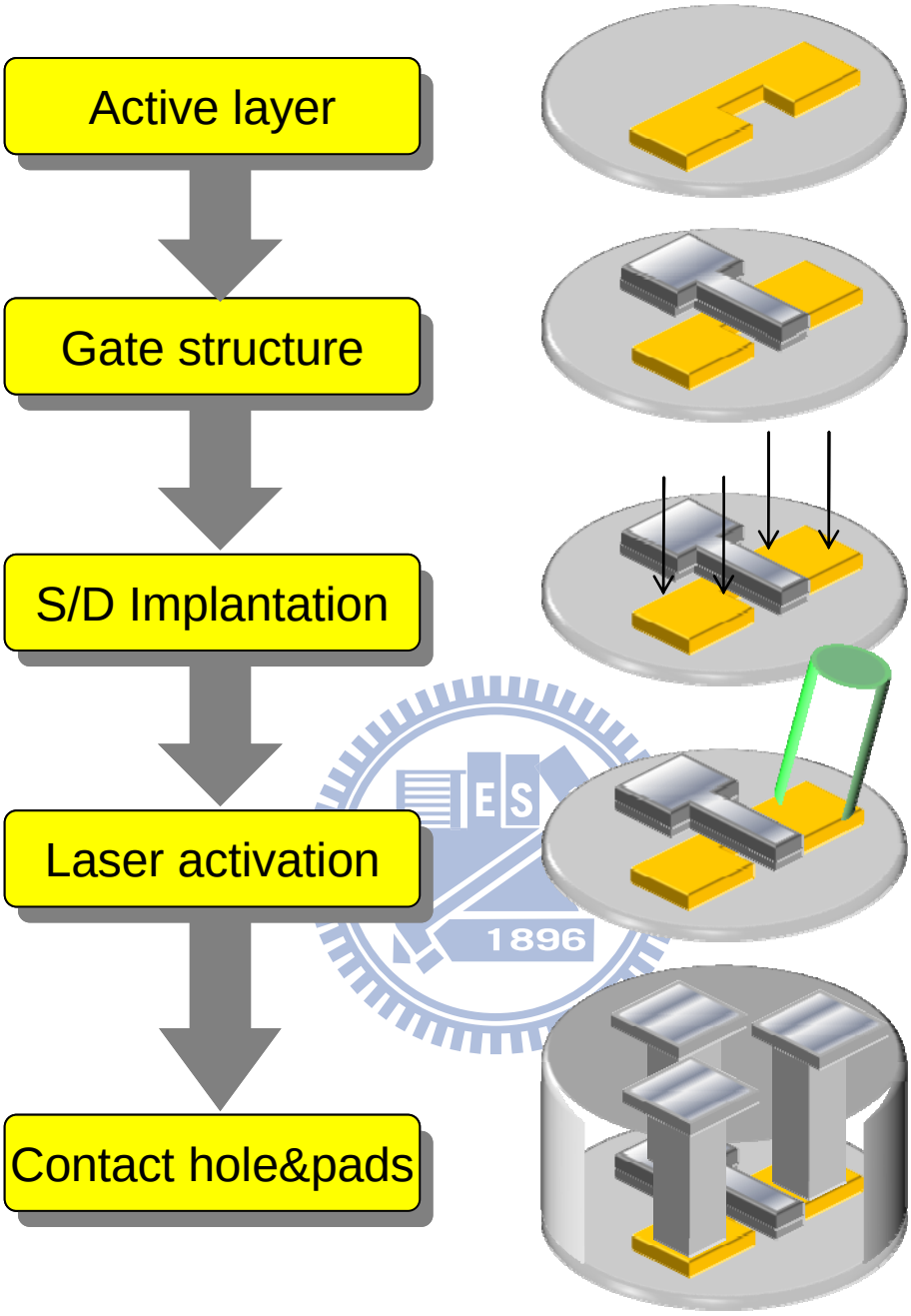


Fig. 5Laser activated self-aligned TFTs fabrication flow chart

3.4 In-situ dopant microcrystalline silicon TFTs

- **Device fabrication flow**

The device structure and fabrication flow chart show in **Fig. 6**

Step 1 . Active region formation. (1st Mask)

Using the HWCVD or HDPCVD to deposit amorphous silicon or microcrystalline silicon as 100nm on glass substrate. Then active region were defined by lithography process , that is first Mask. After lithography process, the patterned active region by RIE etching. After active region forming, acetone solution in supersonic oscillator was used to remove photoresist.

Step 2 . n+ layer formation and source-drain isolation. (2nd Mask)

As active region defined, using HWCVD to deposite n^+ nanocrystals silicon (nc-Si) layer 50nm. This layer made sure the interface between nc-Si and metal as ohmic contact. Before deposition n^+ layer, native oxide was removed by wetting BOE (1:0) 10 sec. After deposition, the source-drain isolation was defined by lithography process. Then the source-drain was patterned by RIE etching. After source-drain region forming, acetone solution in supersonic oscillator was used to remove photoresist.

Step 3 . Gate dielectric and Metal gate defined. (3rd Mask)

As source-drain had been formed , using the high density plasma chemical-vapor deposition system (HDPCVD) to deposited SiO_2 100nm as gate dielectric. The SiO_2 layer was deposited using mixture of SiH_4 of 5 sccm, N_2O of 75 sccm, and Argon of 25 sccm at pressure of 10mtorr and power of 300 watt, and substrate temperature 200^{O}C was used. And then aluminum 250nm was evaporated by E-gun evaporator. After aluminum evaporated, gate region was defined by lithography process named third Mask. Next, using RIE etcher to form gate structure ,then removed photoresist by acetone solution in supersonic oscillator.

Step 4 . Passivation and Contact hole defined. (4^{th} Mask)

Passivation is a process that using a certain thickness dielectric capping on the device to protect components from damage to the external environment. After gate structure was defined, SiO_2 was used as passivation layer which was deposited 500nm by HDPCVD. The fourth Mask was used to define contact hole in lithography process. Then contact hole structure was formed by RIE etcher. After contact hole region forming, acetone solution in supersonic oscillator was used to remove photoresist.

Step 5. Metal pads defined. (5^{th} Mask)

After contact hole was defined, evaporating aluminum 500nm to contact gate, source and drain. And the final step, metal pads was patterned by fifth mask in in lithography process. Then gate, source and drain was isolated by RIE etcher. Finally, a top gate thin film transistor was compeleted.

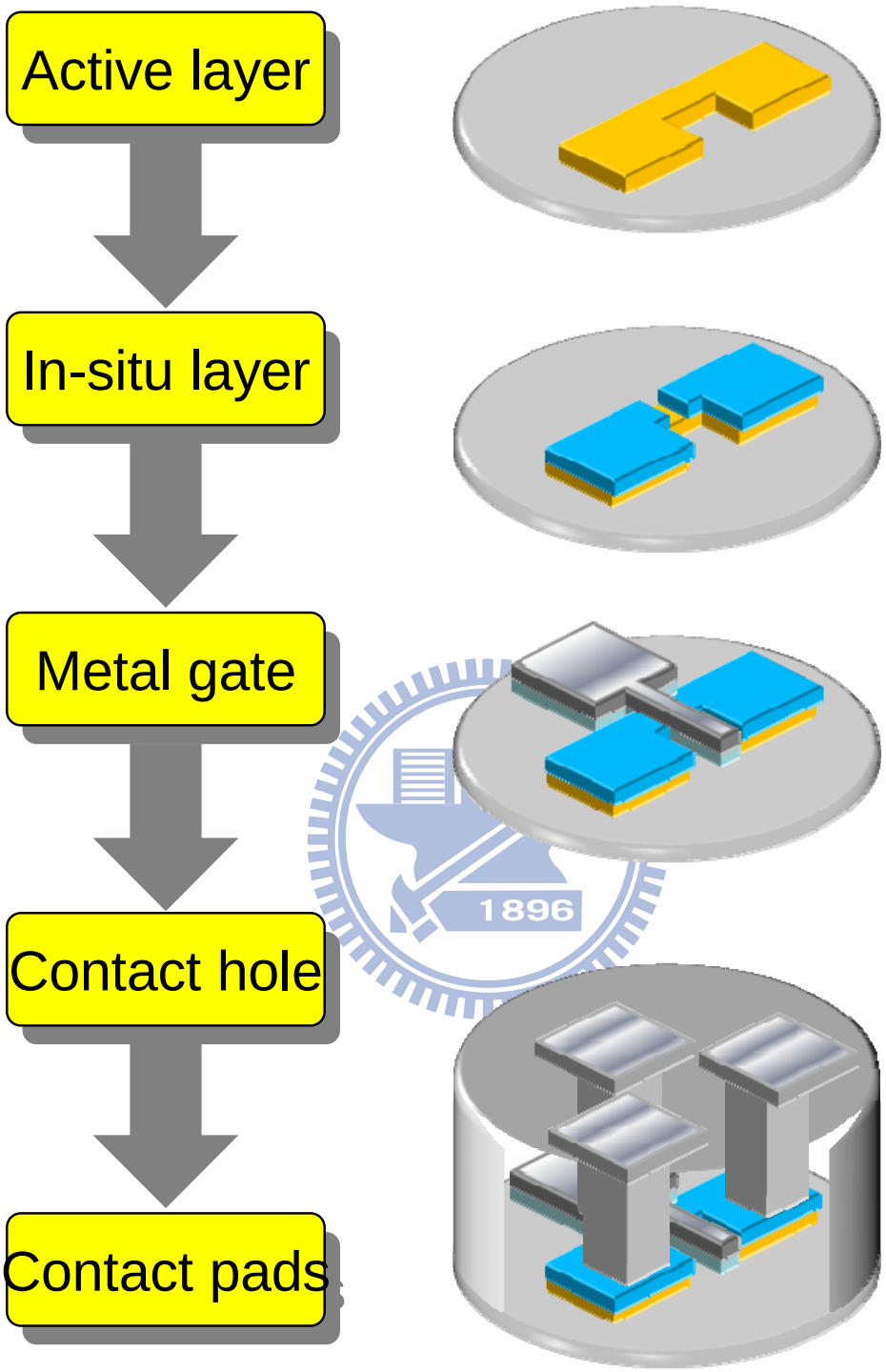


Fig. 6In-situ dopant TFTs fabrication flow chart

Chapter 4 Results and Discussions

4.1 CV measurement

In order to test quality of gate oxide at low temperature of 200°C, test samples were deposited thickness of 100nm with three ICP power of 200,250 and 300W by HDPCVD. Schematic of metal-oxide-semiconductor (MOS) structure and top view shows in **Fig**. **7.** Typical capacitance-voltage (C-V) characteristic of an metal-oxide-semiconductor (MOS) structure with a top circular Al pad, 400 μm in diameter, is presented in **Fig**. **8(a),(b)** and **(c)** as ICP power of 200,250 and 300W respectively. All test capacitors were measured from -10V to 10V incremental 0.1V with high frequency of 100kHz. Although more efficient gas was dissociated with ICP power increasing, but more interface damage was increased from Ion bombardment. **Fig**. **8(c)** shows a very noticeable effect of the interface traps is that the curves are stretched out in the voltage direction. This is due to the fact that extra charge has to fill the traps, so it takes more total charge or applied voltage to accomplish the same surface potential ψ_s, (or band bending).[1] **Fig**. **8(a)**and **(b)** shows good C-V characteristic nearly, but **Fig**. **8(a)** shows lower leakage current density than **Fig**. **8(b)**.

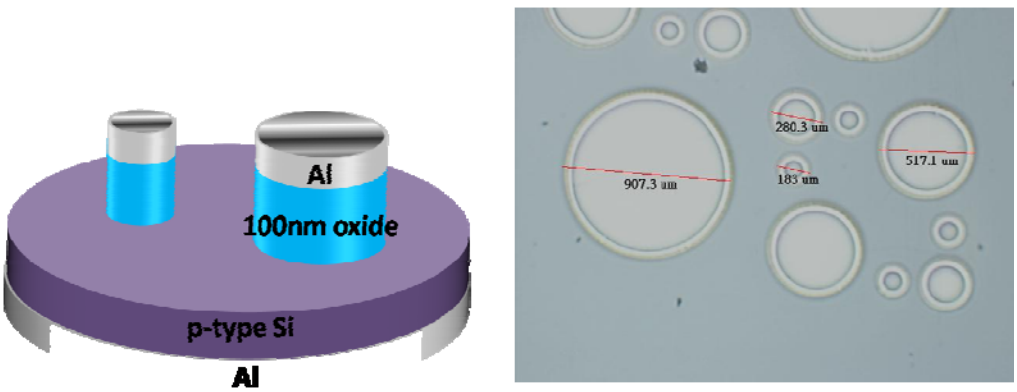
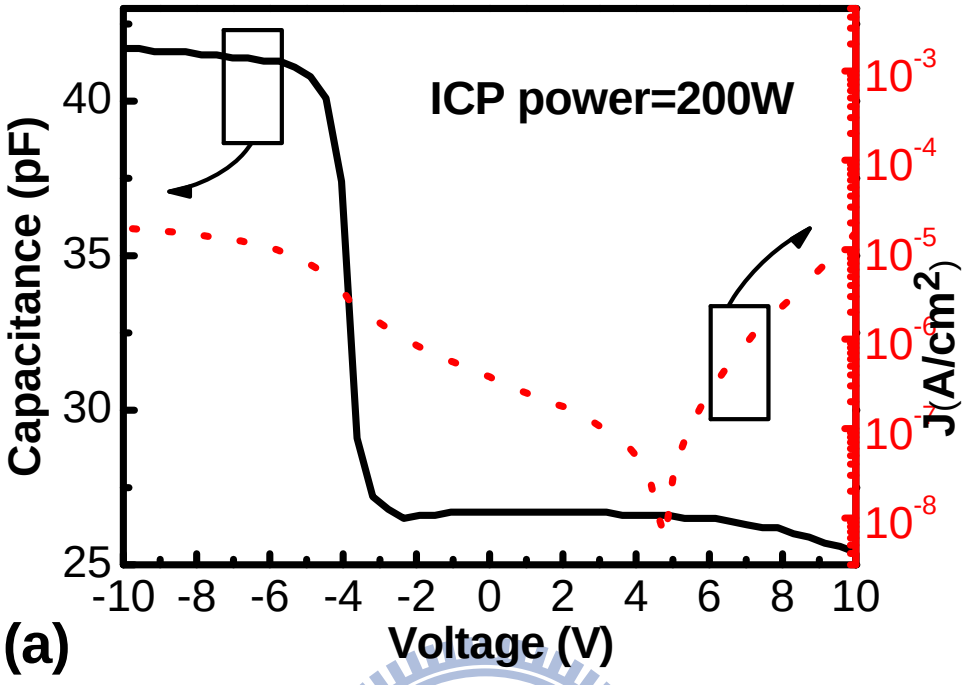
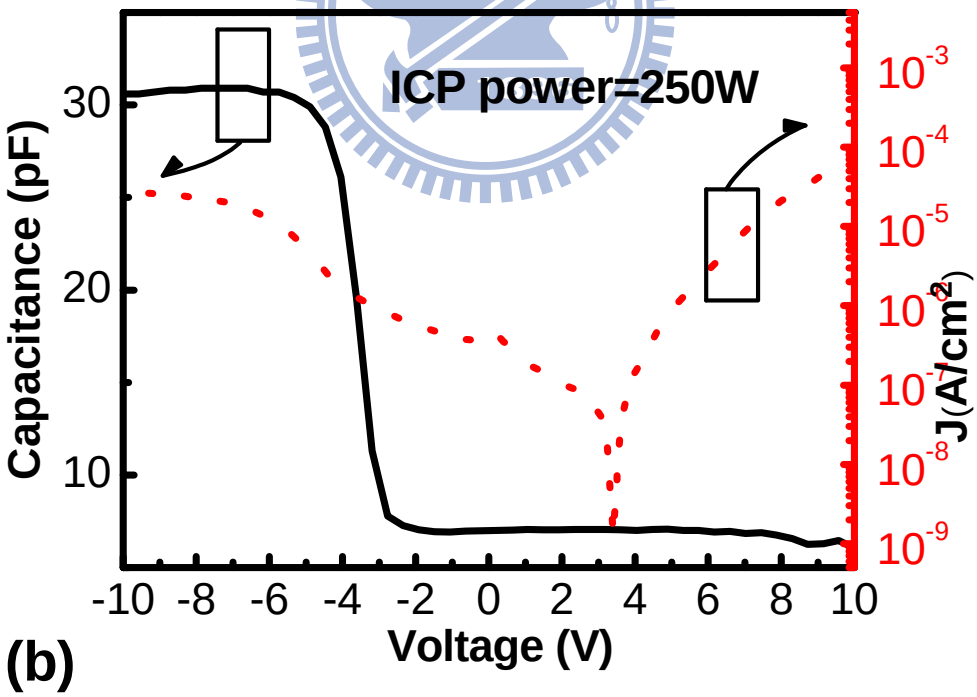


Fig. 7 Schematic of metal-oxide-semiconductor (MOS) structure and top vie


ICP power=200W
Capacitance (pF)
40
35
30
25
-10 -8 -6 -4 -2 0 2 4 6 8 10
Voltage (V)
10-3
10-4
10-5
10-6
10-7
10-8
J(A/cm2)

(a)


ICP power=250W
Capacitance (pF)
30
20
10
-10 -8 -6 -4 -2 0 2 4 6 8 10
Voltage (V)
10-3
10-4
10-5
10-6
10-7
10-8
10-9
J(A/cm2)

(b)

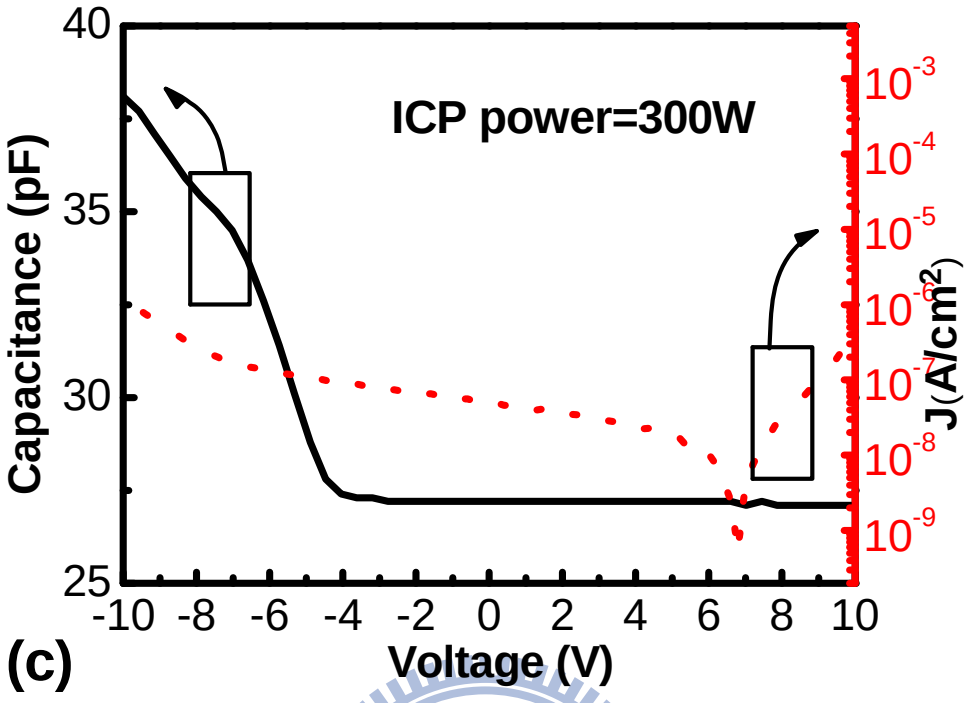


Fig. 8 (a),(b)and (c) Typical capacitance-voltage (C-V) characteristic of MOS capacitors were fabricated with ICP power as 200W,250W and 300W respectively

4.2 Microcrystalline silicon film characterization

There were two intrinsic μc-Si:H films prepared by HDPCVD and HWCVD. First intrinsic μc-Si:H films were prepared by HDPCVD. The μc-Si:H thin films were deposited at the pressure 20mrott, ICP power of 450W, SiH_4=10sccm ,H2=300sccm,substrate temperature of 200°C on the Si(100) wafer with 500 nm oxide and Corning glass substrate. Second intrinsic μc-Si:H films were prepared by HWCVD. The μc-Si:H thin films were deposited at the pressure 10mrott on the Si(100) wafer with 500 nm oxide and Corning glass substrate. For the hot wire we used 4-5 coiled tungsten filaments with 0.5 mm in diameter, the distance between the filament and substrate of 4.5cm, the filament temperature of 1800°C ,SiH4=10sccm,H2=130sccm and the substrate temperature of 200°C.

Fig. 9(a),(b) shows the XRD spectra of μc-Si:H by HDPCVD and HWCVD respectively. The diffraction peaks for (111), (220), and (311) planes are visible for the films deposited on the Si substrate and the preferred orientation is (111). **Fig. 10(a)** shows the TEM image of intrinsic μc-Si:H by HDPCVD. In **Fig. 10(b),** it shows clearly that incubation layer of 20nm**. Fig**. **11(a)-(b)** shows the plane-view SEM images of intrinsic and n-type deposited on the Si substrate with 5000Å oxide at a substrate temperature of 200 °C by HWCVD. It reveals that the μc-Si:H films consisted of a large amount of granular grains as shown in **Fig**. **11(a)** and **(b).** The cross-section of μc-SiH i-layer films structure also was shown in **Fig. 11(c)** It clearly demonstrated that the column μc-Si:H structure with a grain sizes of ~50-100 nm and a column grain height of ~100-300 nm were grown vertically on the substrate. In addition, the deposition rate of μc-Si:H films with large grain sizes was about 5-7 Å/s, which was higher than traditional plasma system, such as PECVD [2]. It considered that the efficient catalytic decomposition of precursor gases at the heated metal filaments [3], good gas utilization (>75%) [2, 4, 6], and thus high deposition rates are

achieved using HWCVD. Whatever, the column structures of μc-Si:H is still advantage of the transport of carriers [7-8]. To verify this benefit of column structure from μc-Si:H, the μc-Si:H TFTs has been fabricated.

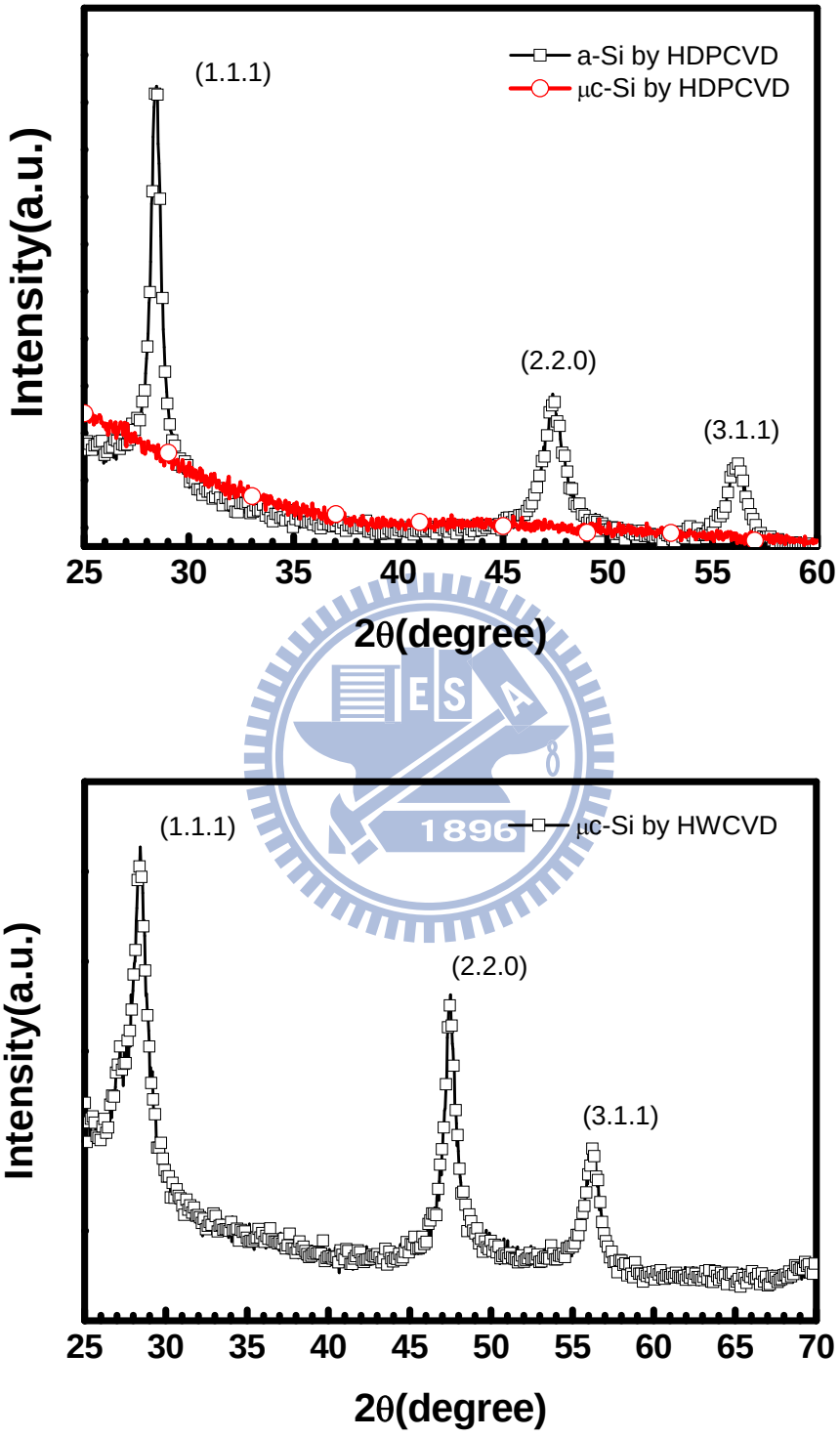


Fig. 9 (a),(b) shows the XRD spectra of μc-Si:H by HDPCVD and HWCVD

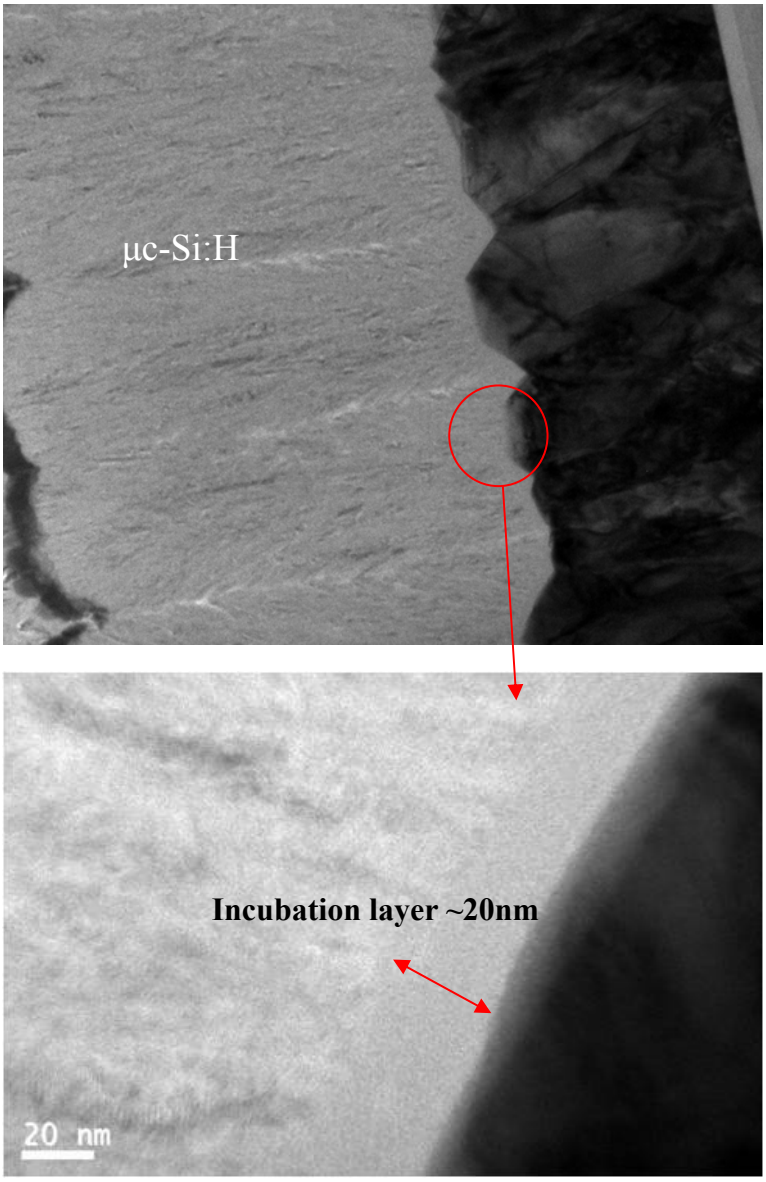


Fig. 10 (a)TEM image of μc-Si:H by HDPCVD (b) Incubation layer of 20nm

H

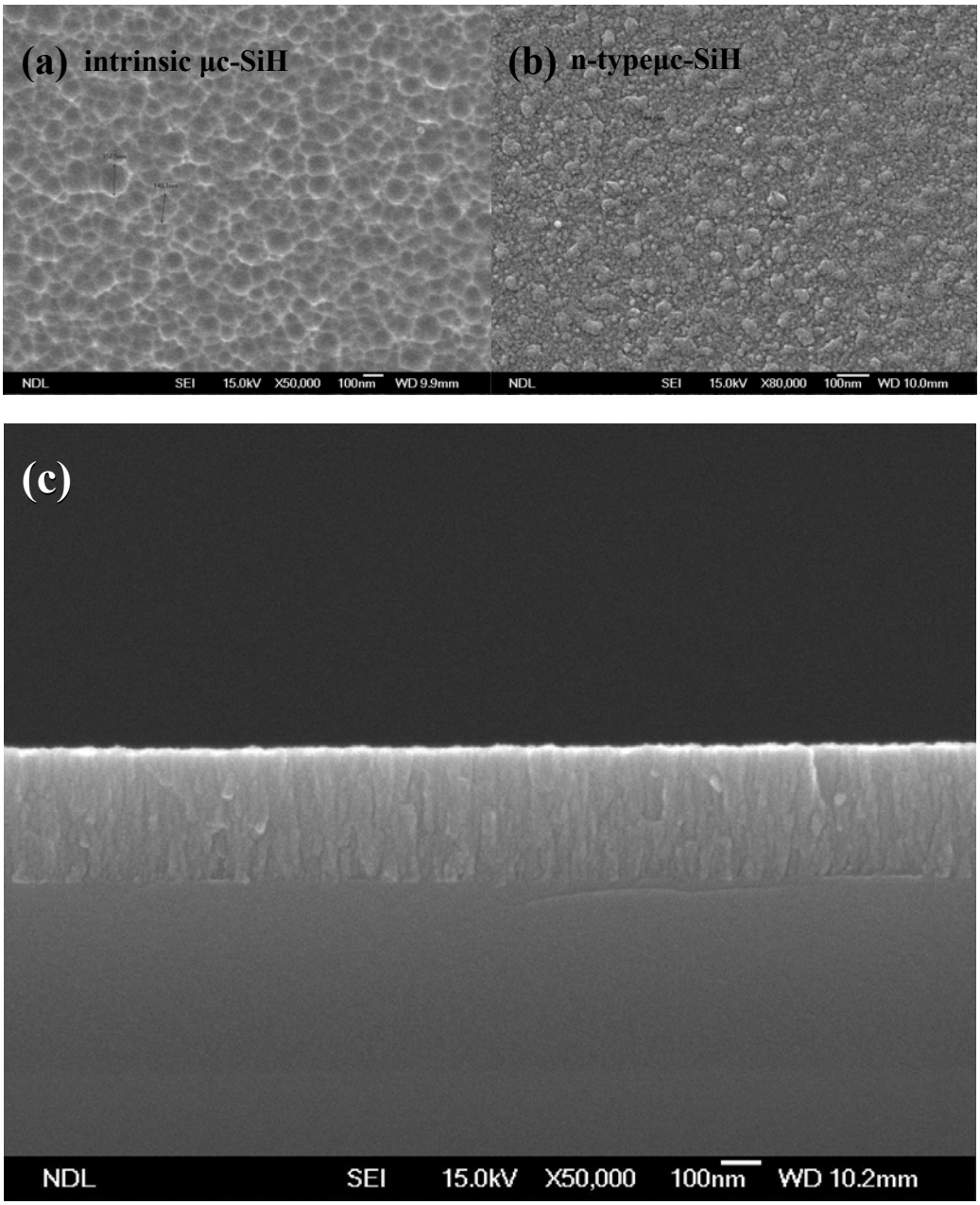


Fig. 11 (a), (b) Plane-view SEM images of intrinsic and n-type µc-Si:H (c) The cross-section of µc-SiH i-layer films structure by HWCVD

4.3 Highly conductive doped flim

In order to made sure the interface between n^+nc-Si and metal as ohmic contact. A metal-semiconductor (MS) device was fabricated with Al/n^+nc-Si:H stack on 500nm oxide on silicon wafer. Schematic of MS device shows in **Fig. 12** The resistance is expressed as $R = \rho \frac{L}{A} = \rho \frac{L}{W \cdot t}$, where ρ is resistivity, L is length , W is electrode width, t is thickness of film respectively. We design the length between two electrodes equal to the width of electrode, then the resistivity ρ is simplification into $\rho = t \times R$. The resistance R can be extracted by fitting the I-V curve. The n+nc-Si:H was deposited at process pressure 5mtorr, SiH_4=3sccm,H_2=36sccm, diluted PH_3=1,2,3,5and 8% and the filament temperature of 1700°C by HWCVD. **Fig. 13(a),(b)** shows resistivity of undoped and difference doped films respectively. According to these results, the n+nc-Si:H with doped PH_3=3% was chosen for S/D of the in-situ doped TFTs.

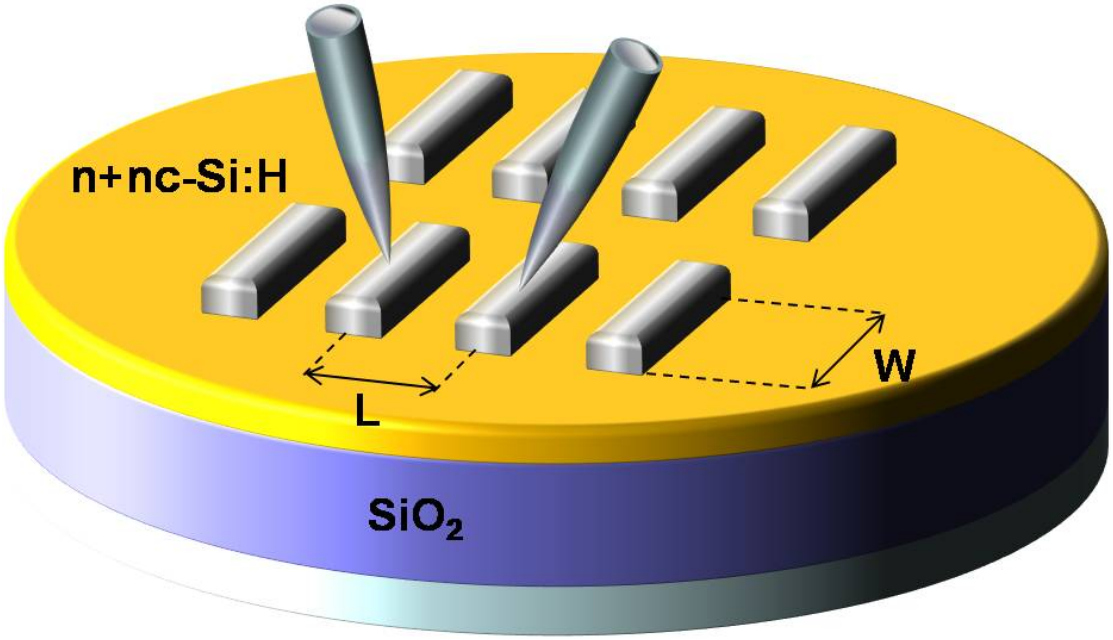


Fig. 12 Schematic of metal-semiconductor device

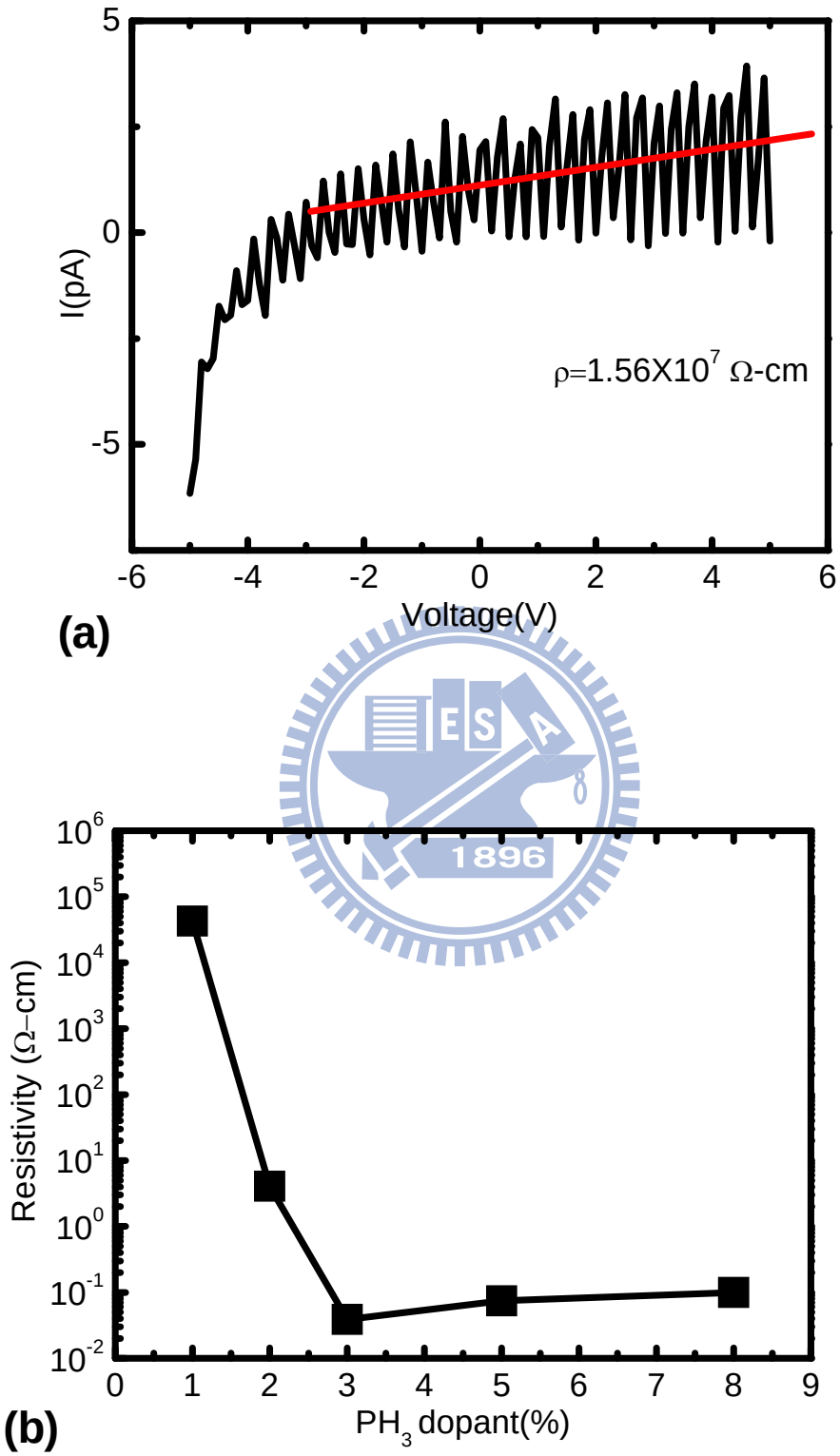


Fig. 13 (a) IV-curve of Intrinsic nc-Si;H film (b) Resistivity of n^+nc-Si:H with different PH_3 dopant

4.4 IV characterization and Density of states of laser-activated self-aligned TFTs

To extract density of states of amorphous/microcrystalline silicon by FEC method from TFTs, three different active layer channel of TFTs with 100nm oxide layer as gate dielectric was fabricated as illustrated on **Fig**. **14**. And **Fig**. 14**(a) and (b)** are amorphous and microcrystalline active channel layer by HDPCVD. **Fig. 14(c)** is microcrystalline active layer by HWCVD **Fig. 15(a) , (b)** shows transfer and output characteristics curves of amorphous silicon active layer TFTs with a channel width of 20 um and a channel length of 15um by HDPCVD. The transfer characteristics curves applied V_g varied from 0 V to 15V with an increment of 0.1 V while the drain voltage V_D was kept constant at 1 V. As the V_g changed from 0V to +15V, the device switches from the off state to the on state with the threshold voltage 8V. The field-effect electron mobility (μ_{eFE}) is calculated from the transconductance of the TFT operating in the linear regime at V_D = 1 V, $\mu_{eFE}=(\partial I_D/\partial V_G)(L/CoxV_DW)$, where $\partial I_D / \partial V_G$, Cox, and L/W are the transconductance, the a-SiOx gate dielectric capacitance per unit area, and the TFT channel length to width ratio, respectively. It is seen that the maximum value of μ_{eFE} is 0.22 cm^2/V-s. The sub-threshold slope is 0.45 V/decade and the ON/OFF current ration more than 10^4. **Fig**. 16**(a) , (b)** shows transfer and output characteristics curves of microcrystalline silicon active layer TFTs by HDPCVD with a channel width of 4 um and a channel length of 15um at V_D=1V. The maximum value of μ_{eFE} is 3.62 cm^2/V-s. The sub-threshold slope is 0.33 V/decade and the ON/OFF current ratio more than 10^5. **Fig**. 17**(a), (b)** shows transfer and output characteristics curves of microcrystalline silicon active layer TFTs with a channel width of 15 um and a channel length of 8um by HWCVD at V_D=1V. The maximum value of μ_{eFE} is 16.26 cm^2/V-s. The sub-threshold slope is 0.25 V/decade and the ON/OFF current ratio more than 10^6.

In order to extract density of states from Field Effect Transconductance (FEC) method, flat-band voltage was required. So we measure these three different TFTs at different temperature from 25°C to 150°C with an incremental of 25°C. **Fig. 18** shows the density of states which were extracted from three different active channel layer TFTs.

The crystallinity of the active channel pay an important role to relate to electrical characteristics of amorphous/microcrystalline TFTs. The field-effect mobility of amorphous/microcrystalline TFTs in the **Fig. 15 (a)**,**Fig. 16(a)** and **Fig. 17(a)** is enhanced from 0.22-16.26 cm^2/V-s as the crystallinity increasing. The results indicate that the crystallinity are improved by degrees. In addition, the reduction of threshold voltage with increasing crystallinity is due to decrease the grain boundaries of active channel layer. It also shows that subthreshold swing slope is lowered initially from 0.45 V/decade to 0.25 V/decade. Since the subthreshold swing slope is usually made use of estimating the interface trap density in standard MOSFET technology. In poly TFTs, the subthreshold swing slope is controlled by both bulk trap states and interface trap density near mid-gap [8]. The subthreshold swing slope *S* of poly-Si TFTs is given by

$$S = \frac{kT}{q} \cdot \ln 10 \cdot \left(1 + \frac{C_D + C_{ts}}{C_{ox}}\right) \qquad \text{Eq.4-1}$$

Where C_{ox} is the oxide capacitance per unit area, C_D is the depletion layer capacitance per unit area, and $C_{ts}=q^2D_{ts}$, where D_{ts} ($ev^{-1}cm^{-2}$) is the density of total trap states in the vicinity[1] of the intrinsic Fermi level. In poly-Si TFTs. The density of trap states near mid-gap D_{ts} includes both bulk trap density D_{bulk} and interface trap density D_{it}. Since the poly-Si film is thin and intrinsic, $C_D \ll C_{ts}$ and the subthreshold swing slope of poly-Si TFTs is given by

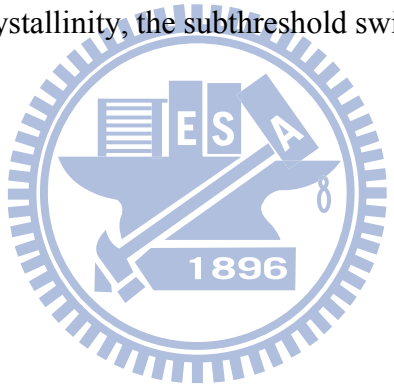
$$S = \frac{kt}{q} \cdot \ln 10 \cdot \left(1 + \frac{C_{ts}}{C_{ox}}\right) = \frac{kt}{q} \cdot \ln 10 \cdot \left(1 + \frac{q^2 \cdot D_{ts}}{C_{ox}}\right) \quad \text{Eq.4-2}$$

Considering that in a first approximation the devices are fully depleted, i.e., the energy band bending occurs over the whole poly-Si film thickness, the D_{ts} can be approximated as

$$D_{ts} = D_{bulk} \cdot t_{Si} + D_{it} \quad \text{Eq.4-3}$$

Where D_{bulk} is the mean bulk trap density, t_{Si} is the poly-Si film thickness, and D_{it} is the interface trap density.

Following above equations, subthreshold swing slope of poly-Si TFTs is reflected by bulk trap density and interface trap density. As the grain boundaries defects are terminated by increasing crystallinity, the subthreshold swing slope is decreased.



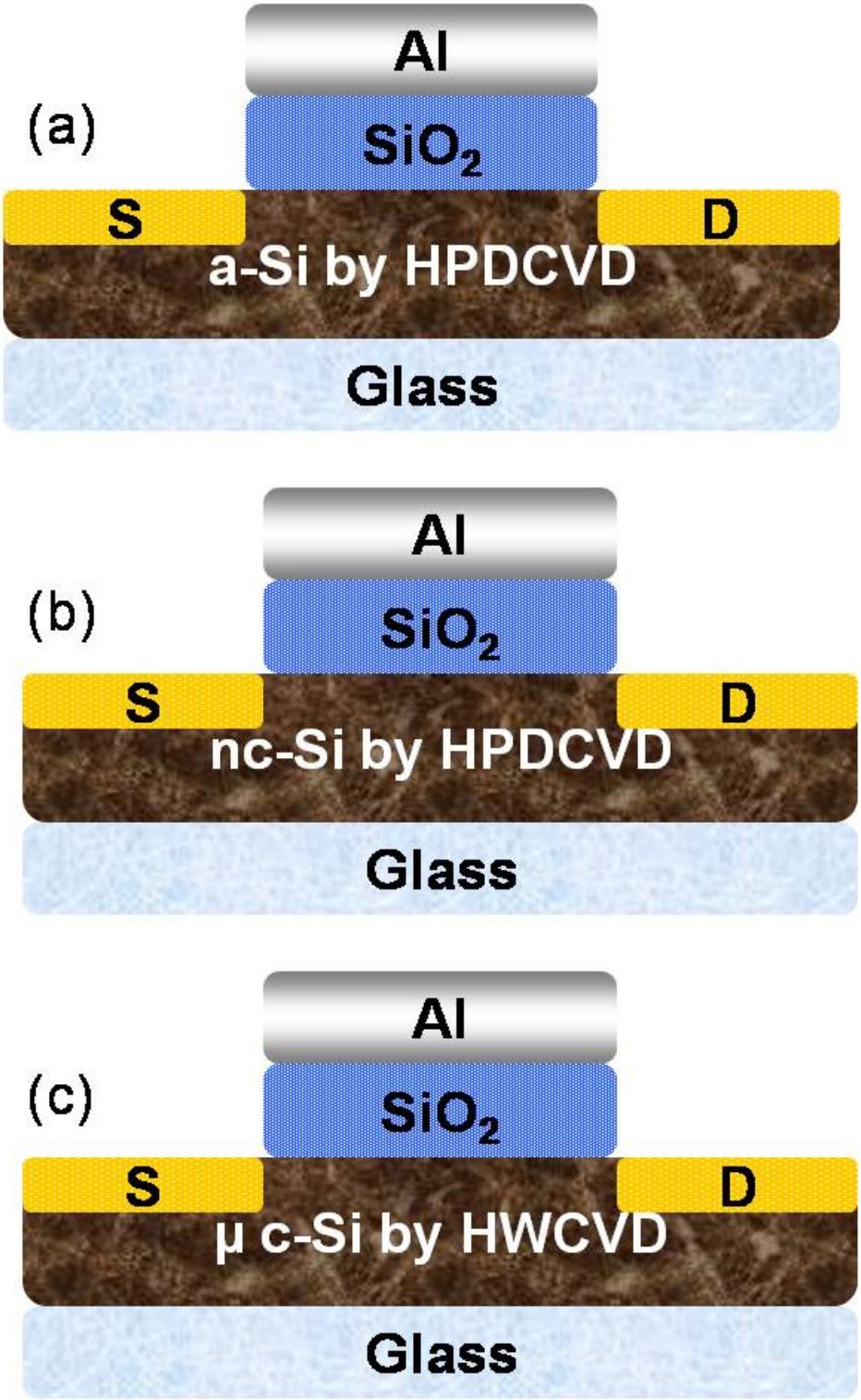


Fig. 14 Schematic cross section of self-aligned amorphous/microcrystalline silicon TFT.

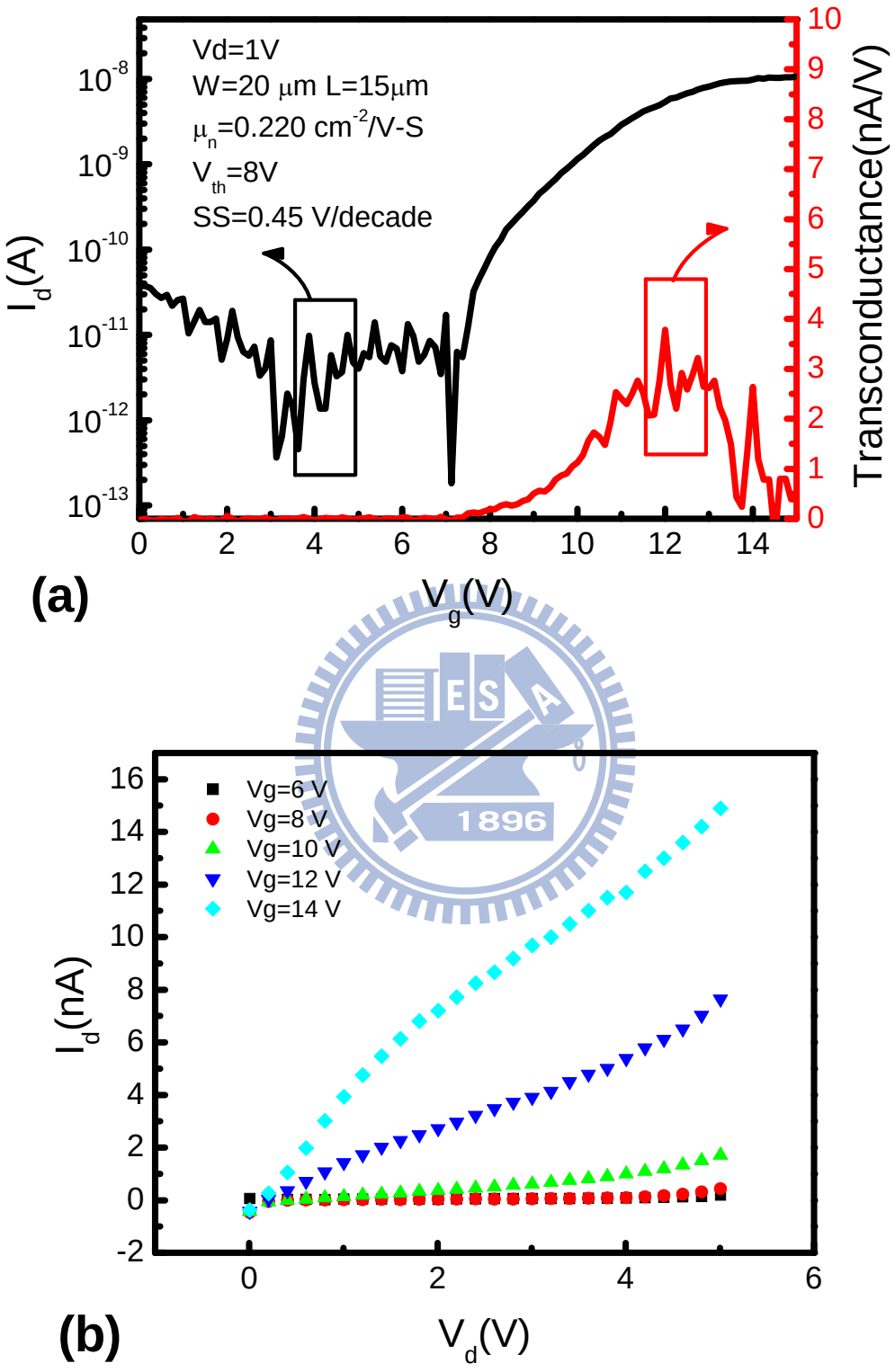


Fig. 15 (a) Transfer and (b) output characteristics of amorphous silicon n-type TFTs by HDP-CVD

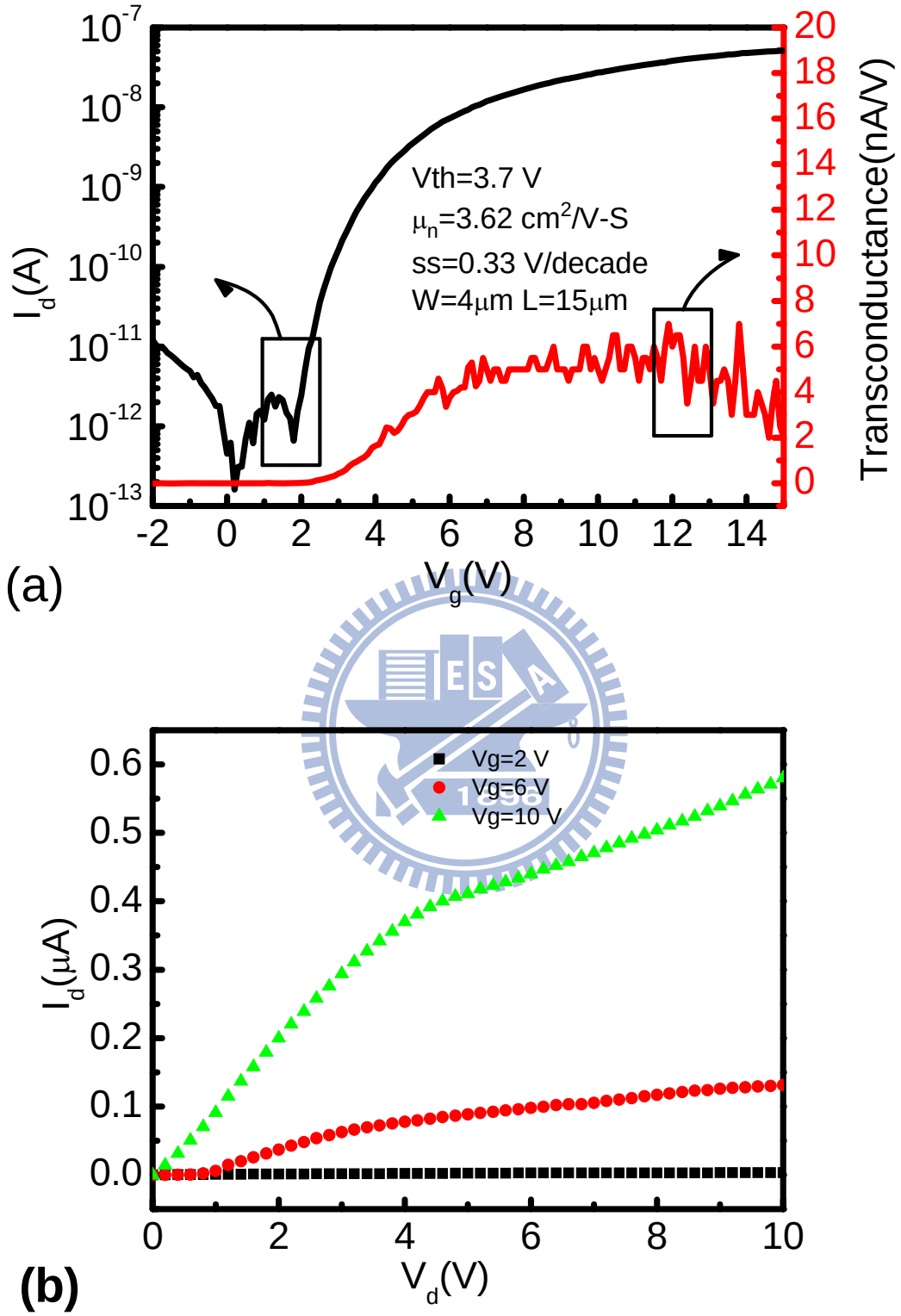


Fig. 16 (a) Transfer and (b) output characteristics of microcrystalline silicon n-type TFTs by HDP-CVD

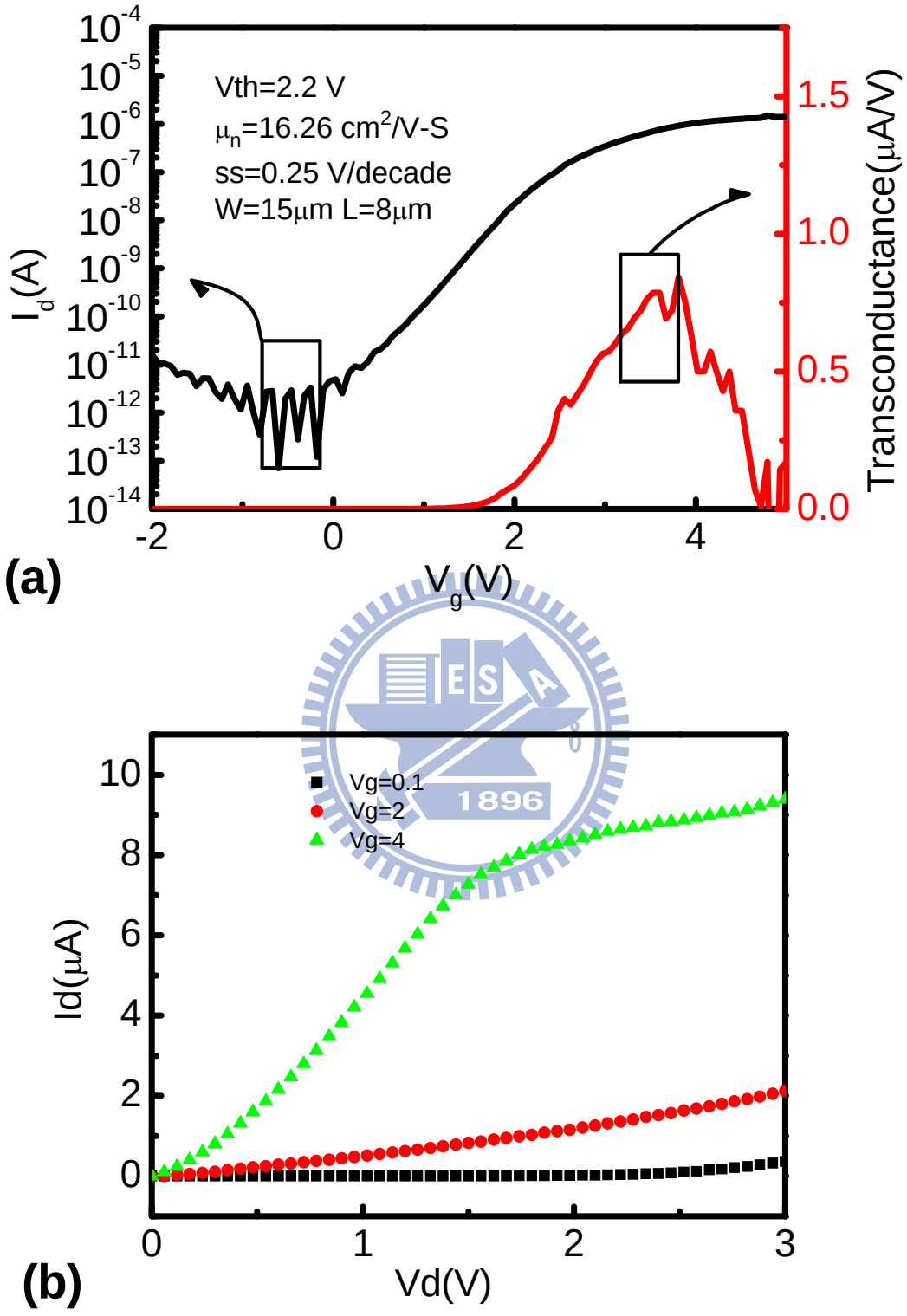


Fig. 17 (a) Transfer and (b) output characteristics of microcrystalline silicon n-type TFTs by HW-CVD

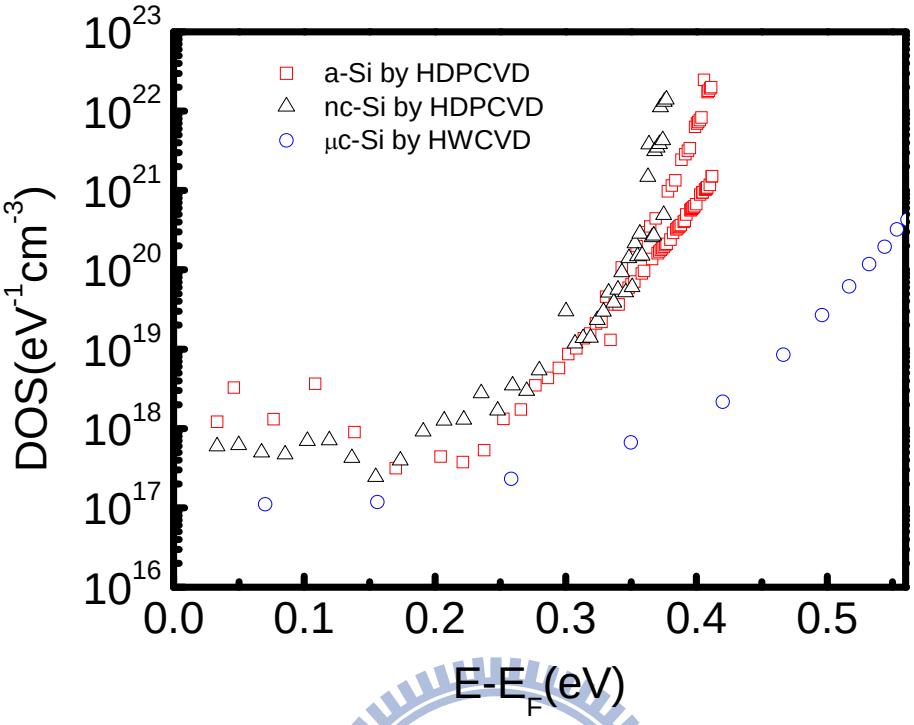


Fig. 18 The density of states distribution of amorphous/microcrystalline TFTs were extracted from Field Effect Conductance (FEC) method.

4.5 IV characterization and Density of states of In-situ dopant TFTs

For the purpose of suitable for flexible display, low temperature TFTs without S/D implantation is necessary. So the highly conductance doped layer is required that the interface between nc-Si and metal is ohmic contact. This type of TFTs was called In-situ dopant TFTs. A TFTs with a microcrystalline active layer of 100nm, in-situ doped layer of 50nm and oxide as gate dielectric of 100nm was fabricated as illustrated on **Fig. 19**. The TFTs with a channel width of 10 um and a channel length of 60um was fabricated on microcrystalline silicon layer on glass substrate. **Fig. 20 (a) , (b)** shows transfer and output characteristics curves of in-situ doped TFTs by HDPCVD. The maximum value of μ_{eFE} is 50.2 cm^2/V-s. The sub-threshold slope is 0.157 V/decade and the ON/OFF current ratio more than 10^4. **Fig. 21 (a) , (b)** shows transfer and output characteristics curves of in-situ doped TFTs by HWCVD. The maximum value of μ_{eFE} is 19.26 cm^2/V-s. The sub-threshold slope is 0.097 V/decade and the ON/OFF current ratio more than 10^4. The density of states distribution shows in **Fig. 22** which was extracted from in-situ doped TFTs by FEC method. **Fig. 23 (a) ,(b)**shows schematic three-dimensional of in-situ doped TFTs and top view.

Defect density associated with the deep state in the silicon energy bandgap exerted a significant influence on the off-state current, and the density related to tail state governed the on-state current.[9] **Fig. 22** shows the corresponding density of states distribution fitted to the curves in **Fig. 20(a)** and **Fig. 21(a)**. The density at the midgap is almost the same order of magnitude. The subthreshold swing slope is also related to midgap defect. **Fig. 20(a)** and **Fig. 21(a)** show low subthreshold swing slope of 0.097 and 0.14 V/decade , because defects at midgap is low(the deep state). The electron mobility could be improved from 19.26 to 50.2 cm^2/V-s due to the reduction of gap state near the conduction band edge or decrease in the slope of gap state near the conduction band edge.[10]

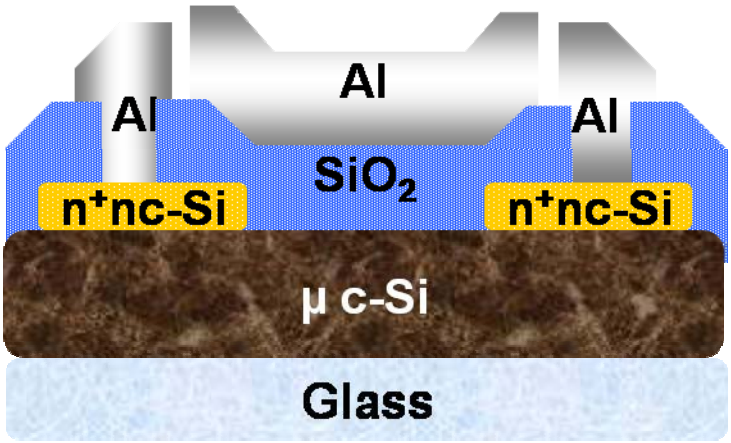


Fig. 19 Schematic cross-section of a standard n-channel top-gate staggered nc-Si:H TFT with n+ nc-Si:H ohmic contacts.

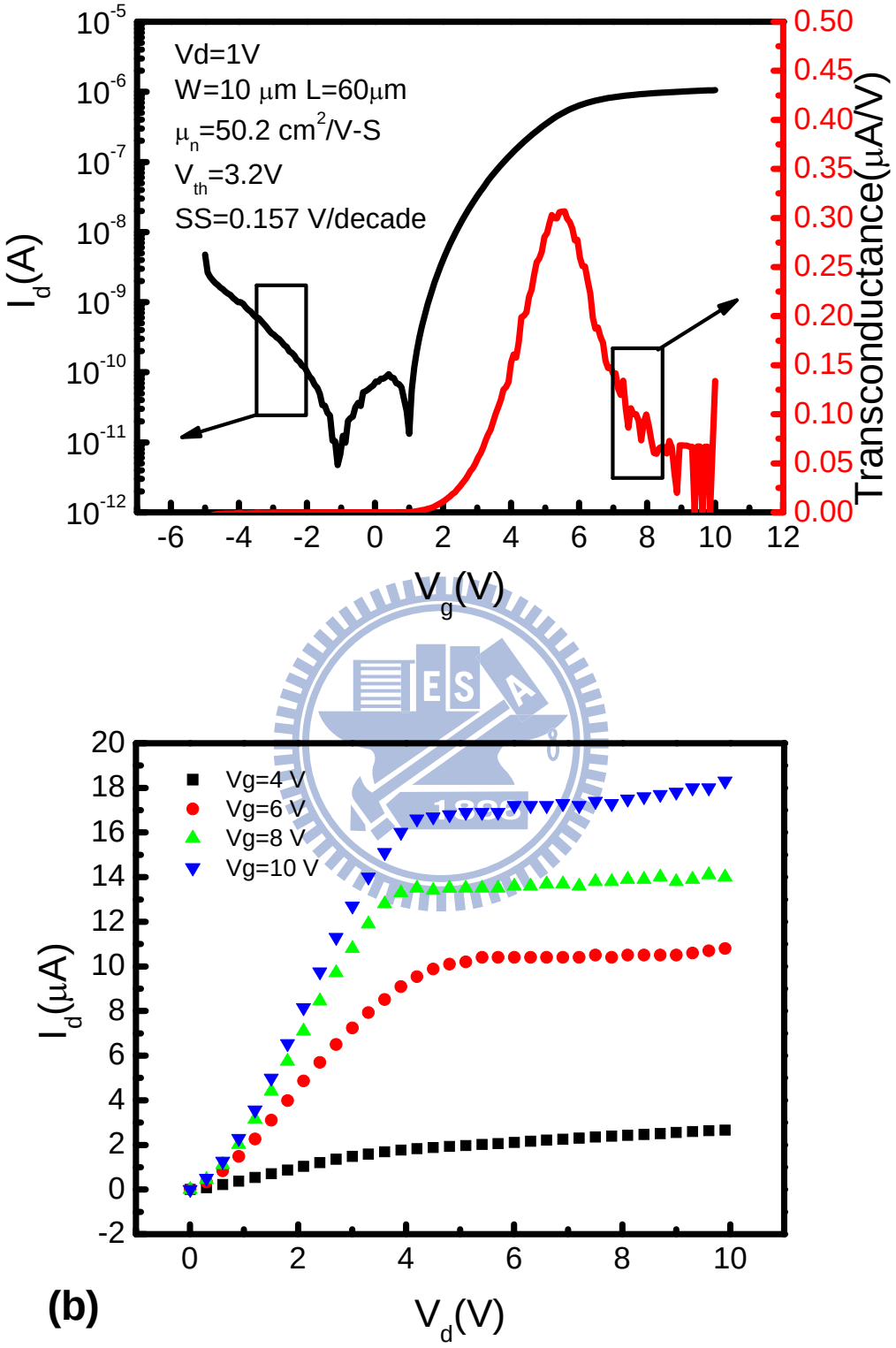


Fig. 20 (a) Transfer and (b) output characteristics of amorphous silicon n-type TFTs by HDP-CVD

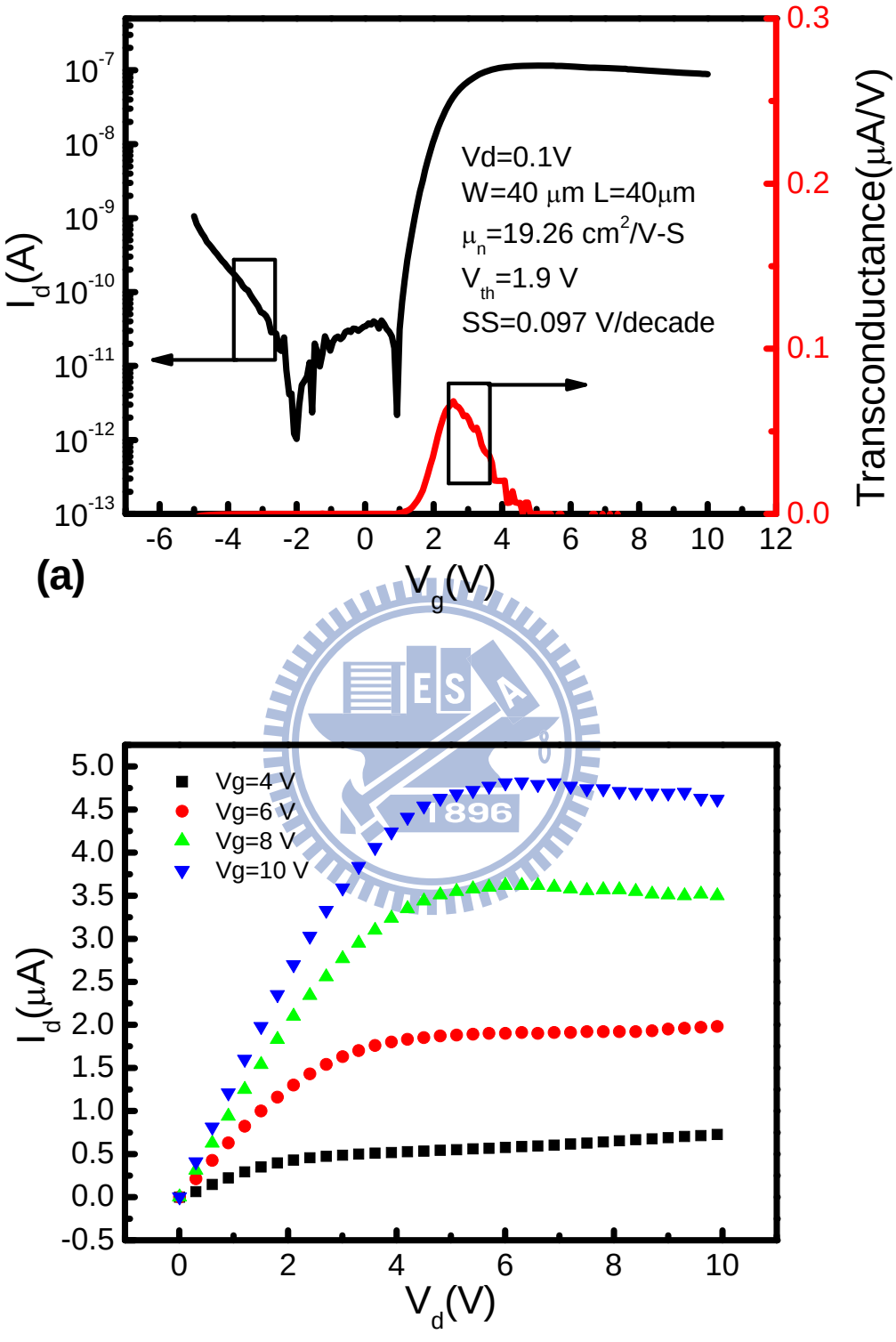


Fig. 21(a) Transfer and (b) output characteristics of amorphous silicon n-type TFTs by HWP-CVD

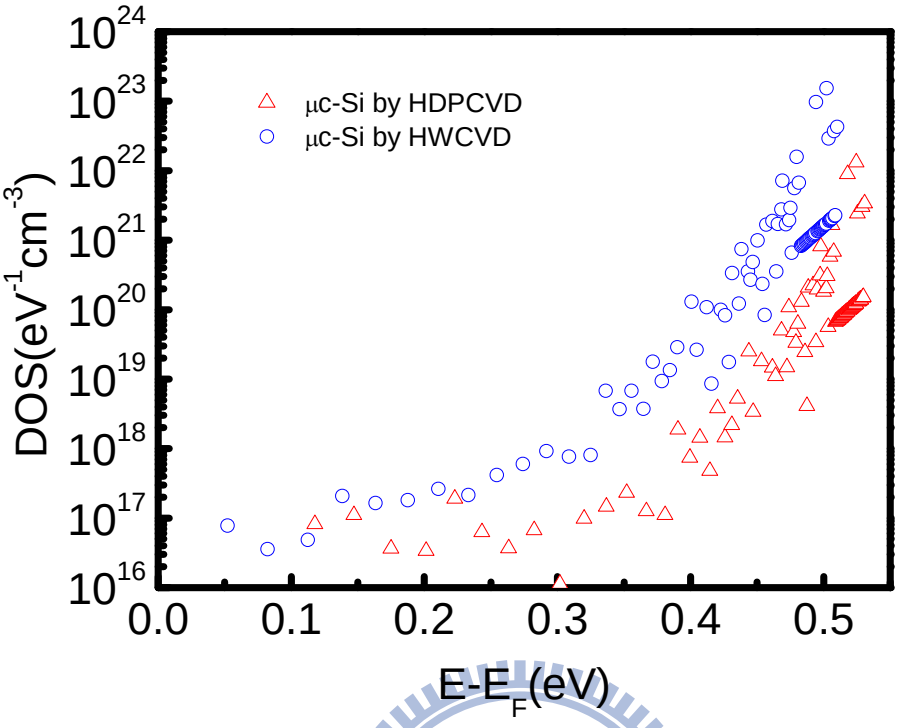


Fig. 22 The density of states distribution of in-situ doped TFTs were extracted from Field Effect Conductance (FEC) method.

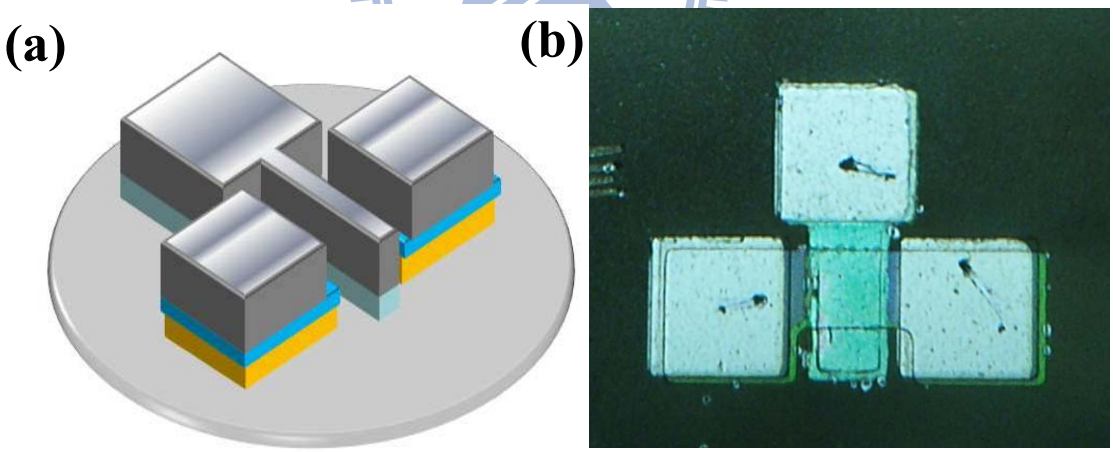


Fig. 23 (a) ,(b)shows schematic three-dimensional of in-situ doped TFTs and top view

Chapter 5 Conclusions and Future work

5.1 Conclusions

In summary, top-gate microcrystalline silicon TFTs were realized at maximum process temperature of 200 °C with high electron charge carrier mobilities exceeding 50 cm^2 /V-s ,and on/off ration exceeding 10^4 under low voltage operation at V_D=0.1V. The V_T and the subthreshold swing are in the range of 1.8-2.5 V and 0.1-0.45 V/decade, respectively. The experimental results reveal that the highest charge carrier mobility and the lowest defect density are obtained when the intrinsic microcrystalline silicon channel material is grown by HDPCVD and HWCVD. Microcrystalline silicon allows for the low temperature integration of high performance TFTs on glass and plastic substrates.

5.2 Future work

The flexible electronics on plastic substrates possess advantageous characteristics, being lightweight, durable, flexible, and have the capacity to be manufactured in a variety of shapes, which leads to freedom of design. Furthermore, the in-situ dopant TFTs use the same material as thin film solar cell, so we can integrate these two devices as new generation green display technology.

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