

高介電值氧化物應用於三五族半導體 金氧半元件之研究

研究生：林鼎鈞

指導教授：張翼 博士

國立交通大學材料科學與工程學系

摘要

當傳統半導體如矽發展至 22 奈米結點時將會遇到瓶頸。在眾多的替代材料中，三五族複合物因為擁有優越的特性如高的電子遷移率而備受期待，但由於三五族複合物並沒有原生氧化物的存在，以至於半導體和閘極氧化層之間的界面品質仍有待提升。高介電值氧化物能使元件擁有更高的電容值且能在較厚的物理厚度下仍能維持與二氧化矽相同的平均氧化層厚度；其能減少漏電流並進一步提升元件特性，因此高介電值氧化物做為閘極氧化層應用在三五族複合物半導體上的金氧半元件一直是三五族複合物半導體主要的研究方向。

本實驗中將二氧化鉛及二氧化銻加上二氧化鉛的閘極堆疊結構做為閘極氧化層沉積在砷化銻鎳上，製作成金氧半結構的電容，接著在不同的快速退火溫度後進行量測與討論；獲得極低的表面捕獲能帶以及磁滯現象。以二氧化銻加上二氧化鉛的堆疊結構做為閘極氧化層的金氧半場效電晶體的量測結果也將被討論。

Study of high-k/III-V MOS devices

Student: Ting-Chun Lin

Advisor: Dr. Edward Yi Chang

Department of Material Science and Engineering

National Chiao Tung University

Abstract

III-V semiconductor material has been researched and considered as the alternative channel material to silicon for complementary Metal-Oxide-Semiconductor (CMOS) applications beyond the 22nm node due to its superior properties. High-k dielectric was introduced as gate dielectrics for III-V material Metal-Oxide-Semiconductor (MOS) structure, because it can maintain the equivalent oxide thickness with thicker physical thickness resulting in the leakage current reduction and the capacitance improvement.

In this study, HfO₂ and CeO₂ were used as gate oxides on InGaAs MOS capacitors; the both oxides have the larger dielectric constant than Al₂O₃ which is commonly used as gate oxide for III-V materials. HfO₂/InAs MOS capacitors with varied Post Deposition Annealing (PDA) temperatures were demonstrated for the first in this study; low interface trap density and hysteresis were obtained which implies excellent interface quality. CeO₂/HfO₂ gate stack structure was introduced as gate dielectrics for InGaAs MOSFET; the design of the stack structure can improve the capacitance meanwhile prevent the diffusion between the oxide and the semiconductor. The MOSFET with CeO₂/HfO₂ gate oxide was also fabricated and the measurement results are discussed.

誌謝

兩年前興奮的看著錄取榜單彷彿還是昨天的事，轉眼間就到了碩士班生涯的終點站，雖然早以經歷過不同階段的分離但心中仍是百感交集，準備迎接未來的雀躍和脫離學生生涯的惆悵互相交織，碩士班生涯過程中有太多要感謝的人，首先要感謝實驗室的大家長張翼教授，提供如此好的研究環境，讓學生能夠充分學習和發揮，而在研究之餘也安排很多集體出遊讓學生在忙碌的研生活中能獲得喘息。再來要感謝元件組的大學長林岳欽學長，能給學長帶到真的是一件非常幸運的事，學長的指導總是不帶架子且親和力十足，跟學弟的互動與討論就像家人一般，不慎犯錯學長也不會一味責備而是馬上討論解決辦法，在這邊要祝福學長新婚愉快及往後的人生事業都能順心如意。再來要感謝宋先敏學長，在我初進實驗室還懵懵懂懂的第一年給予我很多不管是課業或是實驗上的協助，祝學長未來事業鴻圖大展也能快快抱得美人歸。再來要感謝我的實驗搭擋盧柏菁，一起攜手在無塵室的無數個日子我永遠也不會忘，雖然實驗過程中經歷無數失敗但也都撐過來了，你對事情的執著也值得我學習，希望你未來的生涯發展可以順順利利。再來要感謝黃冠寧和郭澤耀學弟，很高興能帶到你們兩個好相處也很聽話的學弟，就靠你們把學長的熱情在組內不斷的傳遞下去了，也祝你們未來一年的碩士班生涯可以快樂順心且無往不利。另外還要

感謝 409 辦公室的室友，游宏偉學長、鐘珍珍學姐、許青翔學長，郭俊佑和王韋傑，謝謝你們給我了一個快樂的 409 生涯，雖然中餐常常連吃學校餐廳好幾天，但跟你們做伙，瓜子醬菜都變成山珍海味。另外還要感謝同組的張嘉華學長和謝廷恩學長以及實驗室其他所有曾協助過小弟的成員，沒有你們不會有今天的我。我還要感謝 405 套房的成員，兩隻蜜袋鼯小朋友妮妮和必魯，每當我拖著疲憊的身軀走進家門總是用大眼睛天真的看著我再加上溫暖的飛撲，馬上讓我的不愉快一掃而空。最重要的我還要感謝我的女朋友妹妹，妳的鼓勵和支持好比武當山的靈丹妙藥，讓我在不斷的失敗中能重新站起來，週末相伴的出遊踏青更是一解苦悶的良方，希望我們能一路攜手走下去。最後的最後我要感謝我的家人，奶奶、阿公、阿媽、我最愛的老爸、老媽還有老弟，雖然你們不懂我實驗在做什麼東西，但給我的鼓勵和建議絕對比任何的研究數據更加珍貴，另外還有爺爺在天之靈的一路庇佑，我愛你們！ 感謝的人實在太多無法一一列出，小弟就先謝天了！

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