Chapter 1

Introduction

1.1 Background and research motivation

According to the Moore's law in Fig. 1-1, the number of transistors that can be placed on an integrated circuits has doubled approximately every two years. In order to follow this trend, the size of transistors should be minimized. But when the devices size was scaled down under 45nm node, the SiO_2 couldn't prevent the direct tunneling due to the thinner thickness, and the unwanted horizontal electron field increases drastically resulting in poor gate modulation ability decreasing. To solve these problems, high dielectric constant oxide was introduced to replace the SiO_2. According to the ITRS roadmap of semiconductor in Fig. 1-2, silicon will reach the limit when transistors gate length scale to 22nm node. III-V semiconductor material has been researched and considered as the alternative channel material to silicon for complementary metal-oxide-semiconductor applications beyond the 22nm node due to its ascendant properties including higher electron mobility and larger saturation velocity.

1.2 Development and challenges of high-k on III-V MOS devices

High-k dielectrics and high mobility channels including stained-Si, germanium and III-V materials have been researched imperiously to

extend the Moore's law and ITRS roadmap. Silicon technology is predicted to reach its limit when entering 22nm node, germanium and III-V material are expected to be alterative p-type and n-type channel materials for next generation high speed devices due to their superior transport properties than silicon including high electron mobility and drift velocity as shown in Fig. 1-3 and Table 1-1. For III-V materials, characteristics like direct band gap and band engineering have been used in optoelectronic and high frequency applications. Integration of III-V material with high-k dielectrics for III-V MOSFET application is the challenge for next generation logic devices.

The main issue of high-k on III-V material is the interface problem. III-V material does not have native oxide like silicon to silicon dioxide, so the interface quality between the high-k oxide and the semiconductor is very poor. There are many interface traps at the interface that degrade the device performance, and comes the Fermi level pinning phenomena.

In the past few years, many reports about the III-V/high-k interface issues have been published. Its well known that the surface pretreatment including sulfide and ammonia solution treatments could eliminated the unwanted particles and native oxide, furthermore, the surface of III-V material could be passivated to prevent the surface exposed to air. With the progress of advanced deposition technologies, many passivation methods had been reported including Gd_2O_3/Ga_2O_3 or Gd_2O_3 growth as gate dielectrics[1-2], the Al_2O_3 growth by Atomic Layer Deposition (ALD)[3-5], oxide formation by oxidation of AlInP[6] and using interface passivation layer (IPL) or interface control layer (ICL) like Ge, Ge_XN_Y

and silicon[7-10].

Among all the deposition technologies, the Molecular Beam Epitaxy system (MBE) shows more superior characteristic for oxide deposition. The MBE deposition was done in ultra high vacuum environment to prevent the unwanted contamination, and the MBE deposition is a very slow process which ensures the films grow epitaxlly. It can achieve the high purity level than any other deposition technology. In this study, the MBE system was used for high-k oxide deposition.

1.3 Focus of this thesis

The $In_XGa_{1-X}As$ channel layer with high indium content can provide the superior properties including larger drive current and higher drift velocity than traditional semiconductor materials. In this study, the $In_XGa_{1-X}As$ material was used as the channel material of MOS devices.

Among all the high-k materials, HfO_2 shows superior properties than the others and many reports about HfO_2 on InGaAs[11-13] have been published in recent years, very few HfO_2 on InAs have been reported. The HfO_2/InAs MOS capacitors were fabricated with various post deposition annealing (PDA) temperature first in this study. The devices characteristics such as interface trap density (D_{it}), flat band voltage shift and hysteresis are evaluated in the following chapters.

In order to achieve larger capacitance for the devices, the oxide with high dielectric constant is needed. CeO_2 has relatively high k-value about 38 but small energy band gap of about 3.2eV. To solve the diffusion and leakage problem, HfO_2 with large energy band gap about 5.5eV was

deposited between the CeO_2 layer and the InGaAs semiconductor material. Thermal stability and Capacitance – Gate Voltage characteristics of the HfO_2/InAs MOS capacitor are evaluated in this study. Both oxides have higher k-value than Al_2O_3 which is common used as gate dielectric for III-V material MOS devices.

CeO_2/HfO_2 stack structure is also demonstrated as gate dielectric for $In_XGa_{1-X}As$ MOS capacitor and the results are compared to the HfO_2/$In_XGa_{1-X}As$ MOS capacitors.
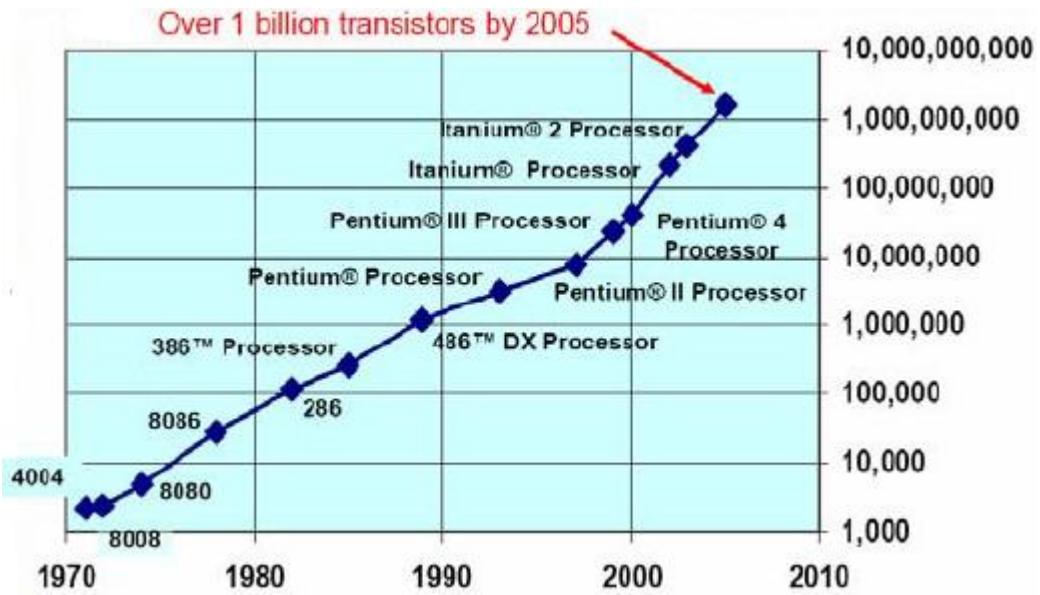
Fig 1-1 Moore's law: The numbers of transistor per chip versus years by
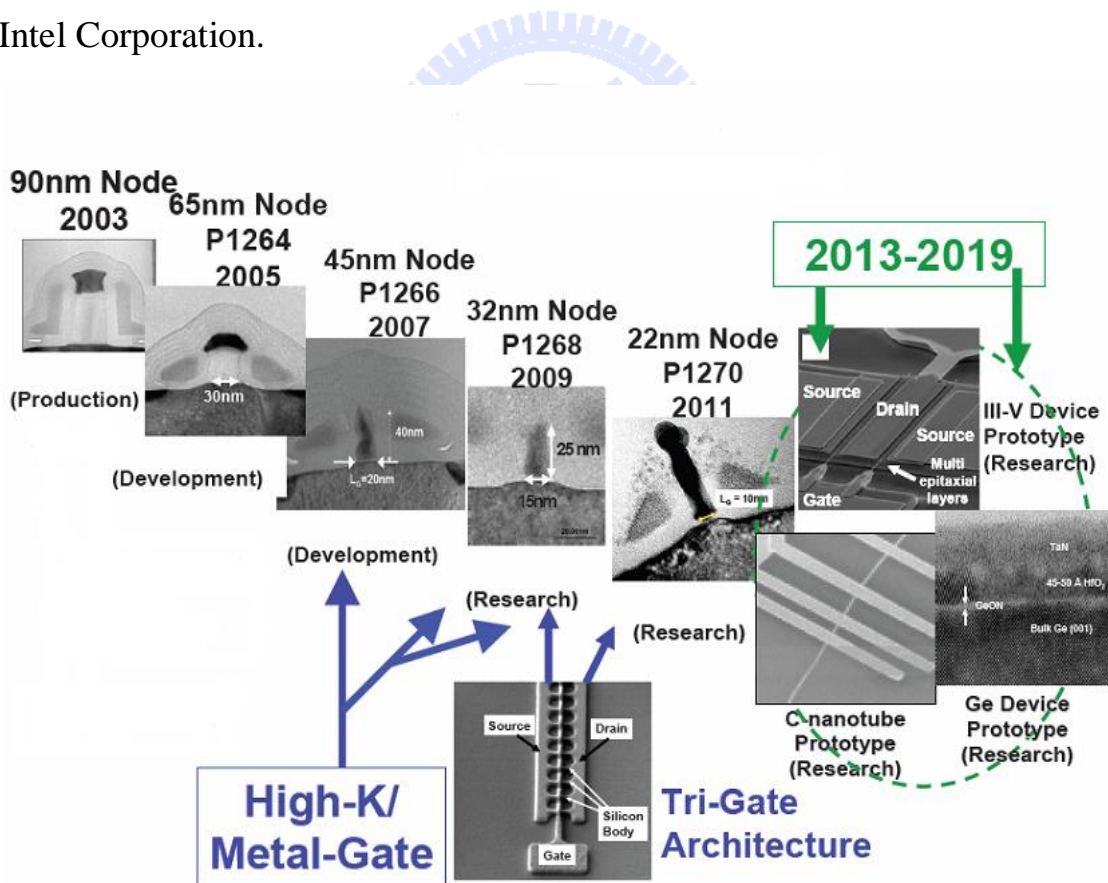
Intel Corporation.

Fig. 1-2 The ITRS roadmap of CMOS scaling by Intel Corporation.

Table 1-1 Comparison for energy band gap and mobility of several

channel material candidates

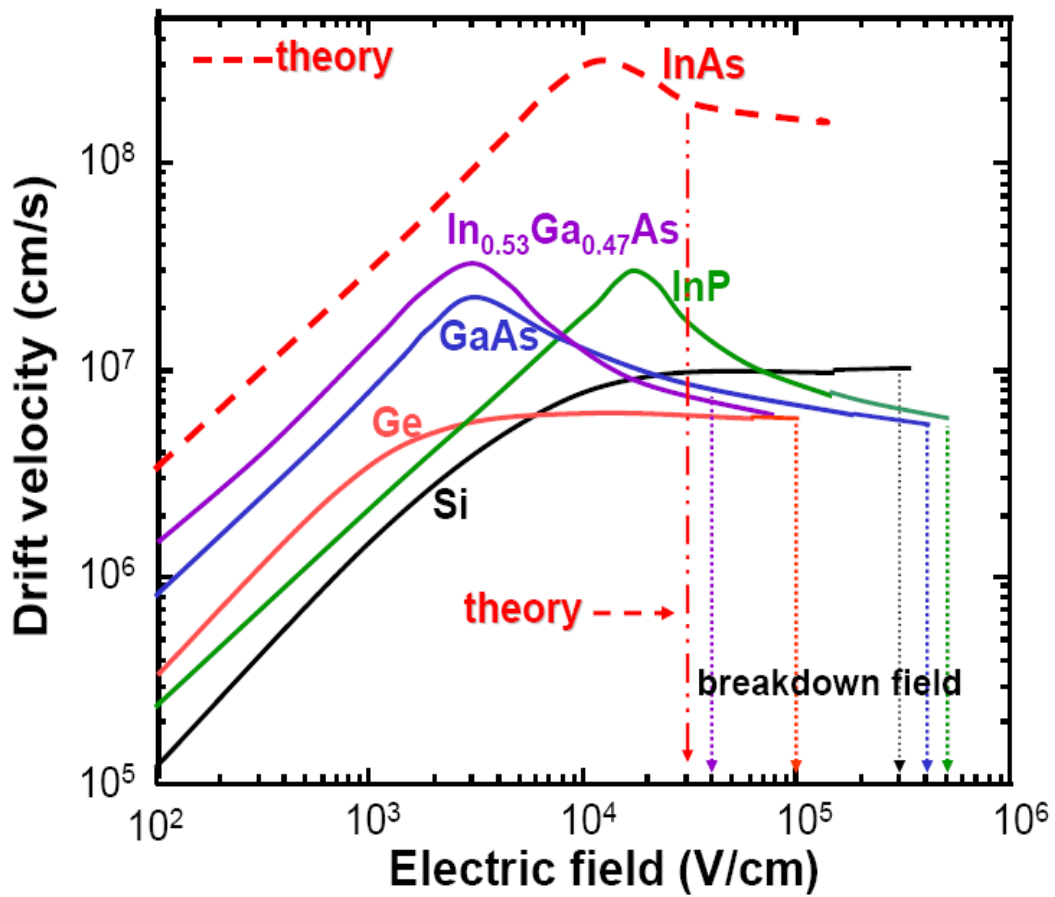|	Silicon	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
$E_g(eV)$	1.12	0.66	1.42	0.75	0.36
$\mu_e(cm^2V^{-1}s^{-1})$	1350	3900	8500	13800	20000

Fig 1-3 Drift velocities versus electrical field as a parameter of

semiconductors

Chapter2

Metal-Oxide-Semiconductor Structure

In this chapter, the structure and basic operation modes of an ideal Metal-Oxide-Semiconductor capacitor (MOSCAP) and ideal Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) are studied. Besides, the non-ideal phenomena are also introduced.

2.1 Metal-Oxide-Semiconductor capacitor(MOSCAP)

In order to understand the Metal-Oxide-Semiconductor field effect transistor (MOSFET), the working principle of Metal-Oxide-Semiconductor capacitor (MOSCAP) which forms the important gate-channel-substrate structure of the MOSFET must be first described. Due to the lacking of native oxide, III-V MOSCAP is also a primary way to check the interface quality between the gate dielectric oxide and semiconductor before the III-V MOSFET fabrication. In the following sections, the basic structure of MOSCAP and its four different operation modes including flatband, accumulation, depletion and inversion are reviewed.

2.1.1 Basic structure and operation modes

The MOS capacitor structure is illustrated in Fig. 2-1. The gate metal is on the top of the MOS capacitor and below following by a thin oxide layer as gate dielectric and semiconductor substrate. The backside electrode is on the bottom of the semiconductor.

Depends on the doping types of CMOS devices, it can divide into PMOS and NMOS. Due to the inversion behavior of MOS structure, PMOS is built on the n-type substrate and has a p-channel with holes as the majority carriers; on the other hand, NMOS is built on the p-type substrate and has an n-channel with electrons as the majority carriers. In the following discussion, only p-type substrate based MOS capacitor is described.

There are four different bias modes of MOS capacitor depends on the different bias voltages. When the energy diagram of the semiconductor is flat, which implies that no charges exists in the semiconductor as shown in Fig. 2-2, it is called *flatband condition* and the gate bias voltage is assumed zero. The flat band voltage is occurred when the applied voltage equals to the differences of work function between the gate metal ($q\emptyset_M$) and the semiconductor ($q\emptyset_S$). As shown in Fig. 2-2, qX is the electron affinity, the energy difference between the conduction band and the vacuum level in semiconductor. Eg is the energy band gap of semiconductor and $q\psi_B$ is the energy difference between Fermi level E_F and intrinsic Fermi level E_i. For an ideal MOS capacitor, the work function difference will be zero.

$$V_{FB} \equiv q\emptyset_{MS} \equiv (q\emptyset_M - q\emptyset_S) = q\emptyset_M - \left(qX + \frac{Eg}{2} + q\psi_B \right) = 0 \qquad (3\text{-}1)$$

If there are fixed charges in the oxide or at the surface between the oxide and semiconductor, the flat band voltage's expression must be modified. For an ideal NMOS capacitor, when we apply a negative voltage which is less than the flat band voltage, the positive carriers (holes) will be

attracted from the substrate to the oxide-semiconductor interface. Only a small band bending upward happens due to the buildup of accumulation charges as shown in Fig. 2-3. It is called *accumulation condition*.

When a positive voltage which is more than the flat band voltage is applied, the energy band is bended downward and the negative charge and built up in the semiconductor. This charge is due to the depletion of the semiconductor from the oxide-semiconductor interface. We call it in *depletion condition* and the band diagram is shown in Fig. 2-4. This is often referred as weak-inversion.

When we apply a larger positive gate voltage and the potential of semiconductor increasing beyond twice of the bulk potential, the minority carriers (electrons) of semiconductor emerges at oxide-semiconductor interface and the energy band bent even more which is shown in Fig. 2-5. The inversion layer is formed. When the applied gate voltage increased, the width of inversion layer will be increased and the carriers in the inversion layer will also be increased. This is the *inversion condition*.

The basic assumption for the derivation of MOS capacitor model is that the charge of the inversion layer is proportional with the applied voltage. The inversion layer charge is below the threshold voltage as described by:

$$Q_{inversion} = C_{ox} \, (V_G - V_{th}) \tag{3-2}$$

$$Q_{inversion} = 0 \tag{3-3}$$

This linear proportionality can be explained by the fact that a gate voltage variation will causes the charge variation in the inversion layer. The gate oxide capacitance is defined as the proportionality constant between the charge and the applied voltage. This assumption also implies that the

inversion layer charge is located exactly at the oxide-semiconductor interface. When the electron concentration is larger than n_i but smaller than the substrate doping concentration (N_A), the capacitor is in **weak inversion**. When the electron concentration in inversion layer reaches N_A, the condition which is called **strong inversion** will occur.

The Fig. 2-6 shows the energy band diagram at the interface of oxide and p-type semiconductor. The electrostatic potential ψ is defined as zero in the bulk of the semiconductor and positive when the band is bent downward, where ψs is the surface potential, the electrons density and holes density can be written as a function of ψ by using this concept:

$$n_P = n_i \exp\left(\frac{q\psi - q\psi_B}{kT}\right) \tag{3-4}$$

$$P_P = n_i \exp\left(\frac{q\psi_B - q\psi}{kT}\right) \tag{3-5}$$

And at the interface, the surface carrier densities are:

$$n_S = n_i \exp\left(\frac{q\psi_S - q\psi_B}{kT}\right) \tag{3-6}$$

$$P_S = n_i \exp\left(\frac{q\psi_B - q\psi_S}{kT}\right) \tag{3-7}$$

And since $\psi_B = \frac{kT}{q}\ln\frac{N_A}{n_i}$ equation (3-6) and (3-7) can be rewritten as

$$n_S = \frac{n_i^2}{N_A} \exp\left(\frac{q\psi_S}{kT}\right) \tag{3-8}$$

$$P_S = N_A \exp\left(-\frac{q\psi_S}{kT}\right) \tag{3-9}$$

The above discussions of flat-band, accumulation, depletion and inversion are summarized below:

$\psi_S < 0$ Accumulation of holes (bands bend upward)

$\psi_S = 0$ Flat-band condition

$$\psi_B > \psi_S > 0 \qquad\qquad \text{Depletion of holes (bands bend downward)}$$

$$\psi_S = \psi_B \qquad\qquad \text{Midgap with } n_s=n_p=n_i \text{ (intrinsic condition)}$$

$$\psi_S > \psi_B \qquad\qquad \text{Inversion (bands bend downward)}$$

2.1.2 MOS capacitor capacitance derivation

The behavior of small-signal capacitance variation with gate bias of MOS capacitor can provide further understanding of the electrical behavior of the MOS system. The static MOS capacitance is defined as:

$$C \equiv \frac{Q}{V} \tag{3-10}$$

Where Q is the total charge on the capacitor and V is the gate bias. The small-signal differential capacitance per unit area is:

$$C' \equiv \frac{dQ_S'}{dV_G} \tag{3-11}$$

For $V_G = V_{OX} + \psi_S$ with $V_{OX} = \frac{Q_S d}{\epsilon_{OX} A} = \frac{Q_S' d}{\epsilon_{OX}}$, equation (3-11) becomes:

$$C' = \frac{dQ_S'}{\frac{d}{\epsilon_{OX}}dQ_S' + d\psi_S} = \frac{1}{\frac{d}{\epsilon_{OX}} + \frac{d\psi_S}{dQ_S'}} = \frac{1}{\frac{1}{C_{OX}'} + \frac{1}{C_D'}} \tag{3-12}$$

where C_D' stands for semiconductor capacitance per unit area or depletion-layer capacitance per unit area. Equation (3-12) also implies that the total capacitance of the MOS capacitor is the series of the fixed capacitance of the oxide and the variable capacitance of the semiconductor as shown in Fig. 2-7, which depends on the applied gate voltage through the Ψ_S.

When the MOS capacitor is in depletion mode, equation (3-12) can be rewritten as

$$C' = \frac{1}{\frac{1}{C_{OX'}} + \frac{1}{\frac{\epsilon_S}{W}}} \qquad (3\text{-}13)$$

When the depletion region width reaches its maximum ($V_G = V_{th}$), the capacitance has it minimum value, the capacitance per unit area at maximum depletion becomes:

$$C' = \frac{1}{\frac{d}{\epsilon_{OX}} + \frac{W_m}{\epsilon_S}} \text{ (MOS capacitance at maximum depletion)} \qquad (3\text{-}14)$$

When the capacitor is in accumulation mode, depletion region diminishes. The capacitance has its maximum value which is equal to C_{OX}'.

$$C' = \frac{1}{\frac{d}{\epsilon_{OX}}} = \frac{1}{\frac{1}{C_{OX'}}} = C_{OX}' \text{ (MOS capacitance in accumulation)} \qquad (3\text{-}15)$$

When the applied voltage $V_G > V_{th}$, there are two extreme conditions: at low frequency, the electron in inversion layer can follow the AC small-signal, the capacitance of the inversion region is equal to the accumulation capacitance, the minority carriers are in thermal equilibrium with the small-signal; and if the frequency is high enough that the minority carriers can not follow, the capacitance will remain unchanged from its value at $V_G = V_{th}$, which is the minimum capacitance of the maximum depletion.

The capacitance per unit area of depletion, accumulation and inversion of high and low frequency in an ideal MOS capacitor are shown in Fig. 2-8.

2.1.3 Non-ideal MOS capacitor

In the former sections, the capacitor is assumed operated the ideal cases. It has been assumed that the insulator gate oxide has infinite resistance to preventing any charge carrier transport across the dielectric oxide layer

when a bias voltage is applied. Indeed, in the real situation, the applied voltage will induce charges in the metal and at the interface between the oxide and semiconductor. There is also a work function difference (q∅ms) between the gate metal and semiconductor. The both two factors will influence the flat band voltage of the capacitor.

(a) Work function difference

In a realistic MOS capacitor, the work function in the metal $q\emptyset_M$, is not equal to the work function in the semiconductor $q\emptyset_S$ resulting in the flat band condition not flat at zero gate voltage.

$$q\emptyset_{MS} = q(\emptyset_M - \emptyset_S) \neq 0 \qquad (3\text{-}16)$$

Fig. 2-2 shows the band diagram of ideal MOS capacitor in equilibrium without considering the work function difference. In the real situation, the flat band voltage is no longer be zero, the Fermi level should be aligned and the vacuum level should be continuous, which results in the band diagram as shown in Fig. 2-9, the band bending is to accommodate the work function difference. In order to obtain the flat band, an additional voltage apply is needed.

(b) Interface trap and oxide charges

The traps at the oxide-semiconductor interface and the unwanted oxide charges will also affect the MOS capacitor performance. Those unwanted defects can be divided into interface-trapped charge (Q_{it}), fixed-oxide charge (Q_f), oxide-trapped charge (Q_{ot}) and mobile ionic charge (Q_m). When the above factors are considered, the flat band voltage can be described as:

$$\Delta V_{FB} = V_{FB} - V_{FB}^O = \emptyset_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_O} \qquad (3\text{-}17)$$

The interface traps and oxide charges are indicated in Fig. 2-10. The poor interface also exhibited a C_{it} (capacitance of interface traps) that influenced the total capacitance and effective mobility. If there are amount of interface traps at the interface, the C-V curve will be distorted resulting in the degradation of devices performance.

2.2 Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

In this section, the basic operation and the non-ideal phenomena of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) are introduced.

2.2.1 Structure and basic operation

The simple MOSFET structure is shown in Fig. 2-11. In the MOSFET, an inversion layer at the oxide/semiconductor interface acts as a conducting channel. For example, in a p-type substrate MOSFET, the n-type inversion layer is formed between the n^+ ohmic source and drain region when the gate voltage applied. The majority carries are electrons. At DC conditions, there is an isolation region which provides from the depletion region and the neutral substrate. Besides there are two distinct electron field exist in the MOSFET structure which play the important roles in devices performance, called the transverse field and the lateral field. The transverse field is caused by the potential between the metal gate and the semiconductor which supports the substrate's depletion region and

inversion layer. The lateral field is formed by the non-zero potential between the source and drain; it can influence the current of MOSFET devices. Two electron fields are indicated in Fig. 2-12.

The ***threshold voltage (V_{th})*** definition is necessary before understanding the MOSFET operation. It is defined as the gate voltage where a depletion region forms in the substrate. The V_{th} separates the *on-* and *off*-states of MOSFET operation. The *on-* and *off*-states barriers are indicated in Fig. 2-13. The average potential energy of the channel electrons in the *off*-state is high relative to those of the source, creating an effective barrier against electron transport from source to drain. In the *on*-state, this barrier becomes lower significantly, promoting the free electrons in the channel region.

● ***The current-voltage relationship***

The basic I_D-V_D characteristic of enhancement-mode n-MOSFET is shown in Fig. 2-14. There are three regions of operation in the MOSFET. When the applied gate voltage is less than V_{th}, there is no conducting channel so the current will be zero; this is called the cut-off region. If we apply a gate voltage over the V_{th} and the drain-source voltage V_{DS} smaller than saturation, the devices is in the troide region. In this region, the lateral electron field increases when the V_{DS} increases and hence the current flow. Increasing the gate voltage enhances the inversion layer density results in larger current. If the V_{DS} increase over the saturation, it falls in the saturation region. In the saturation region, the drain density becomes small and the current is much less dependent on V_{DS}, but it still dependent on V_G. Increasing the V_G can still enhance the inversion layer

density. The voltage and current used in MOSFET operation is summarized below:

$V_G < V_{th}$ $\qquad$ in cut-off region

$V_G > V_{th}, V_{DS} < V_{DS,saturation}$ $\qquad$ in troide region

$$I_D = \left(\frac{W\mu_n C_{ox}}{2L}\right)[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2]$$

$V_G > V_{th}, V_{DS} > V_{DS,saturation}$ $\qquad$ in saturation region

$$I_D = \left(\frac{W\mu_n C_{ox}}{2L}\right)(V_{GS} - V_{th})^2$$

MOSFET operation mode can be divided into two types which are called depletion-mode (D-mode) and enhancement-mode (E-mode); E-mode of a field effect transistor is in which there are no charge carriers in the channel when the gate source voltage is zero. On the other hand, D-mode of a field effect transistor is occurred when charge carriers is presented in the channel when the gate source voltage is zero. In this study, the operation mode of MOSFET is inversion-type of E-mode MOSFET. The four types of MOSFETs are indicated in Table 2-1.

● *Transconductance*

The transconductance of MOSFET is defined as:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \tag{3-18}$$

Where I_D is the drain current. The transconductance is also called the transistor gain. It will increase with width of device increasing or the oxide thickness decreasing. The transconductance of an n-MOSFET is summarized as below:

$g_m = \frac{W\mu_n C_{ox}}{L}V_{DS}$ $\qquad$ in troide region

$$g_m = \frac{W\mu_n C_{ox}}{L}(V_{GS} - V_{th}) \qquad \text{in saturation region}$$

2.2.2 Non-ideal effects of MOSFET device

(a) Subthreshold conduction

In theory, there is no current flow when the V_G is below the V_{th}. But for a non-ideal MOSFET, the drive current is not equal to zero when V_G is below the V_{th} which is indicated in Fig. 2-15(a). This phenomenon is called subthreshold conduction, and the current is called subthreshold current.

Fig. 2-15(b) shows the band diagram of a p-type substrate MOSFET with $\emptyset_S > 2\emptyset_{fp}$, the semiconductor interface will become a lightly-doped n-type material due to the distance between the Fermi level and conduction band shorter than the distance between Fermi level and valence band. It will have a weak inversion layer between the n^+ source and drain which is called *weak inversion* or *subthreshold region*.

For large scale integrated circuits with thousands of MOSFET devices, the subthreshold current become more remarkable to increase the power gain. This phenomenon must be considered cautiously in the circuits design.

(b)Mobility changed

For an ideal MOSFET, the mobility is assumed as an unchanged value. But in reality, mobility changed with the variation of gate voltage. Besides, the effective mobility of carriers is decreased when it approachs the limit speed of saturation. When a positive gate voltage is applied, the

electrons are attracted to the surface. Afterward the electrons are driven out due to the Coulomb force which is called *surface scattering effect*. It could also cause the mobility decreasing. The effective mobility could be defined as:

$$\mu_{eff} = \mu_0 (\frac{E_{eff}}{E_0})^{-1/3} \tag{3-19}$$

μ_0 and E_0 values are decided from experimental results.

(c) High-field effect

High-field effect is occurred when the MOSFET dimensions is shrinked into the deep subs micrometer region but the V_{DS} remain unchanged. When the gate length is reduced, the electron field strength in channel will be increased which results in the acceleration and heating of carriers. The hot electrons will cause the devices failure. Impact ionization and gate current from hot electrons emission across the interface barrier, some researchers have even verified that the hot electrons can create the interface traps to reduce the current drive capability and transconductance. This phenomenon can also be called the hot-carriers effect.

(d) Short channel effect

For the MOSFET devices with very short channel, the charges will constitute a large fraction of the total gate depletion charges and results in the lowering of threshold voltage and limiting the electron drift characteristic in the channel. The most well-known short channel effect is *Drain Induced Barrier Lowering (DIBL)*, which means the barrier between the source and drain decreases when the gate length is decreased. In the other words, the channel becomes more attractive for carriers. The

DIBL effect exists even at zero applied drain bias due to the p-n junction region which is formed between the source and drain to the substrate. This will reduce the slope of I_D-V_G curves, which means a larger change of gate bias is required to induce the same change in drain current. The DIBL also affects the curves of I_D-V_D in the active mode and lowering the MOSFET output conductance.

(e)Gate leakage and oxide thickness

As is mentioned in the former sections, the gate leakage current must be considered as it can degrade the devices performance of non-ideal MOSFET. The oxide with thicker thickness can prevent the leakage current but unsuitable for the device's size reduction progress. In order to solve this problem, high-k oxide is introduced. The oxide with higher dielectric constant can maintain the equivalent oxide thickness while reduce the leakage current and also improve the capacitance per unit area.
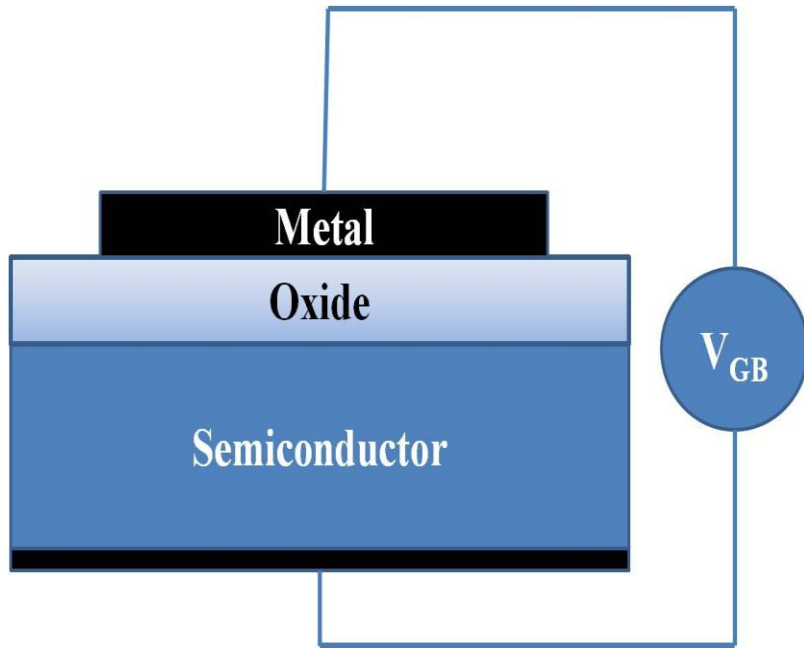
Fig. 2-1 Basic Metal-Oxide-semiconductor capacitor structure
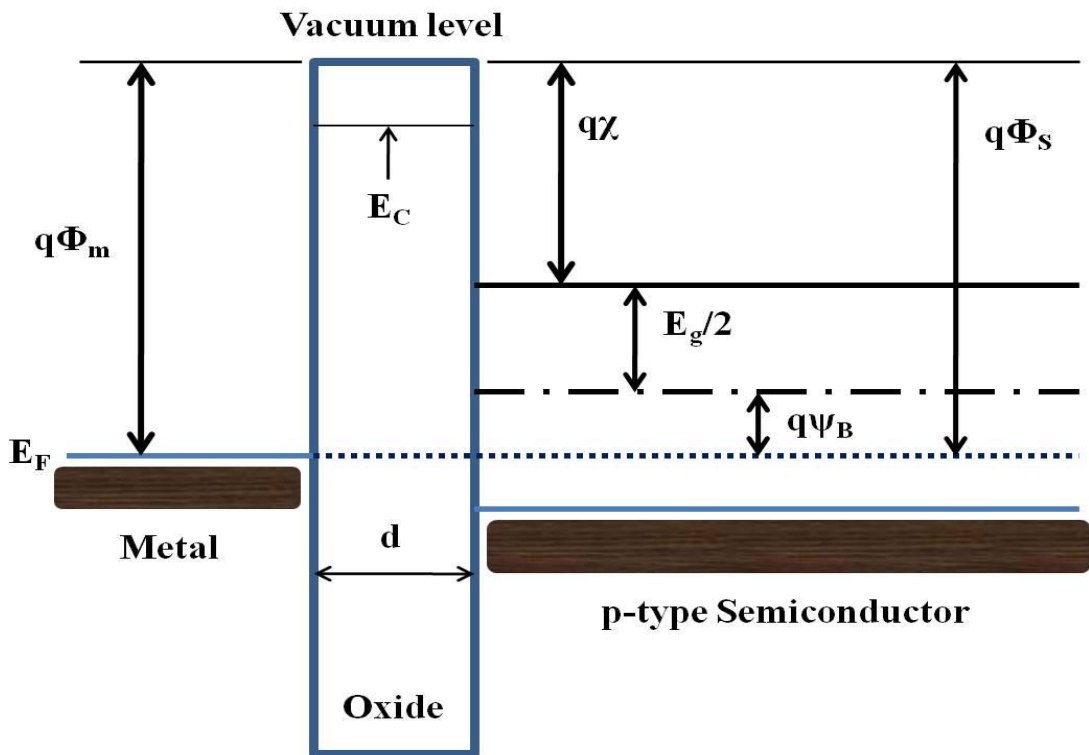
Fig. 2-2 Energy band diagram of an ideal MOS capacitor at $V_G=0$ [14]
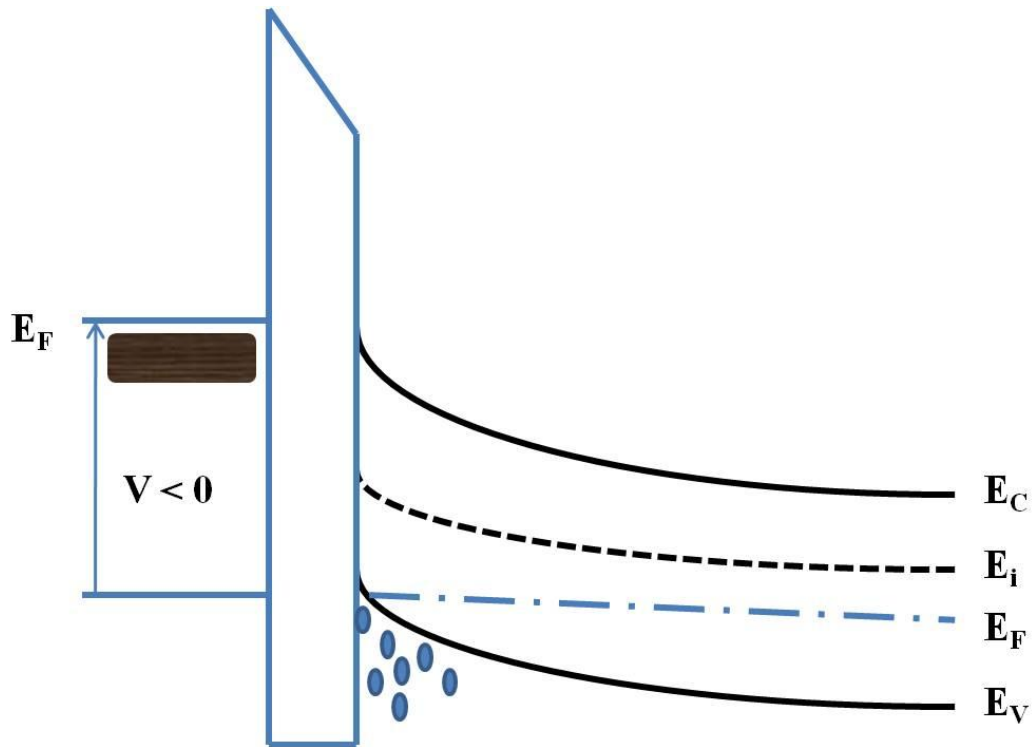
Fig. 2-3 Energy band diagram of an ideal MOS capacitor in accumulation region [14]
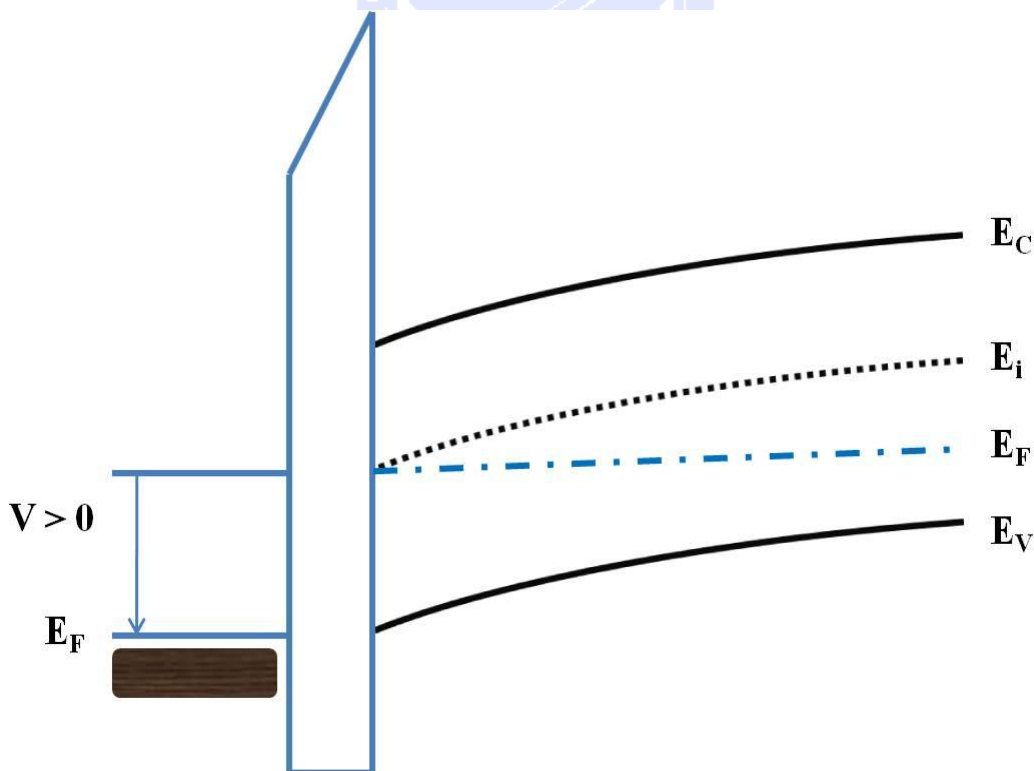
Fig. 2-4 Energy band diagram of an ideal MOS capacitor in depletion region [14]
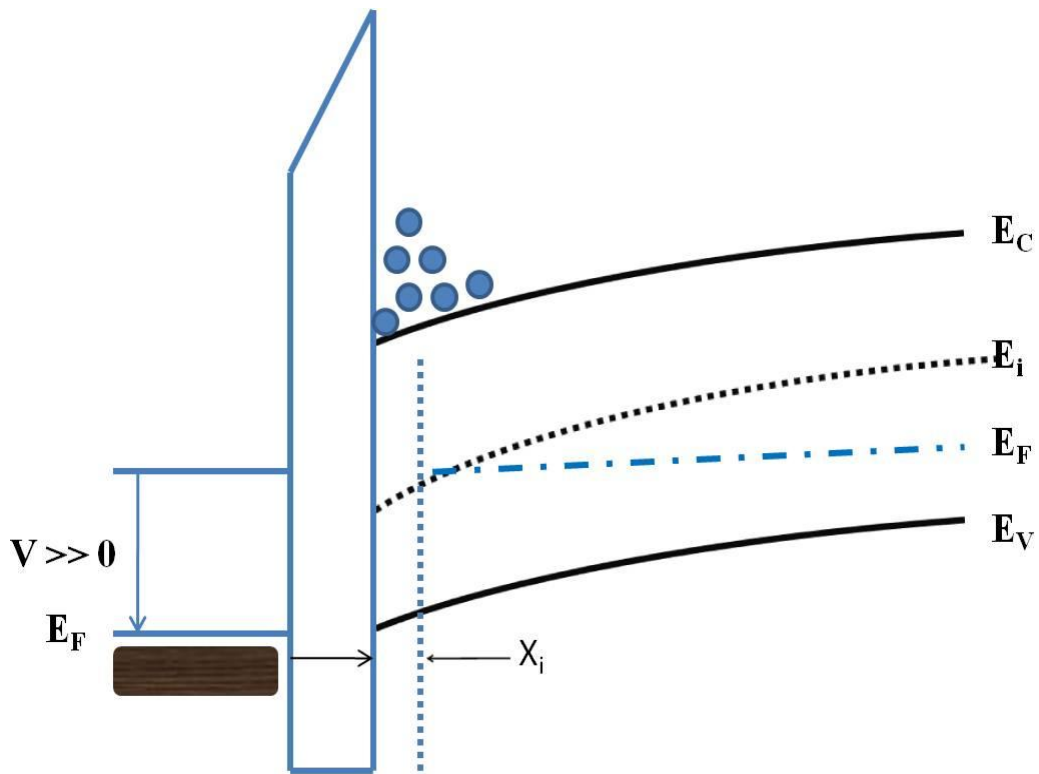
Fig. 2-5 Energy band diagram of an ideal MOS capacitor in inversion region [14]
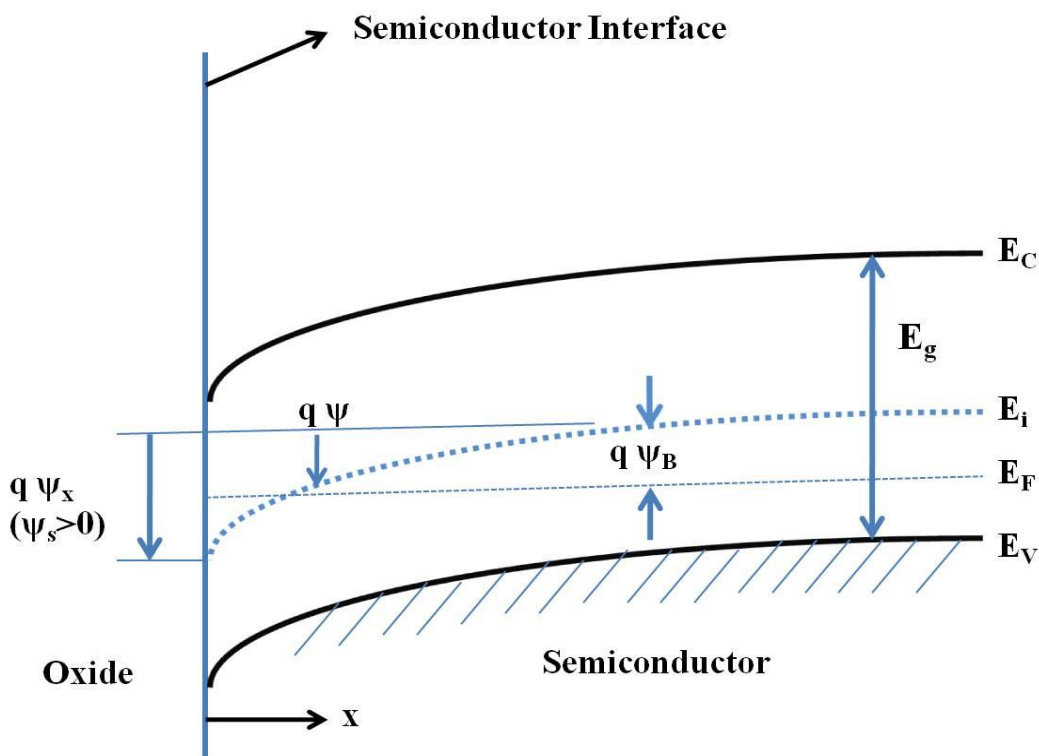
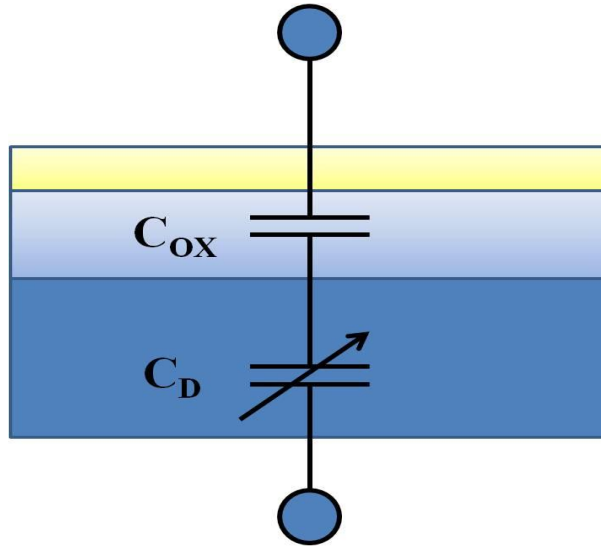Fig. 2-6 Energy band diagrams at the surface of a p-type semiconductor [14]

Fig. 2-7 Cross section of an MOS capacitor showing a simple equivalent circuit of oxide capacitance C_{OX} and semiconductor capacitance C_D in series [14]

p-type semiconductor

n-type semiconductor
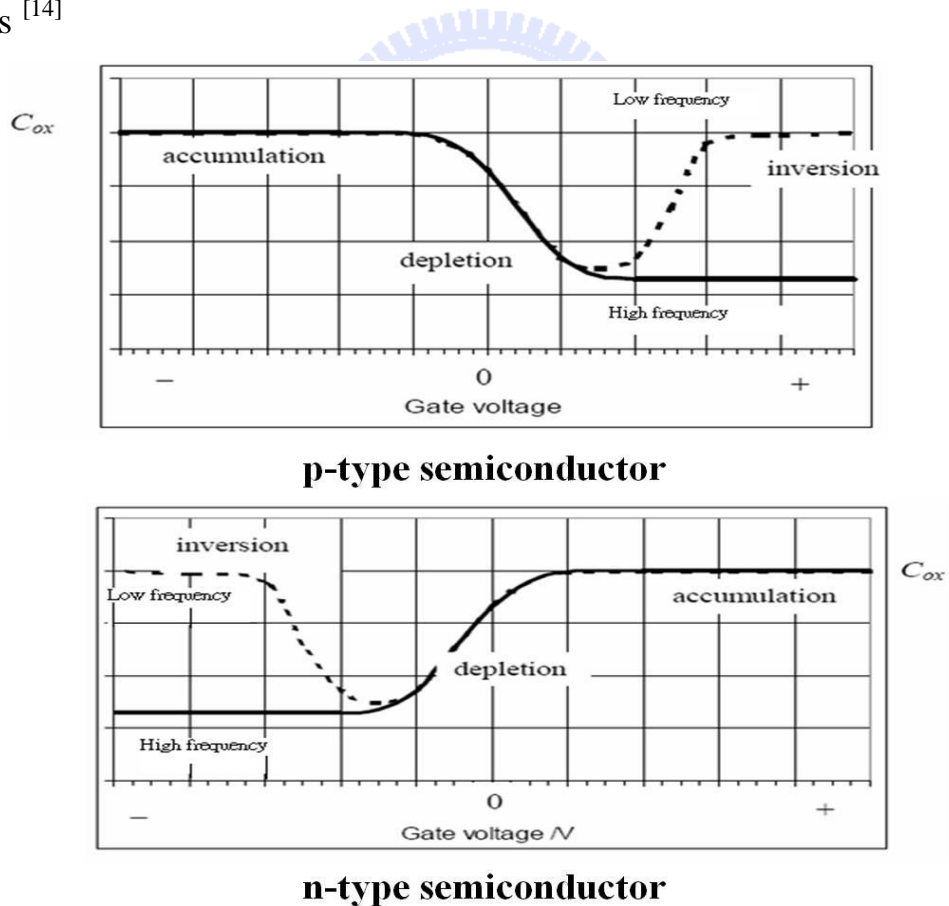
Fig. 2-8 Capacitance versus gate voltage curve for accumulation, depletion, inversion at high and low frequency
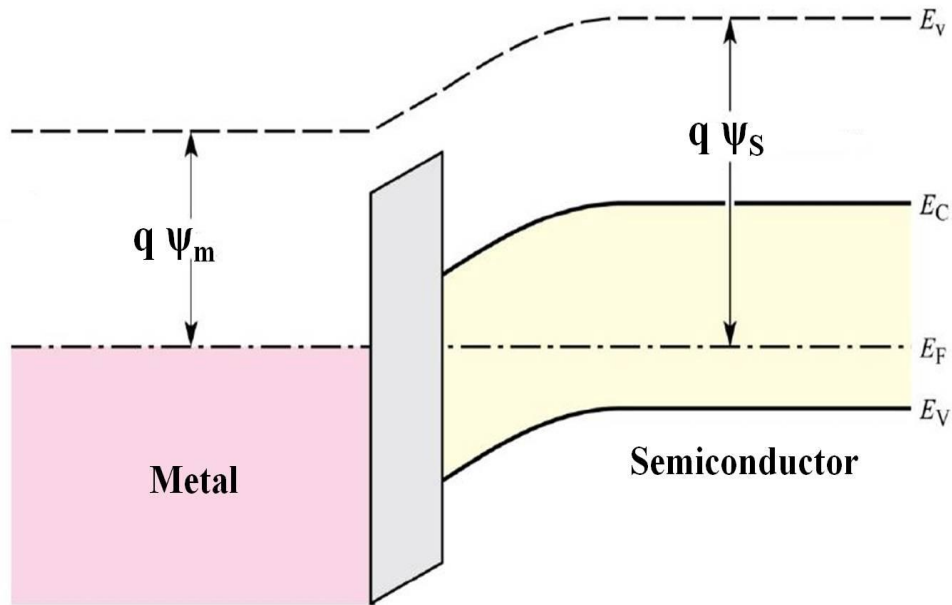
Fig 2-9 Energy band diagram for a MOS capacitor in thermal equilibrium
[14]
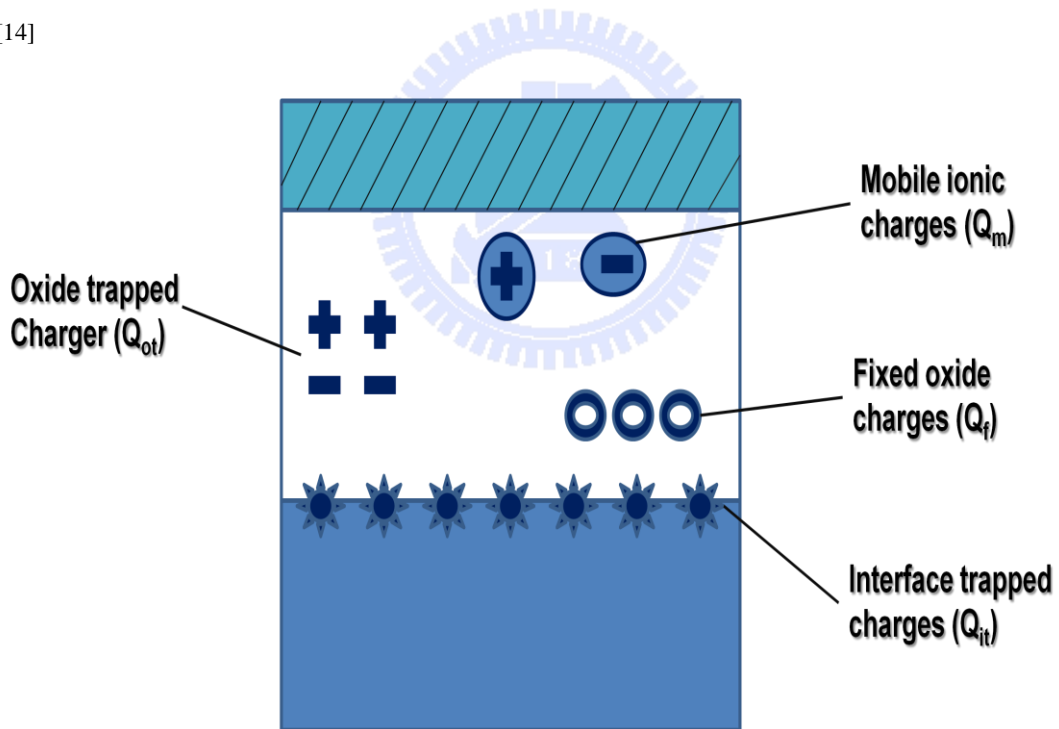
Fig 2-10 Different kinds of trap charges distribution in MOS structure [14]
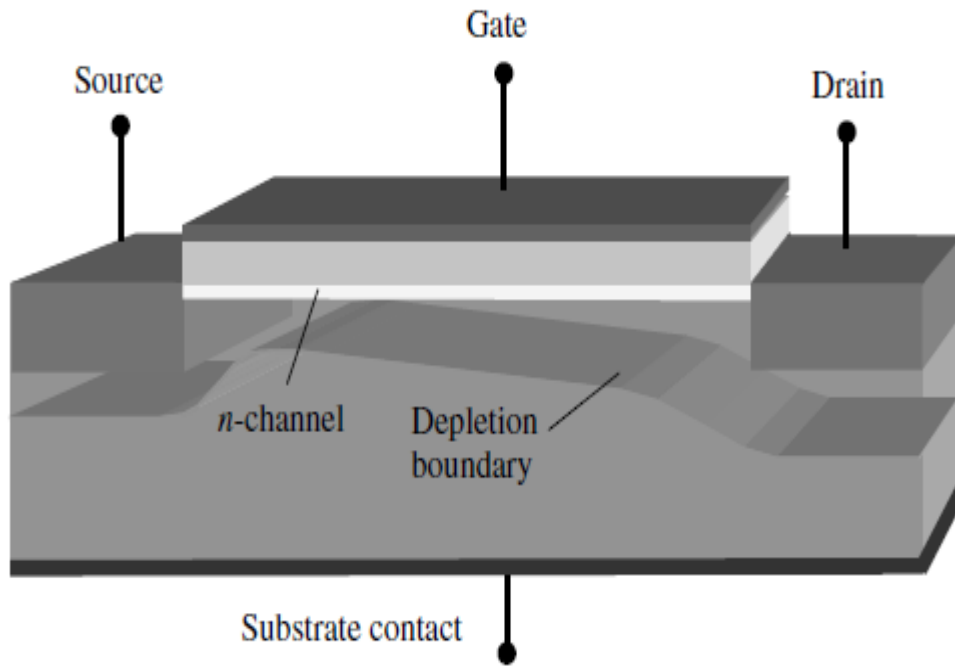
Fig 2-11 Basic structure of Metal-Oxide-Semiconductor Field Transistor (MOSFET) [15]
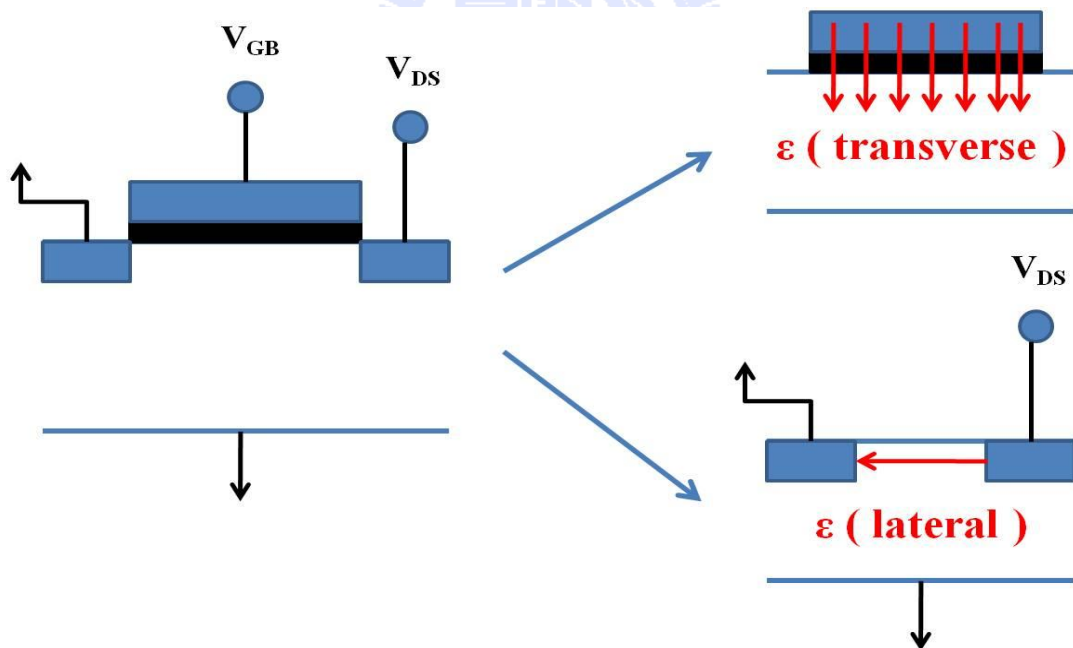
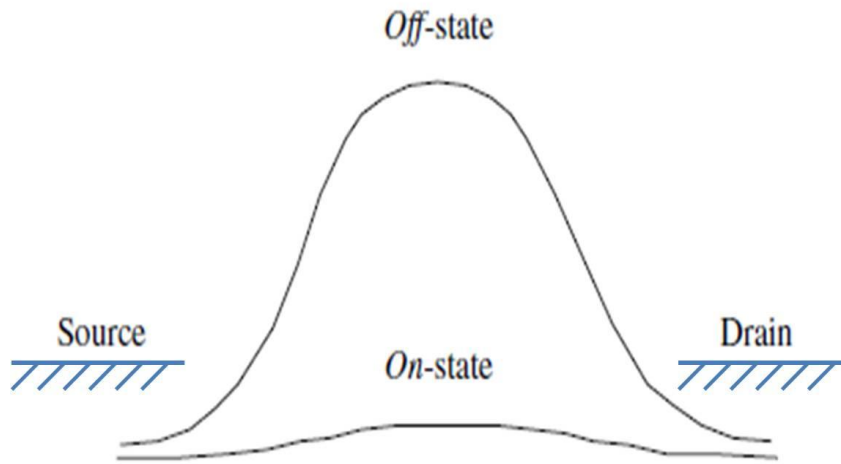Fig. 2-12 Transverse electron field and lateral electron field in MOSFET

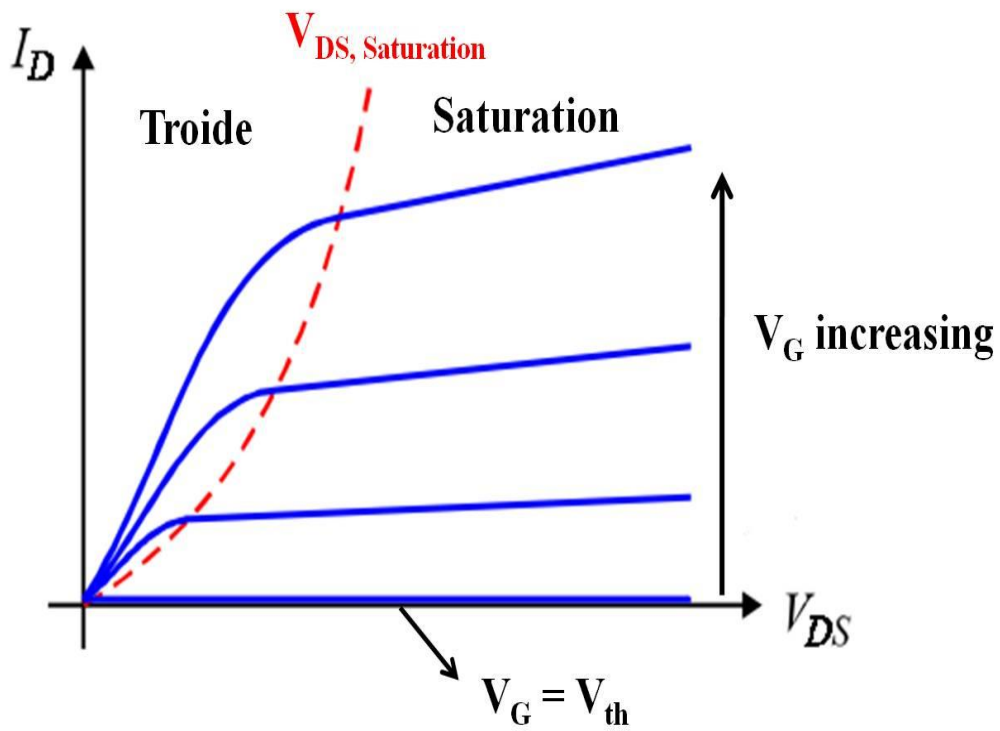Fig 2-13 Barrier heights between the source and drain of *on-* and *off*-states [15]

Fig 2-14 The I_D-V_D characteristic of enhancement-mode n-MOSFET

Table 2-1 Four types of MOSFET modes [14]

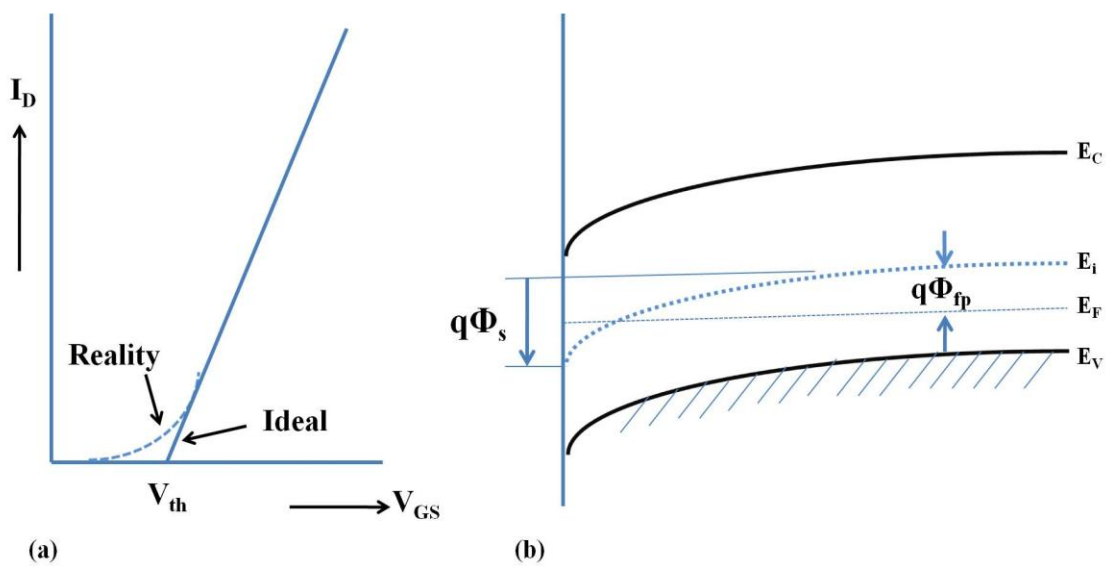| Type	Cross Section	Output Characteristics	Transfer Characteristics
n-Channel Enhancement (Normally Off)			
n-Channel Depletion (Normally On)			
p-Channel Enhancement (Normally Off)			
p-Channel Depletion (Normally On)			

Fig.2-15 (a) The I_D-V_{GS} curve of reality and ideal MOSFET [16] (b) The band diagram of a p-type substrate MOSFET [16]

Chapter 3

High-k oxide on III-V MOS structure

3.1 The requirements of high-k dielectrics oxide

(A) Dielectric constant

Dielectric constant is the most important parameter for dielectrics oxide material used in the MOS structure. Due to the reducing of chip's size in the future, the horizontal electrical field is increasing and the gate modulation ability is decreasing. In order to solve these problems, the capacitance per unit area must be improved to decrease the effect of unwanted electrical field.

$$C = \frac{Q}{V} \tag{3-1}$$

Where C: Capacitance, Q: Charges, V: Turn on voltage

$$C = \varepsilon_0 \varepsilon \frac{A}{d} \ , \ \varepsilon \propto C \tag{3-2}$$

Where C**:** Capacitance, **ε:** Dielectric constant of oxide

A: Cross section area, d: The distance between the two plate

According to equation (3-1), the devices with larger accumulation capacitance can be turn on more easily by a smaller voltage. Using smaller operating voltage will result in higher device efficiency and cost saving. According to the equation (3-2), the MOS device which is using oxide material with larger dielectric constant as its gate dielectric will has larger accumulation capacitance. So, the high-k oxide is needed for III-V MOS devices technology. The energy band gap versus dielectric

constants diagram of different oxide materials is shown in Fig. 3-1.

(B) Energy band gap

The energy band gap of oxide materials is an important factor which influences the leakage current of the MOS devices. The oxide with smaller energy band gap causes the carrier tunneling more easily; it will induce unwanted leakage current to influence the devices performance. The oxide with larger energy band gap can prevent the carriers tunneling. But, the oxide with higher dielectric constant will have the smaller energy band gap. So, it is important to find the suitable oxide to improve the MOS devices performance. Several gate oxide candidates are listed in Table 3-1. Besides, the ***band offset*** of oxide on semiconductor material is also needed to be considered, the value must be exceed 1eV so that the oxide can act as an effective insulator [18]. The predicted band offset of InAs and HfO_2 which are used in this study shown in Fig. 3-2.

(C) Interface quality

Interface quality between the oxide and III-V semiconductor is another important key issue and has been researched for many years. Unlike silicon, the III-V materials don't have their own native oxide which results in very high ***interface state density (D_{it})***, it is usually higher than silicon MOS devices. This is the main problem for III-V material interface because of the – ***Fermi level pinning effect***. The high interface state density will pin the Fermi level and trap the unwanted charges at the interface, it will cause the devices failure or results in unwanted shift or stretch out for CV curve in capacitance – gate voltage measurement.

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Besides, the native oxide which is produced by III-V material will also influence the interface quality, so the pretreatment before high-k dielectric oxide deposition on III-V semiconductor is needed. The progress of vacuum technology and new methods for depositing high-k dielectrics, like Atomic Layer Deposition (ALD) and Molecular Beam Epitaxy (MBE), can also provide the better interface quality.

(D) Thermal stability

The thermal stability of oxide is also needed to be considered for gate dielectrics oxide materials. The oxide with higher thermal stability can prevent the unwanted phase transformation after high temperature process like post deposition annealing (PDA). To reduce current leakage and improve charge storage capacity, the amorphous type or single crystalline gate dielectrics with high re-crystallization temperature are required.

3.2 The factors to determine the MOS device's performance

3.2.1 Capacitance – Gate voltage measurement

To obtain the capacitance- gate voltage characteristic, probing system with LCR impedance analyzer can be used. The frequency dependence CV curves can be plotted by changing the frequency of the supplied AC signal. The parameters which are often used to determine the device performance and can be observed in the C-V characteristic measurement are described below:

(A) Flat band voltage

Flat band voltage is one of the important factors because it determines the gate voltage at which there are no charge occurred in the semiconductor. The ideal flat band voltage can be determined by setting the work function difference in the simulation tool and assuming there are no existing trap charges existing in the oxide or at oxide/semiconductor interface. It separates the accumulation and depletion conditions. By comparing the flat band capacitance between the simulated and measured curves, the shift of flat band voltage ΔV_{FB} can be observed and the oxide quality can be determined.

(B) Equivalent oxide thickness (EOT)

EOT is defined as:

$$EOT = \frac{t_{ox} \times k_{SiO2}}{k} \tag{3-3}$$

This parameter is used to characterize how a given dielectric material can achieve the same capacitance of thin SiO_2 layer with thicker physical thickness. The oxide with larger dielectric constant can achieve the lower EOT with thicker thickness to reduce the device leakage current reducing.

(C) Hysteresis

Hysteresis is measured by sweeping the gate voltage forth and back. The amount of hysteresis stands for the amount of charges trapped by the defects in the oxide, thus it can be used to determine the oxide quality. The defects extracted from hysteresis are also called slow trapping states, where the interface traps are fast trapping states. The counterclockwise hysteresis implies the positive charges were trapped by the defects; on the

other hand, the clockwise hysteresis implies the negative charges were trapped.

(D)Frequency dispersion

Frequency dispersion is the phenomenon of accumulation capacitance varying with operation frequency. In silicon MOS capacitors, it is due to leakage current of ultra thin oxide which making the capacitor cannot storage charge, causing the total capacitance decrease. For high-k/III-V case, the oxide thickness is not as thin as silicon MOS devices; the frequency dispersion is caused by the poor interface quality where large amounts of interface traps exist at the semiconductor surface. The interface traps are frequency dependent; it will capture and emit charges to distort the C-V curves causing frequency dispersion, even to cause the devices failure.

3.2.2 Methods of evaluating the interface trap density (D_{it})

The interface quality is always the biggest challenge for III-V MOS devices. The most direct factor of reflecting this situation is the interface trap density which is called D_{it}. The larger D_{it} value results poor interface quality. It could cause the devices performance degradation or even failure.

Some methods have been utilized to evaluate the D_{it}. For example, low frequency method (quasi-static method), high frequency method (Terman method), charge pumping and conductance method. The first two methods use the capacitance-voltage relationship to extract the D_{it}, the equivalent components models includes: oxide capacitance, depletion

layer capacitance and interface-trap capacitance. Since the depletion-layer capacitance is in parallel with interface trap capacitance, difference in capacitance must be calculated, which leads to inaccuracies in extracting the information of interface state. Furthermore, although the low frequency quasi-static method was the most common one for dielectrics with low leakage current, but with extremely shrinkage of device size, the leakage current associated with direct tunneling through a thin oxide makes the measurement difficult to perform. Charge pumping is very sensitive to the interface states but it requires fully processed MOSFET device.

3.2.3 Extract D_{it} from conductance method

Nicollian and Goetzberger of Bell Lab. gave a detailed and all-inclusive discussion for the conductance method in 1967 about the conductance directly relating to the interface traps, which can give more accurate results. The data extraction is based on the measurement of the *equivalent parallel conductance*, G_P, of a MOS capacitor as a function of bias voltage and frequency as shown in Fig. 3-3. The conductance representing the loss mechanism from interface trap, capturing and emitting carriers, is an index of the interface trap density. Fig. 3-4 shows the equivalent circuit of the measurements, where C_{OX}, C_S, C_{it}, represent oxide capacitance, semiconductor capacitance and interface trap capacitance respectively.

The above assumption neglected the series resistance of substrate and oxide leakage current. From the measured capacitance C_m and

conductance G_m, the parallel conductance G_P is given by equation (3-4), and D_{it} is given by equation (3-5),

$$\frac{G_P}{\omega} = \frac{\omega G_m C_{OX}^2}{G_m^2 + \omega^2 (C_{OX} - C_m)^2} \tag{3-4}$$

$$D_{it} = \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{max} \tag{3-5}$$

Where $(G_P/\omega)_{max}$ is the peak value from a G_P/ω-frequency plot.

Because the actual device has the series resistance from thin oxide and leaky oxide. The equivalent circuit is converted to Fig. 3-5(d) with G_t stands for tunnel conductance and r_s stands for series resistance. Equation (3-4) becomes

$$\frac{G_P}{\omega} = \frac{\omega C_{OX}^2 (G_c - G_t)}{G_c^2 + \omega^2 (C_{OX} - C_c)^2} \tag{3-6}$$

Where

$$C_c = \frac{C_m}{(1 - r_s G_m)^2 + (\omega r_s C_m)^2} \qquad G_c = \frac{\omega^2 r_s C_m C_c - G_m}{r_s G_m - 1} \tag{3-7}$$

The series resistance is determined by biasing the device into accumulation region

$$r_s = \frac{G_{ma}}{G_{ma}^2 + \omega C_{ma}^2} \tag{3-8}$$

Where C_{ma} and G_{ma} are the measured capacitance and conductance in accumulation. The tunnel conductance G_t is determined from G_c by setting the $\omega \to 0$

$$G_c = \frac{G_m}{1 - r_s G_m} \tag{3-9}$$

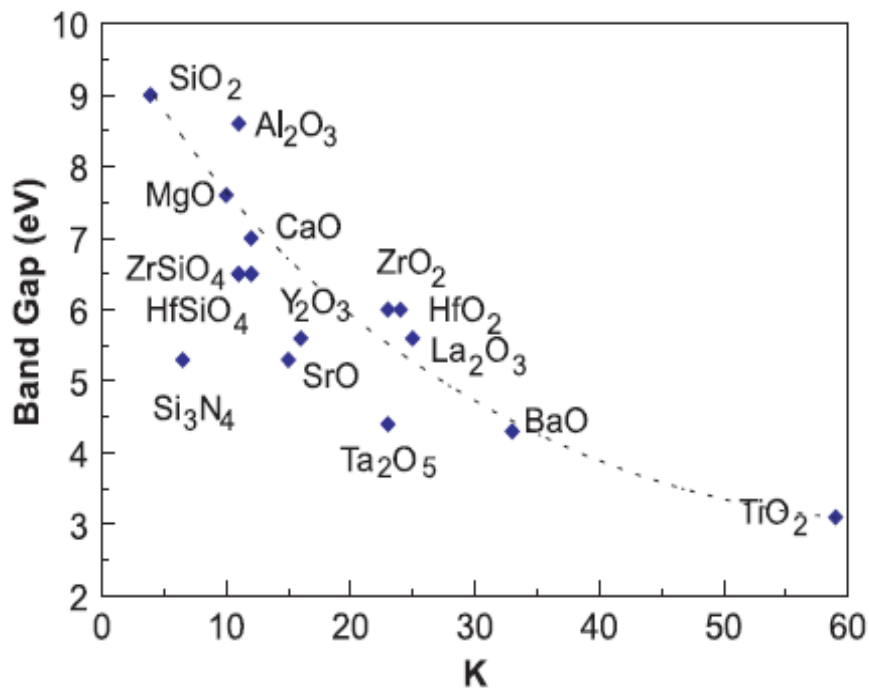For r_s and G_t equal to 0, equation (3-6) reverts to equation (3-4).

Fig. 3-1 Energy band gap versus Dielectric constant diagram of oxides [17]

Table 3-1 Comparison of the gate oxide's properties

Material	Dielectric Constant	Energy Band Gap(eV)	Crystal Structure
SiO_2	3.9	8.9	Amorphous
Si_3N_4	7	5.1	Amorphous
Al_2O_3	9	8.7	Amorphous
Y_2O_3	15	5.6	Cubic
HfO_2	25	5.5	Mono., tetrag., cubic
ZrO_2	25	7.8	Mono., tetrag., cubic
Ta_2O_5	26	4.5	Orthorhombic
La_2O_3	30	4.3	Hexagonal, cubic
TiO_2	80	3.5	Tetrag.
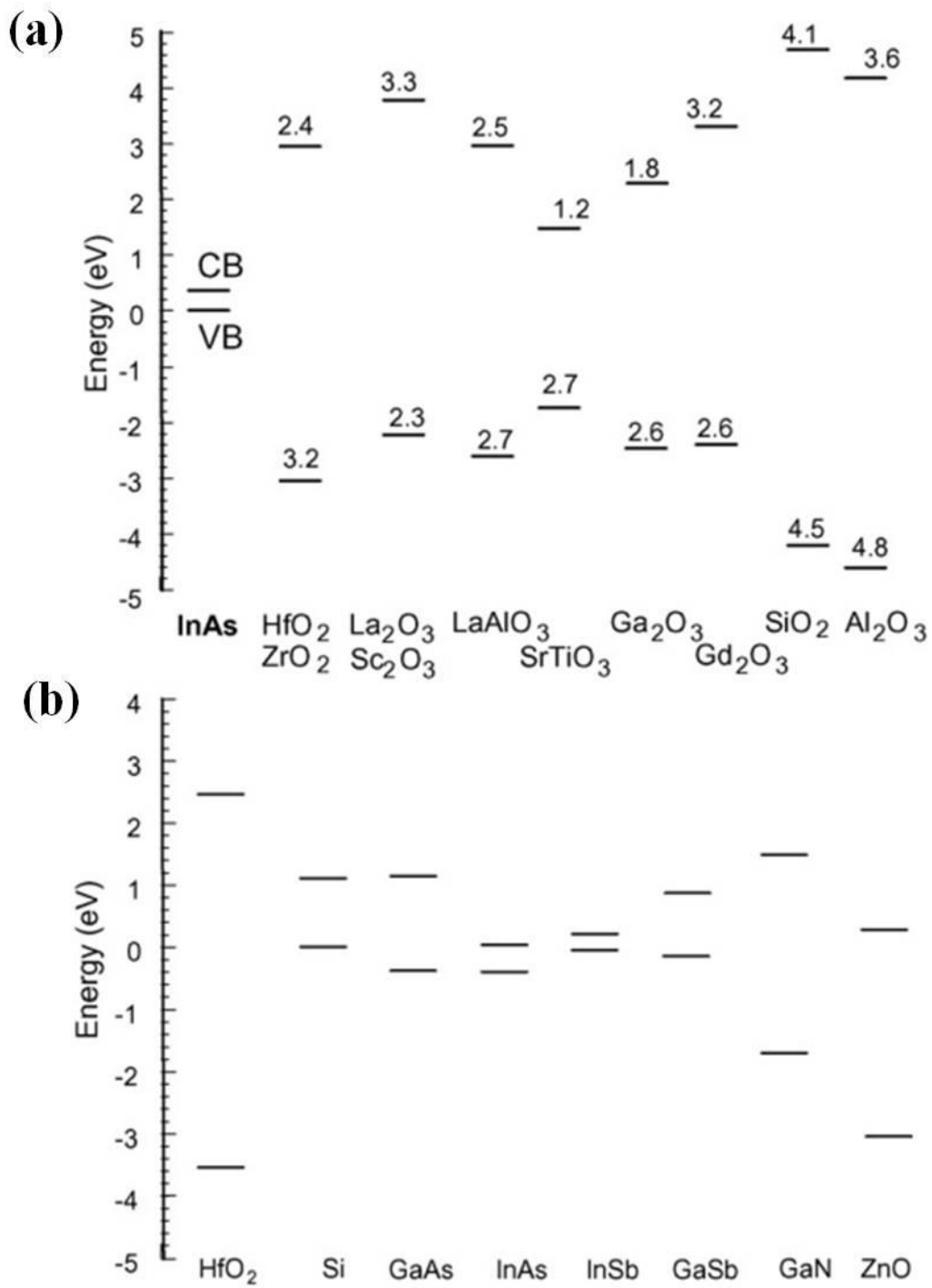
Fig. 3-2 (a) Predicated band offsets on InAs (b) Predicated band offsets on HfO$_2$ [18]
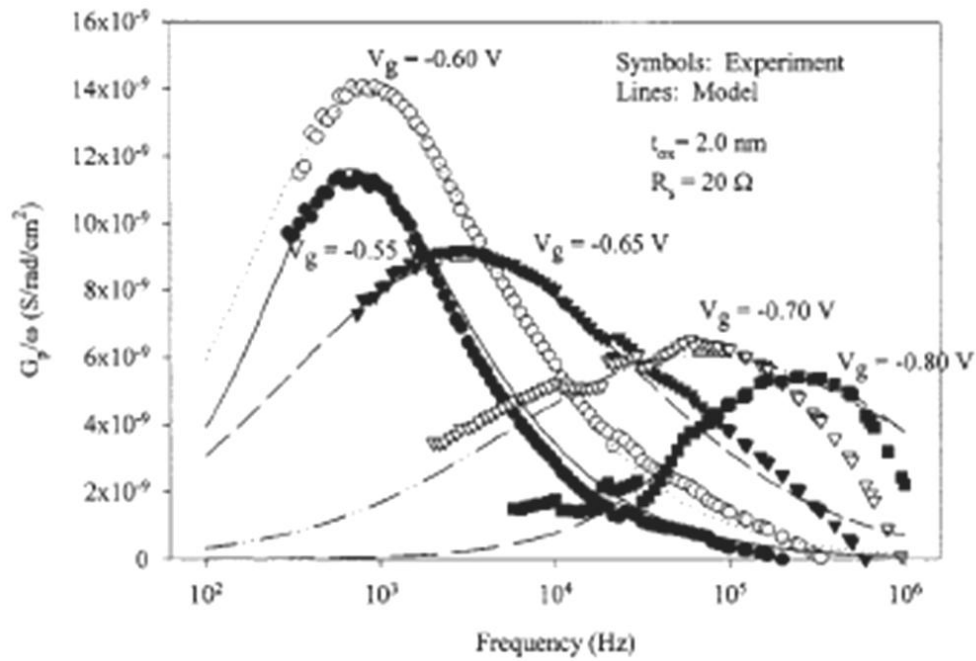
Fig.3-3 Schematic experimental and modeled interface state conductance [19]
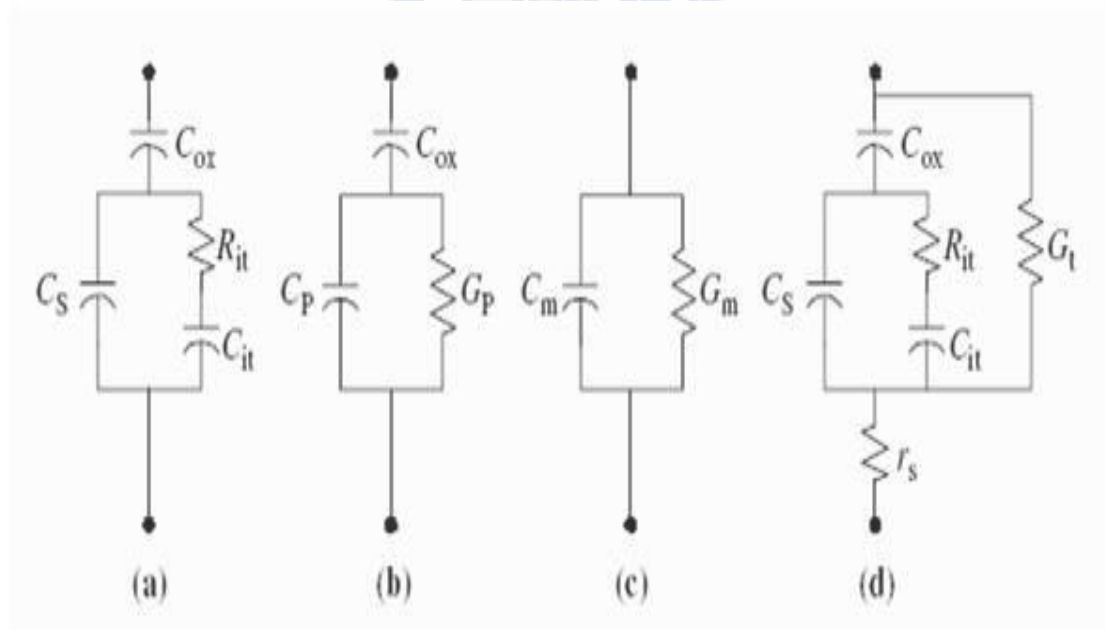
Fig 3-4 Equivalent circuits for conductance measurement: (a) MOSCAP with interface trap time constant $\tau_{it}=R_{it}C_{it}$, (b) simplified circuits of (a), (c) measured circuit, (d) including series r_s resistance and tunnel conductance G_t [20]

Chapter4

Experimental process

In this chapter, the devices epitaxy structure and the complete fabrication process flow of III-V MOS capacitor and III-V MOSFET are introduced.

4.1 MOS capacitor

4.1.1 Devices structure

The first structure is used 3nm Be-doped n-$In_{0.53}Ga_{0.47}As$ and 10nm Be-doped p-$In_{0.7}Ga_{0.3}As$ as buffer layer growth on the InP substrate and the channel layer was Si-doped n-InAs. The front metal electrode is 50nm Ni and backside metal is 50nm Au. The second structure is used 50nm Be-doped n-$In_{0.53}Ga_{0.47}As$ as buffer layer growth on the InP substrate and the channel layer was Be-doped p-$In_{0.7}Ga_{0.3}As$. The front metal electrode is 50nm W and backside metal is 50nm Au. The original epitaxy structure is shown in Fig. 4-1.

4.1.2 Devices process flow

(a) Wafer cleaning

The first step of the process is wafer cleaning, the wafer are immersed by 50% HF solution to remove the native oxide and unwanted particles on the surface.

(b) Surface pretreatment

Surface pretreatment is a very important step before oxide deposition; it

can remove the unwanted native oxide at the surface which will influence the devices performance. After the pretreatment, the native oxide is eliminated and a thin passivation layer form at the top of the devices, it can prevent the reaction between the oxygen in atmosphere and semiconductor.

The wafer are immersed in $(NH_4)_2S$ surface pretreatment solution for 30 minutes at room temperature. The immersing time and solution temperature both could influence the depth of the thin passivation layer.

(c) High-k dielectric deposition by MBE (Molecular Beam Epitaxy)

After the surface pretreatment, the wafers are entered into the MBE chamber immediately to prevent the unwanted reaction between the oxygen and semiconductor.

Several high-k oxides were chosen for gate dielectric by MBE deposition. The RTA (Rapid Thermal Annealing) was used to improve the oxide-semiconductor interface quality after MBE deposition.

(d) Electrode metal formation

W (tungsten) is deposited on the wafer by sputtering as gate contact metal. Finally, Au (gold) is deposited by sputtering on the backside of the n^+InP substrates to form ohmic contacts.

The complete process flow chart of MOS capacitor is shown in Fig. 4-2.

4.2 MOSFET

4.2.1 Devices process flow

(a) Wafer cleaning

The first step of the process is wafer cleaning, the wafer are immersed by ACE and IPA, each for 5 minutes to remove the unwanted particles and contaminate, and then use the blowing nitrogen gas to dry the wafer.

(b) Mesa isolation

The active regions of device are defined by S1818 photo resist. The mesa isolation is carried out by $H_3PO_4:H_2O_2:H_2O$ (5:1:40) solution to etch the $In_xGa_{1-x}As$ layer and the etching depth reached about 5000Å .

(c) Surface pretreatment

The wafer are immersed by $HCl:H_2O$ (1:4) solution to remove the native oxide at the surface, following by dipping the wafer in $(NH_4)_2S$ surface pretreatment solution for 30 minutes at room temperature. The immersing time and solution temperature both could influence the depth of the thin passivation layer.

(d) High-k dielectric deposition by MBE (Molecular Beam Epitaxy)

The wafers are entered into the MBE chamber immediately after surface pretreatment to prevent the unwanted reaction between the oxygen and semiconductor.

After high-k deposition, the post deposition annealing (PDA) is used for improving the interface quality.

(e) Implant

The implant region is defined by ohmic exposure process first, and then used silicon doping implant which was prospected to improve the ohmic contact and reduced the resistivity.

(f) Source and drain region formation

The wafers are dipped in HCl:H_2O (1:4) solution for 2 minutes to remove the oxide of source and drain region. After etching, the wafers are loaded into the E-gun chamber to deposit the ohmic metal (Au/Ge/Ni/Au) immediately.

(g) Metal gate formation

Gate location is defined by E-Beam Lithography System. After definition, the wafers are used ICP system to remove the remnants photo resist and dipped into HCl:H_2O (1:4) solution to eliminate the native oxide , then put the wafer into the E-Gun chamber for Ti/Pt/Au metal deposition. The complete process flow of MOSFET is shown in Fig. 4-3.
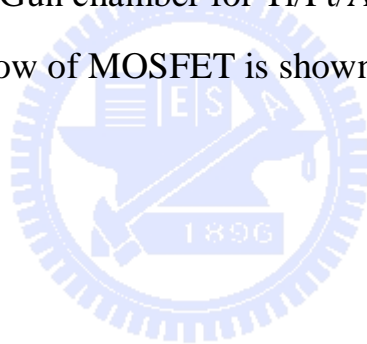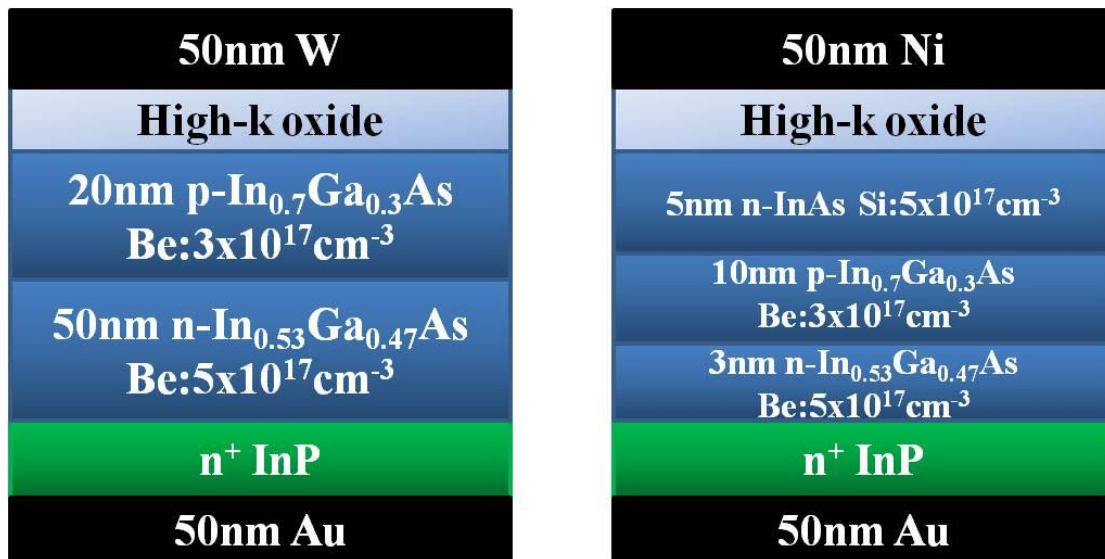
Fig. 4-1 Original epitaxy structure of MOS capacitors
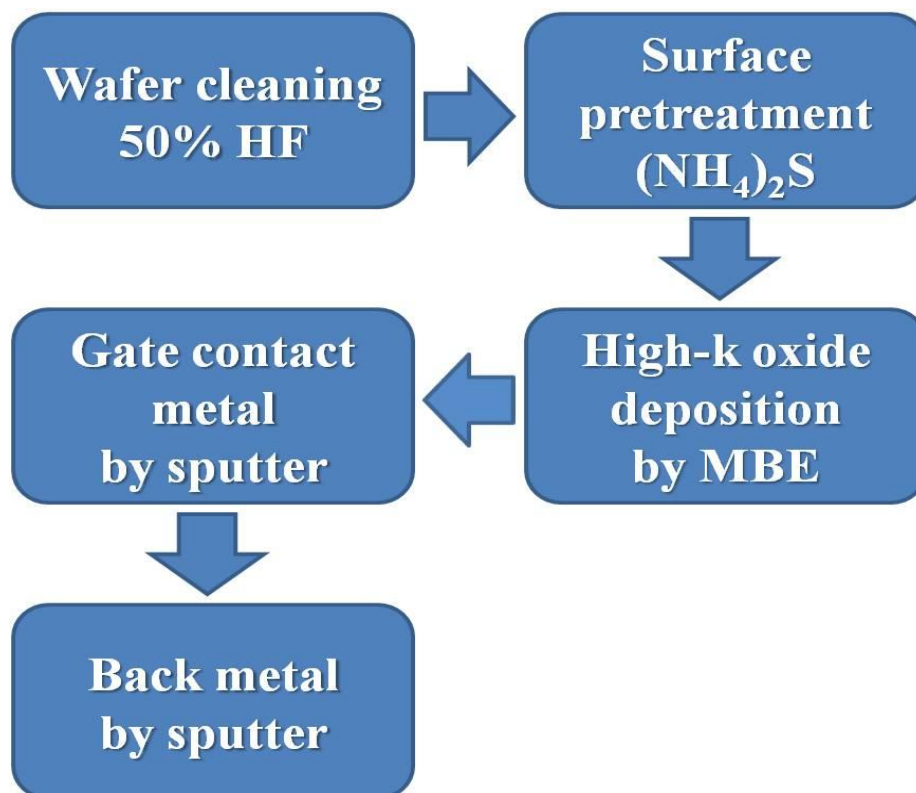
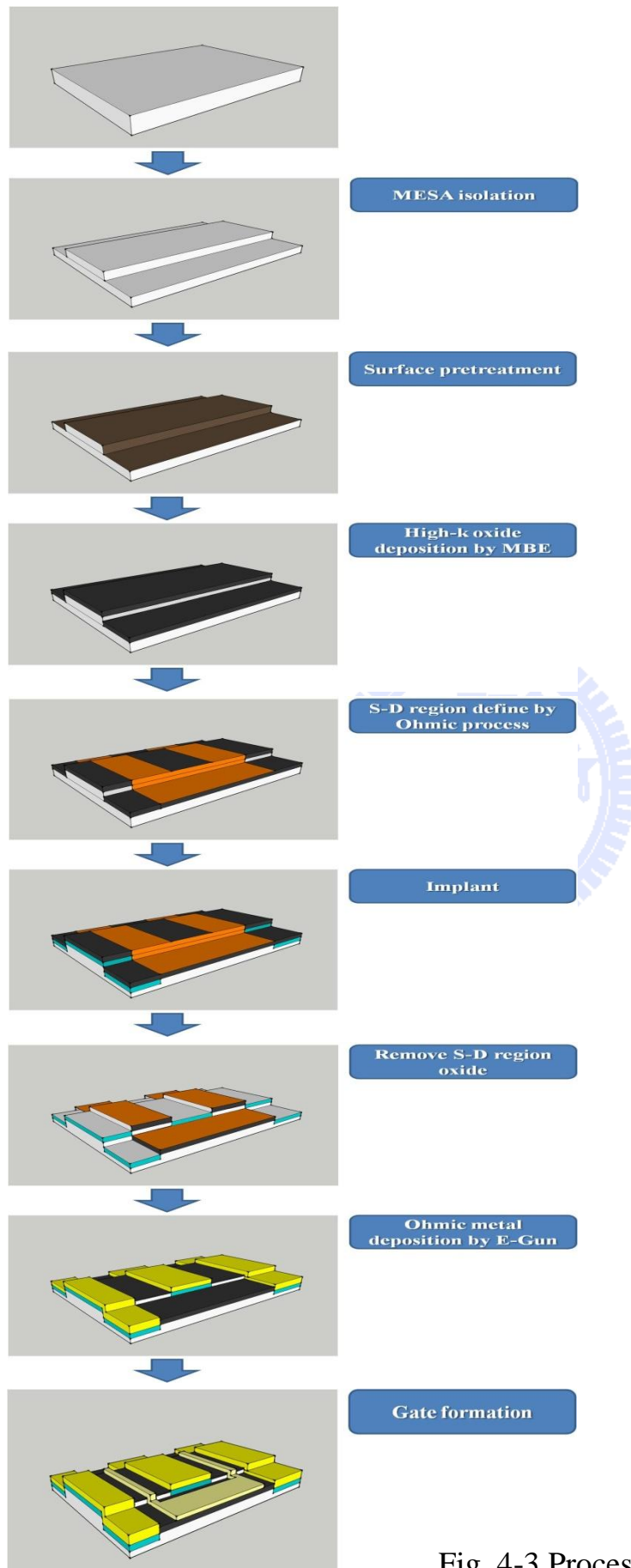Fig. 4-2 Process flow of III-V MOS capacitor

Fig. 4-3 Process flow of III-V MOSFET

Chapter 5

Results and discussion

5.1 Study of high-k/ III-V MOS capacitor

In this chapter, the HfO_2/InAs MOS capacitor was fabricated first. In order to increase the device capacitance, CeO_2/HfO_2 gate stack MOS capacitor was introduced. The experimental results will be discussed in this chapter.

5.1.1 HfO$_2$/n-InAs MOS capacitors with different Post Deposition Annealing (PDA) temperatures

Among the III-V material, InAs shows more potential as channel layer due to its high electron mobility and drift velocity. High indium content InGaAs materials also show better interface quality than GaAs[21]. Based on the sufficient band offsets and thermal stability of HfO_2 material, HfO_2 was chosen as gate dielectric for InAs MOS capacitor. Different PDA temperatures were performed of the results were compared in this study.

For comparison, the HfO_2/n-$In_{0.7}Ga_{0.3}As$ MOS capacitor was also fabricated. The cross-sectional transmission electron microscopy (TEM) images of these two capacitors are shown in Fig. 5-1. With the similar process, there is less interface oxide formation between the HfO_2 and n-InAs as compared to HfO_2/n-$In_{0.7}Ga_{0.3}As$ MOS capacitor.

The Capacitance-Gate voltage characteristics of 15nm HfO_2/n-InAs with various PDA temperatures of $400^{o}C$, $450^{o}C$, $500^{o}C$ and $550^{o}C$ are shown

in Fig. 5-2. The capacitance was reduced when the PDA temperature was increased. At 400$^\text{o}$C, there was no obviously saturation in the inversion region which might be caused by the native oxides at the interface. When PDA temperature increased to 450$^\text{o}$C, the native oxides at the interface was reduced which results in more obviously saturation in the inversion region.

Fig. 5-3 shows the hysteresis behavior for the HfO$_2$/n-InAs MOS capacitors at 100 kHz after annealing at different temperatures. The flat band voltage at 100 kHz shift to a more negative value with the increase of PDA temperature between 400$^\text{o}$C to 500$^\text{o}$C. The flat band voltages are 2.15 V at 400$^\text{o}$C, 1.32 V at 450$^\text{o}$C, 1.11 V at 500$^\text{o}$C. It indicates that the oxide charge was reduced as the PDA temperature was increased from 400$^\text{o}$C to 500$^\text{o}$C. The capacitance at flat band condition decreased with increasing annealing temperature as following: 0.68μF/cm^2 at 400$^\text{o}$C, 0.62μF/cm^2 at 450$^\text{o}$C, 0.61μF/cm^2 at 500$^\text{o}$C, 0.61μF/cm^2 at 550$^\text{o}$C. Besides, Fig. 5-3 also shows the voltage hysteresis improved when the PDA temperature was increased, resulting in the following values: ΔV= -278mV at 400$^\text{o}$C, ΔV= 189mV at 450$^\text{o}$C, ΔV= 37mV at 500$^\text{o}$C. However, as the PDA temperature was increased to 550$^\text{o}$C, Indium started to diffuse into HfO$_2$ and the hysteresis became worse (ΔV= -288 mV).

Fig. 5-4 shows the XPS spectra of the HfO$_2$/n-InAs MOS capacitors with different PDA temperatures from 400$^\text{o}$C to 550$^\text{o}$C. There are three values of In3d$_{5/2}$ for InO$_x$, In$_2$O$_3$ and InAs and two values of As3d of As$_2$O$_3$ and InAs observed. It was found that the amount of InO$_x$ and As$_2$O$_3$ decreased when the PDA temperature was increased from 400$^\text{o}$C to 450$^\text{o}$C as

observed from the XPS result. When the PDA temperature was increased to $500^{o}C$, no clear As_2O_3 peak was observed, and the device had the best hysteresis value of ~ 37mV. When PDA temperature was increased up to $550^{o}C$, a small amount of In diffused into HfO_2 and both In_2O_3 and InOx amount increased as observed from the XPS data. The interface-trap densities (D_{it}) of the capacitors with different PDA temperatures were estimated by conductance method and the results are listed in Table 5-1. It shows that the MOS capacitor with PDA temperature of $500^{o}C$ has the lowest D_{it} of 2.7×10^{12} $cm^{-2} eV^{-1}$ among all the temperatures studied. The leakage current for the 15nm HfO_2 n-InAs MOS capacitors after $500^{o}C$ annealing was less than $1 \times 10^{-5} A/cm^2$ when the bias voltage was between -3.5 V to 3.5 V.

Comparing the C-V characteristics, lower PDA temperature results in higher oxide capacitance, but the difference is not significant. When PDA temperature increased to $500^{o}C$, the device has the lowest hysteresis and lowest D_{it} for all the PDA temperatures studied in this work. When the PDA temperature was increased to $550^{o}C$, In diffused into HfO_2 and results in more Indium oxide formation, and thus both D_{it} and hysteresis values increased and the oxide capacitance decreased.

In the following sections, CeO_2 was used as gate dielectric to improve the MOS capacitance and the CeO_2/HfO_2 gate stack structure is introduced.

5.1.2 Improvement of the capacitance by using CeO_2 as gate oxide on $In_xGa_{1-x}As$ MOS capacitors

CeO_2 has relatively large dielectric constant about 38 and shows the

potential as gate dielectric for $In_xGa_{1-x}As$ MOS capacitor, but it has the small energy band gap of only about 3.2eV.

CeO_2 was deposited directly on $In_{0.7}As_{0.3}As$ with various PDA temperatures from 400^oC to 500^oC. The C-V characteristic is shown in Fig. 5-5.

As we can see from the C-V characteristic, there is no obviously accumulation region and the capacitance increased very rapidly with the increase gate voltage at low frequency, especially for 1kHz. This phenomenon might be caused of high trap density at the oxide/semiconductor interface and the space charge in the CeO_2 layer [22-23]. This phenomenon could also be observed in the CeO_2/silicon capacitor case [22]. The space charges were strongly frequency dependent. It could induce the leakage current in the oxide layer and degraded the capacitor's performance.

We can see the variation of C-V characteristics with various PDA temperatures. The frequency dispersion increased as temperature increased. According to the energy dispersive X-ray spectroscopy (EDX) data at PDA temperature of 500^oC as shown in Fig. 5-6, the elements of the channel material including In, Ga and As have diffused to the CeO_2 layer resulting in larger frequency dispersion. The diffusion was more seriously with higher PDA temperature. The transmission electron microscopy (TEM) image in Fig. 5-5 shows around 6nm crystalline CeO_2 on top of 3nm amorphous CeO_2 layer on n-$In_{0.7}Ga_{0.3}As$ after annealing. The 3nm amorphous CeO_2 might be caused by the interaction between CeO_2 and InGaAs.

5.1.3 Study of CeO$_2$/HfO$_2$ gate stack MOS capacitors

CeO$_2$ has the potential as gate dielectric but the diffusion is seriously when CeO$_2$ was deposited directly on the semiconductor. HfO2 is known to demonstrate the inversion behavior on In$_X$Ga$_{1-X}$As[24-25]. To keep the high accumulation capacitance and form the inversion behavior, HfO$_2$ has deposited between the CeO$_2$ and InGaAs to form the MOS capacitor. The CeO$_2$/HfO$_2$ on InGaAs MOS capacitor could maintain the high capacitance with inversion behavior. Besides, HfO$_2$ has larger energy band gap than CeO$_2$ about 5.5eV which will help to reduce the leakage current.

Fig. 5-7 shows the TEM image and the EDX data for CeO$_2$/HfO$_2$ on n-In$_{0.7}$Ga$_{0.3}$As MOS capacitor with PDA at 500°C. We could observe from the TEM image that there is no amorphous layer on the n-In$_{0.7}$Ga$_{0.3}$As as in the case of CeO$_2$ on n-In$_{0.7}$Ga$_{0.3}$As. The element of Ce was found in the HfO2 layer and the element of Hf was found in the CeO$_2$ layer if the PDA temperature was over 500°C as indicated in EDX data in Fig. 5-6. The C-V characteristics of 6nm CeO$_2$/3nm HfO$_2$ on n-In$_{0.7}$Ga$_{0.3}$As MOS capacitor with PDA at 500°C is shown in Fig. 5-8. The inter-diffusion between the CeO$_2$ and HfO$_2$ resulted in the large frequency dispersion of C-V curve. The frequency dispersion mechanism could be explained by simple circuits. Fig. 5-9(a) shows the equivalent circuits including interface traps effects [26]. C$_{OX}$ and C$_D$ are the oxide capacitance and semiconductor depletion layer capacitance, respectively. C$_{it}$ and R$_{it}$ are the capacitance and resistance associated with the interface traps which are the function of energy. The product C$_{it}$R$_{it}$ is defined as the interface

trap life time τ_{it}, which determines its frequency behavior. The parallel branch of Fig. 5-9 (a) can be converted into a frequency-dependent capacitance C_P and a frequency-dependent conductance G_P in parallel with each other as shown in Fig. 5-9 (b). C_P and G_P which were mentioned in former chapter can also be written as

$$C_P = C_D + \frac{C_{it}}{1+\omega^2\tau_{it}^2} \tag{5-1}$$

$$\frac{G_P}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2} \tag{5-2}$$

At low frequency, R_{it} can be neglected, and C_D is in parallel with C_{it}. If the measurement frequency is too high for interface traps to respond, then C_{it} and R_{it} can be ignored. The simplified equivalent circuits for both conditions are shown in Fig. 5-9 (c) and (d). The measured capacitances for these two conditions are:

$$C_{LF} = \frac{C_{OX}(C_D+C_{it})}{C_{OX}+C_D+C_{it}} \tag{5-3}$$

$$C_{HF} = \frac{C_{OX}C_D}{C_{OX}+C_D} \tag{5-4}$$

For silicon MOS capacitors, when measured at low frequency and biased at the accumulation region, C_D is very large due to no depletion region forms, and C_{it} can be neglected owing to high quality interface. Thus the total capacitance is equal to C_{OX}. But for III-V case, the capacitance of interface traps must be considered, and is frequency dependent, so that the capacitance varied with frequency, causing frequency dispersion. Even measured at high frequency, if the frequency is not sufficiently high, the traps still can response, so the frequency dispersion will also be found in high frequency curve. The interface quality depended on PDA

temperature, in the other words; frequency behavior was affected by PDA temperatures significantly. Therefore, the CeO_2/HfO_2 $In_xGa_{1-x}As$ MOS capacitors with PDA temperature at $400^{\circ}C$ were used for the following samples.

The C-V characteristics of 10nm CeO_2/5nm HfO_2 and 15nm HfO_2 on p-$In_{0.7}Ga_{0.3}As$ and n-InAs MOS capacitors with PDA $400^{\circ}C$ were compared at 100kHz in Fig. 5-10. The capacitor with 10nm CeO_2/5nm HfO_2 as gate dielectric all shows the larger accumulation capacitance for both substrates. It can be seen from Fig. 5-10(a) that the capacitance increased in accumulation region from 0.65 ($\mu F/cm^2$) for HfO_2 /n-InAs capacitor to 1.03 ($\mu F/cm^2$) for CeO_2/HfO_2/n-InAs capacitor and from 0.47 ($\mu F/cm^2$) for HfO_2/p-$In_{0.7}Ga_{0.3}As$ capacitor to 0.69 ($\mu F/cm^2$) for CeO_2/HfO_2/p-$In_{0.7}Ga_{0.3}As$ capacitor as shown in Fig. 5-10(b). The n-InAs MOS capacitor shows larger capacitance than the p-$In_{0.7}Ga_{0.3}As$ MOS capacitor for both gate dielectrics.

Fig. 5-11 shows the C-V characteristics and leakage current of CeO_2 (10nm)/HfO_2 (5nm) on p-$In_{0.7}Ga_{0.3}As$. It can be seen clearly that there is frequency dispersion in the accumulation region. The frequency dispersion may be caused by the thin layer formed at the interface, which has relatively low resistivity [27].

5.2 Study of CeO_2/HfO_2 gate stack MOSFET

MOSFET with 5nm CeO_2/5nm HfO_2 gate stack structure was fabricated. Implant condition was divided into two steps; first is silicon doping ($1*10^{14}cm^2$) with 30keV, and following is silicon doping with 80keV

intensity. The gate was defined by E-beam lithography and the gate length was 0.2μm. The I_D-V_D characteristics are indicated in Fig. 5-12(a). The gate voltage was measured from 0 volt to 2 volt. The MOSFET fabricated is inversion-type e-mode device. It shows non-pinch-off curves, which means the drain current is not zero at the zero gate bias. It might be caused by the drain-substrate space charge area striding across to the source-substrate space charge area. The barrier between source and drain was eliminated in this condition resulting in a large drain leakage current. This phenomenon was called near punch-through effect. It also implied that the implant condition must be modified to the more appropriate conditions. The values of transconductance and drive current were quite low and need to be improved.
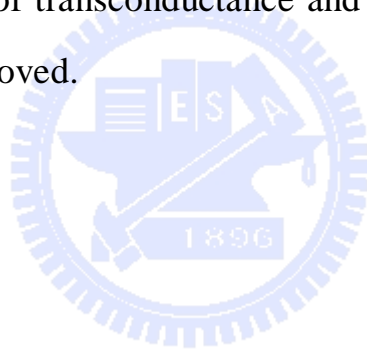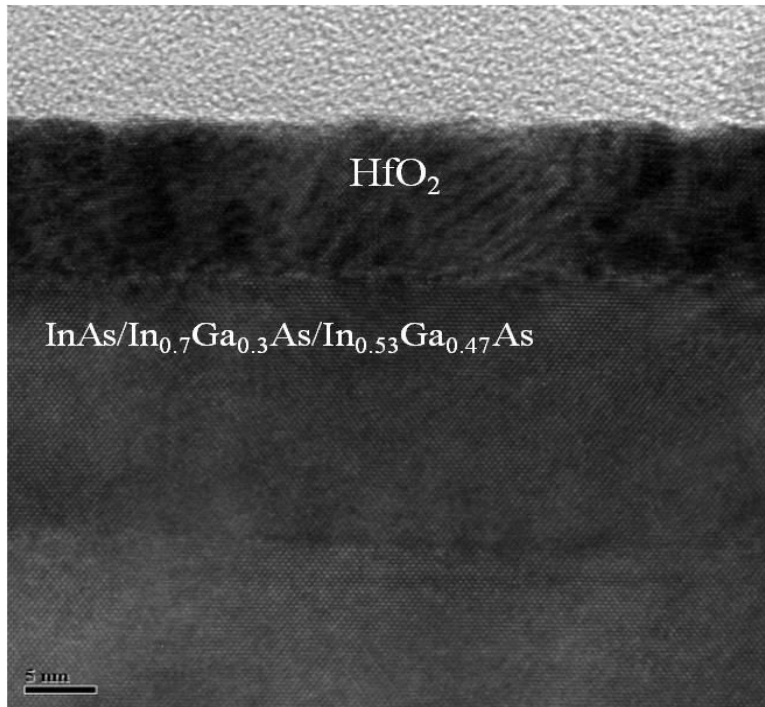
(a)
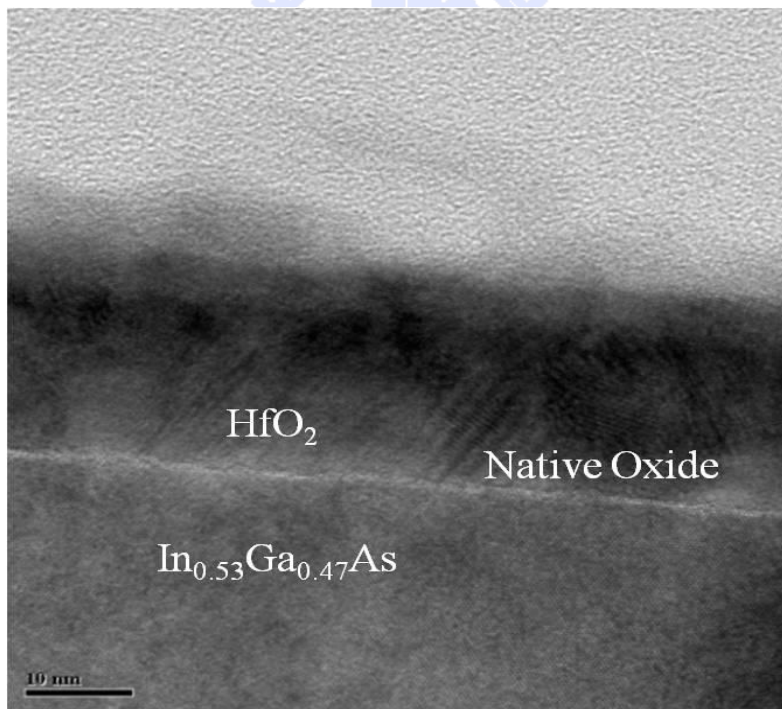
(b)

Fig. 5-1 TEM images of HfO_2 on (a) InAs (b) $In_{0.53}Ga_{0.47}As$, HfO_2/InAs MOS capacitor has no inter-layer at oxide/semiconductor interface which exists in HfO_2/ $In_{0.53}Ga_{0.47}As$ MOS capacitor.
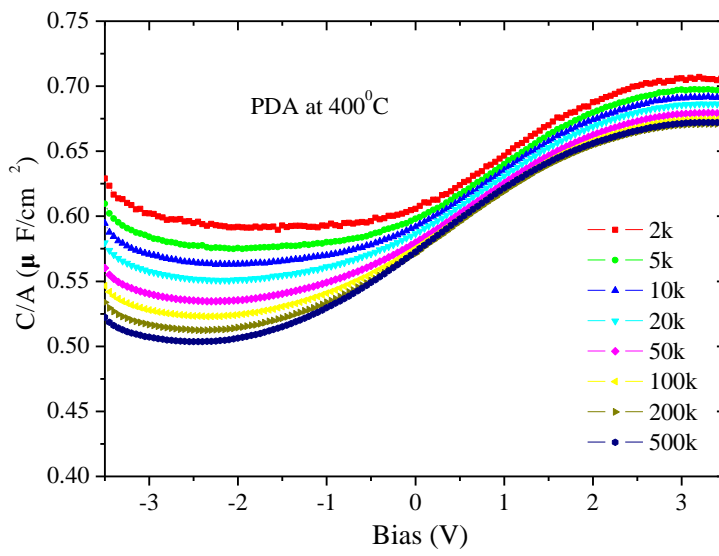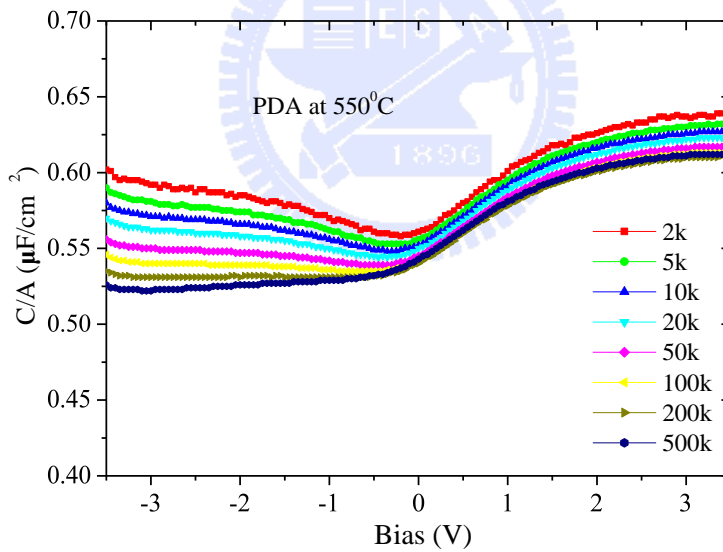
(a) PDA at 400°C
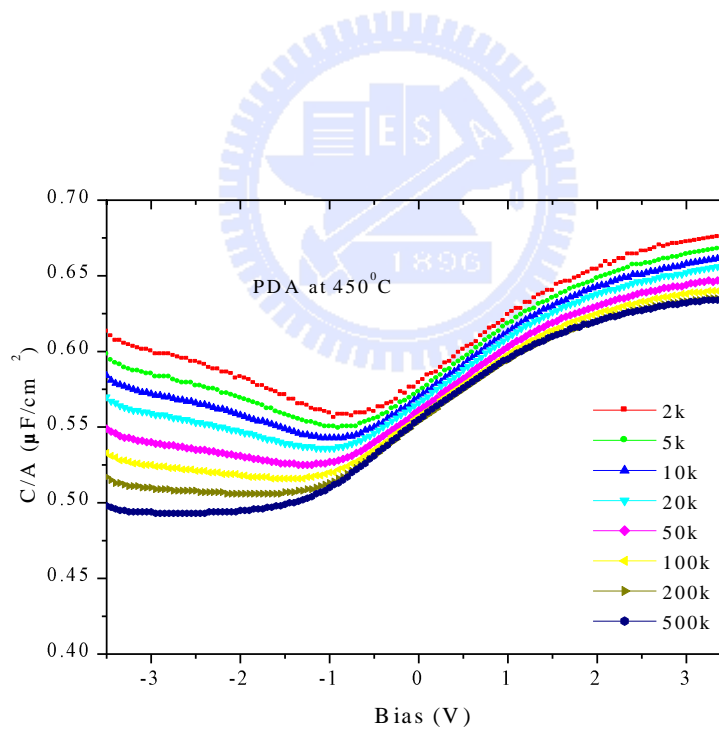
(b)PDA at 450°C
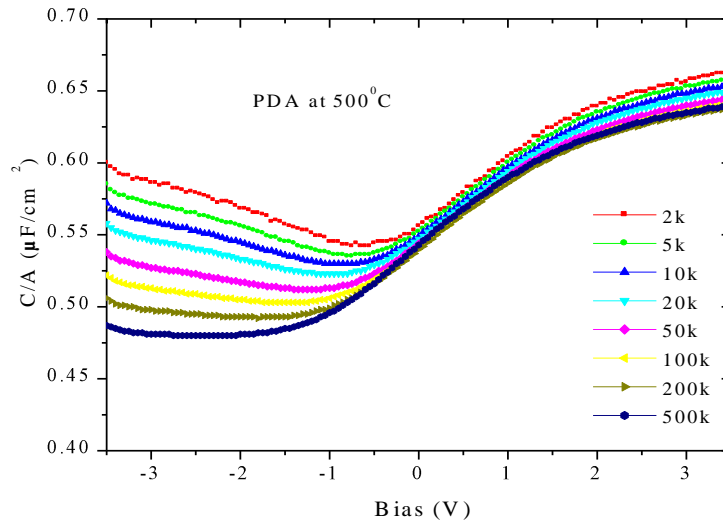
(c)PDA at 500°C

(d)PDA at 550°C

Fig. 5-2 The HfO$_2$/InAs MOS capacitors with varied temperature from 400°C to 550°C, the capacitance reduced with PDA temperature increasing. The sample with 500°C shows the obviously inversion behavior and lowest frequency dispersion.
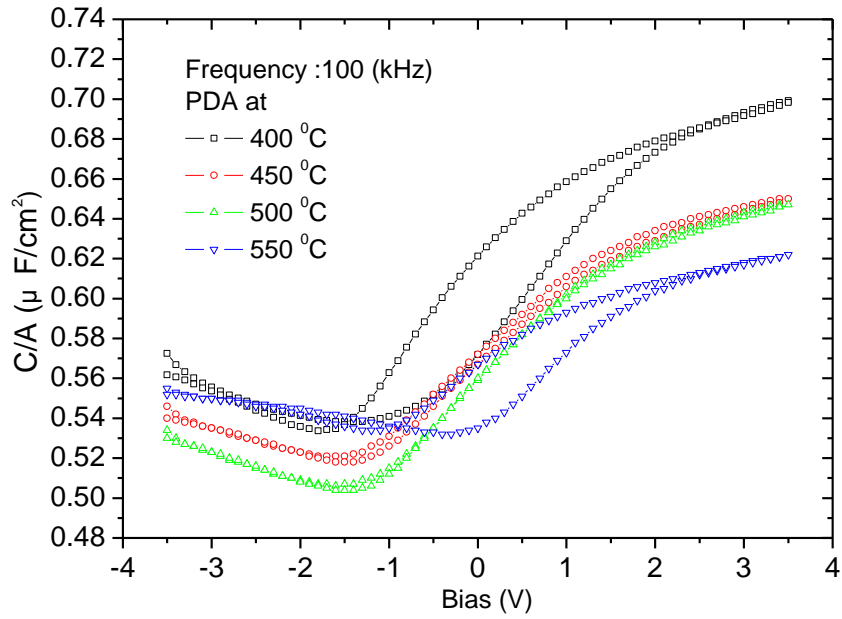
Fig. 5-3 Comparison of HfO_2/InAs MOS capacitors with different PDA temperature at 100kHz

Table 5-1 Comparison for C-V characteristics of HfO_2/n-InAs capacitors at different PDA temperatures.

PDA temperature (^{o}C)	400	450	500	550
Flatband voltage (V) 100KHz	2.178	1.319	1.113	2.138
Cfb ($\mu F/cm^{-2}$)	0.677	0.621	0.606	0.606
Hysteresis (V)	0.278	-0.189	-0.037	0.288
Dit ($cm^{-2}e \cdot V^{-1}$)	1.02×10^{13}	4.37×10^{12}	2.71×10^{12}	5.33×10^{12}
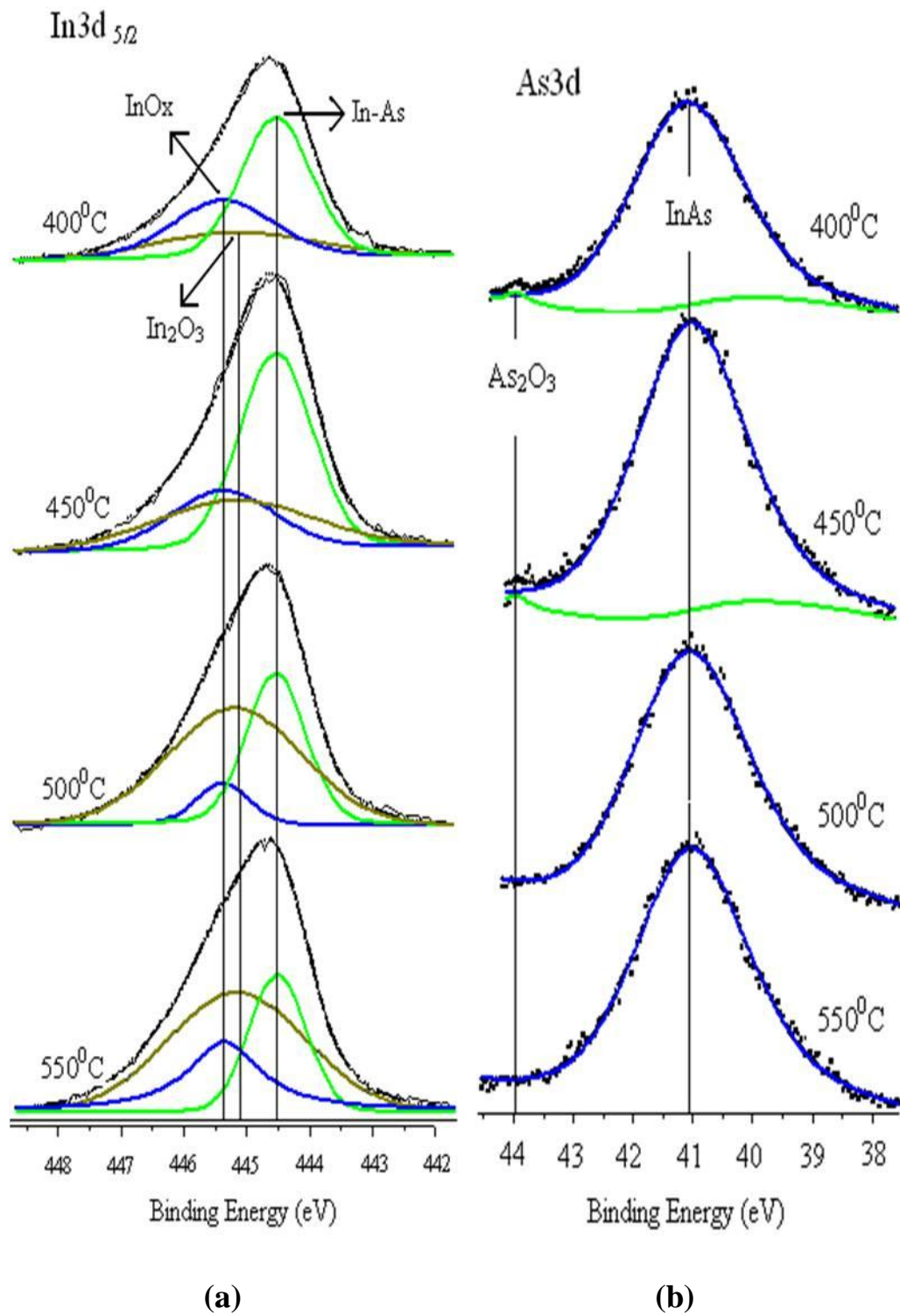
Fig. 5-4 XPS spectra of $HfO_2/InAs$ MOS capacitors with varied PDA temperature from $400^{o}C$ to $500^{o}C$.
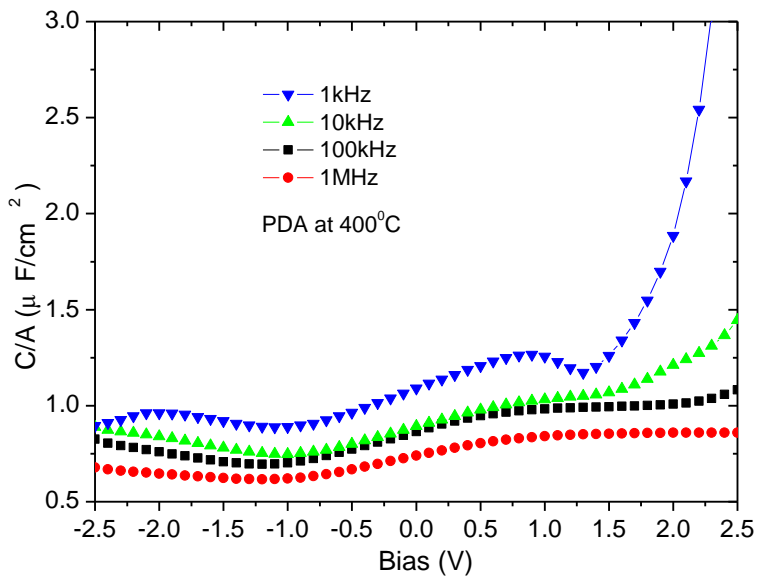
(a) PDA at 400°C
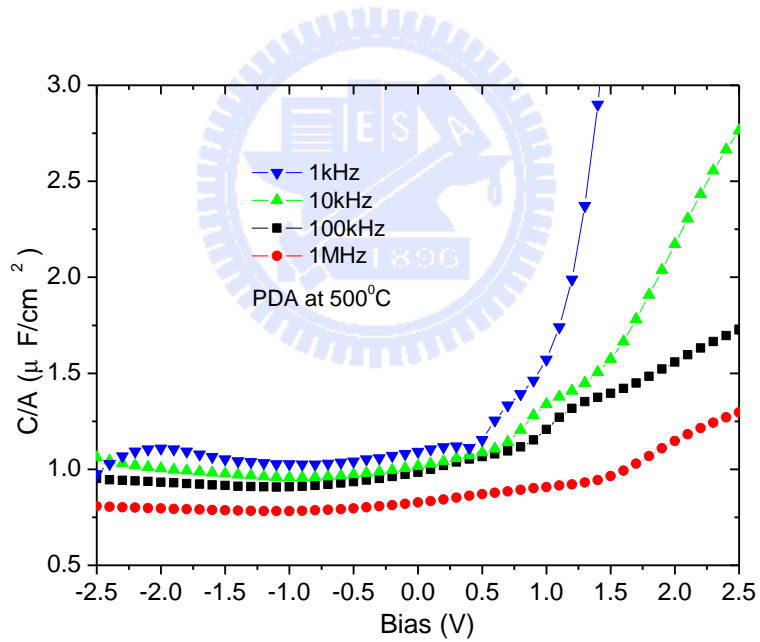
(b) PDA at 500°C

Fig. 5-5 The C-V characteristic of $CeO_2/In_{0.7}Ga_{0.3}As$ MOS capacitors with different PDA temperature (a) 400°C (b) 500°C
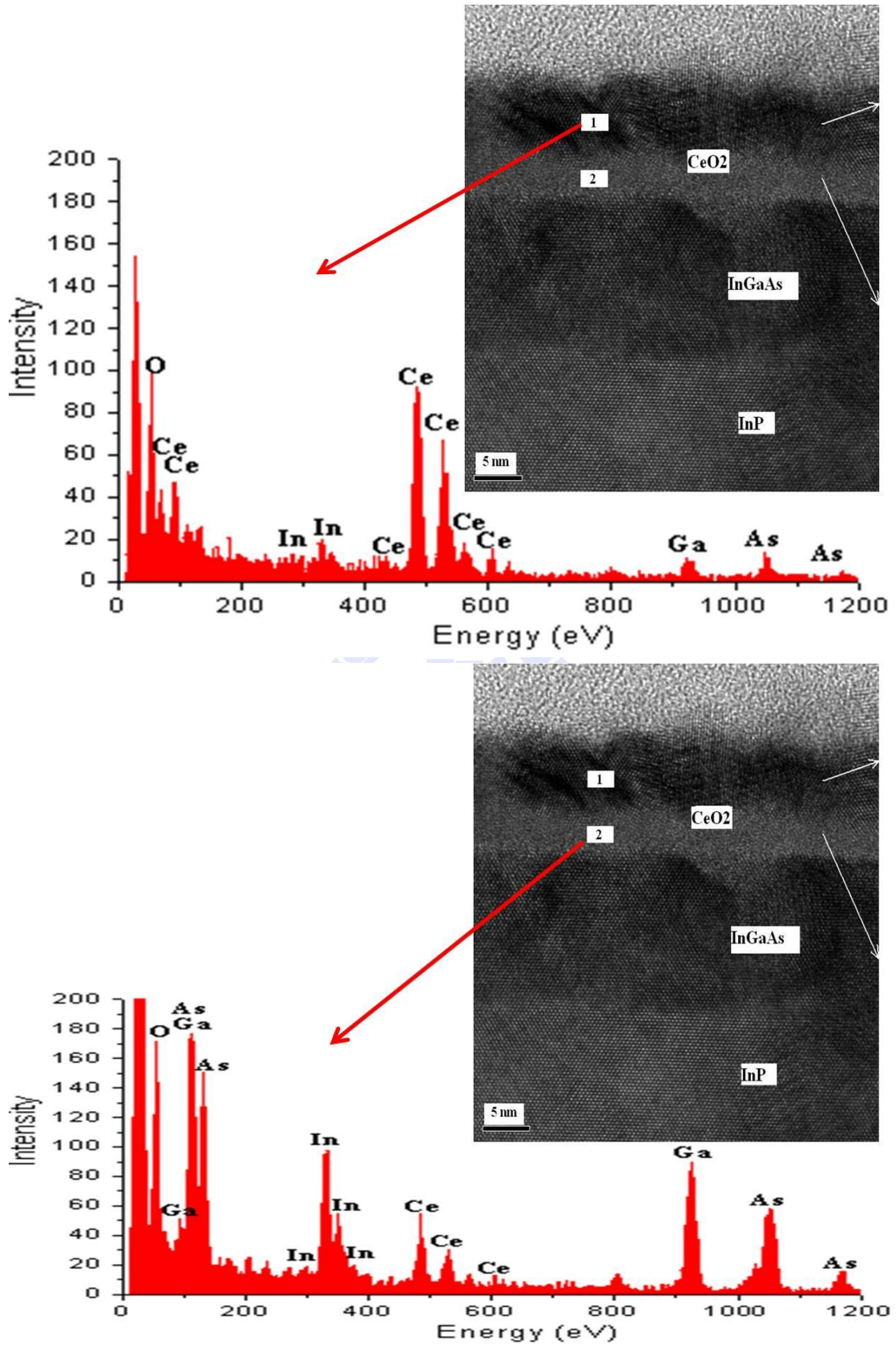
Fig. 5-6 TEM images and EDX results of 9nm $CeO_2/In_{0.7}Ga_{0.3}As$ MOS capacitor with PDA 500^oC
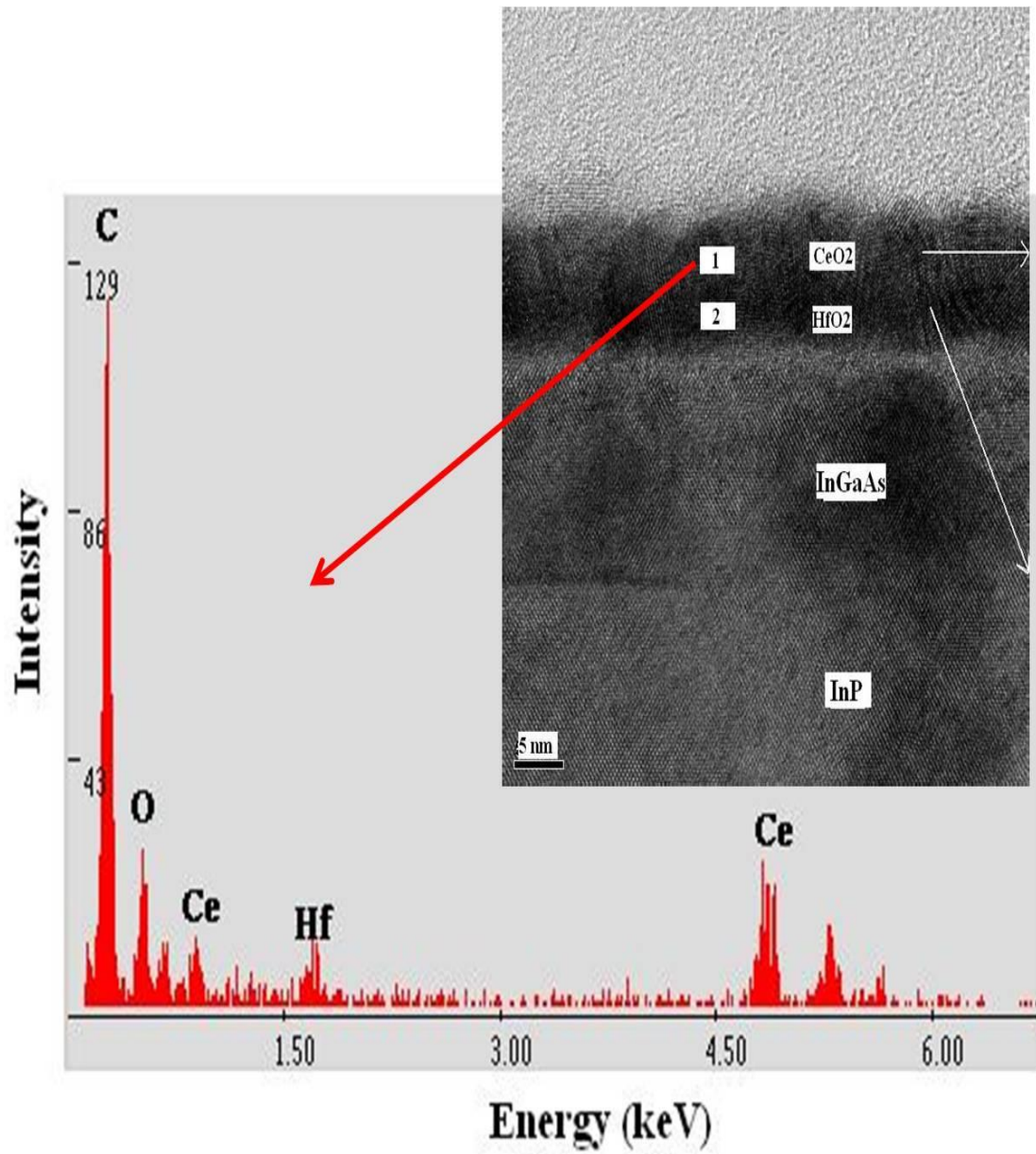
Fig. 5-7 (a) TEM images and EDX results of CeO_2 layer for 6nm CeO_2/ 3nm HfO_2/$In_{0.7}Ga_{0.3}As$ MOS capacitor with PDA $500^{o}C$
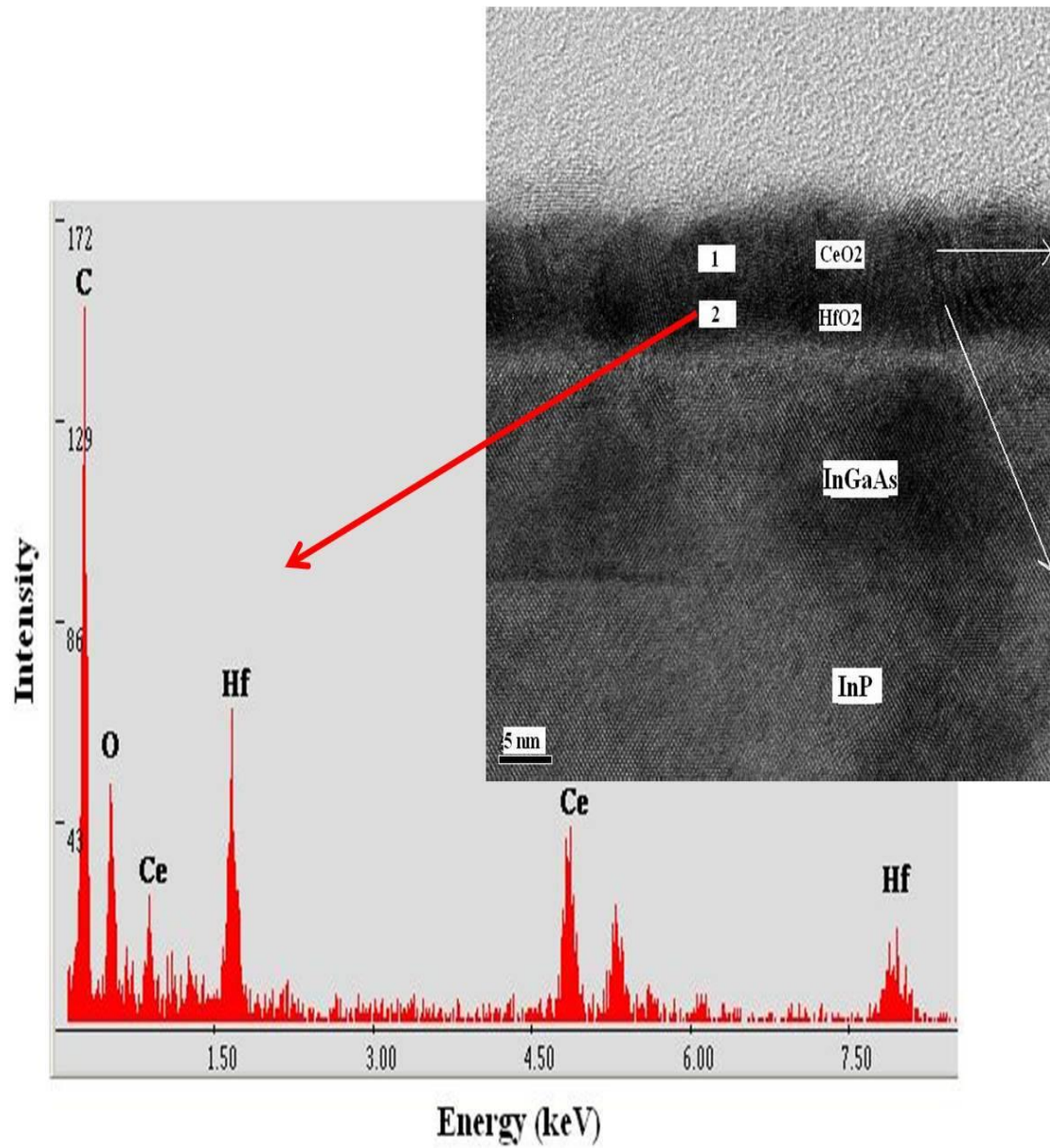
Fig. 5-7 (b) TEM images and EDX results of HfO_2 layer for 6nm CeO_2/ 3nm HfO_2/$In_{0.7}Ga_{0.3}As$ MOS capacitor with PDA 500^oC
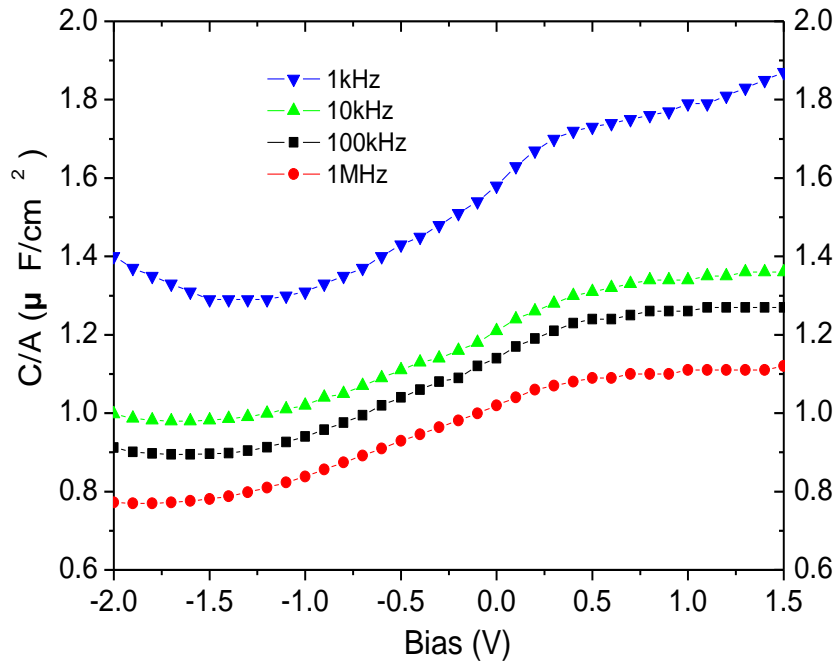
Fig. 5-8 The C-V characteristic of 6nm CeO_2/3nm HfO_2/n-$In_{0.7}Ga_{0.3}$As
MOS capacitor; It shows large frequency dispersion in accumulation
region due to the inter-diffusion between the CeO_2 and HfO_2 which is
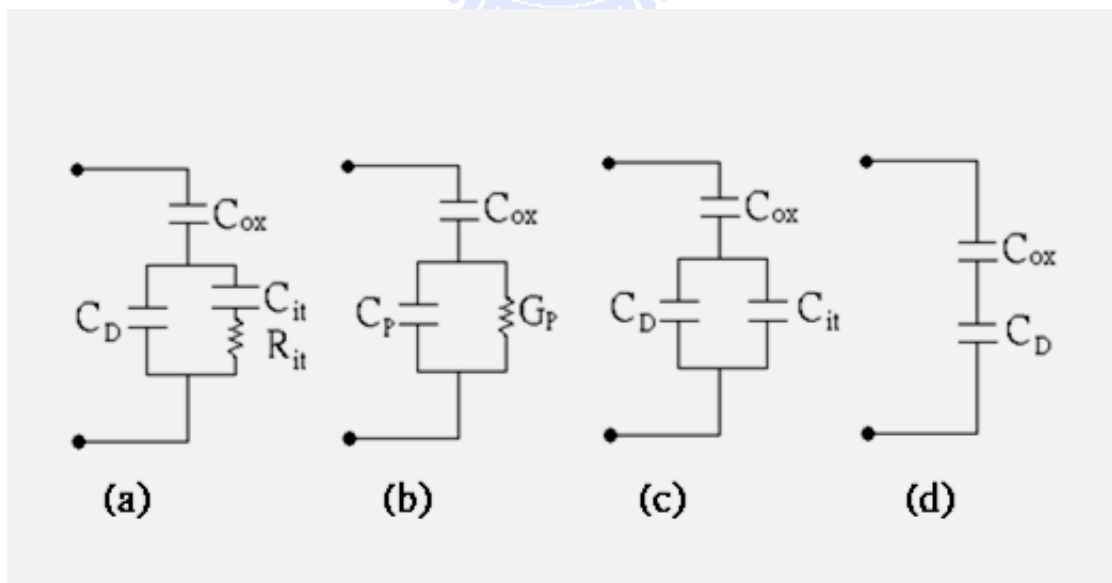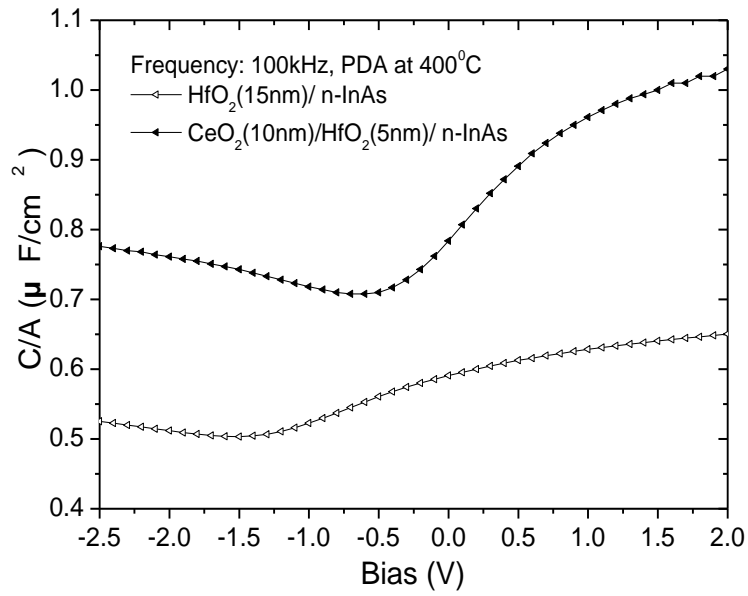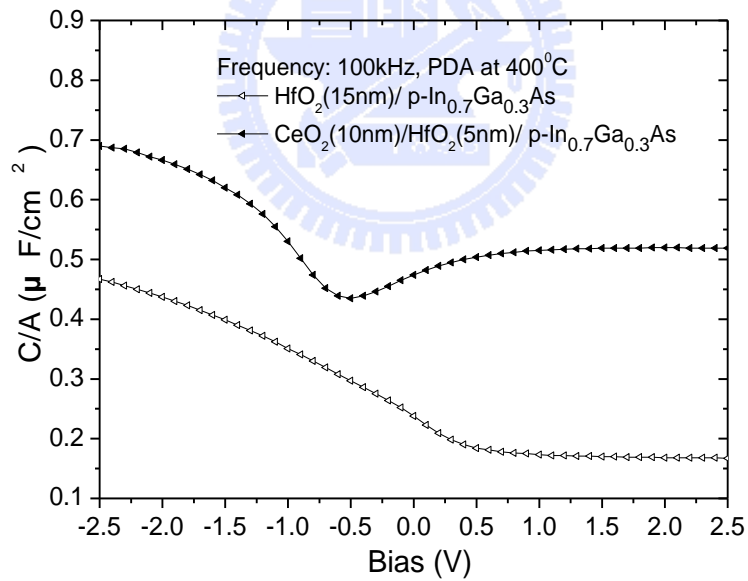indicated in Fig. 5-7.

Fig. 5-9 (a)-(b) Equivalent circuits including interface trap effects, C_{it} and
R_{it}. (c) Low frequency case. (d) High frequency case. [26]

(a)

(b)

Fig. 5-10 The C-V characteristic of 15nm HfO_2 and 10nm CeO_2/5nm HfO_2 on (a) n-InAs (b) p-$In_{0.7}Ga_{0.3}As$ MOS capacitors
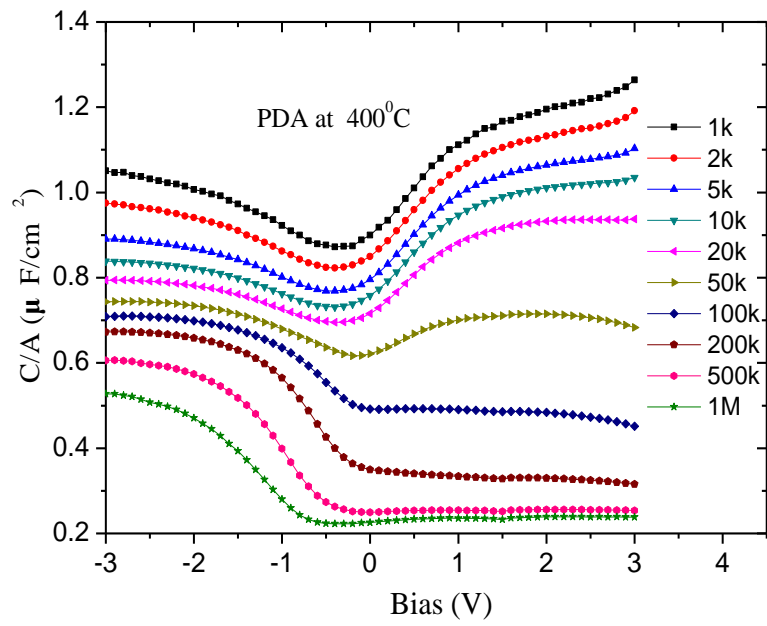
(a)
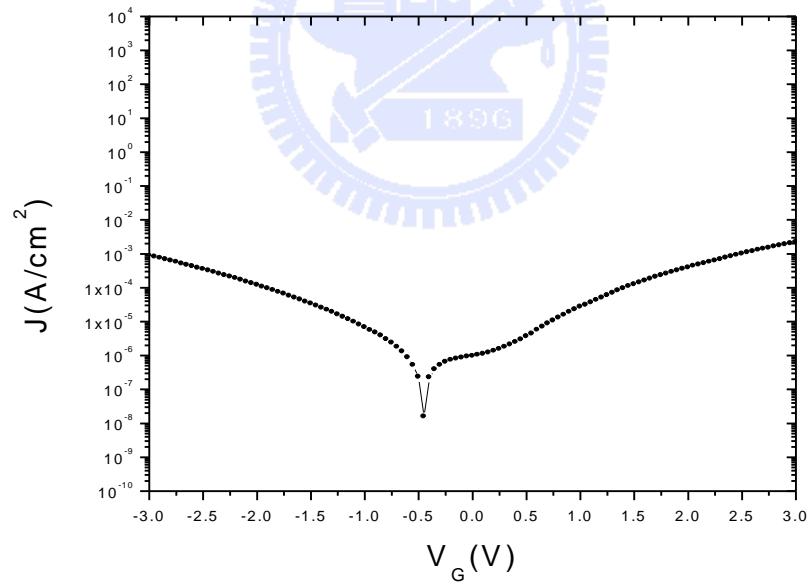
(b)

Fig. 5-11 (a) C-V characteristics (b) leakage current of 10nm CeO_2/5nm HfO_2 on p-$In_{0.7}Ga_{0.3}As$ MOS capacitor
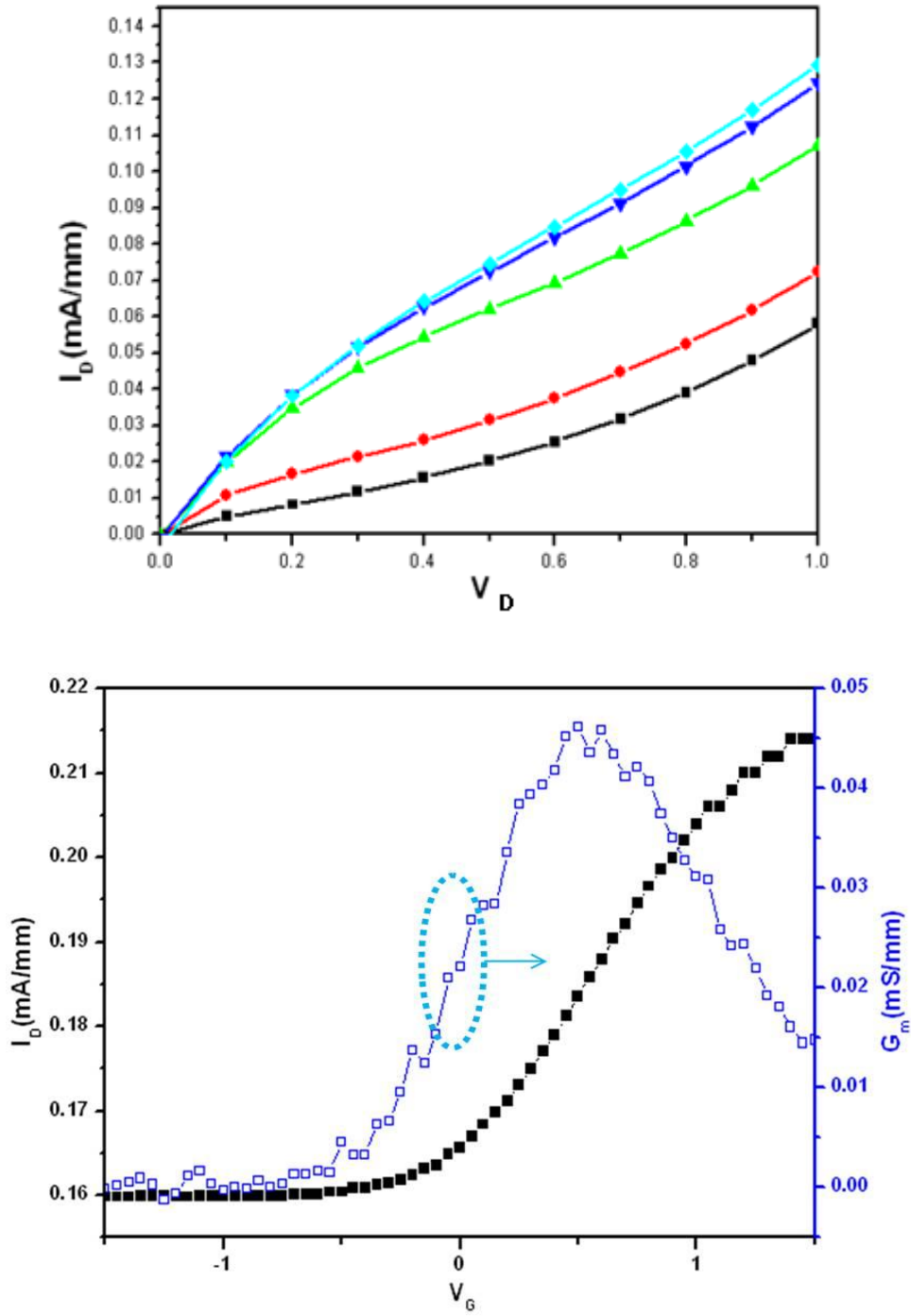
Fig. 5-12 (a) The I_D-V_D characteristics, V_G=0V, 0.5V, 1V, 1.5V, 2V (b) transconductance of 5nm CeO_2/5nm HfO_2 on $In_{0.7}Ga_{0.3}As$ MOSFET; V_D=1V.

Chapter 6

Conclusions

HfO_2, CeO_2, CeO_2/HfO_2 were deposited on $In_XGa_{1-X}As$ as gate dielectrics to fabricate the MOS capacitor in this study.

$HfO_2/InAs$ MOS capacitor had better interface quality with no native oxide formation compared to $HfO_2/In_{0.53}Ga_{0.47}As$ MOS capacitor as observed in TEM image. $HfO_2/InAs$ MOS capacitors were fabricated with various post deposition annealing temperatures. The capacitors with PDA 500°C had the lowest interface trap density (D_{it}), flat band voltage shift and the hysteresis which implied the better interface quality. These characteristics also could be explained by the XPS data. When the PDA temperature increased to 500°C, the InO_X had the lowest peak and the In-As peak was also reduced. Both peaks were observed to increase when the PDA temperature was increased to 550°C.

In order to increase the device's capacitance, CeO_2 was choosing as gate dielectric on $In_XGa_{1-X}As$ MOS capacitor due to its high dielectric constant. But the diffusion between the oxide and semiconductor was serious causing the abnormal C-V characteristics. This phenomenon resulted from the high interface traps at the interface and quite much space charge in the oxide layer, it was also observed in the CeO_2/Si MOS capacitor cases. To solve this problem, HfO_2 was deposited between the CeO_2 and semiconductor. HfO_2 had the larger energy band gap than CeO_2 and more thermally more stable. Furthermore, it had the good interface quality in this study. The C-V characteristic results showed that CeO_2/HfO_2 MOS

capacitor had the larger capacitance than HfO_2 MOS capacitor on both $In_{0.7}Ga_{0.3}As$ and InAs substrates. The inter-diffusion between the CeO_2 and semiconductor was reduced significantly by using CeO_2/HfO_2 gate stack structure which could be observed in the TEM images and EDX data. The MOSFET with CeO_2/HfO_2 gate oxide was also fabricated. The devices performance still needs to improve and the appropriate implant conditions need be done.

$CeO_2/HfO_2/In_XGa_{1-X}As$ MOS capacitor shows the larger accumulation capacitance but also the larger frequency dispersion than $HfO_2/In_XGa_{1-X}As$ MOS capacitor. It implied that interface quality must be improved. To dismiss the diffusion problem, CeO_2 shows potential as gate dielectric due to its high dielectric constant, especially 52 for single crystalline CeO_2. Otherwise, HfO_2 has the superior properties and thermal stability on $In_XGa_{1-X}As$ which is also the excellent gate oxide candidate for III-V MOS structure. These high-k/III-V MOS structure have the potential for the future CMOS technology development.

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