國 立 交 通 大 學

材料科學與工程研究所

碩士論文

多孔矽基板在抗反射層應用之研究

Study of Porous Silicon for Anti-Reflection Applications

研 究 生：阮芝陵

指導教授：張　翼　教授

中華民國九十九年八月

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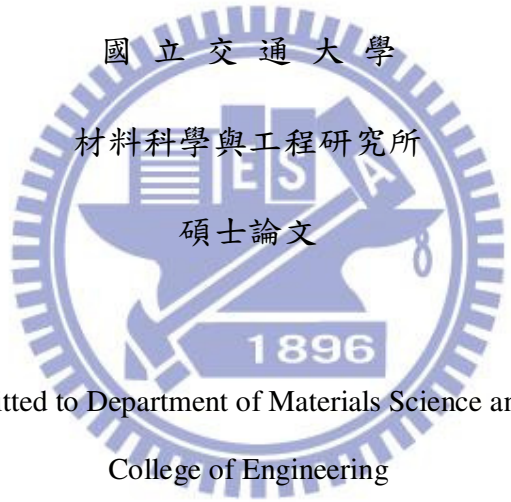

國 立 交 通 大 學

材料科學與工程研究所

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多孔矽應用於抗反射層之研究

研究生：阮芝陵　　指導教授：張 翼 博士

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摘要

在本論文中，我們針對抗反射層利用多孔矽反射係數的數值模擬進行研究。依據數值模擬的分析，我們開發出在單晶矽中形成多孔矽的化學蝕刻液(包含氫氟酸、硝酸及水)。我們都知道在半導體產業裡，氮化矽與二氧化矽過去一向是用在抗反射層。然而，使用氮化矽與二氧化矽抗反射層將會提高太陽能模組的生產成本，不利於低成本的光伏元件。在單晶矽的結構粗糙化製程中，使用斑點蝕刻形成多孔矽的化學蝕刻是一種簡單、快速及低成本的技術。在可見光波段，多孔矽的粗糙化結構更可大幅降低元件表面的反射率。

在此研究中，我們成功地在矽(100)與矽(111)基材表面上製造出多孔矽的粗糙化結構，並利用多樣的氫氟酸、硝酸及水的混合比例去最佳化蝕刻製程。在研究中發現，硝酸在斑點蝕刻裡扮演了非常重要的角色。當硝酸比例在混合溶液中低於 40%，多孔矽的粗糙化結構會成形。而硝酸比例在混合溶液中大於 40%時，多孔性結構形成與一般平滑性的表面蝕刻會處於過渡狀態。此時，細微的孔洞結構會均勻地分佈在晶圓表面，並使表面粗糙化。藉由使用化學蝕刻液的方法，我們可以從裸晶上獲得降低至 0%的反射率。更進一步地，我們可以在大尺寸(7.5x7.5cm^2)的矽(100)基材表面上成功地形成多孔矽的粗糙化結構；並且與傳統使用電漿增強化學氣相沉積法所形成的氮化矽與二氧化矽抗反射層相較，仍然可以保持較低的反射率。因此，我們認為使用斑點蝕刻技術所形成多孔矽的粗糙化結構將會取代傳統的抗反射層。

Study of Porous Silicon for Anti - Reflection Applications

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Department of Materials Science and Engineering

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Abstract

In this dissertation, we numerically study the reflectance of porous silicon (PS) layer for antireflection applications. Based on the numerical study, we develop chemical etchant (HF, HNO_3, H_2O) to form PS layer on crystalline silicon wafer. As we all know, silicon nitride and silicon dioxide are well known antireflection coating used in semiconductor industry. However, the deposition of silicon nitride and silicon dioxide films increase the total cost of solar cell modules which is not suitable for low-cost photovoltaic devices. In the other hand, the chemical etching known as stain etching (SE) porous silicon is a cheap, simple and rapid technique for texturing single-crystalline silicon. In addition, porous silicon shows the remarkable low reflectance at visible light.

In this study, we have successfully fabricated porous silicon layer on top of the Si (100) and Si (111) surfaces. We varied the proportion of the solution of nitric acid, hydrofluoric acid and water to optimize the etching process. We found that nitric acid plays a very important role in stain etching. When the proportion of the

nitric acid is lower than 40% in volume, porous etching occurs. The transition between porous formation and polishing etching occurs when nitric acid content is lager than 40%. Pore size distributes uniform on the surface of wafer. Stain etching also provides the rough surface. After etching in the proper etchant solution, the reflectance of the bare wafer was reduced to 0%. We have also successfully formed porous layer in large size (7.5x7.5cm) Si (100) which has lower reflectance compared with conventional AR PECVD-Si_3N_4, and SiO_2 .We conclude that stain etching porous silicon could be a promising replacement for the conventional AR coatings.

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I wish to thank former and current members in Compound Semiconductor Devices Laboratory of National Chiao-Tung University, Huang. M. Chi, Trinh. H. Dang, Nguyen. H. Quan. Discussions with them opened my viewpoints and inspired my ideas

At last, my special thank to my parents for their moral support and faith on me during all these years.

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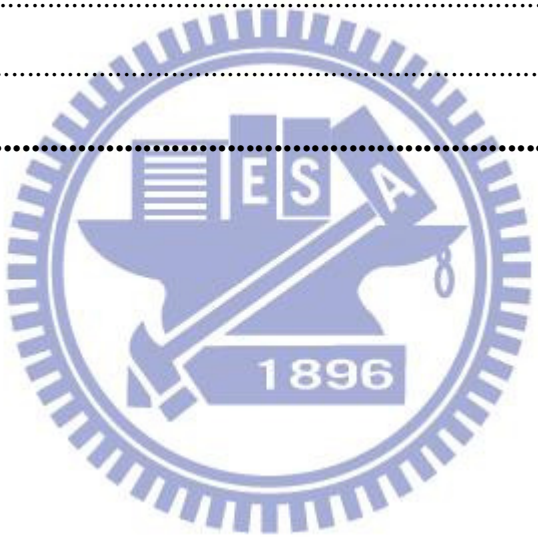

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Chapter 1

Introduction

1.1 General background and Motivation

Currently, the cost of photovoltaics (PV) energy is two to four times the cost of conventional fossil energy. Crystalline Si accounts for more than 90% of the PV modules produced nowaday. Nearly 55% of the cost of a Si photovoltaic module is associated with the crystallization and wafering of the Si substrate. In an effort to reduce the production costs, a great deal of research has been devoted to the development of low-cost PV grade Si substrates. The random grain orientations of the multi-crystalline Si wafers inhibit the formation of uniform and effective surface texturing using conventional alkaline etching techniques. An effective surface texture can result in a 6 to 8% improvement in the conversion efficiency for multi-crystalline Si solar cells [1]

A record laboratory efficiency of 24% were obtained for single-crystal Si solar cell with diffused p - n junctions [1]. However, the structure involved with extremely complex fabrication process. It includes surface structuring - inverted pyramid- by photolithography and etching, high temperature passivation by thermal oxidation, and the contact system has to be formed again by photolithography. It is clear that such fabrication process may not be suitable for mass productions. Thus, the development of anti reflective (AR) material is important to enhance the light trapping efficiency of PV cell. Conventionally, silicon nitride (Si_3N_4), silicon oxide (SiO_2) and others material are used as AR materials in most of the PV devices (table 1.1). But these methods will increase the fabrication cost of PV cells. Therefore, new method is needed in order to reduce the fabrication cost and replace the conventional AR materials. Porous silicon (PS) is one of the materials, which have many unique properties for PV application as well as technological manufacturing simplicity. PS materials contribute low surface reflectance with surface roughness which is comparable to the conventional ARCs. PS material was discovered by Uhlir and Turner [7] in 1956 when they carried out the research for electropolishing Si and

Ge. The (electro-) chemical process is still the most widely applied PS formation technique nowadays.

Table 1.1 Some anti-reflection coatings on Si surface and common process techniques

Films	Refractive Index	Process Technique
SiO_2	1.45	Thermal oxidation, sputtering, LPCVD
Al_20_3	1.85	Sputtering, e-beam, LPCVD
SiO	1.85	Sputtering
Si_3N_4	1.9	LPCVD, PECVD
TiO_2	2.0 – 2.3	APCVD, Spraying
Ta_2O_5	2.1 – 2.3	e-beam
ZnS	2.35	Sputtering, e-beam

By controlling the current density and proportion of hydrofluoric acid (HF), PS is created when the current is passing through the Si. However, electrochemical etching needs a complex set up system to process which is not suitable for mass production.

In the same period, Robbins and Schwartz as well as Turner also came out with alternative chemical etching of Si using a mixture of HF - HNO_3 acids. The PS material resulting from an HF - HNO_3 based etch is called the stain-etched PS. Stain etching offers cheap, simplicity process for PS formation. By optimizing the ingredient of HNO_3 and HF acids, the low reflectance of PS layer on Si can be produced after few second of stain etching

1.2 Outline of Thesis

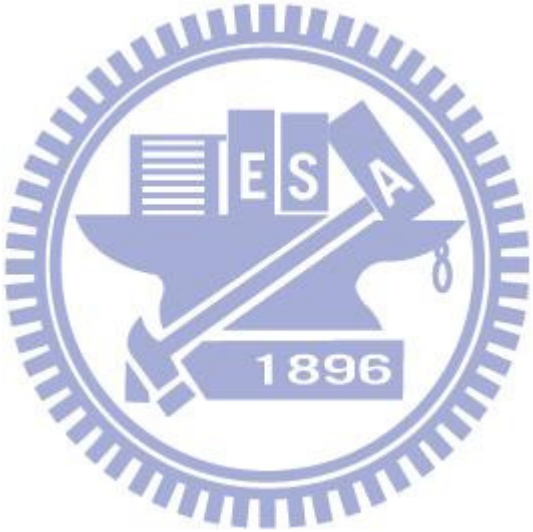
This thesis focuses on the study of the formation of PS by stain etching for anti-reflection applications. The thesis is divided into five chapters.

In the chapter 2, the literature of some of the promising texture methods for AR application are briefly reviewed, including the low-cost porous silicon etching technique used in this thesis.

In chapter 3, the detailed study about porous silicon materials is presented. The optical properties and the application of porous silicon in solar cell devices are also dicussed.

In chapter 4, the fabrication process and measurement instrument are introduced

In chapter 5, the experimental results and discussions are presented. Then, in the final chapter, our study on the PS for AR application in PV cells are summarized and concluded



Chapter 2
A review of texturing crystalline silicon solar cells

2.1 Challenges in Texturing Crystalline Silicon

Some general prerequisites for texturing microcrystalline-Si samples for industrial adaptation require that the method be effective on all crystalline grain orientations, be able to withstand subsequent processing, allow for screen-printed metallization, and justify any increased cost with efficiency improvement . Three of the most promising techniques currently being researched are acidic etching (including PS), mechanical grooving by wafer sawing, and reactive ion etching (RIE) involving dry processing in a plasma machine. Each technology offers unique aspects toward efficiency improvement [1].

Texturing in general offers the potential for increased light trapping effect by changing the angle of incidence of incoming light. If the light is not absorbed at the initial surface, it is reflected toward another part of the substrate so it gets a second chance at being absorbed. In addition, total internal reflection under encapsulation is increased by a very slight texture. Using Snell's law with Figure 2.1

$$n_1 \sin\theta_1 = n_2 \sin\theta_2 \qquad (1)$$

where n_1 is the refractive index of medium 1 (the encapsulation layer n_1=1.5), n_2 is the refractive index of medium 2 (air with n_2=1), θ_1 is the incident angle, and θ_2 is the transmission angle. Recognizing θ_1 as twice the texture angle (i.e., the texture angle = $\theta_1/2$) and setting θ_2 equal to 90^o, total internal reflection conditions are met for a encapsulated solar cell at texture angles greater than 21^o from horizontal, see Figure 2.1**.** A very slight texture will cause total internal reflection.

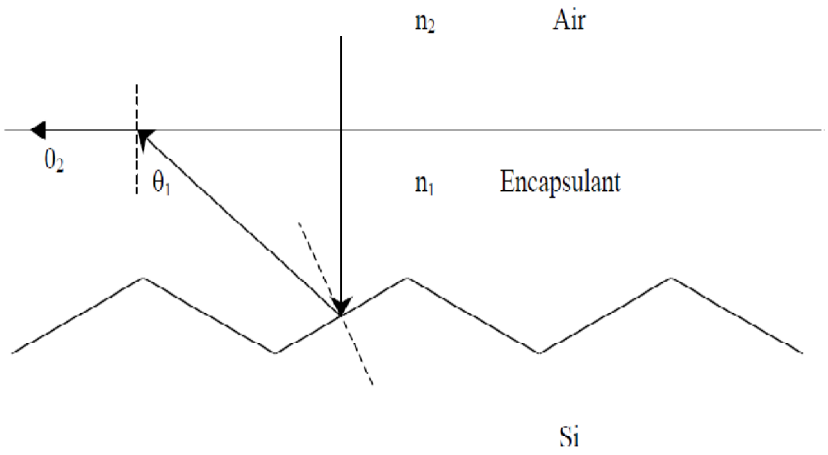


Figure 2.1 Total internal reflection schematic for a textured solar cell.

Each texturing method described below offers control over particular surface structure features but the true challenge for incorporation of surface texturing is the development of an industrially viable process sequence.

2.2 Reactive Ion Etching (RIE)

RIE of Si typically involves either chlorine- (Cl_2) or fluorine (F_2)-based plasma etching. By controlling the kind of gas, the gas ratios, the RF power, the reactor pressure, and so on, a single or mc-Si surface can be etched with homogeneous pyramid- like structures [2]. Very low surface reflectance can be achieved by tailoring the aspect ratio of the feature sizes etched on the Si surface, resulting in so-called "Black Si". Figure 2.2 shows scanning electron microscopy (SEM) images of various RIE textured surfaces with different Cl_2 flow ratios. The Si wafers are immersed directly into the chlorine plasma. Inomata et al found that as the surface structure size increased so did the solar cell dark saturation current [2]

RIE etched surfaces commonly suffer from increased surface damage and often require special processing techniques that do not destroy or remove the texturing while simultaneously providing for solar cell fabrication. Inomata et al achieved a 17.1% efficient large area (225 cm^2) multic-Si solar cell using photolithography techniques and laboratory processing.

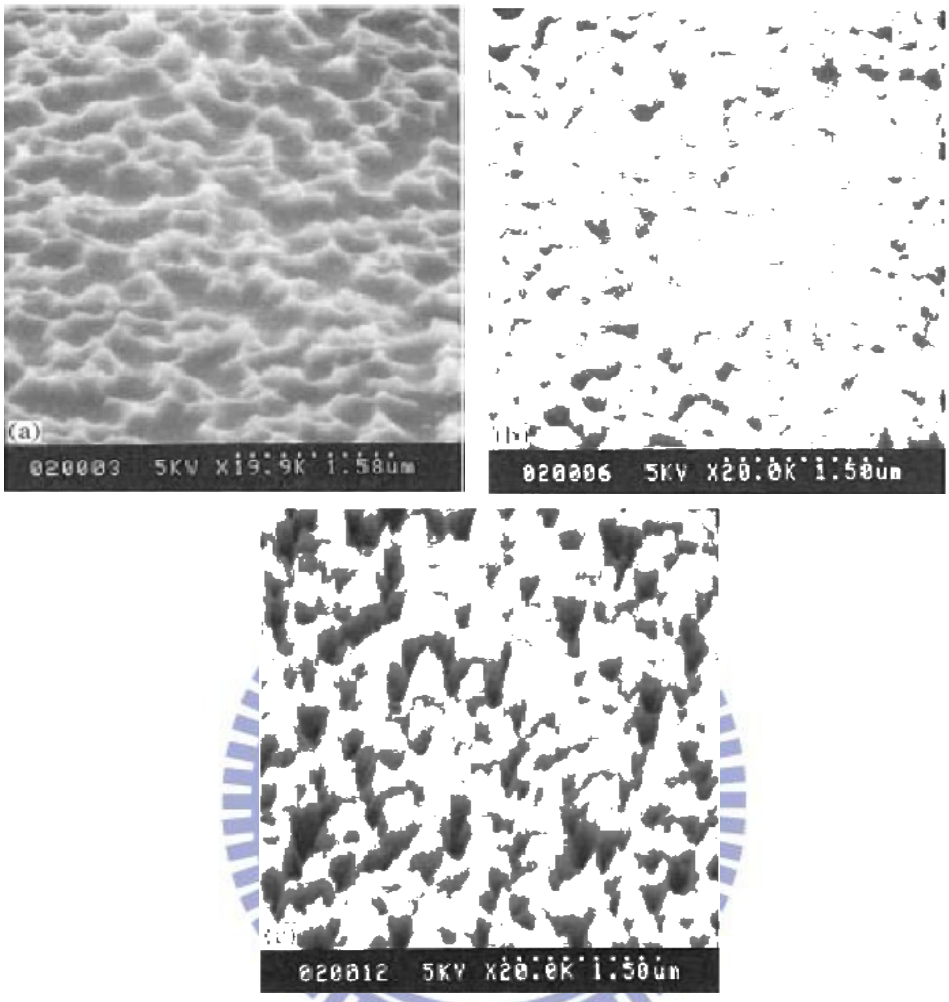


Figure 2.2 SEM pictures of RIE-textured material with different Cl_2 flow ratios.

Damiani et al [1] used industrial screen-printed contacts on RIE-textured wafers treated with different damage removal etches. A maskless SF_6/O_2 plasma process using RIE was developed at Sandia National Laboratories. Table 2.1 shows efficiency data prior to any anti-reflection coating application. RIE-textured solar cells showed up to a 33% increase in efficiency over planar devices. Table 2.2 shows that after SiN deposition, an additional 1% absolute efficiency was gained (or 8% relative efficiency improvement) with a maximum efficiency of 13.7%, thus effectively demonstrating the potential for increased efficiency by incorporating RIE texturing. Figure 2.3 shows the resulting reflectance for various RIE-textured samples. Very low

reflectance across the entire wavelength range (300-1200 nm) were demonstrated. Figure 2.4 shows the external quantum efficiency for the same RIE-textured cells.

The external quantum efficiency measures the percentage of incident photons successfully collected by the solar cell.

Table 2.1 I-V data for RIE multi-crystalline solar cells

Wafer Treatment	Voc (mV)	Jsc (mA/cm^2)	FF	η	Increase
planar controls	574	22.20	0.759	9.7	**0%**
conditioned texture 20 sec nitric	566	23.43	0.733	9.7	**0%**
Al-assisted 20 sec nitric	560	27.02	0.695	10.5	**9%**
Cr-assisted 8-min KOH	576	24.77	0.756	10.8	**11%**
conditioned texture ~ 20-25 sec nitric	577	25.12	0.748	10.8	**12%**
Al-assisted 15-sec nitric,	573	25.83	0.739	10.9	**13%**
conditioned texture 15 sec nitric	582	26.96	0.748	11.7	**21%**
conditioned texture 10 sec nitric	578	27.14	0.748	11.7	**21%**
Cr-assisted no DRE	583	29.18	0.756	12.9	**33%**

Table 2.2 I-V data for SiN coated solar cells.

Wafer Treatment	Voc (mV)	Jsc (mA/cm^2)	FF	η	Increase
planar controls	584	28.25	0.772	12.7	**0%**
conditioned texture 20 sec nitric	575	28.93	0.757	12.6	**-1%**
conditioned texture 10 sec nitric	587	30.84	0.751	13.6	**7%**
Cr-assisted, No DRE	591	30.63	0.759	13.7	**8%**

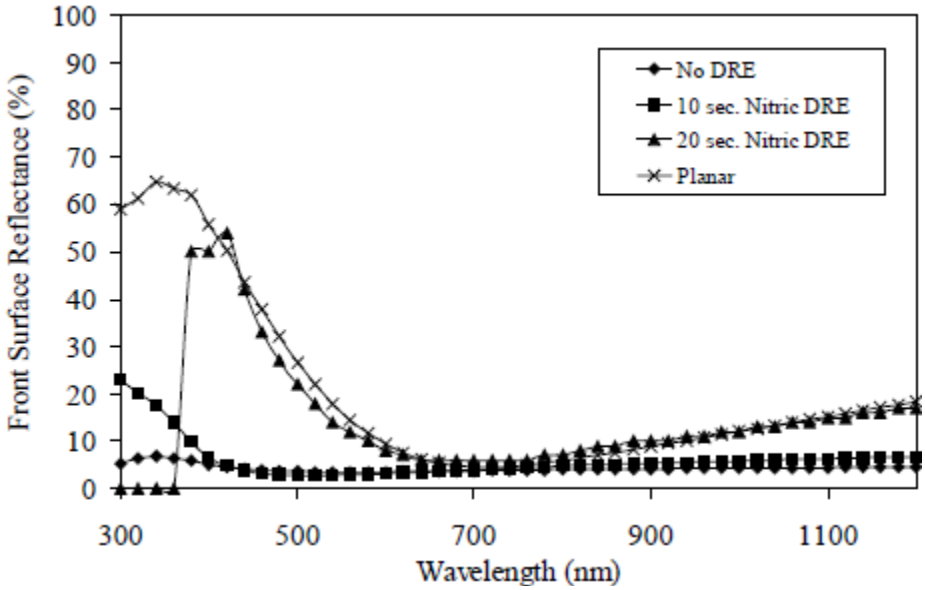


Figure 2.3 Front surface reflectance curves for RIE textured + SiN ARC on multi-crystalline solar cells with varying damage removal etching schemes applied.

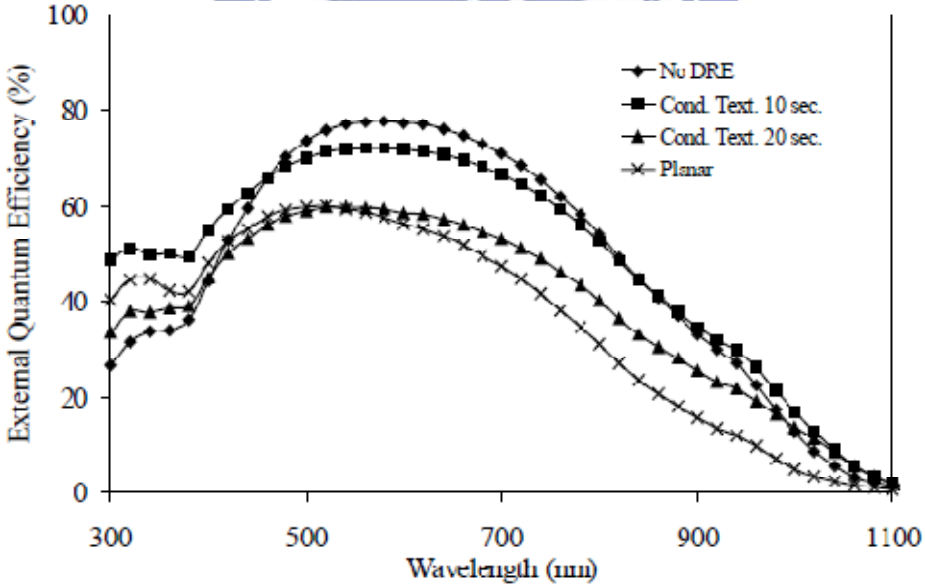


Figure 2.4 External quantum efficiency of RIE textured samples with different damage removal etches applied

RIE offers the potential for an effective surface texture for c-Si solar cells but requires some processing constraints in addition to the use of plasma machines. The capital investment required to purchase, maintain, and operate a RIE plasma machine has restricted widespread implementation. In addition, vacuum processes tend to be time intensive and could potentially reduce throughput.

Only one company, Kyocera, uses RIE to make c-Si cells in production. A more simplified approach, described next, involves mechanical grooving to form surface texturing on c-Si wafers.

2.3 Mechanical Grooving for Surface Texturing of mc-Si Solar Cells

The mechanical grooving technique uses stacked saw blades to groove V shaped trenches on the mc-Si surface with 3 to 4μm tall feature sizes. Figure 2.5 shows a schematic drawing of the mechanical grooving technique, along with a resulting surface structure [3]. A process sequence based on screen-printed contacts fired through SiN resulted in 16.6% efficiency on a 100 cm^2 mechanically grooved mc-Si substrate [4], again demonstrating the high efficiency potential for textured mc-Si solar cells. However, mechanically grooved wafers are highly stressed and therefore are not suitable for all types of mc-Si wafers, especially thin substrates. In addition, mass production of screenprinted contacts directly on a mechanically textured surface presents additional challenges in achieving good fill factors and a low contact resistance.

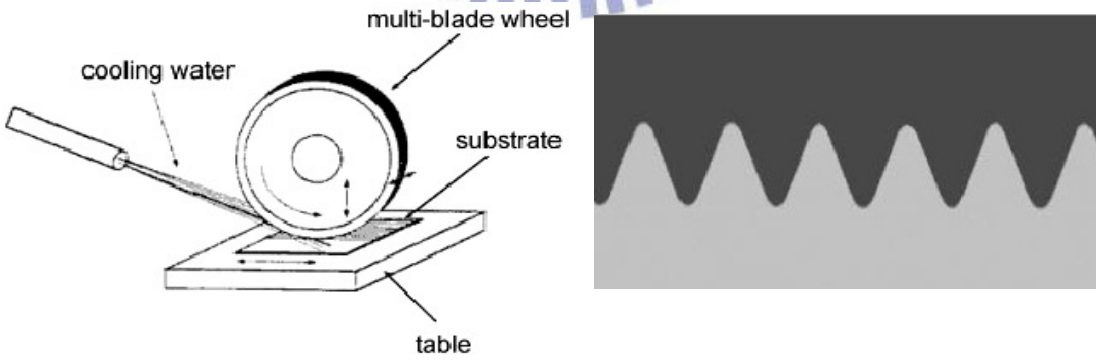


Figure 2.5 Multi-blade V-grooving technique and resulting surface structure with feature size from trench to peak of 3 to 4μm.

2.4 Chemical Etching for Surface Texturing

Chemically etched samples generally fall into two categories: acidic and alkaline. Alkaline etches are typically used for single crystal materials and preferentially etch in the (111) direction, resulting in pyramid formation for (100) oriented surfaces. Acidic etches are typically not sensitive to surface morphology. In some methods, photolithography techniques are used to assist in surface texturing. However, photolithography approaches are not feasible for mass production and therefore are not discussed in this thesis.

2.4.1 Conventional methods

Acidic isotropic etching techniques have become increasingly popular and have been shown to contribute only 0.02-0.03 $/Wp to total cell fabrication costs [5]. However, only wire saw cut wafers can be successfully etched with the technique based on an aqueous solution of HNO_3, HF, and some "additives" for wetting purposes. Currently, more than 80% of the c-Si wafers are produced by wire sawing methods. Therefore, this constraint does not seem so detrimental. Figure 2.6 shows an SEM view of an isotropically acid etched mc-Si surface. The feature size of the texturing results in pits of 1 to 10 μm in diameter, which are uniformly distributed over the Si surface regardless of grain orientation.

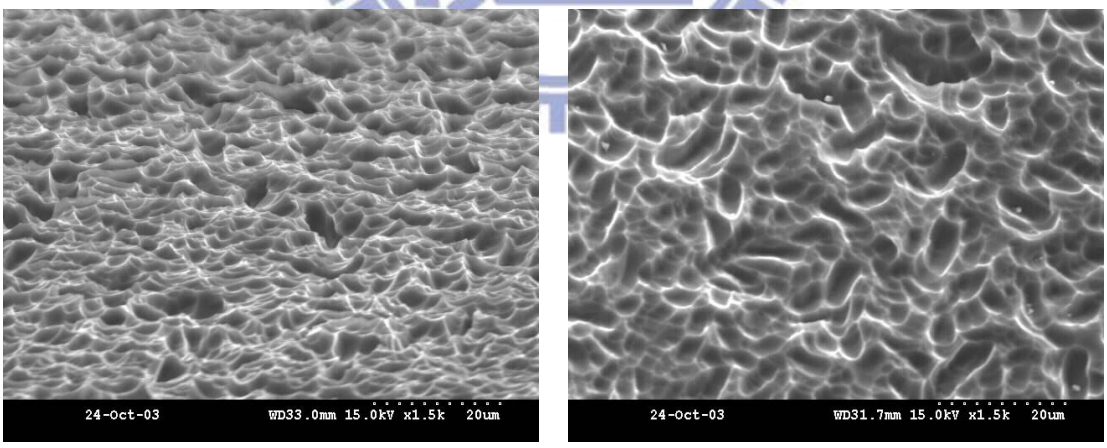


Figure 2.6 SEM image of isotropic acid texture on a mc-Si surface. Right picture is normal to the surface. The top picture is a view of the surface at a slight angle.

The acids used in the isotropic etching are similar to the acids used in the "stain etched" PS technique [6]. PS etching is applicable to all crystal types but results in poor surface passivation and has a high absorption coefficient for short wavelength photons [7].

2.4.2 Alkaline etching methods

Anisotropic etching of single-crystal Si has been widely used in the fabrication of silicon-based micro electro mechanical systems (MEMS) and microelectronic circuits; and the dissolution of Si in liquid solutions plays an important role in deep etching, micromachining, shaping, and cleaning. Aqueous alkaline solutions have been commonly used as anisotropic silicon etchant. There are two categories of etching systems, pure inorganic aqueous alkaline solutions such as KOH, NaOH, CsOH, NH_4OH, etc. and organic alkaline aqueous solutions such as EDP (ethylenediaminepyrocatechol- water), TMAH (tetramethyl ammonium hydroxide) and hyrazines

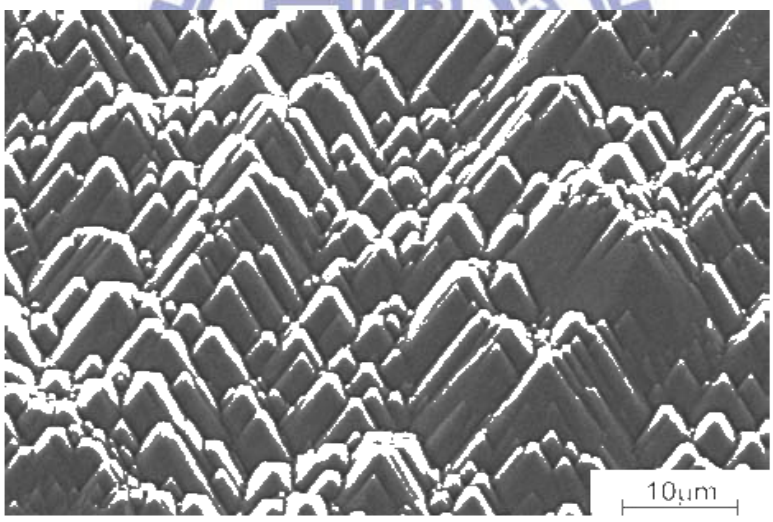


Figure 2.7 SEM micrograph of texture formed on (100) Si surface by with 40% KOH:IPA:DI H_2O and volume ratio 1:3:46 in 15 minutes at temperature 80^0C [8].

Table 2.3 Schematic diagrams of etching profiles produced in Si (100) by various etching solutions [9]

Etchants	Etching parameters	Holes		Islands	
		[h10] $_{h = 2, 3, 4}$	[100]	[h10] $_{h = 2, 3, 4}$	[100]
KOH	7,5 – 10 M 70 – 90 °C	—	(100)	(211), (221) (311), (331) (411), (441)	(100)
	15 M 60 °C	—	(100)	(211) (311) (411)	(100)
KOH + IPA	3 – 10 M 60 – 80 °C	(221) (331) (441)	(110)	(221) (331) (441)	(110)
	15 M 60 °C	—	(100) (110)	(211), (221) (311), (331) (411), (441)	(100) (110)

Chapter 3

Porous Silicon

3.1 Discovery of PS Formation.

PS was discovered in 1955 by Uhlir while trying to use an electrolytic solution to polish Si and Ge semiconductor wafers [10]. In the absence of an external stimulus via either illumination or electrical bias, Si wafers practically do not dissolve in HF. However, once a current flows through the Si/electrolyte interface or when light of sufficient energy/wavelength is incident on the silicon/electrolyte interface, the etching occurs. The dissolution takes place in the presence of holes (h^+) on the wafer surface that are then attacked by negatively charged fluorine ions [11]. In the case of current flow through the Si wafer, the reaction is accomplished by making the Si wafer the anode, and thus positive charge can be delivered to the wafer surface by increasing the current flow. This is often referred to as anodization. Depending on the current density, either electro-polishing or porous etching is achieved. Low current density acts to limit the hole injection at the surface of the Si anode and therefore only localized pits are formed, resulting in a "porous" Si surface. If a high enough current density is used, the surface is saturated with holes and polishing occurs. Figure 3.1 show the electrochemical experiment, surface morphography of PS and the total number of publications (archival journals and conference proceedings) per year since the discovery of the material to the present day.

One year after the original work, Fuller and Ditzenberger [12] reported that similar films could develop in HF–HNO_3 solutions without any externally applied electrical bias to the Si. The ''anodised'' films first received more detailed study by Turner [12] and the chemical ''stain'' films by Archer [12]. These films were not recognised as being PS, let alone a Si nanostructure, for many years. It was Watanabe and co-workers [8] who first reported their porous nature and the ease with which the material could be converted into thick Si oxide films. Pioneering Japanese work [8] on utilising this for dielectric (trench) isolation of active Si devices followed in the 1970's. However, it was Imai's so-called full isolation by porous oxidised Si (FIPOS) process [12] developed at NTT Labs, Tokyo, that prompted a significant rise in the perceived

potential of the material in the 1980's. A number of approaches to realising Si-on-insulator (SOI) circuitry were subsequently developed [8]. Nevertheless, before 1990 there were less than 200 papers published on PS, spanning a period of 35 years.

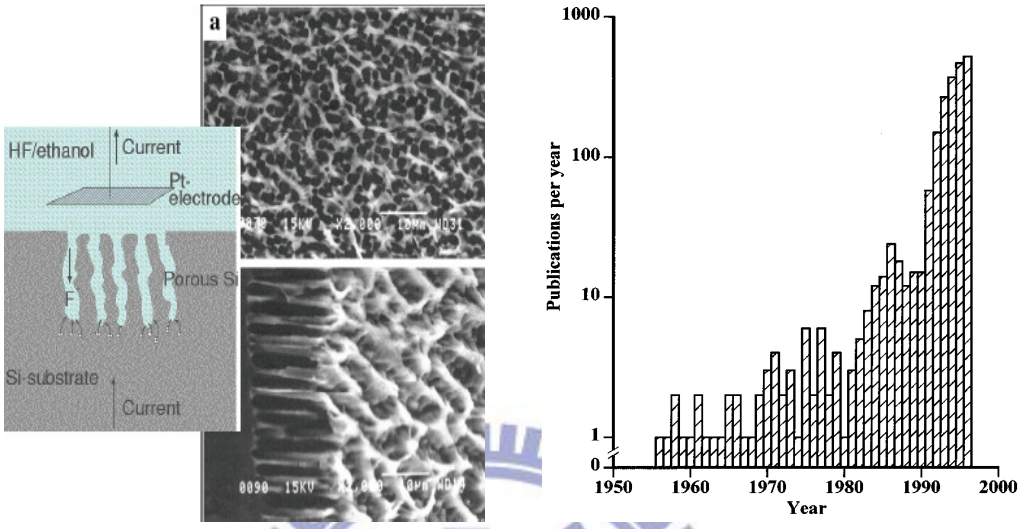


Figure 3.1 Electrochemical experiment set up and surface mophorgraphy of PS by Uhlir and total number of publications and archival journals and conference proceedings per year.

3.2 Pore type, shape, size, volume and surface area in porous silicon

3.2.1 Pore type

Figure 3.2 shows schematically several types of pore that can be created in a Si wafer or film via electrochemical etching. What distinguishes a rough surface from a porous one? In the most general sense a 'pore' is an etch pit whose depth, d, exceeds its width, w (Figure 3.2 (a)) [13]. Since at the nm scale, some increase in surface roughness generally accompanies wafer anodisation, determining the precise onset of nm wide pore formation is not straightforward. Numerous studies of ultrathin (10 - 100 nm) layers have shown that highly porous structures can be created within the first few seconds of anodisation [7]. Despite this, other workers claim anodising conditions exist whereby visibly luminescent structures are created prior to pore formation [7]. Extreme caution, however, is needed in differentiating surface roughening from incipient pore formation via surface topography measurements relying on atomic force microscopy (AFM) or scanning tunnelling microscopy (STM) alone. Such images can be significantly distorted in the vertical direction and completely miss or underestimate the depth of very narrow features [14].

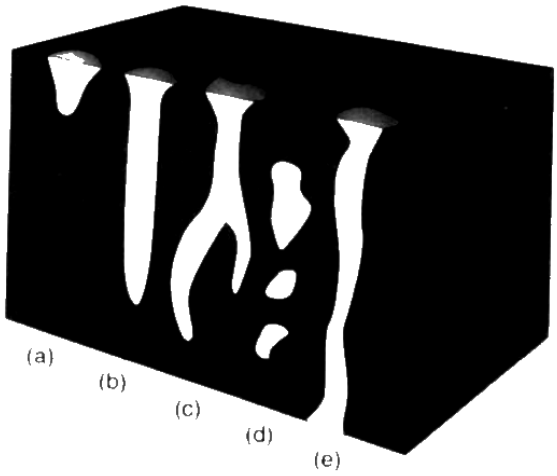


Figure 3.2 Types of pores (a,b) blind, dead-end or 'saccate', (c) interconnected or branched, (d) totally isolated or 'closed', (e) 'through' pores.

Most porous Si layers are a few μm deep and individual pores are generally closed at one end (Figure 3.2 (b)) and interconnected to some degree (Figure 3.2 (c)). Individual pore examination is most frequently made by high resolution transmission electron microscopy (HRTEM) or high resolution scanning electron microscopy (HRSEM). 'Closed' porosity (Figure 3.2 (d)) is created via capping or by thermally-induced reconstruction of the pore network [7].

Pores open at both ends (figure 3.2 (e)) can be realised in porous Si membrane structures by either extended anodisation of wafers [15], anodisation of pre-thinned areas, or the Turner 'lift-off ' technique [16]. In the latter case the current density is ramped high enough to go into the electropolish mode which results in porous overlayer detachment from its substrate. This generates so-called 'free-standing' porous Si films of typically 5 - 5 0 μm thickness that have received much study [17]. PS 'grains' or 'powder' with 'through' porosity can also be generated via laser ablation [31], mechanical abrasion [18] once dried, or ultrasonic treatment whilst wet [19].

3.2.2 Pore shape

Figure 3.3 shows schematically the major types of pore shape reported for electrochemically etched silicon. The most common shape by far is that of cylindrical pores (Figure 3.3(a)) with varying degrees of 'branching' (Figure 3.2 (c)), and 'necking'. Early Japanese studies [7] reported an 'ink-bottle' type morphology (Figure 3.3(b)) where there was a

thin surface porous film (SPF) of much smaller pore size than the rest of the layer. This type of morphology was not evident in mesoporous material but can arise in macroporous layers [7] as clearly shown by the SEM data of Zhang [20]. What is much more common for mesopores is likely to be a very gradual decrease in pore size with depth in thick layers. This arises via secondary chemical dissolution since the top of the layer is exposed to the etchant longer than the bottom of the layer [7]. The use of chemically aggressive electrolytes, excessively long anodisation times or light-assisted etching all act to generate a funnel-type shape as shown in Figure 3.3(c). Crystallographic effects on pore shape are also well documented, at least for macropores and large mesopores [7]. The anodisation of (100) oriented wafers can generate pores of square cross-section (Figure 3.3(d)) whilst (111) oriented wafers can exhibit triangular shaped pores.

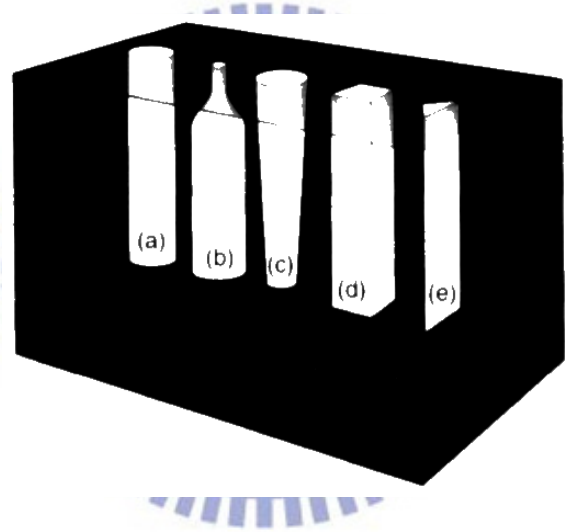


Figure 3.3 Pore shapes (a) cylindrical, (b) ink-bottle, (c) funnel (d) cuboid or slit, (e) triangular or pyramidal.

3.2.3 Pore size

Pore size determines much of the adsorptive properties of a material, and thereby is of major importance in application areas such as sensing or biofiltration. The IUPAC guidelines hence define ranges of pore size which exhibit characteristic adsorption properties [7], as shown in Table 3.1. The vast majority of electrochemically etched luminescent material studied to date is mesoporous. Wholly microporous material formation is, to date, restricted to anodisation in highly concentrated aqueous HF [7]. Such freshly etched layers typically contain

supermicropores (1 - 2 nm width) which could become ultramicropores (<1 nm width) after oxidation [7]. One NMR study has suggested that the skeleton of primarily mesoporous material is also permeated by 1.4 nm wide micropores [7]. At the other extreme, Lehmann and Gruning [7] have recently reported pore size limits achievable within a lithographically defined array of macropores, the maximum pore width attained being ~10 μm in 40 Ωcm n^- substrates.

Table 3.1 IUPAC classification of pore size

Pore width (nm)	Type of pore
≤ 2	Micro
2- 50	Meso
> 50	Macro

Clearly, pore size only has a precise meaning when the geometrical shape of the pores is well defined and known. For 'low' porosity macroporous Si, and sometimes for mesoporous Si, this is the case, but micropore shape is currently ill-defined.

3.2.4 Pore volume or void content

The 'porosity' of layers is frequently measured and may be defined as the fraction of the apparent volume of the sample attributed to pores detected by the method used, or by the apparent density. Table 3.2 shows recommended ranges for 'low', 'medium' and 'high' porosity together with application areas that primarily exploit one class of material. Porosity values ranging from as low as 4% in macroporous layers to above 95% in mesoporous material have been demonstrated. Measurement of porosity is normally carried out by a gravimetric technique with an accuracy of about 1% for large area anodisation and layer thickness of a few microns. Optical techniques have also been developed, together with means of assessing the porosity of thin 'buried' layers and layers with totally 'closed' pores [7].

Table 3.2 Classification of porosity

Void content (%)	Level of porosity	Potential application areas for porous Si
0-30	low	e.g. microcapacitors, wafer bonding, tissue bonding
30-70	medium	e.g. micromachining, sensors, silicon on insulator
70 - 100	high	e.g. light emitting diode, anti-reflection coating, non-linear optics

3.2.5 Surface area

The surface area of PS films normally quoted is the 'specific surface area', defined as the accessible area of solid surface per unit mass of material. It is very much dependent on the method, experimental conditions and size of probe used. The 'BET area', for example varies from <1 m^2 g^{-1} in macroporous Si to 800 m^2 g^{-1} in wholly microporous material. Although gas adsorption measurements are the standard technique for determining surface area, in the case of PS data based on integrated IR absorbance, etch rate in HF and interfacial capacitance has also been used [7]

3.3 Reflection and light scattering in PS

3.3.1 Reflectivity applied to PS

One of the first reflectance measurements in the visible region on PS was performed by Pickering et al [22]. They showed that in the case of p-type PS thin layers reflectance can be described with a homogeneous refractive index mainly depending on the porosity. Although the relation between porosity and the refractive index, n, is not trivial, the possibility to cover a large range of n starting from 1.25 for an oxidised p-type sample to 3 for the lowest porosity obtained with p^+ - type PS (25%) enables many optical applications of this material (these values of n are given in the near infrared (NIR)) to be considered. Reflectance measurements are not limited to the visible region. IR reflection spectroscopy has given rise to many investigations in order to analyse the inner surface composition of PS [23,24].

A synchrotron radiation source was also used in order to obtain reflectance response far in the UV (25 eV). Kramers-Kronig analysis of such reflection spectra has revealed the original

bulk silicon crystallinity in PS. Reflection measurements performed at non-normal incidence have revealed a uniaxial optical anisotropy of the refractive layer of PS. A typical reflectivity spectrum of a microporous Si layer in the NIR/visible/near UV is given in Figure 3.4 (dots).

The reflectance response can be divided into two parts due to the rapid increase of the absorption coefficient as a function of the wavenumber. In the visible region, fringe analysis requires knowledge of the real part of the refractive index and cannot be achieved without inclusion of absorption and scattering losses.

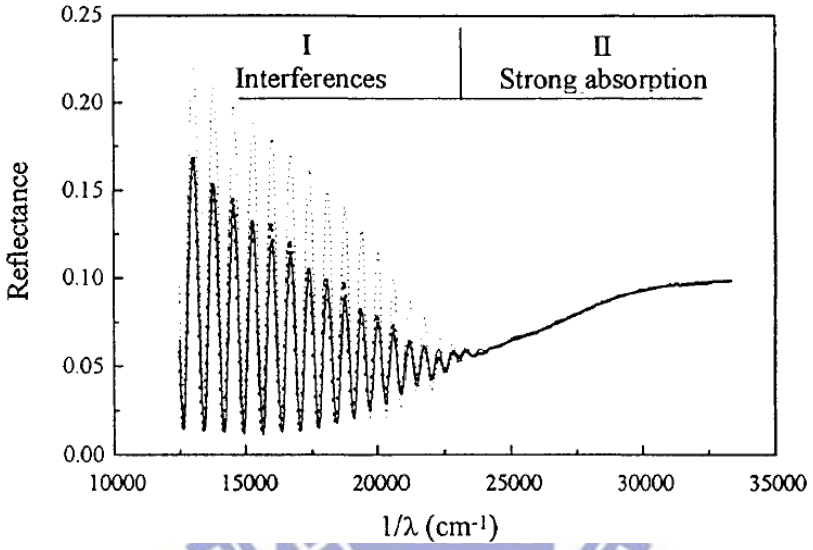


Figure 3.4 Typical reflectivity response of a p-type porous silicon layer, 4 μm in thickness and of 71% porosity (dots). The effect of the small scale fluctuations is shown comparing simulation with (line) and without (small dots) roughness. In addition, an incoherent component induced by layer thickness fluctuations of 0.5% has to be taken into account.

More generally, the reflectance response is well accounted for in PS using a homogeneous thin layer with a given thickness (4 μm) and a complex refractive index strongly depending on the wavelength. There are two contributions to layer thickness fluctuations depending on their typical periodicity: large scale fluctuations induce incoherent effects whereas small scale ones (roughness) are responsible for scattering. Reflection in the UV range is simply given by the Fresnel relation generalised in the case of a complex refractive index.

3.3.2 Light scattering and interface roughness

Optical demonstration of layer thickness fluctuations was made by a study of light scattering measurements in the case of PS. Results are summarised in Figure 3.5. There are three possibilities for the origin of the scattering in PS thin film: air/PS interface, the volume or the inner surface of the material and the PS/bulk Si interfaces. Data obtained on thick PS layers precisely follow the Fresnel law showing clearly no scattering from the volume and the first interface. Consequently, the antireflective effect on PS is simply due to a very low refractive dielectric constant [25]. On the other hand, in the case of p-type PS, scattering intensity originating from the second interface, measured after the PS layer dissolution, increases linearly with layer thickness before saturating. The level of saturation corresponds to the total reflection, which is close to the Fresnel reflection coefficient.

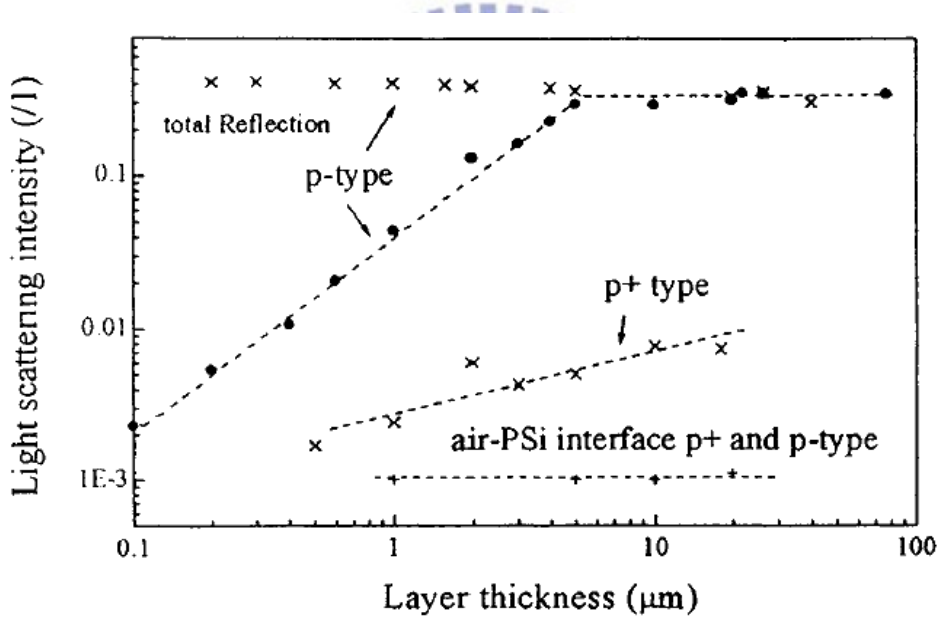


Figure 3.5 Light scattering coefficient in the case of p-type porous silicon thin layers. As an indication, total reflection in the case of p-type is also shown. Illumination wavelength was 457 nm.

A mechanical study of the interface roughness has also been achieved and is shown in Figure 3.6, representing the root mean square amplitude of the roughness, a, as a function of the layer thickness. (Note the correlation between this figure and the previous one.) It has been demonstrated that the fluctuations are isotropic in the layer plane. They are due to

inhomogeneities in the electromechanical dissolution front. They are very sensitive to electrochemical parameters, such as the current density of formation and the viscosity of the electrolyte [26]. The typical spatial periodicity of the roughness is 1 μm. Further study has revealed that due to radial doping level variation in the substrate, large scale fluctuations appear whatever the type and doping level of the substrate, with a typical periodicity of 200 μm and a level, w, comparable to the roughness.

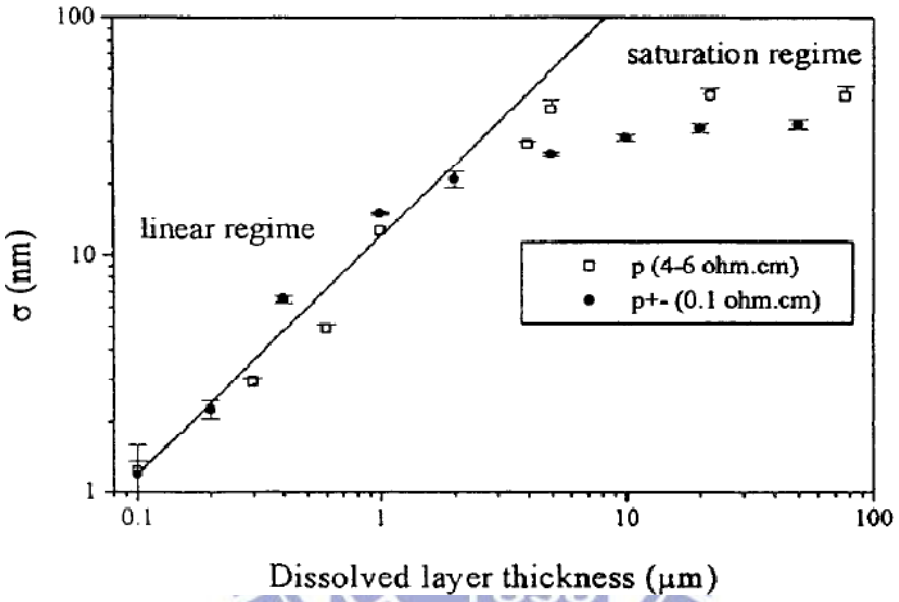


Figure 3.6 Roughness of p-type porous silicon thin layers for the two different doping levels currently used.

Important parameters for optical analysis are σ and w (fig 3.7). The latter parameter has to be dealt with by summing intensities over contributions of slightly different thicknesses, thus smearing fringes. The value of w represents typically 1% of PS thickness.

3.3.3 Reflectivity of rough interfaces

The optical system which has to be considered in the case of a PS thin layer, is shown in Figure 3.7

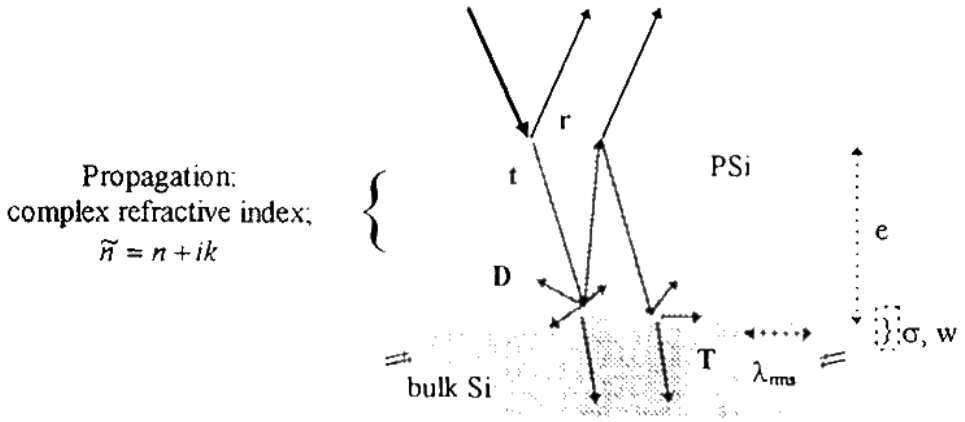


Figure 3.7 Schematic of a porous silicon layer showing the relevant optical parameters.

The Davies-Bennett relation enables the calculation of the attenuation of the reflectivity, R_s, due to the scattering [27,28]:

$$R_s = R_0 e^{-\left(\frac{4\pi\sigma n}{\lambda}\right)^2} \quad (2)$$

where R_0 is the Fresnel reflection coefficient and λ the light wavelength in vacuum. For example, for a 5 μm thick and 70% porosity p-type thin layer at 633 nm, more than 50% of the reflected energy is scattered at the PS/bulk Si interface. This relation has been introduced in the reflectivity calculation [29]. The effect of the roughness is shown in Figure 3.4 (solid line). Small dots represent the optical response when σ is kept at zero. It is clear that the contrast of the fringes in the low absorption range is also modified by the roughness level of the interface

3.4 PS formation by stain etching

3.4.1 Mechanism

The same mechanism of Si dissolution occurs during chemical formation of PS as in the electrochemical method. Similar to anodic etching (electrochemical), the key component of PS formation in the chemical (or stain etched) method is the generation of holes (h^+) at the wafer surface. This is accomplished chemically by eq. (3), where the NO is produced and serves as the h^+ injector to initiate the following reaction:

Cathode: $HNO_3 + 3\ H^+ \rightarrow NO + 2\ H_2O + 3\ h^+$ (3)

Anode: $n\ h^+ + Si + 2\ H_2O \rightarrow SiO_2 + 4\ H^+ + (4\text{-}n)\ e^-$ (4)

$$SiO_2 + 6\ HF \rightarrow H_2SiF_6 + 2\ H_2O \quad (5)$$

$$\text{Overall: } 3\ Si + 4\ HNO_3 + 18\ HF \rightarrow 3\ H_2SiF_6 + 4\ NO + 8\ H_2O + 3\ (4\text{-}n)\ h^+ + 3\ (4\text{-}n)\ e^- \quad (6)$$

where e^- is an electron and n is less than 4. The structural characteristics of PS, and especially stain etched porous silicon, are difficult to obtain. In room light, the appearance of the etched regions varies as a function of etch duration. Such differences in porous layer appearance are attributed to thin-film interference effects [9]. During the etching process, cyclic colour changes are observed which closely resemble the well characterised changes in thermally-grown SiO_2 films on Si. Such films transform from blue to green to gold (with numerous shades in between) several times as film thicknesses increase systematically from ~0.10μm up to 1.5μm.

It also has been determined that the stain etch process is catalysed by HNO_2; thus for many of the reported studies there is a necessary 'incubation' period whereby the concentrated HNO_3 is added to the HF and allowed to react for several seconds in order to initiate porous film formation. [7]

3.4.2 Stain etch PS film composition

As with anodised porous Si samples, infrared absorption spectroscopy has been commonly employed to examine the chemical composition of the films. In the mid-1960s, Beckmann [30] and Yoshioka and co-workers [31,32] independently reported the vibrational modes of these stain films etched in dilute HNO_3/concentrated HF mixtures. These bands are listed in Table 3.3

Table 3.3 Common infrared absorption bands for stain etch derived porous Si.

Wavenumber (cm^{-1})	**Assignment**	**Ref**
3700	ν(Si-OH)	[31,32]
3310	ν(Si-OH) and/or chemisorbed H_2O	[31,32]
2240	ν(-OSiH)	[33]

2117, 2145	ν(Si-H)	[33]
2085	ν($Si-H_2$)	[33]
1438	ν(NO_3)	[33]
1095	ν(Si-O-Si)	[31]
906	δ($Si-H_2$)	[33]
860	δ($Si-H_2$/oxygen) wag	[33]
733	δ(NO_3^-)	[31,32]
705	δ(O-SI-O) bend	[33]
665	δ(Si-H) wag	[33]
611*	ν(Si-Si)	[33]

*[33] notes that when corrected for substrate absorption, the Si-Si stretch actually appears at 628 cm^{-1}.

Although some of the initial assignments were incorrect, these early reports carefully noted several differences between stain etch and anodised films. These included the dominance of the intensity of the silicon monohydride (Si-H) mode at 2117 cm^{-1} over that of the SiH_2 species and the appearance of nitrate vibrations (1438 and 733 cm^{-1}) in the film as well. In a series of systematic measurements, Yoshioka [31] noted that as the HF to HNO_3 ratio in the reactant bath increased, the intensity of the modes associated with the silicon mono- and dihydride species all increased (reported by this author as 2120, 2090, and 904 cm^{-1}, respectively), while the ν (Si-OH), ν (Si-O-Si) and NO_3^- related modes (3310, 1438, 1090, and 733 cm^{-1}) all diminished in relative intensity. In a manner similar to anodised films, both the back-bonded oxyhydride ($OSiH_x$) species near 2240 cm^{-1} and the Si-O-Si mode near 1100 cm^{-1} grow in intensity upon prolonged air exposure. More recent measurements by Liu et al [33] have noted that stain etch porous Si shows unique modes at 705 cm^{-1} (assigned to the O-Si-O bending modes) and 860 cm^{-1} (SiH_2 wagging mode, shifted by oxygen), modes not common to anodised porous Si. Another unique and interesting measurement described by Steckl et al [34] noted that on stain films derived from polycrystalline Si, a broad weak absorption in the 880 - 890 cm^{-1} region (attributed to a SiH_2 bend in the presence of oxygen) is only observed in crystalline Si samples, and only these films exhibit visible PL under UV excitation. It was concluded that there

was a possible correlation between the presence of crystallinity in the initial Si substrate and the presence of surface Si oxyhydrides and visible PL in the resultant stain film.

3.4.2 Microstructure

Because of the porous and fragile nature of the films, microstructural analyses of anodised porous Si films by conventional electron microscopic methods are exceedingly difficult [35]. Stain films being even thinner than the typical micron thick layers of the anodised counterparts makes such measurements even more challenging; other alternative surface characterisation morphology tools such as AFM have been employed as a consequence [36, 37]. Shih et al [38], however, have developed a new 'minimal damage' approach for the examination of porous Si stain films by transmission electron microscopy. Their process essentially employs a 1:3:5 $HF/HNO_3/H_2O$ etch of a single crystal Si disc prepared by traditional chemical-mechanical polishing for TEM measurements. As a result, they were able to observe microcrystallites on the order of 15 to 100 $\AA$ and a pore size of 400 $\AA$ in these in-situ prepared samples.

3.5 Porous silicon (PS) for photovoltaic application

For the first time, considerable capacity of PS as the material for a Si PVs was noted in papers [39-41]. Herein, the following ways and advantages of PS PV application were formulated, proceeding from the analysis of microstructure and properties of this material:

- The surface of the PS is highly texturized, which enhances light trapping and reduces reflection losses. It can be used for creation of antireflecting coatings for Si solar cell.
- The possibility of technological control of band-gap of PS (from 1.5 up to 1.8 eV) may be utilized to optimize sunlight absorption. In second, its wide bandgap may make it a candidate for the window layer in a heterojunction cell or as the base material for the top cell in a tandem construction. The wide bandgap may also be used to realise front or rear surface in a diffusion junction Si solar cell.
- PS can be used for solar light transformation from an ultraviolet range (thanks to it's luminescent properties) in more long wavelength range, it's optimum for photovoltaic conversion in silicon SC.

- The PS developed surface alongside with its high chemical activity can serve for effective impurity gettering in silicon solar cell substrates.
- The simplicity of PS technological formation and using of its electrochemical growth technology on silicon large area wafers particularly appealing for solar cell cheap fabrication.

To the present time practical approbation in the PV application field have passed only the first and second points of the unique properties PS considered above. It is possible to explain this phenomenon only considering the problems, which arise on a way of inclusion the PS to SC structure [42]. At first, this is a PS high specific resistance, which limits an effective carriers transport in a material volume. Secondly, there is insufficient understanding of the mechanism of generation and collection of photogenerated carriers in PS. It prevents the creation of a high efficiency SC design on its basis. Thirdly, it is a low mechanical strength of PS layers (especially with a high porosity) and also their insufficient thermal conductivity and high sensitivity to high-temperature processing. It actually is a problem of stability of this material during SC fabrication. The detailed consideration and experience analysis of PS utilization in silicon SC structures is given further. The special attention to positive results achieved in this area, is given. Thus their physical interpretation based on a known experimental material about the nature and properties of PS also is considered separate.

3.6 Anti reflecting coating on electrochemical porous silicon base

For the first time the attention of the PV specialists was concentrated on PS in 80 years thanking its porous nature of a rough surface, low refractive index and blue shift of fundamental absorption edge (Fig. 3.8) [43]. These properties of PS assumed its availability as a material of an antireflecting coating for Si SC. The first experimental researches in this direction were carried out by Prasad et al. [44]. The authors of this paper used the por-Si layer for reflection reduction of polycrystalline SC with diffusion p^+ - n junction by depth 0.6 μm. Conventional electrochemical anodization for PS layer formation was not used. It was a method of photostimulated chemical etching. Thus the PS growth in the HF- based electrolyte take due to a course of a photocurrent, induced in structure with p^+ - n junction by electrical illumination. A

porous film thickness supervised on changing its interference colour. It might be typically 74 ± 2 nm.

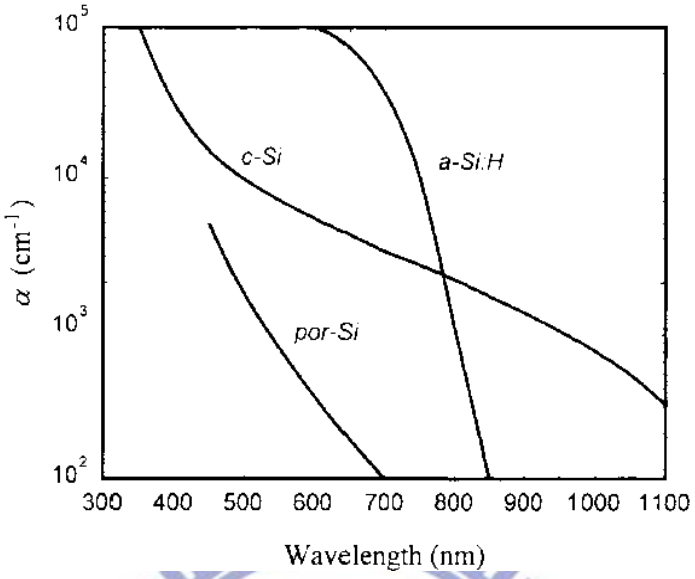


Figure 3.8 Optical absorption coefficient versus wavelength for self-supporting 20 mm thick PS layer. Data for crystalline Si and amorphous Si:H is also shown

Ellipsometric measurements determined the refractive index of the PS layer. It was in arange 1.95 ± 0.05. Such thin frontal layer of the PS in the silicon SC structure reduces its optical losses from 37 to 8% (Fig. 3.9) and increases a short-circuit current by 25% and open-circuit voltage by 20 mV, as experimental researches have shown. If the nonreflecting properties can explain such essential increase of a photocurrent, the gain of a SC output voltage is a result of a passivation by the PS layer of a Si surface and as a consequence a reduction of a saturation current. The PS antireflecting coating insignificantly influences on the form of the current-voltage characteristic of SC shown in fig 3.9. Thus such characteristics as the fill factor, series and shunting resistance essentially did not vary. It is important that the PS antireflecting coatings have demonstrated the weatherproof fact during several months.

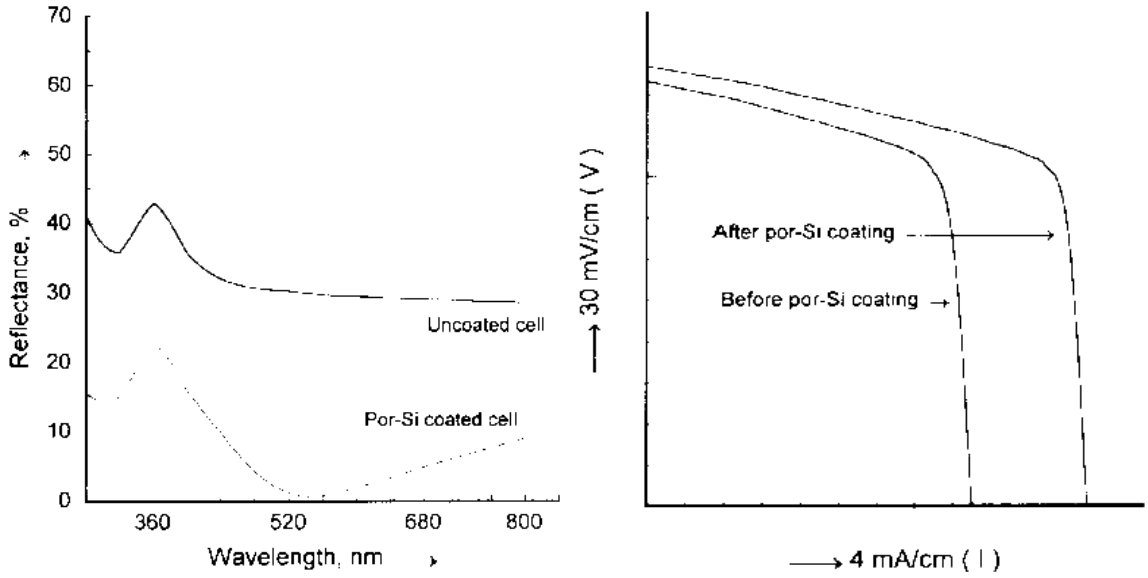


Figure 3.9 Spectral reflectance and illuminated I-V characteristics of polycrystalline solar cells with and without PS coating [44]

The researching of PS based antireflecting coverings was continued after more than ten years interruption. At that PS layer was formed on a surface of c-Si wafers by an electrochemical anodization and its thickness about 10 mm. The integrated reflectance of such nonreflecting coating changes from 1.6 to 3.4% in a spectral range from 400 to 900 nm have shown measurements of optical losses. The received results are compared on efficiency with the best antireflecting coatings of the double MgF_2/ZnS layer on the basis put on a texturized Si surface [1]. At the same time, if similar PS layer to use on a substrate surface of polycrystalline Si, the integrated reflective ability decreases only up to 10% for light waves with length from 400 to 900 nm [41].

The antireflecting coating in SC structure with dot contact has given effect of increase efficiency in consequence of optical losses minimization. But this effect was accompanied by a degradation of an open-circuit voltage and short circuit current in time [41]. Dependence of porous layer reflectance of its porosity is investigated as PS parameter optimization necessity for its using as silicon SC antireflecting coating. It was established that the lowest coefficient of PS reflection is reached with its porosity about 70% (Fig. 3.10). Thickness optimization of an antireflecting coating was carried out as porous layer surface optical reflection minimization.

The integrated reflectance of PS layer a little bit depends from a type and doping degree of an initial polycrystalline substrate was established eventually and it changes in a spectral range 350 - 1120 nm from 4.7 to 4.9% (Fig. 3.11).

The further researches of Si SC with PS frontal layer have confirmed its antireflecting properties, but essential increase of photoconversion efficiency could not demonstrate in consequence of the unoptimized structure of a SC. The results of subsequent papers [45-47] were more successful.

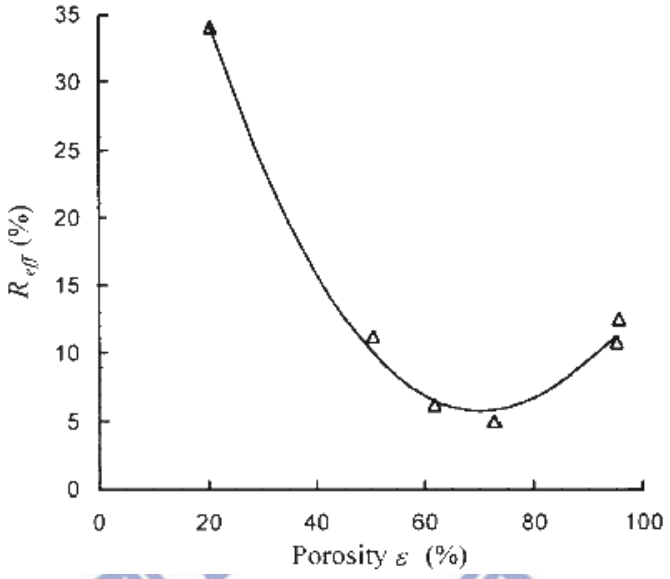


Figure 3.10 Effective reflectance coefficient as a function of E, the measured porosity of the PS layers [1].

The result of paper [47] was the SC with the 5 x 5 cm^2 area. PS layer on its frontal surface was received by chemical etching in solutions with controllable composition. Efficiency of this SC under AM 1.5 illumination was 14.1%. However its spectral sensitivity, extended in infra-red range, and high quality of a surface passivation testify to a potential opportunity of the further increase of the output characteristics of this type of SC.

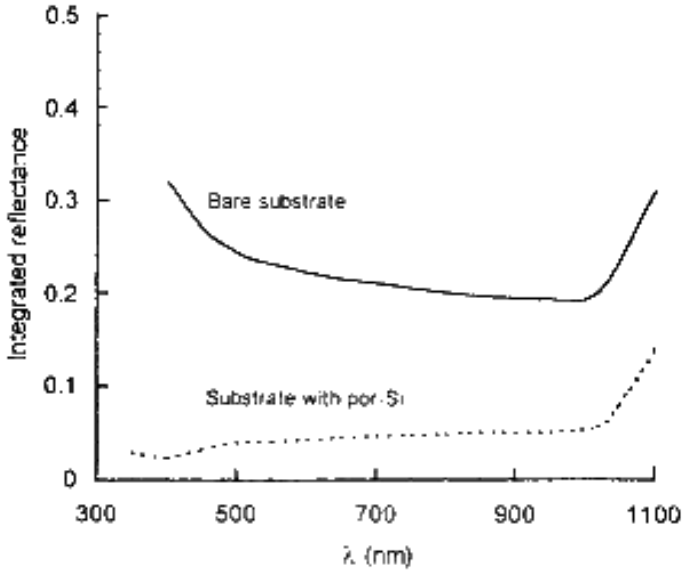


Figure 3.11 Integrated reflectance of a PS layer formed on a p doped, 1 Ωcm, as cut, polycrystalline wafer (Wacker, SILSO). The reflectance of bare substrate is also shown.

The result of paper [47] was the SC with the 5 x 5 cm^2 area. PS layer on its frontal surface was received by chemical etching in solutions with controllable composition. Efficiency of this SC under AM 1.5 illumination was 14.1%. However its spectral sensitivity, extended in infra-red range, and high quality of a surface passivation testify to a potential opportunity of the further increase of the output characteristics of this type of SC.

Reference [48] has presented the most wide-ranging and productive researches of influence of a thin frontal PS layer on photoelectric properties of the multicrystalline SC. The parameter optimization of a porous layer as for optical losses minimization on a reflection, as for achievement of the maximum of the output characteristics SC was its purpose. These two directions are incompatible among themselves, but even in some cases are opposite on technological realization for the first time was shown. This conclusion is based on the fact that the increase of PS layer thickness which is necessary for optical losses decreasing simultaneously conducts to increase of series resistance of structure SC and lowers its fill factor. This was illustrated most clearly in [48] by the dependence of output parameters of SC on the charge value passed through the device structure during process of the PS layer formation. (Fig. 3.12). As it follows from Fig. 3.12, there is certain value of the charge (and, consequently, thickness of the porous layer), when the output electrical characteristics begin to decrease

sharply at exceedance of it. This means, that to reach maximal positive effect from the use of antireflective PS layer in the structure of SC is possible only under detailed optimisation of its parameters.

According to the results of ref [49] the optimal parameters of the por-Si- based antireflecting coating for multicrystalline SC studied with shallow (0.4 mm) n^+ - p junction are the following: thickness 80 nm, porosity 69%, refraction index 1.64. The use of such optimised PS layer in structure of SC has allowed to increase the short-circuit current of the SC more than by 20% and improve the effciency from 7.5 - 8.5 to 10 - 11%. The increase of photoresponse of the PS/ n^+-multi-Si/p^- multi-Si structures.

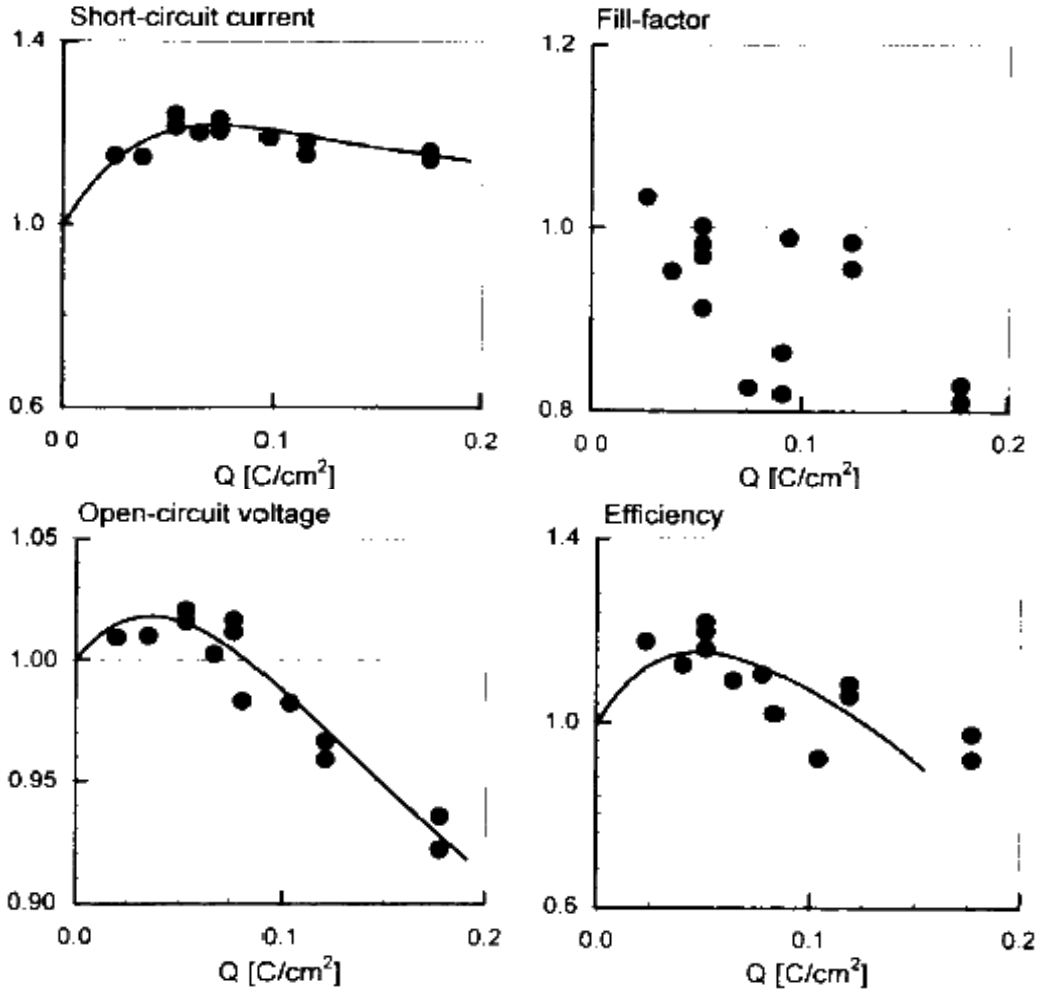


Figure 3.12 Multicrystalline solar cell parameters as a function of the electrical charge passed through the cell during anodization. The data are normalised to the values before anodization

In conclusion, PS formation is simple and is accomplished by either electrochemical or chemical etching but is still not completely understood or developed for PV. PS offers a low-cost and high through-put route to surface texturing and can also serve as an anti-reflection coating. This provided the motivation to understand and develop low-cost manufacturable porous silicon etching for crystalline Si cells understood or developed for PV. Porous silicon offers a low-cost and high through-put route to surface texturing and can also serve as an anti-reflection coating.

3.7 Applications and Limitations of Stain Etching Porous Silicon for Solar Cells

PS also offers potential for cost reduction through low-cost ARC applications as well as increased through-put. So far, the use of PS for ARC has been the most widely investigated. The typical process sequence for an industrial type solar cell using PS is shown in Figure 3.13. Traditionally, the Ps etch has been implemented after junction formation and metallization. This approach can lead to selective emitter formation, proper surface reflectance, hydrogen surface passivation, and good electrical contact. However, there are some major drawbacks of the PSetch at the end of the SC process. The porous silicon etch attacks the screen-printed metal contacts and results in Fill Factor (FF) degradation and a high surface recombination velocity. In addition, a heavily diffused emitter with a junction depth of ~1.0 μm is necessary to avoid destruction of the emitter during porous silicon etching. The highly reactive surface causes concern over the longevity of the solar cell in the field.

Initial investigations of PS ARCs and surface passivation were made in the mid 1990s. Although early work cited the effectiveness of a very thin porous layer (< 0.1 μm) to reduce the reflectance from 37% on bare Si to 8% [50]. It was shown that etching time, porosity, current or HNO_3 concentration, and layer thickness control the reflectance of porous silicon [1]

Many investigations claimed various R_w values for chemical and electrochemical etching methods [50, 51]. Some groups obtained better reflectance values using the electrochemical process than with the chemical or stain etch process. However, this trend is not replicated in all studies. Figure 3.14 shows some reflectance curves in the wavelength range of interest. The R_w of a bare Si sample can be reduced from ~37% down to ~5 to 6% [21]. It can be comparable to

the R_w achieved by a double layer ARC of ZnS + MgF_2, which is the premium coating in solar cell processing.

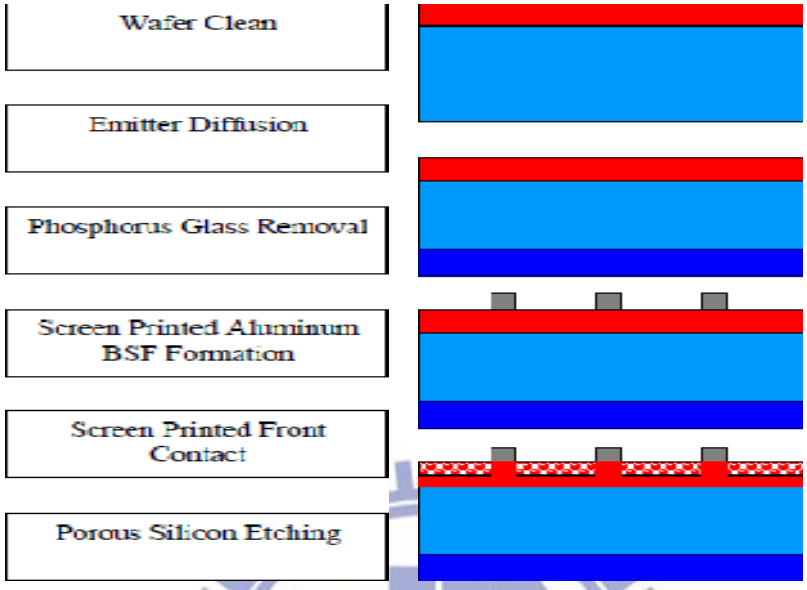


Figure 3.13 Typical process steps for a PS ARC solar cell [1]

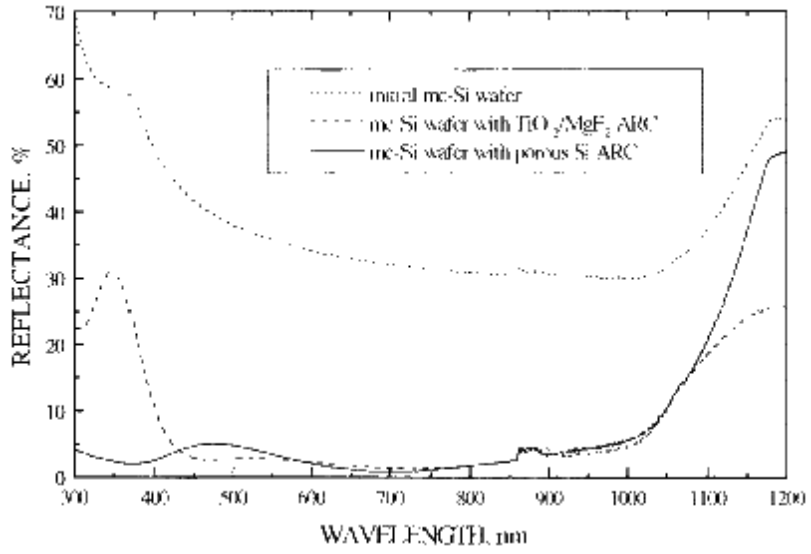


Figure 3.14 Reflectance characteristics of non-textured mc-Si wafer after PS formation by stain etching and pre-textured mc-Si wafer with Double Layer Anti Reflectance Coating (DLARC).

Although the reflectance values that can be achieved are among the very best possible, there are some additional considerations that arise with the use of PS. If porous silicon is formed early in a solar cell process, the high temperature endurance needs to be considered, as well as the junction formation technique used for a uniform diffusion. Figure 3.15 shows the progress in efficiency of Si cells using porous Si texturing. A conversion efficiency of 14.1% (25 cm^2) on a large area mc-Si sample was achieved with evaporated contacts [52]. It was shown that the photocurrent (J_{sc}) increased ~40% and the open circuit voltage improved by 4 to 6 mV over a bare Si surface. No FF degradation was observed because evaporated contacts were used in conjunction with the relatively short etch time (< 4s). The improved J_{sc} was attributed to ARC and removal of Figure 3.15. Reflectance characteristics of non-textured mc-Si wafer after PS formation by stain etching and pre-textured mc-Si wafer with DLARC heavy doping effects that cause photo-generated carriers to recombine in the emitter because of Auger mechanisms before being collected.

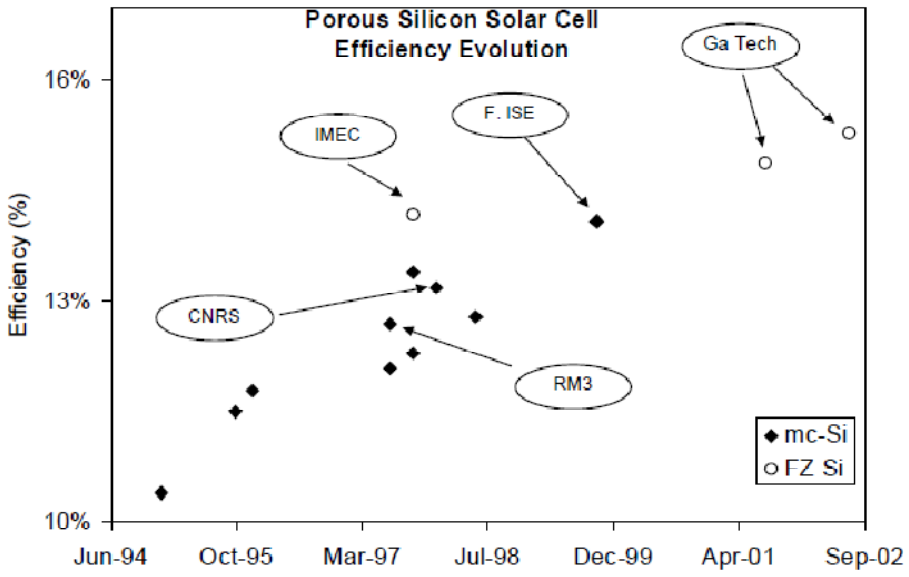


Figure 3.15 Efficiency evolution for all solar cells using porous silicon as part of the solar cell design [54, 55].

Most investigations implement PS as a final step in the process sequence. This is to take advantage of the selective emitter formation in addition to surface texture and ARC (fig. 3.13). Unfortunately, the PS etch attacks screen-printed metal contacts, resulting in lower device performance along with a highly reactive surface. Matic et al. [53] tried PS etching prior to screen-printed metallization in an effort to achieve a more stable surface, with no contact

degradation. They showed that PS ARC quality was not greatly altered during the screen-printed metal firing step at 800-900^{o}C [53], thus demonstrating a new possibility for ARC and contact preservation. A major drawback for such a process sequence may arise because of the possibility of the extremely high series resistance of the PS layer underneath the contacts, which translates into low FF (high series resistance) and reduced cell efficiency.

Based on the literature search, the advantages and disadvantages of industrially viable Si SCs with porous silicon ARC are summarized below.

3.7.1 Potential Advantages

1. PS texturing does not depend on crystallographic orientation. Therefore mc-Si of all kinds can be textured.
2. The ARC can be optimized by tailoring the porosity (or refractive index) of the PS layer for a given cell structure.
3. PS etching allows for selective emitter formation to improve the short wavelength (300 to 500 nm) response.
4. Partial shaving of the heavily diffused emitter region reduces heavy doping effects during PS etching.
5. PS serves as an effective light diffuser with an effective light entrance angle of 60^{o} [56] that could improve collection efficiency of photo-generated carriers.
6. Good surface passivation may be achieved by hydrogen terminated surface states (Si-H stretching mode) [56] or through band-edge discontinuity resulting from higher bandgap of PS.
7. PS formation is simple and industrially scalable.
8. Using a PS anti-reflection coating instead of the traditional SiN layer saves a significant amount of time and avoids the cost associated with a plasma deposition machine.

9. The formation of the PS layer allows for higher through-put (<10 seconds).

3.7.2 Potential Disadvantages [1]

1. The PS etching attacks screen-printed contacts, resulting in a lower FF and decreased efficiency.

2. A deeper emitter diffusion is required to avoid shunting and junction removal during etching. To achieve > 0.65μm phosphorus diffusion, more time at a high temperature is needed, potentially reducing through-put.

3. PS etching as the final processing step does not allow for surface passivation.

4. If PS is formed after emitter diffusion and before metallization, a high series resistance is realized because of the PS layer.

5. PS etched surfaces do not withstand conventional phosphorus diffusion and glass removal. Therefore, the use of porous silicon anti-reflection coatings must be formed after the phosphorus emitter diffusion.

6. The implementation of PS ARC as the final processing step could result in the loss of device performance and reproducibility.

7. There are appreciable absorption losses in porous silicon layers as a result of direct bandgap behavior that decreases the short wavelength response (300 to 500 nm) [24].

Chapter 4

Fabrication Process and Measurement

In this chapter, the fabrication process for PS in p-type silicon wafer (100) orientation is discussed. Using stain etching, Si wafers were dipped into different ratios of HF: HNO_3 and HF: HNO_3+ H_2O solution to form porous layers. The HF, HNO_3, and H_2O proportion were optimized to make PS layer with the lowest reflectance in the wavelength region from 200 to 1000 nm The acid etchant were divided into three group such as HF dominant(group I), HNO_3 dominant (group II) and acid mixtures adding water (group III) . For industrial purpose, not only small wafer (2 x 2 cm) but also large wafer (7.5 x 7.5 cm) was used to form the porous layer. The measured reflectivity of PS layer is compared with the conventional ARCs layer such as PECVD Si_3N_4 and SiO_2. In additional, porous formation of different type of Si wafers is also investigated

The fabrication process of the PS in this study includes:

1. Wafer cleaning.
2. Initial weight (m_1) measurement.
3. Wafer cleaning (second times)
4. Stain etching to create PS layer.
5. Wafer cleaning in DI water.
6. Weight measurement after etching (m_2)

4.1 Deposition of Si_3N_4 and SiO_2

Plasma-enhanced chemical vapor deposition (PECVD) is a commonly used process to deposit thin films from a gas state (vapor) to a solid state on a substrate. PECVD is an excellent approach for depositing a variety of thin films at lower temperature than those utilized in CVD

reactors without settling for lesser film quality. Chemical reactions are involved in the process, which occur after the creation from plasma of the reacting gases. The plasma is generally created by RF (AC) frequency or DC discharge between two electrodes, the space between which is filled with the reacting gases.

Plasma is a state in which a significant percentage of the atoms or molecules are ionized. Fractional ionization in plasmas used for deposition and related materials processing varies from about 10^{-4} in typical capacitive discharges to as high as 5–10% in high density inductive plasmas. These atomic and molecular fragments interact with a substrate and, depending on the nature of these interactions, either etching or deposition processes occur at the substrate. Since the formation of the reactive and energetic species in the gas phase occurs by collision in the gas phase, the substrate can be maintained at a low temperature. Therefore, film formation can be occurred on substrate at a lower temperature than possible in the conventional CVD process. This is the crucial advantage of PECVD.

In this study, silicon dioxide (SiO_2) deposited from silane (SiH_4) and oxygen (O_2), typically at pressures from a few hundred millitorr to a few torr. Plasma-deposited silicon nitride (Si_3N_4), formed from silane and ammonia (NH_3) with nitrogen (N_2) as carrier gas in the PECVD system (STS 300 PC series – 310PC) located in Compound Semiconductor Device laboratory (CSD Lab) as shown in figure 4.1.

The reaction for SiO_2 , Si_3N_4 formation are showed below :

$$SiH_4 + O_2 \rightleftharpoons SiO_2 + 2H_2 \qquad (7)$$

$$SiH_4 + NH_3 \longrightarrow SiN : H + 3H_2$$

$$SiH_4 + N_2 \longrightarrow SiN : H + 3H_2$$

Carrier gas N_2 had a flow rate of sccm during film deposition.

Figure 4.1 PECVD system (STS 300 PC series – 310PC)

4.2 Morphology Analysis Instruments

4.2.1 Scanning Electron Microscope (SEM) [57]

The scanning electron microscope (SEM) is instrument that images the sample surface by scanning it with a high-energy beam of electrons. The electrons interact with the atoms that make up the sample producing signals that contain information about the sample's surface topography, composition and other properties such as electrical conductivity.

The electron beam, which typically has an energy ranging from 0.5 keV to 40 keV, is focused by one or two condenser lenses to a spot about 0.4 nm to 5 nm in diameter. The beam passes through pairs of scanning coils or pairs of deflector plates in the electron column, typically in the final lens, which deflect the beam in the x and y axes so that it scans in a raster fashion over a rectangular area of the sample surface. The design of SEM system is shown in Figure 4.2

Magnification in a SEM can be controlled over a range of up to 6 orders of magnitude from about 10 to 500,000 times. Unlike optical and transmission electron microscopes, image magnification in the SEM is not a function of the power of the objective lens.

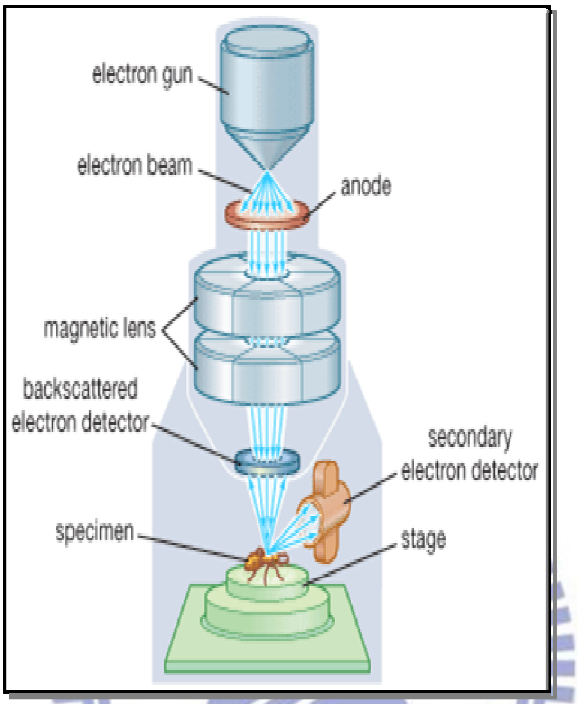


Figure 4.2 SEM schematic

4.2.2 Atomic Force Microscope (AFM) [58]

AFM or scanning probe microscope (SPM) is widely used to measure the surface morphology or features on the surface of sample. The precursor to the AFM, the scanning tunneling microscope (STM), was developed by Gerd Binnig and Heinrich Rohrer in the early 1980s at IBM Research – Zurich. Later on, that development earned them the Nobel Prize for Physics in 1986. Binnig, Quate and Gerber invented the first AFM in 1986.

The AFM consists of a cantilever with a sharp tip (probe) at its end that is used to scan the specimen surface. The cantilever is typically Si or Si_3N_4 with a tip radius of curvature on the order of nanometers. When the tip is brought into proximity of a sample surface, forces between the tip and the sample lead to a deflection of the cantilever according to Hooke's law. Depending

on the situation, forces that are measured in AFM include a lot of forces such as mechanical contact force, van der Waals forces, capillary forces, chemical bonding, electrostatic forces, magnetic forces, Casimir forces, solvation forces,…Conventionally, the deflection of tip is measured by using a laser spot reflected from the top surface of the cantilever into an array of photodiodes.

The feedback mechanism of tip bending employed to adjust the tip-to-sample distance to maintain a constant force between tip and sample. The AFM can be operated in a number of modes, depending on the application. In general, possible imaging modes are divided into contact modes (tapping modes) and non-contact modes where the cantilever is vibrated. In contact modes, the tip contact the surface, the force between tip and surface is kept constant during measurement. In the contrast, in non-contact mode, the tip of cantilever does not tapping the sample surface. The cantilever is instead vibrated at a frequency slightly above its resonance frequency where the amplitude of oscillation is typically a few nanometers (<10 nm).

The non- contact mode is preferable to contact mode because it does not suffer from tip or sample degradation effects. Figure 4.3 shows the schematic and typical cantilever tip respectively.

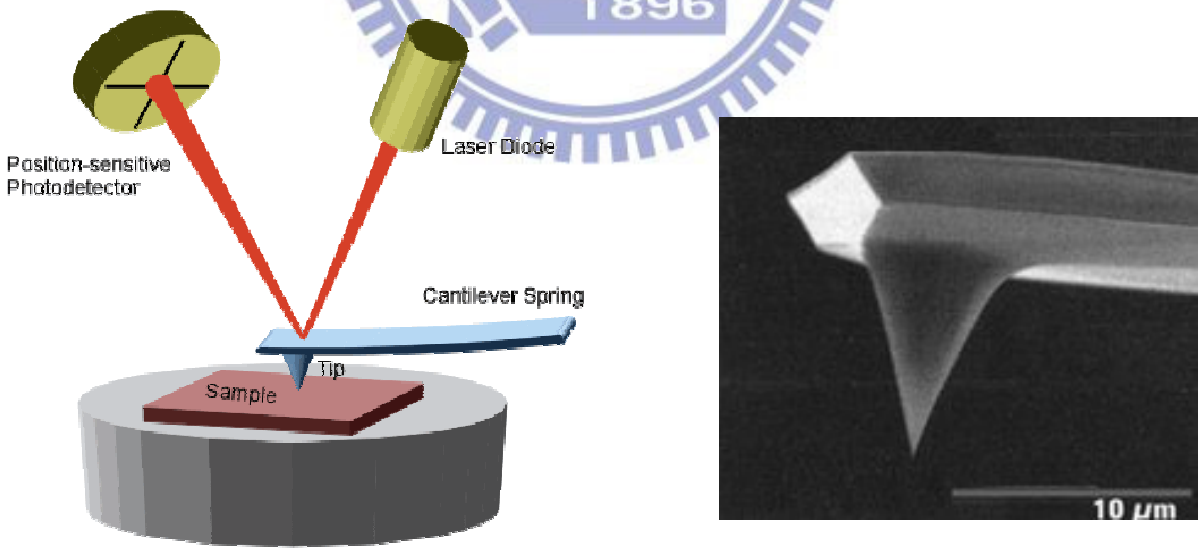


Figure 4.3 TEM operating principle and typical cantilever tip

4.3 Reflectance Measurement

The reflectance of PS layer and PECVD Si_3N_4, SiO_2 were measured using an n&k analyzer (model 1200, N&K Tech. Inc.) Deuterium and tungsten lamp were used in this instrument, which can provide the reflectance for the wavelength range from 190nm to 1000nm. n&k analyzer system is showed in Figure 4.4

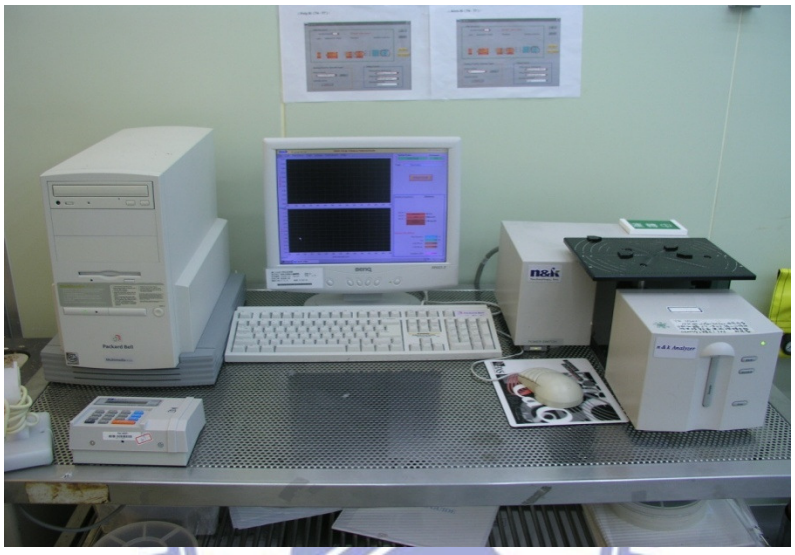


Figure 4.4 n&k analyzer system

4.4 Gravimetric analysis, electron phonon scattering (EPS) and Photoluminescence (PL)

Gravimetric analysis describes a set of methods in analytical chemistry for the quantitative determination of an analyte based on the mass of a solid [59]. Etching rate can be calculated by equation (3)

$$\text{Etching rate} = \quad r = \frac{\Delta d}{t_{\text{etch}}} = \frac{\Delta m}{t_{\text{etch}}} \frac{1}{A\rho(\text{Si})} \qquad (8)$$

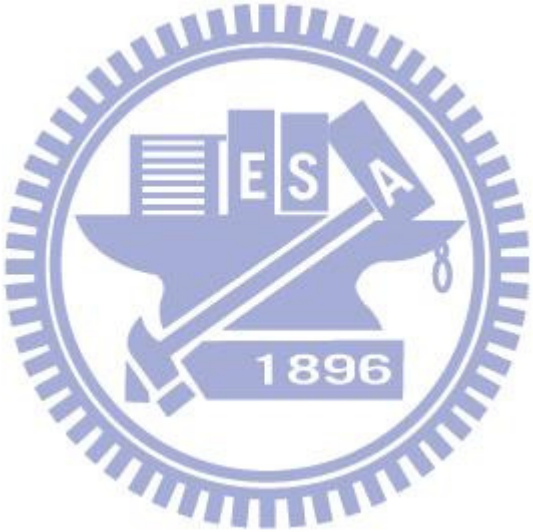
where $\Delta m = m_1 - m_2$: weight loss (g).

t : etching time (s).

A : initial surface area (cm^2).

ρ = 2.33g/cm^3 for silicon.

In addition, EPS and PL measure were used to test the composition on top of etched surface and PL properties of PS.



Chapter 5

Results and Discussion

5.1 Formation of PS

5.1.1 Experimental

In this study, we have modified the surfaces of single crystalline wafer by stain etching in a variety of aqueous HF, HNO_3 and H_2O. Silicon wafer (p-type, boron doped) with both (100) (1-12 Ωcm) and (111) orientations have been subjected to HF:HNO_3, HF:HNO_3 + H_2O solutions at room temperature. The proportions of assay HF, HNO_3 were varied from 10% to 90% in volume. To obtain a producible porous silicon layer by HF/HNO_3 etching, the role of each component of the solution must be understood. Three groups of etchant were employed such as HF-dominant, HNO_3-dominant and HF: HNO_3 + H_2O.

The silicon wafer was first cleaned in HF: H_2O (1:100) and dried with N_2 flux to remove dust and any unwanted oxide on the silicon surface. Then, the wafers were weighed to measure the initial weight following gravimetric analysis method as mentioned in chapter 4. In the third step, the silicon wafer was cleaned again in HF: H_2O and N_2 flux. After that, the wafer was subjected into etchant solutions for few seconds to create the porous layer. Finally, etched wafer cleaned by DI water, N_2 flux and weighed again to get the weight after etching process. The overall process is shown in Fig 5.1.

After the etching process, the reflectance of etched wafers was tested by n&k measurement. Etching process modified not only in optical properties but also the surface morphology of wafer. In order to investigate the relations among etching parameters and film morphology. AFM, SEM analysis were carrying to figure out the effect of acid etchant.

5.1.2 Results and Discussion

After a few second (10-180s) of etching process, the acid etchant reduced the reflectance of original substrate (Si (100)) to below 5%. Figure 5.3 shows total reflectance for PS layers etched in a solution HF: HNO_3 + H_2O (7:3 + 70) with different etching times. The reflectance reduces with the increase of etching time. At wavelength 200- 400 nm, the reflectance shifts toward longer wavelength and reduced to 5% after 180s etched in the acid mixture. The result is consistent with the literature, where PS is known to behave similar to a SiO_2 layer with increasing thickness. Thus, when the PS layer becomes thicker, the corresponding wavelength for destructive interference ($2nd = \lambda/4$) increase. The reflectance of porous layer will also be compared with the PECVD conventional Si_3N_4 and SiO_2 AR coating to test the capability of PS to replace the traditional ARCs.

SEM observations show that the stain etched PS films are quite similar to PS obtained by electrochemical etching. Theses hillocks have previously been associated with chemically etched porous silicon and again in this study we note their presence without exception. The flat and smooth surface (fig 5.3 a) was changed to very rough surface with lots of pore sites. The top surface of substrate is seen decorated with micro-size crates (fig 5.3 b). The smaller pore site with nano particles can be seen at the higher magnification SEM image (fig 5.3 c) which can explain the trapping light effect as we have discussed in chapter 3.

By using isotropically stain etching, surface have been successfully fabricated the porous layer on top of the silicon wafer. The effect of acid proportion in etching solution is also compared with the enhancement of light trapping effect. PS layer provides very low reflectance as compared to the untreated substrate. Further parts in this thesis will give more evidence to show that the conventional ARC materials could be replaced by the PS layer.

5.2 Effect of proportion HF, HNO_3 in porous formation

5.2.1 HF dominant group

In the etchants of type 1, the proportion of hydrofluoric is larger than that of nitric acid. The total volume of etchant were kept instant about 200ml. Specifically, HF: HNO_3 = 9:1, 4:1, 7:3, 2:1.

Figure 5.4 shows the comparison of total reflectance between the PS samples prepared with different etchants. As we can see, at the wavelength 200-1000nm, three types of ratio i.e 4:1, 9:1, 7:3 reduced the reflectance to almost 0%. The HF will remove the Si which is oxidized by the HNO_3. It is found out that HNO_3 acts as the key component in stain etching. Figure 5.5 shows the average etching rate (AER) as the function of HNO_3 ratio. When the HF proportion was decrease (HNO_3 proportion increase), the AER tended to rapidly increase from 4.12μm/s (ratio 9:1) to 17.55μm/s (ratio 2:1). As a result, the sample etched in ratio 2:1 became very thin with lots of damages on the surface which may explain why ratio 2:1 has higher total reflectance than the others. The stain etching at very high etching rate caused the sereve damage to the substrate.

Structurally, the surface morphology remarkably changes when the substrates were subjected into the etchant mixture. Figure 5.6 describes three types of porous such as micro-, macro-, and meso-porous based on the size of the pore. The sample etched at ratio 2:1 offers micro-porous with closed pore shape. Figure 5.7 shows the PL spectra of these samples. The sample etched at ratio 9:1 exhibit the highest PL intensity due to major population on silicon nanocrystals [60] in comparison with sample etched at ratio 4:1. However, the sample etched at ratios 7:3, 2:1 do not have any PL peak. As we all know, silicon is indirect bandgap material which mean does not has PL peak. Porous layer shows the response in red light which proves that the photoluminescence properties of porous silicon.

5.2.2 HNO_3 dominant group

For the etchant of type 2, the converse is true, with the proportion of nitric acid is higher than hydrofluoric acid.The ratios of HF: HNO_3 used are 1:9, 6:40, 8:40, 3:7 (90%, 86.95, 83.33 and 70% HNO_3 in volume, respectively). Starostina [61] has reported that if nitric acid proportion is larger than hydrofluoric acid, no porous silicon forms. These samples in this group once again prove that conclusion is correct. As can be seen in fig 5.10, the surfaces of all samples are smooth. There is no clue of porous layer on these sample surface surface. As a result, the reflectance of all these samples except the one etched by ratio 3:7 are similar to that of the bare wafer . This means that the etchant mixture does not have any effect on these substrates (fig 5.8). In the other hand, for the sample etched at ratio 3:7, the total reflectance reduced by about 30% in the visible light and AER higher than other samples (1.29μm/s > 0.53μm/s > 0.27μm/s ~ 0.27μm/s, respectively) as described in fig 5.9. With the increasing of nitric acid proportion, the average etching rate decrease. It is observed that with this type of etchant, porous formation shift to polishing etching by gradual decrease in the proportion of the acids.

The formation of porous silicon in HF: HNO_3 etchants is investigated. Porous silicon with uniform surface morphology, low reflectance (~0%) in the wavelength 200-1000nm are produced. Different types of porous structure (micro-, meso-, and macro-porous) have been fabricated. These experiments have also shown the transition from etch polishing to porous formation by controlling the proportion of nitric acid and hydrofluoric acid. Figure 5.11 clearly shows two regions of stain etching. When the proportion of nitric acid is lower than 40% in volume, porous etching occurs. The average etching rate also increases with the increases of nitric acid volume. The transition between porous formation and polishing etching appears when nitric acid content is lager than 40%, when the average etching rate reduced rapidly. Porous formation transfers to polishing etching with smooth surface. Figure 5.12 shows the PL response for porous formation and polishing etching samples.The polishing sample exhibit no luminescence which means no porous layer in top surface.

5.2.3 Effect of content water in etching solution

In this part, water is added into the acid mixture to control the average etching rate which is very important to achieve thin PS solar cell applications. The disadvantage of stain etching is hard to control the etching rate. In this study, the etchant of HF: HNO_3 + H_2O, with H_2O varied from 10 ml to 70 ml were used. Following previous experiment, three ratios HF: HNO_3 = 9:1, 4:1, 7:3 were used to test the effect of adding water. Figures 5.13 and 5.14 show the total reflectance and the AER for ratio 9:1 + H_2O, respectively. For small amount of water, (20ml) AER was reduced from 4 μm/s to 1.9 μm/s but the still low reflectance (almost 0%) as sample without adding. For larger amount of adding water (plus 30, 40, 50 ml H_2O) samples, the total reflectance are about 20% at visible wavelength. The surface morphology of these sample are shown in Figure 5.15. Porous shape changes from open-structure to nano particles. The change in surface morphology can be explained by the average etching rate. At lower AER (with more adding water), etchant has less effect on the surface and the pore formation rate is lower than that of higher AER (with less adding water).

The similar tests were carried out for other acid ratio of (HF: HNO_3 + H_2O= 4:1 + 60, 7:3 + 70). The total reflectance for each ratio was shown in Figures 5.17, and 5.18. Figures 5.19 and 5.20 show the optimized results in AER for each etchant 4:1 + 50, 4:1 + 60, 7:3 + 50, and 7:3 + 70, respectively.

Consequently, it can be conclude that by adding wafer in the $HNO_3$and HF can reduce the etching rate of stain etching. These three ratios: 9:1 +20, 4:1 + 60, 7:3 + 70 were chosen for further experiment in this study. For industrial application – large size devices, adding wafer promises the huge potential to control the etching rate.

5.3 Formation of PS on different types of silicon wafer

5.3.1 Different resistivity silicon wafer

The effect of acid etching the Si with different resistivity also investigated. The etchant of HF: HNO_3 + H_2O = 7:3 + 70 was chosen, and the resistivity of wafer vary from 1 Ωcm to 12 Ωcm.

The results showed that the etched wafer with higher resistivity (8-12 Ωm) have lower AER but higher total reflectance than that of Si (1-10 Ωm) and Si (1-5 Ωm). The etching rates of three samples are 0.169 μm/s, 0.288 μm/s, 0.348 μm/s, respectively. Figure 5.20 shows the reflectance spectrum for etched wafer with different resistivity. The etchant mixture acts more active in low resistivity substrate. After etching with the same duration, the low resistivity (1-5 Ωcm) wafer presented the lowest total reflectance (1%) as compared with 3% and 7% for 1-10Ωcm, 8-12Ωcm Si (100) wafer, respectively. The surface morphographies of these three samples are shown in Figure 5.21. At high magnification, low resistivity substrates (1-5Ωcm, 1-10Ωcm) have similar structure with random and open pore site.

5.3.2 Si with different orientations

In this part, we use the same previous etchant (HF: HNO_3 + H_2O= 7:3 + 70) for experiment. After 180s etching, both Si (100), Si (111) etched sample have total reflectance below 2%. However, Si (111) etched sample has total reflectance lower than that of Si (100) as can be seen in Figure 5.22. This result can be explained by the ARE, etchant reacts faster on Si (111) than on Si (100): 0.233 μm/s > 0.169 μm/s. The surface roughness increases with the increases of AER. Thus, the etched Si (111) sample resulted in the lower total reflectance. Surface morphology of these two samples is quite similar which shown in Figure 5.23.

It can be concluded that both resistivity and orientation have effects on the AER and reflectance of the stain etching porous silicon. Starostina et al [61] noted that the doping concentration or resistivity of wafer strongly affect the etching rate. When the resistivity increases, the etching rate decreases. In this part, the same results with this conclusion. In addition, Si (111) is preferable for stain etching because it has the lower reflectance but higher

etching rate than Si (100). However, both the Si (111) and Si (100) wafer after stain etching process offered very low reflectance (below 2%)

5.4 Comparison between PS and Si_3N_4, SiO_2 ARCs

In the final experiment part of this thesis, we tried to form porous layer on large size Si wafer (7.5x7.5cm). After that, the reflectance of the etched wafers were compared with 200 nm Si_3N_4 and 200 nm SiO_2. The set up parameters for formation of PS are shown in Table 5.1

Figure 5.24 shows the total reflectance for each etched samples. PS3 sample gives the lowest reflectance (almost 0%). The PS1 and PS2 samples also provide the low reflectance (below 5%). Figure 5.26 explains why PS3 exhibits the lowest reflectance. The etched sample of PS3 has a very rough surface morphology. The root mean square (RMS) roughness observed from AFM image (Fig 5.27) shows PS3 sample has higher RMS value at 45.314 nm as compared to PS1, PS2 samples (29.464nm and 22.772 nm, respectively). Many researchers mentioned about the luminescence properties of PS [7, 62]. The PL spectra of three PS samples are shown in figure 5.27. PS1 and PS2 samples show the response in red peak, but PS3 sample does not present PL. The emission wavelength is located at around 650 nm. This correspond to a cluster size of 2-3nm in diameter as shown in Fig 5.25. This is consistent with previous conclusion as given by Kalem [62].

After the fabrication porous layer in large size wafer, we continue to compare these three PS samples with the conventional ARC material. These comparisons were shown in Figure 5.28, 5.29, 5.30, respectively.

Firstly, the total reflectance between PS samples and bare Si wafer with covered Si_3N_4 or SiO_2 are compared. After covered Si_3N_4 or SiO_2, these PS samples present interference reflectance. It can be seen that etched wafer show the remarkable low total reflectance compared with the wafer covered by Si_3N_4 or SiO_2. Secondly, the effect of Si_3N_4, or SiO_2 deposited onto porous surface is also investigated. It is shown that reflectance of three original PS samples was not affected by covered Si_3N_4, SiO_2 layers.

Finally, EDS was carried on to see the composition in surface of etched samples. As many researchers mentioned, Si very easy oxidized in air ambient to form SiO_2. EDS analysis shows that on top of porous layer presented oxygen and silicon elements (Fig 5.32). The top surface includes 7.48% oxygen and 92.52% silicon in weight which are shown in table 5.2

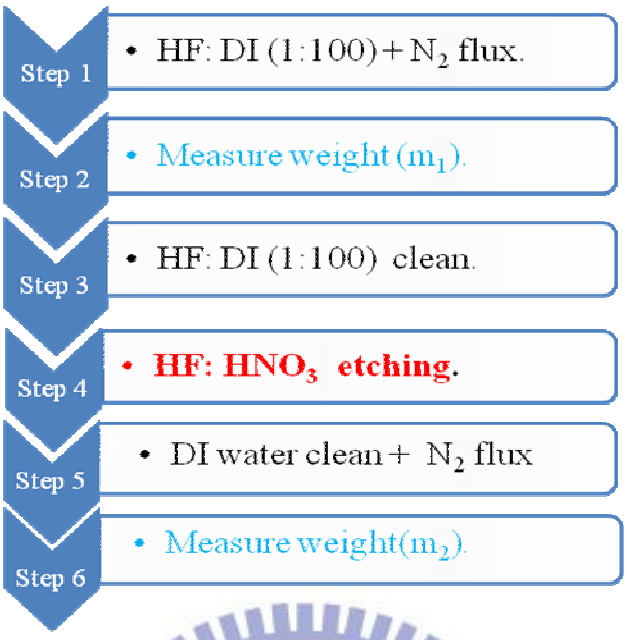


Fig. 5.1 Overall process for porous silicon formation

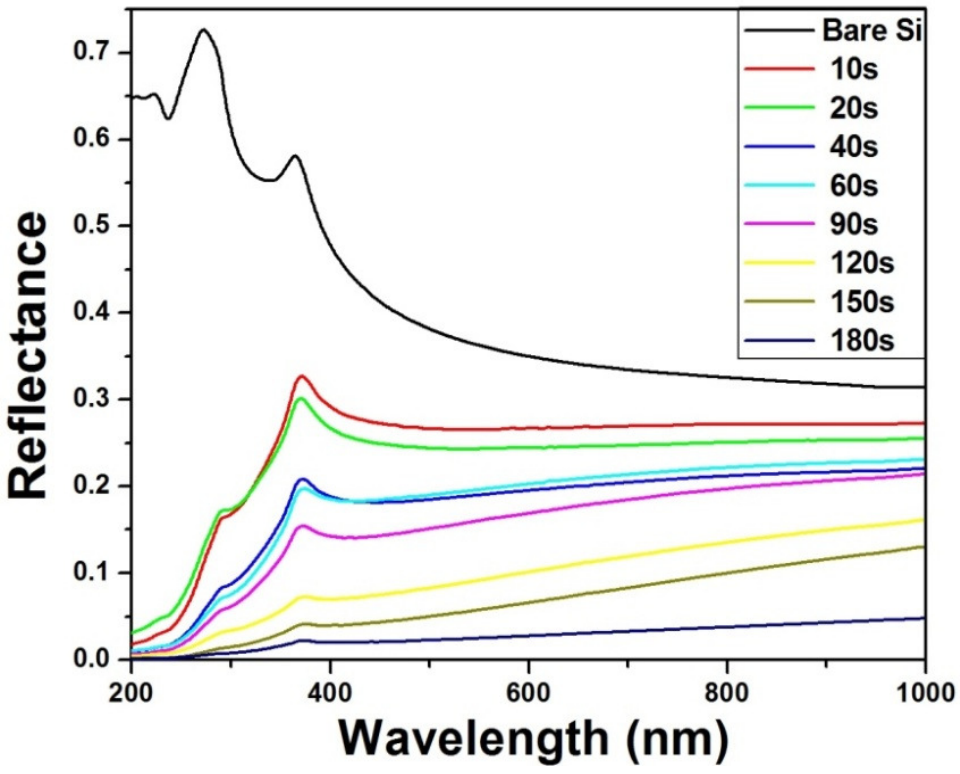


Fig. 5.2 Total reflectance for porous silicon layers etched in a solution HF: HNO_3 + H_2O (7:3 + 70) with varying etching time etching.

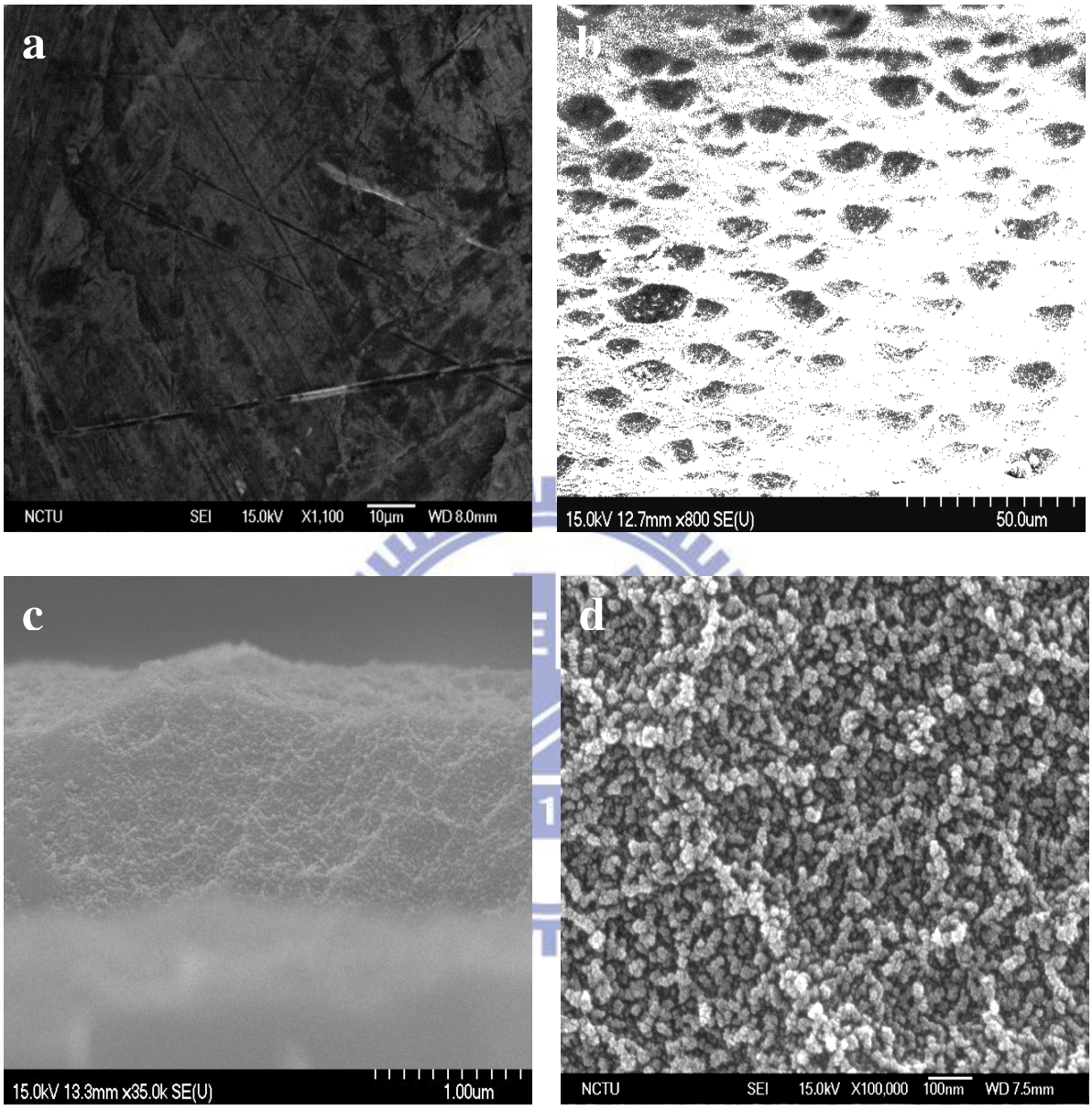


Fig. 5.3 SEM image : a) Before etching. b) After etching. c) Cross-section d) high magnification top-view of porous layer

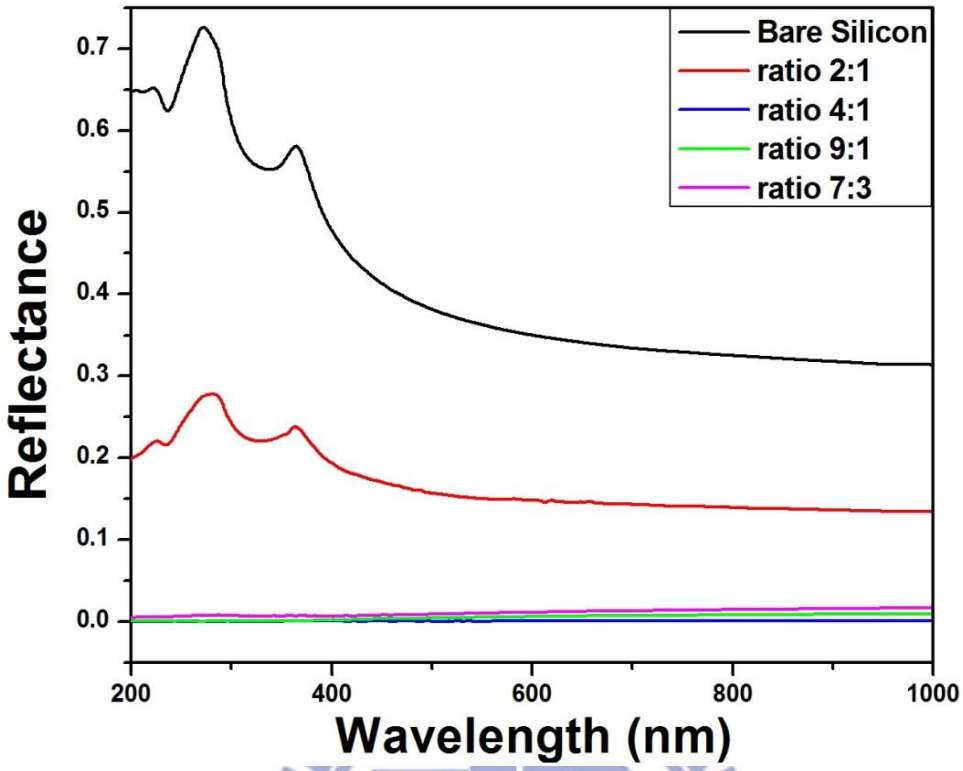


Fig 5.4 Reflectance spectrum for HF dominant group

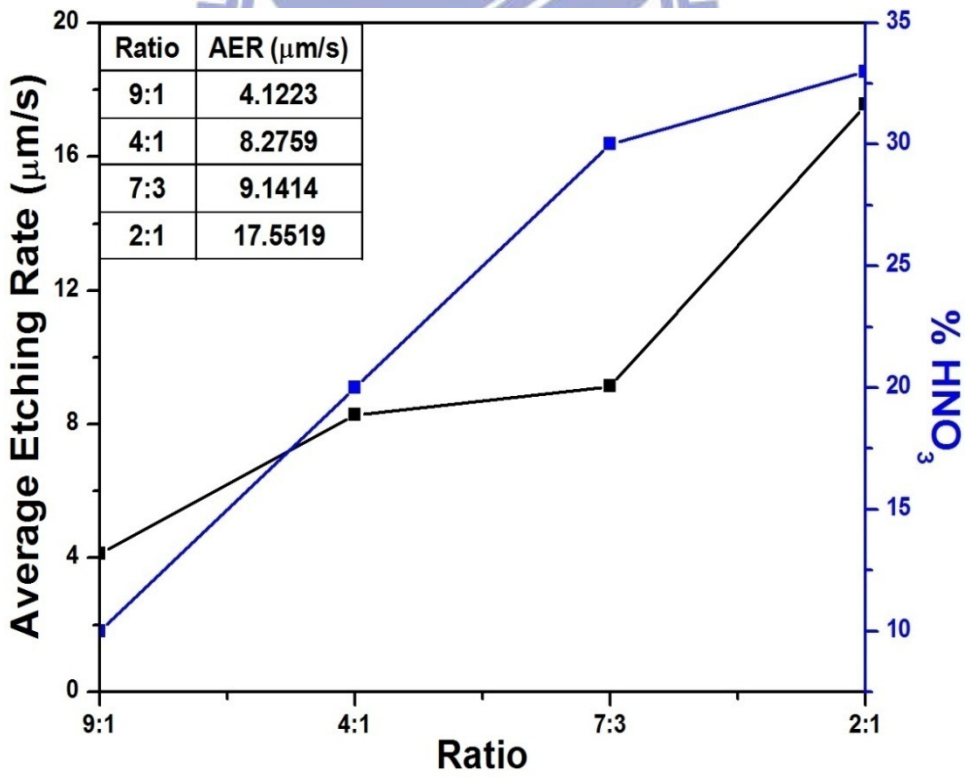


Fig 5.5 The average etching rate as the function of HNO_3 proportion

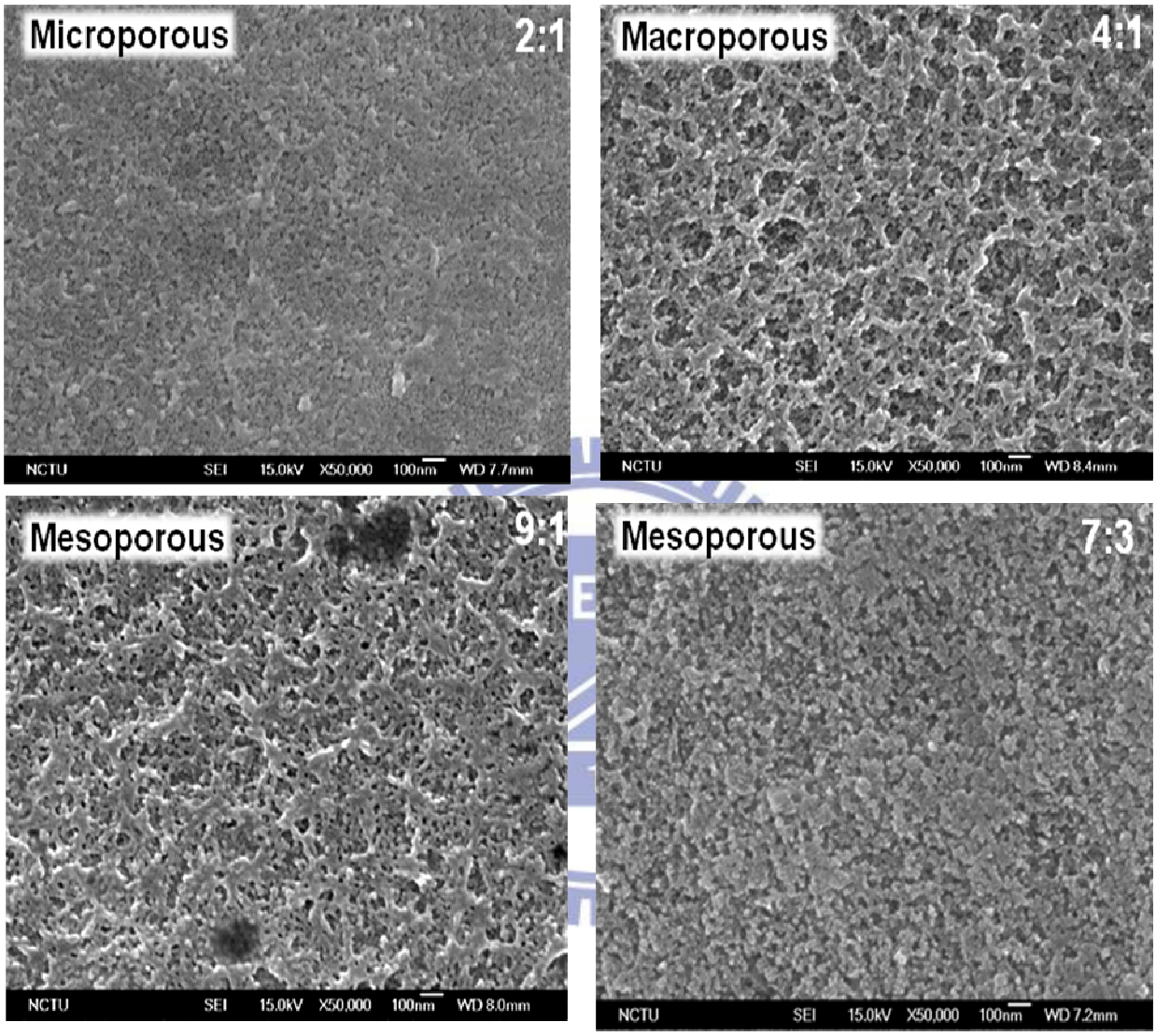


Fig 5.6 Top-view SEM image for HF dominant group

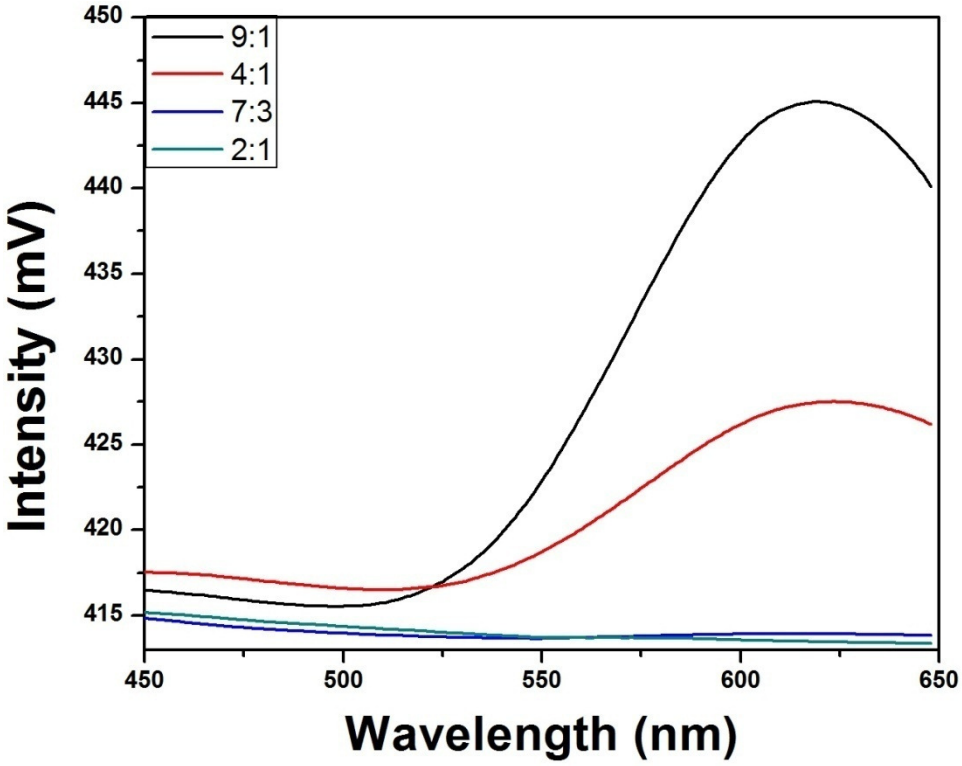


Fig 5.7 PL spectrum for HF dominant group

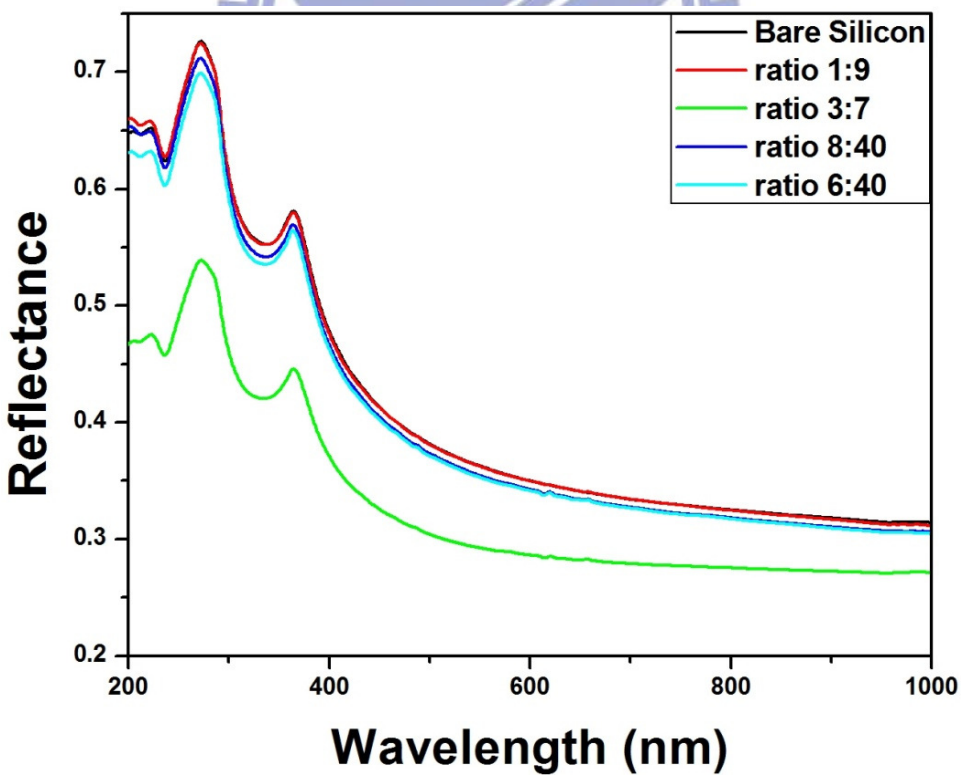


Fig 5.8 Reflectance spectrum for HNO_3 dominant group

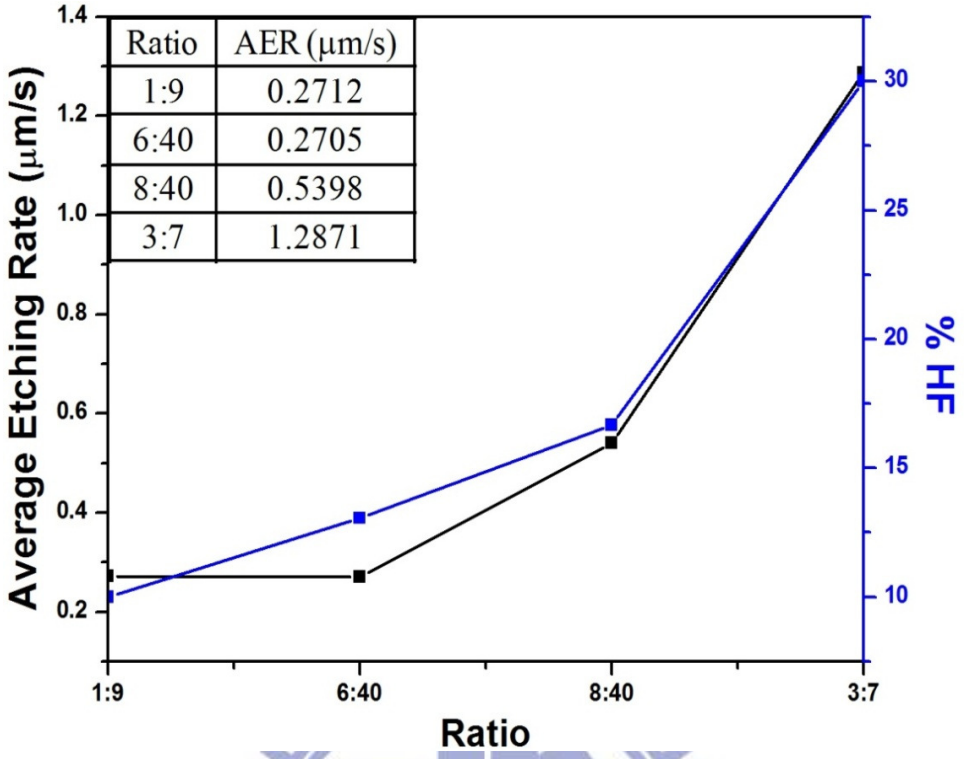


Fig 5.9 The average etching rate as the function of HF proportion

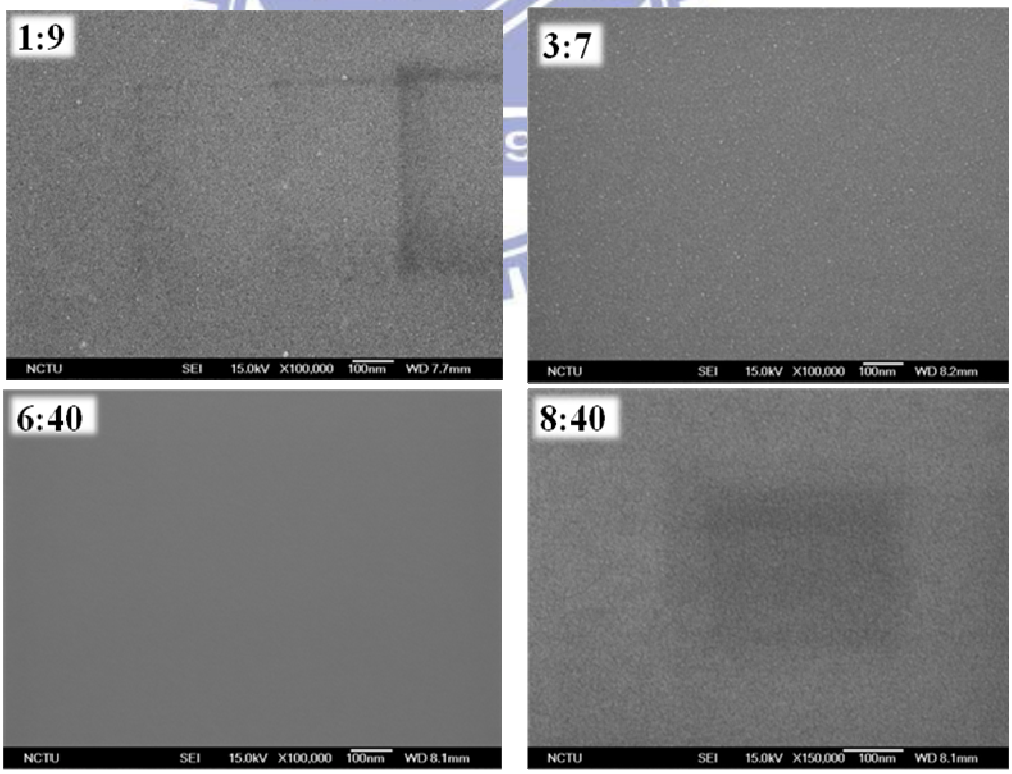


Fig 5.10 Top-view SEM image for HNO_3 dominant group

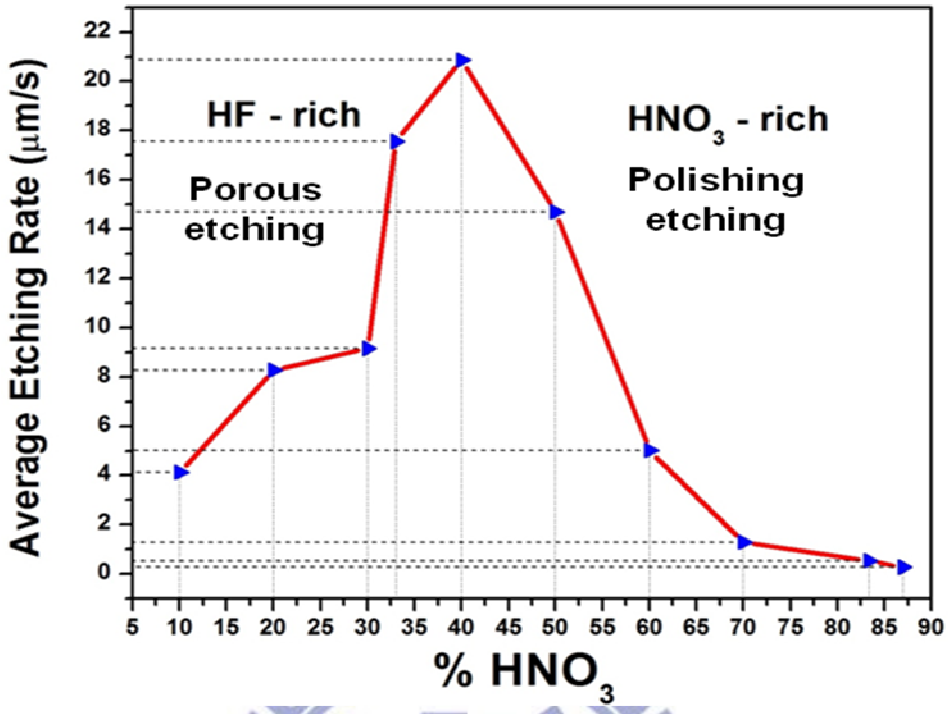


Fig 5.11 Transition from polishing etching to porous formation

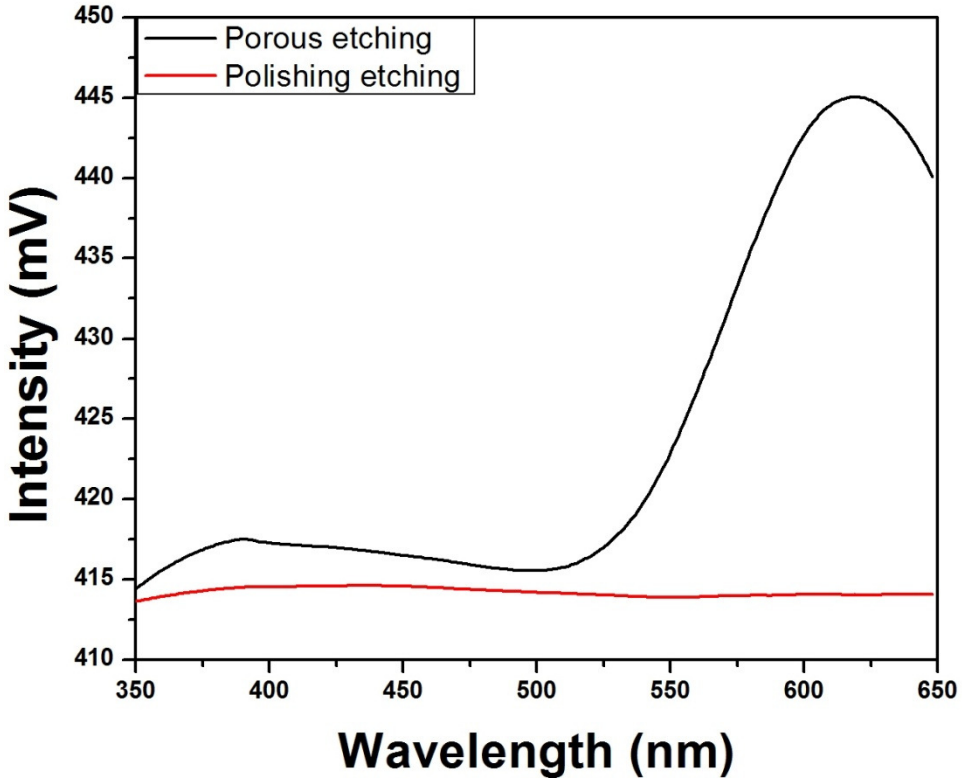


Fig 5.12 PL spectrum for porous etching and polishing etching

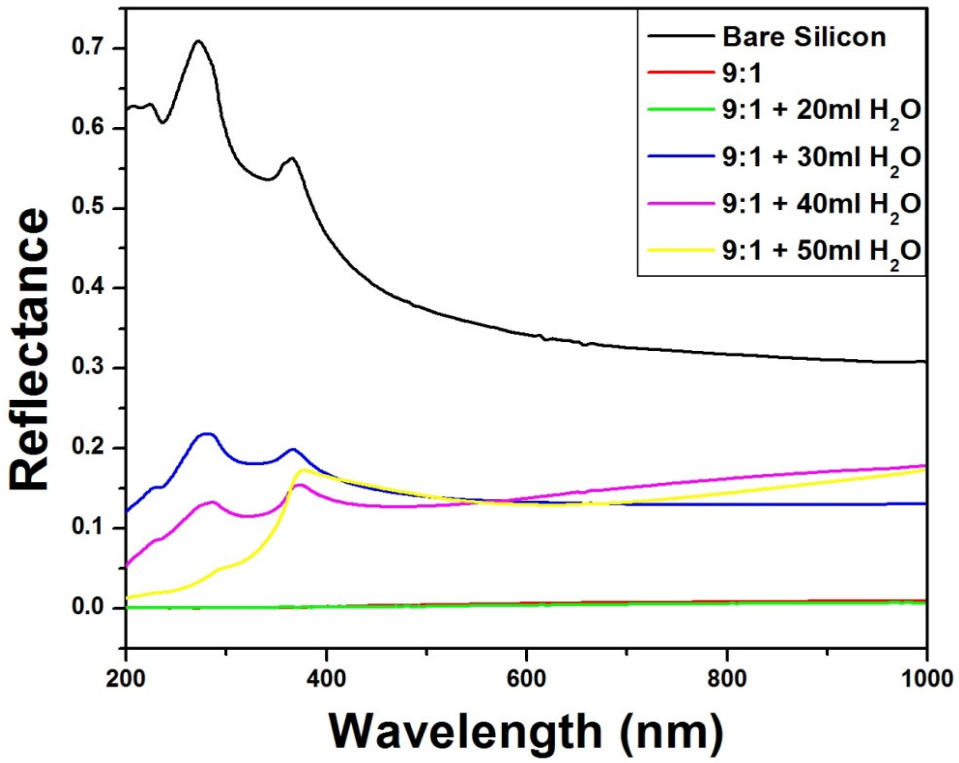
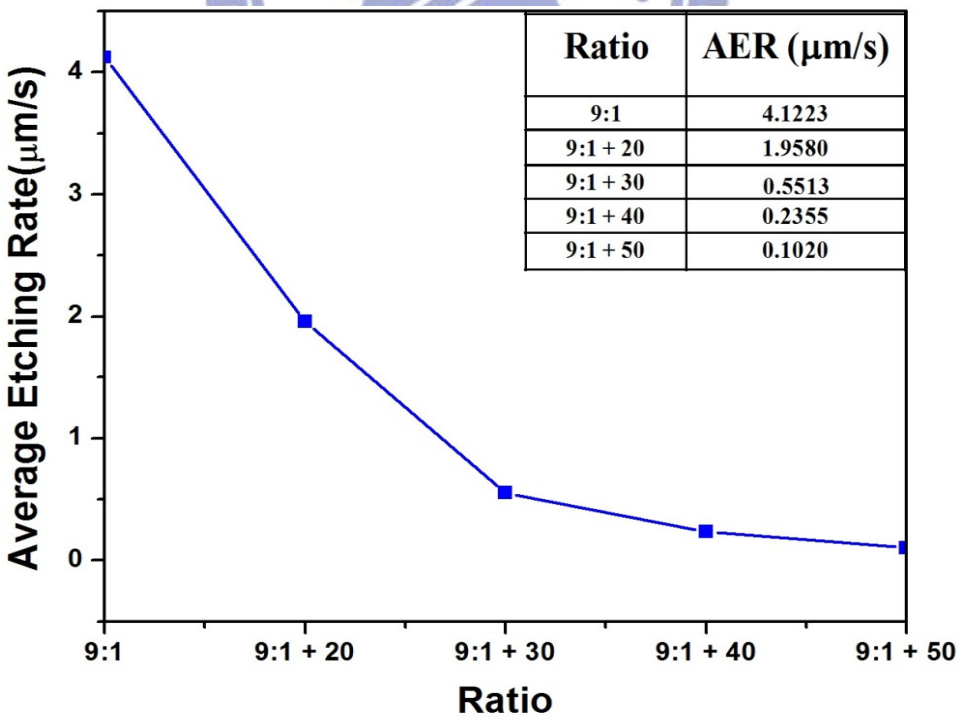


Fig 5.13 Reflectance spectrum for etchant HF: HNO_3 + H_2O = 9:1 + H_2O



Ratio	AER (μm/s)
9:1	4.1223
9:1 + 20	1.9580
9:1 + 30	0.5513
9:1 + 40	0.2355
9:1 + 50	0.1020

Fig 5.14 Average etching rate for etchant HF: HNO_3 + H_2O = 9:1 + H_2O

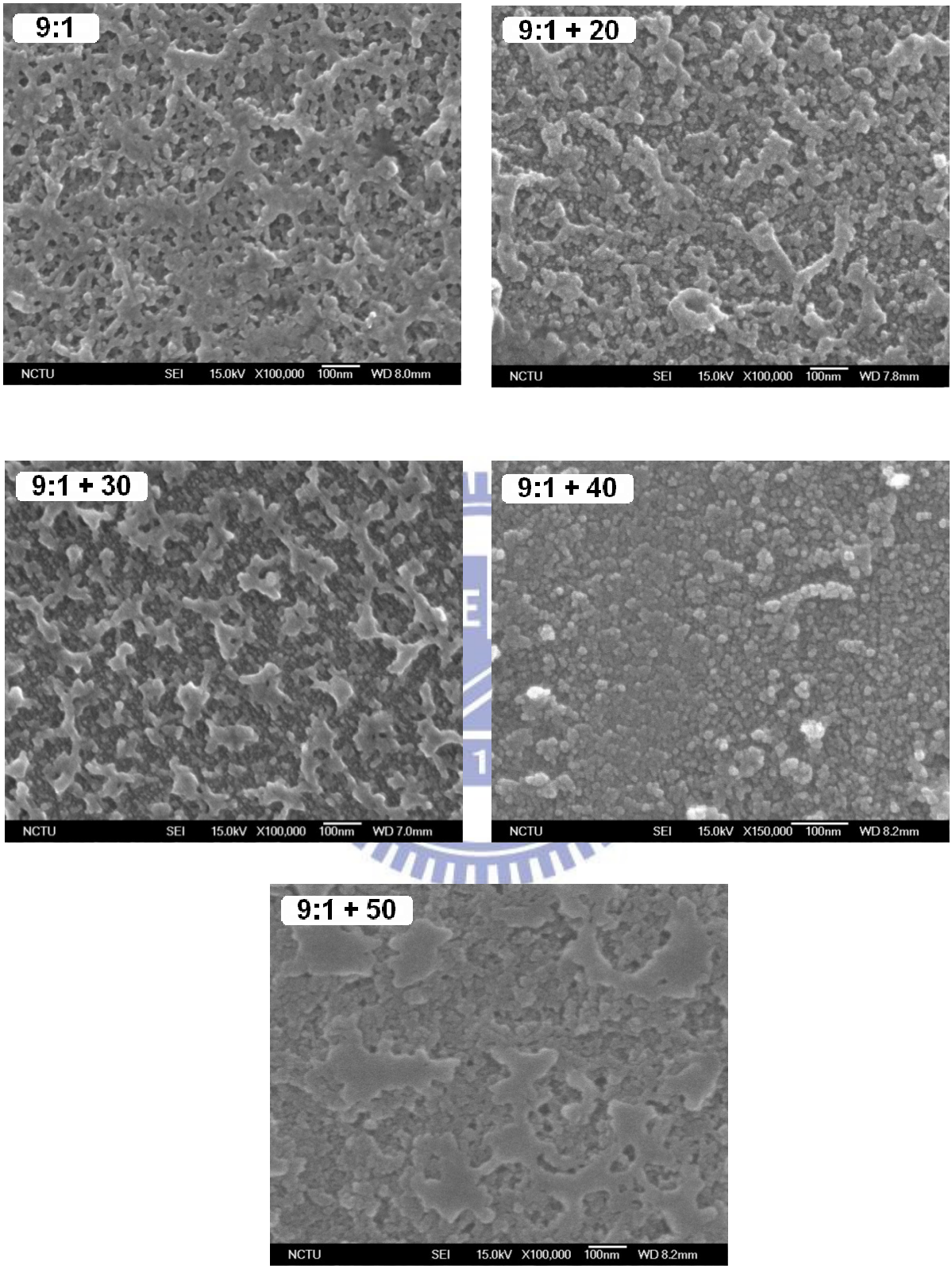


Fig 5.15 Top-View SEM image for etchant HF:HNO_3 +H_2O= 9:1 + H_2O

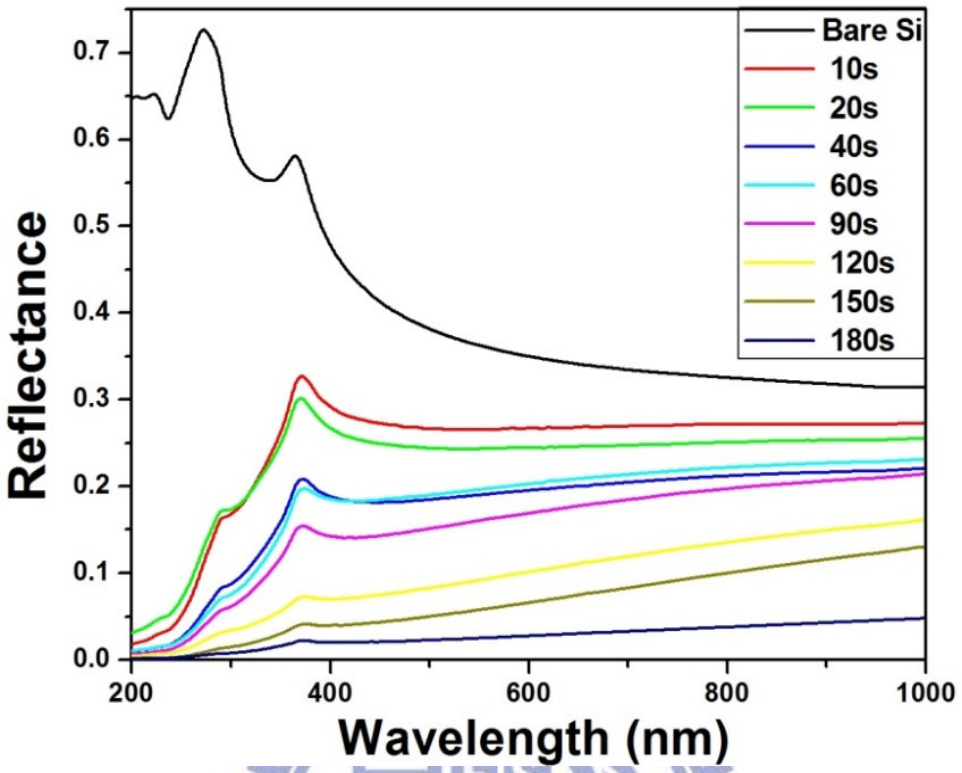


Fig 5.16 Reflectance spectrum for etchant HF: HNO_3 + H_2O = 7:3 + 70

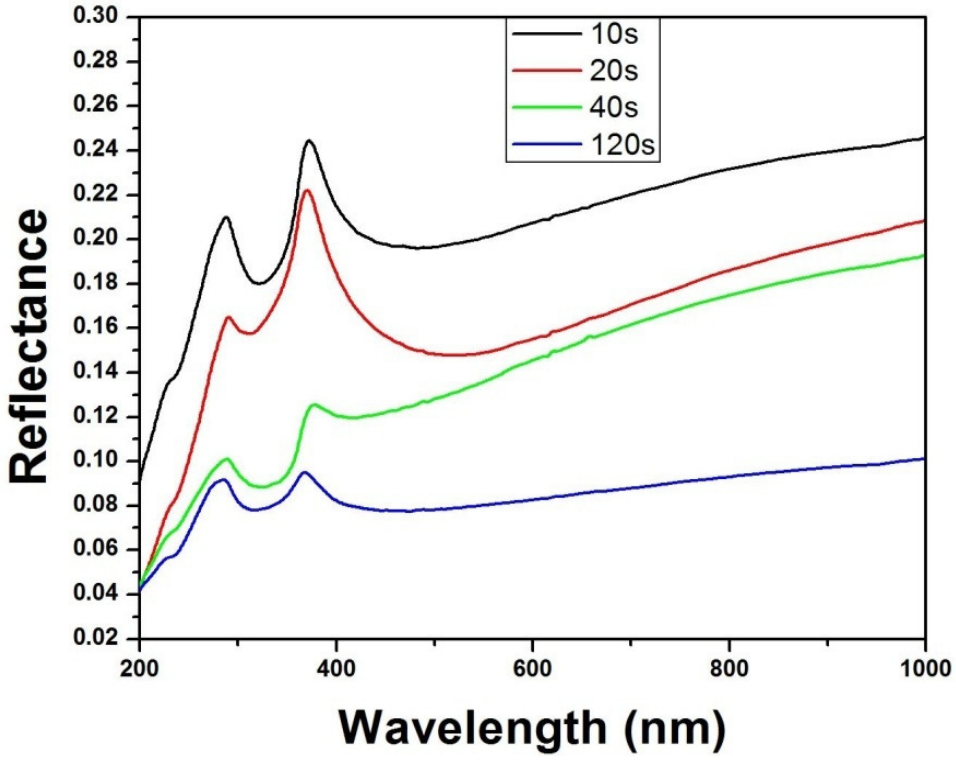


Fig 5.17 Reflectance spectrum for etchant HF: HNO_3 + H_2O = 4:1 + 60

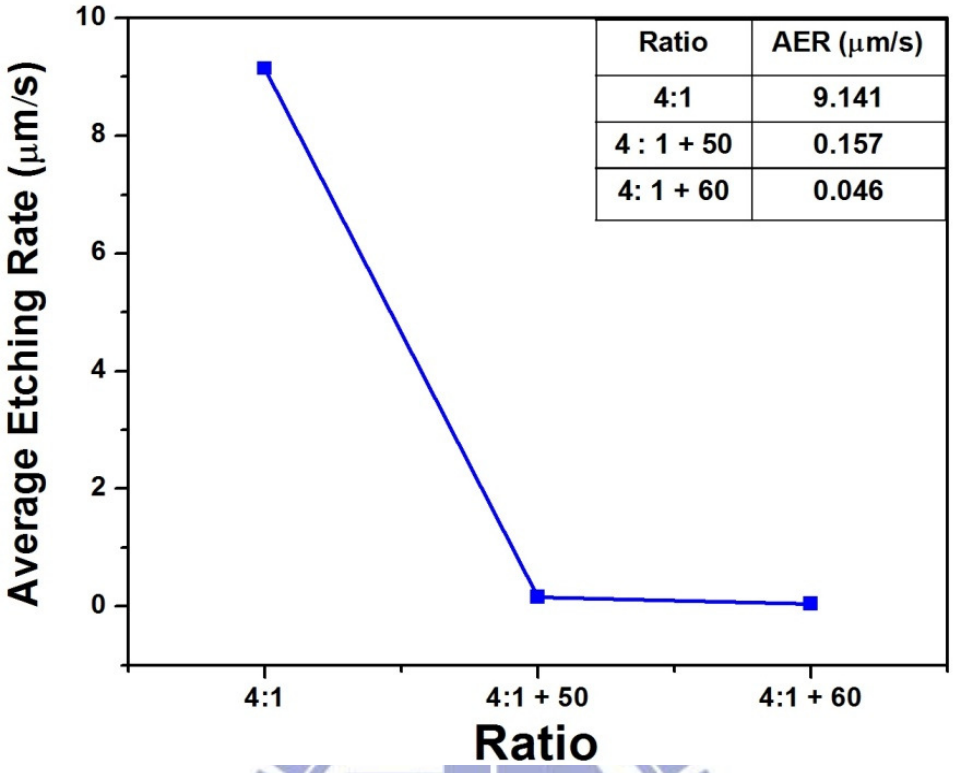


Fig 5.18 Average etching rate for etchant HF: HNO_3 + H_2O = 4:1 + H_2O

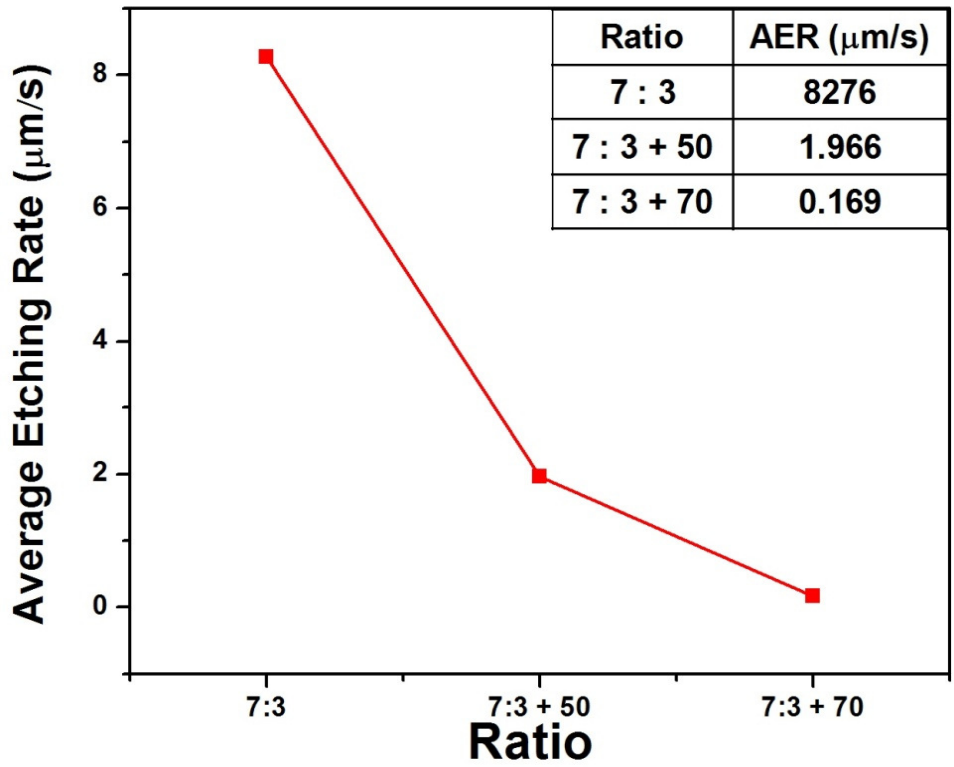


Fig 5.19 Average etching rate for etchant HF: HNO_3 + H_2O = 7:3 + H_2O

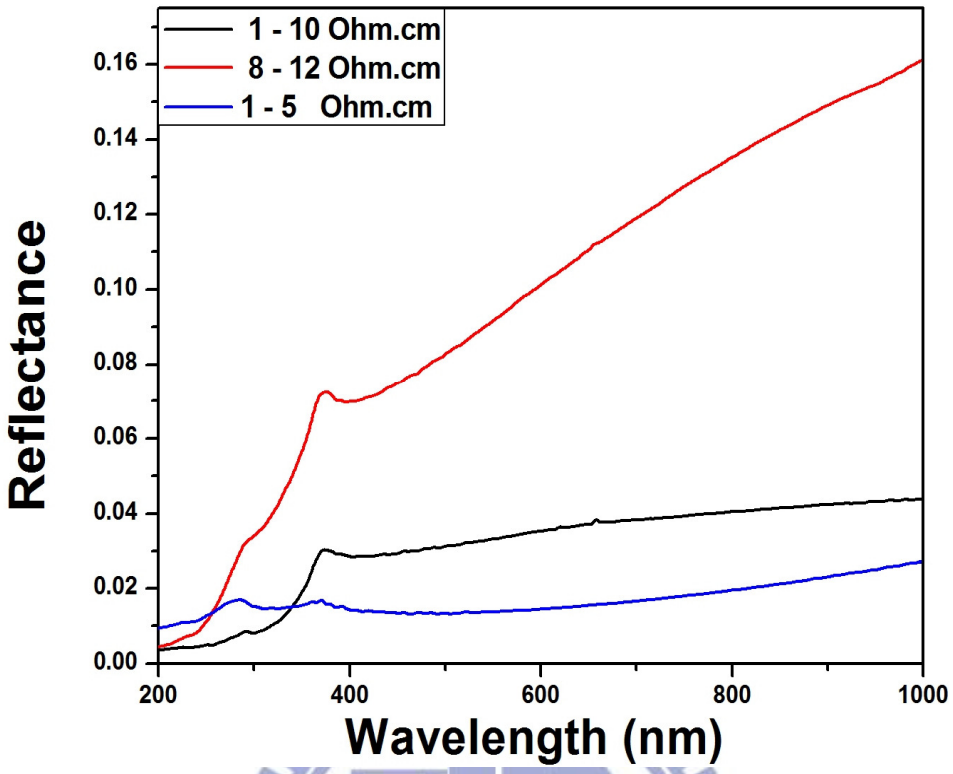


Fig 5.20 Reflectance spectrum for different resistivity etched wafer

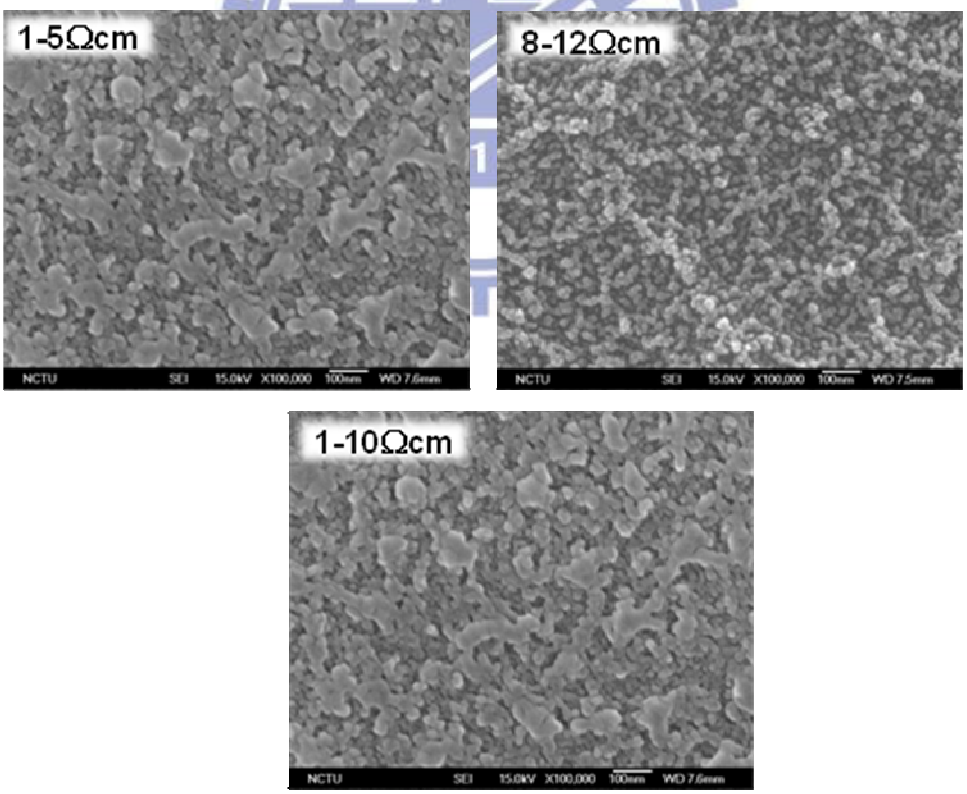


Fig 5.21 Top-view SEM image of different resistivity etched wafer

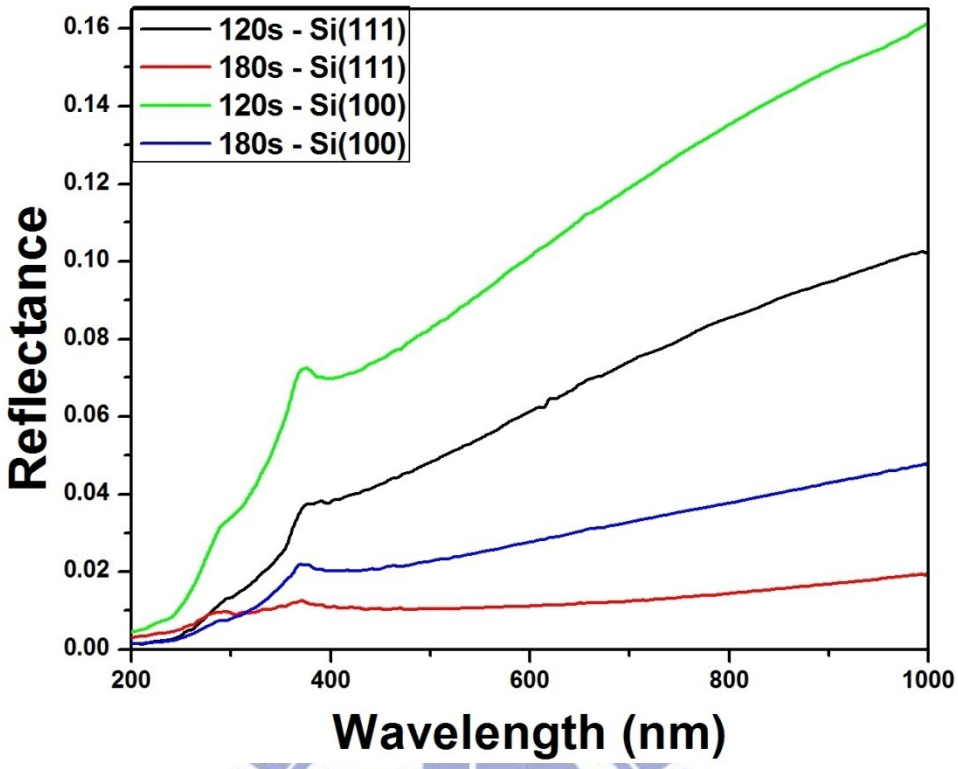


Fig 5.22 Reflectance spectrum for different orientation etched wafer

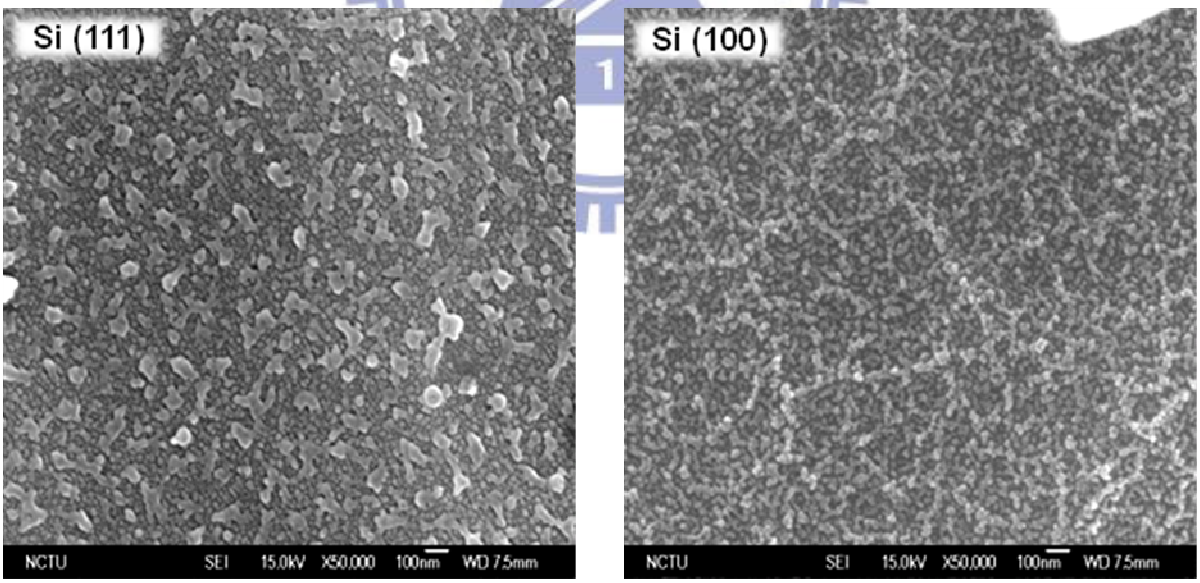


Fig 5.23 Top-view SEM image of different orientation etched wafer

Table 5.1 Parameter set up for formation of PS in big size wafer

Sample	PS1	PS2	PS3
Etchant **HF: HNO_3 + H_2O**	4:1 + 60	9:1 + 20	7:3 + 70
AER (μm/s)	0.414	2.147	2.467
RMS (nm)	29,464	22,772	45,314

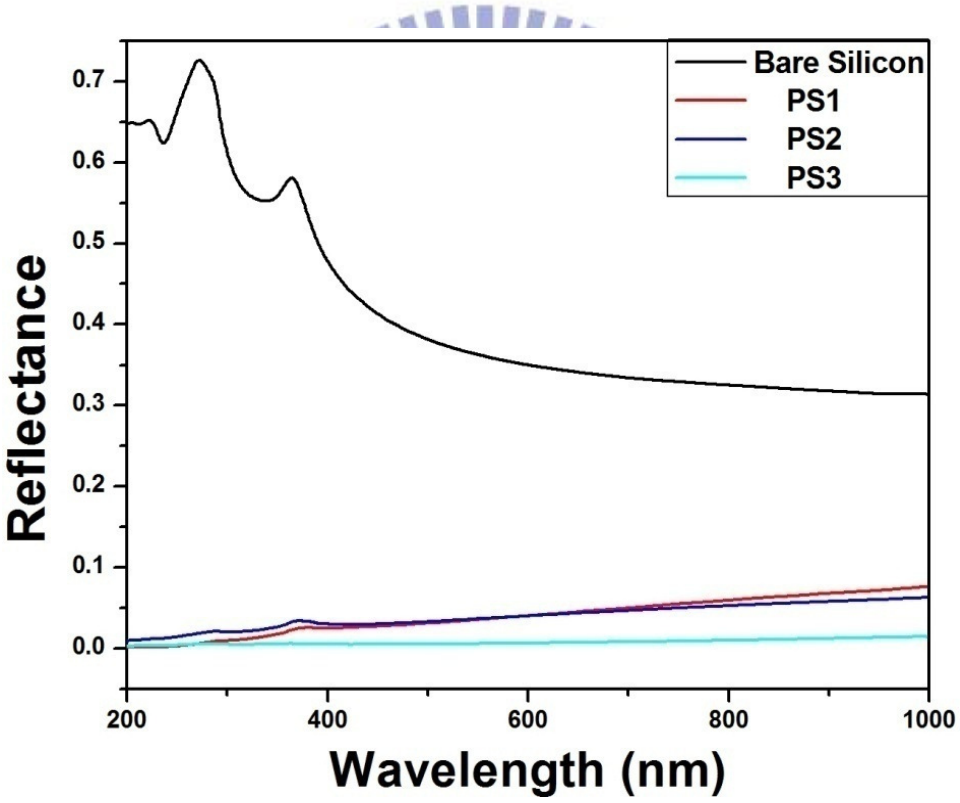


Fig 5.24 Reflectance spectrum for PS1, PS2, PS3 sample.

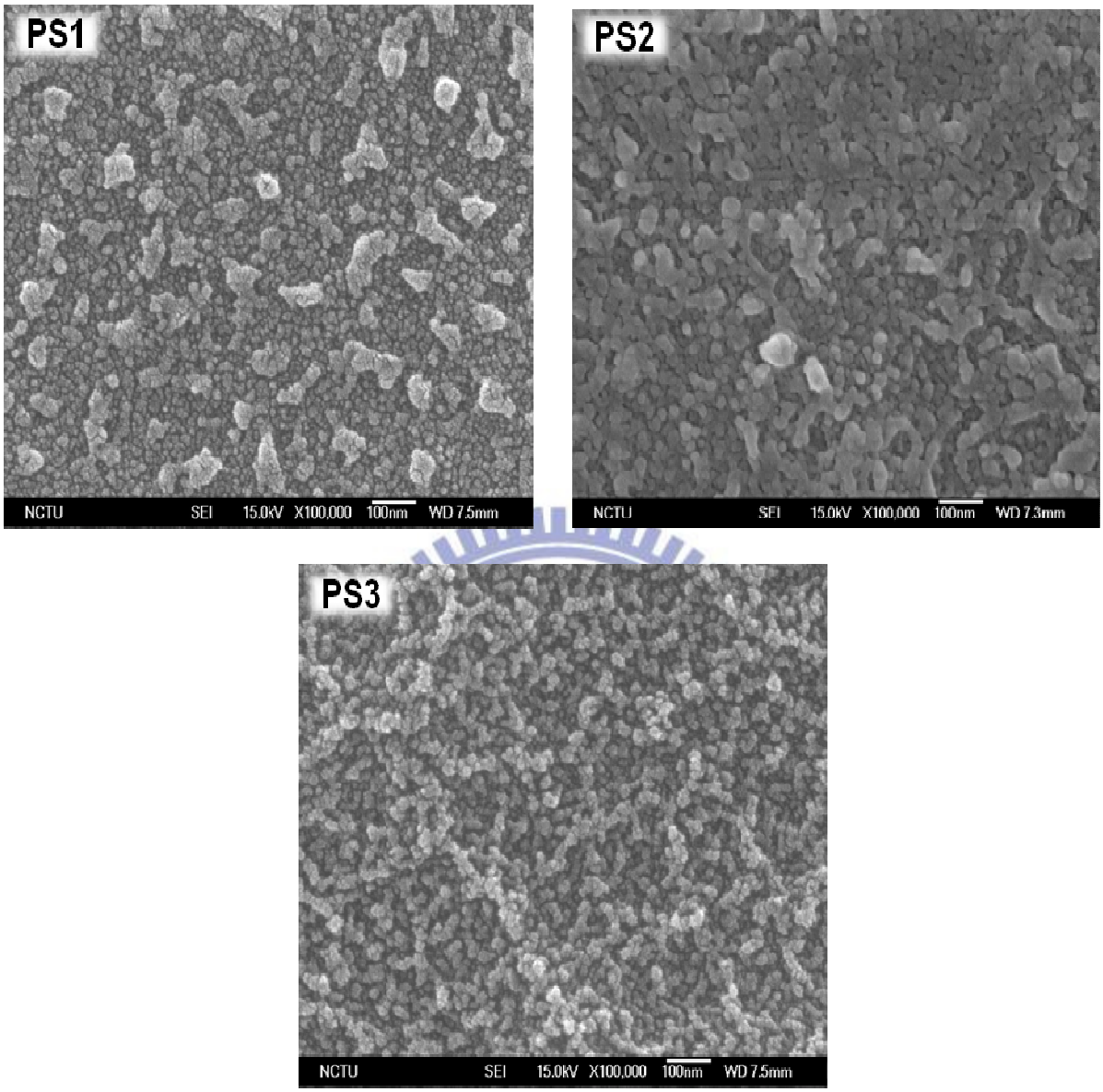


Fig 5.25 Top-view SEM image of PS1, PS2, PS3 sample

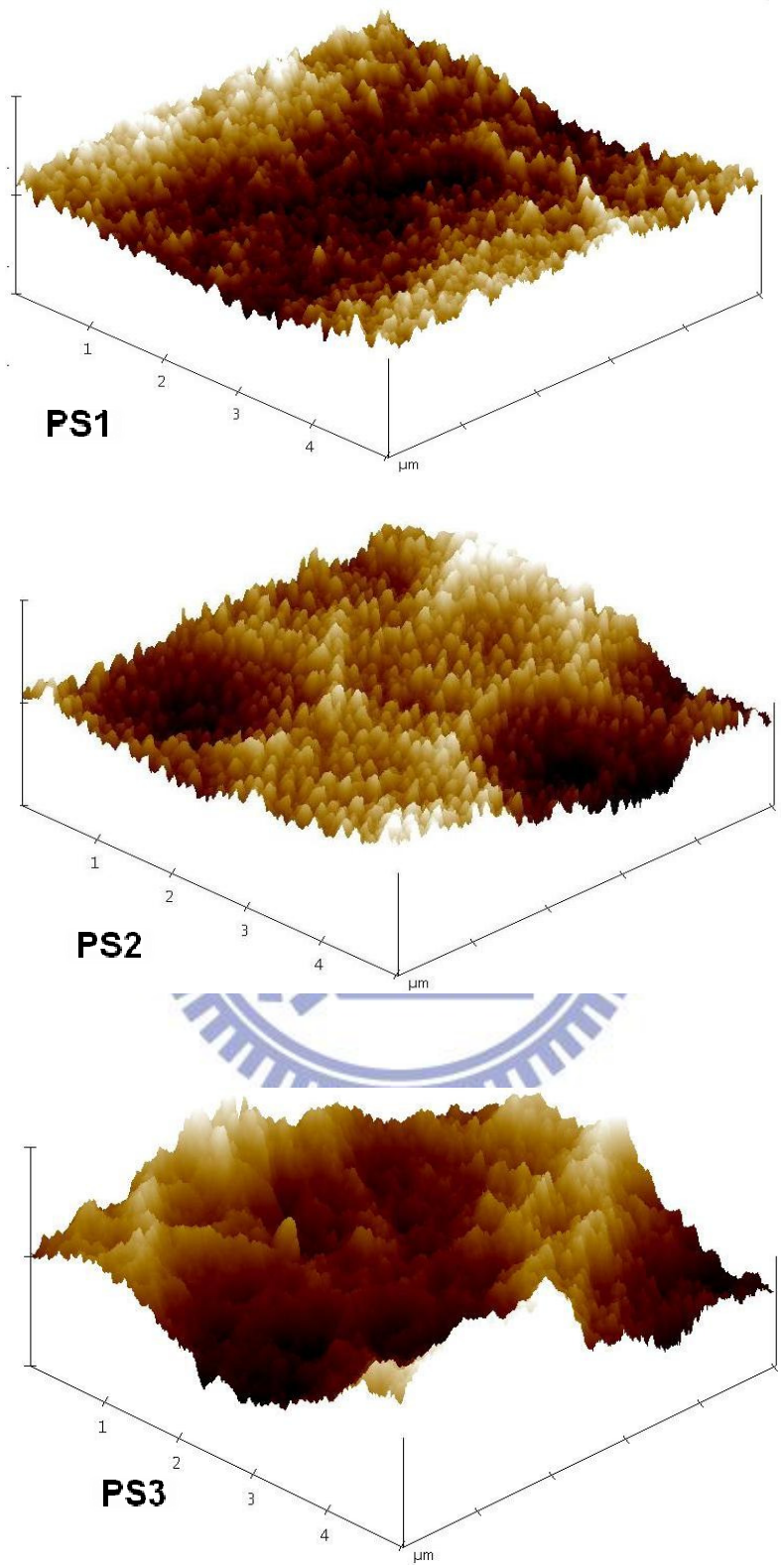


Fig 5.26 AFM image for PS1, PS2, PS3 sample

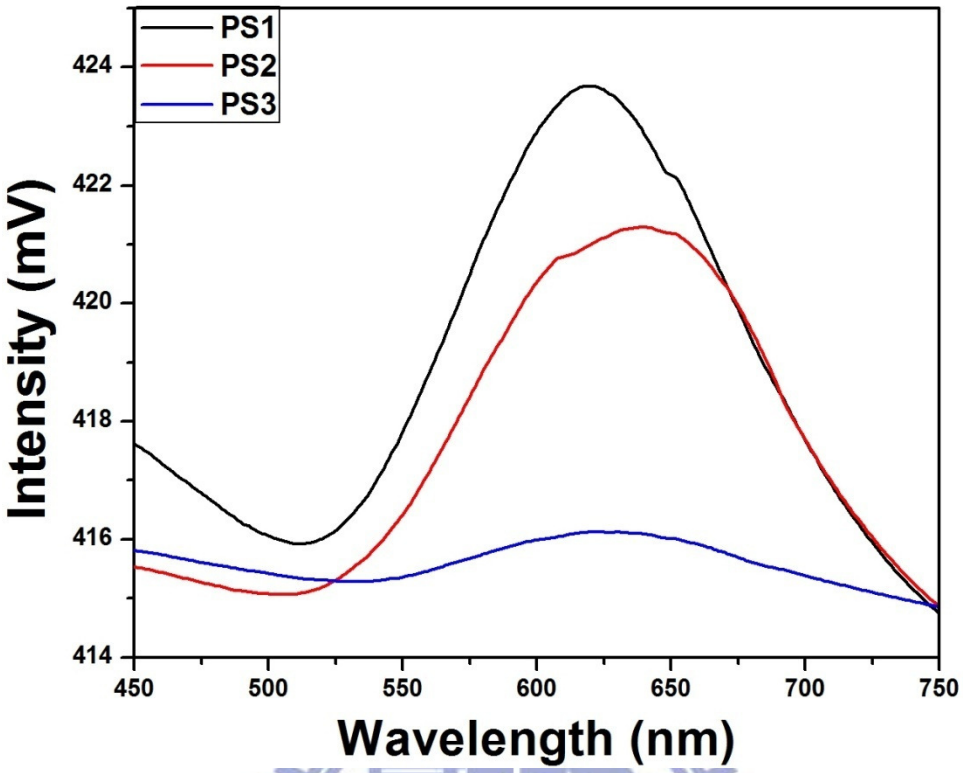


Fig 5.27 PL spectrum for PS1, PS2, PS3 sample

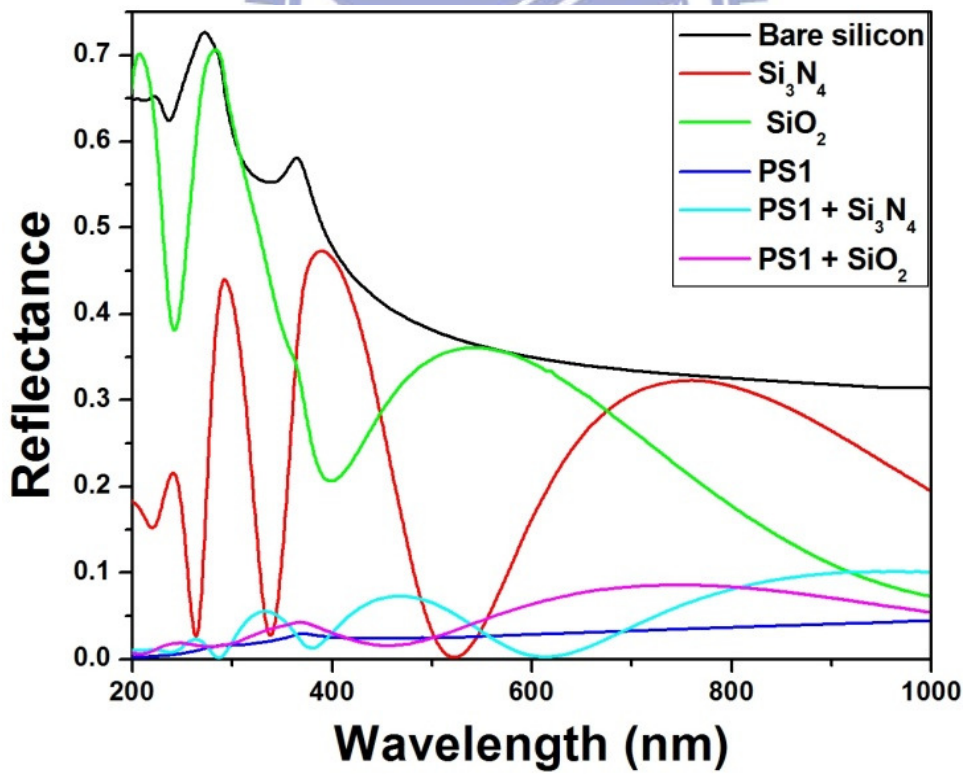


Fig 5.28 Reflectance spectrum for PS1, Si_3N_4, SiO_2

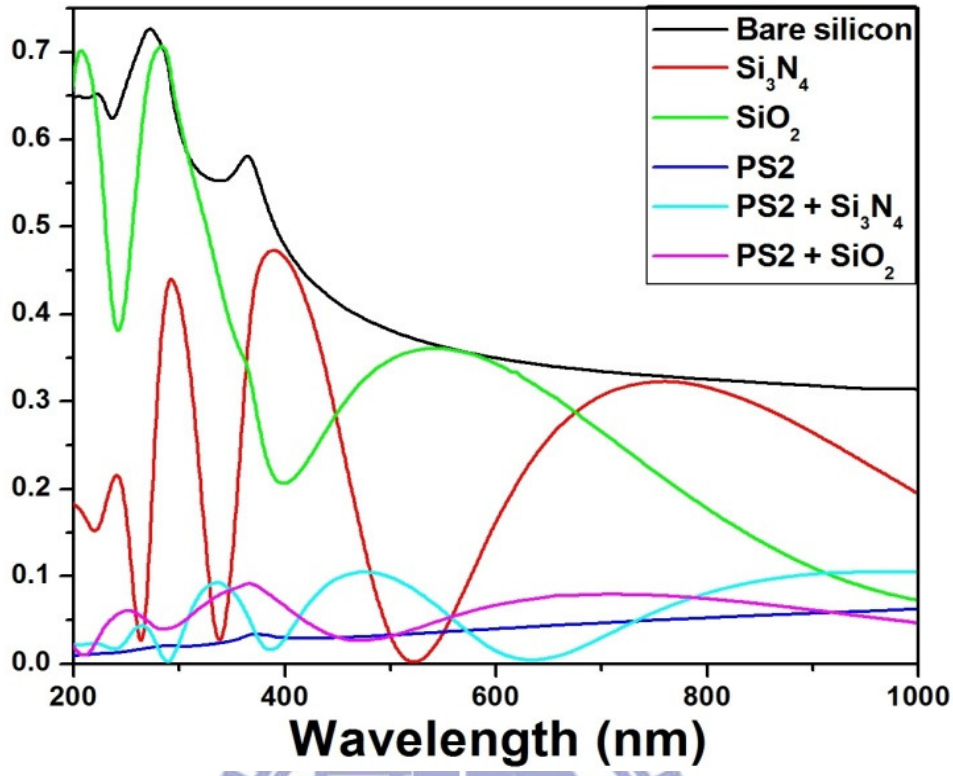


Fig 5.29 Reflectance spectrum for PS2, Si_3N_4, SiO_2

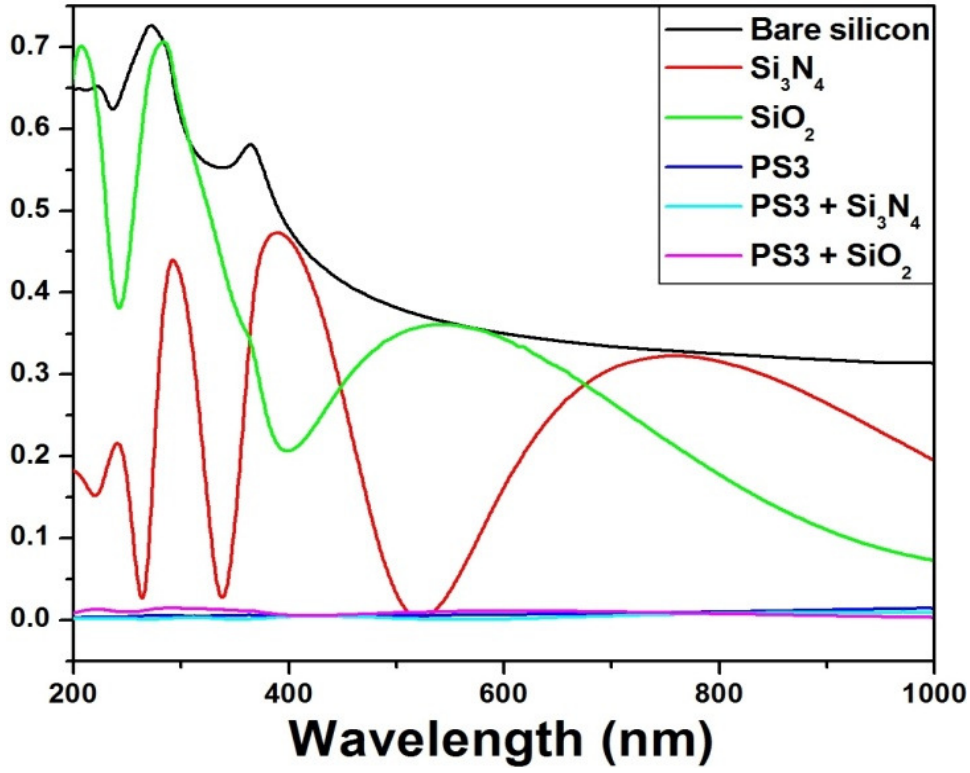


Fig 5.30 Reflectance spectrum for PS3, Si_3N_4, SiO_2

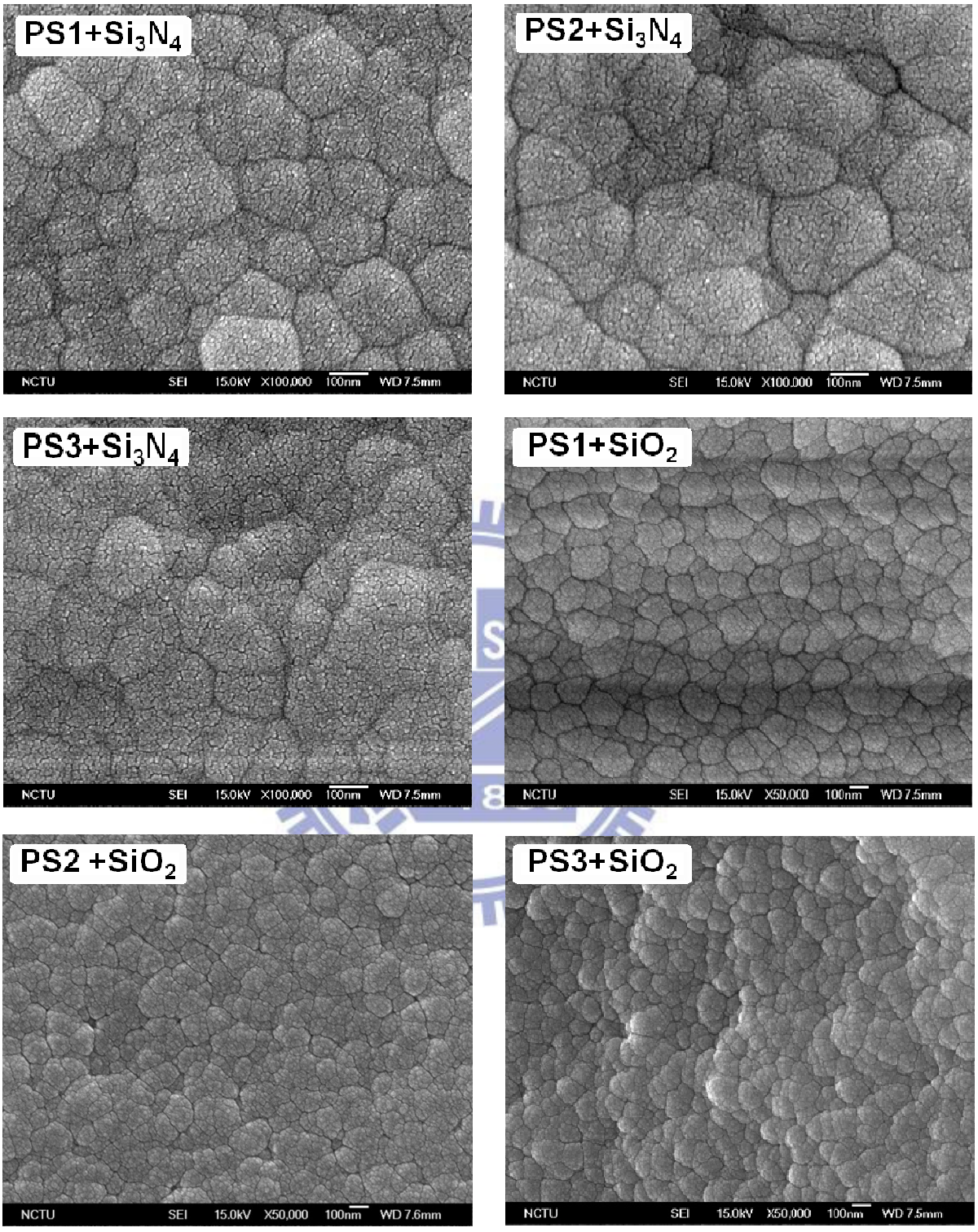


Fig 5.31 Top-view SEM image of PS sample covered Si_3N_4, SiO_2

Table 5.2 EDS analysis for porous sample

Element	Weight%	Atomic%
O K	7.48	12.43
Si K	92.52	87.57
Totals	100.00	

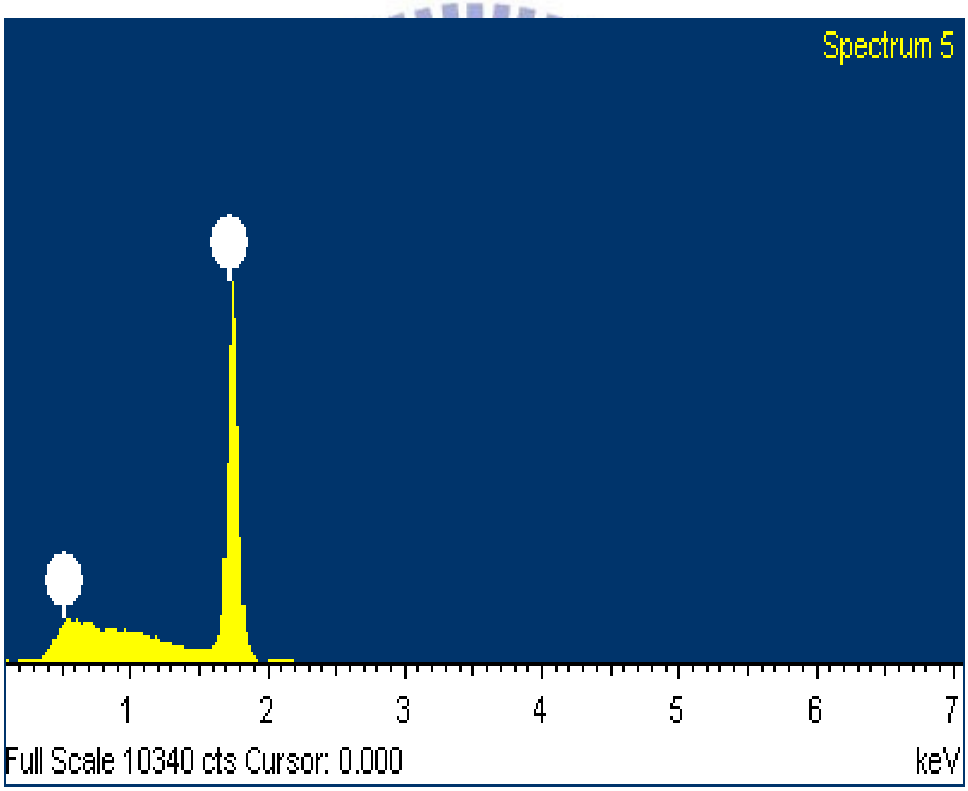


Fig 5.32 EDS analysis for porous silicon

Chapter 6

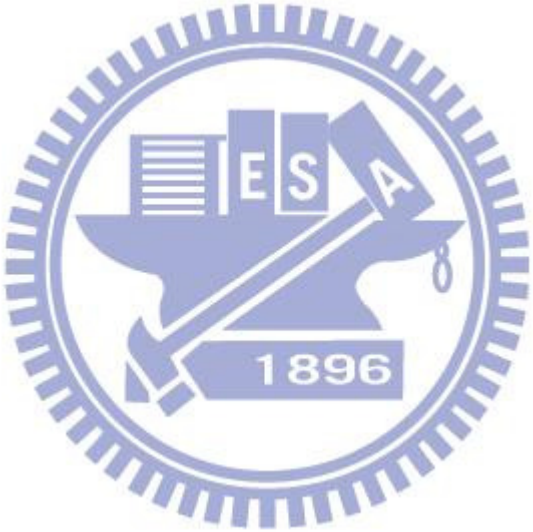
Conclusions and future works

6.1 Conclusions

We have investigated the chemical formation of PS in HF: HNO_3, HF: HNO_3 + H_2O etchants and determined the ranges in which the ratio of HNO_3 should be varied in order to change from etch polishing to porous formation. The etching transition was applied to p-type Si (100) with ρ=8-10Ωcm. When the proportion of HNO_3 is lower than 40% in etching solution, porous etching occurs. We successfully fabricated porous layer on top of Si substrate with lower total reflectance (0% in visible light) as compared with bare silicon wafer or conventional AR within Si_3N_4, or SiO_2. We observed that after covering 200nm Si_3N_4, or SiO_2 on top of etched wafer, these AR coating do not have effect on reflectance of porous silicon layer. For controlling the etching rate which is the disadvantage of PS stain etching, adding water is the solution. Adding water into the acid etchant not only reduce the etching rate but also skips the total reflectance of etched wafer at acceptable level for ARC applications. We successfully optimized the stain etching process from small size Si wafer (2x2cm) to large size Si (7.5x7.5cm). We obtained that three etchant solutions HF: HNO_3 + H_2O = 9:1 + 20, 4:1 + 60, 7:3 + 70 are suitable for industrial purpose. In addition, in this study, we also observed the PL properties of PS layer. Comparing with bare Si which does not have PL response, porous layer presents PL signal at red peak (630nm). Consequently, PS layer not only offers low reflectance in visible light but also presents the PL properties which open the huge potential for ARCs application and light emitting based silicon devices.

6.2 Future works

The effect of resistivity on stain etching process not clearly understood, our future works will be figured out this effect. Thus, we have to consider about life time of carrier in PS layer which is very important for AR applications. After clarifying these problems, we will carry on fabricate complete PS anti reflection solar cell module.



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