國立交通大學

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碩士論文

動態臨限電壓場效電晶體之零溫度係數點模型研究

Zero Temperature Coefficient Point Model of Dynamic Threshold MOSFETs

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摘要

在本論文中，我們提供三種金氧半場效電晶體的操作模式，分別是 DT-A 模式 ($V_{bs} = 0.7V_{gs}$)、DT-B 模式 ($V_{bs} = V_{gs}$) 以及傳統操作模式。每種操作模式皆搭配三種不同閘級材料，即 polysilicon、TiN 以及 TaC，用以比較不同操作模式以及不同閘極材料對元件的性能的影響。其中，DT-B 模式搭配金屬閘極可以得到非常優良的電性，例如：它能夠提供最佳的臨限電壓變化特性(threshold voltage roll-off)、減少汲極產生的位勢降低量(DIBL) 以及接近理想值的次臨限擺動(subthreshold swing)。然而，在同樣的閘極條件下，DT-A 模式則能擁有最佳化的驅動電流(drive current)。此外，在廣泛的操作溫度範圍下[223K，398K]，我們進一步地從理論及實驗層面去分探討臨限電壓、汲極產生的位勢降低量以及次臨限擺盪對溫度的相依性。

為了能夠在低溫操作下得到較高的電流增益，我們推演出動態臨限電壓金氧半場效電晶體的零溫度係數點(zero temperature coefficient point) 模型，並且將零溫度係數點在線性區與飽和區的預測理論值與實驗值做比較。在這個縝密的模型分析過程中，我們不僅考慮基板偏壓效應(body bias effect δ)，還修正了飽和區理想電流公式中的次方項。因此，不論是在線性區或者飽和區，我們都得到非常小的誤差值(< 5%)。

Zero Temperature Coefficient Point Model of Dynamic Threshold MOSFETs

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Abstract

In this work, we provide three operation modes of MOSFET, respectively DT-A mode ($V_{bs} = 0.7V_{gs}$), DT-B mode ($V_{bs} = V_{gs}$), and normal mode, and three gate materials, namely polysilicon, TiN and TaC, to compare their performance. Although DT-B mode accompanied with metal gate shows the excellent characteristics, such as the lowest threshold voltage roll-off, better DIBL and the near ideal value of subthreshold swing, the DT-A mode counterpart exhibits the optimized drive current. Furthermore, the temperature dependence of threshold voltage, DIBL and subthreshold characteristics are investigated both theoretically and experimentally over the wide operation temperature ranges from 223K to 398K.

In addition, in order to obtain high current gain at low operation temperature, we develop a zero temperature coefficient (ZTC) point model for DTMOS to compare with experimental results in the linear and saturation regions. The analysis takes in to the consideration of body bias effect δ and the modification of ideal square-law condition in the saturation region to obtain very small error ($< 5\%$) no matter in the linear or nonlinear region.

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Chapter 1

Introduction

1.1 General Background

1.1.1 High-K Dielectric/ Metal Gate

As CMOS device are scaled down, the conventional polysilicon/oxide gate stack suffers from high gate leakage current, intolerable resistive-capacitive delay, poly depletion, and Boron penetration especially for PMOS [1].

The use of high-K dielectric collocating with metal gate is becoming increasingly necessary to reduce gate leakage, poly depletion effect and gate resistivity at very thin oxide. As a result, metal gate/ high-k stacks are being heavily pursued recently, and the identification of suitable N/P metals is the most challenging task due to that the metal gates to replace n+ and p+ poly for bulk CMOS devices must have correct work functions; they have to fall within 0.2 eV of silicon conduction and valence band edges, even after a high-temperature anneal during source/drain activation [2-4].

1.1.2 Dynamic Threshold Voltage MOS (DTMOS)

During the past few years, demand for high-performance and low-power digital systems has grown rapidly. The low-power-consumption approach is intended for battery-operated applications, such as laptop and notebook computers as well as personal communication systems. While the high-performance approach is appropriate for applications such as microprocessors, power consumption is now becoming a critical parameter.

Power supply scaling is the most common approach for reducing power. This is due

to the fact that in CMOS digital circuits, delivered power is proportional to the square of power supply voltage:

$$P = C_L V_{dd}^2 f_d \qquad \text{(eq. 1-1)}$$

where P is the power consumed by one gate, C_L is the total switching capacitance of the gate, V_{dd} is the power supply voltage, and f_d is averaged cooperating frequency of that gate.

Since reducing power supply voltage to below three times the threshold voltage will degrade circuit speed significantly, scaling of the power supply should be accompanied by threshold voltage reduction. However, the lower limit for threshold voltage is set by the amount of off-state leakage current that can be tolerated. It is seen that if standard MOSFETs are used, a lower bound for power supply voltage or a larger leakage current become inevitable.

To extend the lower bound of power supply to ultra-low voltages (0.7V and below), we propose a dynamic threshold voltage MOS (DTMOS). By shorting the gate to the body, the threshold voltage operated under the dynamic threshold (DT) mode is reduced by forward biasing of the body, so its current drive can be significantly enhanced in the on state; on the other hand, since the device exhibits normal threshold voltage in the off state, low standby power consumption is maintained. It actually improves the circuit speed without compromising the standby power consumption. Furthermore, steep subthreshold slope, high carrier mobility, and other improved electric characteristic are available in the DT transistor because gate bias is applied to the silicon body [5-7].

1.1.3 Low Temperature Operation

With CMOS device performance gains becoming increasingly difficult to gather as a direct profit of dimensional scaling, one suggestion for improving device performance is operation at reduced temperatures, that offers decreased junction leakage, sharper subthreshold turn-off transition, higher switching speed due to increased carrier mobility and decreased electrical resistance, and increased reliability due to exponential slow down of thermally activated processes such as diffusion, electromigration, and chemical reaction. Furthermore, low-temperature CMOS (LT-CMOS) is also unconditionally latch up-free because of the decreased bipolar gains of the parasitic transistors. According to above, LT-CMOS with sub-micrometer channel lengths offer great promise for high-density, high-performance, and reliable VLSI logic systems [8-9].

1.1.4 Zero Temperature Coefficient Point (ZTC point)

There is a growing need in a number of important industries for integrated electronics that can operate reliably for extended periods under severe environmental conditions. Among these are the automobile, the earth and space exploration (probes), the geothermal exploration, the aircraft engine, and the nuclear reactor industries. Considerable progress has been made in recent years towards characterizing silicon CMOS technologies for wide temperature range operation. Accurate analytical and experimental studies have revealed that most digital, and many analogue, VLSI circuits can be operated satisfactorily up to 250℃ and beyond [10-12]. In addition, because conventional bipolar and weak inversion MOSFET derived, band gap-reference circuits are highly sensitive to leakage currents, they are useful over relatively narrow temperature ranges, and therefore inadequate for our purposes [13].

It is desirable to drive circuits designed for high temperature applications. It is a well established experimental fact that n and p-channel MOSFETs exhibit zero-temperature-coefficient (ZTC) points where the drain currents shows zero or very small variation with temperature in the linear and saturation regions. This criterion ensures that circuit parameters such as the offset voltage drift are less sensitive to the device matching tolerance [11-15].

1.2 Organization of the Thesis

By comparing the experimental data with theoretical concepts, we present a detailed study of the dependence of gate material and operation mode on the electric characteristics, such as threshold voltage, DIBL, and subthreshold swing, respectively. Here we will demonstrate the experimental results at 223K with excellent electrical characteristics.

Extending the above issue, we start to discuss the influence of temperature on the electric characteristics over the temperature range from 223K to 398K, and the results would encourage us to start the anticipation of ZTC point for DTMOS in the next section.

In the last part, for DTMOS, we first deduce a drain current model, and then present the analytical and experimental investigations of the ZTC point in the linear and saturation regions. We take into accounts of the parameters which depend on temperature, such as threshold voltage, mobility, and the body effects for the analysis; moreover, here show a series steps to extract those parameters. Finally we compare and analyze the ZTC bias values extracted from the theory and experimental results respectively.

Chapter 2

Performance of DTMOS with Polysilicon and Metal Gates under Different Operation Temperatures and Body Bias Effects

2.1 Introduction

2.1.1 Backgrounds

Among many metal gate materials, TiN is a very attractive candidate of mid-gap materials because of its excellent thermal stability, low resistivity and high CMOS-process compatibility [16-17]; also, TaC has been reported as a promising n-type material. On the other hand, speaking of high-k materials, Hf-based materials are more likely to be introduced in high-K/ metal gate application due to their good stability and compatibility with the conventional polysilicon gate process [2-3]. According to above, we will discuss the device characteristic issues of three different gate materials such as polysilicon, TaC, and TiN with HfSiON, respectively.

As to operation mode, even if DTMOS has big superiority, unfortunately, this device has a main drawback that the leakage current of the forward-biased p-n junction at the source fatally increases while $V_{bs} > 0.7V$ [5][7]. Therefore, the supplied voltage must be limited to make eq. 2-1 be tenable as shown as following:

$$V_{bs} \leq 0.7V \qquad \text{(eq. 2-1)}$$

As a result, the validation range of α could be expressed as following:

$$V_{bs} = \alpha V_{gs}, \text{and } 0 \leq \alpha \leq 1 \qquad \text{(eq. 2-2)}$$

As V_{gs} is fixed, low value of α would result in low V_{bs}, which prevents the DTMOS from enjoying a large threshold voltage reduction in on-state, and thus minimizes the current gain, but that actually could increase its upper limit of V_{gs}. As a result, there are three operation modes existing, respectively DT-A mode ($\alpha = 0.7$), DT-B mode ($\alpha = 1$), and normal mode ($\alpha = 0$), to discuss the trade-off between threshold voltage reduction and upper limit of gate voltage.

Reference to operation environment temperature, although the operation at low temperature brings about many preferential benefits, while the temperature approaching absolute zero, silicon FET's would exhibit freezeout of mobile carriers in nondegenerate substrates [9]; furthermore, below 200 K, the relationship between the inverse mobility and the vertical field for n-channel devices is modified presumably due to the change of the scattering mechanism, and the traditional deduction of mobility has not been suitable anymore [18]. Therefore, we lower the operation temperature only to 223K to avoid the freeseout problem and additional scattering mechanisms, and then freely enjoy the mentioned benefits from low temperature operation.

2.1.2 Motivation

According to above, high-K/ metal gate arranging in pairs DT-operation at low temperature may obtain very excellent current gain, especially when the applied gate bias surpasses the ZTC point bias. We will compare the fit and unfit quality of polysilicon and metal gates, and simultaneously discuss those advantages and disadvantages of normal and DT modes to figure out the trade-off.

2.2 Experiment

2.2.1Device fabrication

All transistors used in this work were fabricated by state-of-the-art 300 mm wafer foundry technology. HfSiO with Hf/(Hf+Si) ratio of 50% was annealing under NH_3. The high-K and 100Å metal films were deposited by atomic-layer deposition (ALD) with 40 cycles and physical vapor deposition (PVD) techniques, respectively, followed by a 1000 Å polysilicon cap layer. In addition, before deposited the high-K dielectric, the chemical oxide was used as the interfacial layer. After gate patterning, halo implantation was used to optimize the short channel control. Eventually, a high-temperature annealing during source/drain activation and BEOL followed.

2.2.2Measurement setup

First, we set three operation modes, namely DT-A mode ($\alpha = 0.7$), DT-B mode ($\alpha = 1$), and normal mode ($\alpha = 0$). Here, the threshold voltage is defined by constant current method [$I_d = 40(\frac{W}{L})$ nA] which painstakingly makes drain current independent of device geometry, and the measurement is simple with only one voltage measurement necessary.

In addition, the definition of drain induced barrier lowing (DIBL) and subthreshold swing (SS) are as following:

$$\text{DIBL} \equiv \frac{\Delta V_t}{\Delta V_{ds}}\Big|_{V_{ds}=0.1 \text{ and } 0.7 \text{ V}} \qquad \text{(def. 2-1)}$$

and

$$\text{SS} \equiv \left(\frac{\partial \log I_d^{sub}}{\partial V_{gs}}\right)^{-1} \qquad \text{(def. 2-2)}$$

We would extract DIBL and subthreshold swing from $I_d - V_{gs}$ curves measured by Keithley 4200 semiconductor parameter analyzer over wide operation temperature ranges from 223K to 398K.

Finally, CV characteristics are measured at a frequency of 1MHz with different metal gate devices to extract the equivalent oxide thicknesses and discuss the gate control capability.

2.3 Results and Discussions

2.3.1 The Comparison of Performance for DTMOS with Polysilicon and Metal Gates under Different Body Bias Effects

2.3.1.1 Characteristics of Drain Current

Fig. 2-1 shows the characteristics of $I_d - V_{gs}$ with polysilicon, TaC, and TiN gates under DT-mode, respectively. In DT-mode with connecting gate to bulk together, due to the threshold voltage is a function of V_{bs}, the higher V_{bs} would reduce the body charge and thus the threshold voltage.

The reduction of body charge would lead to a lower effective normal field in the device and bring on the higher carrier mobility. The normal field could be expressed as following:

$$E_{eff,normal} \equiv \frac{Q_B + \frac{Q_n}{2}}{\epsilon_s} \qquad \text{(eq. 2-3)}$$

In addition, the net result of threshold voltage reduction is effective to increase the inversion charge or equivalently the gate capacitance as shown in eq. 2-4, and provide an effectively thinner gate oxide for DTMOS [5].

$$dQ_n = C_{ox}\left(\partial V_{gs} - \frac{\partial V_t}{\partial V_{gs}}\right) = C_{ox}\left(\partial V_{gs} + \left|\frac{\partial V_t}{\partial V_{gs}}\right|\right) \quad \text{(eq. 2-4)}$$

The improvements of mobility and inversion charge lead to a higher current drive in DTMOS, especially under DT-B mode which has the highest body bias while V_{gs} is fixed. Moreover, low temperature operation and metal gate actually further enhance the performance [19].

However, we have forbidden that $V_{bs} > 0.7V$, so, although higher value of α brings about higher reduction of threshold voltage and higher drain current gain, but it also reduces the upper bound of V_{gs} and thus the corresponding on-state drain current.

2.3.1.2 Characteristics of Threshold Voltage

The theoretical threshold voltage for large-geometry, n-channel device on uniformly doped substrates with body bias $V_{bs} = \alpha V_{gs}$ is expressed as [20]:

$$V_t = V_{fb} + 2\emptyset_{fp} + \frac{\sqrt{2 \in_{Si} qN_a\left(2\emptyset_{fp} - \alpha V_{gs}\right)}}{C_{ox}}$$

$$= \emptyset_{ms} - \frac{Q_{ss}}{C_{ox}} + 2\emptyset_{fp} + \frac{\sqrt{2\in_{Si} qN_a\left(2\emptyset_{fp} - \alpha V_{gs}\right)}}{C_{ox}} \quad \text{(eq. 2-5)}$$

$\emptyset_{ms}$ is the working function difference between the gate material and the bulk semiconductor; V_{fb} is the flat band voltage; $\emptyset_{fp}$ is the potential difference between the Fermi level and the intrinsic Fermi level of the bulk semiconductor; C_{ox} is the gate oxide capacitance; Q_{ss} is the fixed oxide charge, and N_a is the channel doping concentration.

Here, supposing Q_{ss}, N_a, and $\emptyset_{fp}$ of the three devices are the same, for a low threshold voltage, it's preferable to have low $\emptyset_{ms}$, high C_{ox}, and high α. As shown

in Table 2.1 [2][3][21] and Fig. 2-2, $\emptyset_{ms}$ actually induces the profoundest influence on threshold voltage. So, even though polysilicon gate device shows the lowest C_{ox} in Fig. 2-3 due to poly-depletion capacitance [22], still has the lowest threshold voltage among the three devices. Similar results for PMOS are shown in Fig. 2-4 and 2-5.

Before discussing V_t roll-off, we need to know how the gate influences the formation of inversion layer under DT-mode. In subthreshold region, V_{bs} would lower the potential barrier height of the source node [23]:

$$\emptyset_{source} = \emptyset_{source\ o} - V_{bs} \qquad \text{(eq. 2-6)}$$

$\emptyset_{source\ o}$ is the intrinsic potential of source node. In the thermal equilibrium $(V_{gs} = 0, V_{fb} = 0)$:

$$\emptyset_{source\ o} - \emptyset_s = \emptyset_{bi} \qquad \text{(eq. 2-7)}$$

$\emptyset_s$ is the surface potential, and $\emptyset_{bi}$ is the intrinsic potential of p-n^+ junction for p type substrate and n^+ type source region.

On other hand, the influences of body bias on surface potential is negligible due to no inversion charge, so $\emptyset_s$ can be consider as a function of only normal bias [20][23]. In addition, the lowing of $\emptyset_{source}$ induced by V_{bs} could promote the formation of inversion layer, so we define the gate control capability of DTMOS in subthreshold region as following:

$$\text{Gate control capability}|_{sub} \equiv \frac{d\emptyset_s}{dV_{gs}} + \left(-\frac{d\emptyset_{source}}{dV_{gs}}\right) \qquad \text{(def. 2-3)}$$

We know that applying V_{bs} to the substrate is equivalent to dropping the voltages of all other node of the device, namely, gate, drain, and source, by V_{bs}. So, now the

normal bias equals $V_{gs} - V_{bs}$ [23], and we have the following relationship:

$$V_{gs} - V_{bs} - V_{fb} = V_{gs} - \alpha V_{gs} - V_{fb} = \emptyset_s + \frac{\sqrt{2\epsilon_{Si} q N_a \emptyset_s}}{C_{ox}} \qquad \text{(eq. 2-8)}$$

Differentiating eq.2-8 with respect to V_{gs} yields:

$$1 - \alpha = \frac{d\emptyset_s}{dV_{gs}} + \frac{d\emptyset_s}{dV_{gs}} \frac{\sqrt{\frac{\epsilon_{Si} q N_a}{2\emptyset_s}}}{C_{ox}} = \frac{d\emptyset_s}{dV_{gs}} \left(1 + \frac{C_d}{C_{ox}}\right) \qquad \text{(eq. 2-9)}$$

C_d is the capacitance of depletion layer. The relative change of $\emptyset_s$ and V_{gs} is calculated as:

$$\frac{d\emptyset_s}{dV_{gs}} = \frac{1-\alpha}{1+\frac{C_d}{C_{ox}}} \qquad \text{(eq. 2-10)}$$

On the other hand, the relative change of $\emptyset_{source}$ and V_{gs} is calculated as following:

$$-\frac{d\emptyset_{source}}{dV_{gs}} = -\frac{d(\emptyset_{source\,o} - V_{bs})}{dV_{gs}} = -\frac{d(\emptyset_{source\,o} - \alpha V_{gs})}{dV_{gs}} = \frac{d\alpha V_{gs}}{dV_{gs}} = \alpha \qquad \text{(eq. 2-11)}$$

So, def. 2-3 is calculated as:

$$\frac{d\emptyset_s}{dV_{gs}} + \left(-\frac{d\emptyset_{source}}{dV_{gs}}\right) = \frac{1-\alpha}{1+\frac{C_d}{C_{ox}}} + \alpha = \frac{1+\alpha\frac{C_d}{C_{ox}}}{1+\frac{C_d}{C_{ox}}} \qquad \text{(eq. 2-12)}$$

According to eq. 2-7, while $(\emptyset_{source} - \emptyset_s)$ equals $(\emptyset_{bi} - 2\emptyset_{fp})$, a large amount of electrons inject to the surface from source node, and then inversion layer is formed. Now V_{bs} would influences not only $\emptyset_{source}$ but also $\emptyset_s$ due to the injection of inversion charge. Finally the surface potential begins to couple with the body bias.

From mathematics viewpoint, according to eq. 2-12, lower $\frac{C_d}{C_{ox}}$ and higher α could increase the result value. Furthermore, we use body effect parameter as following to figure out the gate control capability:

$$\delta \equiv \frac{\partial V_t(V_{bs})}{\partial V_{sb}} = \frac{\sqrt{\frac{q\epsilon_{Si}N_a}{2(2\phi_{fp}-V_{bs})}}}{C_{ox}} = \frac{C_d}{C_{ox}} \qquad \text{(def. 2-4)}$$

As shown in Fig. 2-6, metal gates would have better gate control capability, especially at low temperature, and thus improve the V_t roll-off as in Fig. 2-7.

Ideally, if α equals 1, no matters how $\frac{C_d}{C_{ox}}$ changes, the gate control capability would not be effected and always equals 1, but in reality, there are some non-ideal factors existing, such as substrate parasitic resistance [7], so the gate control capability under DT-B mode don't equal 1, and it changes from device to device. For all this, the V_t roll-off under DT-B mode is still improved much better than the other two modes as usual.

2.3.1.3 Characteristics of Drain Induced Barrier Lowing (DIBL)

Source and drain depletion regions are a certain fraction of the channel. When the effective channel length L_g is shorter, the drain is closer to the source, and V_{ds} can influence $\emptyset_{source}$, so that the channel carrier concentration at that location is no longer fixed, and short channel effect (SCE) starts to occur. The lowing of $\emptyset_{source}$ causes an injection of extra carriers, thereby increasing the currents in both on-state and subthreshold regimes, so, short L_g would enhance DIBL effect as shown in Fig. 2-8 and 2-9, and also result in higher subthreshold swing as shown in next section [20]. Under DT-mode, due to the narrower S/D depletion width induced by forward body bias, DT-B mode shows the lowest DIBL [7]. In addition, the two metal gates

exhibit their inherent stronger gate control capability once more as shown in Fig. 2-10.

Being worth mentioning, the DIBL effect is defined as the vertical parallel shift of $I_d - V_{gs}$ curve at a given drain voltage and elevated drain voltage in the subthreshold regime [24]. For PMOS counterparts, long-channel behavior is totally lost while L_g scaling down to 0.1μm, and the $I_d - V_{gs}$ curves are no longer vertical parallel; as a result, the gate length small than 0.1μm is not discussed here.

2.3.1.4 Characteristics of Subthreshold Swing

When $V_{gs} < V_t$, the corresponding drain current is called the subthreshold current. In weak inversion and depletion, the electron charge is small and the drain current is dominated by diffusion. According to def. 2-3, we can deduce that subthreshold current for DTMOS could be as following [23]:

$$I_d^{sub} \propto e^{\frac{q(\emptyset_s - \emptyset_{source})}{KT}} \qquad \text{(eq. 2-13)}$$

According to def. 2-2, subthreshold swing of DTMOS can now be calculated as:

$$SS \equiv \left(\frac{\partial \log I_d^{sub}}{\partial V_{gs}}\right)^{-1} = \ln 10 \frac{KT}{q}\left(\frac{\partial(\emptyset_s - \emptyset_{source})}{\partial V_{gs}}\right)^{-1} = 2.3\frac{KT}{q}\frac{1+\frac{C_d}{C_{ox}}}{1+\alpha\frac{C_d}{C_{ox}}} \qquad \text{(eq. 2-14)}$$

According to ex-part about DIBL, we've known that SCE would induce higher subthreshold swing as in Fig. 2-11 and 2-12. Furthermore, as in Fig. 2-13, metal gate devices under DT-B mode unfold the better performance again due to their excellent gate control capability.

As well as DIBL, while L_g down to sub-0.1μm the subthreshold swing for PMOS counterparts become too worst to be extracted; massive increasing of above-threshold and subthreshold currents cause those devices not turned off any more.

2.3.2 Comparison of Performance for DTMOS under Different Operation Temperatures

In the section, by comparing the experimental data with theoretical concepts, we present a study of the temperature dependence on the electric characteristics for DTMOS.

From the basic equations as shown as following [25]:

$$\emptyset_{fp} = \frac{KT}{q} \ln\left(\frac{N_a}{N_i}\right) \quad \text{(eq. 2-15)}$$

and

$$N_i \propto T^{\frac{3}{2}} \exp\left(\frac{-Eg_0}{2KT}\right) \quad \text{(eq. 2-16)}$$

Eg_0 is the energy gap at T= 0K, we abtain:

$$\frac{d\emptyset_{fp}}{dT} = \frac{\emptyset_{fp}}{T} - \frac{K}{2q}\left(3 + \frac{Eg_0}{KT}\right) < 0 \quad \text{(eq. 2-17)}$$

and

$$\frac{dV_t}{dT} = \frac{d\emptyset_{fp}}{dT}\left(2 + \frac{1}{C_{ox}}\sqrt{\frac{2\epsilon_{Si} q N_a}{2\emptyset_{fp} - \alpha V_{gs}}}\right) < 0 \quad \text{(eq. 2-18)}$$

According to def. 2-4 and eq. 2-17, we know that:

$$\frac{d\delta(V_{bs},T)}{dT} > 0 \quad \text{(eq. 2-19)}$$

In terms of eq. 2-18 and 2-19, elevated temperature results in threshold voltage reduction and degradation of gate control capability as shown in Fig. 2-6 [24][26-27]. Hence high temperature deteriorates SCE, such as V_t roll-off, DIBL, and subthreshold swing shown as from Fig. 2.-14 to Fig. 2-37.

In addition, in order to derive the detailed temperature dependence of subthreshold swing, we start from eq. 2-14 where the terms $\frac{KT}{q}$ and $\frac{1+\frac{C_d}{C_{ox}}}{1+\alpha\frac{C_d}{C_{ox}}}$ both increase with

temperature while $\alpha < 1$, so the subthershold swing of DTMOS would be more sensitive in temperature.

2.3.3 Existence of ZTC point for DTMOS

According Fig. 2-38, we infer that there is a way to obtain low leakage and high on-state current at the same time: If the ZTC point for DTMOS exists, we could apply V_{gs} higher than $V_{gs}(ZTC)$, the ZTC bias, under low temperature operation to obtain the excellent current gain.

From Fig. 2-39, regardless of normal or DT modes, a remarkable staggered spot appears, that's a strong evidence of the existence of ZTC point. By far, the phenomenon is more obvious in Fig. 2-40. At $V_{gs} = 0.8V$, the drain current at high temperature is high due to $V_{gs}(ZTC) > 0.8V$; at $V_{gs} = 1.1V$, since the ZTC point appears, the $I_d - V_{gs}$ curves collaborate with each other; At $V_{gs} = 1.4V$, high temperature results in low on-state current, and then we can deduce that $1.4V > V_{gs}(ZTC)$. After proving the existence of ZTC point, now we are going to deliberate the theoretical model of ZTC point for DTMOS in next chapter to help us achieve the excellent current gain.

2.4 Summary

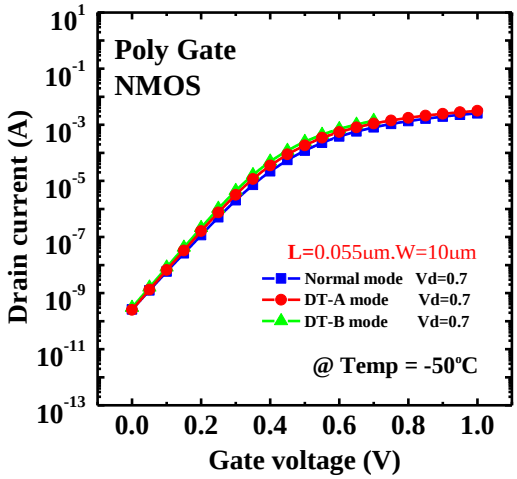
In the session, we define the gate control capability for DTMOS. From the theoretical inference process, we find that higher α and lower $\delta(V_{bs})$ can result in higher gate control capability; on the other hand, from the experimental results, metal gates have lower $\delta(V_{bs})$ than polysilicon gate, and low temperature operation further reduces $\delta(V_{bs})$, so metal gate devices under DT-B mode at low temperature operation bring about best gate control capability, along with excellent performance, such as

improved V_t roll-off, better DIBL, and lower subthreshold swing.

In the end of the chapter, we show the existence of ZTC point for DTMOS, which could tell us how to hypothesize the supply voltage to get the best current gain under low temperature operation.

(a)

(b)



(C)

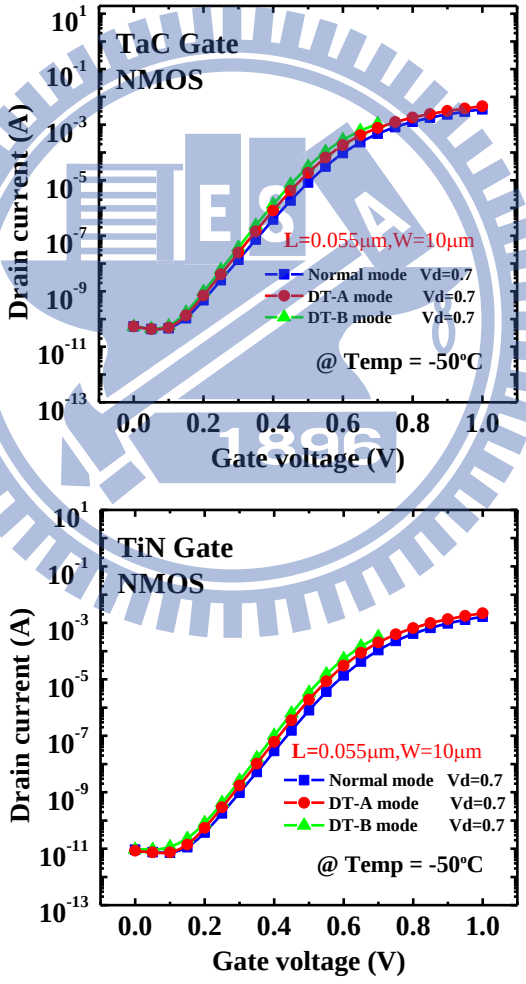
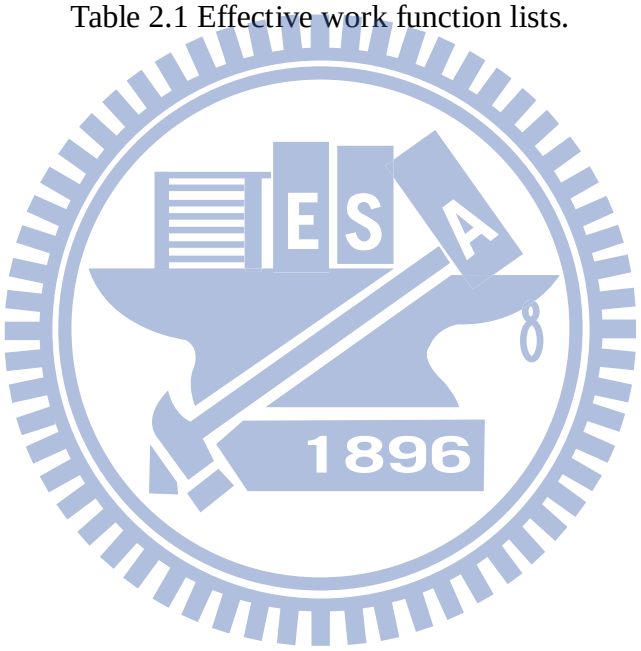


Fig. 2-1 Drain current versus gate voltage for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223K.

	Poly-Si	TaC	TiN
NMOS_EWF (eV)	4.1	4.45	4.7
PMOS_EWF (eV)	5.2	4.45	4.7

Table 2.1 Effective work function lists.



(a)

(b)

(C)

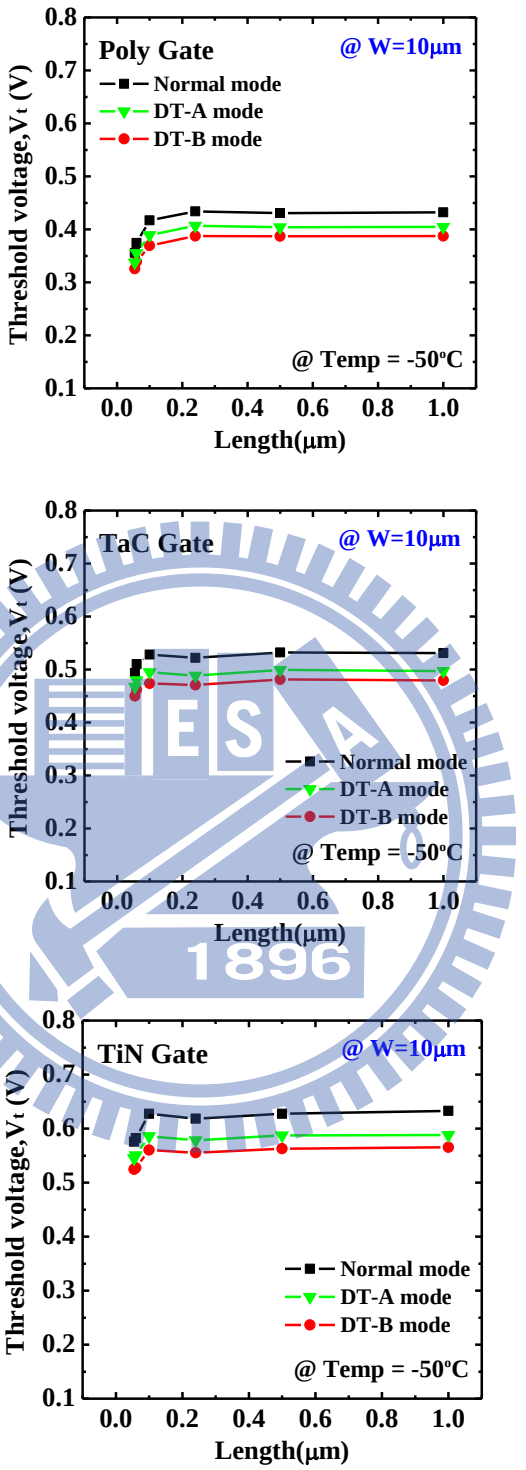


Fig. 2-2 Threshold voltage versus gate length for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223K.

(a)

(b)

(C)

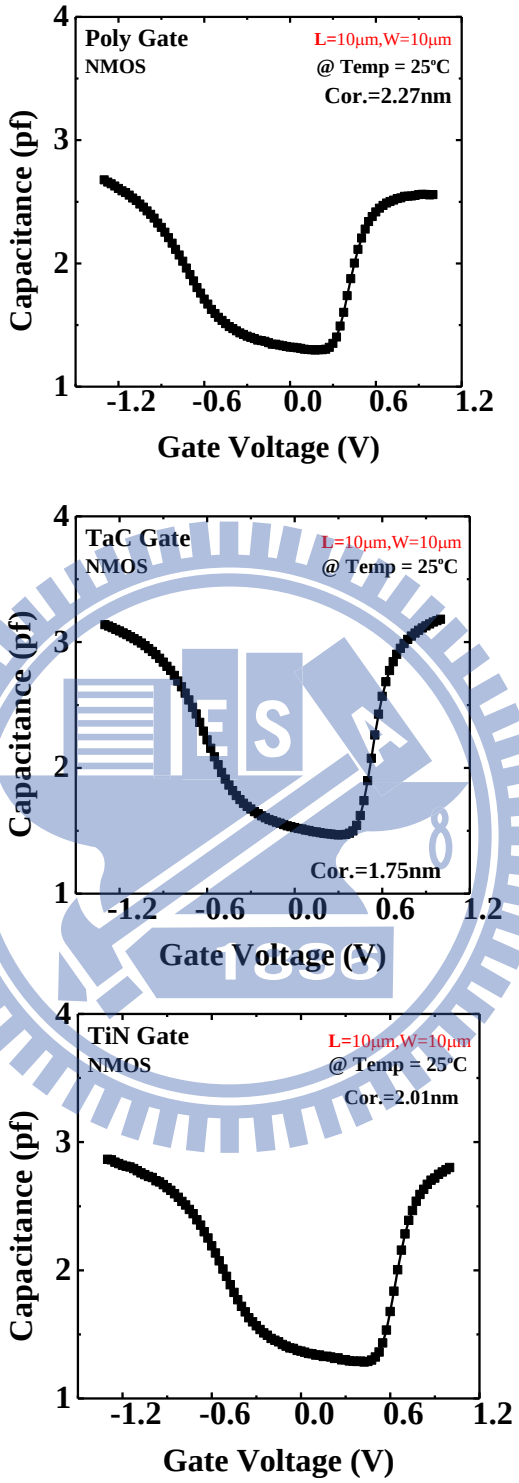
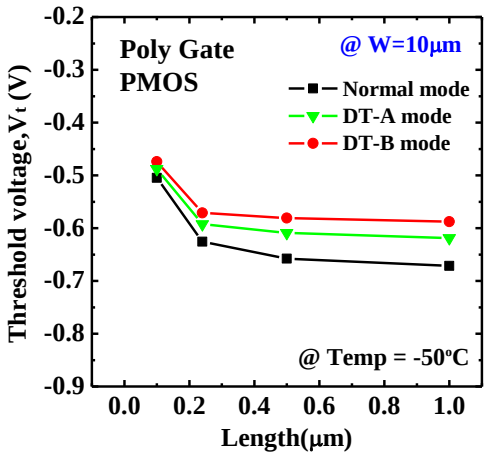


Fig. 2-3 High frequency C-V characteristics at 1 MHz for NMOS with (a) polysilicon (b) TaC (c) TiN gate.

(a)



(b)

(C)

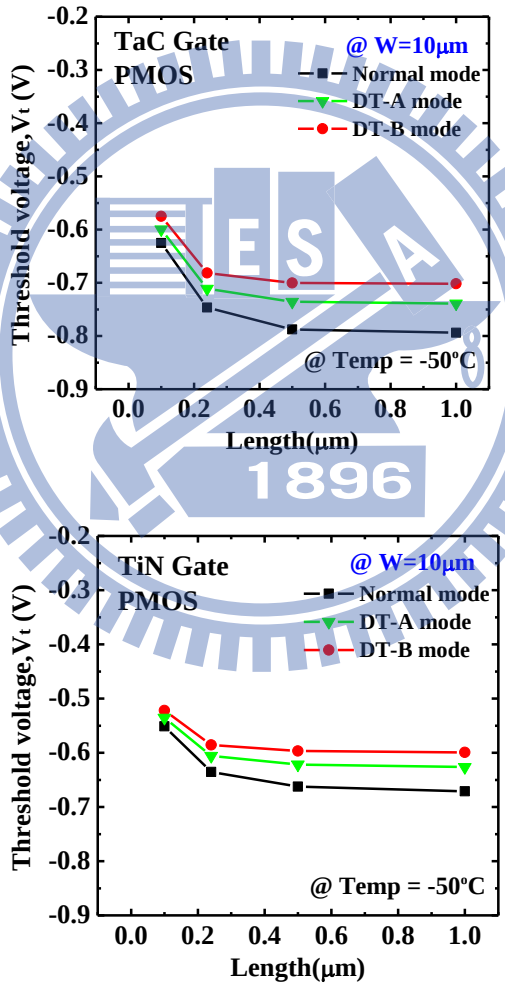


Fig. 2-4 Threshold voltage versus gate length for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223 K.

(a)

(b)

(C)

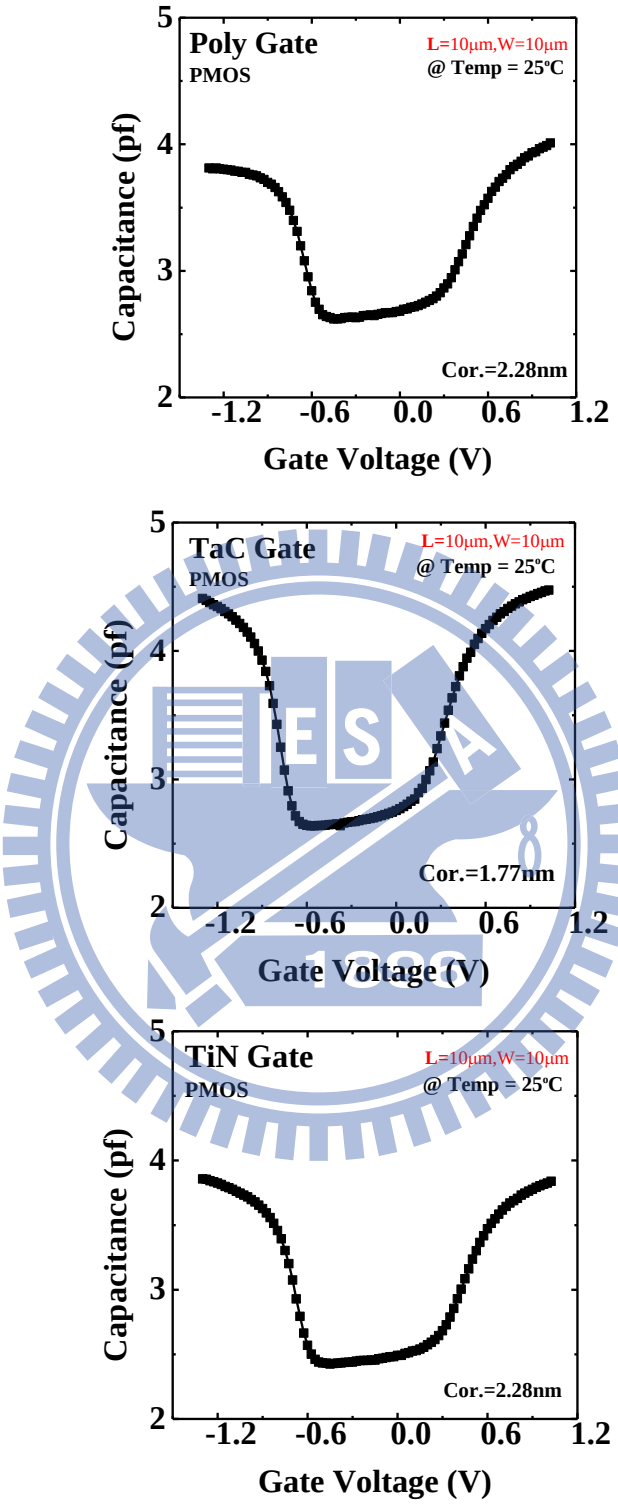
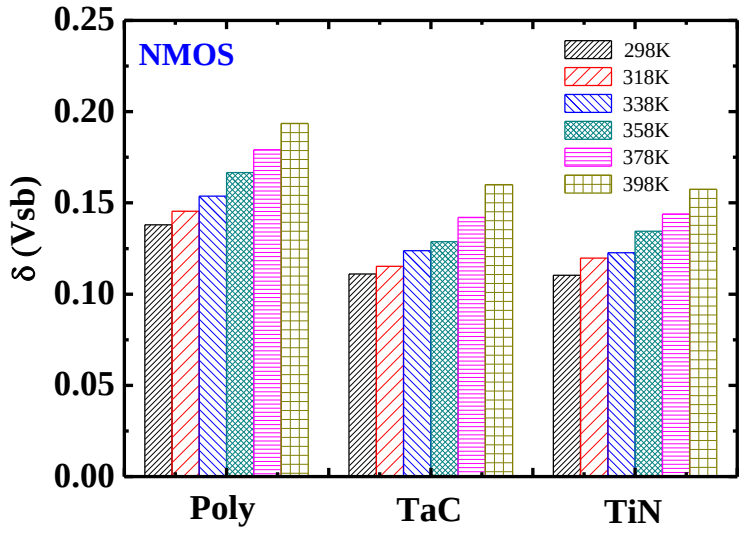


Fig. 2-5 High frequency C-V characteristics at 1 MHz for PMOS with (a) polysilicon (b) TaC (c) TiN gate.

(a)



(b)

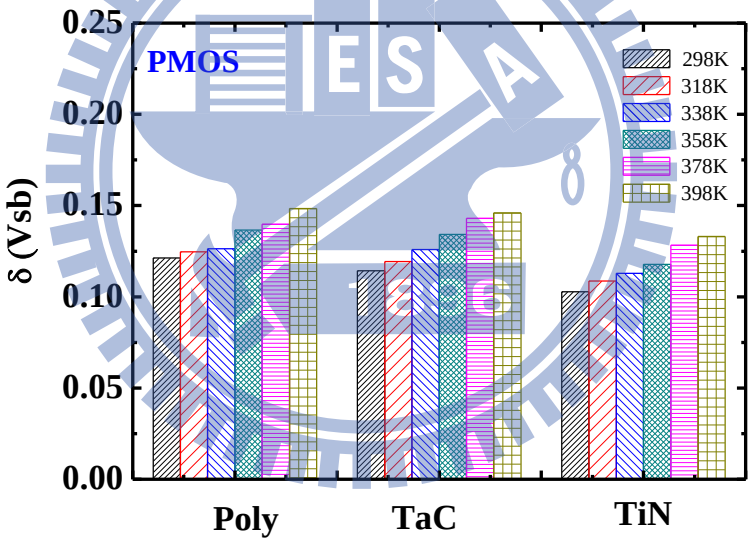
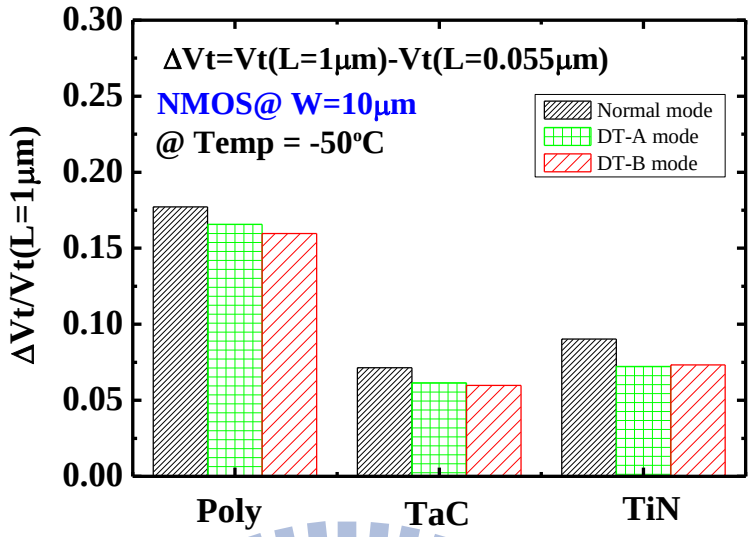


Fig. 2-6 $\delta(V_{bs}, T)$ of polysilicon, TaC, and TiN gates over a range of operation temperature from 298K to 398K for (a) NMOS (b) PMOS.

(a)



(b)

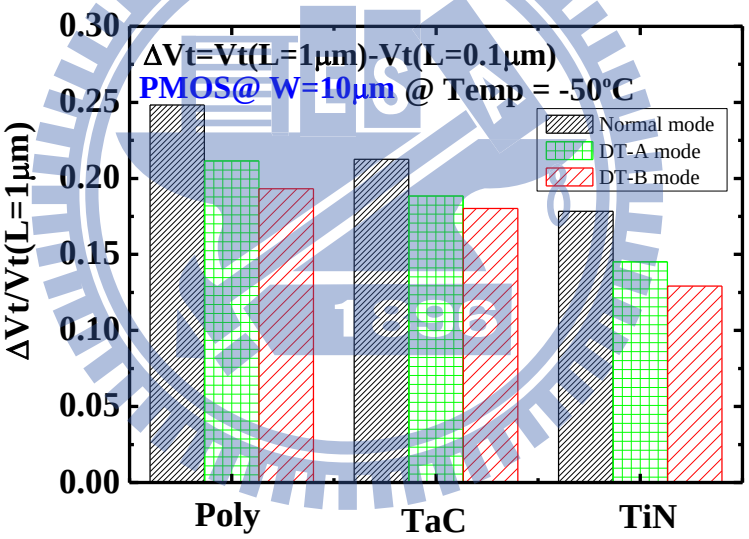
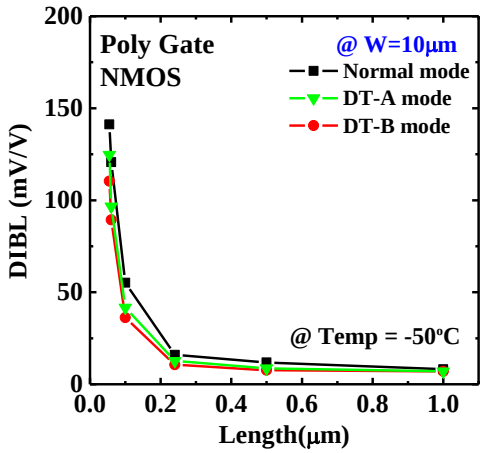
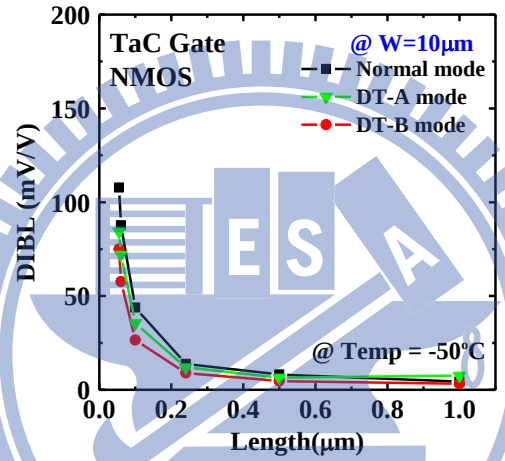


Fig. 2-7 Threshold voltage roll-off characteristics of (a) NMOS (b) PMOS with polysilicon, TaC and TiN gate under normal, DT-A and DT-B modes, respectively. The operation temperature is fixed at 223K.

(a)



(b)



(C)

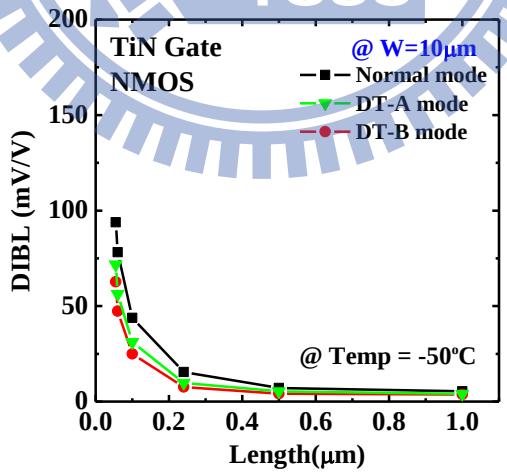


Fig. 2-8 DIBL versus gate length for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223K.

(a)

(b)

(C)

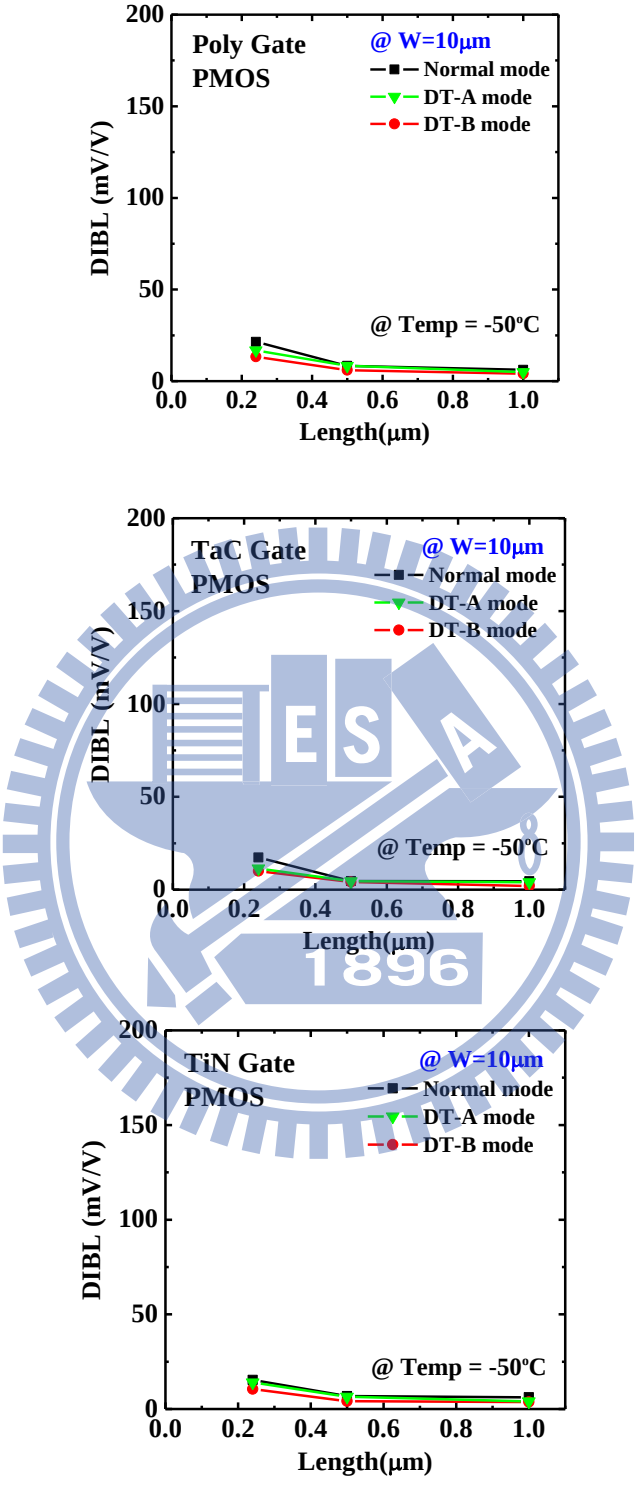
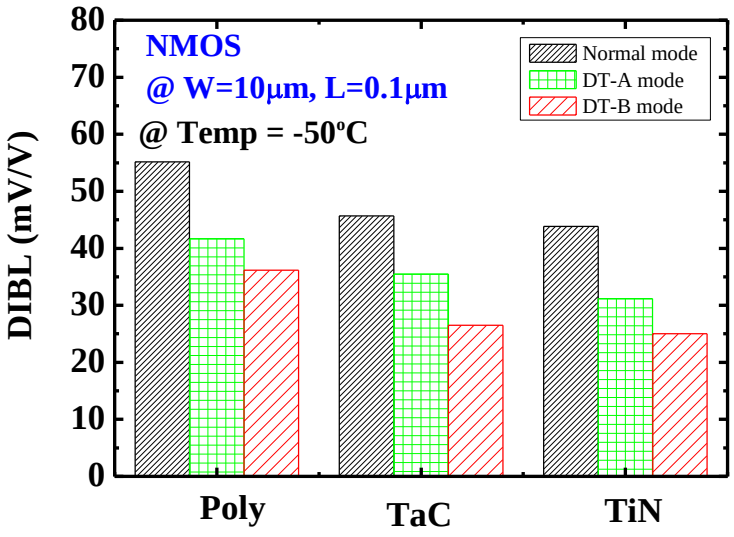


Fig. 2-9 DIBL versus gate length for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223K.

(a)



(b)

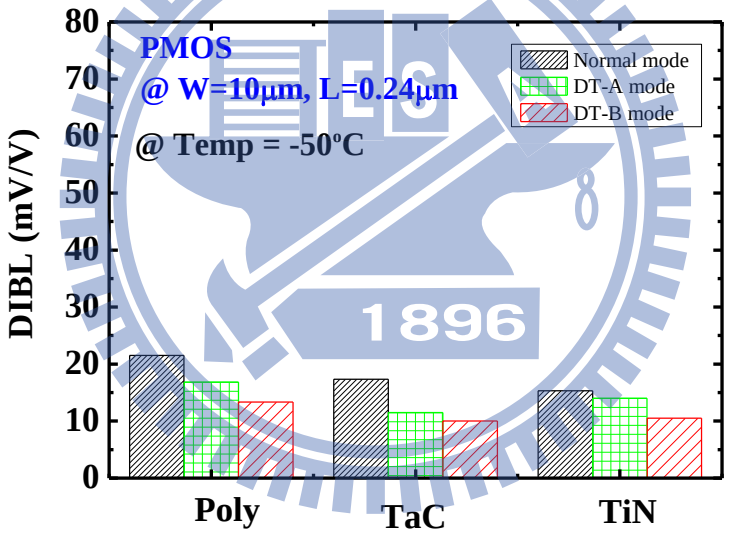


Fig. 2-10 DIBL of (a) NMOS (b) PMOS with polysilicon, TaC and TiN gate under normal, DT-A and DT-B modes, respectively. The operation temperature is fixed at 223K.

(a)

(b)

(C)

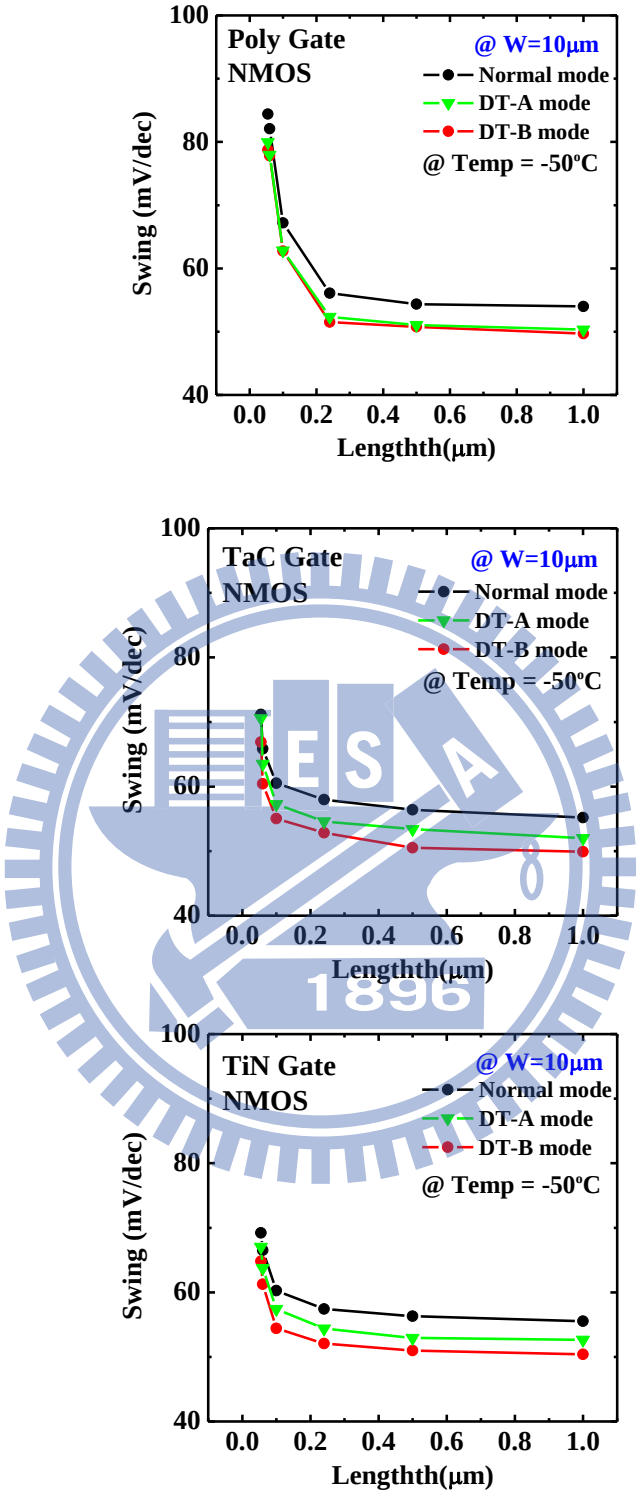


Fig. 2-11 Subthershold swing versus gate length for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223K.

(a)

(b)

(C)

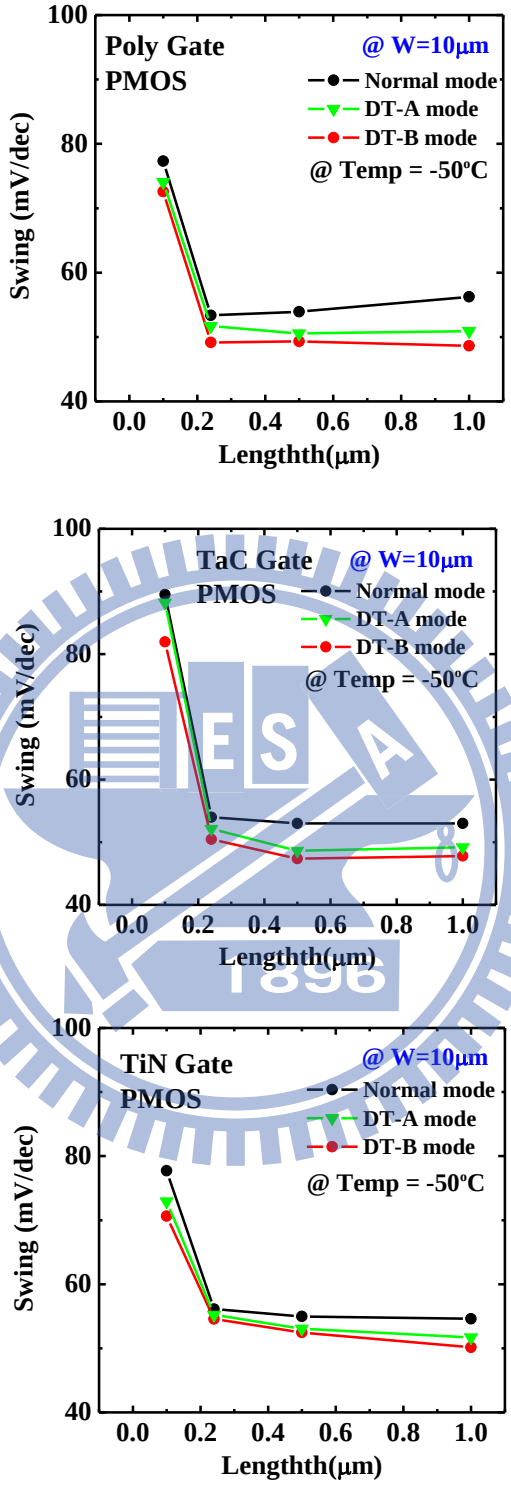
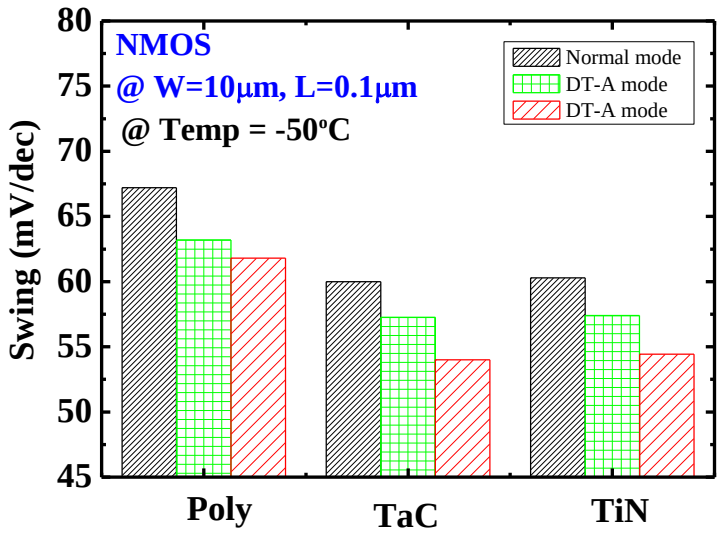


Fig. 2-12 Subthershold swing versus gate length for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A and DT-B modes. The operation temperature is fixed at 223K.

(a)



(b)

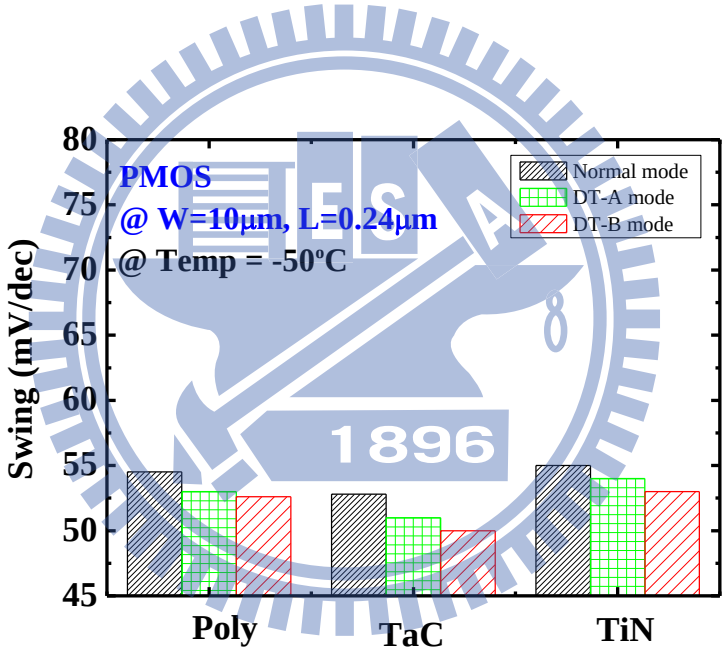


Fig. 2-13 Subthershold swing of (a) NMOS (b) PMOS with polysilicon, TaC and TiN gate under normal, DT-A and DT-B modes, respectively. The operation temperature is fixed at 223K.

(a)

(b)

(C)

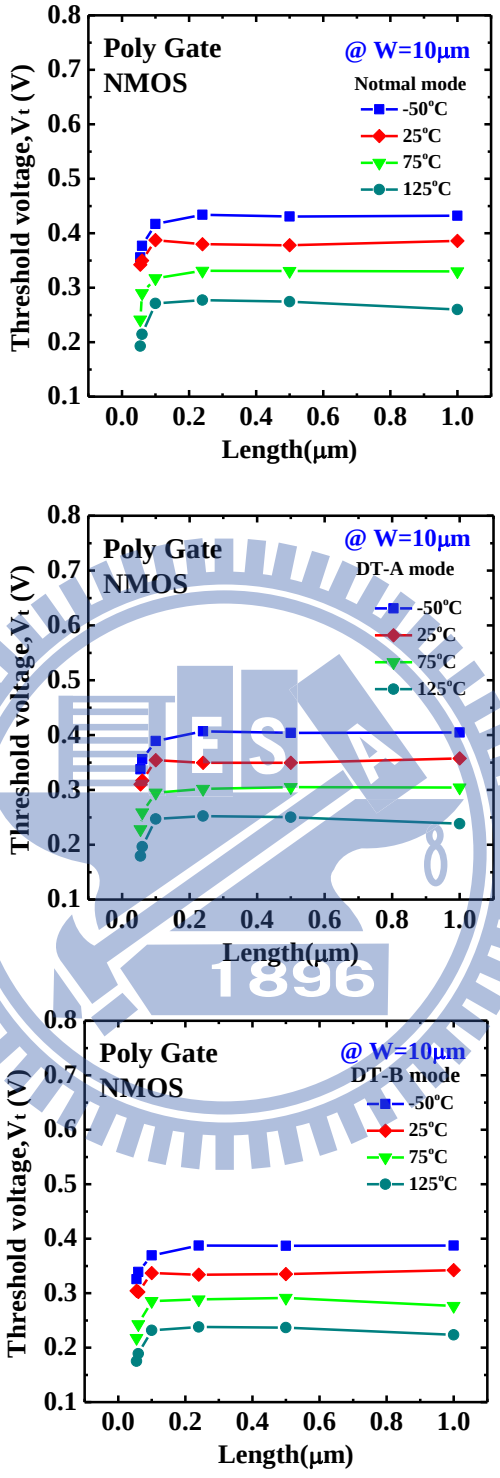


Fig. 2-14 Threshold voltage versus gate length for NMOS with polisilicon gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

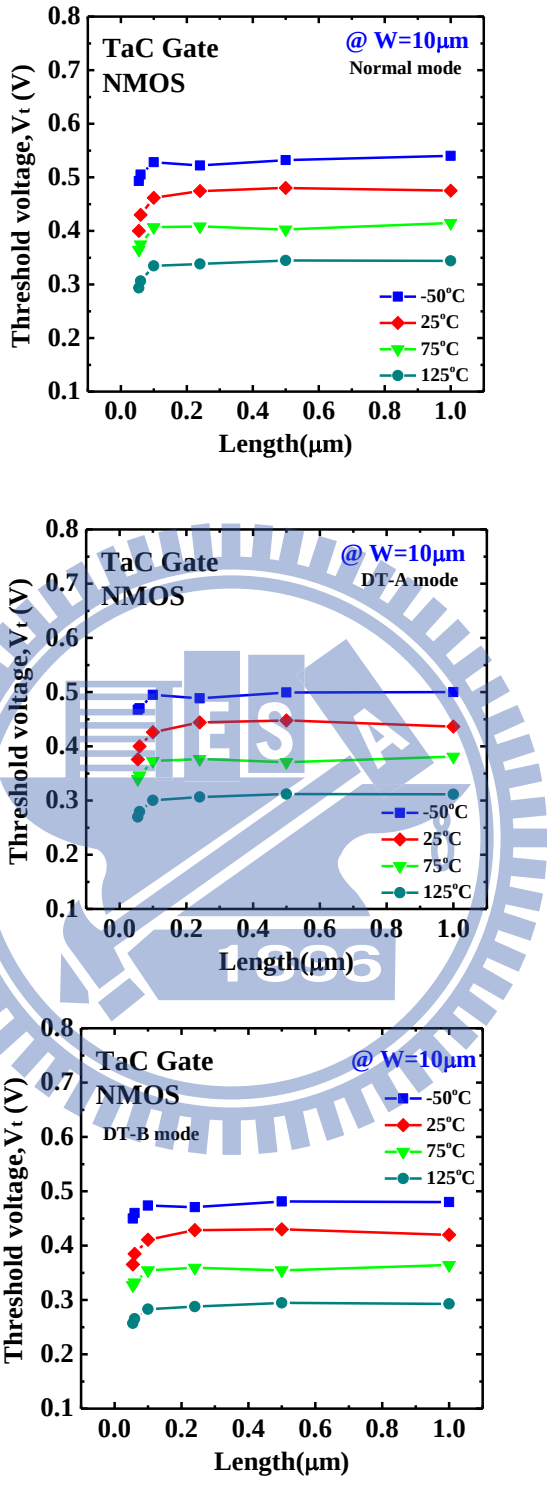


Fig. 2-15 Threshold voltage versus gate length for NMOS with TaC gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

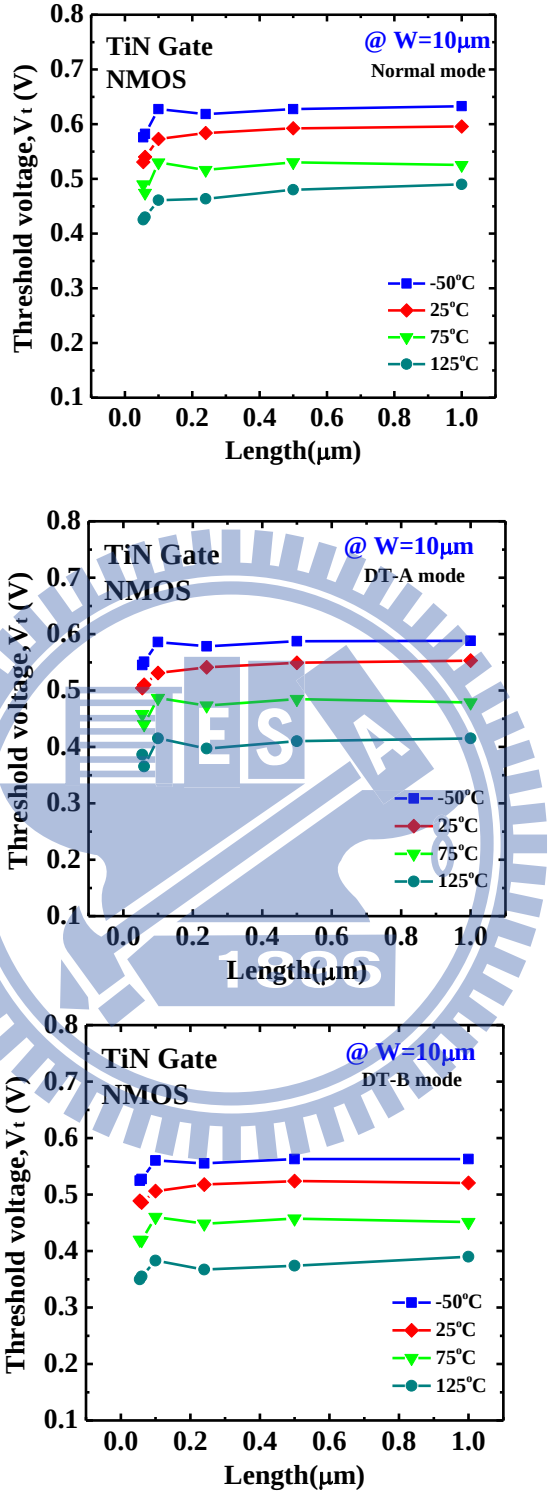
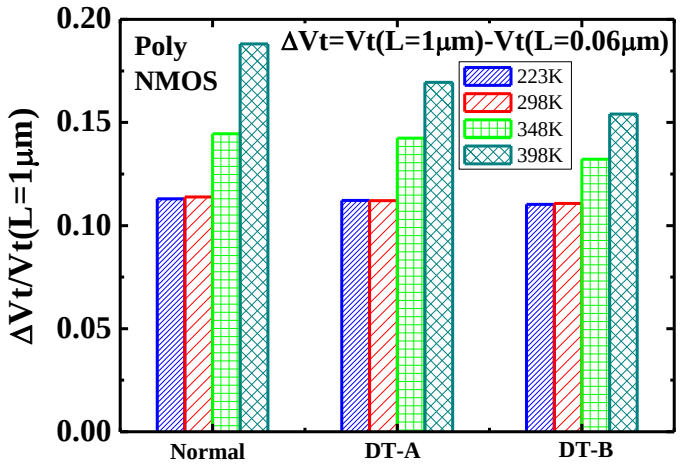


Fig. 2-16 Threshold voltage versus gate length for NMOS with TiN gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)



(C)

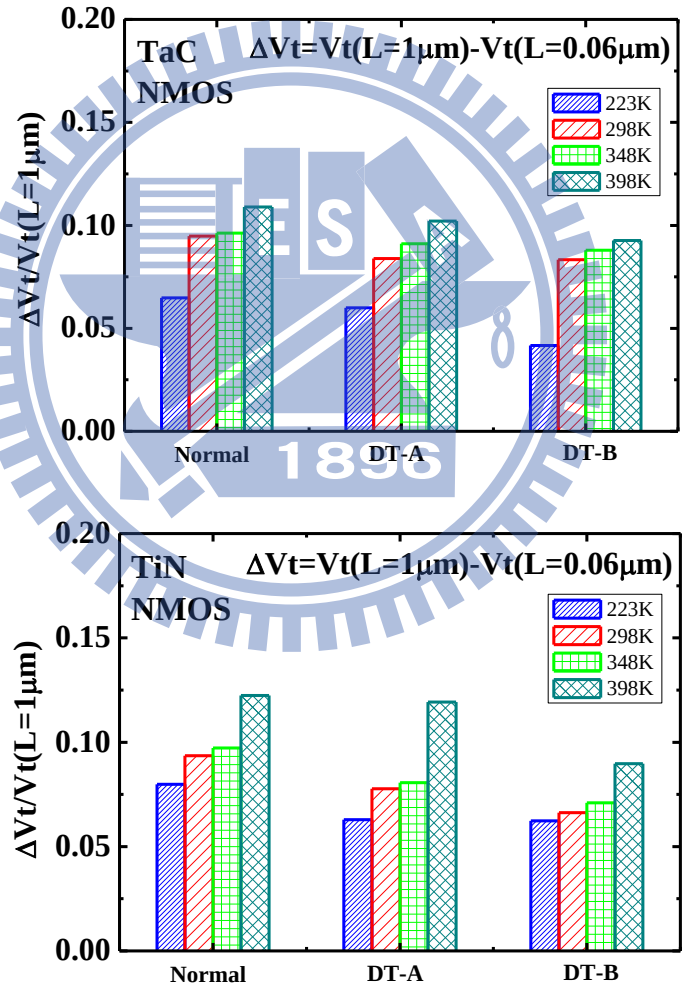


Fig. 2-17 Threshold voltage roll-off for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A, DT-B gate mode for different operation temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

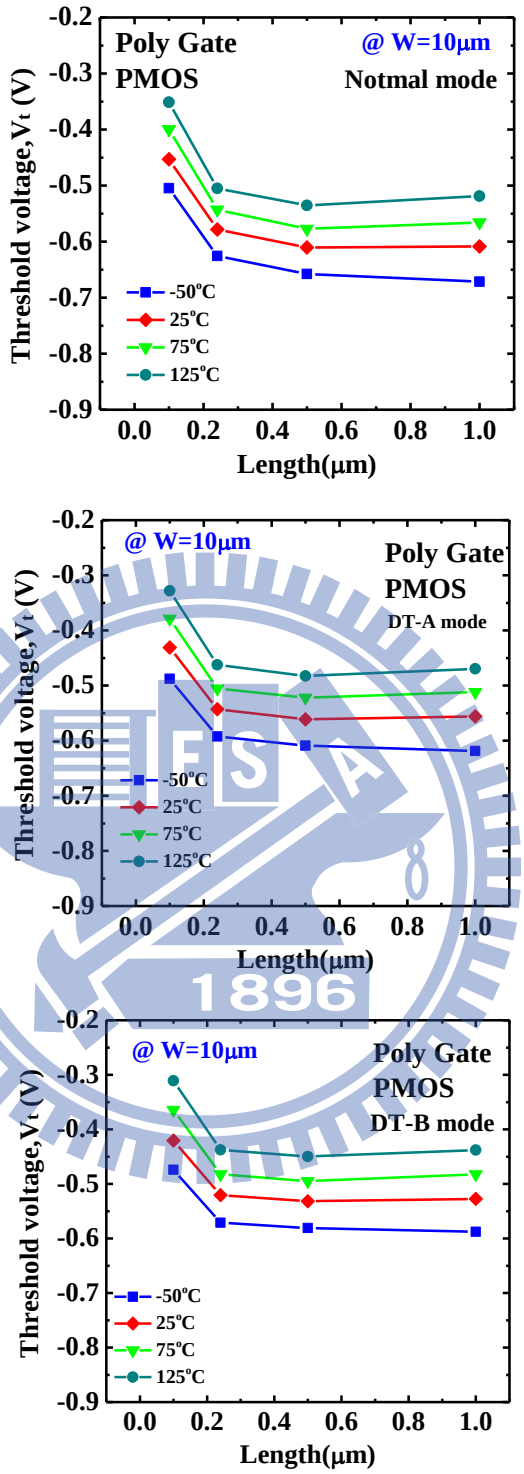


Fig. 2-18 Threshold voltage versus gate length for PMOS with polisilicon gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

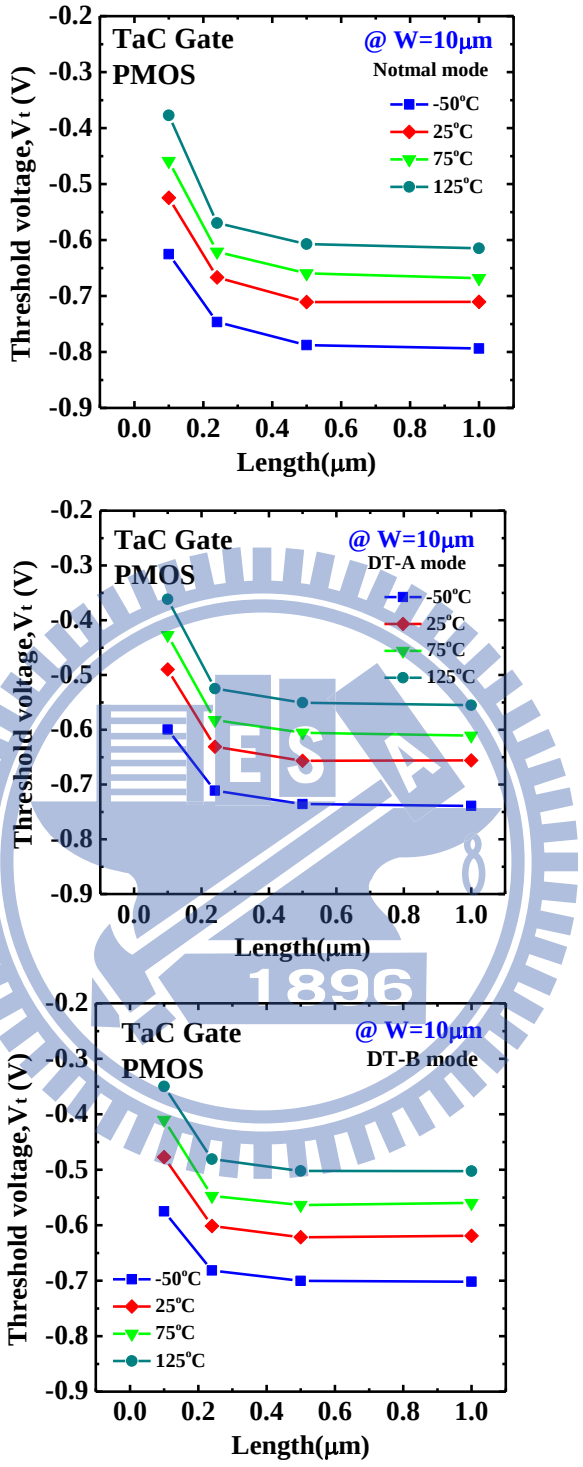


Fig. 2-19 Threshold voltage versus gate length for PMOS with TaC gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively

(a)

(b)

(C)

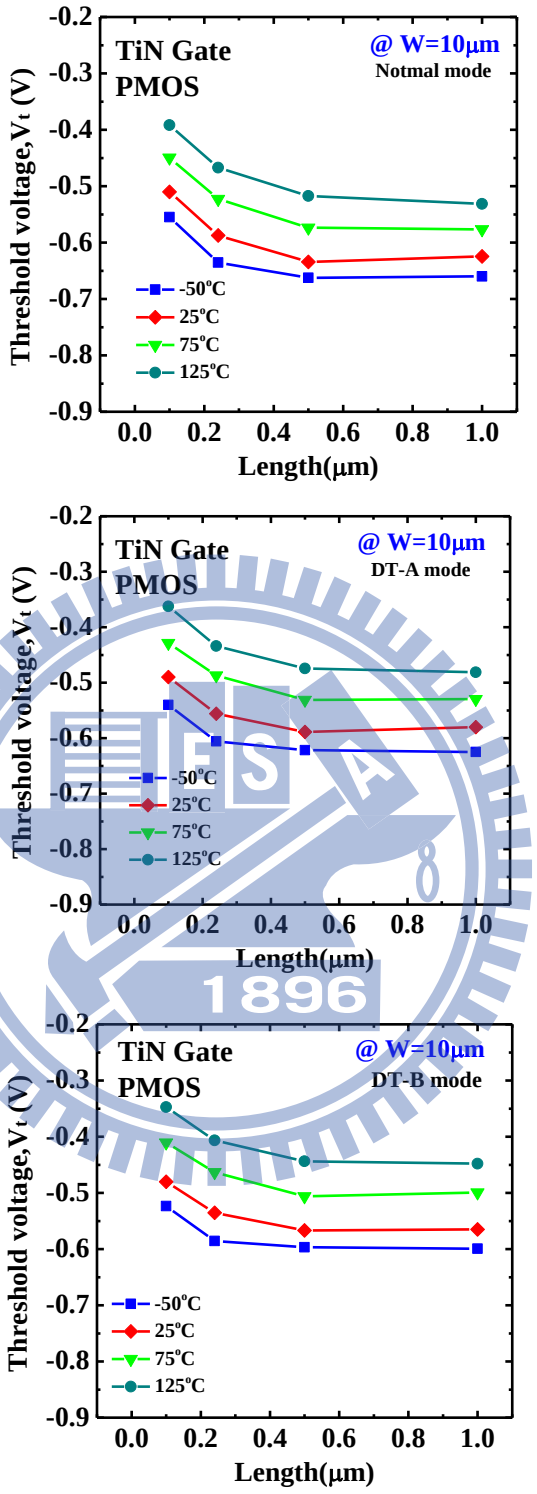


Fig. 2-20 Threshold voltage versus gate length for PMOS with TiN gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

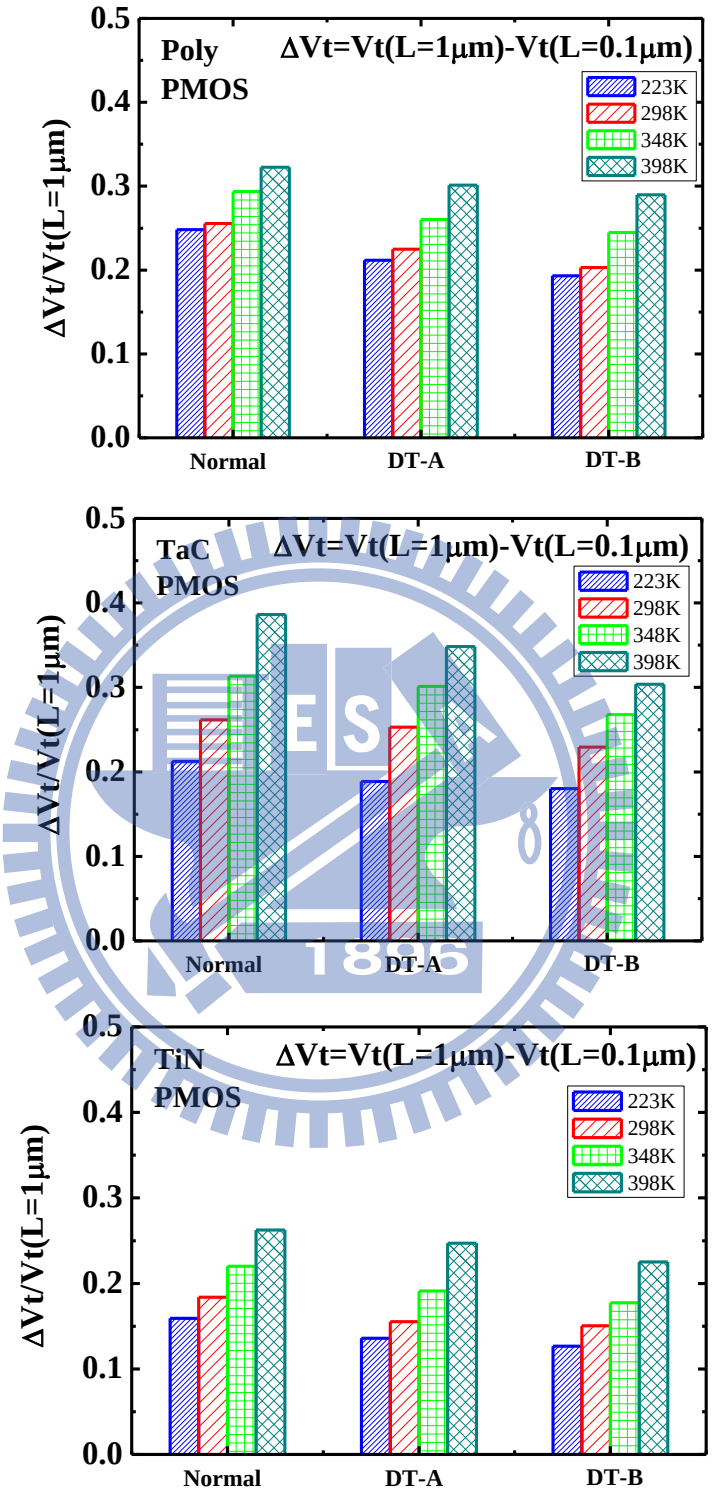


Fig. 2-21 Threshold voltage roll-off for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A, DT-B gate mode for different operation temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

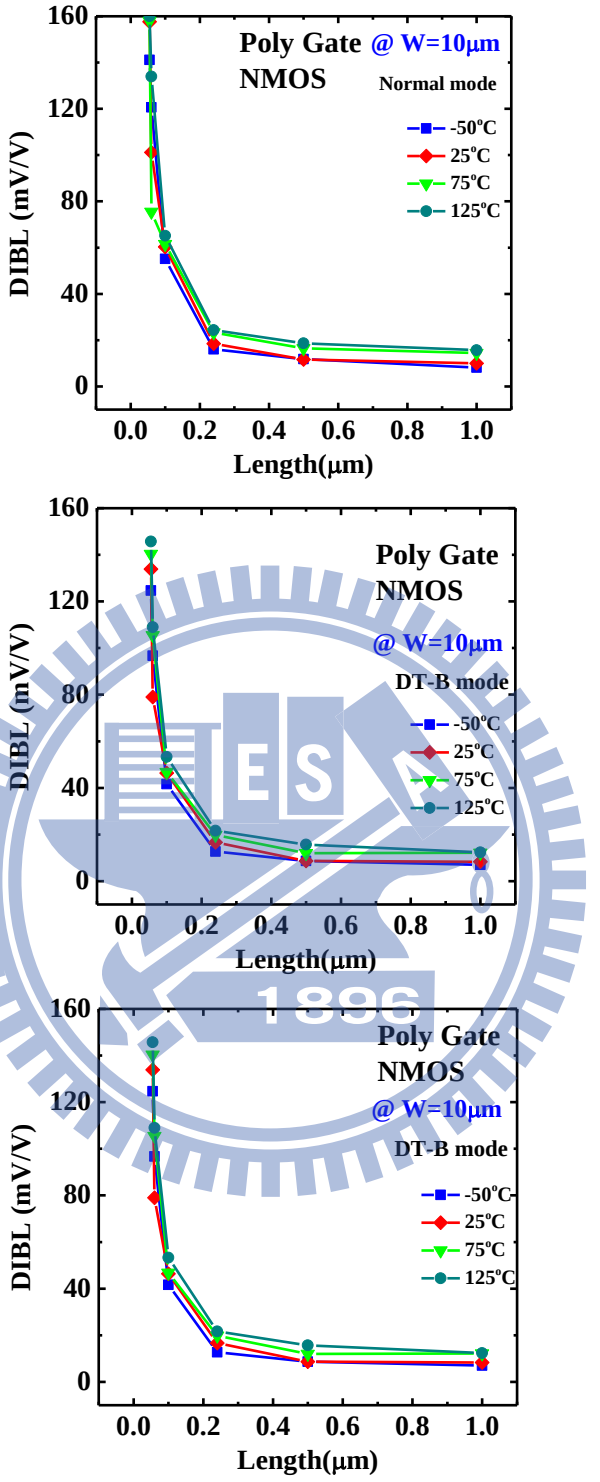


Fig. 2-22 DIBL versus gate length for NMOS with polisilicon gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

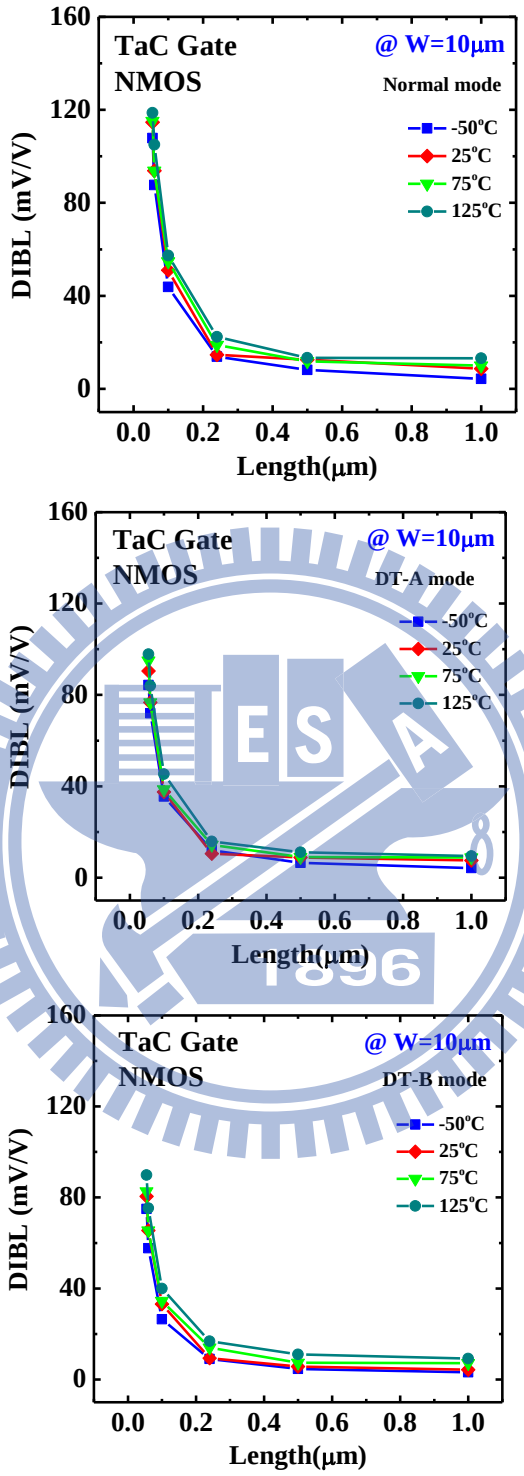


Fig. 2-23 DIBL versus gate length for NMOS with TaC gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

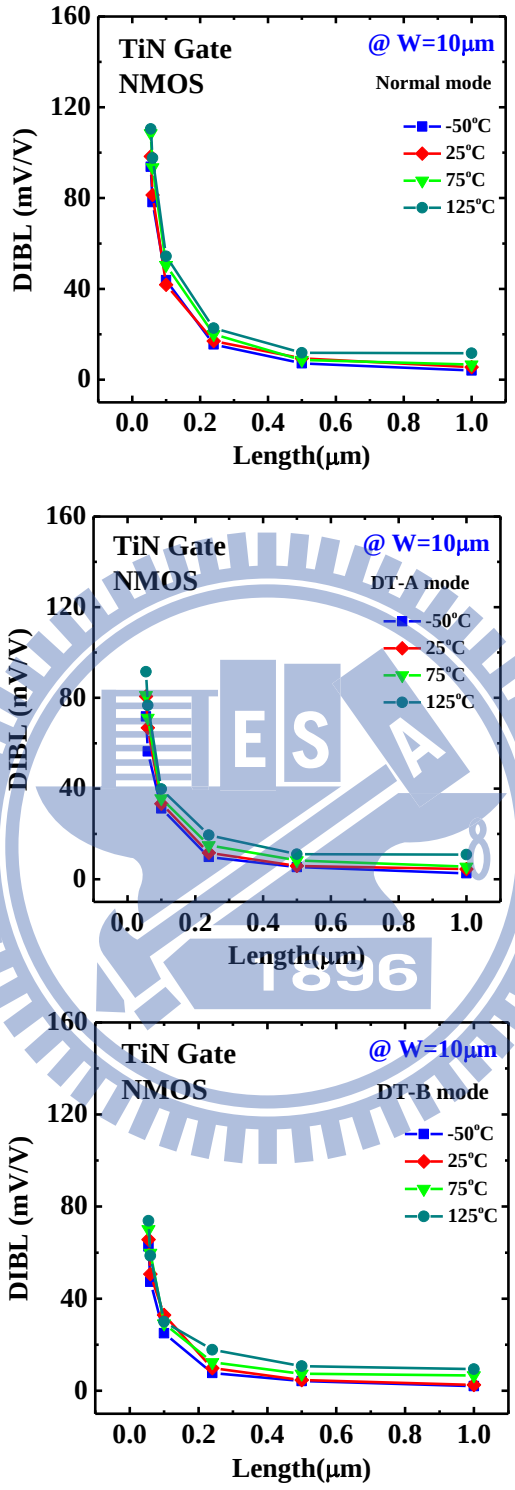
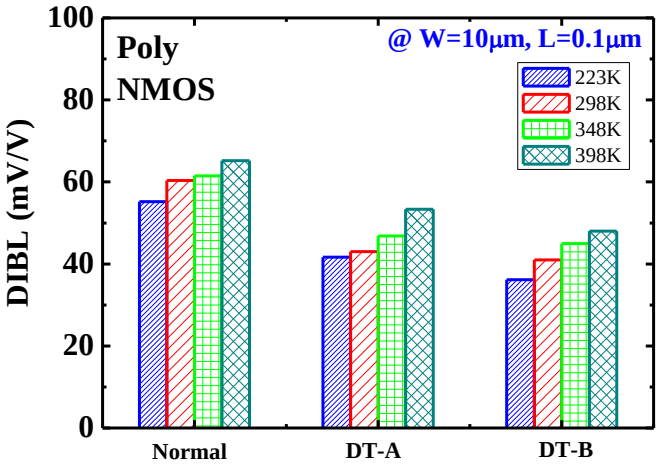


Fig. 2-24 DIBL versus gate length for NMOS with TiN gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)



(C)

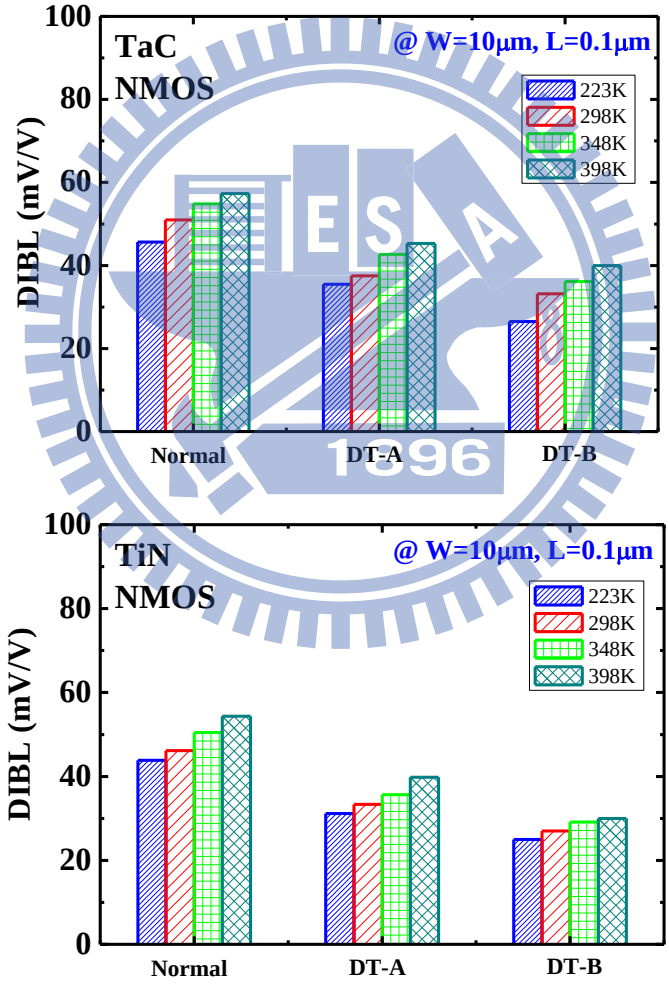


Fig. 2-25 DIBL for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A, DT-B gate mode for different operation temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

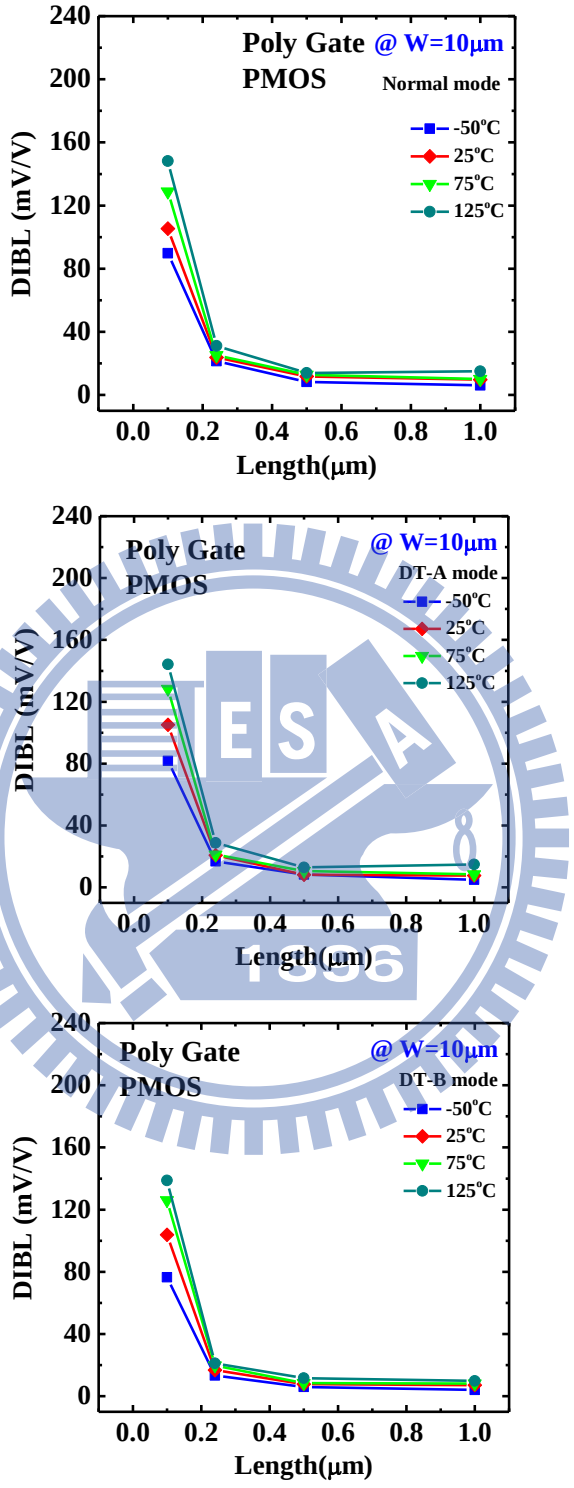


Fig. 2-26 DIBL versus gate length for PMOS with polisilicon gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

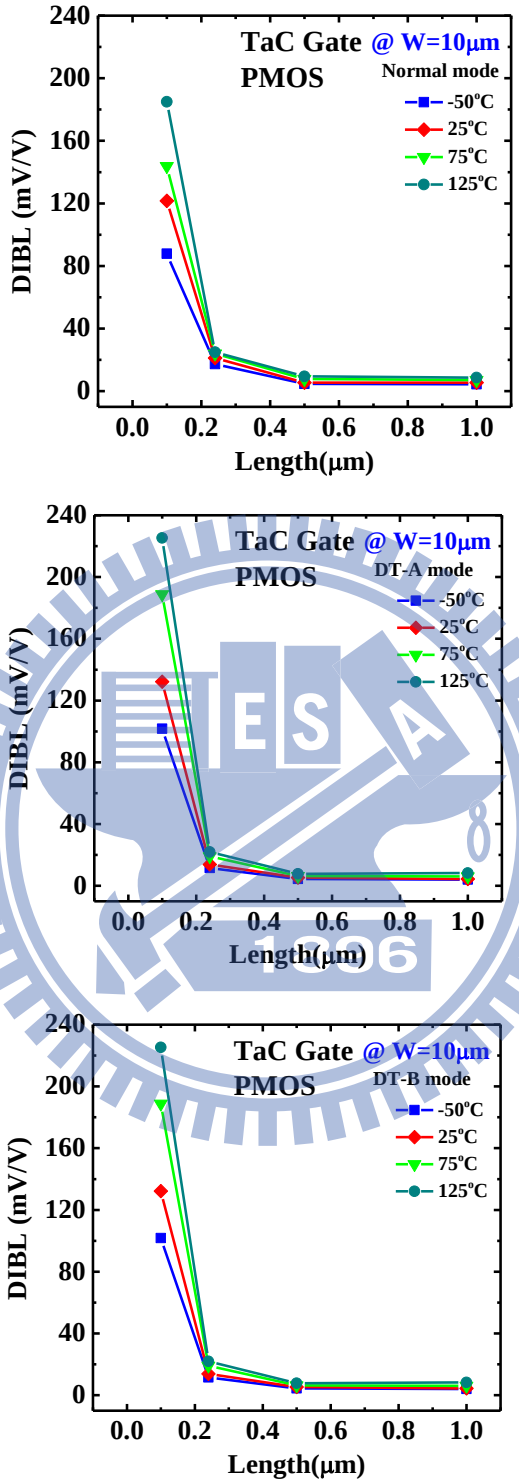
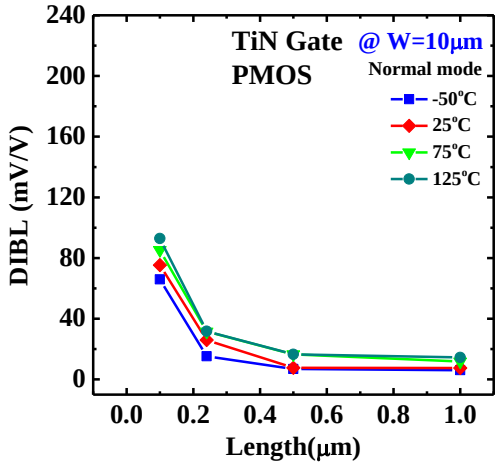


Fig. 2-27 DIBL versus gate length for PMOS with TaC gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)



(C)

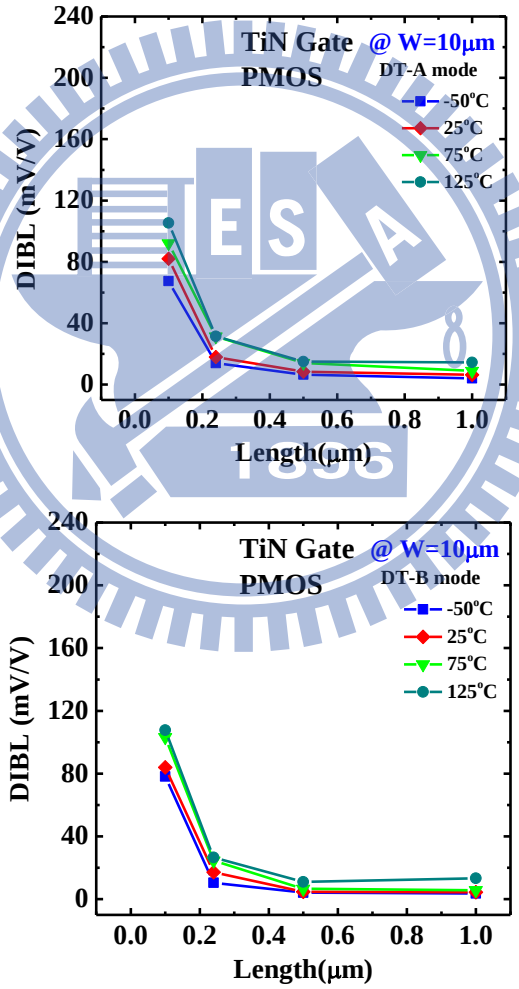


Fig. 2-28 DIBL versus gate length for PMOS with TiN gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

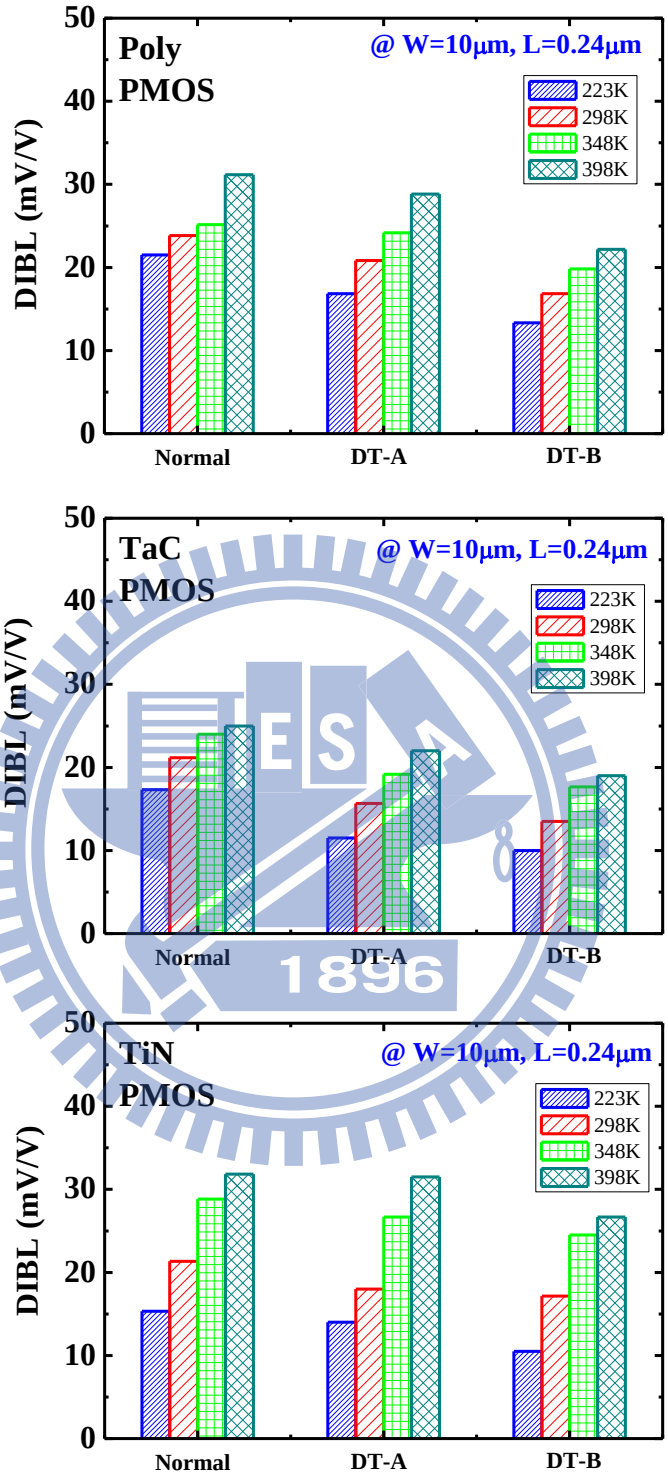


Fig. 2-29 DIBL for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A, DT-B gate mode for different operation temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

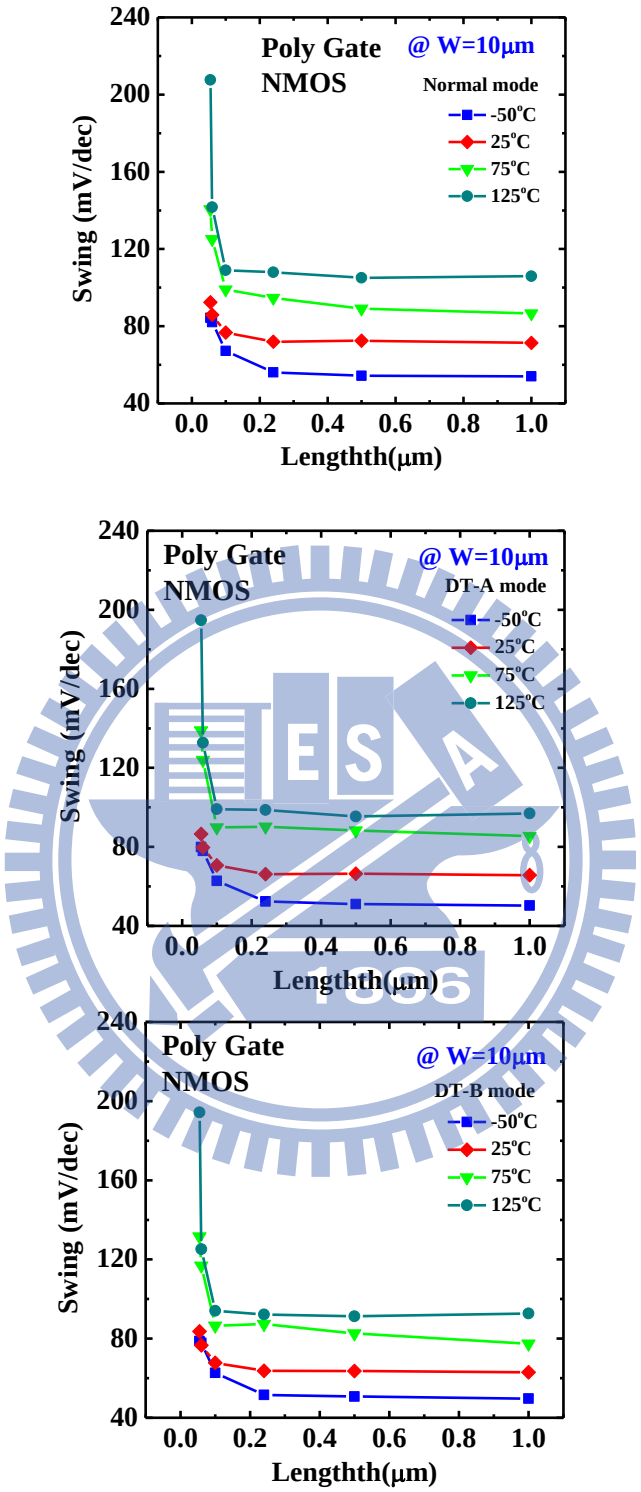


Fig. 2-30 Subthershold swing versus gate length for NMOS with polisilicon gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

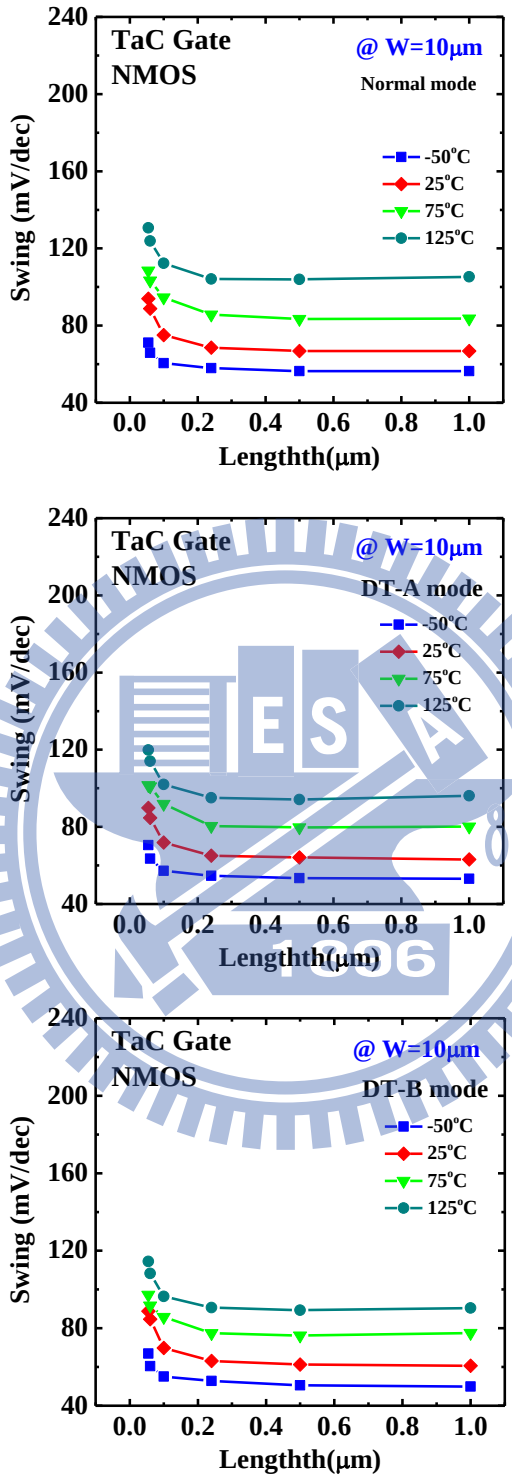


Fig. 2-31 Subthershold swing versus gate length for NMOS with TaC gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

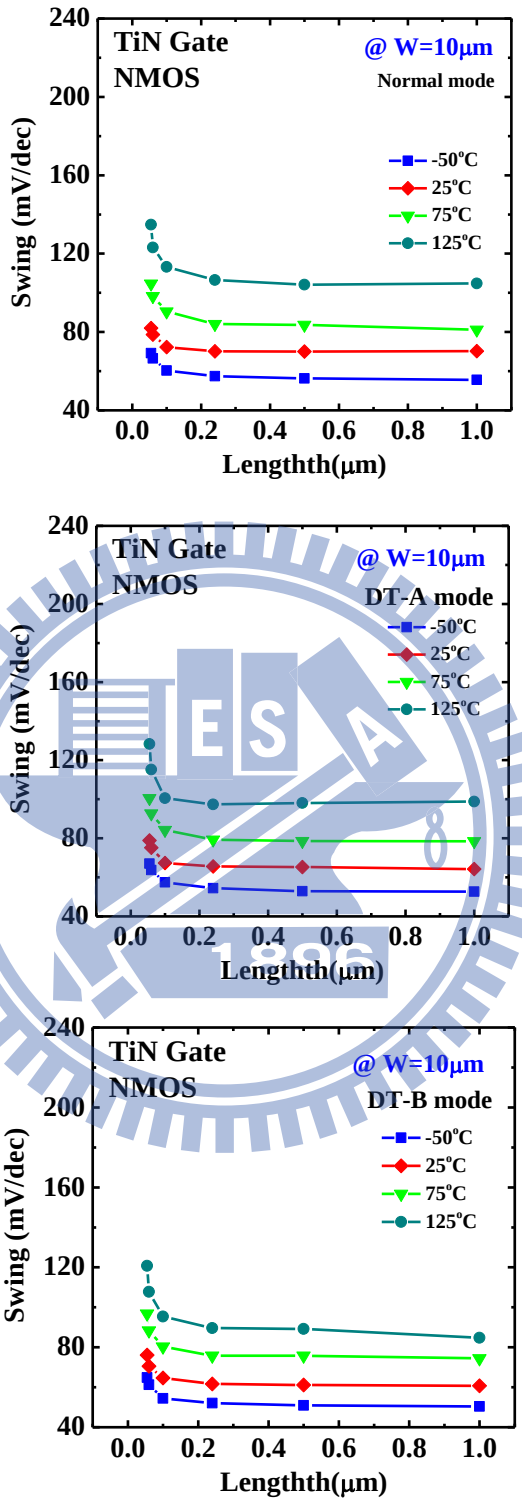


Fig. 2-32 Subthershold swing versus gate length for NMOS with TiN gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

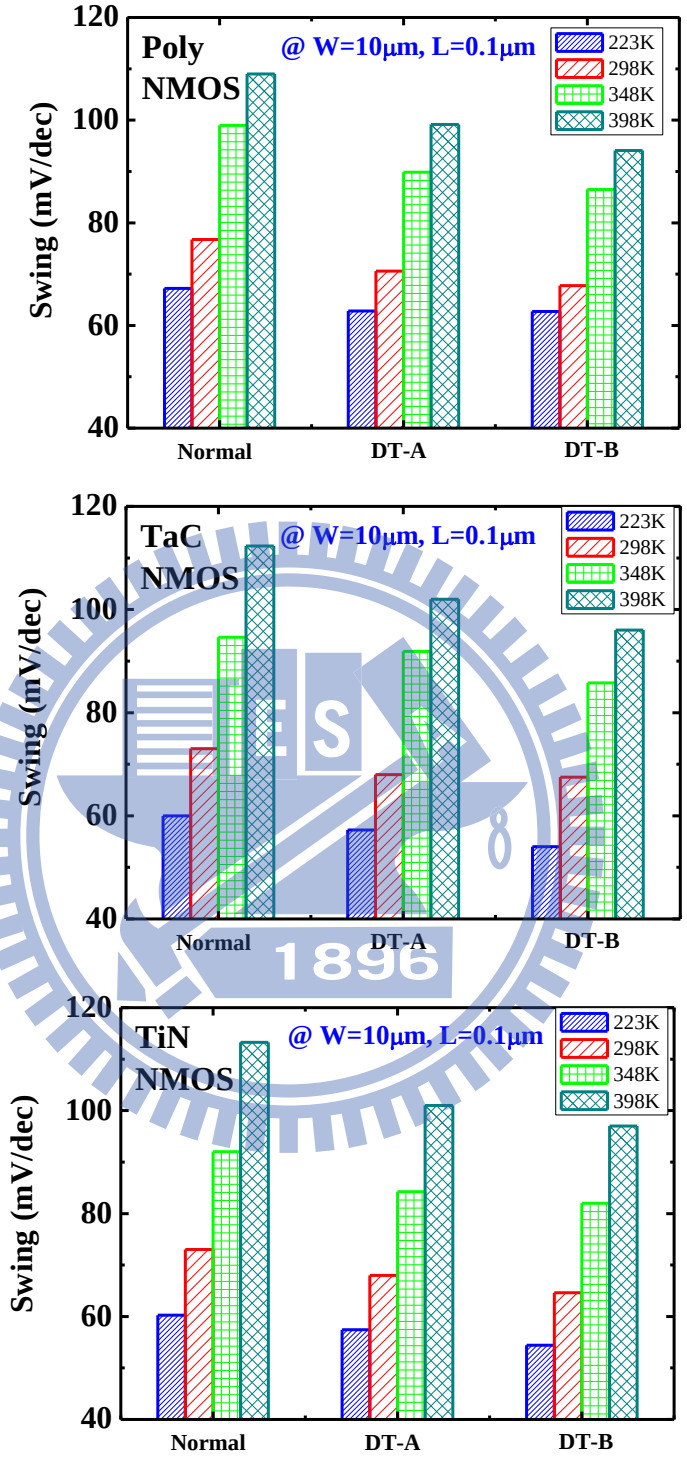


Fig. 2-33 Subthershold swing for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A, DT-B gate mode for different operation temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

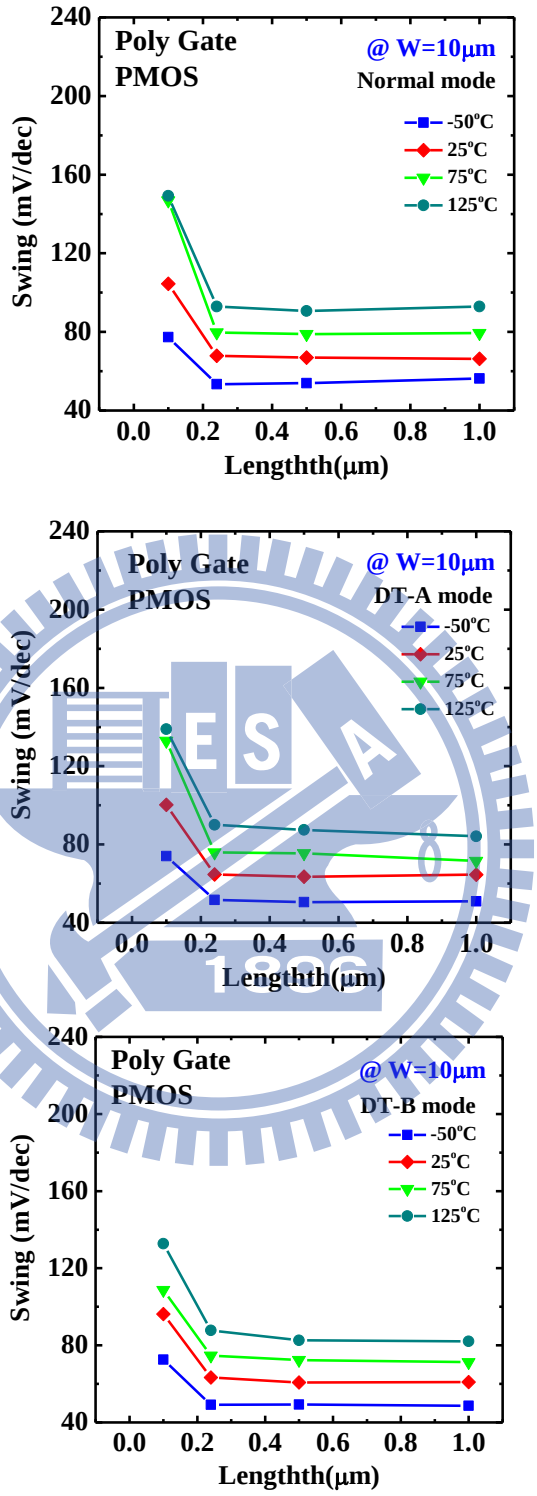
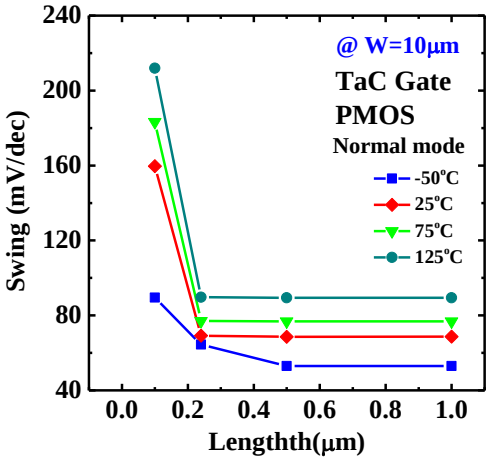


Fig. 2-34 Subthershold swing versus gate length for PMOS with polisilicon gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)



(C)

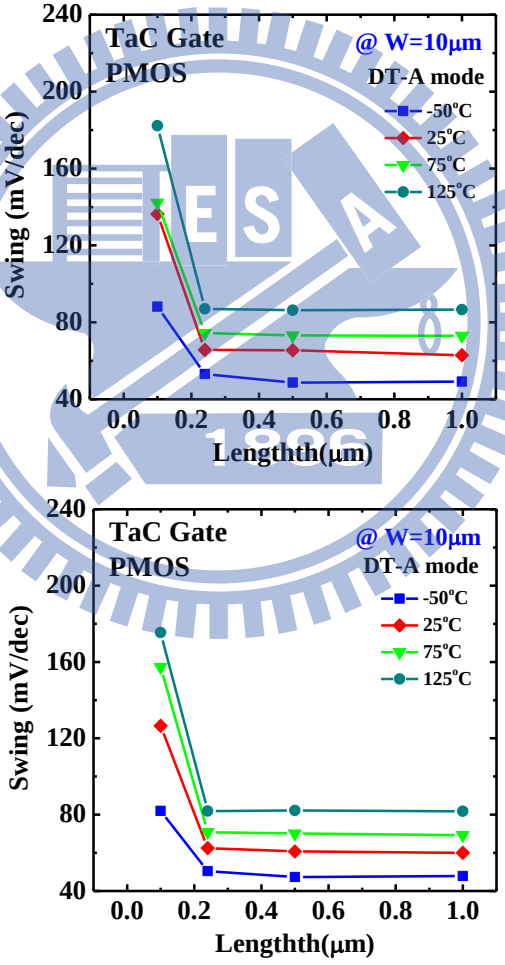


Fig. 2-35 Subthershold swing versus gate length for PMOS with TaC gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

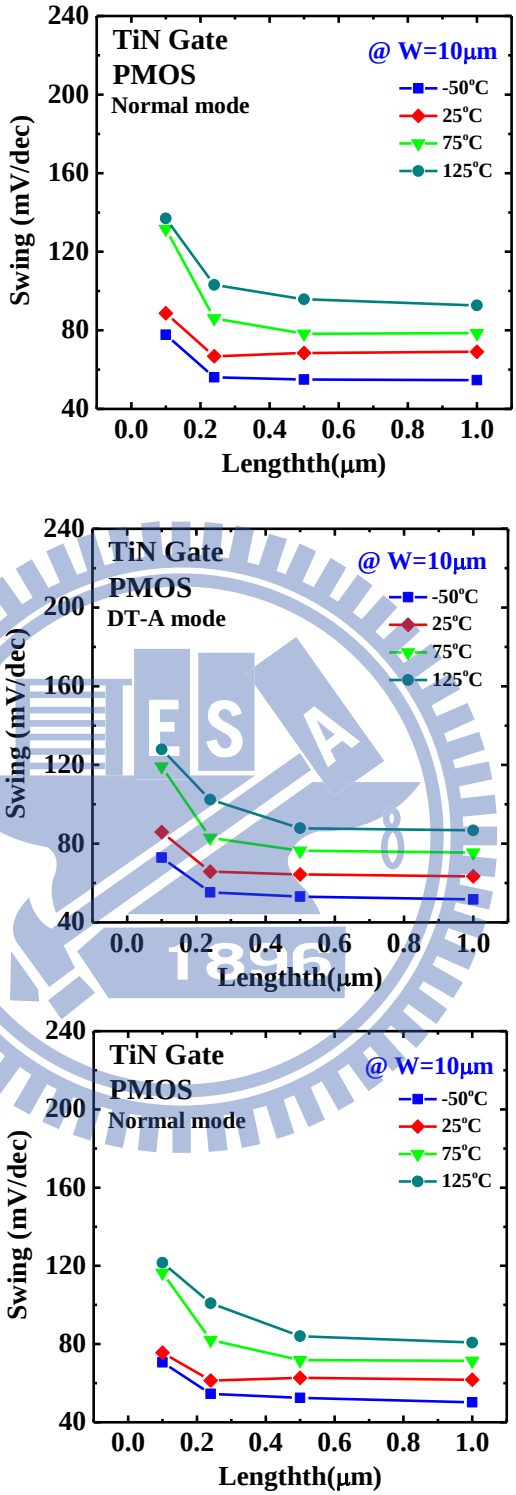


Fig. 2-36 Subthershold swing versus gate length for PMOS with TiN gate under (a) normal (b) DT-A (c) DT-B gate mode for different temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)

(b)

(C)

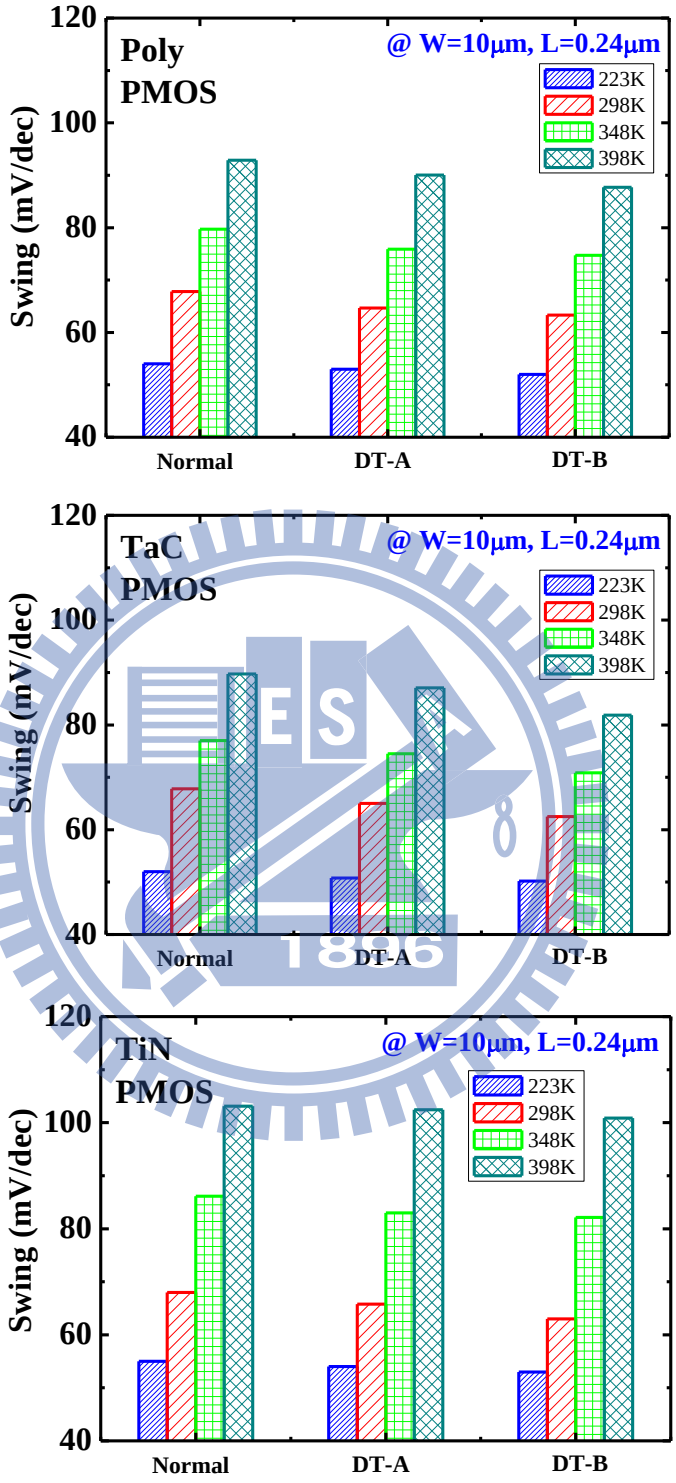
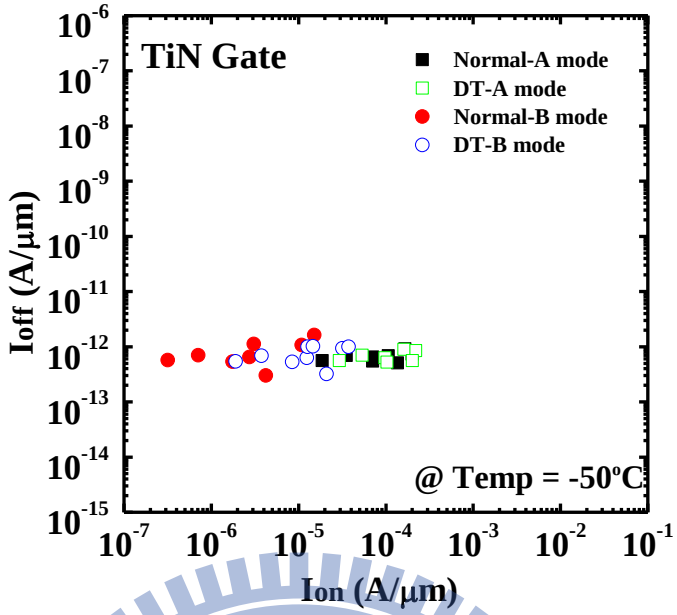


Fig. 2-37 Subthershold swing for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal, DT-A, DT-B gate mode for different operation temperatures. The operation temperatures are fixed at 223K, 298K, 348K, and 398K, respectively.

(a)



(b)

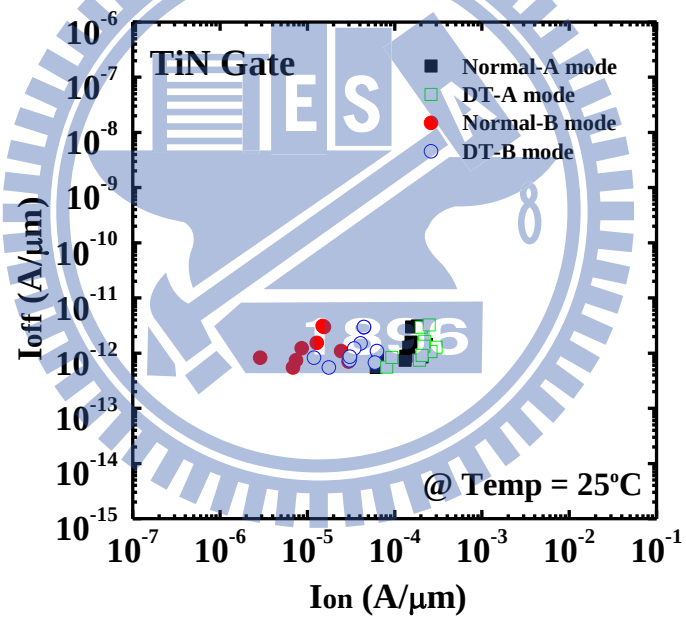
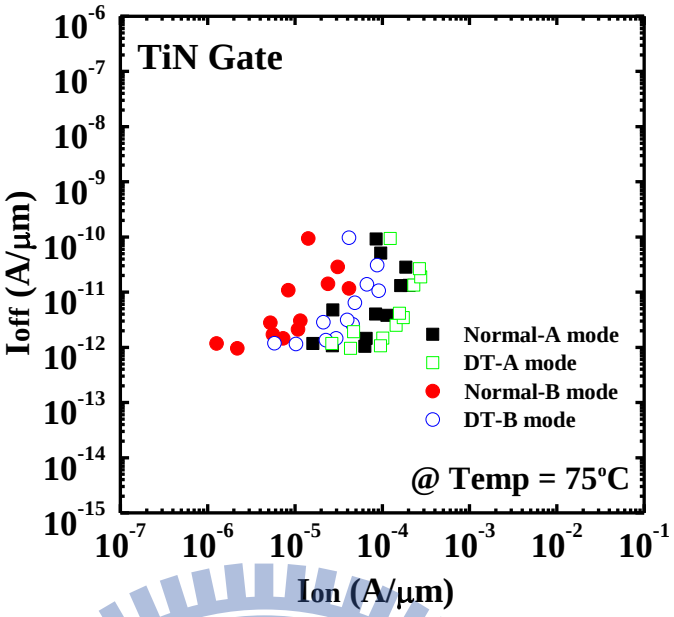


Fig. 2-38 Ion-Ioff characteristics of TiN gate NMOS at (a) 223K (b) 298K.

(c)



(d)

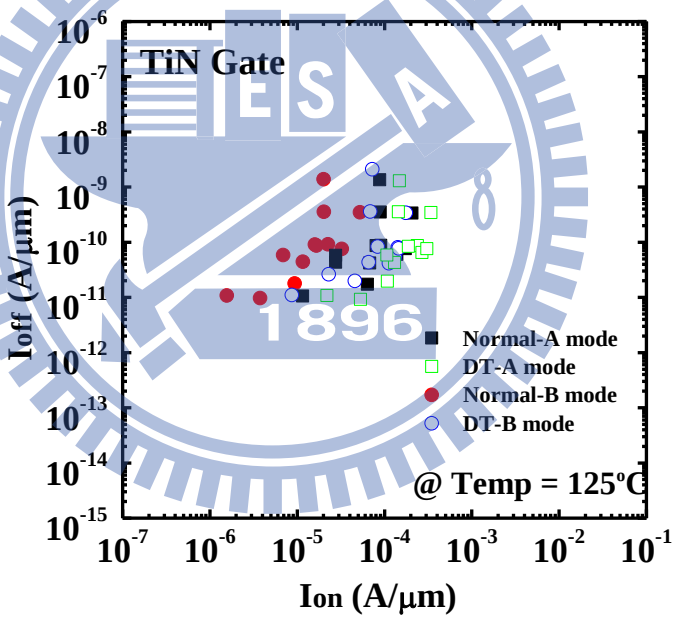
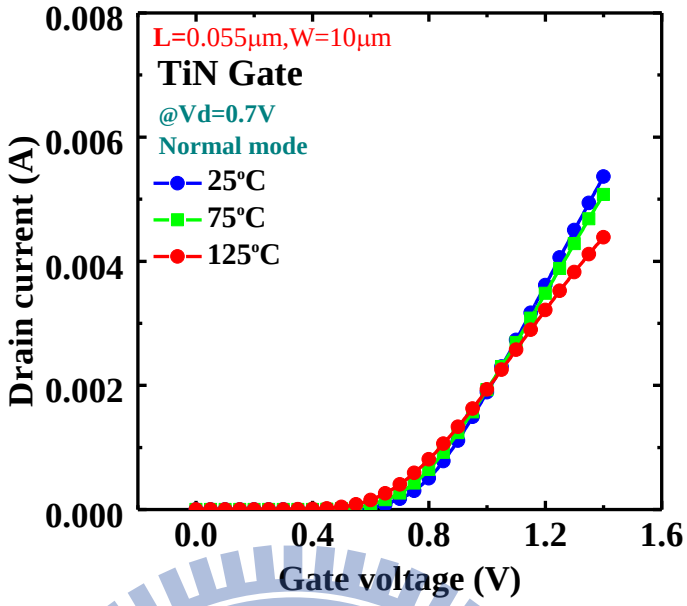


Fig. 2-38 Ion-Ioff characteristics of TiN gate NMOS at (c) 348K (d) 398K.

(a)



(b)

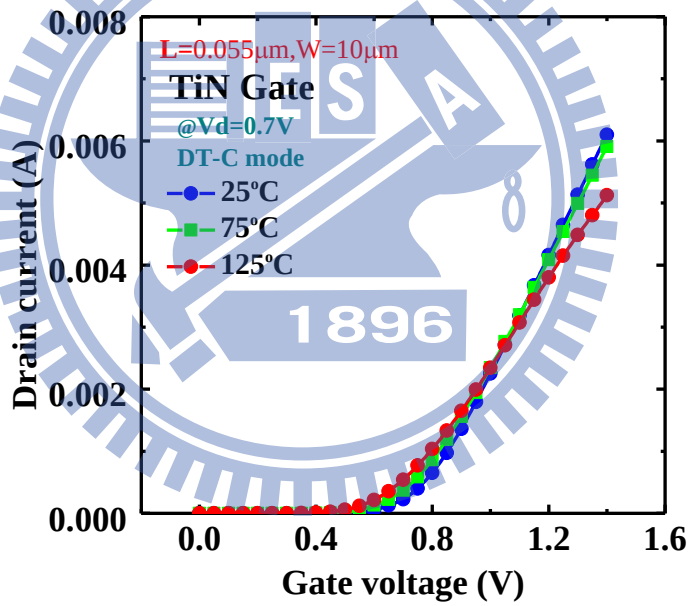
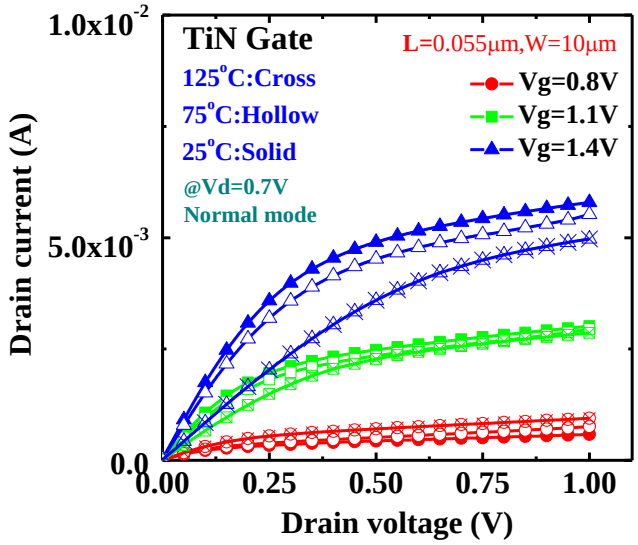


Fig. 2-39 Drain current versus gate voltage for TiN gate NMOS with different gate bias and different operation temperatures under (a) normal (b) DT-C mode. The sweep range of gate bias is from 0.8V to 1.4V, and the operation temperatures are fixed 298K, 348K, and 398K, respectively.

(a)



(b)

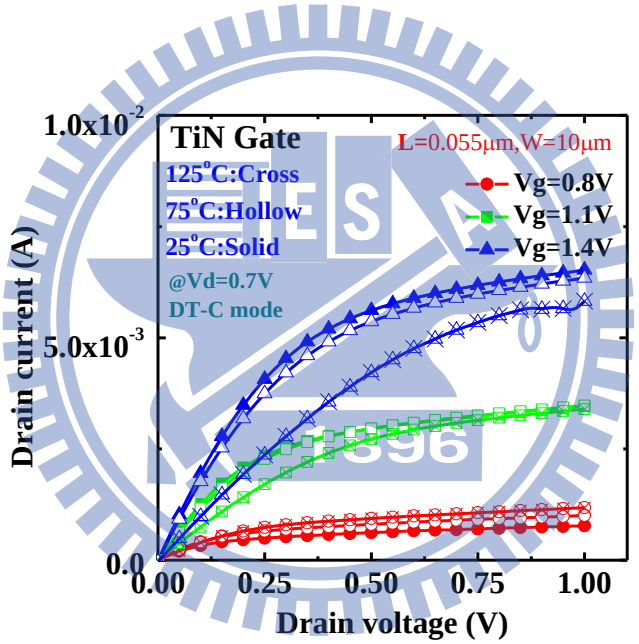


Fig. 2-40 Drain current versus drain voltage for TiN gate NMOS with different gate bias and different operation temperatures under (a) normal (b) DT-C mode. The sweep range of gate bias is from 0.8V to 1.4V, and the operation temperatures are fixed 298K, 348K, and 398K, respectively.

Chapter 3

The Compact Modeling of ZTC Point for DTMOS

3.1 Introduction

3.1.1 Backgrounds

According to the general backgrounds, recently there has been a growing interest in designing circuits that operate reliably over a widespread temperature range. It is desirable to drive circuits designed for high temperature applications at ZTC point where the drain current shows insensitive to the temperature.

The most main origin of ZTC point is because of mutual compensation of the dependences of mobility and threshold voltage on temperature in FETs. Exactly said, carrier mobility and threshold voltage both drop along with the temperature rise, and that results in the existence of ZTC point in MOS transconductance characteristics [28]. Many literatures had already confirmed the existence of ZTC point by the empirical datum, and developed the ZTC point theory from simple drain current model. With increasing the consideration factors, the error between the empirical datum and the theoretical value would reduce.

While at ZTC point, the drain current would not change along with temperature; therefore, the necessary condition of the existence of ZTC point is shown as following:

$$\frac{\partial I_d}{\partial T} = 0 \qquad \text{(eq. 3-1)}$$

We can obtain the corresponding gate bias, $V_{gs}(ZTC)$, from eq. 3-1. When $V_{gs} = V_{gs}(ZTC)$, those parameters related to temperature appearing in the drain

current theoretical formula $I_d(ZTC)$ must compensate mutually with each other, causing this dependence of $I_d(ZTC)$ on temperature to offset, and that's just the sufficient condition of the existence of ZTC point [10].

In addition, the optimal $V_{gs}(ZTC)$ is obtained by the least squares method which is minimizing the difference between the left- and the right-hand sides of the necessary condition (eq. 3-1) over a specified operating temperature range $[T_o, T_1]$ [10-15].

At first, for the bulk MOSFET, the drain current model is in direct proportion to $[V_{gs} - V_t(T)]^x$, where x=1 is in the linear region and x=2 is in the saturation region, and that expresses the ideal square-law condition. Besides, the considered parameters which depend on temperature are carrier mobility and threshold voltage variation factors; as shown as following expressions eq. 3-2 and 3-3, the assumptions are based on physical basis and experiment results:

$$\mu_n^{eff}(T) = \mu_n^{eff}(T_o)\left(\frac{T}{T_o}\right)^{-1.5} \quad \text{(eq. 3-2)}$$

and

$$V_t(T) = p_o T + q_o \quad \text{(eq. 3-3)}$$

$\mu_n^{eff}(T_o)$ is low field mobility at reference temperature T_o (=300K). The error of $V_{gs}(ZTC)$ value between the theoretical predicted result and the experimental data are $\leq 5\%$ in the linear region, and $\leq 14\%$ in the saturation region, respectively [10-11].

According to the above, we know that using simple drain current model may avoid the complex mathematical computation process, but the neglected body effect parameter δ actually causes overlooking the fact that the ZTC point in the linear region relays on the drain bias, so in order to improve the ZTC point theory, some literatures took the influence of body effect parameter, and continued using the formerly hypothesis eq. 3-3, but there was small change about carrier mobility:

$$\mu_n^{eff}(T) = \mu_n^{eff}(T_o)(\frac{T}{T_o})^{-K_1} \quad \text{(eq. 3-4)}$$

Where K_1 is extracted from the experimental results. In addition, here is also a body factor hypothesis as shown as following:

$$\delta = aT + b \quad \text{(eq. 3-5)}$$

With considering more physical parameters related with temperature, the error could reduce effectively, and it had also been verified experimentally and theoretically that the ZTC point in the linear region depends on the drain bias [14].

Moreover, the carrier mobility could further express as following:

$$\mu_s(T) = \frac{\mu_n^{eff}(T)}{1+\theta(T)[V_{gs}-V_t(T)]} \quad \text{(eq. 3-6)}$$

The parameter $\theta(T)$ specifies the degradation of the mobility with the applied transverse electric field. Unfortunately, adding this term will largely increase the complexity of mathematics [15].

In the end, recently, the literatures point out that ZTC point is often located at high gate voltage that may exceed the power supply voltage of modern circuits, and that would disturb the applications of ZTC point in a wide temperature range. One solution is biasing the body node of the device to vary the ZTC point [29].

3.1.2 Motivation

In our opinions, there are two advantages of ZTC point for the electric circuit application. One is that for design of circuits operating in a wide temperature range, the drain current is stable in the vicinity of ZTC bias point; the other is that for circuits operation at low temperature condition, once the power supply voltage

surpasses ZTC bias point, the drain current may obtain the bigger benefit than operated at higher temperature. According to above, combining the idea of ZTC point and DTMOS application perhaps could attain the improved current gain.

3.2 Measurement Setup

The gate widths of the devices used here are all 10 μm, and the corresponding gate lengths are all 1 μm. The I-V characteristics are measured by using Keithley 4200 semiconductor parameter analyzer over the operation temperature ranges from 298K to 398K. Here, we set one operation DT-mode ($\alpha = 0.4$) to discuss the ZTC point of DTMOS. For understanding the dependence of V_t on the body bias, we extract the V_t under normal mode with wide body bias ranges at each operation temperature by linear extrapolation method at $V_{ds} = 0.1V$, which is the common method to find the point of maximum slop on the I_d–V_{gs} curve by a maximum in the transconductance, and then exploit the known V_t to obtain the corresponding body bias effect δ and other parameters.

3.3 Results and Discussions

3.3.1 The Drain Current Model of DTMOS

Before inferring the ZTC point theoretical formula under DT-mode, we must determine the drain current model for DTMOS first. At present up to, there is no literature recorded DTMOS drain current theoretical equation in detail, and therefore we embark on that by ourselves from a simple equivalent circuit model. In order to simplify the mathematical results, we have to use two simple approximations, namely, gradual-channel approximation (GCA) and charge-sheet approximation [23].

Gradual-channel approximation assumes that the variation of the electric field along the channel direction is smaller far than the corresponding variation perpendicular to the channel. And, we assume that both the hole current and the generation and recombination currents are neglected. According to the assumptions, the drain-to-source current I_d maintains the same anywhere along the channel, expressed as following equation:

$$I_d = -\mu_n \frac{W}{L} \int_0^{V_{ds}} Q_n(V_C) dV_C \qquad \text{(eq. 3-7)}$$

where V_{ds} is the bias voltage between the source and drain node; $Q_n(V_C)$ is the inversion charge, and V_C is the channel bias (the bias at any point along the channel).

Charge-sheet approximation assumes that all of the inversion charges are distributed over the silicon surface like a sheet of charge, and no band bending or potential drop traverses the inversion layer, so we have the following relationships:

$$Q_n(V_C) = Q_{Si} - Q_b \qquad \text{(eq. 3-8)}$$

$$Q_{Si} = -C_{ox}\left[V_{gs} - V_{fb} - \left(2\emptyset_{fp} + V_C\right)\right] \qquad \text{(eq. 3-9)}$$

$$Q_b = -\sqrt{2q \in_{Si} N_a\left(2\emptyset_{fp} + V_C\right)} \qquad \text{(eq. 3-10)}$$

Q_{Si} is the total charge in the silicon; Q_b is the body charge, and here the channel surface potential $\emptyset_s$ is expressed as $2\emptyset_{fp} + V_C$.

For DTMOS, we make a contact between the substrate and the gate, so that the substrate node is biased. Eq. 3-7 is derived while $V_{bs} = 0V$, so we must write the drain current expressed formulor with body factor. Due to the fact that applying V_{bs} to the substrate is equivalent to dropping the voltages of all the other nodes by V_{bs} in

the device, as shown in Fig. 3-1, Eq. 3-7, 3-8, and 3-9 could be modified to become the new following equations:

$$Q_{Si} = -C_{ox}\left[V_{gs} - V_{bs} - V_{fb} - \left(2\emptyset_{fp} + V_C\right)\right] \quad \text{(eq. 3-11)}$$

$$Q_n(V_C) = -C_{ox}\left[V_{gs} - V_{bs} - V_{fb} - \left(2\emptyset_{fp} + V_C\right)\right] + \sqrt{2q \in_{Si} N_a\left(2\emptyset_{fp} + V_C\right)} \quad \text{(eq. 3-12)}$$

$$I_d = -\mu_n \frac{W}{L}\int_{-V_{bs}}^{V_{ds}-V_{bs}} Q_n(V_C)dV_C \quad \text{(eq. 3-13)}$$

And then eq. 3-13 becomes:

$$\mu_n \frac{W}{L}\int_{-V_{bs}}^{V_{ds}-V_{bs}} \{C_{ox}\left[V_{gs} - V_{bs} - V_{fb} - \left(2\emptyset_{fp} + V_C\right)\right] - \sqrt{2q \in_{Si} N_a\left(2\emptyset_{fp} + V_C\right)}\}\, dV_C$$
$$= \mu_n C_{ox}\frac{W}{L}\{(V_{gs} - V_{fb} - 2\emptyset_{fp} - \frac{V_{ds}}{2})V_{ds} - \frac{2\sqrt{2q\in_{Si}N_a}}{3C_{ox}}\left[\left(2\emptyset_{fp} + V_{ds} - V_{bs}\right)^{\frac{3}{2}} + \left(2\emptyset_{fp} - V_{bs}\right)^{\frac{3}{2}}\right]\} \quad \text{(eq. 3-14)}$$

We expand the complex mathematics expression in the second medium parentheses into a power series in V_{ds} and take to the second-order terms as shown as eq. 3-15. Now I_{ds} would follow a parabolic curve before saturation. By the way, some literatures have proved that there is a good approximation between the two $I_{ds} - V_{ds}$ curves calculated respectively from the full equation and parabolic approximation [23].

$$\left(2\emptyset_{fp} + V_{ds} - V_{bs}\right)^{\frac{3}{2}} + \left(2\emptyset_{fp} - V_{bs}\right)^{\frac{3}{2}} = \frac{3}{2}\sqrt{2\emptyset_{fp} - V_{bs}}V_{ds} + \frac{3}{8}\frac{1}{\sqrt{2\emptyset_{fp} - V_{bs}}}{V_{ds}}^2 \quad \text{(eq. 3-15)}$$

Then the drain current becomes:

$$I_d = \mu_n C_{ox} \frac{W}{L}\{\left[V_{gs} - V_{fb} - 2\emptyset_{fp} - \frac{1}{C_{ox}}\sqrt{2q \in_{Si} N_a(2\emptyset_{fp} - V_{bs})}\right]V_{ds} - \frac{1}{2}\left[1 + \frac{1}{C_{ox}}\sqrt{\frac{q \in_{Si} N_a}{2(2\emptyset_{fp} - V_{bs})}}\right]{V_{ds}}^2\}$$

$$= \mu_n C_{ox} \frac{W}{L}\{[V_{gs} - V_t(V_{bs})]V_{ds} - \frac{1}{2}m{V_{ds}}^2\} \quad \text{(eq. 3-16)}$$

Now, here presents many parameters related to V_{bs}:

$$V_t(V_{bs}) = V_{fb} + 2\emptyset_{fp} + \frac{\sqrt{2q\in_{Si}N_a(2\emptyset_{fp} - V_{bs})}}{C_{ox}} \quad \text{(eq. 3-17)}$$

$$m = 1 + \frac{\sqrt{q\in_{Si}N_a/2(2\emptyset_{fp} - V_{bs})}}{C_{ox}} = 1 + \frac{\partial V_t(V_{bs})}{\partial V_{sb}} = 1 + \delta \quad \text{(eq. 3-18)}$$

In addition, once the V_{ds} beyond saturation voltage, I_{ds} stays constant, independent of V_{ds}. A general form of the saturation voltage is obtained by solving the following eq. 3-19:

$$\frac{dI_{ds}}{dV_{ds}} = 0 \quad \text{(eq. 3-19)}$$

that is equivalent to letting $Q_n = 0$ at the drain node:

$$Q_n|_{drain} = -C_{ox}\left[V_{gs} - V_{bs} - V_{fb} - (2\emptyset_{fp} + V_{ds} - V_{bs})\right] + \sqrt{2q \in_{Si} N_a(2\emptyset_{fp} + V_{ds} - V_{bs})} \quad \text{(eq. 3-20)}$$

We expand $\sqrt{2q \in_{Si} N_a(2\emptyset_{fp} + V_{ds} - V_{bs})}$ into a power series in V_{ds} and take to the first-order terms, and then eq. 3-20 becomes:

$$C_{ox}\left[V_{gs} - V_t(V_{bs}) - mV_{ds}\right] = 0 \quad \text{(eq. 3-21)}$$

Then we get the saturation voltage and saturation current theoretical model under ideal square condition:

$$V_{ds}^{sat} = \frac{V_{gs} - V_t(V_{bs})}{m} \quad \text{(eq. 3-22)}$$

$$I_d^{sat} = \mu_n C_{ox} \frac{W}{L} \frac{[V_{gs} - V_t(V_{bs})]^2}{2m} \quad \text{(eq. 3-23)}$$

If $2\emptyset_{fp} - V_{bs} < 0$, then $Q_b = 0$ and $Q_{Si} = Q_n(V_C)$. eq. 3-20 becomes:

$$Q_n(V_C) = -C_{ox}\left[V_{gs} - V_{bs} - V_{fb} - \left(2\emptyset_{fp} + V_C\right)\right] \quad \text{(eq. 3-24)}$$

Now eq. 3-14 becomes simpler as following:

$$I_d = -\mu_n \frac{W}{L} \int_{-V_{bs}}^{V_{ds}-V_{bs}} Q_n(V_C) dV_C$$

$$= \mu_n \frac{W}{L} \int_{-V_{bs}}^{V_{ds}-V_{bs}} C_{ox}\left[V_{gs} - V_{bs} - V_{fb} - \left(2\emptyset_{fp} + V_C\right)\right] dV_C$$

$$= \mu_n \frac{W}{L} C_{ox}\left[\left(V_{gs} - V_{fb} - 2\emptyset_{fp}\right)V_{ds} - \frac{1}{2}{V_{ds}}^2\right]$$

$$= \mu_n \frac{W}{L} C_{ox}\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{1}{2}{V_{ds}}^2\right] \quad \text{(eq. 3-25)}$$

$$V_t = V_{fb} + 2\emptyset_{fp} \quad \text{(eq. 3-26)}$$

Eq. 3-25 will be the drain current in the linear region, and V_t is shown in eq. 3-26; on the other hand, in the saturation region, now $m = 1$ and eq. 3-23 becomes eq 3-27 as following,

$$I_d^{sat} = \mu_n C_{ox} \frac{W}{L} \frac{[V_{gs} - V_t]^2}{2} \quad \text{(eq. 3-27)}$$

In this thesis, we only discuss the operation region with $2\emptyset_{fp} - V_{bs} > 0$ as shown

in Table 3-1, which only show the parameters of NMOS with polysilicon gate for representative.

3.3.2 The ZTC Point Model of DTMOS

We'd haven the drain current model for DTMOS, and then could start to calculate its ZTC point theoretical formula. Following those experiences of predecessors, for obtaining simple mathematical results, we must make some suppositions of these parameters related to temperature and body bias.

Just like the beforehand literatures, no matters how threshold voltage is defined, it could be expressed as approximately a first-order polynomial dependent on temperature. Moreover, the influence of V_{bs} on $\frac{\partial V_t(T,V_{bs})}{\partial T}$ is negligible, but distinct on the value shift of $V_t(T,V_{bs})$, so we part the dependence of $V_t(T,V_{bs})$ on V_{bs} from temperature, and also take to first-order polynomial dependence on V_{bs} for convenience as following [29].

$$V_t(V_{bs}) = p_o T + q_o + r_o V_{bs} = p_o T + q_o + r_o \alpha V_{gs} \qquad \text{(eq. 3-28)}$$

The body effect parameter δ is an important factor which urges that the dependence exists between V_{ds} and the ZTC point in the linear region. And, we have discussed the δ effects on the device characteristics in the chapter 2. In addition, according to our experimental results, the variation of δ with elevated temperature could still be expressed as eq. 3-5 as following.

$$\delta = aT + b \qquad \text{(eq. 3-5)}$$

Now, let us consider the temperature dependence of mobility. Here we do not consider the factor $\theta(T)$ in eq. 3-6 for two reasons: for the first, the ZTC point bias is

too small to go through the enhanced surface roughness scattering. For the second, $\theta(T)$ will cause the ZTC point mathematical equation to become so complex that we are unable to resolve it. As a result, the mobility degradation factor of K_1 with elevated temperature could still be expressed as eq. 3-4.

$$\mu_n^{eff}(T) = \mu_n^{eff}(T_o)(\frac{T}{T_o})^{-K_1} \quad \text{(eq. 3-4)}$$

For the parameter of K_1, it would change along with scattering mechanism; when phonon scattering mechanism is dominant, the temperature dependence is remarkable; yet, there are other scattering mechanisms as well, so the value of K_1 relays on experimental results with different operation conditions [28].

In addition, to increase the accuracy, we need to correct the square term under the saturation mode:

$$I_d^{sat} \propto [V_{gs} - V_t(V_{bs})]^x \quad \text{(eq. 3-29)}$$

In those reference papers, the value x equals 2, corresponding to the ideal square law. Nevertheless, the saturation theoretical value, $V_{gs}^{sat}(ZTC)$, always brings about quite notable error ($> 10\%$); therefore we estimate the actual power dependence of I_d^{sat} on $[V_{gs} - V_t(V_{bs})]$ from the experiment data in behalf of lowing the error [11].

After explaining all parameter assumptions, we start to calculate the theoretical value of $V_{gs}(ZTC)$ from the necessary condition eq. 3-1. We start from the linear mode first and repeat the needed equations for convenience:

$$I_d^{lin} = \mu_n C_{ox} \frac{W}{L}\{[V_{gs} - V_t(V_{bs})]V_{ds} - \frac{1}{2}mV_{ds}^2\} \quad \text{(eq. 3-16)}$$

$$\frac{\partial I_d^{lin}}{\partial T} = 0 \quad \text{(eq. 3-1)}$$

By substituting eq. 3-16 to eq. 3-1, we get the following statement:

$$V_{gs}^{lin}(ZTC) - V_t(V_{bs}) = -\frac{T}{K_1}\left[\frac{\partial V_t(V_{bs})}{\partial T} + \frac{V_{ds}}{2}\frac{\partial \delta}{\partial T}\right] + \frac{V_{ds}}{2}(1+\delta) \quad \text{(eq. 3-30)}$$

With using the least squares method, we minimize the difference between the left- and the right-hand sides of eq.3-30 over a temperature range $[T_o, T_1]$ as following:

$$\frac{\partial}{\partial V_{gs}}\int_{T_o}^{T_1}\{V_{gs}^{lin}(ZTC) - V_t(V_{bs}) + \frac{T}{K_1}\left[\frac{\partial V_t(V_{bs})}{\partial T} + \frac{V_{ds}}{2}\frac{\partial \delta}{\partial T}\right] - \frac{V_{ds}}{2}(1+\delta)\}^2 dT = 0 \quad \text{(eq. 3-31)}$$

We replace those theoretical parameters by the parameter supposition and rewrite eq. 3-31:

$$\frac{\partial}{\partial V_{gs}}\int_{T_o}^{T_1}\{V_{gs}^{lin}(ZTC) - [p_o T + q_o + r_o \alpha V_{gs}^{lin}(ZTC)] + \frac{T}{K_1}(p_o + \frac{V_{ds}}{2}a) - \frac{V_{ds}}{2}(1 + aT + b)\}2dT = 0 \quad \text{(eq. 3-32)}$$

Because V_{gs} and T are independent, we can make differential first and then integral. It becomes:

$$2(1-\alpha r_o)\int_{T_o}^{T_1}\{V_{gs}^{lin}(ZTC)(1-\alpha r_o) - q_o - \frac{V_{ds}}{2}(1+b) + [-p_{o+}\frac{1}{K_1}(p_o + \frac{V_{ds}}{2}a) - \frac{V_{ds}}{2}a]T\}dT = 0 \quad \text{(eq. 3-33)}$$

After making integral, it becomes:

$$[V_{gs}^{lin}(ZTC)(1-\alpha r_o) - q_o - \frac{V_{ds}}{2}(1+b)](T_1 - T_o) + \frac{1}{2}\left(\frac{1}{K_1} - 1\right)(p_o + \frac{V_{ds}}{2}a)(T_1 - T_o)(T_1 + T_o) = 0 \quad \text{(eq. 3-34)}$$

It is easy to show that the solution is given as following:

$$V_{gs}^{lin}(ZTC) = \frac{-\frac{1}{2}\left(\frac{1}{K_1}-1\right)\left(p_o+\frac{V_{ds}}{2}a\right)(T_1+T_o)+q_o+\frac{V_{ds}}{2}(1+b)}{(1-\alpha r_o)} \quad \text{(eq. 3-35)}$$

Repeating the above steps, we substitute eq. 3-23 to eq. 3-1 and obtain the following results for saturation mode:

$$V_{gs}^{sat}(ZTC) - V_t(V_{bs}) = \frac{-xT(1+\delta)\frac{\partial V_t(V_{bs})}{\partial T}}{K_1(1+\delta)+T\frac{\partial \delta}{\partial T}} \quad \text{(eq. 3-36)}$$

Then use the least squares method again:

$$\frac{\partial}{\partial V_{gs}}\int_{T_o}^{T_1}\left[V_{gs}^{sat}(ZTC) - V_t(V_{bs}) + \frac{xT(1+\delta)\frac{\partial V_t(V_{bs})}{\partial T}}{K_1(1+\delta)+T\frac{\partial \delta}{\partial T}}\right]^2 dT$$

$$= \frac{\partial}{\partial V_{gs}}\int_{T_o}^{T_1}\left\{V_{gs}^{sat}(ZTC) - [p_oT+q_o+r_o\alpha V_{gs}^{sat}(ZTC)] + \frac{xT(1+aT+b)p_o}{K_1(1+aT+b)+aT}\right\}^2 dT$$

$$= 2(1-\alpha r_o)\int_{T_o}^{T_1}\left\{V_{gs}^{sat}(ZTC) - [p_oT+q_o+r_o\alpha V_{gs}^{sat}(ZTC)] + \frac{xT(1+aT+b)p_o}{K_1(1+aT+b)+aT}\right\} dT = 0$$

(eq. 3-37)

We do differential first and then integral:

$$[V_{gs}^{sat}(ZTC)(1-\alpha r_o) - q_o + \frac{xp_o(1+b)}{a(1+K_1)^2}](T_1-T_o) +$$

$$\left[-\frac{p_o}{2}+\frac{xp_o}{2(1+K_1)}\right](T_1-T_o)(T_1+T_o) - \frac{xp_oT_z{}^2}{K_1(1+K_1)(T_1-T_o)}\ln\frac{T_1+T_z}{T_o+T_z} = 0 \quad \text{(eq. 3-38)}$$

The only one additional assumption is:

$$T_z = \frac{K_1(1+b)}{(1+K_1)a} \quad \text{(eq. 3-39)}$$

The ZTC point in saturation region is as following:

$$V_{gs}^{sat}(ZTC) = \frac{p_o\left[\frac{1}{2}-\frac{x}{2(1+K_1)}\right](T_1+T_o)+q_o-\frac{xp_oT_z}{K_1(1+K_1)}\left(1-\frac{T_z}{T_1-T_o}\right)\ln\frac{T_1+T_z}{T_o+T_z}}{(1-\alpha r_o)} \quad \text{(eq. 3-40)}$$

Besides, there is another method to acquire DTMOS ZTC point theoretical formula. First, we calculate the ZTC point theoretical formula under a fixed body bias, and then take the intersection point between the resulted formula and eq. 2-2, $V_{bs} = \alpha V_{gs}$, and that would be the DTMOS ZTC point.

We begin from the same statement. At first there would be the same results under the linear mode, such as eq. 3-30 and 3-31. Now something different occurs. The term $r_o V_{bs}$ in eq. 3-28 would not equal $r_o \alpha V_{gs}$ anymore, so that changes the differential result as follow:

$$\frac{\partial}{\partial V_{gs}} \int_{T_o}^{T_1} [V_{gs}^{lin}(ZTC) - (p_o T + q_o + r_o V_{bs}) + \frac{T}{K_1}(p_o + \frac{V_{ds}}{2} a) - \frac{V_{ds}}{2}(1 + aT + b)]^2 dT$$

$$= 2 \int_{T_o}^{T_1} [V_{gs}^{lin}(ZTC) - (p_o T + q_o + r_o V_{bs}) + \frac{T}{K_1}(p_o + \frac{V_{ds}}{2} a) - \frac{V_{ds}}{2}(1 + aT + b)] dT$$

$$= 0 \qquad \text{(eq. 3-41)}$$

and then:

$$[V_{gs}^{lin}(ZTC) - q_o - r_o V_{bs} - \frac{V_{ds}}{2}(1 + b)](T_1 - T_o) +$$

$$\frac{1}{2}\left(\frac{1}{K_1} - 1\right)(p_o + \frac{V_{ds}}{2} a)(T_1 - T_o)(T_1 + T_o) = 0 \qquad \text{(eq. 3-42)}$$

The solution for normal mode in the linear region at a fixed body bias is:

$$V_{gs}^{lin}(ZTC) = -\frac{1}{2}\left(\frac{1}{K_1} - 1\right)(p_o + \frac{V_{ds}}{2} a)(T_1 + T_o) + q_o + r_o V_{bs} + \frac{V_{ds}}{2}(1 + b) \qquad \text{(eq. 3-43)}$$

If $V_{bs} = \alpha V_{gs}$, it returns back to eq. 3-35, the solution of the theoretical ZTC point for DTMOS from the regular method in the linear region.

Similarly, the different part also occurs in nonlinear region, eq. 3-37 becomes:

$$\frac{\partial}{\partial V_{gs}}\int_{T_o}^{T_1}[V_{gs}^{sat}(ZTC)-V_t(V_{bs})+\frac{xT(1+\delta)\frac{\partial V_t(V_{bs})}{\partial T}}{K_1(1+\delta)+T\frac{\partial \delta}{\partial T}}]^2dT$$

$$=\frac{\partial}{\partial V_{gs}}\int_{T_o}^{T_1}[V_{gs}^{sat}(ZTC)-(p_oT+q_o+r_oV_{bs})+\frac{xT(1+aT+b)p_o}{K_1(1+aT+b)+aT}]^2dT$$

$$=2\int_{T_o}^{T_1}[V_{gs}^{sat}(ZTC)-(p_oT+q_o+r_oV_{bs})+\frac{xT(1+aT+b)p_o}{K_1(1+aT+b)+aT}]dT=0 \quad \text{(eq.3-44)}$$

and then:

$$[V_{gs}^{sat}(ZTC)-q_o-r_oV_{bs}+\frac{xp_o(1+b)}{a(1+K_1)^2}](T_1-T_o)+\left[-\frac{p_o}{2}+\frac{xp_o}{2(1+K_1)}\right](T_1-T_o)(T_1+T_o)-$$

$$\frac{xp_o{T_z}^2}{K_1(1+K_1)(T_1-T_o)}\ln\frac{T_1+T_z}{T_o+T_z}=0 \quad \text{(eq. 3-45)}$$

The solution is figured out:

$$V_{gs}^{sat}(ZTC)=p_o\left[\frac{1}{2}-\frac{x}{2(1+K_1)}\right](T_1+T_o)+q_o+r_oV_{bs}-\frac{xp_oT_z}{K_1(1+K_1)}(1-\frac{T_z}{T_1-T_o})\ln\frac{T_1+T_z}{T_o+T_z}$$

(eq. 3-46)

If $V_{bs}=\alpha V_{gs}$, eq. 3-46 also returns back to eq. 3-40 as expected.

3.3.3 Parameter Extraction Setup

By linear approximation fitting, we can extract the slopes of V_t-T curves shown in Fig. 3-2 and 3-3, and calculate the averaged value, that's just the value of p_o:

$$p_o=\frac{\partial V_t(T,V_{bsi})}{\partial T}\Big|_{ave,V_{bsi}=0\sim0.6V} \quad \text{(eq. 3-47)}$$

Then we obtain the corresponding value r_o by eq. 3-48 as following, that's also an averaged value over the range of temperatures and body biases:

$$r_o=\frac{V_t(T_f,V_{bsi})-V_t(T_f,V_{bsj})}{V_{bsi}-V_{bsj}}\Big|_{ave,\,T_f=298\sim398K,V_{bs}=0\sim0.6V,i\neq j} \quad \text{(eq. 3-48)}$$

Using the known values of p_o and r_o, we could get the value of q_o as following:

$$q_o = [V_t(T_f, V_{bsi}) - p_o T_f - r_o V_{bsi}]|_{ave,\ T_f=298\sim398K, V_{bsi}=0\sim0.6V} \quad \text{(eq. 3-49)}$$

Applying $V_t - V_{bs}$ curves in Fig. 3-4 and 3-5 to extract every corresponding value of δ at every operation temperature, we could make the $\delta - T$ curve as shown in Fig. 3-6 and 3-7. In the same way, employing linear approximation fitting to the $\delta - T$ curve to get the slope, that's the value of a:

$$a = \frac{\partial \delta(T)}{\partial T} \quad \text{(eq. 3-50)}$$

Then the value of b is readily solved as follow:

$$b = \delta(T_f) - aT_f \quad \text{(eq. 3-51)}$$

While operating MOSFET under normal mode in linear region, we can assume $\frac{d\mu_n^{eff}(T)}{dV_{gs}}$ is negligible and then calculate the homologous transconductance [12]:

$$G_m^{lin} = \mu_n^{eff}(T) C_{ox} \frac{W}{L} V_{ds} \quad \text{(eq. 3-52)}$$

Now we can find out the tendency between mobility and temperature by investigating the tendency between transconductance and temperature as shown in Fig. 3-8 and 3-9. At low V_{gs}, substrate impurity scattering is dominant and there exists a relationship: $\mu_n^{eff}(T) \propto V_{gs} - V_t$; however, elevated V_{gs} would result in enhanced surface roughness scattering, and then the relation between $\mu_n^{eff}(T)$ and $(V_{gs} - V_t)$ becomes negative tendency as shown in eq. 3-6, so the maximum values of mobility and thus transductance exist. Here we only consider these values of transductance

before the extreme value due to the reason as mentioned that the ZTC point is too small to undergo the enhanced surface roughness scattering.

Then, we consider the influence of phonon scattering on mobility. The mutual compensation of $(V_{gs} - V_t)$ and temperature in eq. 3-4 $[\mu_n^{eff}(T) = \mu_n^{eff}(T_o)(\frac{T}{T_o})^{-K_1}]$ would result in a quasi-ZTC point for transductance, whose location would be before the maximum point [29].

However, we must choose these transductance values in the regime where exists outstanding dependence of mobility on temperature to tune the value K_1, and that's just the regime between its quasi-ZTC point and the extreme point:

$$\frac{\mu_n^{eff}(T_j)}{\mu_n^{eff}(T_i)} = \frac{Gm(T_j)}{Gm(T_i)} = \left(\frac{T_i}{T_j}\right)^{K_1}\Bigg|_{ave} \qquad \text{(eq. 3-53)}$$

Finally, using $I_d - V_{ds}$ curve shown in Fig. 3-10 and 3-11, we tune out the appropriate value of x:

$$\frac{I_d^{sat}(V_{gsi})}{I_d^{sat}(V_{gsj})} = \left(\frac{V_{gsi} - V_t}{V_{gsj} - V_t}\right)^x\Bigg|_{I_d^{sat}@V_{ds}^{sat} = V_{gs} - V_t} \qquad \text{(eq. 3-54)}$$

All of those parameter extractions are shown in Table. 3.2.

3.3.4 The ZTC Point Measurements of DTMOS

Extending the viewpoint of the above theory, the experimental value also could be obtained by two ways; we can operate the device under DT-mode, directly extracting the ZTC point as seen from Fig. 3-12 to 3-15, or we can employ the curve $V_{gs}(ZTC) - V_{bs}$ and the line $V_{bs} = \alpha V_{gs}$ as shown from Fig. 3-16 to Fig. 3-19 to get

the intersection point, that's also the ZTC point for DTMOS. The experimental and the theoretical values are listed in Table 3.3 and the corresponding currents in Table 3.4. Here K_1 don't have to equal 1.5, and it depends on the experimental results which reflect the scattering mechanisms and the qualities of devices. Being worth mentioning, the errors in the linear and saturation region are both smaller than 5%.

3.4 Summary

The purpose of this section is combining the idea of ZTC point with DTMOS application. For DTMOS operation, smaller threshold voltage than conventional MOS results in lower ZTC point value; besides, by adjusting the value of α, we can change the V_t shift and thus the ZTC point shift.

First, we present a drain current model of DTMOS. Then, distinct two ZTC point models are identified, one is in the linear region, and the other is in the saturation region. Additionally, we take the factor δ and the modification of ideal square-law condition under saturation mode to increase the accuracy. Then we show a series steps to extract those considered parameters so that the ZTC point predicted value could be figured out. On the other hand, we also operate the device under DT-mode to get the ZTC point experimentally.

Furthermore, we employ the ZTC point under normal mode at a fixed body bias and the equation $V_{bs} = \alpha V_{gs}$ to take the point of intersection as another method of extracting DTMOS ZTC point both theoretically and experimentally.

In the end, owing to considering many extra parameters than beforehand researches, we attain very small error between predicted value and experimental data ($< 5\%$) no matters in the linear or nonlinear regions.

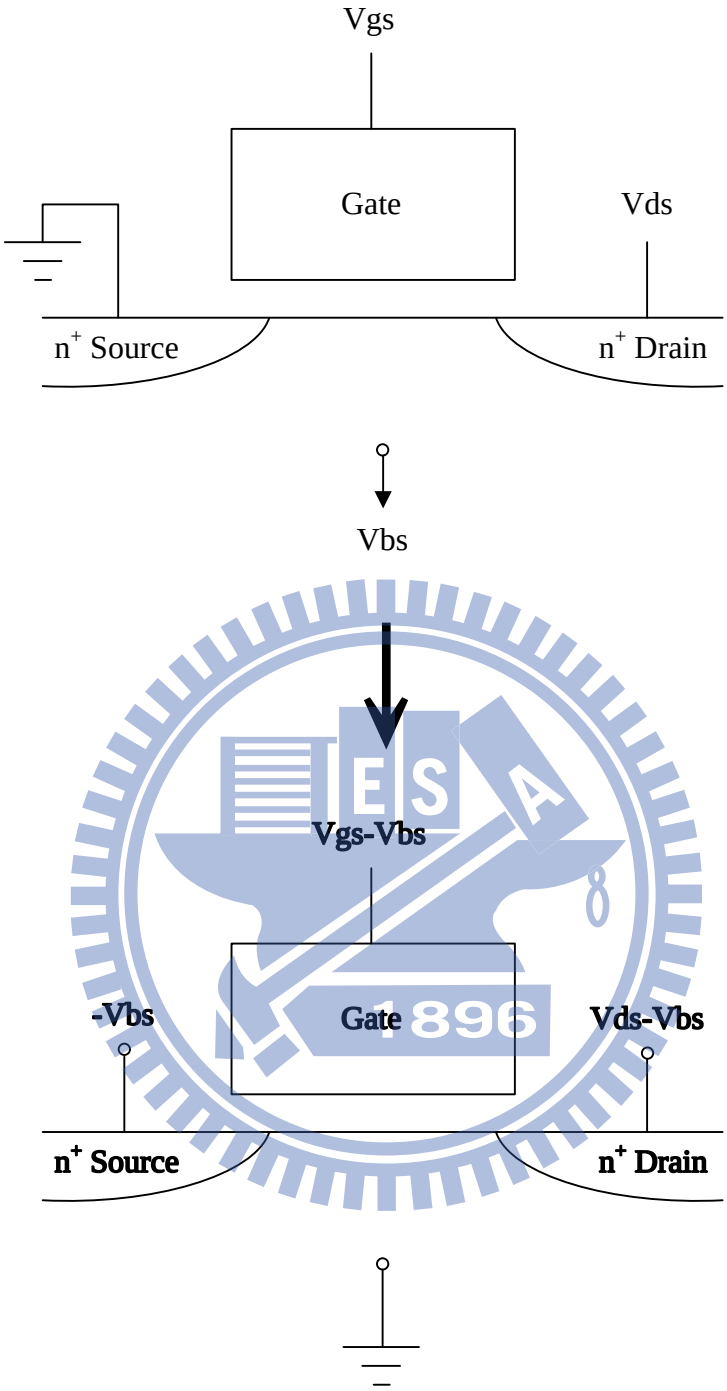


Fig. 3-1 Equivalent circuits used to evaluate the effect of substrate bias on MOSFET I-V characteristics.

Temperature	300K	375K	400K
$N_i\ (cm^{-3})$	$1.5 * 10^{10}$	$1.6 * 10^{12}$	$5.2 * 10^{12}$
$2\emptyset_{fp}\ (V)$	0.954	0.726	0.669

Table 3.1 $N_i\ (cm^{-3})$ and $2\emptyset_{fp}\ (V)$ lists for polysilicon gate at different temperatures.

(a)

(b)

(C)

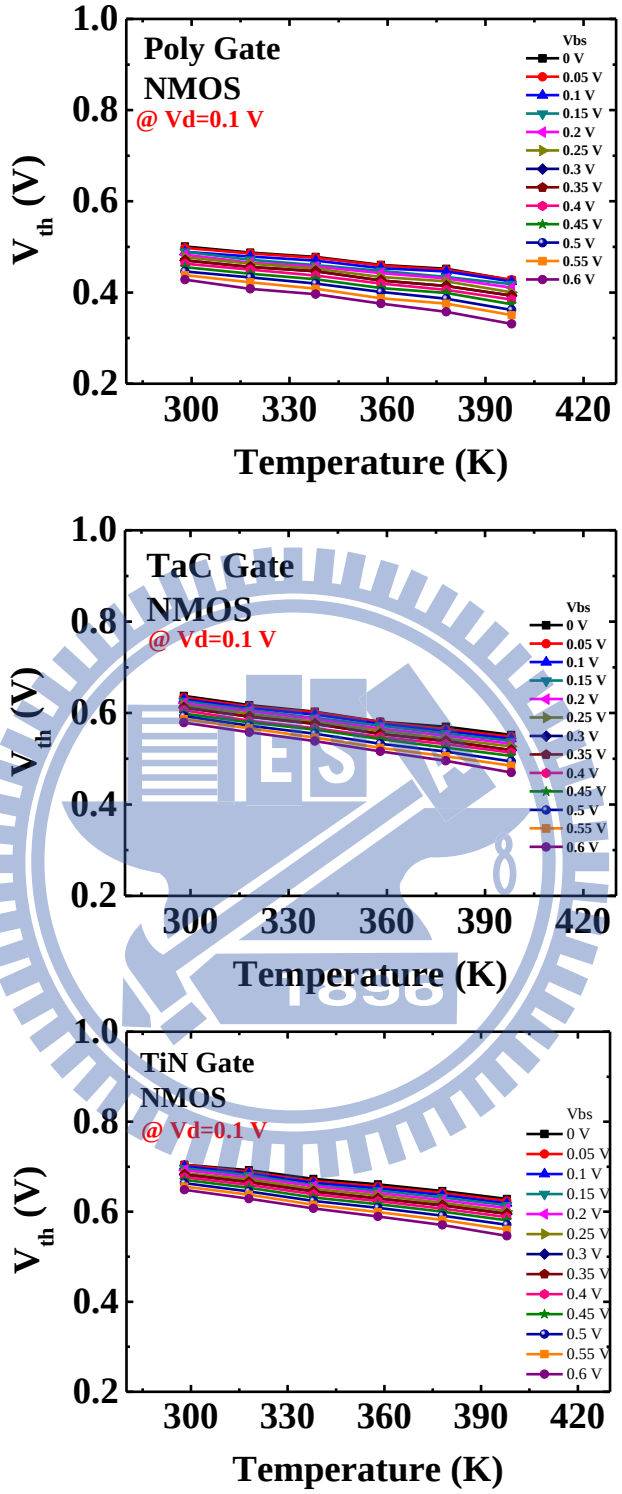


Fig. 3-2 Threshold voltage versus temperature for NMOS with (a) polysilicon (b) TaC (c) TiN gate under different body bias. The sweep range of body bias is from 0V to 0.6V.

(a)

(b)

(C)

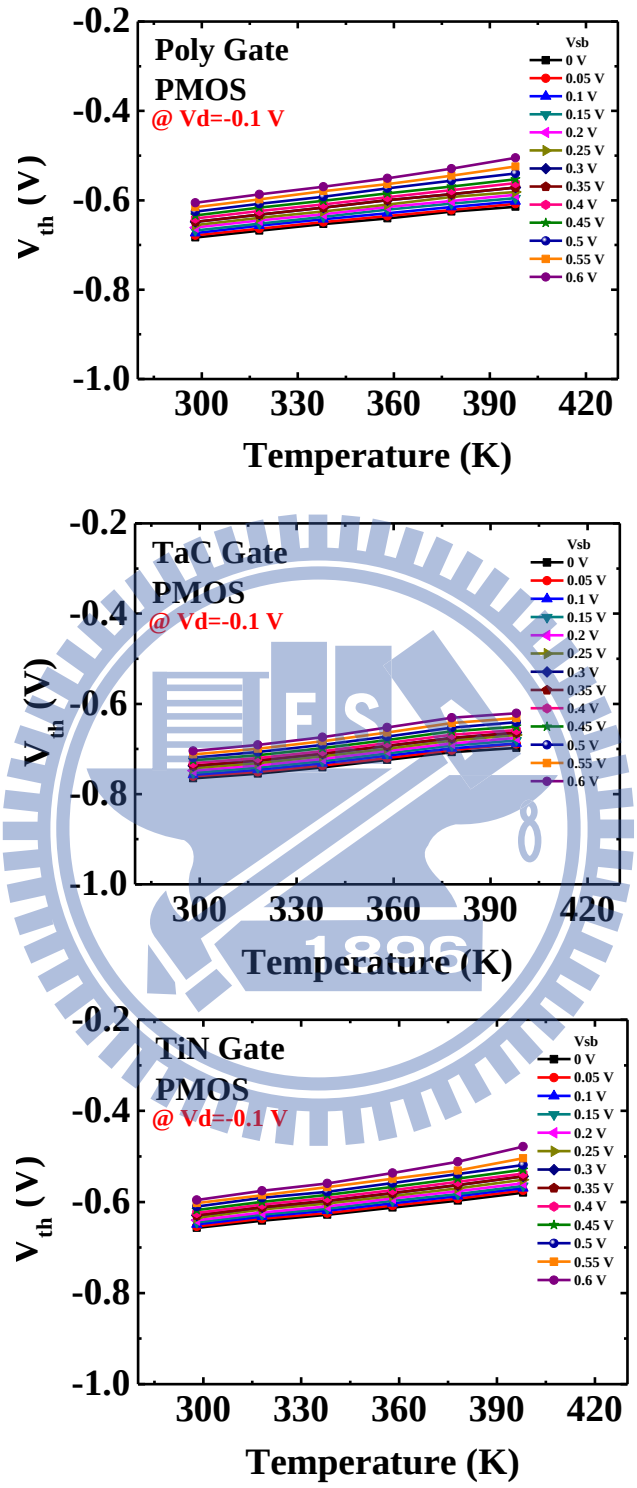
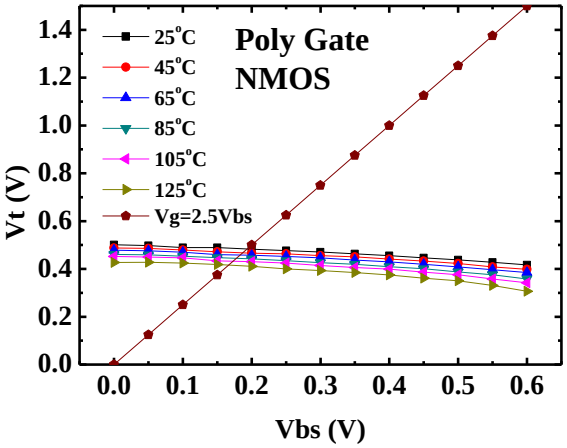


Fig. 3-3 Threshold voltage versus temperature for PMOS with (a) polysilicon (b) TaC (c) TiN gate under different body bias. The sweep range of body bias is from 0V to 0.6V.

(a)



(b)

(C)

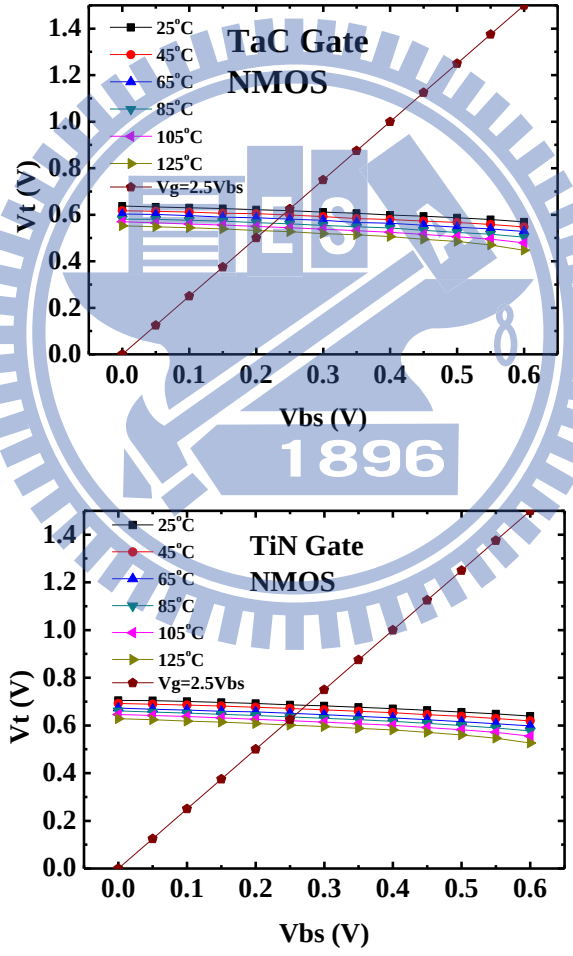
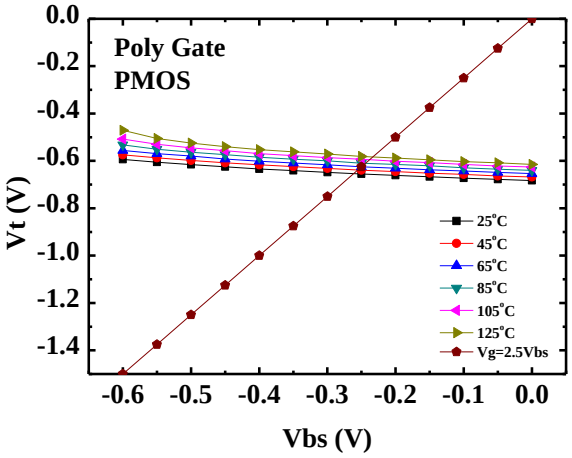
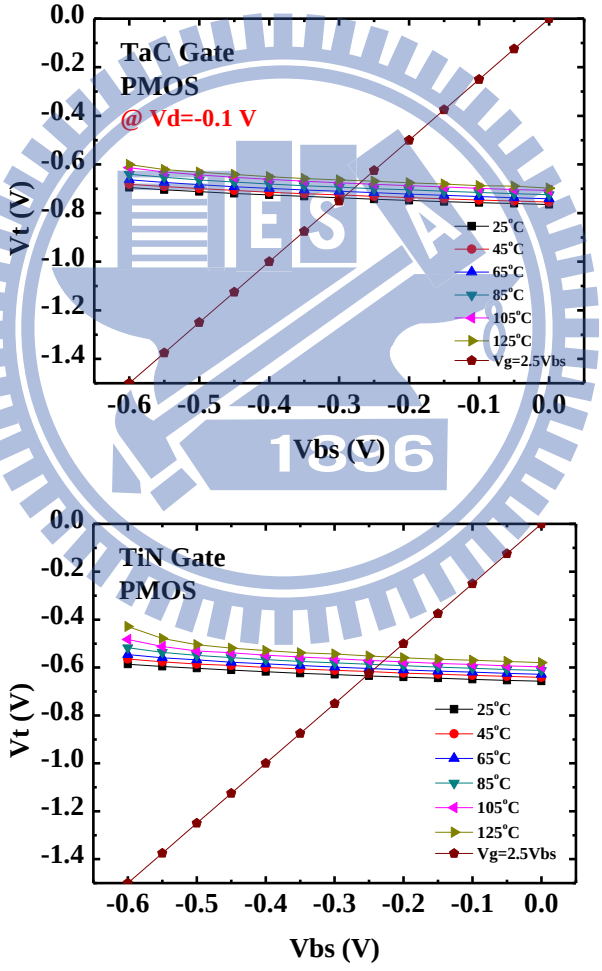


Fig. 3-4 Threshold voltage versus body bias for NMOS with (a) polysilicon (b) TaC (c) TiN gate for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively.

(a)



(b)



(C)

Fig. 3-5 Threshold voltage versus body bias for PMOS with (a) polysilicon (b) TaC (c) TiN gate for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively.

(a)

(b)

(C)

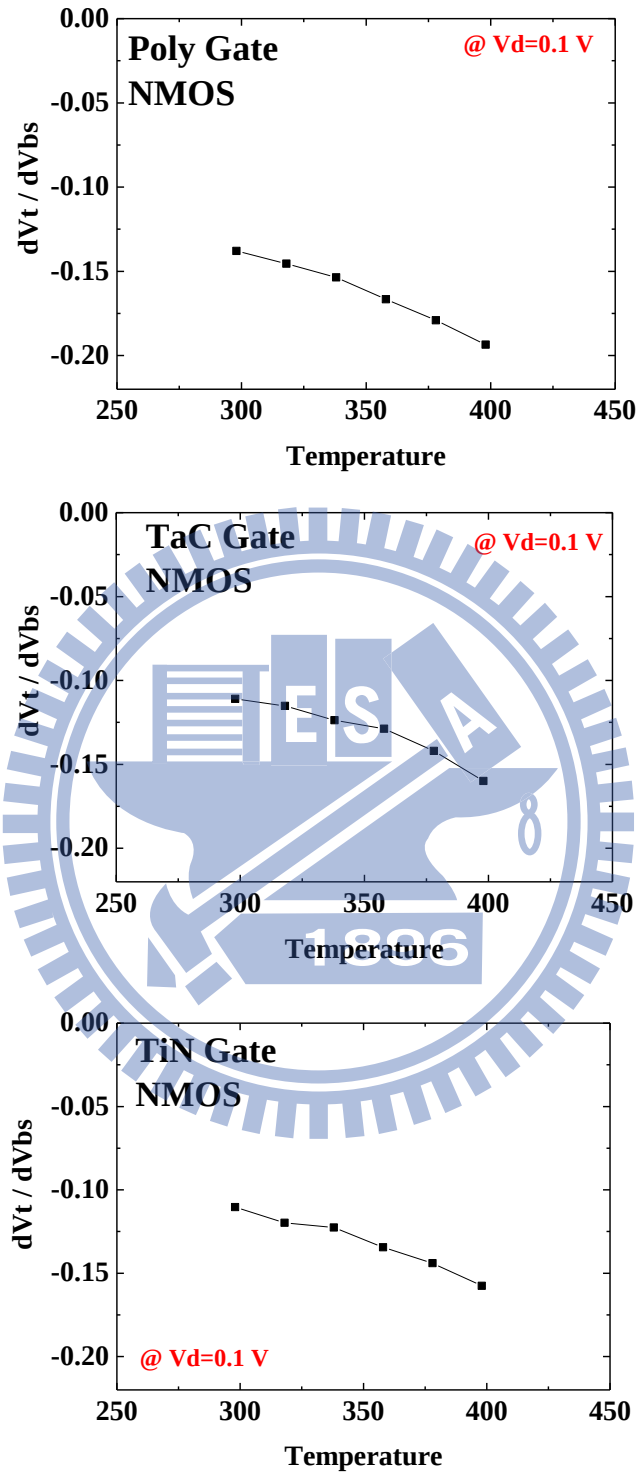
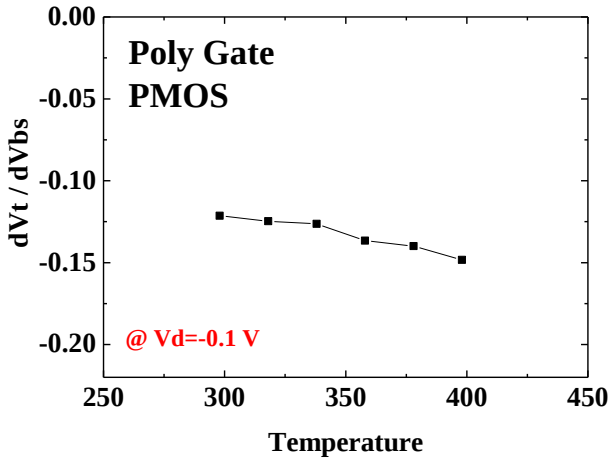


Fig. 3-6 Averaged values of minus body effect parameter versus temperature for NMOS with (a) polysilicon (b) TaC (c) TiN gate material. The sweep range of body bias is from 0V to 0.6V.

(a)



(b)

(C)

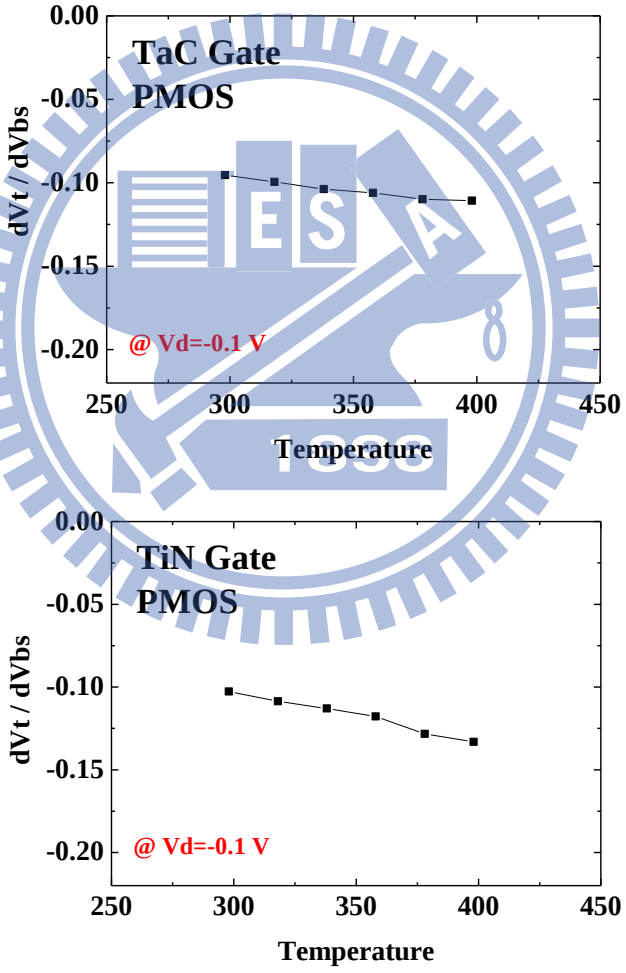
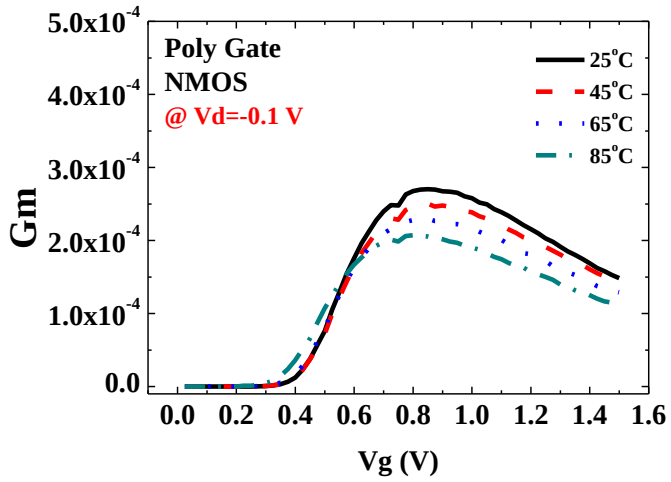


Fig. 3-7 Averaged values of minus body effect parameter versus temperature for PMOS with (a) polysilicon (b) TaC (c) TiN gate material. The sweep range of body bias is from 0V to 0.6V.

(a)

(b)



(C)

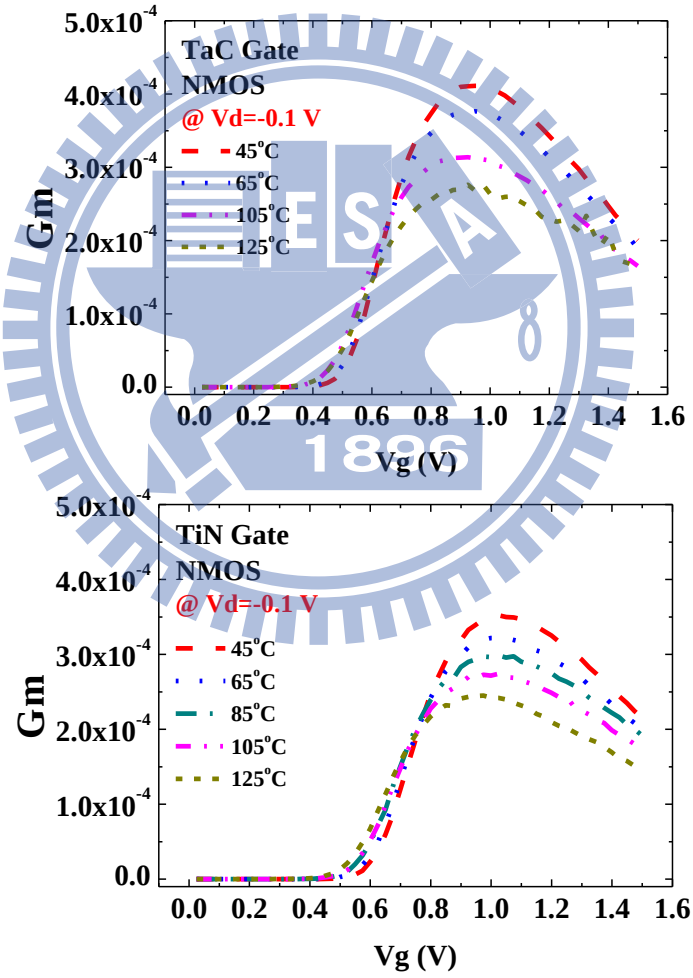
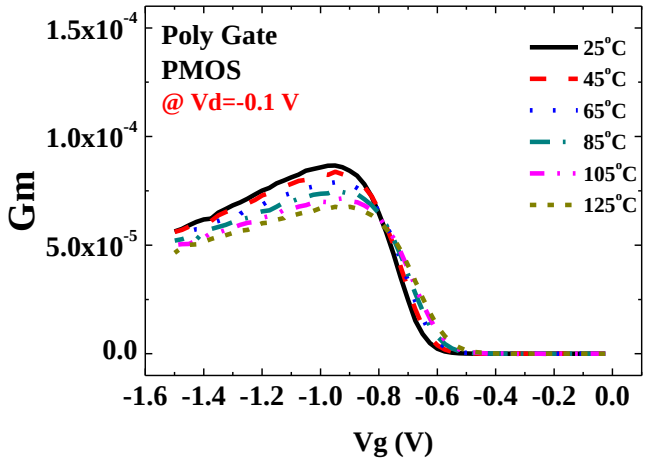


Fig. 3-8 Transconductance versus gate voltage for NMOS with (a) polysilicon (b) TaC (c) TiN gate under normal mode for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively.

(a)



(b)

(C)

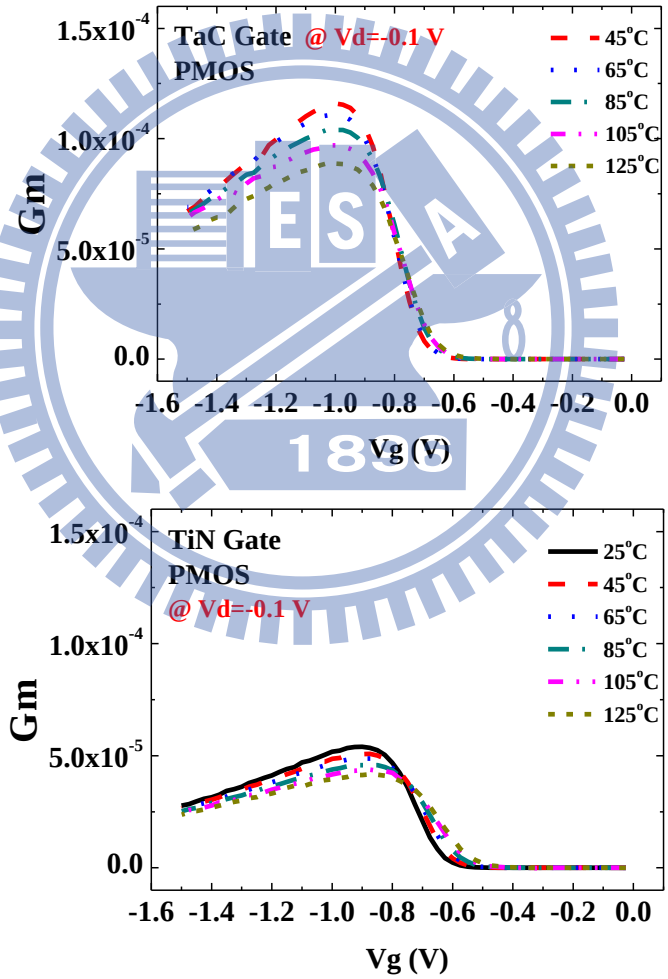
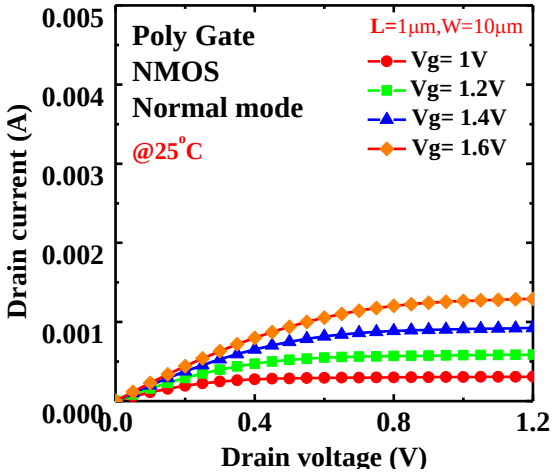


Fig. 3-9 Transconductance versus gate voltage for PMOS with (a) polysilicon (b) TaC (c) TiN gate under normal mode for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively.

(a)

(b)



(C)

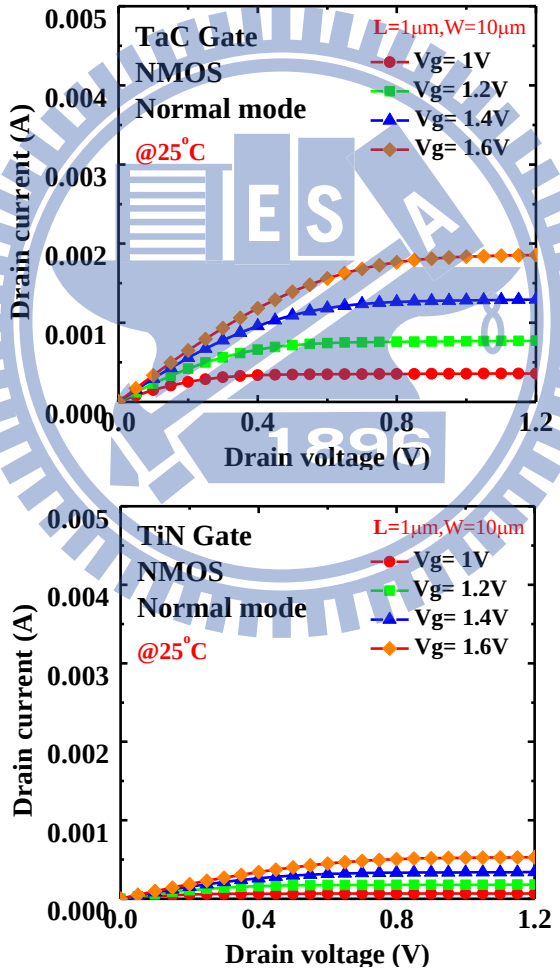
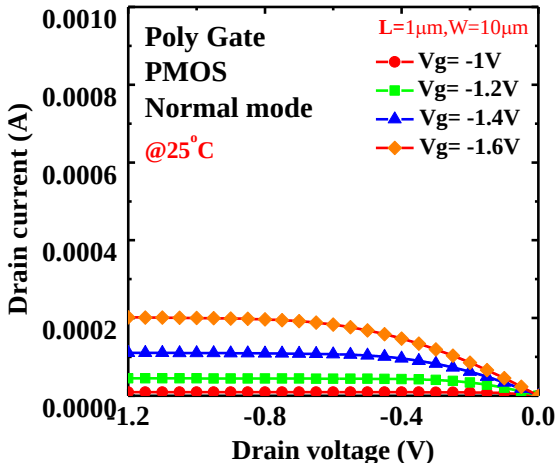


Fig. 3-10 Drain current versus drain voltage for NMOS with (a) polysilicon (b) TaC (c) TiN gate material under normal mode with different gate bias. The sweep range of gate bias is from 1V to 1.6V.

(a)

(b)



(C)

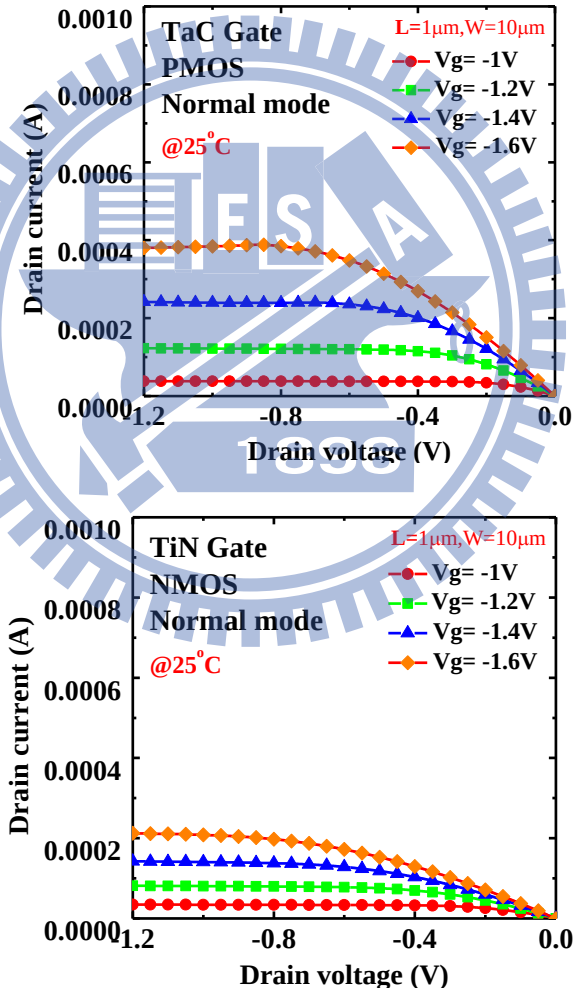


Fig. 3-11 Drain current versus drain voltage for PMOS with (a) polysilicon (b) TaC (c) TiN gate material under normal mode with different gate bias. The sweep range of gate bias is from -1V to -1.6V.

(a)

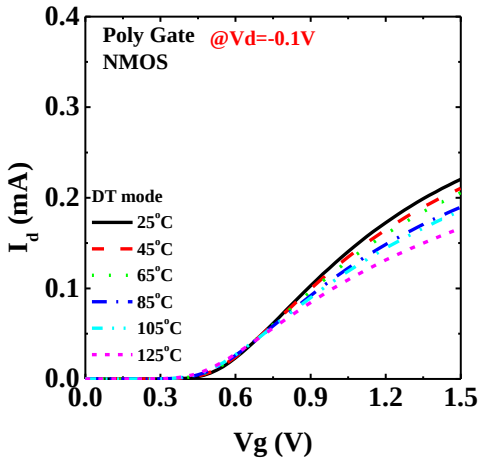
Gate	Poly	TaC	TiN
suggested K1	1.2	1.5	1.3
Po (mV/K)	-0.78	-0.94	-0.88
qo (V)	0.748	0.922	0.976
ro	-0.166	-0.134	-0.136
a (1/V)	0.00056	0.00047	0.00046
b (K/V)	-0.028	-0.029	-0.026
x	1.8	1.8	1.8

(b)

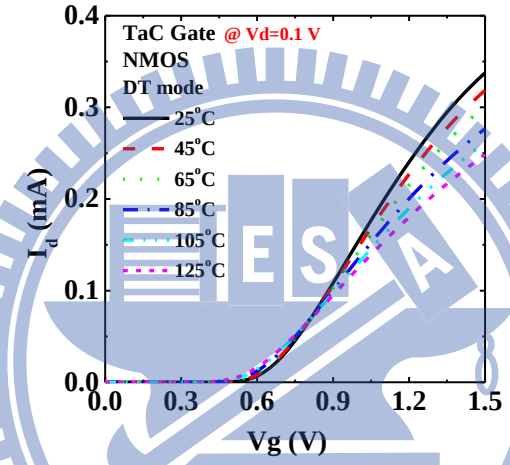
Gate	Poly	TaC	TiN
suggested K1	0.9	0.9	0.9
Po (mV/K)	0.817	0.775	0.91
qo (V)	-0.937	-1.01	-0.943
ro	-0.18	-0.174	-0.163
a (1/V)	0.00027	0.00016	0.00031
b (K/V)	0.04	0.049	0.011
x	1.9	1.9	1.9

Table 3.2 Extracted parameters for (a) DT-NMOS and (b) DT-PMOS.

(a)



(b)



(C)

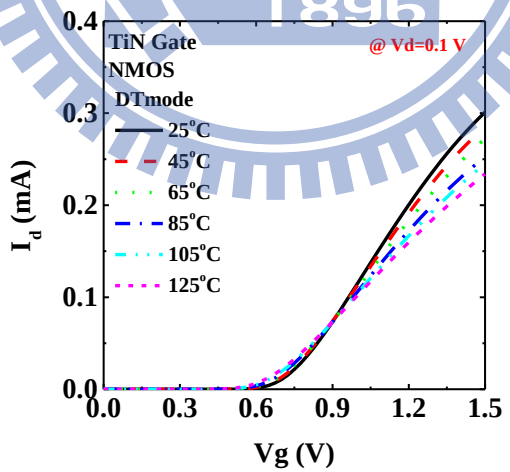
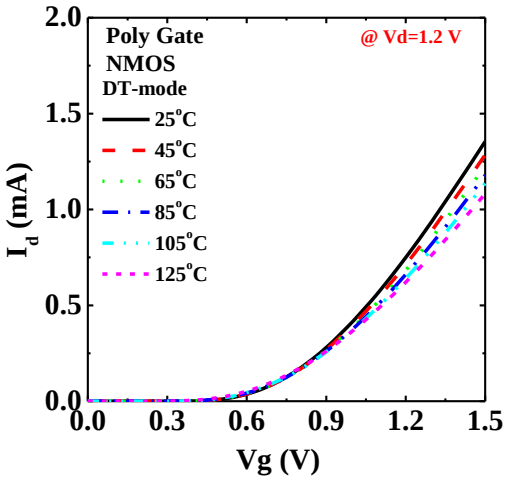
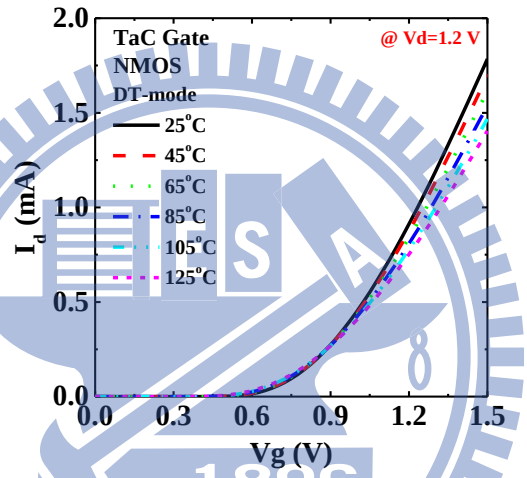


Fig. 3-12 Drain current versus gate voltage for DT-NMOS with (a) polysilicon (b) TaC (c) TiN gate for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively and the applied drain voltage is 0.1V.

(a)



(b)



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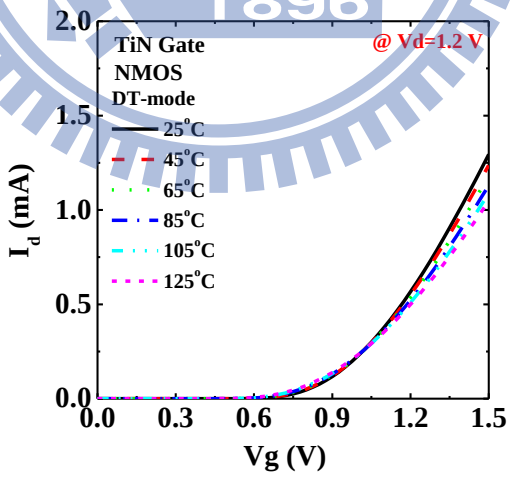
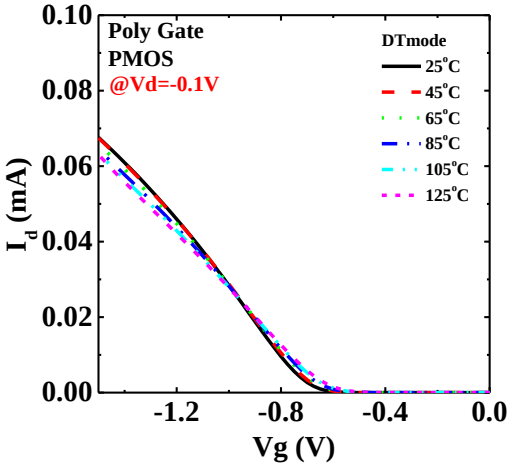
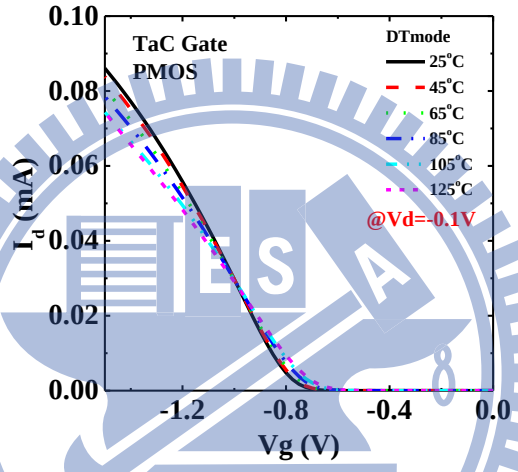


Fig. 3-13 Drain current versus gate voltage for DT-NMOS with (a) polysilicon (b) TaC (c) TiN gate for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively and the applied drain voltage is 1.2V.

(a)



(b)



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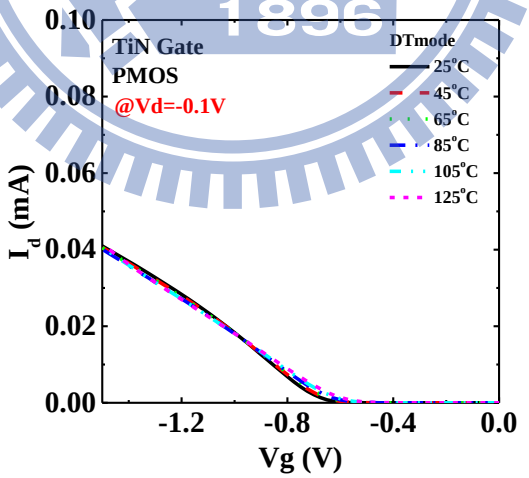
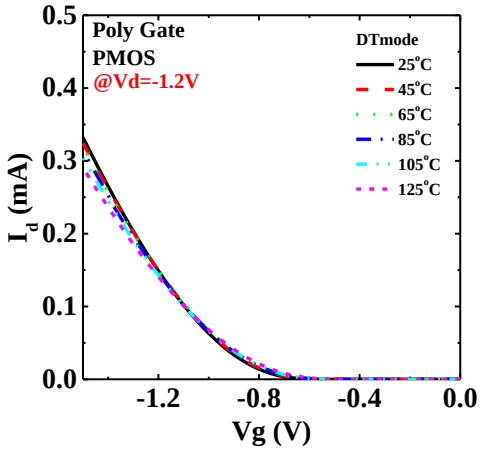
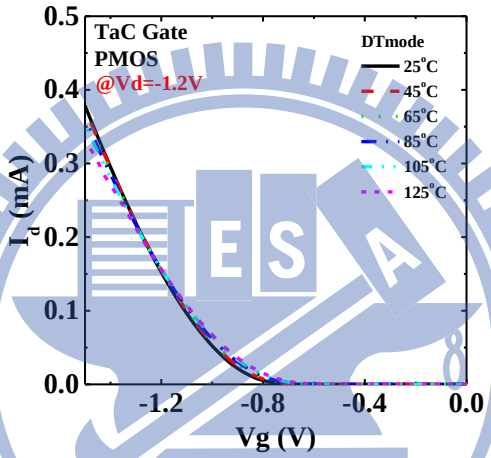


Fig. 3-14 Drain current versus gate voltage for DT-PMOS with (a) polysilicon (b) TaC (c) TiN gate for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively and the applied drain voltage is -0.1V.

(a)



(b)



(C)

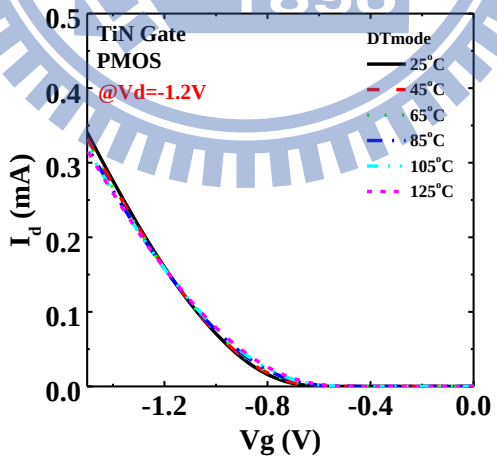
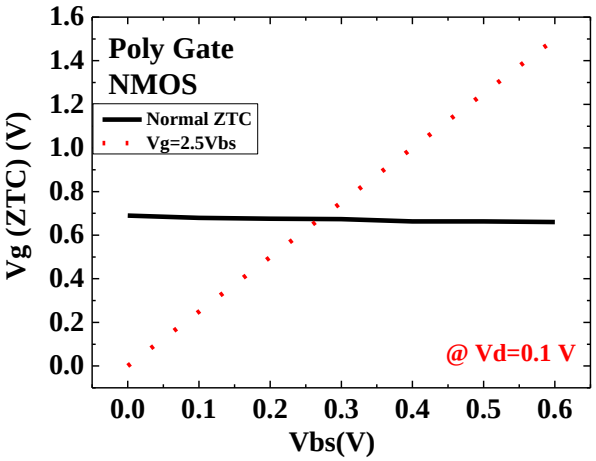
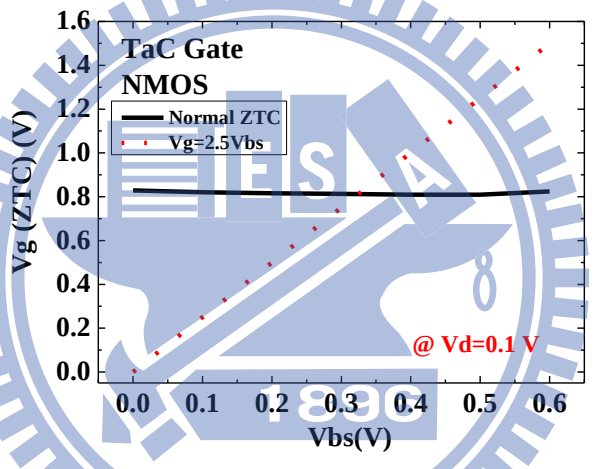


Fig. 3-15 Drain current versus gate voltage for DT-PMOS with (a) polysilicon (b) TaC (c) TiN gate for different operation temperatures. The operation temperatures are fixed 298K, 318K, 338K, 358K, and 398K, respectively and the applied drain voltage is -1.2V.

(a)



(b)



(C)

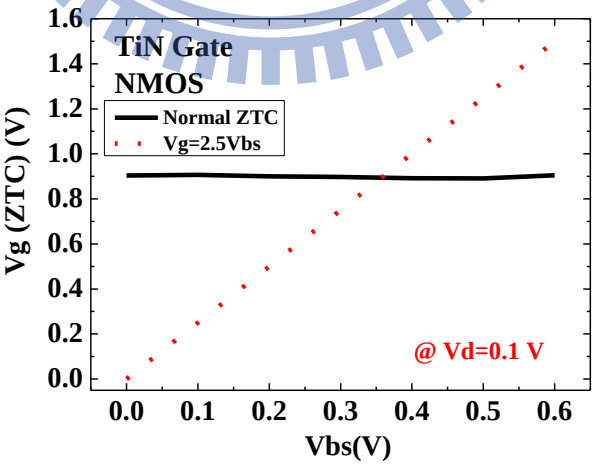


Fig. 3-16 Experimental value of ZTC point versus body bias for NMOS with (a) polysilicon (b) TaC (c) TiN gate. The applied drain voltage is 0.1V.

(a)

(b)

(C)

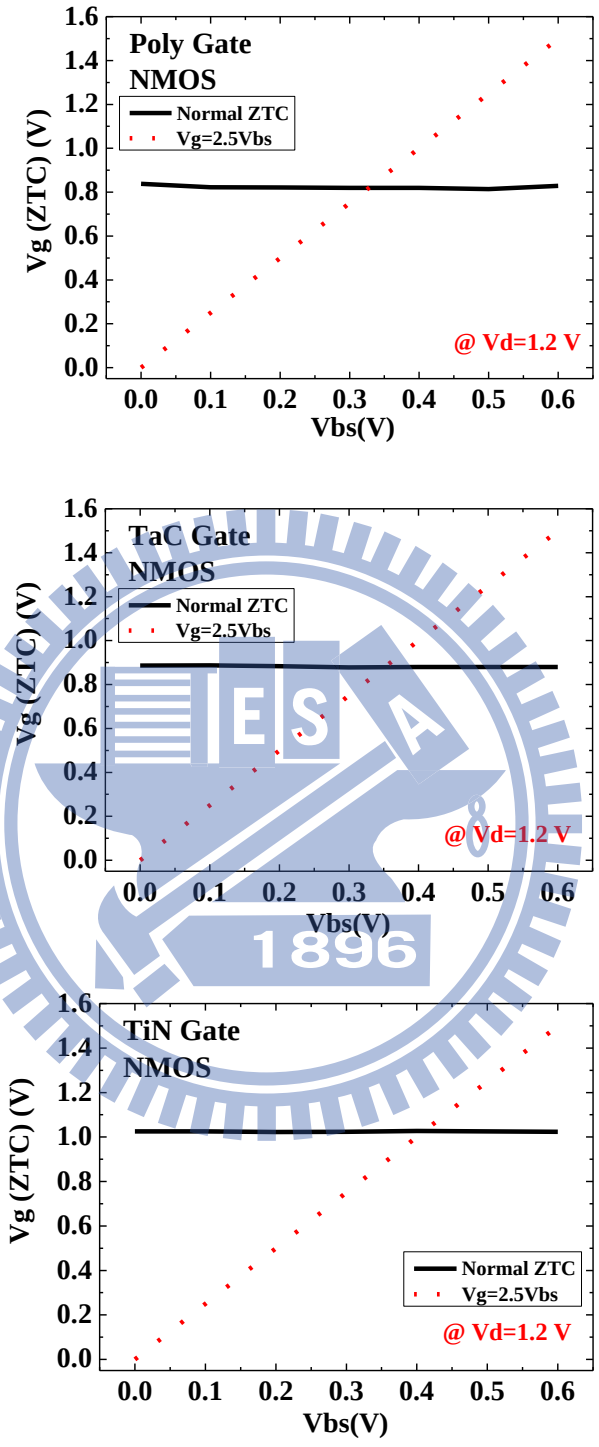
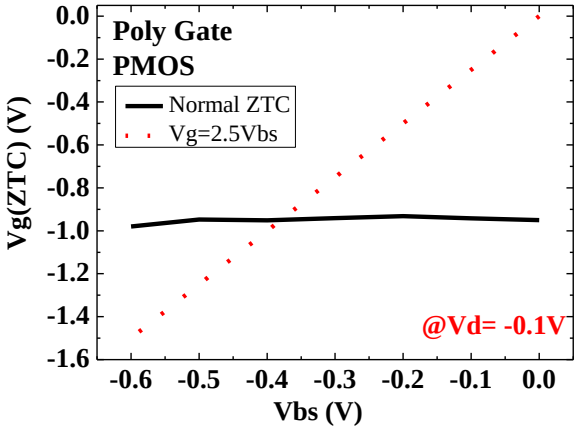
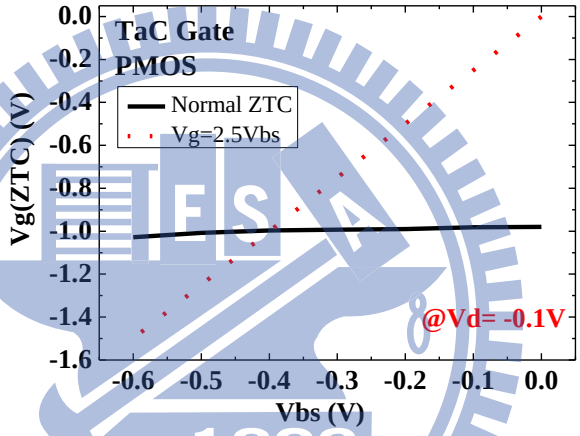


Fig. 3-17 Experimental value of ZTC point versus body bias for NMOS with (a) polysilicon (b) TaC (c) TiN gate. The applied drain voltage is 1.2V.

(a)



(b)



(C)

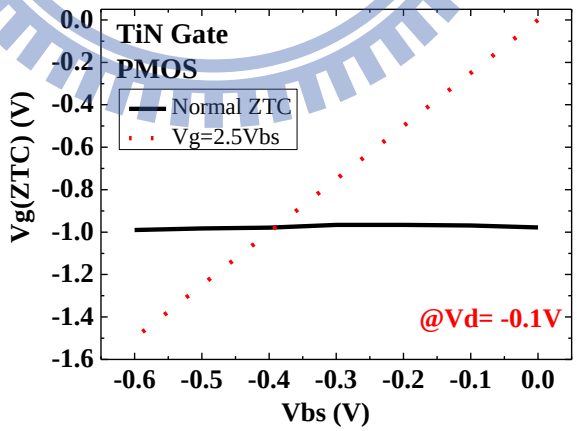
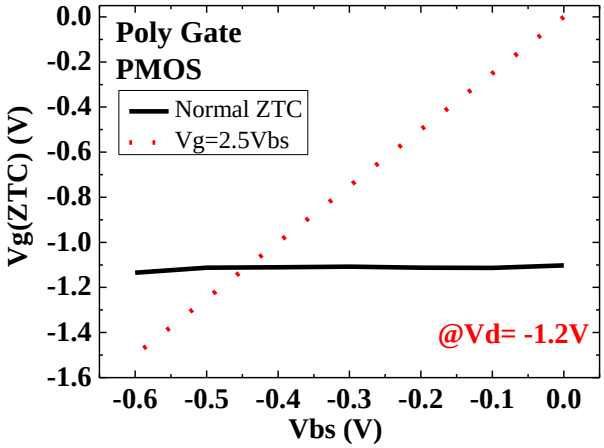


Fig. 3-18 Experimental value of ZTC point versus body bias for PMOS with (a) polysilicon (b) TaC (c) TiN gate. The applied drain voltage is -0.1V.

(a)

(b)



(C)

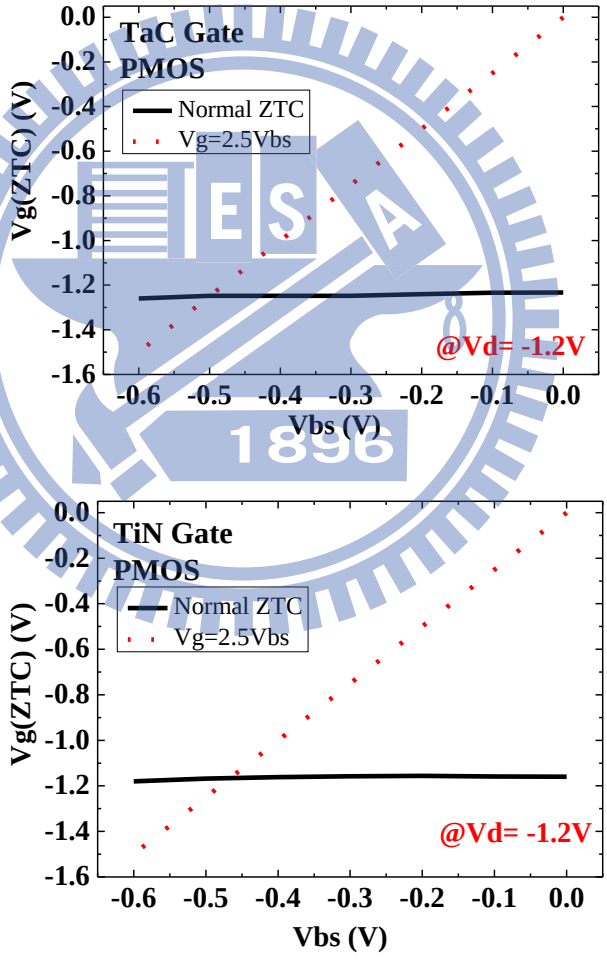


Fig. 3-19 Experimental value of ZTC point versus body bias for NMOS with (a) polysilicon (b) TaC (c) TiN gate. The applied drain voltage is -1.2V.

(a)

Vg(ZTC)Id	Poly	TaC	TiN
lin_theoretical (V)	0.706	0.821	0.906
lin_experimental (V)	0.688	0.811	0.898
lin_error	2.61%	1.24%	0.92%
sat_theoretical (V)	0.782	0.904	0.997
sat_experimental (V)	0.801	0.883	1.02
sat_error	2.37%	2.45%	2.18%

(b)

Vg(ZTC)	Poly	TaC	TiN
lin_theoretical (V)	-0.951	-1.02	-0.964
lin_experimental (V)	-0.942	-0.996	-0.973
lin_error	1%	2.8%	0.94%
sat_theoretical (V)	-1.12	-1.2	-1.154
sat_experimental (V)	-1.109	-1.23	-1.162
sat_error	1.02%	2.3%	0.68%

Table 3.3 Comparison of the ZTC point between theoretical value and experimental value for (a) DT-NMOS and (b) DT-PMOS.

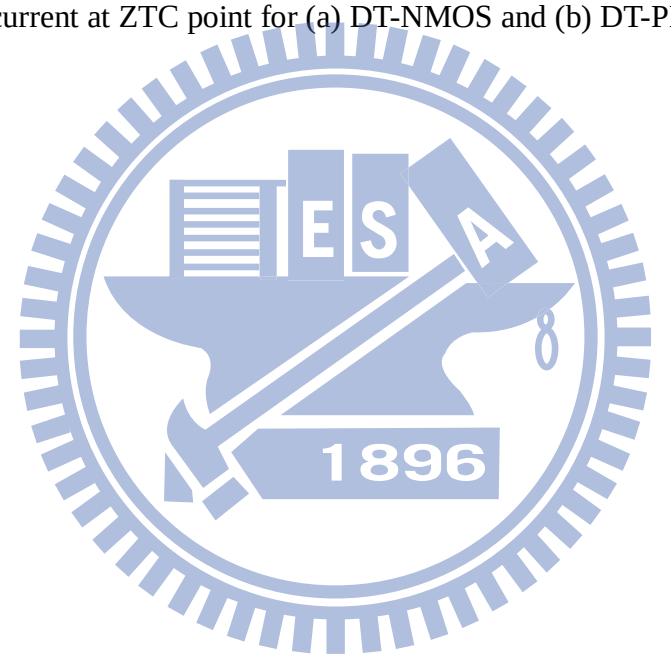
(a)

Id(ZTC)	Poly	TaC	TiN
lin_experimental (mA)	0.045	0.071	0.074
sat_experimental (mA)	0.176	0.456	0.259

(b)

Id(ZTC)	Poly	TaC	TiN
lin_experimental (mA)	0.024	0.028	0.017
sat_experimental (mA)	0.101	0.167	0.142

Table 3.4 Drain current at ZTC point for (a) DT-NMOS and (b) DT-PMOS.



Chapter 4

Conclusion and Future Work

4.1 Conclusion

From the theoretical and experimental results, metal gates have better gate control capability than polysilicon gate. Additionally, a high α with the low operation temperature further improves the gate control capability. As a result, high-K metal gate stack operated at the low operation temperature (223K) under DT-mode could bring about best performance.

Moreover, we deduce a drain current model of DTMOS, and then the corresponding both ZTC point models in the linear and saturation regions are identified. The analytical expression which takes in to consideration of the body bias effect δ and the modification of ideal square-law condition in the saturation region could effectively reduce the errors (< 5%). Furthermore, the analysis could help us to get the best current gain under low temperature operation for DT devices.

4.2 Suggestions for Future Work

In the chaper 3, we assume that threshold voltage is only dependent on temperature and body bias as in eq. 3-28. In fact, it should also depend on drain voltage due to DIBL effect, especially for the short channel devices. So, we can rewrite eq. 3-28 anew as following:

$$V_t(V_{bs}) = p_o T + q_o + r_o V_{bs} + \eta V_{ds} \qquad \text{(eq. 4-1)}$$

Since DIBL is dependent on temperature, so we further assume η as:

$$\eta = cT + d < 0 \qquad \text{(eq. 4-2)}$$

Extracting η, namely c and d, and taking it in to our ZTC point models, we can increase the accuracy, especially in the saturation region.

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碩士論文題目:

動態臨限電壓場效電晶體之零溫度係數點模型研究

Zero Temperature Coefficient Point Model of Dynamic Threshold MOSFETs