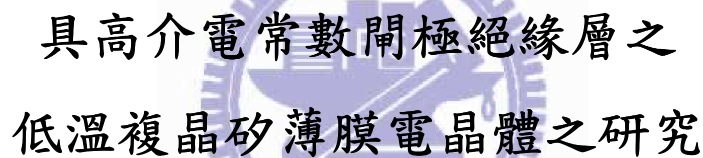
國 立 交 通 大 學

電子物理研究所

碩士論文



具高介電常數閘極絕緣層之

低溫複晶矽薄膜電晶體之研究

Investigation on LTPS-TFTs

With High-κ Gate Dielectrics

指導教授 ： 趙天生 博士

研 究 生 ： 劉聿民

中華民國 九十九 年 七 月

具高介電常數閘極絕緣層之低溫複晶矽薄膜電晶體之研究

Investigation on LTPS-TFTs With High-κ Gate Dielectrics

指導教授：趙天生 博士　　　Advisor： Dr. Tien-Sheng Chao

研究生：劉聿民　　　Student：Yu-Min Liu

國立交通大學

電子物理研究所

碩士論文

Submitted to Institute of Electrophysics

College of Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Master of Science in Electrophysics

July 2010

Hsinchu, Taiwan, Republic of China.

中華民國 九十九 年 七 月

具高介電常數閘極絕緣層之低溫複晶矽薄膜電晶體之研究

指導教授 ： 趙天生 博士　　　　　　　研究生：劉聿民

國立交通大學

電子物理研究所

摘要

在本論文中，我們製作並且研究具有不同厚度二氧化鉿閘極絕緣層的Ｐ形通道低溫複晶薄膜電晶體。我們比較了具有不同厚度二氧化鉿閘極絕緣層的Ｐ形通道低溫複晶薄膜電晶體的電性和可靠度。在電性方面，我們發現轉導電導的峰值會隨著二氧化鉿絕緣層的厚度增加而升高。這個現象違反了我們之前的認知：閘極的控制能力應會隨著閘極電容值的上升而增強。因此，造成這個現象的原因值得我們探討。我們發現具有小厚度二氧化鉿的薄膜電晶體其轉導電導的峰值會因為二氧化鉿產生相變而發生劣化；另外，具有較厚二氧化鉿閘極絕緣層的薄膜電晶體會因其中具有較多本質的帶正電荷的氧缺陷使其轉導電導的峰值獲得較大幅度地提升。最後，我們系統性地探討了閘極負偏壓高溫應力(NBTI)對具有不同厚度二氧化鉿閘極絕緣層Ｐ形通道薄膜電晶體的劣化機制，我們發現臨界電壓漂移、次臨界擺幅和轉導電導峰值的劣化主要和二氧化鉿絕緣層的厚度、應力溫度和應力偏壓的大小有關。

Investigation on LTPS-TFTs With High-κ Gate Dielectrics

Advisor: Dr. Tien-Sheng Chao **Student: Yu-Min Liu**

Department of Electrophysics
National Chiao Tung University

Abstract

In this thesis, p-channel LTPS-TFTs with different thickness of the HfO_2 gate dielectrics were fabricated and investigated. We compared the electrical characteristics and the NBTI reliability issue of the p-channel LTPS-TFTs with the different thickness of HfO_2 gate dielectrics. As for the electrical characteristics, we found that the peak transconductance (G_{m_max}) increases with the HfO_2-thickness. This phenomenon violates the well known knowledge that the gate control ability should be enhanced with a higher gate capacitance. Therefore, it is worthwhile to investigate the mechanism of this phenomenon. We found that the phase change of the HfO_2 layers contributes to the G_{m_max} degradation of the TFTs with the thin HfO_2 layer. Besides, it was found that the enhanced G_{m_max} of the p-channel TFTs with the thicker HfO_2 layer is related to the intrinsic charged oxygen vacancies in the HfO_2 layer. Finally, the degradation mechanism of the NBTI stress was systematically studied. It was found that the behavior of V_{th} variation, S.S. degradation and the G_{m_max} degradation are mainly dependent on the thickness of the HfO_2 layer, stress temperature and the stress bias.

誌謝

時光飛逝，兩年的碩士生活一下子就要面臨尾聲。在這短短兩年的研究生涯，真的受到太多人的愛護與幫助。首先非常感謝指導教授趙天生老師的栽培，感謝趙老師在聿民對研究生活最徬徨的時候給予我莫大的鼓勵和指引，燃起聿民對知識的渴求以及對研究的熱忱。老師溫文儒雅的學者風範，不論是在待人接物抑或治學態度上都將是聿民心目中永遠的典範。

接下來，聿民要感謝的是指導我的馬鳴汶、江宗育還有葉啟瑞學長，感謝馬鳴汶和葉啟瑞學長即使已在業界服務，但在忙碌之餘還是時常關心聿民的實驗進度並給予指導。聿民最要感謝的是江宗育學長，感謝您從我碩一開始，就不辭辛勞地帶著我進無塵室做實驗，你總是不厭其煩地跟我反覆解釋每一道製程步驟，因為您的悉心指導，讓聿民對實驗的技巧越來越純熟，做事態度也越來越細心。另外在最後的量測和 data 分析部分，如果沒有您的用心指導，聿民的論文絕對無法如期完成，您對我的恩惠，聿民將永遠銘記在心。另外感謝實驗室的學長姐及同學平日的照顧與鼓勵，讓我感受到實驗室無比的溫暖和喜悅。這其中包括了：郭柏儀學長、林哲緯學長、呂宜憲學長、呂侑倫學長、王冠迪學長、廖家駿學長、吳翊鴻學長、林威良學長、王智盟學長、黃士安學長、林玉喬學姐、楊才民學長、曾繁達學長、劉聖賢學長、嚴立丞學長。以及同學：時璟、政昌、岷臻、琬琦。學弟妹：其儒、芳昌、添舜、立盈以及昱璇...等。感謝大家平日帶給聿民的幫助和歡樂，都是因為你們一路的陪伴，讓聿民的研究生活變得多采多姿。

最後，我要對我的父母劉智先生和楊怡文女士致上最深的謝意，感謝您們從小到大給聿民一個最好的教育環境，並且以身教，言教激發鼓勵聿民奮發上進；您們對聿民日常生活的呵護備至，讓聿民可以無後顧之憂地專心完成學業，感謝您們對聿民不辭辛勞的照顧及栽培，聿民日後將努力貢獻所學於國家社會以榮耀我偉大的父母親。另外我還要特別感謝在論文寫作期間一路陪伴我的女友芷瑋，在我面臨研究最挫折的時候給我打氣，讓我充滿了突破困境的能量，也可以共同分享寫論文的甘苦，寶貝我愛妳！！我謹以這篇論文獻給所有在論文寫作期間曾經給予我幫助以及關懷的人。

Contents

Abstract (Chinese)……………………………………………………..……..i

Abstract (English)…………………………………………….…….…….ii

Acknowledgement……………………………………………..………......iii

Contents…………………………………….……………….……….….....iv

Table Caption………………………………….…………….……….....vii

Figure Caption…………………………..…………………….…..vii

Chapter 1 Introduction

1.1 Overview of Thin-Film Transistors……………………………………1

1.2 Poly-Si TFTs using High-k Gate Dielectrics…………………………....3

1.3 Negative Bias Temperature Instability of LTPS TFTs…………………...4

1.4 NBTI Stress in High-κ Gate Dielectrics……………………………...7

1.5 Mobility Issues in High-k Dielectrics………………………………...8

1.6 Motivation…………………………………………………………..9

Chapter 1 Reference……………………………………………………..12

Chapter 2 Experimental Details and Method of Parameter Extraction

2.1 Device Fabrication………………………………………………...21

2.2 Measurement……………………………………………………22

2.3 Method of Parameter Extraction (Determination of Threshold Voltage)..22

2.3.1 Determination of subthreshold swing……………………………....24

2.3.2 Determination of on/off current ratio……………………………….24

2.3.3 Determination of field effect mobility……………………………………25

2.3.4 Determination of the trap state density…………………………………...26

Chapter 2 Reference………………………………………………………..31

Chapter 3 Electrical Characteristics of the p-channel LTPs TFTs with Different Thickness of High-κ Gate Dielectrics

3.1 Electrical Characteristics..32

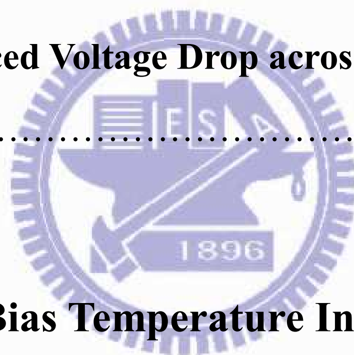
3.2 Material Analysis………………………………………………………34

3.2.1 Crystallization……………………………………………………….35

3.2.2 Source/Drain sheet resistance………………………………………....36

3.3 Oxygen Vacancy Induced Voltage Drop across the HfO_2 Layer……….37

Chapter 3 Reference………………………………………………………..51



Chapter 4 Negative Bias Temperature Instability in p-Channel LTPS TFTs with Different Thickness of HfO_2 Gate Dielectrics

4.1 Gate Leakage Current…………………………………………………53

4.2 NBTI Stress…………………………………………………………..56

4.2.1 V_{G_stress}-V_t = -3V at 25℃………………………………………………58

4.2.2 V_{G_stress}-V_t=-5V at 25℃……………………………………………..62

4.2.3 V_{G_stress}-V_t=-3V at 125℃……………………………………………66

4.2.4 V_{G_stress}-V_t=-4V at 125℃……………………………………………………69

Chapter 4 Reference……………………………………………………………..93

Chapter 5 Conclusion

5.1 Conclusion…………………………………………………………………96

Vita (Chinese)…………………………………………………………...…..99

Table Caption

Chapter 1

Table 1.1 Variation of electronic parameters and corresponding possible degradation mechanism and the main degraded locations……………………..10

Chapter 3

Table 3.1 (a) The electrical parameters of the TFTs incorporating HfO_2 gate dielectrics before sintering……………………………………………………..43

Table 3.1 (b) The electrical parameters of the TFTs incorporating HfO_2 gate dielectrics after sintering……………………………………………………….43

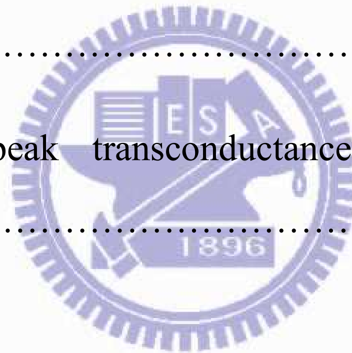


Table 3.2 The initial peak transconductance and the modified peak transconductance…………………………………………………………………48

Chapter 4

Table 4.1 The material composition of the transition layer in the 250Å sample, it is observed that the transition layer is mainly composed of Al and O atoms…..72

Table 4.2 The material composition of the transition layer in the 1700Å sample, it is observed that the transition layer is mainly composed of Al and O atoms..72

Figure Caption

Chapter 1

Fig. 1.1 The schematic plot of the NBTI stress mechanism in the TFTs with SiO_2 gate dielectrics………………………………………........................11

Chapter 2

Fig. 2.1 The device fabrication of the HfO_2-poly-Si TFTs……………………..30

Chapter 3

Fig. 3.1 (a) The transfer characteristics of the TFTs incorporating HfO_2 gate dielectrics after sintering of the first run, which had physical thickness of 250Å, 500Å, 700Å, 1000Å and 1700Å, respectively…………………………………41

Fig. 3.1 (b) The peak transconductance (G_{m_max}) increases with the thickness of the HfO_2 layer in the first run……………………………………………………..41

Fig. 3.2 (a) The transfer characteristics of the TFTs incorporating HfO_2 gate dielectrics before sintering at 400℃ in a N_2 ambient of the second run, which had physical thickness of 175Å, 415Å and 745Å, respectively………………..42

Fig. 3.2 (b) The transfer characteristics of the TFTs incorporating HfO_2 gate dielectrics after sintering at 400℃ in a N_2 ambient of the second run, which had physical thickness of 175Å, 415Å and 745Å, respectively……………………42

Fig. 3.2 (c) The peak transconductance (G_{m_max}) increases with the thickness of the HfO_2 layer after sintering in the second run. (d) temperature dependence of the G_{m_max}, it is obvious that the G_{m_max} still increases with the HfO_2 thickness even at high temperature of 100℃……………………………………………..43

Fig. 3.3 (a) The peak positions and intensities of the XRD spectra for three main crystalline phase of HfO_2, obtained from powder diffraction ICDD card files..44

Fig. 3.3 (b) XRD spectra of the 175Å-thick HfO_2 layer, showing the clear peaks correspond to the monoclinic phase in the Fig. 3-3 (a), indicating that the phase transformation completes after sintering at 400℃ in a N_2 ambient…………….44

Fig. 3.3 (c) XRD spectra of the 415Å-thick HfO_2 layer. No obvious peak was observed, indicating that the phase remains amorphous after sintering at 400℃ in a N_2 ambient……………………………………………………………45

Fig. 3.3 (d) XRD spectra of the 745Å-thick HfO_2 layer. No obvious peak was observed, indicating that the phase remains amorphous after sintering at 400℃ in a N_2 ambient……………………………………………………………45

Fig. 3.4 (a) The atomic-force microscopy (AFM) image of the poly-Si surface of the TFTs with 250Å-thick HfO_2 layer. The mean surface roughness is about 0.33nm………………………………………………………………………46

Fig. 3.4 (b) The atomic-force microscopy (AFM) image of the poly-Si surface of the TFTs with 1700Å-thick HfO_2 layer. The mean surface roughness is about 0.43nm…………………………………………………………………….....46

Fig. 3.5 (a) The extraction of the source/drain sheet resistance of the TFTs incorporating the 175Å-thick HfO_2 gate dielectric……………………………47

Fig. 3.5 (b) The extraction of the source/drain sheet resistance of the TFTs incorporating the 415Å-thick HfO_2 gate dielectric……………………………47

Fig. 3.5 (c) The extraction of the source/drain sheet resistance of the TFTs incorporating the 745Å-thick HfO_2 gate dielectric……………………………48

Fig. 3.6 (a) Cross-sectional TEM image of TFTs incorporating 250Å-thick HfO_2 gate dielectric…………………………………………………………….…..49

Fig. 3.6 (b) Cross-sectional TEM image of TFTs incorporating 1700Å-thick HfO_2 gate dielectric……………………………………………………………49

Fig. 3.7 Schematic of the silicon-metal oxide stack, showing the mechanism of transport of oxygen from the ambient to the silicon interface…………………50

Fig. 3.8 It become easier for holes to get across the grain boundary potential barrier height after the grain boundary potential barrier height is lowered by the voltage drop induced by the positively charged oxygen vacancies…………….50

Chapter 4

Fig. 4.1 Gate leakage current versus gate voltage of at 25℃…………………..71

Fig. 4.2 (a) Gate leakage current of 415Å-thick HfO_2 TFT sample versus gate voltage at different temperature, ranging from 25℃, 50℃, 75℃, 125℃……...73

Fig. 4.2 (b) Gate leakage current of 415Å-thick HfO_2 TFT sample versus gate voltage at different temperature, ranging from 25℃, 50℃, 75℃, 125℃……...73

Fig. 4.2 (c) Gate leakage current of 745Å-thick HfO2 TFT sample versus gate voltage at different temperature, ranging from 25℃, 50℃, 75℃, 125℃……...74

Fig. 4.3 The schematic plot of the V_{th} contribution separating method. We can derive the V_{th} shift attributed to oxide trapping by shifting the V_{on} of the initial I_D-V_G curve to the Von of the I_D-V_G curve after stressing. On the other hand, we can derive the V_{th} shift attributed to the interface states generation after shifting the V_{on} of the initial I_D-V_G curve……………………………………………74

Fig. 4.4 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at $V_{G_stress} - V_{th} = -3V$ from 2 to 1000 seconds at 25℃………………………………………………………………75

Fig. 4.4 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.....75

Fig. 4.4 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.....76

Fig. 4.4 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.....76

Fig. 4.4 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.....77

Fig. 4.4 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -5V after tress time of 1000 seconds at 25℃.....77

Fig. 4.4 (g) Schematic energy band diagram and the schematic degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25 ℃.....78

Fig. 4.4 (h) Schematic energy band diagram and the schematic degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 25℃.....78

Fig. 4.4 (i) Schematic energy band diagram and the schematic degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with

V_{G_stress}-V_t=-3V at 125℃……………………………………………………79

Fig. 4.5 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃……………………………………………………………………79

Fig. 4.5 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃……………………………………………..80

Fig. 4.5 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃……………………………………………...80

Fig. 4.5 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃………………………………………………………………81

Fig. 4.5 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃………………………………………………………………81

Fig. 4.5 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -5V after tress time of 1000 seconds at 25℃……………………………………………………………………………82

Fig. 4.5 (g) Schematic energy band diagram and the schematic degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25 ℃…………………………………………………………..82

Fig. 4.5 (h) Sechematic energy band diagram and the schematic degradation

mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25℃……………………………………………………...83

Fig. 4.5 (i) Schematic energy band diagram and the schematic degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25℃……………………………………………………...83

Fig. 4.6 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃……………………………………………………………...84

Fig. 4.6 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃……………………………………………84

Fig. 4.6 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃……………………………………………85

Fig. 4.6 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃…………………………………………………………..85

Fig. 4.6 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃…………………………………………………………..86

Fig. 4.6 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -3V after tress time of 1000 seconds at 125℃……………………………………………………………………...86

Fig. 4.6 (g) Sechematic energy band diagram and the schematic degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 125℃ 87

Fig. 4.6 (h) Sechematic energy band diagram and the schematic degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 125℃ 87

Fig. 4.6 (i) Schematic energy band diagram and the schematic degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 125℃ 88

Fig. 4.7 (a) The total V_{th} shift of TFTs with 175 Å, 415 Å and 745 Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃ 88

Fig. 4.7 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃ 89

Fig. 4.7 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃ 89

Fig. 4.7 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃ 90

Fig. 4.7 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000

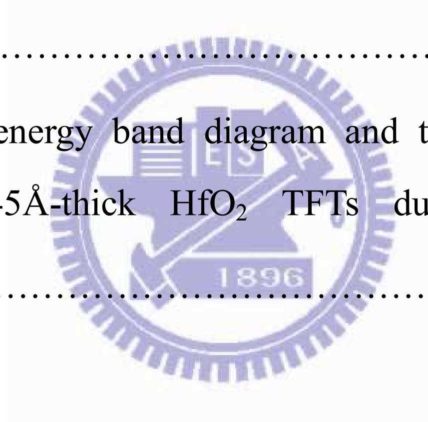
seconds at 125℃……………………………………………………………..90

Fig. 4.7 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -4V after tress time of 1000 seconds at 125℃…………………………………………………………………...91

Fig. 4.7 (g) Schematic energy band diagram and the schematic degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-4V at 125℃…………………………………………………….91

Fig. 4.7 (h) Schematic band diagram and the schematic degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-4V at 125℃…………………………………………………………………...92

Fig. 4.7 (i) Schematic energy band diagram and the schematic degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-4V at 125℃…………………………………………………….92



Chapter 1

Introduction

1.1 Overview of Thin-Film Transistors

A thin-film transistor (TFT) is a special type of field-effect transistor made by depositing thin films of a semiconductor active layer as well as the dielectric layer and metallic contacts over a substrate. A common substrate is glass, since the primary application of TFTs is in liquid crystal displays. This is different from the conventional transistor where the substrate material is typical semiconductor material, such as a silicon wafer. The first TFT device was proposed in 1961 by Dr. P.K. Wenimer in Radio Company of America (RCA). In 1966, the first polycrystalline silicon thin film transistors (Poly-Si TFTs) were demonstrated by C.H. Fa et al [1]. However, the study of poly-Si TFTs fabricated with low temperature of 600℃ was not proposed until 1980s. With its simplicity of structure and fabrication, the low-temperature polycrystalline silicon TFT (LTPS-TFT) has drawn much attention for the application in image sensors and displays. In recent years, the flat panel display (FPD) is widely used in advanced electronic products such as mobile phones, portable computers, digital cameras and PDA, etc. In all types of flat panel displays, active matrix liquid crystal display is the most popular type of FPD due to its higher refresh rate compared with the conventional passive matrix display [2]-[3]. Besides, LTPS-TFTs have been exhibited in a variety of industrial applications, such as active matrix liquid crystal displays (AMLCDs) [2]-[4], active matrix organic light emitting displays (AMOLEDs) [5]-[7], high density static random access

memories (SRAMs) [8], electrical erasable programming read only memories (EEPROM) [9]-[10], and 3D ICs' applications [11].

It has been known that the hydrogenated amorphous silicon (a-Si) TFTs were widely used for the pixel switching devices of AMLCDs . The advantages of a-Si:H TFTs are their thermal compatibility with low temperature process on large area glass substrates and high off-stated which results in low leakage current. However, the low electron mobility typically below $1cm^2V^{-1}sec^{-1}$ will limit the performance for AMLCD applications. Consequently, the invention of poly-Si-TFTs will suppress the limitation of a-Si:H TFTs to derive higher field effect mobility due to its larger grain size of poly-grains. The high field effect mobility and drive current of poly-Si-TFTs make it possible to use them as the switching pixels and driver circuits [12]. What's more, the aperture ratio and the panel brightness can be also prompted a lot because that there is just a small size of device needed by utilizing LTPS-TFTs [13]. Therefore, the performance of displays can be improved and thus the poly-Si -TFTs have a great potential to realize the high-performance large-area AMLCDs and system on panels (SOP). However, the low temperature process is necessary because the switch pixels are required to be embedded on the glass substrates for the applications of FPD. Generally the melting point of glass is about 660℃, so the maximum process temperature of poly-Si TFTs must be controlled below 600℃ to avoid the glass substrate melting. Furthermore, the formation of gate insulator and the dopant activation are also limited by the low-temperature process. Hence, a new low temperature process of poly-Si TFTs is needed to make the poly-Si TFTs possible to be compatible to the industrial requirements.

It has been known that the conduction mechanism of poly-Si TFTs is

strongly related to the grain boundaries between the poly-grains and the intra-granular defects in the grains. The grain boundaries consist of large amount of dangling bonds and strained bonds [14]. These imperfect bondings will trap mobile carriers in the channel and become charged to result in a high potential barrier at these locations. So the carrier mobility and subthreshold swing will be severely degraded in the poly-Si TFTs. Moreover, the grain boundaries also provide the paths of leakage current to enhance the standby power consumption. In order to obtain higher drive current and lower leakage current of LTPS-TFTs, the most import thing is to enlarge the grain size of poly-Si so that the grain boundary density will be reduced [15]. Generally speaking, growing poly-Si by low temperature chemical vapor deposition (LPCVD) will obtain the small size of poly-grains and result in a poor electrical performance of devices. However, re-crystallization of a-Si will get larger poly-grain size than growing poly-Si directly. For achieving this goal, variety methods were proposed to re-crystallize the a-Si films such as SPC (solid phase crystallization) [16]. ELA (excimer laser annealing) [17], and MILC (metal induced lateral crystallization) [18] to obtain the large grain size of poly-Si and thus enhance the field effect mobility. Apart from the method of re-crystallization of a-Si, lots of plasma treatment methods are also proposed to passivate the trap states in grain boundaries. Several plasma sources such as H_2 [19], NH_3 [20], N_2O [21] and O_2 [22] plasma have been widely investigated recently.

1.2 Poly-Si TFTs using High-k Gate Dielectrics

Low temperature polycrystalline-silicon thin-film transistors (LTPS-TFTs)

have been widely used in active-matrix liquid crystal displays (AMLCD) with integrated peripheral circuits as the pixel array on the glass substrate because of their superior performance [23]. Recently, the practicability of integrating the entire system on panels (SOP) has been proposed successfully [24]. To fulfill this goal, it requires that the display driving circuits contain LTPS-TFTs are capable of operating at low voltages while delivering high drive currents. Traditionally, we use silicon dioxide (SiO_2) as the gate dielectric materials in LTPS-TFTs. However, with the scaling down of the gate oxide thickness to obtain the higher drive current and better gate control ability, SiO_2 encounters many problems including high gate leakage current [25]. Consequently, to maintain the physical dielectric thickness while increasing the gate capacitance, the conventional SiO_2 gate dielectric layer must be replaced with a material that offers a higher dielectric constant κ than SiO_2, several new high-k materials have been proposed including Al_2O_3, Ta_2O_5 and HfO_2 [26]-[28]. Among these high-k materials, HfO_2 has been viewed as the most appropriate high−κ dielectrics for the TFTs due to its high value of κ (14 to 20) , wide band-gap (~ 5.8eV) and excellent thermal stability in contact with poly-Si [29]-[30]. Hf oxide and Hf silicate thin films, currently being considered for gate dielectric applications result in a multilayer structure that includes a SiO_2-like layer either spontaneously or intentionally formed at the interface with the substrate [31].

1.3 Negative Bias Temperature Instability of LTPS TFTs

Negative bias temperature instability (NBTI) mainly occurs in the p-channel devices. During negative bias stress at elevated temperature (typically

100℃-150℃), several important electrical parameters such as threshold voltage (V_{th}), driving current (I_D), carrier mobility and the peak transconductance (G_m) of the device will be severely degraded [32]-[33]. The degradation of these device parameters can lead to circuit failures, both for analog and digital applications.

The NBTI induced degradation is mainly attributed to interface states and fixed oxide charges and it can be thermally and electrically activated. The NBTI stress has been widely investigated in the p-channel TFTs and the reaction-diffusion (R-D) model [34]-[35] has been used to explain the phenomenon of NBTI stress in p-channel TFTs and the physical model of NBTI stress is shown in the Fig. 1.1. The NBTI-degradation mechanism of p-channel TFTs is described as follows [32]:

It is assumed that the Si dangling bonds at the poly-Si/SiO_2 interface are passivated by the hydrogen atoms in the horizontal furnace initially. During the NBTI stress, the inversion holes will react with the Si-H bonds at the poly-Si/SiO_2 interface and in the grain boundaries, and then the hydrogen atoms of the Si-H bonds become weakly bonded to the Si atoms. Thus, the hydrogen atoms can be easily released from the weak Si-H bonds by sufficient thermal energy. The release of hydrogen results in the generation of interface states and grain boundary trap states. The released hydrogen related species from the interface either diffuse or drift into the gate oxide and react with it, forming OH groups bounded to Si atoms of oxide and leaving positive fixed oxide charges behind in the gate oxide, becoming the reacting-limiting factor.

In order to clarify the mechanisms that modify the device electrical

parameters during NBTI stress, we have to understand every possible factor that contributes to the degradation of electrical parameters in TFTs. In poly-Si TFTs, unlike the fundamental theory of MOSFETs, the electrical parameters such as threshold voltage (V_{th}), subthreshold swing (S.S.) and transconductance (G_m) are all dependent on the generation of interface states and trap states at the interface and/or in the grain boundaries. Based on the degradation mechanism of poly-Si TFTs, the main degradation mechanism of the electrical parameters of poly-Si TFTs will be described as follows: The generation of fixed oxide charge and charge trapping in the gate dielectric will cause the V_{th} shift. The interface states would contribute to V_{th} shift and degrade the subthreshold swing (S.S.) and transconductance (G_m). The trap states generated in the TFTs are usually divided into two types and their effects on the electrical performance are different [36]-[37]. (1) deep trap states : Deep trap state is a type of trap states that located in the mid-gap of the silicon energy level. The deep trap states are usually caused by the dangling bonds (defects) at the HfO_2/poly-Si interface or in the grain of the poly-Si channel film. The generation of deep trap states would severely cause the V_{th} shift and degrade the subthrethold swing (S.S.) , whereas it has little effect on the transconductance (G_m) (2) tail trap states: the tail trap state is one type of trap states that located near the conduction band or the valence band edge of the silicon energy level. The tail trap states are attributed to the strained bonds at the poly-Si/IL interface or in the grain boundary trap states. The generation of tail trap states would severely contribute to the degradation of the transconductance (G_m), whereas it has little impact on the subthrethold swing (S.S.). The degradation of the electrical parameters after stress discussed above will help us to clarify the generation and distribution of defects and trap states of LTPs TFTs. These proposed mechanisms are

summarized in the Table 1.

1.4 NBTI Stress in High-κ Gate Dielectrics

It is generally recognized that HfO_2 layer has a significant larger amount of bulk traps than that in SiO_2. The presence of bulk traps complicates the mechanism of NBTI further [38]. Charge trapping characteristics of HfO_2 MOSFETs were affected by the process conditions. One factor is the thickness of the HfO_2 layer. It was observed that the charge trapping was enhanced for the thicker HfO_2 layer [39]. Charge trapping is dominant in the thick films and dominates the generation of interface traps that are formed during the stress. The oxide trapped charge at the interface between the dielectric and the substrate is recognized to make the most significant contribution to V_{th} [40]. It was also reported that the charge trapping is related to the neutral HfOH centers, indicating that the charge trapping in the HfO_2 layer is hydrogen-related [41]. Huard et al. [42] reports that the V_{th} shift contributed by charge trapping is composed of two steps: firstly, hole traps (meta-stable states) which recover, and interface states (P_{b0}) which are stable (no recovery). It was also reported that the mechanism taking place in the NBTI stress is described as follows: The hydrogen release induces interface states and the holes will be captured by the oxide traps [43]. The observed similarities between high-κ gate dielectrics and nitride silicon dioxide [43] tell us that the property of the interfacial layer between the HfO_2 and the substrate is very close to the amorphous silicon dioxide, so the mechanism of NBTI stress in SiO_2 MOSFETs will help us to understand the NBTI stress in the HfO_2 MOSFETs [43].

1.5 Mobility Issues in High-k Dielectrics

High-permittivity dielectrics, as an alternative of conventional SiO_2 gate oxide, are widely investigated in metal-oxide-semiconductor (MOS) devices for their capability to reduce gate leakage current for the same electrical capacitance [44]-[45]. Among all the candidates for high-κ gate dielectrics, Hf-based oxides, such as HfO_2 or $HfSi_xO_y$ have attracted much attention. However, there are many issues to be studied and solved for these new materials. Among the issues raised by the integration of high-κ materials, the degradation of carrier mobility for the metal gate/high-κ gate stacks remains one of the most serious issues [46]. The degradation is attributed to intrinsic properties of high-κ materials such as fixed charges induced remote coulomb scattering [47], remote surface roughness scattering [48], remote soft-optical phonon scattering (RPS) [49], interfacial dipole scattering [50] and crystallization [51].

Recently, high-κ materials are not only used in the complementary metal-oxide-semiconductor (CMOS) process but also studied in the poly-silicon thin film transistors. By using the high-κ gate dielectrics, we can preserve the physical gate-dielectric thickness while increasing the gate capacitance density and then improving the mobile carrier density in the channel region.[52]-[54] .

1.6 Motivation

As far as we know, the gate capacitance is inversely proportional to the thickness of the gate dielectrics. That is to say, the thinner gate dielectric will result in the higher peak transconductance (G_{m_max}). However, the G_{m_max} of the TFT devices using HfO_2 gate dielectrics increases with the HfO_2 thickness in our work. This phenomenon is contrary to the knowledge we had before. As a result, it is interesting and worthwhile to find out the main cause of this phenomenon.

Apart from the investigation on the electrical characteristics of the TFTs with different HfO_2 thickness, the NBTI stress is also studied to compare the reliability of the TFTs with different thickness of HfO_2 layers.

Table 1.1 Variation of electronic parameters and corresponding possible degradation mechanism and the main degraded locations.

Electrical parameters after stressing	Mainly depending on → distribution
V_{th} (threshold voltage)	charge trapping → gate dielectric fixed charge → gate dielectric interface states → HfO_2/Poly-Si interface
S.S. (subthreshold swing)	interface states → HfO_2/Poly-Si interface intra-grain defect density → poly-Si film
G_m (transconductance)	interface states → HfO_2/Poly-Si interface tail trap states → grain boundary

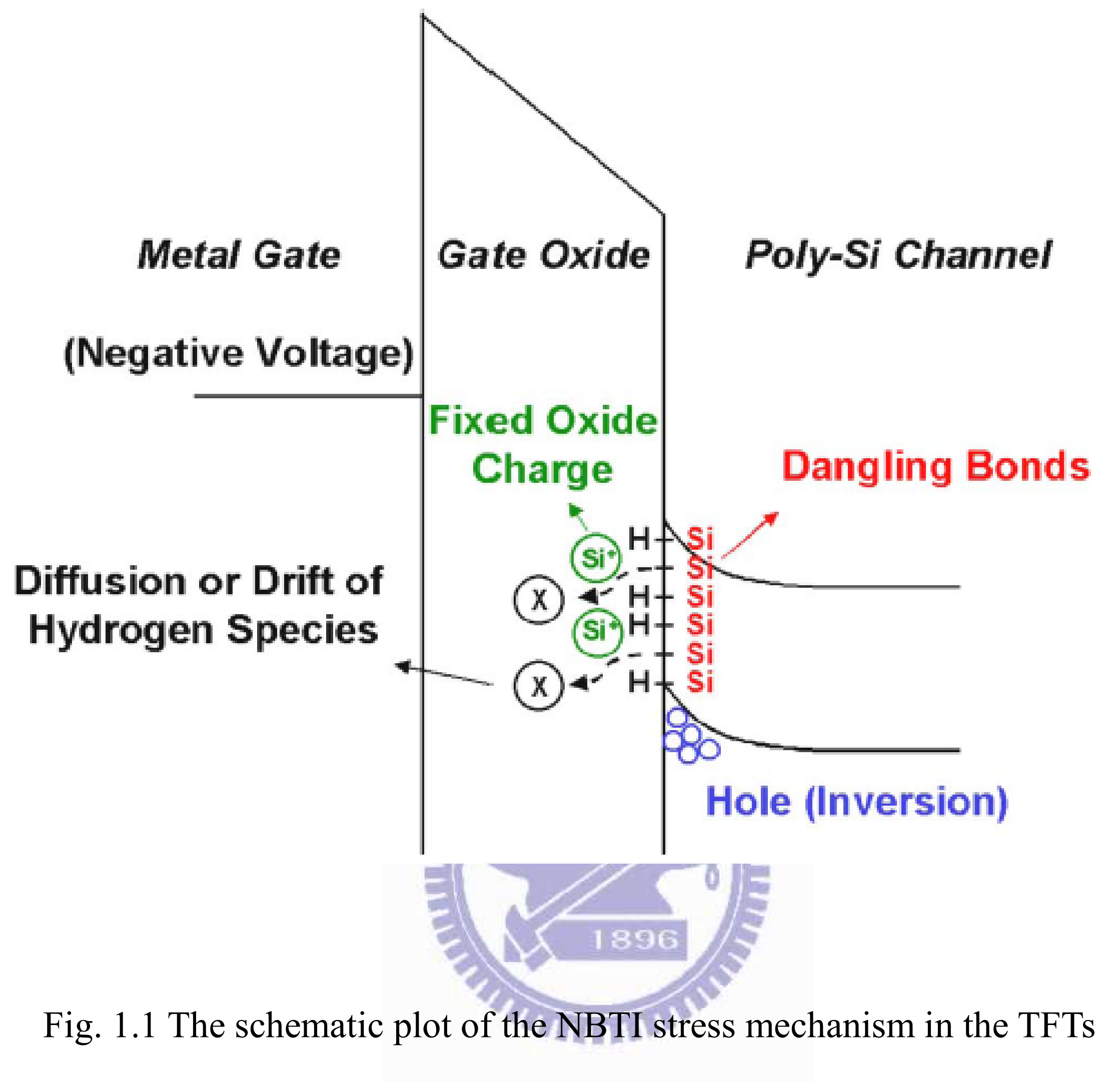


Fig. 1.1 The schematic plot of the NBTI stress mechanism in the TFTs with SiO_2 gate dielectrics [32].

Reference

Chapter 1

[1] C. H. Fa, and T. T. Jew, "The polysilicon insulated-gate field-effect transistor," *IEEE Trans. Electron Devices*, vol. 13, no. 2, pp. 290, 1966.

[2] R. E. Proano, R. S. Misage, D. Jones, D. G. Ast, "Guest-host active matrix liquid-crystal display using high-voltage polysilicon thin film transistors," *IEEE Trans. Electron Devices*, vol.38, no. 8, pp. 1781-1786, Aug. 1991.

[3] Y. Oana, "Current and future technology of low temperature poly-Si TFT-LCDs," *J. Soc. Inf. Disp.*, 9, pp. 169, 2001.

[4] S. Morozumi, K. Oguchi, S. Yazawa, Y. Kodaira, H. Ohshima, and T. Mano, "B/W and color LC video displays addressed by poly-Si TFTs," *SID Dig.*, pp. 156, 1983.

[5] M. Stewart, S. Pobert. Howell, Leo Pires, Miltiadis K. Hatalis, Webester Howard, and Olivier Prache, "Polysilicon VGA active matrix OLED displays – technology and performance," *in IEDM tech, Dig.*, 1998, pp. 871-874.

[6] Mark Stewart, Pobert S. Howell, Leo Pires, Miltiadis K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays, "*IEEE Trans. Electron Device*, vol. 48, pp. 845-851, 2001.

[7] Z. Meng and M. Wong, "Active-matrix organic light-emitting diode

displays realized using metal-induced unilateral crystallized polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 49, pp. 991-996, 2002.

[8] S. Batra, "development of drain-offset (DO) TFT technology for high density SRAM's," Extended Abstracts, vol.94-2, in *Electrochemical Soc. Fall Mtg., Miami Beach, FL*, Oct. pp. 677, 1994.

[9] M. Cao, et al., "A simple EEPROM cell using twin polysilicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 15, pp. 304, 1994.

[10] N. D. Young, G. Harkin, R. M. Bunn, D. J. McCulloch, and I. D. French, "The fabrication and characterization of EEPROM arrays on glass using a low temperature poly-Si TFT process," *IEEE Trans. Electron Devices*, vol. 43, pp. 1930-1936, 1996.

[11] K. Banerjee, S. J. Souri, P. Kapur, and K. C. saraswat, "3-D ICs: a novel chip design for improving deep-submicrometer interconnect performance and system-on-chip integration, " *Proceedings of the IEEE*, vol. 89, pp. 602-633, 2001.

[12] W. G. Hawkins, "Polycrystalline-silicon device technology for large-area electronics, " *IEEE Trans. Electron Devices*, vol. 33, pp. 477-481, 1996.

[13] I. Wu, "Cell design considerations for high-apeture-ratio direct-view and projection polysilicon TFT-LCDs," in *SID Tech. Dig*., pp. 19, 1995.

[14] S. Seki, O. Kogure, and B. Tsujiyama, "Effects of crystallization on trap state densities at grain boundaries in polycrystalline silicon, " *IEEE*

Electron Device Lett., vol. 18, no. 8, pp. 368-370, 1987.

[15] H. Kuriyama et al., “Enlargement of poly-Si film grain size by excimer laser annealing and its application on high-performance poly-Si thin film transistor,” *Jpn. J. Appl. Phys.*, vol. 30, pp. 3700-3703, 1991.

[16] W. Little, K. I. Takahara, H. Koike, T. nakazawa, I. Yudasaka, and H. Ohshima, “ Low temperature poly-Si TFTs using solid phase crystallization of very thin films and an electron resonance chemical vapor deposition gate insulator,” *Jpn. J. Appl. Phys.*, vol. 30, no. 12B, pp. 3724, 1991.

[17] H. Kuriyama, S. Kiyama, S. Nouguchi, “ Enlargement of poly-Si film grain size by excimer laser annealing and its application to high-performance poly-Si thin film transistor,“ *Jpn. J. Appl. Phys.*, vol.30, no. 12B, pp. 3700-3703, 1991.

[18] S. W. Lee and S. K. Joo,” Low temperature poly-Si thin-film transistors fabrication by metal-induced lateral crystallization,” *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 160-162, 1996.

[19] A. Yin, and S. J. Fonash, “ High-performance p-channel poly-Si TFT’s using electron cyclotron resonance hydrogen plasma passivation,” *IEEE Electron Device Lett.*, vol. 15, no. 12, pp. 502-503, 1994.

[20] C. K. Yang, T.F. Lei, C. L. Lee, “The combined effects of low pressure NH_3 annealing and H_2 plasma hydrogenation on polysilicon thin-film-transistors,” *IEEE Electron Device Lett.*, vol. 15, pp. 389-390, 1994.

[21] J. W. Lee, N. I. Lee, J. I. Kan, C.H. Han, ”Characterization of polysilicon thin-film transistor with thin-gate dielectric grown by electron cyclotron resonance nitrous oxide plasma,” *IEEE Electron Device Lett*., vol. 18, pp. 172-174, 1997.

[22] K. C. Moon, J. H. Lee, M. K. Han, “Improvement of polycrystalline silicon thin film transistor using oxygen plasma pretreatment before laser crystallization,” *IEEE Trans. Electron Devices*, vol. 49, pp. 1319, 2002.

[23] H. Oshima and S. Morozumi. “Future trends for TFT integrated circuits on glass substrates, “ in *IEDM Tech .Dig*., 1989, pp. 157-160.

[24] K. Wener, “The flowering of flat displays,” *IEEE Spectrum*, vol. 34, no. 5. pp. 40-49, May 1997.

[25] A. Takami, A. Ishida, J. Tsutsumi, T. Nishibe, and N. Ibaraki,“Threshold voltage shift under the gate bias stress in low-temperature poly-silicon TFT with the thin gate oxide film,” in *Proc. Int. Workshop AM-LCD*, Tokyo , Japan, Jul. 2000, pp. 45-58.

[26] M. Y. Um, S. K. Lee, and H. J. Kim, “Characterization of thin film transistor using Ta_2O_5 gate dielectric,” in *proc. Int. Workshop AM-LCD*, Tokyo, Japan, Jul. 1998, pp. 45-46.

[27] Z. Jin, .S. Kwok, and M. Wong, “High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators,” *IEEE Electron Device Lett*., vol. 19, no. 12, pp. 502-504, Dec. 1998.

[28] C. P. Lin, B. Y. Tsui, M. J. Yang, R. H. Huang, and C. H. Chien,

"High-Performance poly-Silicon TFTs using HfO_2 gate dielectric," *IEEE Electron Device Lett*," vol. 27. no. 5, May. 2006.

[29] C. Hobbs, H. Tseng, K. Reid, B. Taylor, L. Herbert, R. Garcia, R. Hegde, J. Grant, D. Gilmer, A. Franke, V. Dhandapani, M .Azrak, L. Prabhu, R. Rai, S. Bachi, J. conner ,S. Backer, F. Dumbuya, B. Nguyen, and P, Tobin, "80nm poly-Si gate CMOS with HfO2 gate dielectric," in *IEDM Tech. Dig*., 2001, pp. 651-654.

[30] Y. Kim, C. Lim, C. D. Young, K. Mathews ,J. Barnett ,B. Foran, A. Agarwal, G. A. Brown, G. Bersuker, P. Zeitzoff, M. Gardner, R. W. Murto, L. Larson, C. Metzner, S. Kher, and H. R. Huff, "Conventional poly-Si gate MOS transistors wit ha novel, ultra thin Hf-oxide layer," i*n VLSI Symp. Tech. Dig*., 2003, pp. 167-168.

[31] M. J. Yang, C. H. Chien, Y. H. Lu, C. Y. Shen, and T. Y. Huang,"Electrical properties of low-temperature-compatible p-channel polycrystalline-silicon TFTs using high−κ gate dielectrics," *IEEE Trans. Electron Devices*, vol. 55, no. 4, Apr. 2008.

[32] C.Y. Chen, J.W. Lee, S.D. Wang, M.S. Shieh, P.H. Lee, W.C. Chen, H.Y. Lin K.L. Yeh, T.F. Lei, "Negative bias temperature instability on low-temperature polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 53, no. 12, pp. 2993-3000, 2006.

[33] C. Y. Chen, M. W. Ma, W. C. Chen, H. Y. Lin, K. L. Yeh, S. D. Wang, T. F. Lei, "Analysis of negative bias temperature instability in body-Tied low-temperature polycrystalline silicon thin-film transistors," *IEEE*

Electron Device Lett., vol. 29, no. 2, pp. 165-167, 2008.

[34] S. Mahapatra, P. B. Kumar, and M.A. Alam, "Investigation and modeling of interface and bulk trap generation during negative bias temperature instability of pMOSFETs," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 1371-1379, 2004.

[35] A. T. Krishnan, S. Chakravarthi, P. Nicollian ,V. Reddy, S. Krishinan, "Negative bias temperature instability mechanism: The role of molecular hydrogen," *Appl, Phys, Lett.,* no. 88, 153518, 2006.

[36] I-W. Wu, Y-Y. Huang, W. B. Jackson, A. G. Lewis, and A. C. Chiang, " Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett*, vol. 12, pp. 181-183, 1991.

[37] G. A. Armstrong, S. Uppal, S. D. Brotherton, and J. R. Ayres, " Differentiation of effects due to grain and grain boundary traps in laser annealed poly-Si film transistors," *Jpn. J. Appl. Phys*.,vol. 37, pp. 1721-1726, 1998.

[38] Harris HR, Choi R, Lee BH, Young CD, Sim JH, Mathews K, Zeitzoff P, Majhi P, Bersuker G: Comparison of NMOS and PMOS stress for determining the source of NBTI TiN/HfSiON devices. In*: IRPS: 2005; San Jose Ca*; 2005: 80-83.

[39] K. Onishi, C. S. Kang, R. Choi, H-J. Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. C. Lee, „ Charging effects on reliability of HfO_2 devices with polysilicon gate electrode," in *Proc, IRPS*, 2002, pp.

419-420.

[40] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*. New York : Wiley, 1991.

[41] K. Onishi, R. Choi ,C. S. Kang , H-J. Cho, Y. H. Kim, R. E. Nieh, J. H. Siddharth, A. Kirshnan, M. S. Akbar, and J. C. Lee. "Bias-temperature instability of polysilicon gate HfO_2 MOSFETs," *IEEE, Trans, Electron Devices.*, vol. 50, no. 6, Jun. 2003.

[42] V. Huard, F. Monsieur ,G. Ribes, and S. Bruyere, "Evidence for hydrogen-related defects during NBTI stress in p-MOSFETs," in *Proc, Int. Reliability Physics Symp.*, 2003, pp. 178-182.

[43] G. Ribes, J. Mitard, M. Denais, s. Bruyeree, F. Monsieur, C. Parthasarathy, E.Vincent, and G. Ghibaudo,"Review on High−κ dielectrics reliability issues," *IEEE, Trans, Device and Materials Reliability.*, vol. 5, no. 1, Mar. 2005.

[44] M. Fischetti, "Scaling MOSFETs to the limit: A physicist's perspective," *J. Comput. Electron.*, vol. 2, no. 2-4, pp. 73-79, 2003.

[45] G. Bersuker, P. Zeitzoff, G. Brown, and H. Huff, "Dielectrics for future transistors," *Mater. Today*, vol. 7, no. 1, pp. 26-33, 2004.

[46] S. Saito, K. Torii, Y. Shimamoto, O. Tonomura, D. Hisamotom T. Onai, M. Hiratanim, S. Kiimura, Y. Manabe, M. Caymax, J. W. Maes, "Remote-charge-scattering limited mobility in field-effect transistors with SiO_2 and Al_2O_3/SiO_2 gate stacks," *J. Appl. Phys.*, Vol.

98, pp. 113706, 2005.

[47] L. A. Ragnarsson, S. Guha, M. Copel, E. Cartier, N. A. Bojarczuk, and J. Karashinski," Molecular-beam-deposited yttrium-oxide dielectrics in aluminum-gated metal–oxide–semiconductor field-effect transistors: Effective electron mobility," *Appl. Phys. Lett.*, Vol. 78, pp. 4169, 2001.

[48] S. Saito, K. Torii, Y. Shimamoto, s. Tsujikawa, H. hamamura, O. Tonomura, T. Mine, D. Hisamoto, T. Onai ,J. Yugami," Effects of remote-surface-roughness scattering on carrier mobility in field-effect-transistors with ultrathin gate dielectrics," *Appl. Phys. Lett.*, Vol. 84, pp. 1395, 2004.

[49] M. V. Fischetti, D. A. Neumayer, and E. A. Cartier," Effective electron mobility in Si inversion layers in metal–oxide–semiconductor systems with a high-κ insulator: The role of remote phonon scattering," *J. Appl. Phys.*, Vol. 90, pp. 4587, 2001.

[50] H. Ota, A. Hiranto, Y. Watanabe, N. Yasuda, K. Iwamoto, K. Akiyama, K. Okada, S. Migita, T. Nabatame, and A. Toriumi," Intrinsic origin of electron mobility reduction in high-k MOSFETs-from remote phonon to bottom interface dipole scattering-," in *VLSI Symp. Tech. Dig.*, pp. 65-68, 2007.

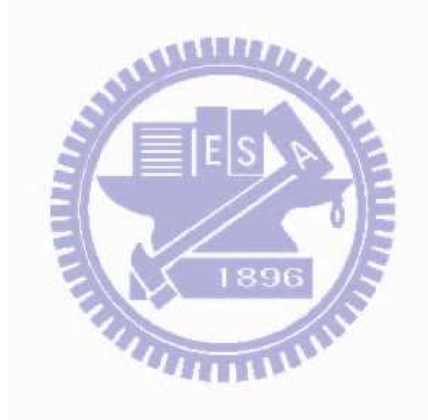
[51] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima,"Additional scattering effects for mobility degradation in Hf-silicate Gate MISFETs," in *IEDM Tech. Dig.*, p.621, 2002.

[52] C. P. Lin, B. Y. Tsui, M. J. Yang, R. H. Huang, C. H.

Chien," High-performance poly-silicon TFTs using HfO_2 gate dielectric," *IEEE Electron Device Lett.*, vol. 19, no. 12, pp. 502-504, Dec. 1998.

[53] B.F. Hung, K.C. Chiang, C. C. Huang, A. Chin, S.P.McAlister,"High-performance poly-silicon TFTs incorporating $LaAlO_3$ as the gate dielectric," *IEEE Electron Device Lett*., Jun, vol. 26, no. 6, pp. 384-386, 2005.

[54] T. M. Pan, C. L. Chan, T. W. Wu," High-performance poly-Silicon TFTs using a High−κ $PrTiO_3$ gate dielectric," *IEEE Electron Device Lett*., vol. 30.



Chapter 2

Experimental Details and Method of Parameter Extraction

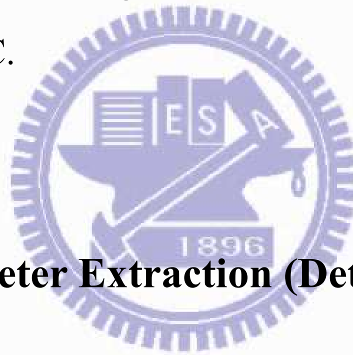
2.1 Device Fabrication

As shown in the Fig 2.1, the fabrication of the device was started by depositing a 50nm-thick un-doped amorphous Si (a-Si) layer at 550℃ by low pressure chemical vapor deposition (LPCVD) on the Silicon substrate which was capped with a 500nm-thick thermal oxide layer. Then the a-Si layer was re-crystallized to poly-silicon channel film by the SPC process at 600℃ for 24hr in a N_2 ambient. The source and the drain regions were implanted with boron for p-channel TFTs (15keV at $5x10^{15}cm^{-2}$). Then the S/D regions were activated at 600℃ for 24hr annealing in a N_2 ambient. After the implantation of S/D regions, a 500nm-thick TEOS oxide was deposited on the poly-Si channel film at 700℃ by the LPCVD system for the device isolation. Then the TEOS oxide film was patterned and then etched to be the field oxide for the active region formation. For the HfO_2-TFTs, the 175Å, 415Å and 745Å-thick HfO_2 films were deposited by the electron-beam evaporator system at room temperature and the process pressure of 10^{-5} torr. Then all the samples were annealed in the horizontal furnace with O_2 at 400℃ for 0.5hr to improve the quality of the gate dielectrics. After the patterning of the contact holes, aluminum (Al) was deposited by the electron-beam system at room temperature and $5x10^{-7}$ base pressure as the gate electrodes and the S/D contact pads. Finally, the TFT devices were finished by the definition of source, drain and gate contact pads. All the fabrication

processes were shown in the Fig. 2.1.

2.2 Measurement

The NBTI tests are performed on 10μmx10μm p-channel TFTs with HfO_2 thickness of 175, 415 and 745Å, with source and drain grounded during the stress. The samples are stress at a constant voltage for 1000 seconds. The threshold voltage (V_{TH}) and the transconductance (G_m) are extracted using I_d-V_g sweeps performed during periodic interruptions of the stress. Measurements are performed at various stress voltages and 2 different temperature – Room temperature (RT) and 125°C.



2.3 Method of Parameter Extraction (Determination of Thresholod Voltage)

Threshold voltage V_{th} is one of the most important electrical parameter of semiconductor. However, the precise threshold voltage of the device is difficult to define. Therefore, several methods have been proposed to extract the V_{th} of different kinds of devices. In MOSFETs, there are two common methods for the determination of V_{th}. One of them is the linear extrapolation method with the drain current measured at a drain voltage of 50~100mV to make sure the operation in the linear regime. According to the ideal I_d-V_g relation in the linear regime:

$$I_d = \mu_{eff} C_{ox} (\left(\frac{W}{L}\right)[(V_{GS} - V_{th}) - \frac{1}{2}(V_{DS} - I_D R_{SD})](V_{DS} - I_D R_{SD}) \quad (2.1)$$

$$\cong \mu_{eff} C_{ox} \left(\frac{W}{L}\right)[V_{GS} - V_{th} - \frac{1}{2} V_{DS}](V_{DS}) \quad (2.2)$$

It is worthy to note that the equation (2.2) is only valid as the series resistance is negligible such as source and drain resistance R_{SD}, which usually can be ignored at a low drain current and low drain bias. It is a common practice to find the point of the maximum slope of the I_d-Vg curve (G_{m_max}) and fit a straight line to I_d=0 from this point. According to the equation (2.2), we can obtain a V_G point which is corresponding to I_d=0. Hence, the V_{th} defined by the extrapolation method is :

$$V_{th} = V_{GS} - \frac{V_{DS}}{2} \quad (2.3)$$

In this work, V_{th} is defined by the other method which is different from the above description. We make use of a more simple way which is called constant drain current method. This method is utilized in almost every paper in the TFT field. The V_{th} derived by this way is close to the V_{th} obtained from the extrapolation method. Here, the V_{th} is defined as the point at V_{DS}= | 0.1V | where the drain current I_d=(W/L)*100nA for n and p channel, where the W and L are the channel width and the channel length respectively. In this paper, devices were all measured in the size of W=10μm and L=10μm. Thus the V_{th} is defined as the gate voltage where the drain current $I_d=1*10^{-7}$ A in all of our discussions.

2.3.1 Determination of subthreshold swing

Subthreshold slope (S.S.) is a typical parameter to describe the gate control ability, which reflects how fast the device can be switched from off state to on state. It is defined by the amount of the gate voltage needed to increase or decrease the drain current by one order of magnitude. The S.S should be independent of gate voltage and drain voltage. However, the S.S. of a device is usually affected by the various degradation effects such as charge sharing, avalanche multiplication and punchthrough effect. The S.S. is usually related to the undesirable and inevitable phenomenon such as series resistance and interface states. In LTPS TFTs, the S.S. is also dependent on the trap state in the grain boundaries. It has been reported that the the S.S is strongly related to the trap states near the mid-gap (deep energy level), which is originated from the dangling bonds [1], besides, the low temperature process of the LTPS-TFTs will result in a poor interface between the gate dielectrics and the channel films. Briefly speaking, the bulk trap states and interface states will degrade the S.S. of LTPS-TFTs.

The formula of subthreshold slope was defined as :

$$S.S. = [\frac{\partial(\log I_{DS})}{\partial(V_{GS})}]^{-1} \quad \ldots\ldots\ldots\ldots \quad \ldots\ldots\ldots\ldots\ldots(2.4)$$

2.3.2 Determination of on/off current ratio

On/off drain current ratio is other important parameters of TFT devices. High On/off ratio reflects not only the high on current but a small off current (or

leakage current). In TFTs, the on/off drain current ratio of six orders is required for the applications of AMLCDs.

In this paper, the on current is defined as the point at a fixed drain bias of 0.1V where the drain current is at a maximum of the I_d-V_g curve. The off current is defined as the point at a fixed drain bias of 0.1V where the drain current is at a minimum. Therefore, the on/off drain current ratio can be derived by the following formula:

$$I_{on}/I_{off} = \left. \frac{I_{d_max}}{I_{d_min}} \right|_{V_d = 0.1V} \quad \text{.................................(2.5)}$$

2.3.3 Determination of field effect mobility

The field effect mobility (μ_{FE}) is usually determined from the maximum value of transconductance (G_m) at a low drain bias. The drain current in the linear region ($V_{DS} < V_{GS}-V_{th}$) can be approximated as the following equations :

$$I_{DS} = \mu_{FE} C_{ox} (\frac{W}{L}) \left[(V_{GS} - V_{th}) V_{DS} - \frac{1}{2} V_{DS}^{\ 2} \right] \text{......... ....(2.6)}$$

where W and L are the channel width and the channel length, respectively；C_{ox} is the gate oxide capacitance per unit area and V_{th} is the threshold voltage. Thus, the transconductance is given by the differential equation:

$$G_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{FE} C_{ox} (\frac{W}{L}) V_{DS} \text{.................. ....(2.7)}$$

Therefore, the field-effect mobility is defined as follows:

$$\mu_{FE} = \left. \frac{G_{m_\max}}{C_{ox}(\frac{W}{L})V_{DS}} \right|_{V_{DS}\to 0} \quad \text{.............................(2.8)}$$

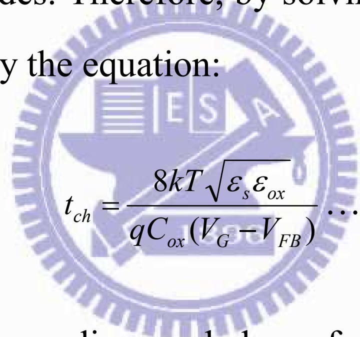
2.3.4 Determination of the trap state density

In LTPS-TFTs, the trap state density (N_t), which originates from dangling bonds or strained bonds located in the grain boundaries of poly-Si films. The trap state in the channel region will trap free carriers and result in potential barrier height V_B to degrade the carrier transportation like the degradation of the field-effect mobility (μ_{FE}), higher threshold voltage (V_{th}), subthreshold swing (S.S.) and leakage current. Therefore, the grain boundary trap state density is an important parameter that affects the electrical transport properties significantly of poly-Si films. Therefore, it is necessary to extract the trap state density in the channel film. Many researchers have investigated the electrical characteristics and the carrier transport mechanism in the poly-Si TFTs. Among the lots of grain boundary trap state-extraction method, The trap state density is usually derived by the Lenvinson and Proano method [2][3]. And the method is described as follows:

By modifying the mobility μ_b and replacing the dopant concentration with gate induced charge density N_G, the corrected expression of the transfer characteristics (I_D-V_G) at low drain voltage in the poly-Si films is very similar with that in the regular MOSFET's. It is expressed as:

$$I_D = \mu_0 C_{ox}(\frac{W}{L})(V_G - V_{th})V_D \exp(-\frac{q^3 N_t^2 t_{ch}}{8kT\varepsilon_s C_{ox}(V_G - V_{th})}) \quad \text{......................(2.9)}$$

The equation above was modified by Proano et al [3]. It is found that the behavior of the carrier mobility under low gate bias can be expressed more accurately by using the flat-band voltage V_{FB} instead of the threshold voltage (V_{th}). The flat-band voltage V_{FB} is defined as the gate voltage which corresponds to the minimum drain current. Furthermore, Lenvinson et al. [2] assumed that the channel thickness t_{ch} is constant and equal to the thickness of the poly-Si film $t_{poly\text{-}Si}$. This simplified assumption is acceptable only for the very thin film ($t_{poly\text{-}Si}$), which is not applicable to the common thickness for the poly-Si TFTs. As a result, a better approximation for the channel thickness t_{ch} in an undoped poly-Si film is given by defining the channel thickness as the thickness at which 80% of the total charge resides. Therefore, by solving the Poisson' equation, the channel thickness is given by the equation:



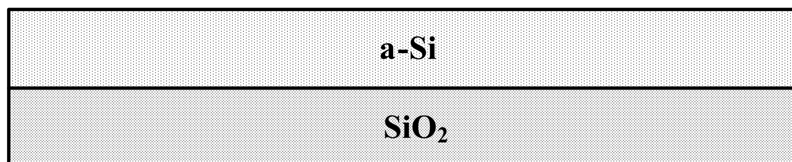
$$t_{ch} = \frac{8kT\sqrt{\varepsilon_s \varepsilon_{ox}}}{qC_{ox}(V_G - V_{FB})} \quad \text{..........................(2.10)}$$

Substituting the modified terms discussed above for the equation (2.9), thus the drain current I_D can be expressed as the following equation:

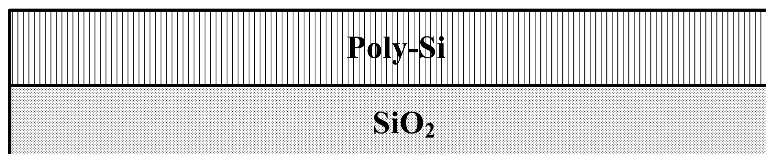
$$I_D = \mu_0 C_{ox}(\frac{W}{L})(V_G - V_{FB})V_D \exp(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{ox}/\varepsilon_s}}{C_{ox}^2 (V_G - V_{FB})^2}) \quad \text{..............(2.11)}$$

According to the equation (2.11), we can extract the trap state density (N_t) from the slope of the curve $\ln[I_D/(V_G\text{-}V_{FB})]$versus $(V_G\text{-}V_{FB})^{-2}$. the effective grain boundary trap state density N_t can be determined from the square root of the slope described as follows:

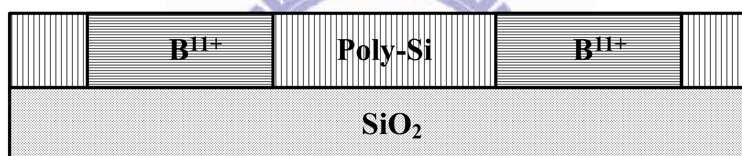
$$N_{trap} = \frac{C_{ox}}{q}\sqrt{|slope|} \quad \text{................................(2.12)}$$



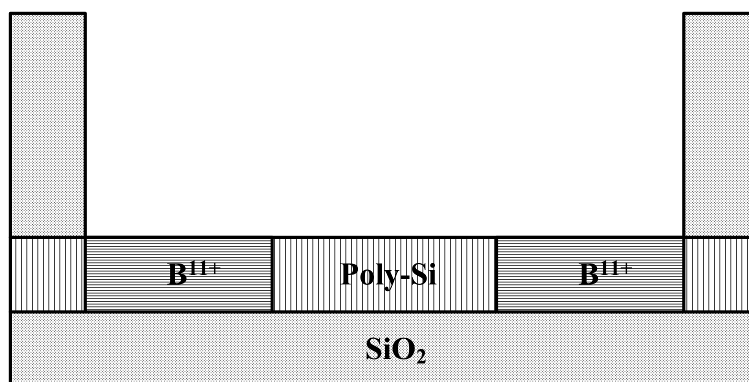
(a) Thermal oxidation and an amorphous Si (α-Si) film was deposited by LPCVD.



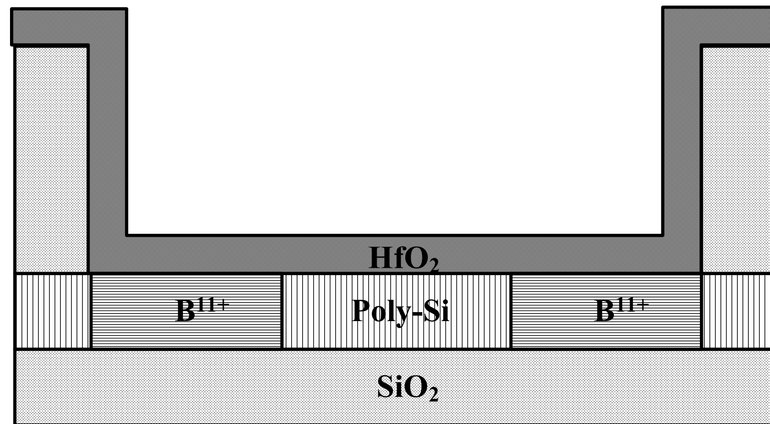
(b) The α-Si film was crystallized into the poly-Si film by SPC at 600℃ for 24hr.



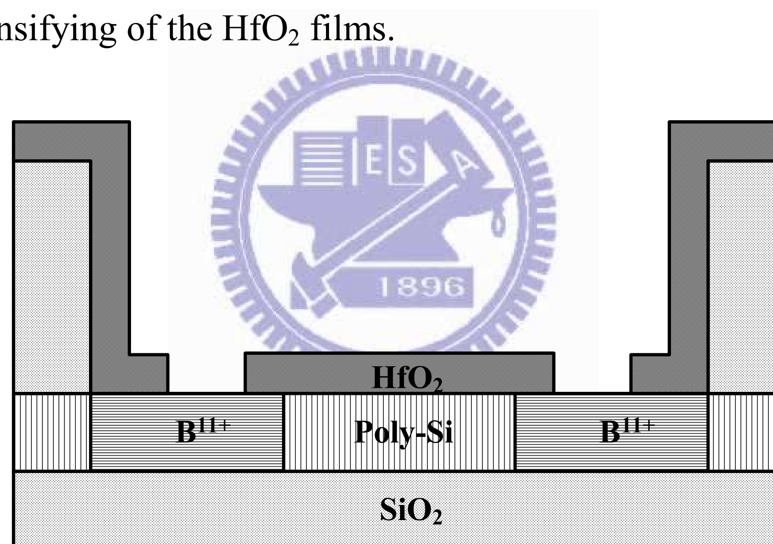
(c) The source and drain regions (S/D) were implanted with boron and then activated at 600℃ for 24hr.



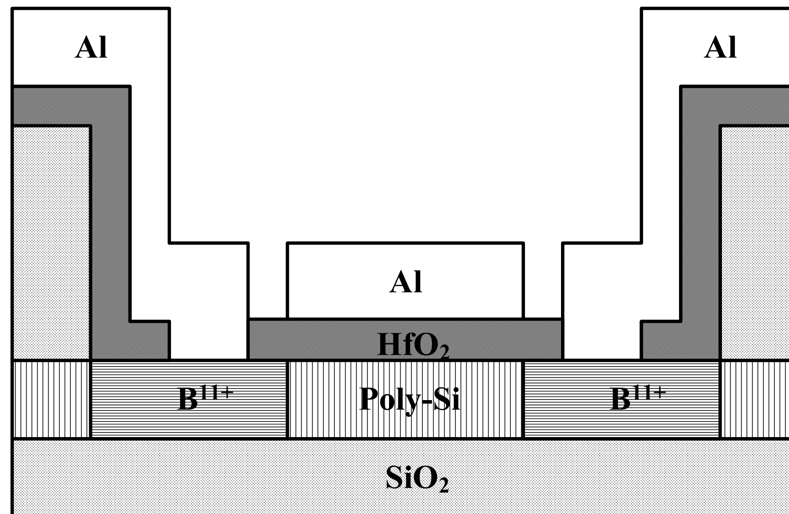
(d) TEOS SiO_2 was deposited as the field oxide and the active region was defined.



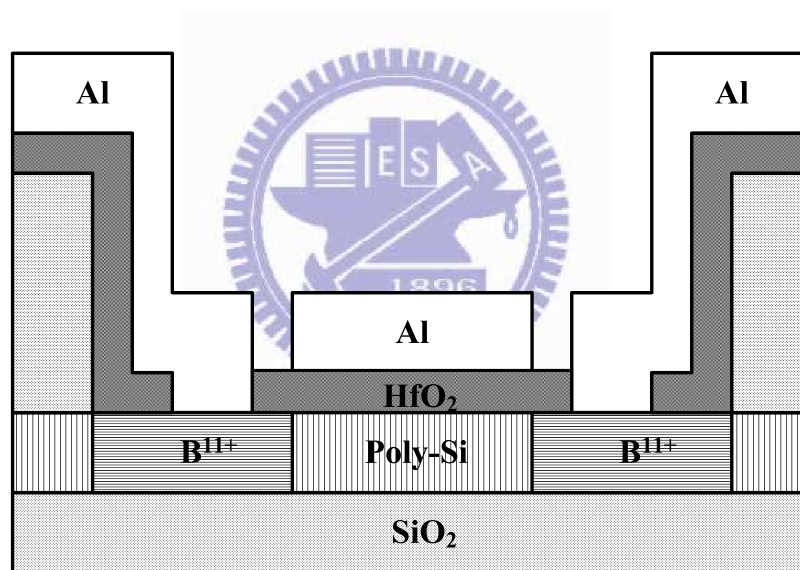
(e) The HfO_2 films with the thickness of 175Å, 415Å and 745Å were deposited by the e-beam evaporator as the gate dielectrics. Post deposition anneal (PDA) was performed at 400℃ in the O_2 ambient for the densifying of the HfO_2 films.



(f) S/D Contact holes were defined and opened.



(g) Aluminum films were deposition by the e-beam evaporator as gate electrodes and the gate and S/D regions were defined and opened.



(h) The HfO_2-TFT Devices are sintered at 400℃ for 30 min in a N_2 ambient.

Fig. 2.1 The device fabrication of the HfO_2-poly-Si TFTs.

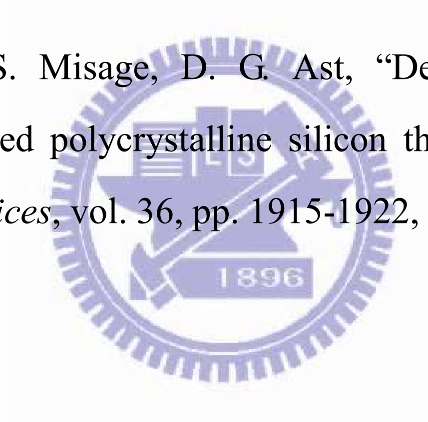
Chapter 2

Reference

[1] I-W. Wu, Y-Y. Huang, W. B. Jackson, A. G. Lewis, and A. C. Chiang, " Passivation kinetics of two types of defects in polysilicon TFT by plasma hydrogenation," *IEEE Electron Device Lett*, vol. 12, pp. 181-183, 1991.

[2] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, " Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys,* vol. 53, pp.1193-1202, 1982.

[3] R. E. Proano, R. S. Misage, D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 1915-1922, 1989.



Chapter 3

Electrical Characteristics of the p-channel LTPs TFTs with Different Thickness of High-κ Gate Dielectrics

3.1 Electrical Characteristics

In this work, several possible mechanisms that contribute to the degradation or the enhancement of the peak transconductance (G_{m_max}) are systematically investigated and a new model is firstly proposed to explain the enhanced G_{m_max} for the TFTs with the thicker HfO_2 gate dielectrics.

Fig. 3.1 (a) shows the transfer characteristics (I_D-V_G) of the poly-Si TFTs with HfO_2 gate dielectrics, which had physical thickness of 250, 500, 700, 1000 and 1700Å, respectively. It is surprisingly that the value of the peak transconductance (G_{m_max}) increases with the thickness of the HfO_2 layer. To further confirm this phenomenon, we have measured and extraccted five values of G_{m_max} and calculated the average of them of each sample with different HfO_2 thickness as shown in the Fig. 3.1 (b). We found that the same trend is observed clearly. Considering the instability of the fabrication process, this phenomenon may be due to some errors in the fabrication process. Thus, to make sure the repeatability of this phenomenon, we performed the second run of the poly-silicon TFTs with different thickness of the HfO_2 layers, which had physical thickness of 175, 415 and 745Å, respectively. The transfer characteristics (I_D-V_G) of the poly-Si TFTs with 175Å to 745Å-thick HfO_2 gate dielectrics before and after sintering are shown in the Fig. 3.2 (a) and (b),

respectively. As shown in the Fig. 3.2 (a), the G_{m_max} of the 175Å and the 415Å sample (TFTs with 175Å, 415Å and 745Å-thick HfO_2 layer are called 175Å, 415Å and 745Å sample for short thereafter in this paper) are nearly the same but are much smaller than that of the 745Å sample before sintering, whereas the value of G_{m_max} increases with the HfO_2 thickness after sintering of TFT devices at 400℃ for 30 minutes in a N_2 ambient. To further confirm this phenomenon, we also measured and extracted five values of G_{m_max} of each device with different thickness of HfO_2 and calculated the average of them. We found that the same trend is also shown in the Fig. 3.2 (c). The Figure 3.2 (d) shows the G_{m_max} dependence of temperature. We found that the G_{m_max} still increases with the HfO_2 thickness even at high temperature of 100℃ and therefore we can rule out the contribution of the remote phonon scattering that degrades the field effect mobility of the TFTs with the thin HfO_2 layer. The measured as well as the extracted device parameters before and after sintering are summarized in the Table 2.1 (a) and (b). It is proved that the phenomenon that the G_{m_max} increases with the HfO_2 thickness is repeatable. As far as we know, the field effect mobility (μ_{FE}) is proportional to the value of the G_{m_max} versus the gate capacitance density (C_{ox}). What's more, the gate capacitance density is inversely proportional to the thickness of the gate dielectrics, that is to say, a smaller gate capacitance density will be obtained for a thicker gate dielectric film. As a result, it is suggested that the field effect mobility increases with the thickness of the HfO_2 layer more significantly if the G_{m_max} is divided by the gate capacitance. Based on the knowledge we had before, the grain boundary potential barrier height in the channel region is reduced with the increasing free carrier density during the strong inversion. Because the larger gate capacitance will result in the

larger amount of the inversion carrier density, the larger field effect mobility should be derived for the thinner HfO_2 layers. However, the field effect mobility increases with the thickness of the HfO_2 layer, it is probably due to either the degradation mechanism contributes to the lower field effect mobility of the 175Å sample or some mechanism leads to the higher field effect mobility of the 415Å and the 745Å sample.

Before the discussion, we predicted that the amount of the fixed charges and the bulk traps both increase with the thickness of the HfO_2 films because it is more difficult for oxygen to passivate the fixed charges and the interface states in the thicker HfO_2 films at the PDA step in an O_2 ambient. As a result, G_{m_max} should decrease with the increasing thickness of the HfO_2 layer if the fixed charge induced remote Coulomb scattering dominates the degradation of the G_{m_max}. However, the fact that the G_{m_max} increases with the thickness of the HfO_2 layer indicates that it is reasonable to rule out the contribution of the remote Coulomb scattering that degrades the G_{m_max} degradation of the TFTs with the thin HfO_2 layer. In addition, the remote surface roughness scattering can also be neglected because the HfO_2 layers are too thick (>175Å) to result in the remote surface roughness scattering.

3.2 Material Analysis

In what as follows, we will investigate the G_{m_max} degradation of the HfO_2 poly-Si TFTs in terms of three degradation mechanisms by a series of material analysis including X-ray diffraction (XRD) for detecting the crystallization of the HfO_2 layer, source/drain sheet resistance, Atomic force microscopy (AFM) for detecting the surface roughness scattering.

3.2.1 Crystallization

It was reported that the crystallization of the high-k film has an important role on the mobility degradation [1]. Hence, the crystallization of the HfO_2 films may be one of the main causes of the phenomenon that the values of G_{m_max} increase with the increasing HfO_2 thickness. Therefore, the X-ray diffraction patterns were performed for the HfO_2 films with the thickness of 175Å, 415Å and 745Å as shown in the Fig. 3.3 (b) to (d). With the reference of the XRD spectra presented by the previous research as shown in the Fig. 3.3 (a) [2], the Fig. 3.3 (a) shows the peak positions and the intensities for crystalline HfO_2 from the powder diffraction ICDD card files. We can see that the three resolved peaks of (111), (220), (311) in the Fig. 3.3 (a) correspond to the peak positions of the monoclinic phase. Consequently, it means that there is a phase change of the 175Å-thick HfO_2 in which an amorphous phase transforms to a polycrystalline film in the monoclinic phase, whereas the XRD pattern of the 415Å and 745Å-thick HfO_2 sample shows primarily the broad maxima characteristics of an amorphous sample, with a very weak peak near $2\theta = 30.4°$. This may indicate a very small crystalline fraction in the orthorhombic or tetragonal phase [2]. It has been widely reported that the fraction of crystallization depends on the thermal budget. That is, the crystallinity of the Hf-based films was enhanced by increasing the thermal budget [3]. As a result, when the thickness of the film gets thicker, the more thermal budget is required for the crystallization. That's why the 415Å and 745Å-thick HfO_2 film didn't show the obvious phase change like the 175Å-thick sample. As a result of the crystallization, the charges trapped in the grain boundaries or the crystal/amorphous boundaries will strongly degrade the carrier mobility due to

the additional coulomb scattering [1]. Because the degradation of G_{m_max} by phase change is reduced upon the increasing thickness of the HfO_2 gate dielectric films, the G_{m_max} of the 175Å is smaller than that of the 415Å and the 745Å sample even if the 175Å sample has the higher gate capacitance density.

3.2.2 Surface roughness scattering

It was reported that the roughness of the channel surface will degrade the carrier mobility at high electric field. Therefore, it is necessary to investigate the roughness of the channel surface to find the main reason that dominates the values of the G_{m_max} in our experiment. For this reason, we performed the atomic-force microscopy (AFM) plots of the poly-silicon channel surface of the thick (1700Å) and the thin (250Å) HfO_2 TFTs after removing the aluminum gates. As shown in the Fig. 3.4 (a) and (b), the mean surface roughness of the 250Å and the 1700Å samples are 0.33 and 0.43nm, respectively. The little difference of the surface roughness between the thin and the thick HfO_2 poly-Si TFTs is speculated to have negligible impact on the values of G_{m_max}.

3.2.3 Source/Drain sheet resistance

To find out the main reason why the values of G_{m_max} increase with the increasing HfO_2 films, the source/drain sheet resistance is also necessary to be considered because the transconductance is close related to the source/drain sheet resistance ($R_{S/D}$), and the relationship between them is described as follows:

$$G_{m_max}' = G_{m_max} / (1 + G_{m_max} R_{S/D})$$
$$\Rightarrow G_{m_max} = G_{m_max}' (1 + G_{m_max} R_{S/D})$$
$$\Rightarrow G_{m_max} = G_{m_max}' (1 - G_{m_max}' R_{S/D}) \qquad \text{.................. (1)}$$

As shown in the Fig. 3.5 (a) to (c) and Table 3.2, we extracted the source/drain sheet resistance of the TFTs with the 175Å, 415Å and 745Å-thick HfO_2 films. We can see clearly that the $R_{S/D}$ decrease with the increasing HfO_2 thickness. Fig. 3.6 (a) and (b) show the cross-sectional transmission electron microscopy (TEM) of the TFTs with HfO_2 gate dielectric of 250Å and 1700Å, respectively. It is found that the thickness of the poly-Si channel film decreases with the thickness of the HfO_2 layer. As far as we know, the resistance is inversely proportional to the area that the drain current passes through. Therefore, it is suggested that it may be attributed to the consumption of Si atoms. The oxygen atoms in the HfO_2 layer may react with the Si atoms at the poly-Si/HfO_2 interface to form a thin silicate $HfSiO_x$ or a SiO_x interfacial layer. It is easier for oxygen atoms to diffuse into the HfO_2/poly-Si interface of the thin HfO_2 layer to react with the Si atoms in the channel surface. Consequently, the interfacial layer between the HfO_2 and the poly-Si layer may increase with the decreasing HfO_2 layer and thus the consumption of the Si atoms will be enhanced with the thin HfO_2 layer.

3.3 Oxygen Vacancy Induced Voltage Drop across the HfO_2 Layer

Generally, the defects in HfO_2 are speculated to be intrinsic in nature, specifically positively charged oxygen vacancies [4]-[5]. This phenomenon is based on the observation of the variations of the silicon bend bending with

varying oxygen impurities during annealing [6]. It is also found that the flat-band voltage (V_{fb}) shift toward positive as annealing at higher partial pressure of oxygen due to the decrease of positive charges. The positively charged oxygen vacancy generation mechanism is described as follows [7]:

It is well known that dissolved oxygen in the metal electrode acts as the source of oxygen for the growth of the interfacial silicon oxide layer and that the overlying metal oxide layer mediates atomic oxidation of the silicon. We view the process of oxygen transfer and the subsequent interfacial oxide layer growth as a sequence of the following steps and the mechanism is shown in the Fig. 3.7. [7]: (1) transfer of the oxygen atoms from the O_2 ambient to an oxygen site (O_0) in the metal oxide by annihilation of an oxygen vacancy (V_O), $V_O^{2+}+2e+1/2O_2=O_O^0$ or $V_O^0+1/2O_2=O_O^0$, depending on whether the vacancy is charged or neutral; (2) migration of the oxygen atom by vacancy exchange to the metal oxide/SiO_2 interface; (3) transfer of atomic oxygen from the metal oxide into the SiO_2 layer with the return of an oxygen vacancy to the metal oxide and oxidation of the overlying silicon, $1/2Si+O_O^0=[V_O^0$ or $(V_O^{2+}+2e)]+1/2\ SiO_2$, here the superscripts “0” and “2+” represents the neutral or doubly charged species. The neutral oxygen vacancy V_O^0 can behave as electron donors in oxide, and its energy level is at 3.8eV above the valence band of HfO_2 [5] and the doubly charged oxygen vacancy V_O^{2+} is located at 0.8eV below the conduction band of the HfO_2. The oxygen vacancies that are positively charged can contribute to the voltage drop across the metal oxide-dielectric layer. Therefore, it is concluded that the positively charged oxygen vacancy V_O^{2+} really exist in the HfO_2/poly-Si interface, and we believed that these charged defects will play an important role on the G_{m_max} of the TFTs with HfO_2 gate dielectrics.

As shown in the Fig. 3.8, it is the band diagram along the poly-Si channel

direction as the channel is in the inversion state of the p-channel TFTs. There are several potential barrier heights at the grain boundaries in the channel region. These potential barrier heights will impede the transport of the mobile carrier and degrade the field effect mobility. However, if there are charged defects like V_O^{2+} which is very close to the channel surface, these charged defects will lower the potential barrier heights that mobile holes see. Thus, the G_{m_max} and the field effect mobility will be enhanced due to the lowering of the potential barrier height. Because it is easier for oxygen atoms to diffuse into the HfO_2/poly-Si interface to passivate the oxygen vacancies. As a result, the thicker HfO_2 film is better for the oxygen transfer in the HfO_2 layer and thus induces more positively charged oxygen vacancies; and it is consistent with the fact that the threshold voltage increases with the HfO_2 thickness after sintering in our experiment due to larger voltage drop across the thicker HfO_2 film. This point of view can be used to well explain the phenomena that the G_{m_max} increase with the increasing HfO_2 thickness.

In conclusion, the main cause of the phenomenon that the G_{m_max} of the HfO_2-TFTs increases with the HfO_2-thickness can be divided into two parts: (1) Crystallization contributes to the field effect mobility degradation of the TFTs with thin HfO_2 layer. Because enough thermal budget is required to crystallize the HfO_2 films, the thick HfO_2 layer may remain the amorphous phase even if the thin HfO_2 layers have been fully crystallize into the polycrystalline phase. As a result, the field effect mobility degradation of the TFTs with thin HfO_2 gate dielectric is attributed to the additional coulomb scattering resulted from the charges at the grain boundaries or the crystal/amorphous boundaries. (2) Positively charged oxygen vacancy induced grain boundary potential barrier height lowering of the p-channel TFTs: the positively charged oxygen vacancies

resulted from the oxygen transfer from the O_2 ambient to the HfO_2/poly-Si interface will induce a voltage drop across the HfO_2 layer, which will lower the grain boundary barrier height of the p-channel TFTs and thus enhance the field effect mobility of the HfO_2-TFTs, With the larger amount of oxygen vacancies in the thicker HfO_2 layer, the enhancement of the field effect mobility will be intensified so that the field effect mobility increases with the thickness of the HfO_2 layer.

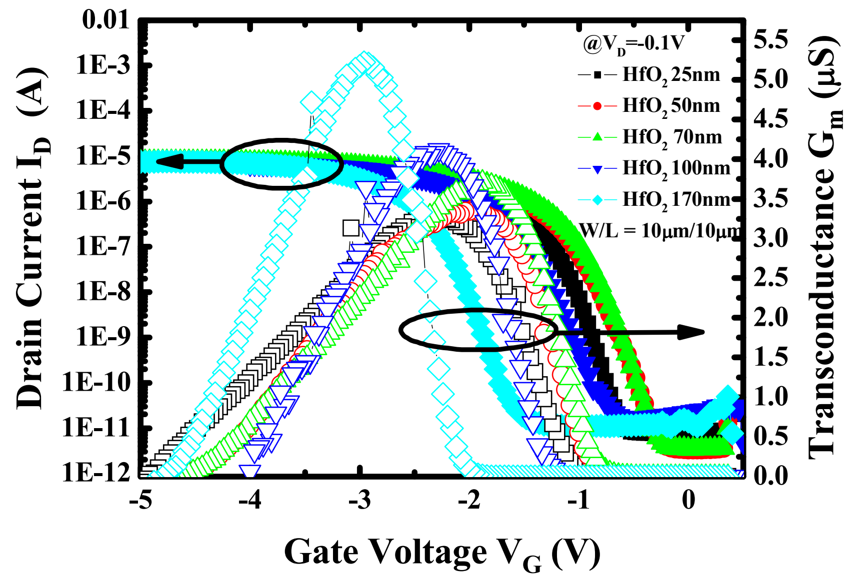


Fig. 3.1 (a) The transfer characteristics of the TFTs incorporating HfO_2 gate dielectrics after sintering of the first run, which had physical thickness of 250Å, 500Å, 700Å, 1000Å and 1700Å, respectively.

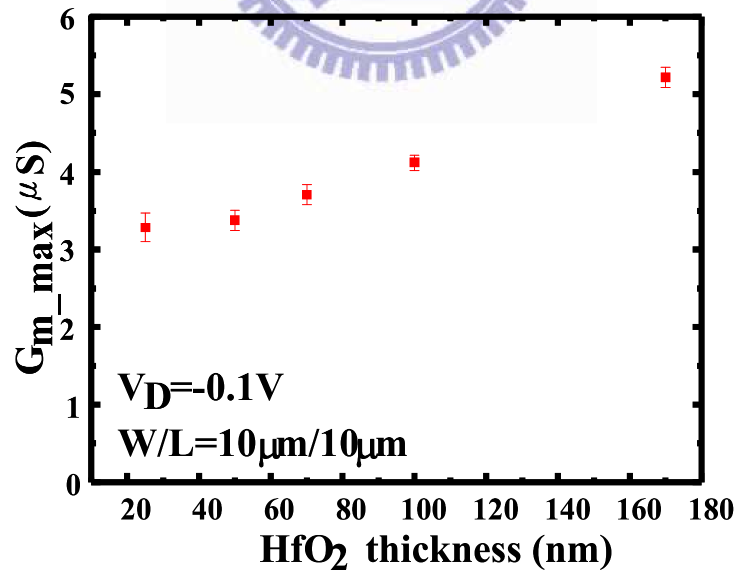


Fig. 3.1 (b) The peak transconductance (G_{m_max}) increases with the thickness of the HfO_2 layer in the first run.

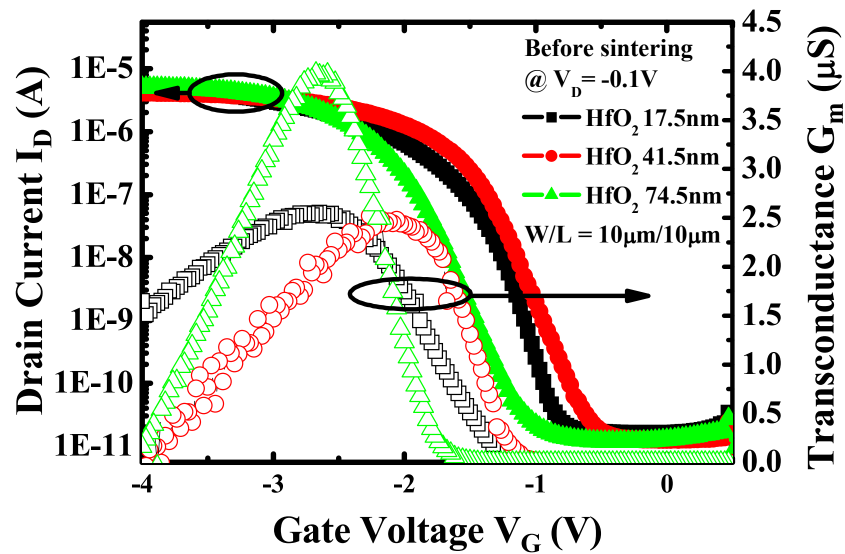


Fig. 3.2 (a) The transfer characteristics of the TFTs incorporating HfO_2 gate dielectrics before sintering at 400℃ in a N_2 ambient of the second run, which had physical thickness of 175Å, 415Å and 745Å, respectively.

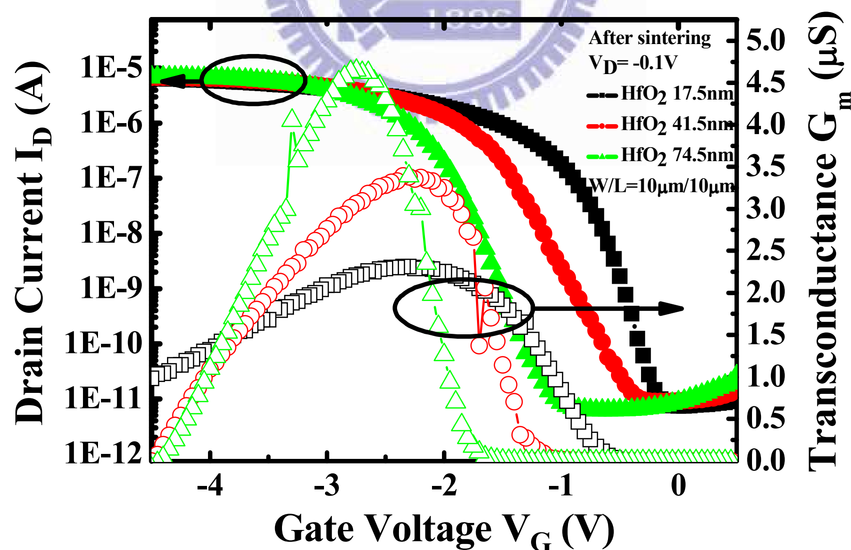


Fig. 3.2 (b) The transfer characteristics of the TFTs incorporating HfO_2 gate dielectrics after sintering at 400℃ in a N_2 ambient of the second run, which had physical thickness of 175Å, 415Å and 745Å, respectively.

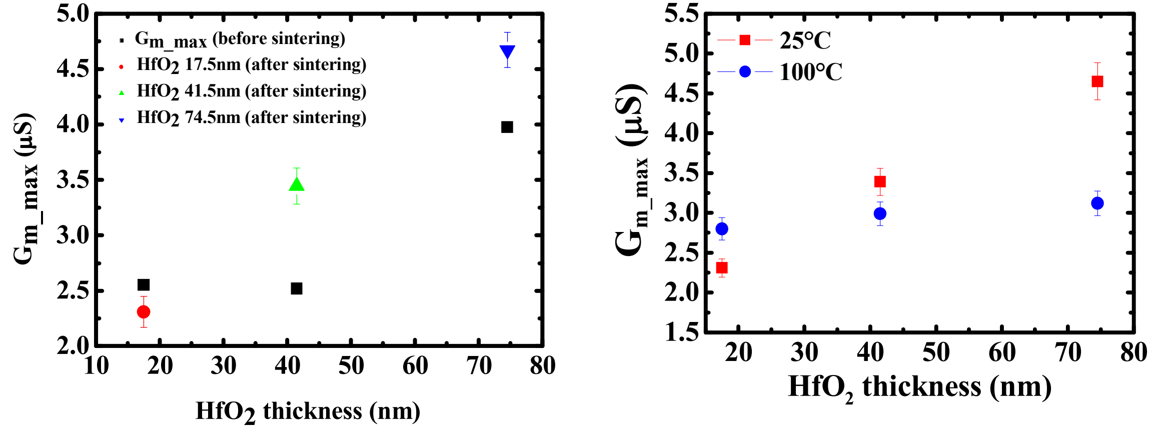


Fig. 3.2 (c) The peak transconductance (G_{m_max}) increases with the thickness of the HfO_2 layer after sintering in the second run. (d) temperature dependence of the G_{m_max}, it is obvious that the G_{m_max} still increases with the HfO_2 thickness even at high temperature of 100℃.

Table 3.1(a) The electrical parameters of the TFTs incorporating HfO_2 gate dielectrics before sintering.

Gate dielectric	V_{TH} (V)	S.S. (mV/dec)	G_{m_max} (μS)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
HfO_2 17.5nm	-1.52	155.90	2.55	5.27×10^{-6}	1.61×10^{-11}	3.28×10^{5}
HfO_2 41.5nm	-1.37	200.53	2.52	4.10×10^{-6}	1.21×10^{-11}	3.38×10^{5}
HfO_2 74.5nm	-1.89	211.32	3.98	4.91×10^{-6}	1.15×10^{-11}	4.26×10^{5}

Table 3.1(b) The electrical parameters of the TFTs incorporating HfO_2 gate dielectrics after sintering.

Gate dielectric	V_{TH} (V)	S.S. (mV/dec)	G_{m_max} (μS)	I_{on} (A)	I_{off} (A)	I_{on}/I_{off}
HfO_2 17.5nm	-0.89	152.4	2.31	6.47×10^{-6}	7.43×10^{-12}	8.71×10^{5}
HfO_2 41.5nm	-1.42	260.7	3.39	6.74×10^{-6}	8.93×10^{-12}	7.54×10^{5}
HfO_2 74.5nm	-1.91	196.1	4.65	6.85×10^{-6}	6.23×10^{-12}	$1.1. \times 10^{6}$

Fig. 3.3 (a) The peak positions and intensities of the XRD spectra for three main crystalline phase of HfO_2, obtained from powder diffraction ICDD card files [5].

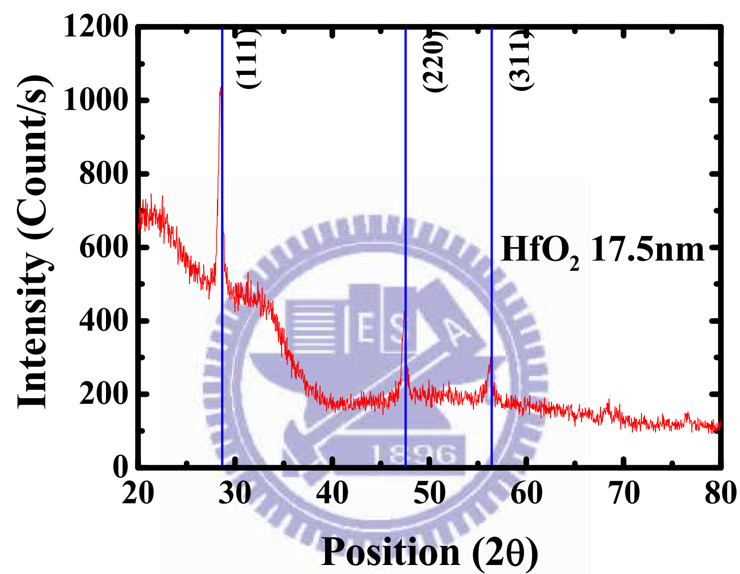


Fig. 3.3 (b) XRD spectra of the 175Å-thick HfO_2 layer, showing the clear peaks correspond to the monoclinic phase in the Fig. 3-3 (a), indicating that the phase transformation completes after sintering at 400℃ in a N_2 ambient.

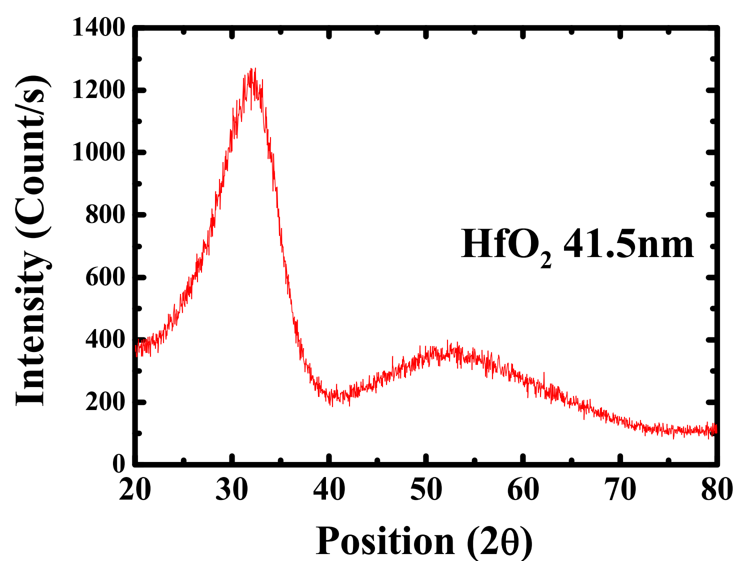


Fig. 3.3 (c) XRD spectra of the 415Å-thick HfO_2 layer. No obvious peak was observed, indicating that the phase remains amorphous after sintering at 400℃ in a N_2 ambient.

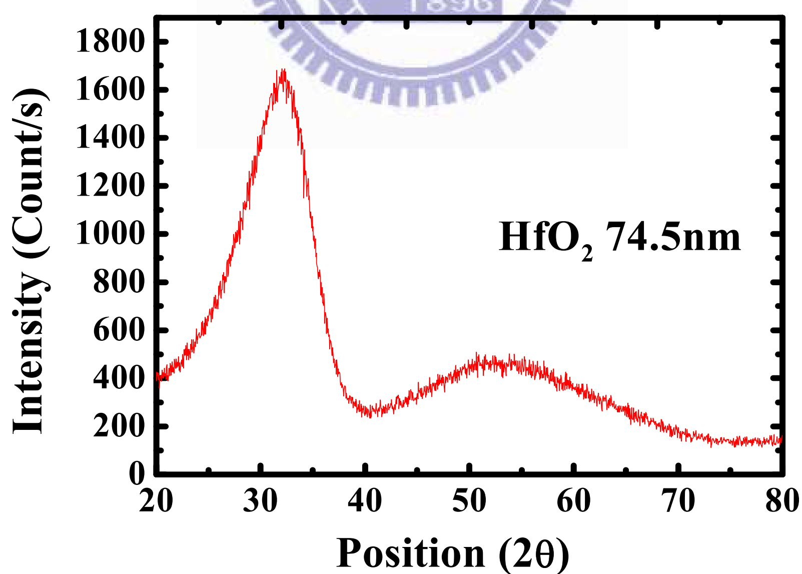


Fig. 3.3 (d) XRD spectra of the 745Å-thick HfO_2 layer. No obvious peak was observed, indicating that the phase remains amorphous after sintering at 400℃ in a N_2 ambient.

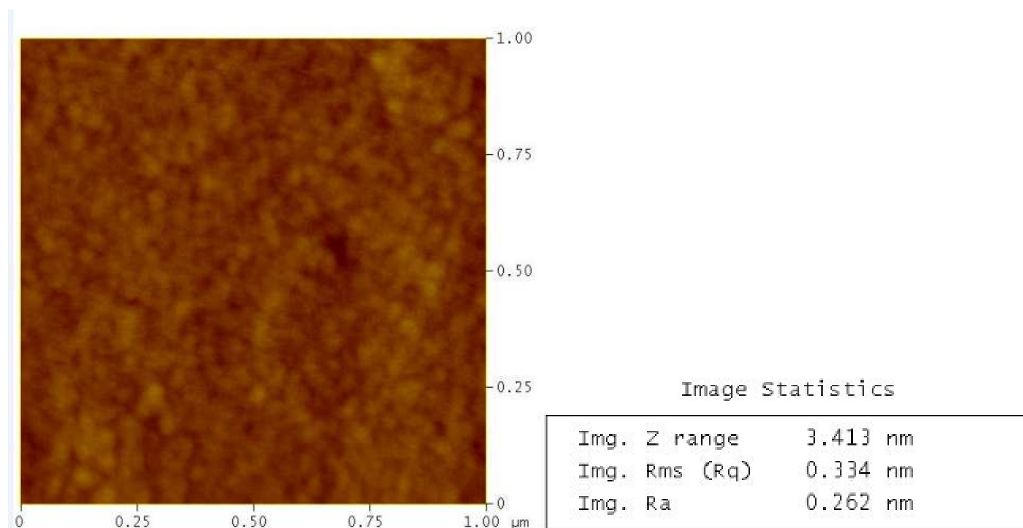


Fig 3.4 (a) The atomic-force microscopy (AFM) image of the poly-Si surface of the TFTs with 250Å-thick HfO_2 layer. The mean surface roughness is about 0.33nm.

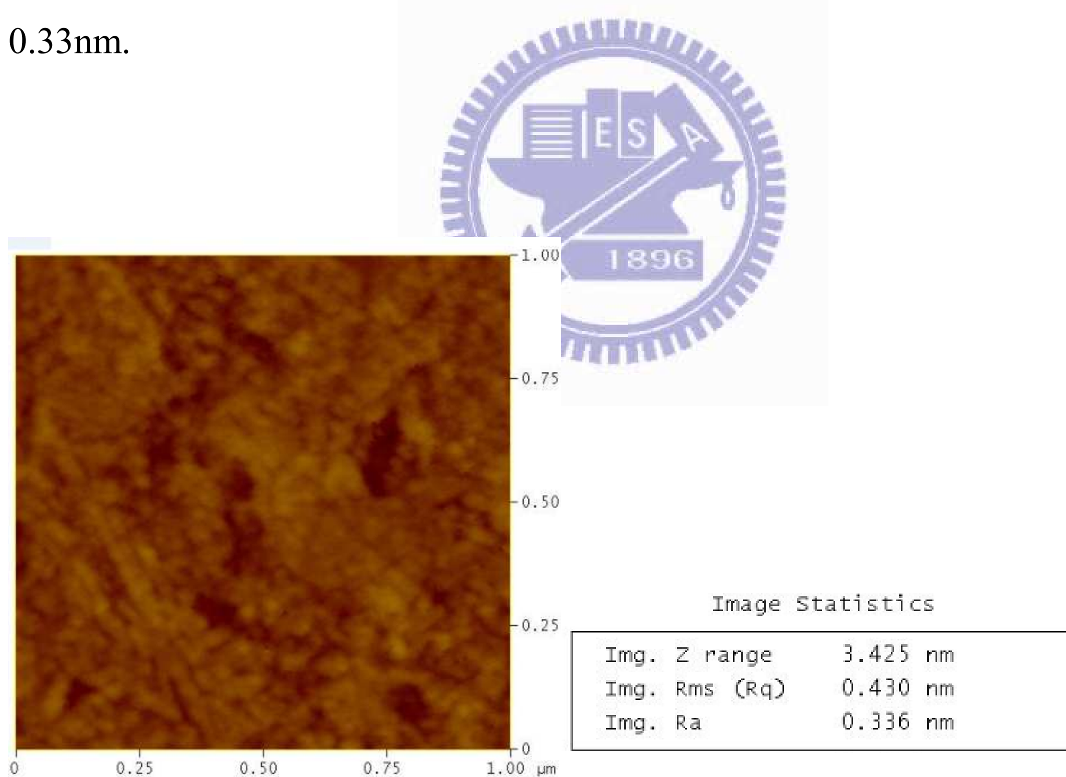


Fig. 3.4 (b) The atomic-force microscopy (AFM) image of the poly-Si surface of the TFTs with 1700Å-thick HfO_2 layer. The mean surface roughness is about 0.43nm.

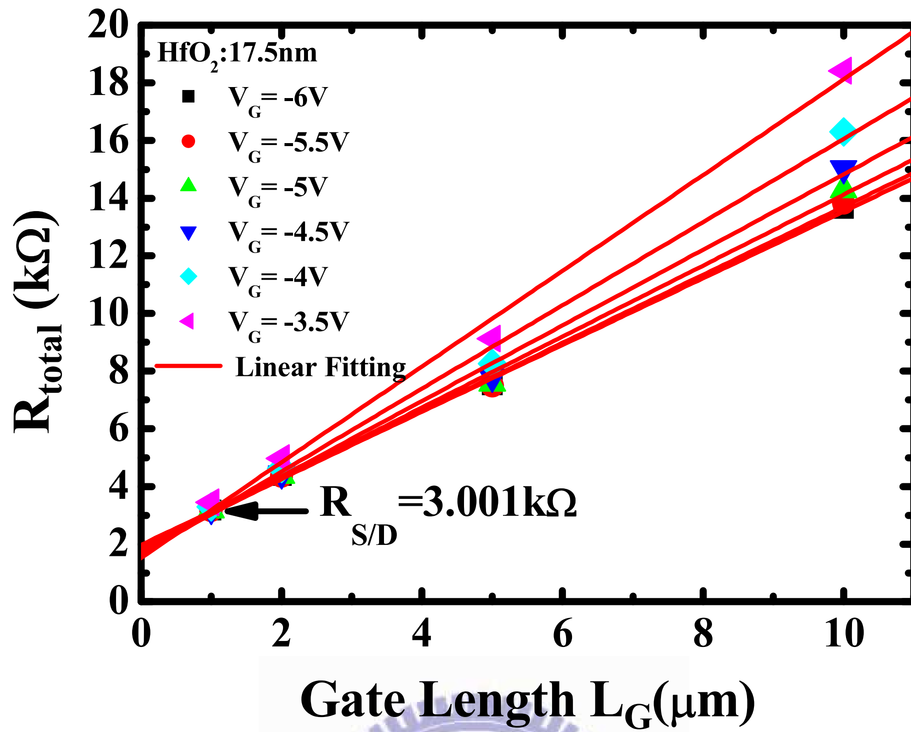


Fig. 3.5 (a) The extraction of the source/drain sheet resistance of the TFTs incorporating the 175Å-thick HfO_2 gate dielectric.

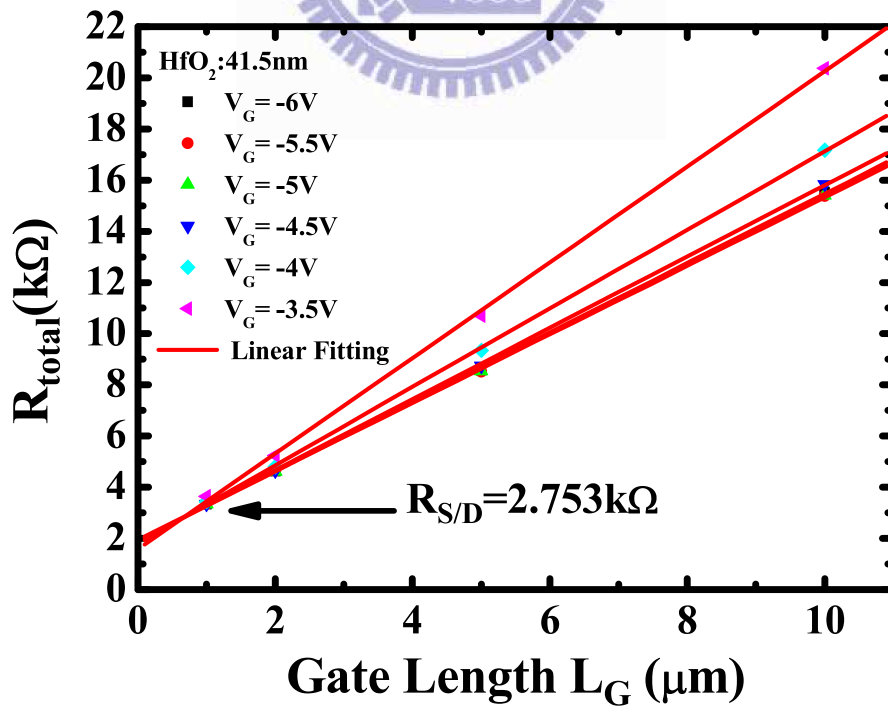


Fig. 3.5 (b) The extraction of the source/drain sheet resistance of the TFTs incorporating the 415Å-thick HfO_2 gate dielectric.

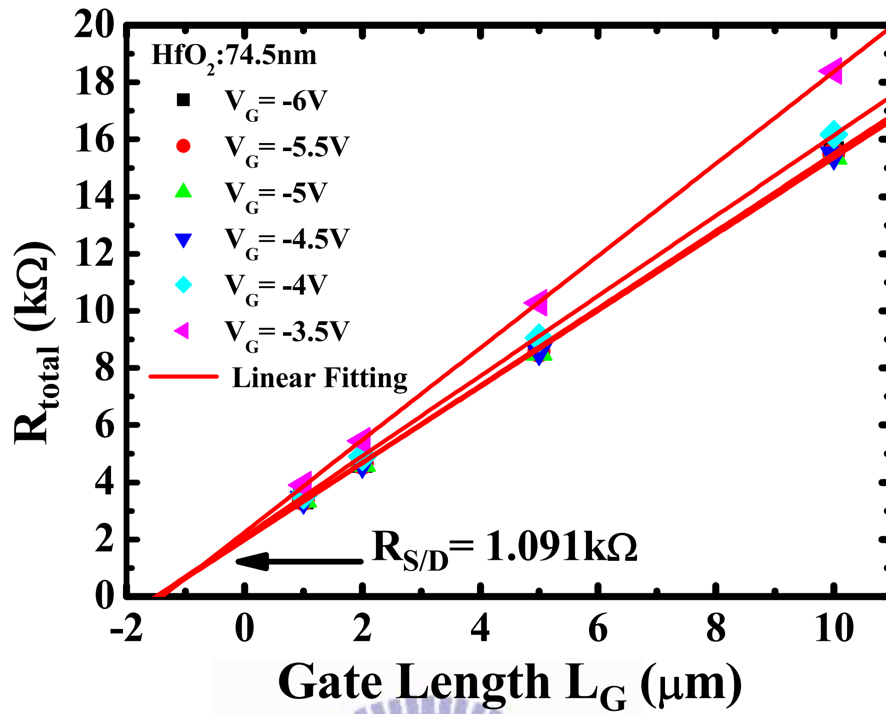


Fig. 3.5 (c) The extraction of the source/drain sheet resistance of the TFTs incorporating the 745Å-thick HfO_2 gate dielectric.

Table 3.2 The initial peak transconductance and the modified peak transconductance.

HfO_2 thickness (nm)	$R_{S/D}$ (kΩ)	G_{m_max}' (μS)	G_{m_max} (μS)
17.5	3.001	2.31	2.29
41.5	2.753	3.39	3.36
74.5	1.091	4.65	4.63

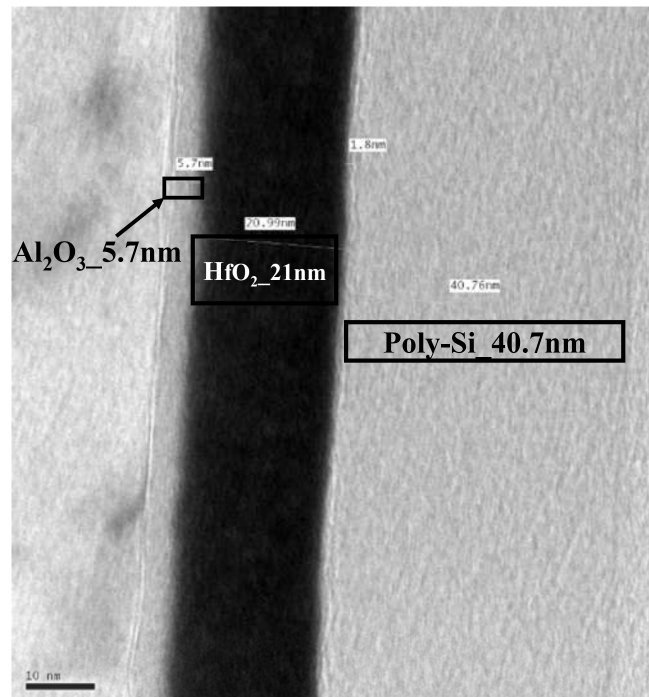


Fig. 3.6 (a) Cross-sectional TEM image of TFTs incorporating 250Å-thick HfO_2 gate dielectric.

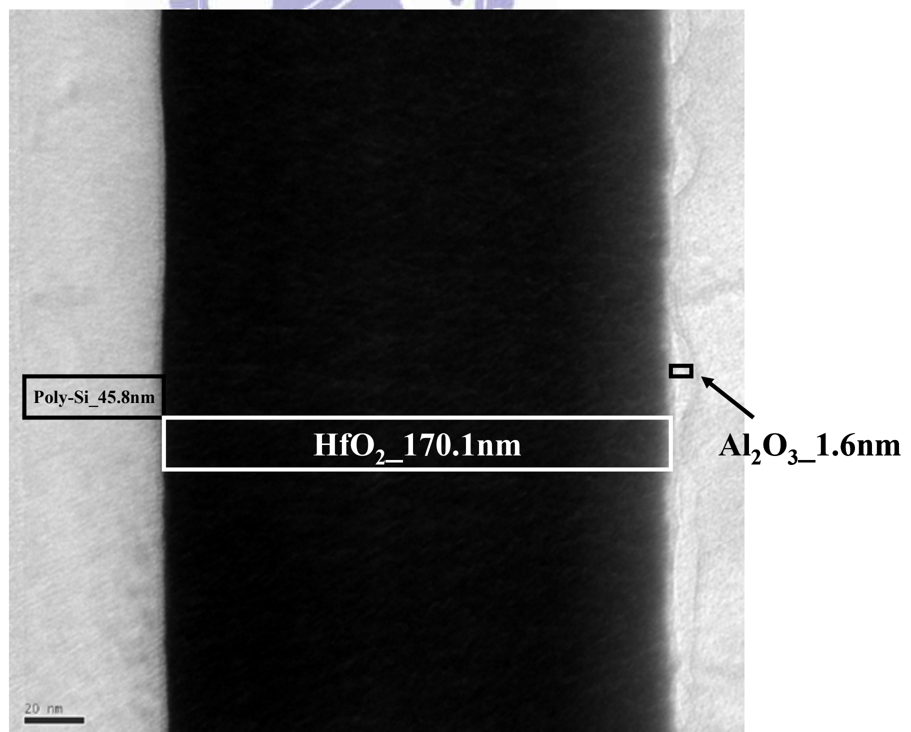


Fig. 3.6 (b) Cross-sectional TEM image of TFTs incorporating 1700Å-thick HfO_2 gate dielectric.

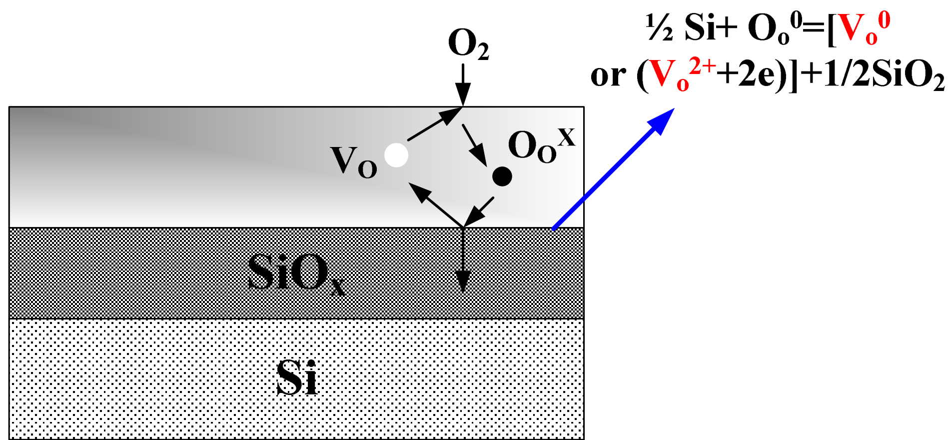


Fig. 3.7 Schematic of the silicon-metal oxide stack, showing the mechanism of transport of oxygen from the ambient to the silicon interface [7].

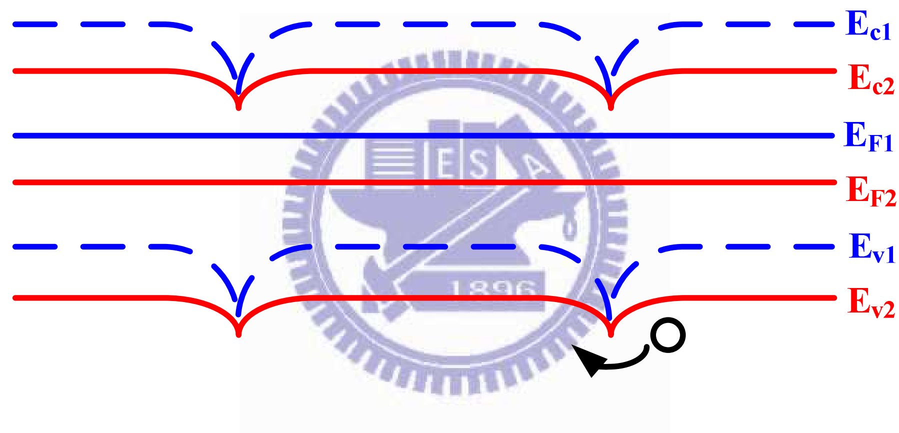


Fig. 3.8 It becomes easier for holes to get across the grain boundary potential barrier height after the grain boundary potential barrier height is lowered by the voltage drop induced by the positively charged oxygen vacancies.

Chapter 3

Reference

[1] T. Yamaguchi, R. Iijima, T. Ino, A. Nishiyama, H. Satake, and N. Fukushima,"Additional scattering effects for mobility degradation in Hf-silicate Gate MISFETs," in *IEDM Tech. Dig*., p.621, 2002.

[2] M. Y. Ho, H. Gong, G. D. Wilk, B. W. Busch, M. L. Green, P. M. Voyles, D. A. Muller, M. Bude, W. H. Lin, A. See, M. E. Loomans, S. K. Lahiri, and Petri I. Räisänen," Morphology and crystallization kinetics in HfO2 thin films grown by atomic layer deposition," *J. Appl. Phys.*, vol. 93, pp. 1477-1481, 2003.

[3] S. Saito, Y. Matsui, K. Torii, Y. Shimamoto, M. Hiratani and S. Kimura," Inversion electron mobility affected by phase separation in high-permittivity gate dielectrics," *Jpn. J. Phys. Phys.*, vol. 42, pp. L1425-L1428, 2003.

[4] K. Shiraishi, K. Yamada, K. Torii, Y. Akasaka, K. Nakajima, M. Konno, T. Chikyow, H. Kitajima, T. Arikado," Oxygen vacancy induced substantial threshold voltage shifts in the Hf-based High-K MISFET with p^+ poly-Si gates -a theoretical approach," *Jpn. J. Phys. Phys.*, vol. 43, pp. L1413-L1415, 2004.

[5] K. Xiong, J. Robertson, M. C. Gibson, and S. J. Clark, "Defect energy levels in HfO_2 high-dielectric-constant gate oxide," *Appl. Phys. Lett.*, vol. 87, pp. 183505-183507, 2005.

[6] J. K. Schaeffer, L. R. C. Fonseca, S. B. Samavedam, Y. Liang, P. J. Tobin, B. E. White," Contributions to the effective work function of platinum on hafnium dioxide," *Appl. Phys. Lett.*, vol. 85, pp.1826-1828, 2004.

[7] S. Guha and V. Narayanan," Oxygen vacancies in high dielectric constant oxide-semiconductor films," *Phys. Rev. Lett.*, vol. 98, pp. 196101, 2007.

Chapter 4

Negative Bias Temperature Instability in p-Channel LTPS TFTs with Different Thickness of HfO_2 Gate Dielectrics

4.1 Gate Leakage Current

Before the discussion of the degradation of the parameters during NBTI stress, it is necessary to investigate the gate leakage mechanism at different temperature and sweep gate voltage of the TFTs with different thickness of HfO_2 gate dielectrics. Due to the field dependence or the temperature dependence of the gate leakage current, knowing the behavior of gate leakage will help us know the kinetics of the carrier transport in the HfO_2 gate stacks with different thickness.

Fig. 4.1 plots the gate leakage current versus the sweep gate voltage from 0.5V to -4.5V of the TFT devices with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at room temperature (25℃). As shown in the Fig. 4.1, the gate leakage current nearly doesn't change with the HfO_2 thickness when the gate bias is less than about -3.5V. However, the gate leakage current increases drastically when the gate bias is higher than about -3.5V for the three devices and the slopes of the curves increase with the HfO_2 thickness. It is obvious that the magnitude of the gate leakage current is not correlated to the HfO_2 thickness as the gate voltage is smaller than about -3V. In addition, it is found that the gate voltage dependence of the gate leakage is insignificantly as the gate bias is

smaller than -3V. Considering the HfO_2 thickness and the energy band diagram of the TFT devices, the slow increase of the gate leakage current at low field is likely due to the trap-assisted tunneling (TAT) through the bulk traps in the HfO_2 layer [1]-[2]. Due to the fact that the gate leakage resulted from TAT is associated with the voltage drop across the HfO_2 layer rather than the electric field across the HfO_2 layer, the gate leakage current just increases with the gate bias but not change with the HfO_2 thickness. It has been reported that the gate leakage current induced by trap-assisted tunneling is proportional to the trap state density of the high-k films. [3]. Although the trap state density of the HfO_2 dielectrics is predicted to increase with the HfO_2 thickness [4], the tunneling probability of the electrons is largely reduced by the Al_2O_3 layer as shown in the cross-sectional TEM images of the HfO_2-TFTs in the Fig. 3.6 (a) and (b). A thin transition layer is observed between the Al gate and the HfO_2 film. We further analyze the material composition of this transition layer by EDX. Table 4.1 and Table 4.2 show the percentage of the main ingredients of the transition layer of the 250Å and the 1700Å sample. It is found that this transition layer is mainly composed of Al and O atoms. Therefore, it is suggested that this transition layer is an Al_2O_3 layer. It has been reported that when Hf or Zr metals are in contact with dielectrics, like SiO_2, the oxygen from the dielectric can easily diffuse into the metal forming a metal oxygen solid solution. Thus, the formation of Al_2O_3 happened in our experiment [5]. Because the thickness of the Al_2O_3 layer increases with the decreasing HfO_2 thickness, the gate leakage current just changes a little with the thickness of the HfO_2 layer as the gate voltage is smaller than -3.5V.

When the gate bias is higher than -3.5V, the gate leakage currents break off from the initial trend and drastically increase with the gate bias. What's more,

the magnitude of the enhancement increases with the HfO_2 thickness. Considering the band diagram and the low electric field across the HfO_2/SiO_2 gate stacks, Frenkel-Poole (FP) and the Schottky emission (S-E) are the most possible mechanisms to explain the increase of the gate leakage at the higher gate bias. To confirm the mechanism that dominates the gate leakage at gate bias higher than -3.5V, we measured the gate leakage current at different temperature from 25℃ to 125℃.

Fig. 4.2 (a) to (c) show the gate leakage versus sweep gate voltage at different temperatures from 25℃ to 125℃ of the devices with 175Å, 415Å and 745Å-thick HfO_2 gate dielectric. As shown in the Fig. 4.2 (a) and (b), the gate leakage current of the 175 and 415Å sample increases rapidly with temperature as the gate bias is higher than about -3.5V. It has been reported that the Frenkel-Poole (F-P) conduction and Schottky emission (S-E) both have strong temperature dependence. Because the Al/Al_2O_3 barrier height is expected to be around 3.2V, it is suggested that the most possible gate leakage mechanism is the Frenkel-Poole (F-P) conduction [5]. However, the increase of the gate leakage current of the 745Å sample just changes slightly with temperature as shown in Fig. 4.2 (c). Thus, it is recognized that the dominant kinetic of the gate leakage through HfO_2 layer is different from the 175Å and the 745Å sample. We have observed that there is an Al_2O_3 layer at the HfO_2/poly-Si interface. Due to the existence of this Al_2O_3 interfacial layer, it is possible for electrons to tunnel directly from the Al gate to the poly-Si channel. What's more, the fact that the thickness of Al_2O_3 layer decreases with the increasing HfO_2 thickness can explain the phenomena that the gate leakage current increases with the HfO_2 thickness at gate bias larger than -3.5V even though the electric field across the

HfO_2 layer decreases with the increasing HfO_2 thickness.

Considering the thicker Al_2O_3 layer of the 175Å and the 415Å sample, injected electrons will first pass through the Al_2O_3 layers by Frenkel-Poole (F-P) conduction and then move through the HfO_2 layer by trap-assisted tunneling (TAT). As for the 745Å sample, the increase of the gate leakage current changes slightly with temperature, indicating that the conduction mechanism of electrons from the Al gate to the poly-silicon channel is no more strong temperature dependent. Thus, the most possible mechanism of the gate leakage current flow through the Al_2O_3 layer is direct tunneling (DT) or Fowler-Nordheim (FN) tunneling. And it is consistent with the fact that the thickness of the Al_2O_3 layer decreases with the increasing HfO_2 thickness so that the DT and FN tunneling are the most possible mechanism for the gate leakage current generated at the Al_2O_3/HfO_2 interface in the 745Å sample. On the other hand, we can see that the gate leakage current decreases slightly with the measurement temperature. It may be because of that the bulk traps are located at the deep energy level in the bandgap of the Al_2O_3 so that the gate leakage is reduced at elevated temperature.

4.2 NBTI Stress

In this section, variation of the threshold voltage (V_{th}), degradation of peak transconductance (G_{m_max}) and subthrethold swing (S.S.) of p-channel TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics during NBTI stress was investigated.

NBTI stress was carried out on the structure of Al/HfO_2/poly-Si TFT devices at different temperatures at 25℃ and 125℃, respectively, with a constant gate bias of $V_{G_stress}-V_{th_initial}$=-3V, -4V and -5V and with source, drain

grounded. The threshold voltage (V_{th}) of the p-channel TFTs was recorded periodically during the stress by measuring its transfer characteristics (I_D-V_G) at a fixed drain voltage of -100mV. Poly-Si-TFTs incorporating 175Å, 415Å and 745Å-thick HfO_2 gate dielectric were compared.

With the observation of the total V_{th} shift of the TFTs during NBTI stress, we can find that the V_{th} variation in the transfer characteristics is (I_d-V_G plots) mainly resulted from the parallel V_{th} shift without S.S. degradation and the V_{th} shift resulted from the S.S. degradation instead of the parallel V_{th} shift. As far as we know, the parallel V_{th} shift is dominated by oxide trapping in the gate dielectrics. However, the V_{th} shift resulted from the S.S. degradation is mainly attributed to the interface states generation. As a result, before the discussion of the behavior of NBTI stress, we proposed that the total V_{th} variation during the NBTI stress can be divided into two parts as (1) V_{th} shift attributed to oxide trapping and (2) V_{th} shift attributed to the interface states generation. With this assumption, we separate the V_{th} shift into the (1)V_{th} shift attributed to oxide trapping and (2) V_{th} shift attributed to the interface states generation.

The method of separating is described as follows: As shown in the Fig. 4.3, we can find that the I_D-V_G curve with red color (after stress) is different from the I_D-V_G curve with black color (initial), The gate voltage corresponds to the minimum drain current of the red curve is several mV negative shift away from the gate voltage correspond to the minimum drain current of the black curve. The quantity of the parallel shift of the gate voltage corresponds to the minimum drain current is defined as the V_{th} shift attributed to oxide trapping. On the other hand, after parallel shifting the red curve to the gate voltage corresponds to the minimum drain current of black curve, we can find that the V_{th} of the red curve is still several mV negative shift away from the V_{th} of the black curve. This kind

of V_{th} shift is mainly resulted from the S.S. degradation and thus we defined it as the V_{th} shift attributed to interface states generation.

4.2.1 V_{G_stress}-V_t = -3V at 25℃

As shown from the Fig. 4.4 (a) to (c), the V_{th} shift resulted from oxide trapping dominates the total V_{th} shift and the V_{th} shift resulted from interface states nearly can be neglected, indicating that the Si-H bonds at the interface are not damaged severely under this stress condition.

The quantity of the V_{th} shift resulted from oxide trapping is totally different from each other of the three samples. However, there is nearly no V_{th} shift resulted from the interface states for the three samples. As far as we know, the R-D model [6] tells us that the inversion holes will react with the Si-H bonds and then release the hydrogen related species and then leave fixed oxide charges and interface states behind at the silicon/dielectric interface. However, we just see a little S.S. degradation and little V_{th} shift resulted from interface states, indicating that the stress temperature is not high enough to offer sufficient energy to break the weak Si-H bond.

In spite of that the interface states generation nearly can be neglected under this stress condition; the most part of total V_{th} shift is still attributed to oxide trapping. The V_{th} shift resulted from oxide trapping of the 175Å sample increases toward positive and then saturates at 50 seconds of stress time, indicating that electron trapping takes place in the Al_2O_3/HfO_2 gate dielectric stack. With a longer stress time, the band distortion induced by electron trapping stops the electron trapping so that the positive V_{th} shift saturates after 50 seconds of stress time.

As for the 415Å and 745Å sample, the V_{th} shift toward positive initially and then shift toward negative, and the negative V_{th} shift of the 415Å sample is more significant than the 745Å sample. Obviously, electron trapping dominate the positive V_{th} shift initially and then the positive charge trapping dominates the oxide trapping of the 415Å and the 745Å sample. The positive V_{th} shift may be due to the neutralization of the positively charged vacancies by electron trapping. The origin of the positive charges may be due to the trapping of holes produced by electron impact ionization at the anode. (Anode hole injection) [7]. The electrons tunneling through the thin Al_2O_3 layer arrive at the anode with a maximum energy qVg will create electron-hole pairs. The generated hot holes are driven by the large negative bias and then directly tunnel into the bulk traps in the HfO_2 layers. As a result, the amount of hole trapping strongly depends on the impact ionization rate. It was reported that the impact ionization rate is highly electric field dependent[7], As a result, the hole trapping or the negative V_{th} shift attributed to hole trapping of the 415Å sample is more severe than the 745Å samples due to the larger electric field across the thinner gate stack.

Except for the V_{th} shift and the S.S. degradation, the mechanism of peak transconductance (G_{m_max}) degradation during NBTI stress is also discussed in this paper. As we can see in the Fig. 4.4 (e), the G_{m_max} degradation of the 175Å and the 415Å sample are nearly the same before stress time of 100 seconds. However, the G_{m_max} degradation of the 415Å sample increases more rapidly than the 175Å samples after the stress time of 100 seconds. It was widely reported that the G_{m_max} degradation of the TFT devices is mainly dependent on the interface states generation and the tail trap states generation in the grain boundaries [8]. Because there is nearly no interface states generation under this stress condition, the G_{m_max} degradation is probably resulted from the generation

of tail trap states in the grain boundaries. For this reason, we extract the grain boundary trap state density by the Lenvinson and Proano method [9]-[10] as shown in the Fig. 4.4 (f). The slopes of these curves stands for the grain boundary trap state density in the poly-Si channel film. We found that the grain boundary trap states generation of the 175Å and 745Å sample just changes a little after the stress time of 1000 seconds. It is reasonable that the interface states generation should be proportional to the grain boundary trap states generation [6]. Unlike the 175Å and the 745Å sample, the grain boundary trap states of the 415Å samples increases significantly after the stress time of 1000 seconds. This may be due to the fact that the impact ionization rate is severe in the 415Å sample during stress. The accelerated electrons with large kinetic energy may break the Si-H bonds in the grain boundaries and thus result in many grain boundary trap states. In comparison with the plots of G_{m_max} degradation and the plots of the trap states generation, it is suggested that the G_{m_max} degradation of the 175Å and the 415Å sample is mainly attributed to the grain boundary trap states generation. Unlike the 175Å and the 415Å sample, the G_{m_max} degradation has no proportionality with the grain boundary trap state density generation of the 745Å sample, indicating that the G_{m_max} degradation is not resulted from the grain boundary trap states. Therefore, we suggested that the annealing of the positively charged oxygen vacancy (V_O^{2+}) by electron trapping is the main reason that results in the G_{m_max} degradation of the 745Å samples. As a matter of fact, lots of electrons with small kinetic energy will transport from the Al gate to the HfO_2 layer by trap-assisted tunneling instead of tunneling through the Al_2O_3 layer by direct tunneling (DT) or F-N tunneling. Thus, some electrons near the HfO_2/silicon interface may be trapped by the positively charged oxygen vacancies (V_O^{2+}) and the positively charged oxygen

vacancy will be neutralized after electron trapping. According to the theory that we proposed before, the positively charged oxygen vacancy (V_O^{2+}) can lower the grain boundary potential barrier height in the poly-Si channel. Hence, the neutralized oxygen vacancy will no longer have impact on the grain boundary potential barrier height and the G_{m_max} degrades significantly.

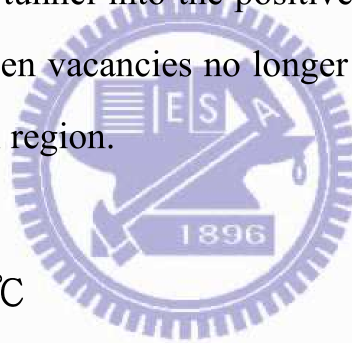
Summary

In summary, we found that the total V_{th} shift of the 175, 415 and 745Å sample is mainly attributed to oxide trapping during the NBTI stress under V_{G_stress}-V_t=-3V at 25℃. With the 175Å sample, electron trapping dominates over the positive V_{th} shift. On the other hand, the positive charge trapping leads to the negative V_{th} shift for the 415Å and the 745Å sample. The origin of the positive charge is probably resulted from the (1) hole trapping induced by anode hole injection (AHI) (2) holes at a given gate bias directly tunnel into the bulk traps in the HfO_2 layers. Furthermore, with the higher impact ionization rate of the 415Å sample than that of the 745Å sample, the negative V_{th} shift resulted from the 415Å sample is larger than the 745Å sample due to the larger amount of the hole injection resulted from the higher impact ionization rate.

As for the interface states generation, the V_{th} shift attributed to interface states and the S.S. degradation of the three samples nearly can be neglected, indicating that the HfO_2/poly-Si interface is not severely damaged under this stress condition.

As for the G_{m_max} degradation, the G_{m_max} degradation increases with the HfO_2 thickness. Moreover, the G_{m_max} of the 745Å sample degrades much more significantly than the 175 and the 415Å sample. By introducing the trap states

density generation after the stress time of 1000 seconds, we can find that the G_{m_max} degradation is not correlated to the trap states generation. The trap states density just changes little for the 175Å and the 745Å sample, indicating that the Si-H bonds in the grain boundaries in the channel regions of the 175Å and the 745Å sample are not damaged significantly. Unlike the 175Å and the 745Å sample, the trap states generation of the 415Å sample is significantly, it is probably because the impact ionization rate of the 415Å sample is the highest among the three samples. Besides, the trap states generation of the 745Å sample is nearly negligible but the G_{m_max} shift of the 745Å sample is severely degraded. It maybe due to the fact that the electrons transported from the Al gate to the HfO_2/poly-Si interface will tunnel into the positively charged oxygen vacancies so that the neutralized oxygen vacancies no longer have impact on the potential barrier height in the channel region.



4.2.2 V_{G_stress}-V_t=-5V at 25℃

With separating the total V_{th} shift into the V_{th} shift attributed to oxide trapping and the interface states, it is obvious that the total V_{th} shift is dominated by oxide trapping instead of the interface states under the stress condition of V_{G_stress}-V_t=-3V at 25℃. However, the V_{th} shift attributed to the interface states and the S.S. degradation no longer can be neglected under the stress condition of V_{G_stress}-V_t=-5V at 25℃, indicating that the injected electrons with energy qV_g arriving at the anode could result in more energetic electrons and holes than that during the stress of V_{g_stress}-V_{th}= -3V.

As wee can see from the Fig. 4.5 (a) to (c), the total V_{th} shift is still

dominated by oxide trapping like the stress condition of V_{G_stress}-V_t=-3V at 25℃. The V_{th} shift attributed to oxide trapping of the 175Å sample is positive from initial to the stress time of 1000 seconds, indicating that the electron trapping dominates the oxide trapping of the 175Å sample during stress time of 0 to 1000 seconds. However, the magnitude of the positive V_{th} shift is not as high as the 175Å sample under the stress condition of V_{G_stress}-V_t=-3V, indicating that there are more positive charge trapping in the gate stack under this stress condition. The origin of the positive charge may be due to the several parts like (1) trapping of the hot holes produced by the electron impact ionization at the anode. (AHI) (2) electron tunneling through the very thin Al_2O_3 layer with large kinetic energy arrive at the anode may release H^+ and then the protons will be accelerated by the electric field across the HfO_2 layer, leading to the breaking of bridging oxygen bonds and the trapping of proton by the HfOH sites [11]. (3) the inversion holes react with the Si-H bonds and then result in the positive fixed oxide charges at the interface, or (4) the hydrogen induced $[Si_2=OH]^+$ and/or $[Hf_2=OH]^+$ centers due to the transport of H^+ released by the broken Si-H bonds in the gate dielectric stack [12]. As for the 415Å and 745Å sample, the V_{th} shift attributed to oxide trapping is nearly negligible, indicating that the amount of the electron trapping and the positive charge trapping are nearly the same. Nevertheless, the negative V_{th} shift of the 415Å sample are still higher than that of the 745Å sample like the stress condition of the V_{G_stress}-V_t=-3V. However, the trend of the V_{th} shift attributed to oxide trapping is not in the same correlation with the V_{th} shift attributed to the interface states. It stands for that the oxide trapping of the 415Å and the 745Å sample is mainly resulted from the hole trapping instead of the fixed oxide charge generation. In accordance with the

correlation of the V_{th} shift attributed to oxide trapping, the amount of hole trapping mainly depends on the impact ionization rate. The impact-ionization induced hot holes may be directly tunnel into the bulk traps in the HfO_2 layer rather than react with the Si-H bonds at the poly-Si/HfO_2 interface. As for the reason why the amount of the hole trapping of the 415Å sample is higher than the 745Å sample is the same as the discussion presented for the stress condition of V_{G_stress}-V_t=-3V.

As for the V_{th} shift attributed to the interface states, we can see that the interface states contribution of the 415Å sample and the 745Å sample is higher than that of the 175Å sample. This is because for the thinner gate dielectric stacks; it is easier for electrons to tunnel through the very thin Al_2O_3 layer and with a small consumption of the kinetic energy. As a result, the electrons with larger kinetic energy may release more protons and therefore the interface states generation become more significantly. Due to the fact that the thickness of the Al_2O_3 layer decreases with the increasing HfO_2 thickness, the electrons in the thicker HfO_2 layer may break more Si-H bond at the poly-Si/HfO_2 interface and thus the interface states generation increases with the thickness of the HfO_2 layers.

As for the G_{m_max} degradation, we can see that the G_{m_max} degradation has the same correlation with the V_{th} shift attributed to the interface states generation. What's more, the grain boundary trap states generation and the G_{m_max} degradation of the 175Å and the 415Å sample are in the same correlation, indicating that the G_{m_max} degradation is mainly attributed to the grain boundary trap states generation and interface states generation of the 175Å and the 415Å sample. However, the G_{m_max} degradation and the grain boundary trap states generation of the 745Å sample are not in the same order. The explanation for this

phenomenon is the same as the discussion of the G_{m_max} degradation of 745Å sample under the stress condition on V_{G_stress}-V_t= -3V at room temperature.

There is a special phenomenon that the S.S. degradation and the G_{m_max} degradation of the 745Å sample particularly become less severe at stress time of 500 seconds and it seems like the S.S. and the G_{m_max} somewhat recovers at this stress time. Due to the fact that the G_{m_max} and the S.S. degradation mainly depends on the interface states generation. We suggested that the released hydrogen may return back to the interface to passivate the interface and it is reasonable that the V_{th} shift becomes worse at this stress time. However, the real mechanism of this recovery behavior can't be understood yet.

Summary

In summary, the V_{th} shift attributed to oxide trapping dominates the total V_{th} shift. The electron trapping still dominates over positive charge trapping of the 175Å sample under this stress condition because the Al_2O_3 layer of the 175Å sample is too thick to tunnel through by direct tunneling (DT) and thus the electron trapping of the 175Å sample is more severe than that of the 415Å and the 745Å sample. Unlike the 175Å sample, the V_{th} shift resulted from oxide trapping of the 415Å and the 745Å sample mainly attributed to hole trapping induced by impact ionization (AHI) because the V_{th} shift attributed to oxide trapping has no proportionality with the interface states generation for the three samples. In addition, the V_{th} shift resulted from the interface states generation no longer can be neglected like the stress condition of V_{G_stress}-V_t=-3V. It indicates that the electrons tunnel through the thin Al_2O_3 have enough kinetic energy to release the protons and then leave the interface states behind. And it is consistent with the fact that the interface states generation increases with the HfO_2

thickness because the Al_2O_3 layer decrease with the increasing HfO_2 layer.

As for the G_{m_max} degradation, G_{m_max} degradation has proportionality with the interface states generation. Furthermore, the G_{m_max} degradation has the same correlation with the grain boundary trap states generation of the 175Å and the 415Å sample, indicating that the G_{m_max} degradation of the 175Å and the 415Å sample are attributed to the interface states and the grain boundary trap states generation. However, the G_{m_max} degradation of the 745Å sample is not correlated to the grain boundary trap states generation, it is suggested that the G_{m_max} degradation of the 745Å sample is due to the neutralization of the positively charged oxygen vacancies in the HfO_2 layer.

4.2.3 V_{G_stress}-V_t= -3V_125℃

Besides the discussion of the behavior of NBTI stress at room temperature, we also present the behavior of NBTI stress at elevated temperature in this chapter. Fig 4.6 (a) to (f) are the plots of parameter degradation during NBTI stress under stress condition of V_{G_stress}-V_t = -3V at 125℃. As we can see from the Fig. 4.6 (a) to (d), the total V_{th} of the three samples are nearly the same. However, the S.S. degradation and the V_{th} shift attributed to the interface states both decrease with the increasing HfO_2 thickness. Although the total V_{th} shift of the three samples are nearly the same, the V_{th} shift attributed to oxide trapping and the one attributed the interface states exhibit the different trend for the three samples.

As shown in Fig. 4.6 (c), we can see that V_{th} shift attributed to the interface states of the 745Å sample is much smaller than that of the 175Å and the 415Å sample but the amount of that of the 175Å and the 415Å sample are nearly the

same. However, the V_{th} shift attributed to oxide trapping shows the opposite behavior that the oxide trapping of the 175Å and the 415Å sample are much less than that of the 745Å sample. With the same proportionality of the V_{th} shift attributed to the interface states and the V_{th} shift attributed to oxide trapping of the 175Å and the 415Å sample, it is concluded that the interface states generation and the oxide trapping are resulted from the broken Si-H bonds, indicating that the Si-H bonds at the interface is severely damaged and the oxide trapping of the 175Å and the 415Å sample are attributed to fixed oxide charge generation. On the other hand, the interface states generation and oxide trapping of the 745Å sample seem not to be resulted from the broken Si-H bonds because they are not in the same correlation. Considering the very thin Ai_2O_3 layer of the 745Å sample, most of the hot holes near the HfO_2/poly-Si interface may tunnel into the HfO_2 layer immediately instead of reacting with the Si-H bonds at the interface. That's why the oxide trapping is not proportional to the interface states generation.

As for the G_{m_max} degradation, we can see that the interface states generation and the G_{m_max} degradation have nearly the same correlation but not in the same correlation with the grain boundary trap states generation for the three samples indicating that the G_{m_max} degradation is mainly dependent on the interface states generation. It indicates that the damage of the HfO_2/poly-Si layer interface is much more severe than that of the grain boundaries in the poly-silicon channel films under this stress condition. In addition, we can find that although the interface states generation of the 175Å sample is larger than that of the 415Å sample, the G_{m_max} degradation of the 175Å sample is less severe than that of the 415Å sample. It is because the electron transported by trap-assisted tunneling through HfO_2 layer of the 415Å sample is likely to be trapped by the positively

charged oxygen vacancy. Thus, the positively charged defect becomes neutral and has no impact on the potential barrier height at grain boundaries in the channel region.

Summary

In summary, the total V_{th} shift of the three samples is nearly the same. However, the V_{th} shift attributed to oxide trapping and the interface states generation of the three samples is different. The same correlation of the interface states generation and oxide trapping of the 175Å and the 745Å sample indicates that the Si-H bonds at the poly-Si/HfO_2 interfaces are severely damaged. On the other hand ,oxide trapping and the interface states generation of the 745Å sample are not in the same correlation because the kinetic energy of impact ionization induced hot holes is so high that they directly tunnel into the HfO_2 layer rather than react with the Si-H bonds. The V_{th} shift attributed to the interface states generation shows highly field dependence because the stress temperature under this stress condition is high enough to release the protons from the weak Si-H bonds and the protons and thus positive fixed charges leads to the negative V_{th} shift.

The G_{m_max} degradation of the three samples nearly has the same proportionality with the interface states generation, indicating that the G_{m_max} degradation is mainly attributed to the interface trap state generation. However, the G_{m_max} degradation of the 415Å sample is larger than that of the 175Å sample, indicating that the positively charged oxygen vacancies may be neutralized by electron trapping.

4.2.4 V_{G_stress}-V_t= -4V at 125℃

As shown in the Fig. 4.7 (d) and (e), we can see that the V_{th} shift attributed to the interface states generation and the S.S. degradation decreases with the HfO_2 thickness. It is because the NBTI stress is enhanced by the electric field across the gate dielectric stacks [13]. The higher the electric field across the gate dielectric stacks, the more released protons will diffuse into the gate stacks and thus enhance the generation of the interface states. However, the trend of the V_{th} shift attributed to the oxide trapping is opposite, indicating that the oxide trapping is not dominated by the fixed oxide charge generation resulted from the released protons. The behavior with this stress condition of oxide trapping is related to the thickness of the Al_2O_3 layer of the three samples. Due to the fact that the thickness of Al_2O_3 layer decreases with the HfO_2 thickness, the amount of the electrons tunnel through the Al_2O_3 layer from the Al gate depends on the thickness of the Al_2O_3 layer. With the high temperature, every electron tunnels through the Al_2O_3 layer must create electron-hole pairs. Therefore, the amount of hole trapping is Al_2O_3 thickness dependent rather than the electric field dependent of the impact ionization rate.

With the comparison of the plots of the grain boundary trap states generation (Fig. 4.7(f)) and the one of the V_{th} shift attributed to the interface states generation (Fig. 4.7(c)), we can find that they have the same correlation, indicating that during the NBTI stress, the inversion holes will react with the Si-H bonds at the grain boundaries and the poly-Si/HfO_2 interface at the same time. If the thermal energy is high enough, the hydrogen related species will be released from the Si-H bonds and then diffuse into the gate dielectric stacks.

As for the G_{m_max} degradation as shown in the Fig. 4.7 (e), we can see that

the G_{m_max} degradation of the 175Å and the 745Å sample has proportionality with the interface state generation and the grain boundary trap state generation, indicating that the grain boundary trap states and the interface states generation both contribute to the G_{m_max} degradation of the 175Å and the 745Å sample. However, the G_{m_max} degradation of the 415Å sample is similar with the 175Å sample. It may be due to the fact that the most electrons transported from Al gate to the HfO_2 layer are trapped by the positively charged defects of the 415Å sample and thus the positively charged oxygen vacancy are neutralized.

Summary

In summary, the V_{th} shift resulted from the interface states generation decreases with the increasing HfO_2 layer, indicating that the Si-H bonds at the poly-Si/HfO_2 interface are damaged severely. The electric field across the HfO_2 layer accelerated the generation of the protons and thus accelerated the interface states generation. However, the behavior of oxide trapping is opposite, the V_{th} shift attributed to oxide trapping increases with the HfO_2 thickness. It is because the thickness of the Al_2O_3 decreases with the thickness of HfO_2, the amount of the electron impact ionization induced hot holes increases with the thickness of the HfO_2 layer. As a result, hole trapping increases with the HfO_2 thickness.

Besides, the G_{m_max} degradation has the same proportionality with the grain boundary trap states generation and the interface states generation of the 175Å and the 745Å sample, indicating that the Si-H bonds in the grain boundaries and at the poly-Si/HfO_2 interface of the 175Å and the 745Å sample are damaged and both of them lead to the G_{m_max} degradation under this stress condition.

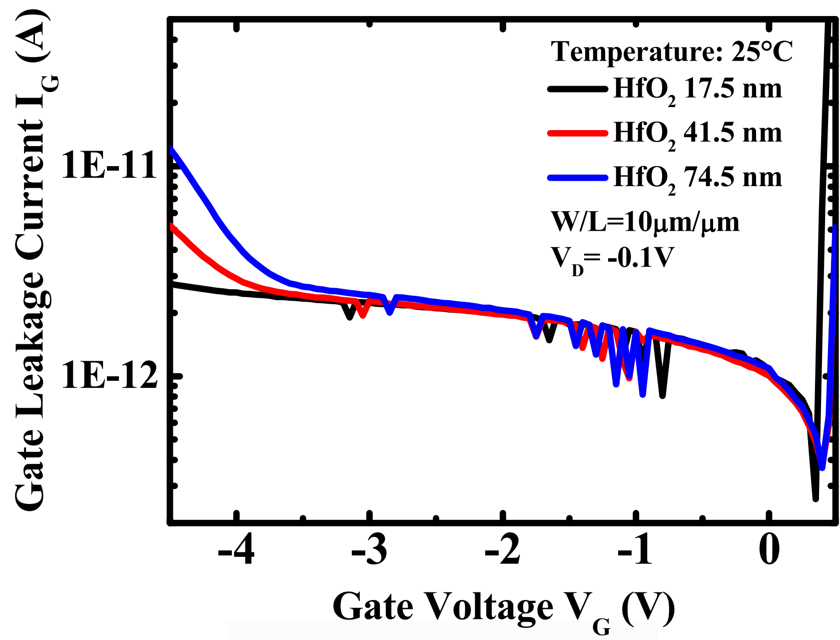


Fig. 4.1 Gate leakage current versus gate voltage of at 25℃

Table 4.1 The material composition of the transition layer in the 250Å sample, it is observed that the transition layer is mainly composed of Al and O atoms.

Element	Weight %	Atomic %
O	34.09	47.48
Al	63.18	52.18
Hf	2.73	0.34

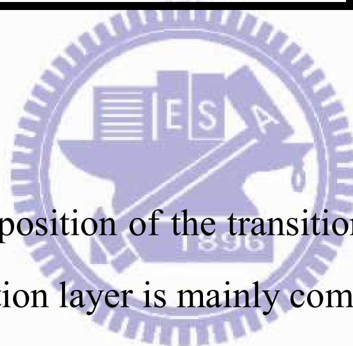


Table 4.2 The material composition of the transition layer in the 1700Å sample, it is observed that the transition layer is mainly composed of Al and O atoms.

Element	Weight %	Atomic %
O	33.75	43.61
Al	74.91	57.39
Hf	-8.66	-1.00

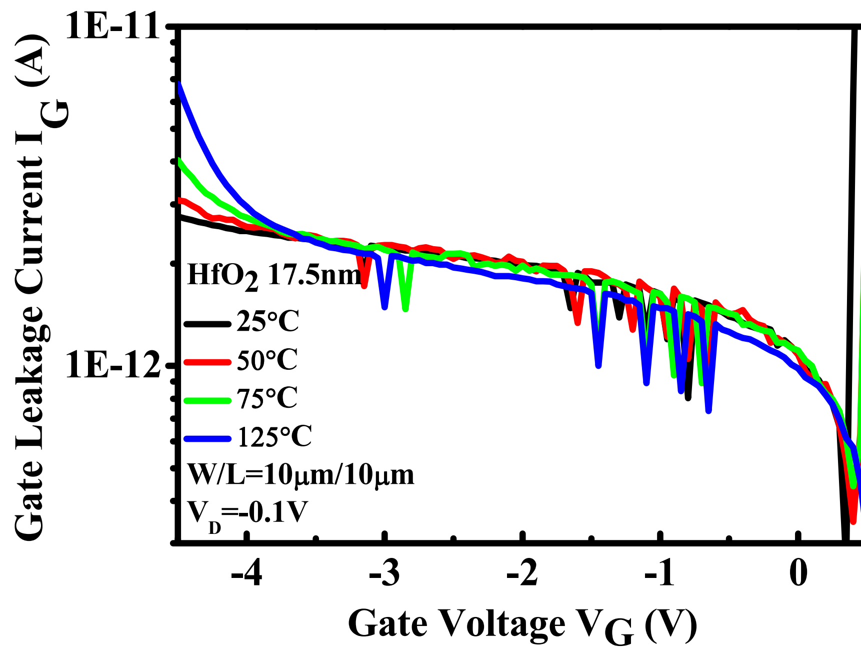


Fig. 4.2 (a) Gate leakage current of 175Å-thick HfO_2 TFT sample versus gate voltage at different temperature, ranging from 25℃, 50℃, 75℃, 125℃.

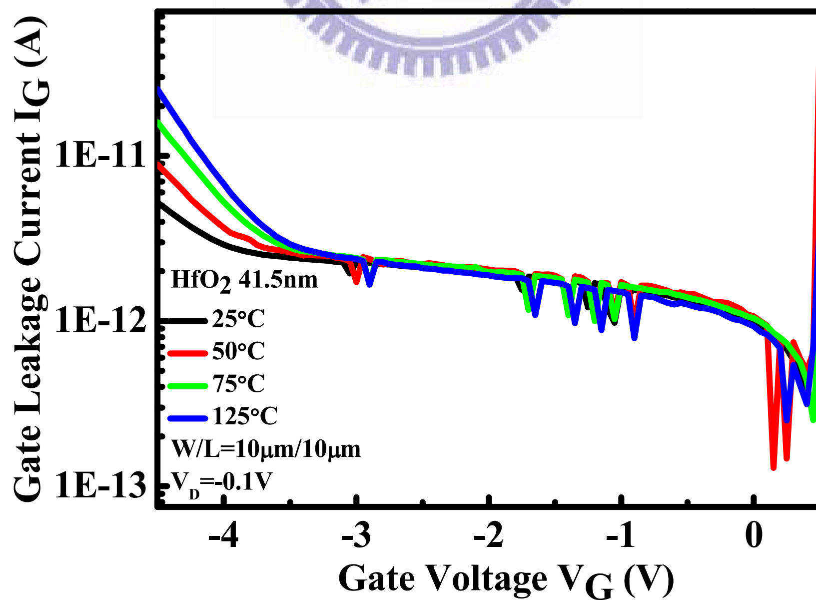


Fig. 4.2 (b) Gate leakage current of 415Å-thick HfO_2 TFT sample versus gate voltage at different temperature, ranging from 25℃, 50℃, 75℃, 125℃.

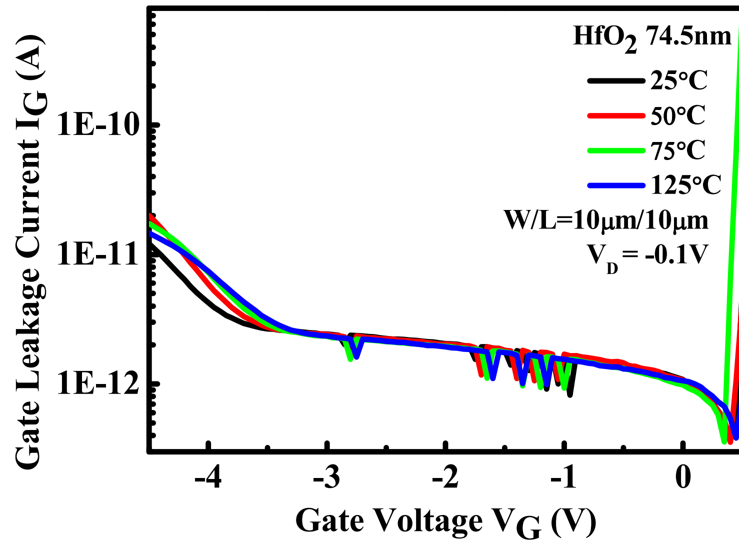


Fig. 4.2 (c) Gate leakage current of 745Å-thick HfO_2 TFT sample versus gate voltage at different temperature, ranging from 25℃, 50℃, 75℃, 125℃.

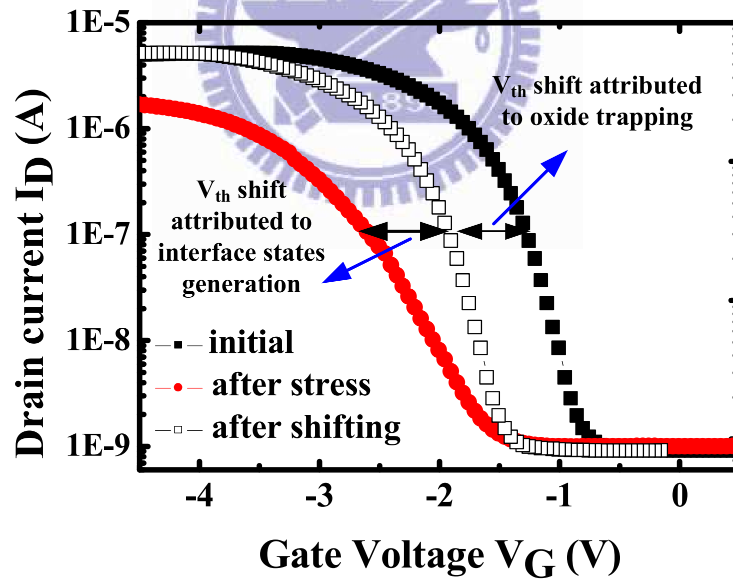


Fig. 4.3 The schematic plot of the V_{th} contribution separating method. We can derive the V_{th} shift attributed to oxide trapping by shifting the V_{on} of the initial I_D-V_G curve to the V_{on} of the I_D-V_G curve after stressing. On the other hand, we can derive the V_{th} shift attributed to the interface states generation after shifting the V_{on} of the initial I_D-V_G curve.

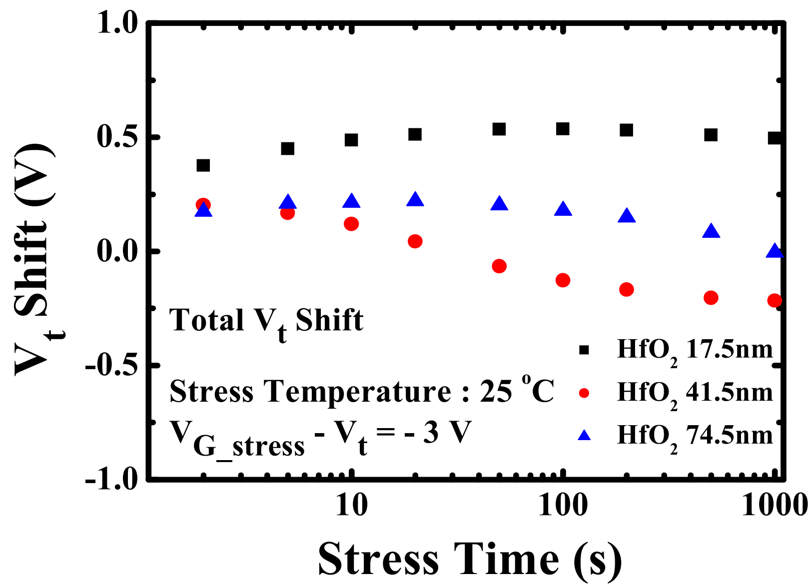


Fig. 4.4 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.

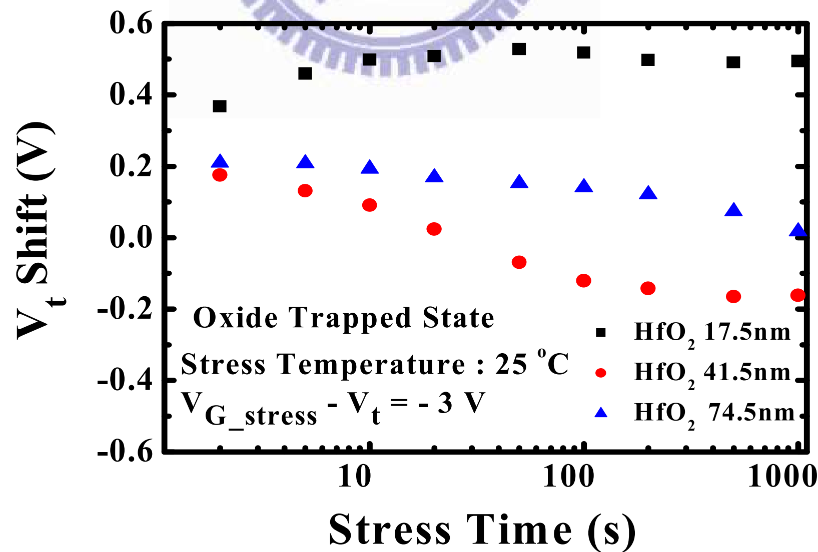


Fig. 4.4 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.

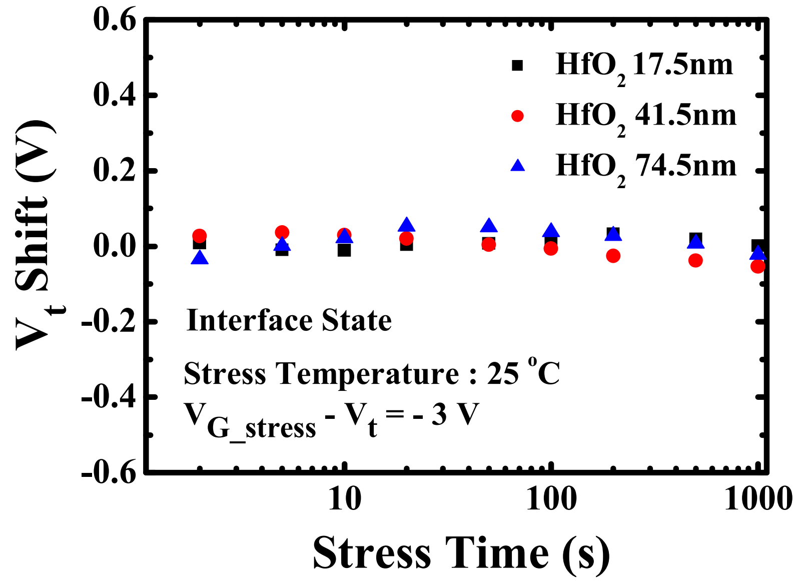


Fig. 4.4 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.

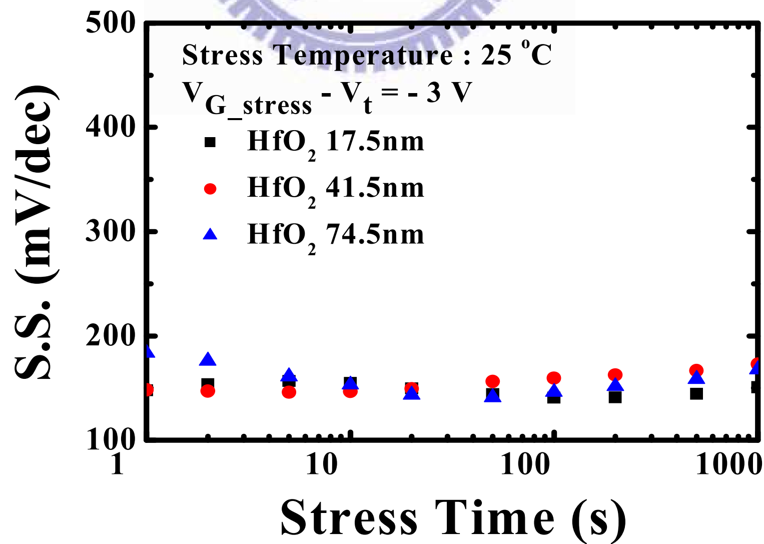


Fig. 4.4 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.

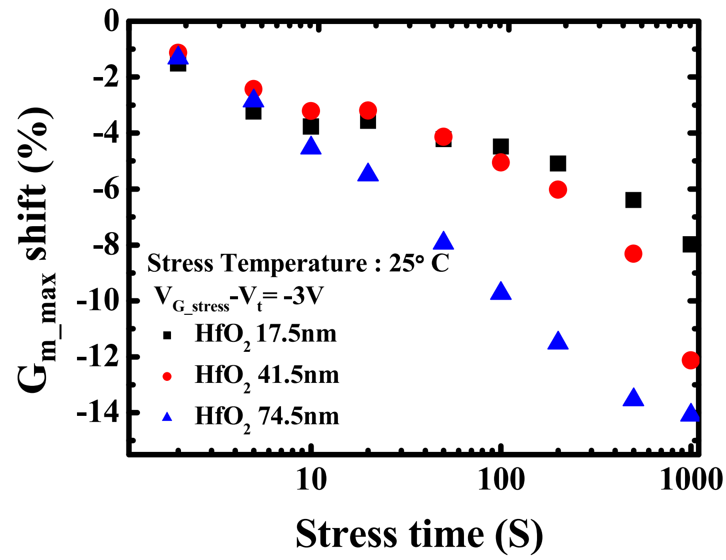


Fig. 4.4 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 25℃.

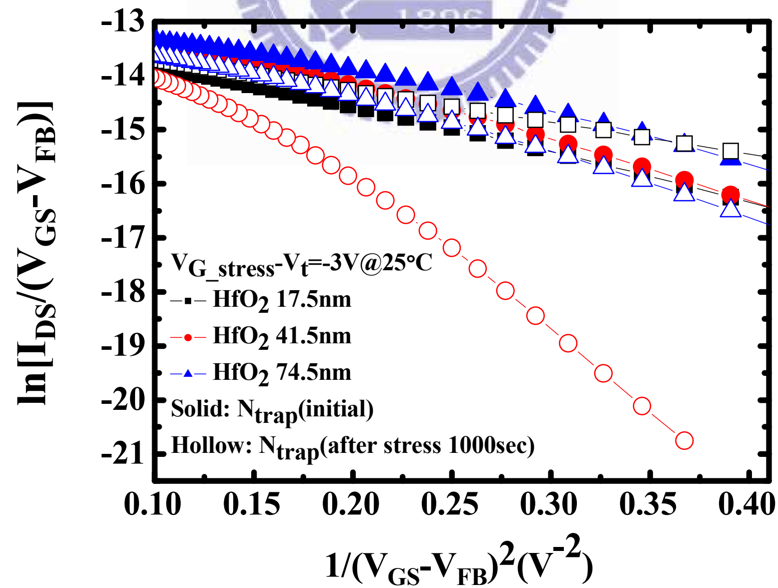


Fig. 4.4 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -3V after tress time of 1000 seconds at 25℃.

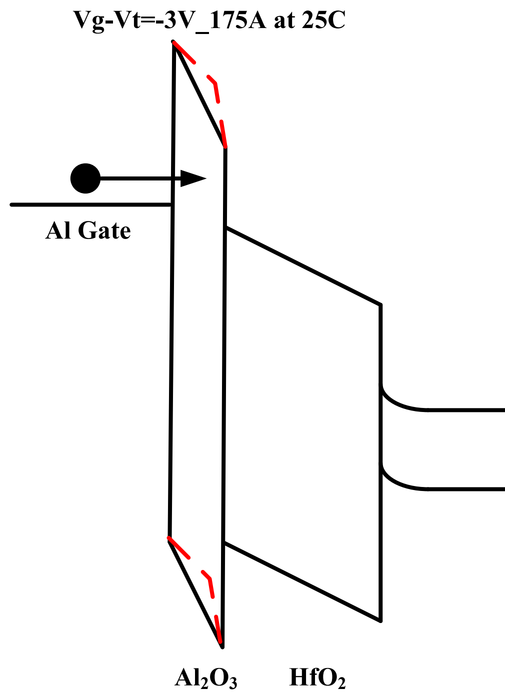


Fig. 4.4 (g) Schematic energy band diagram and the degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 25℃.

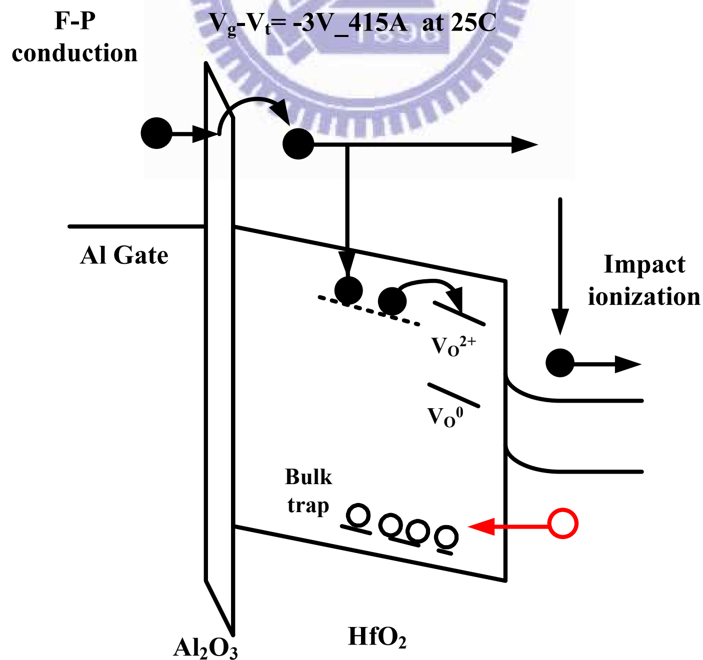


Fig. 4.4 (h) Schematic energy band diagram and the degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 25℃.

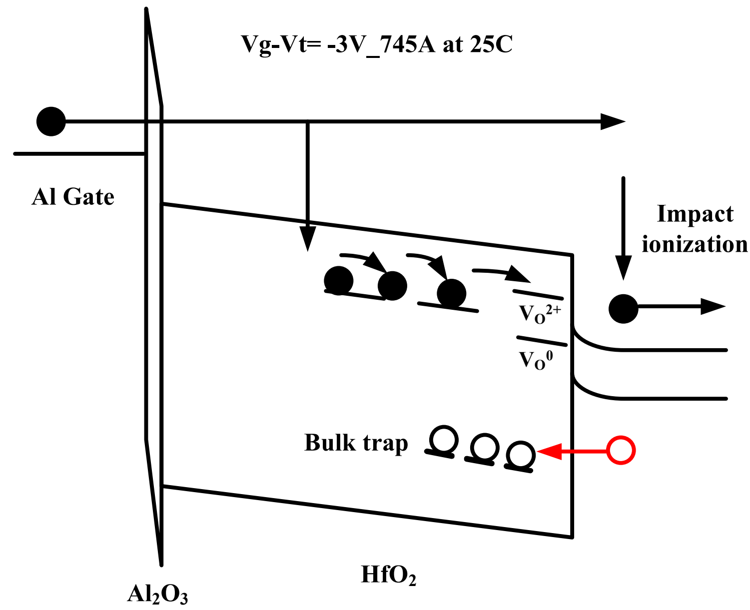


Fig. 4.4 (i) Schematic energy band diagram and the degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 25℃.

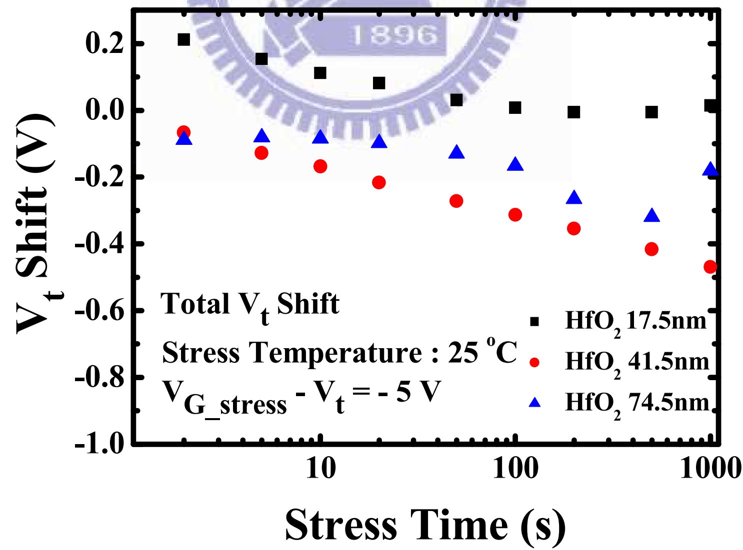


Fig. 4.5 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃.

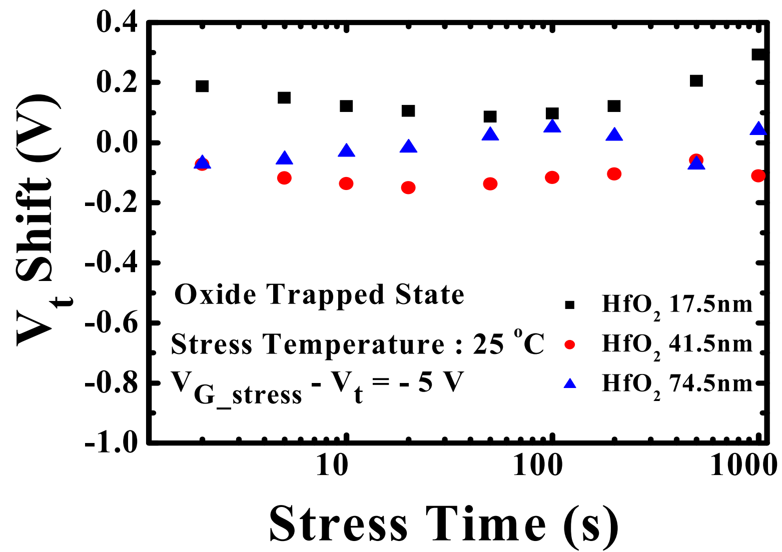


Fig. 4.5 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃.

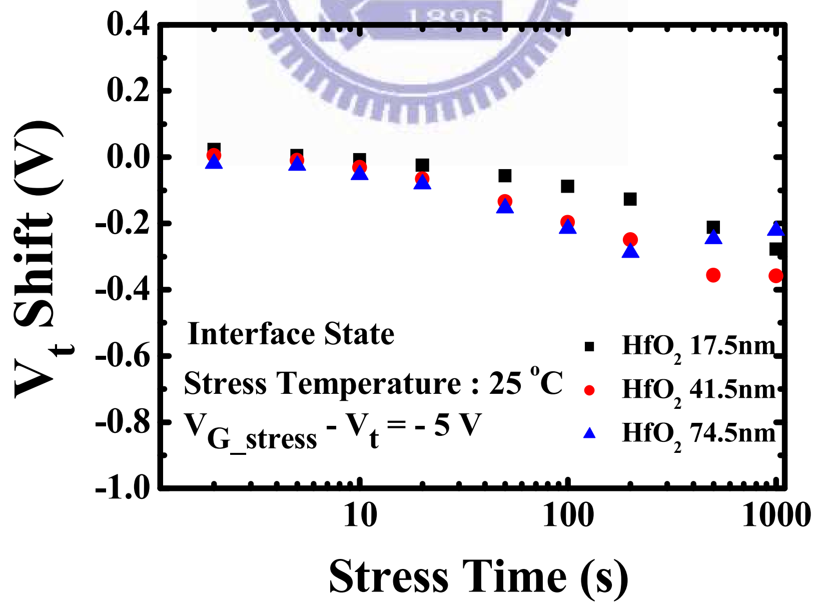


Fig. 4.5 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃.

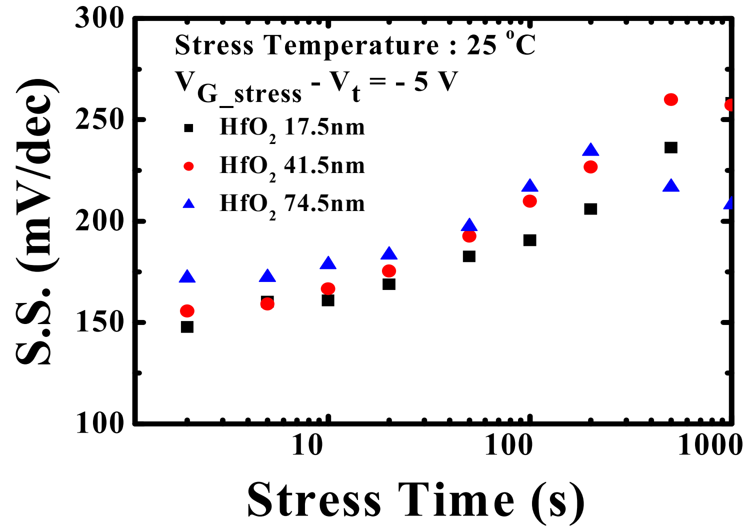


Fig. 4.5 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃.

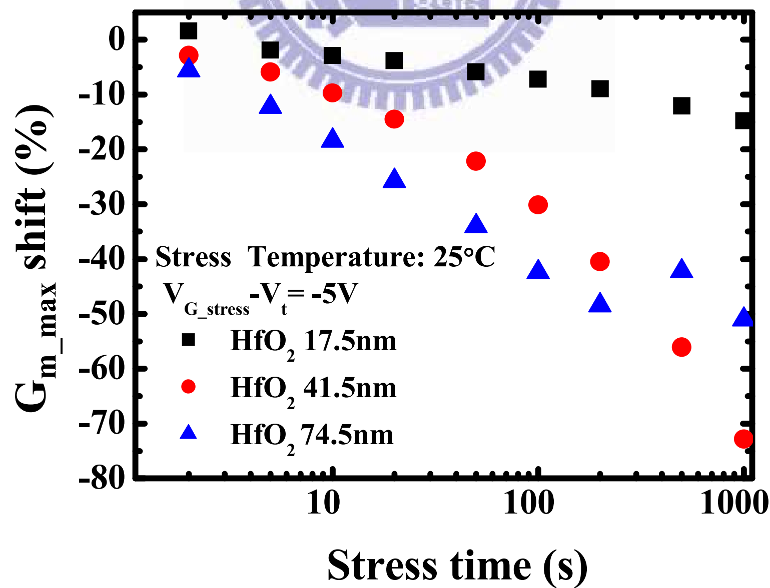


Fig. 4.5 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -5V from 2 to 1000 seconds at 25℃.

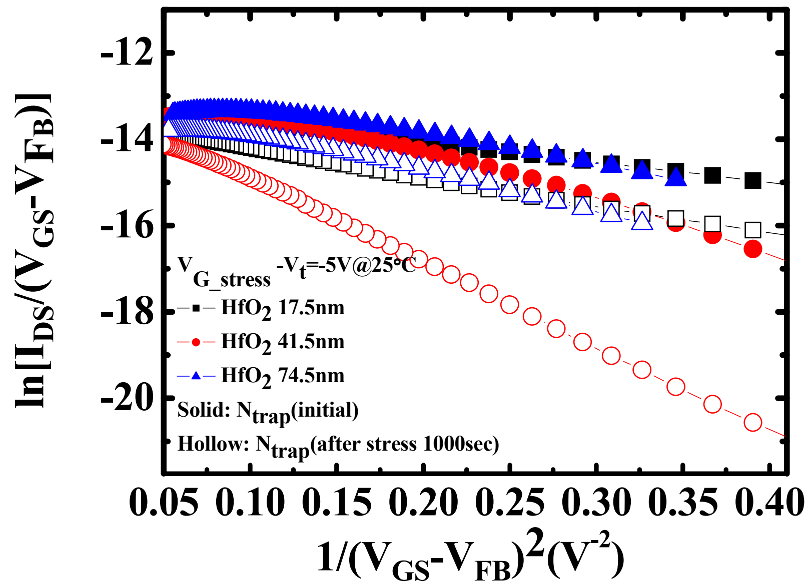


Fig. 4.5 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -5V after tress time of 1000 seconds at 25℃.

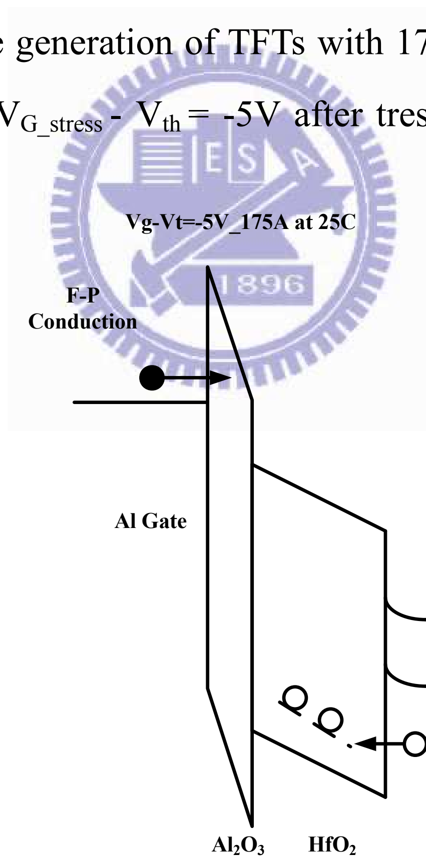


Fig. 4.5 (g) Schematic energy band diagram and the degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25 ℃.

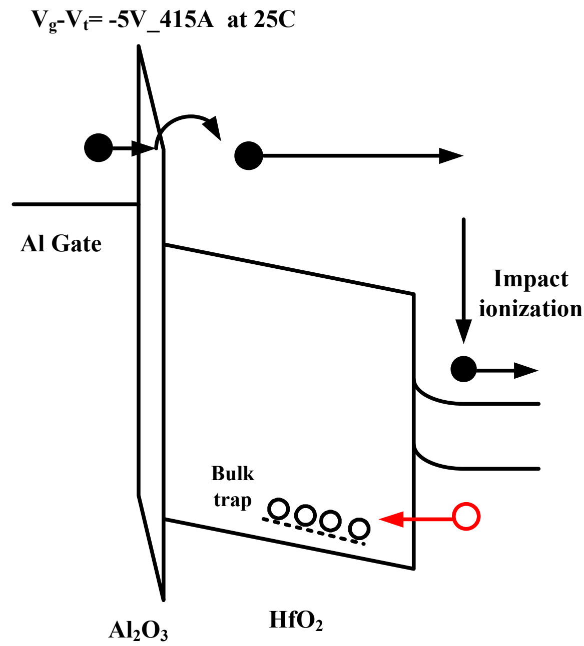


Fig. 4.5 (h) Schematic energy band diagram and the degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25℃.

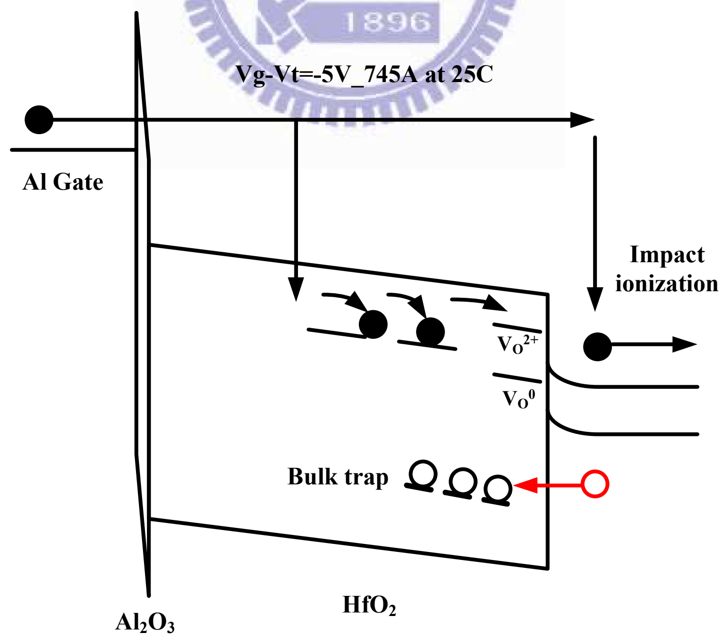


Fig. 4.5 (i) Schematic energy band diagram and the degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-5V at 25℃.

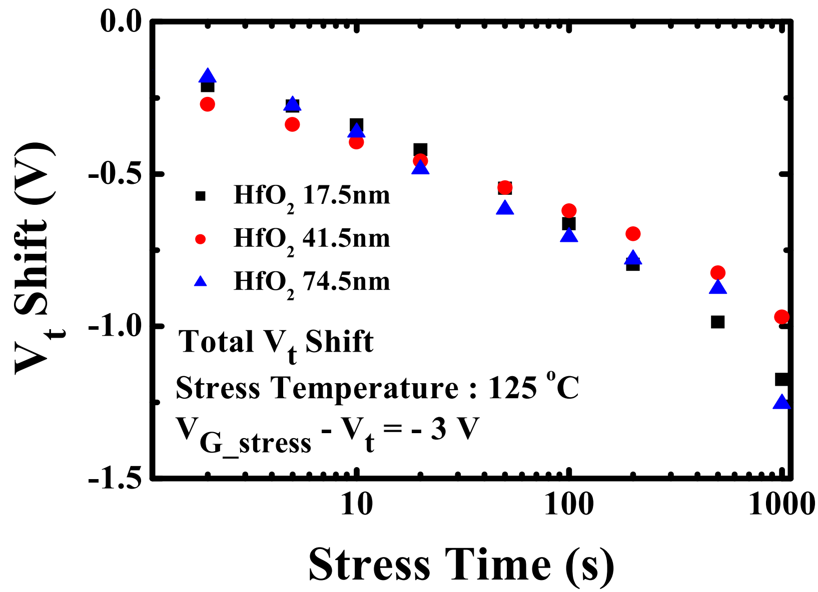


Fig. 4.6 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃.

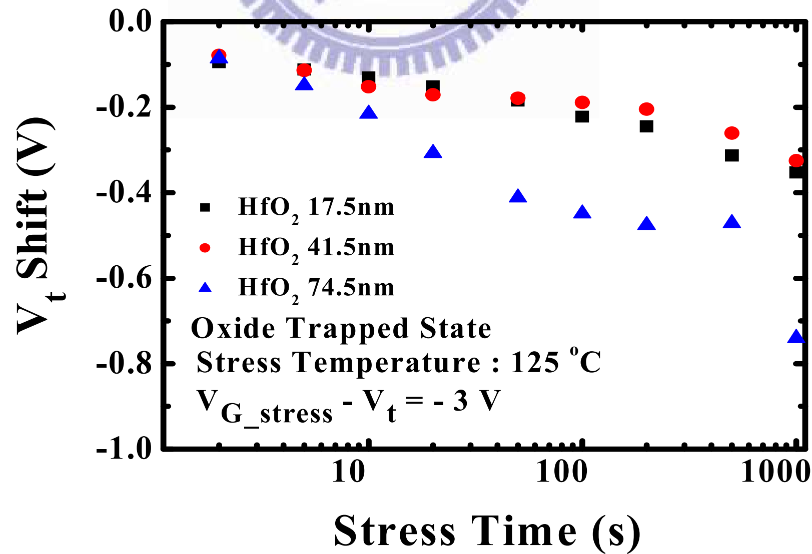


Fig. 4.6 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃.

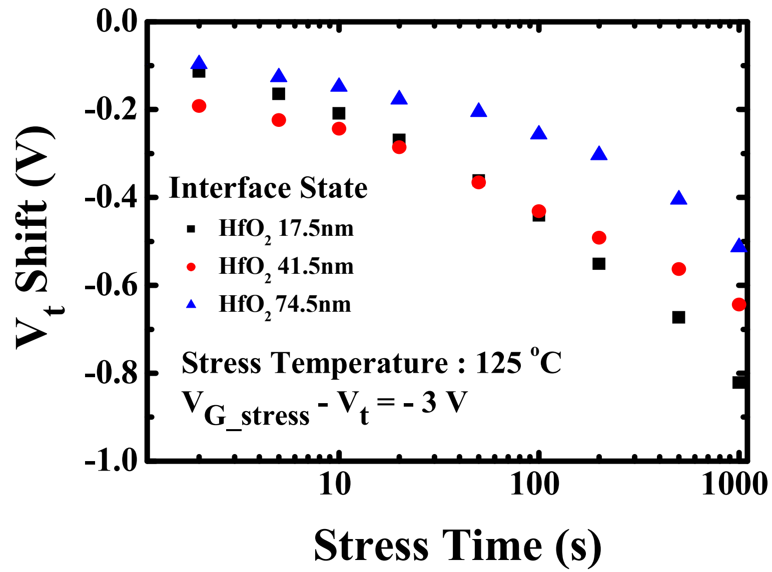


Fig. 4.6 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃.

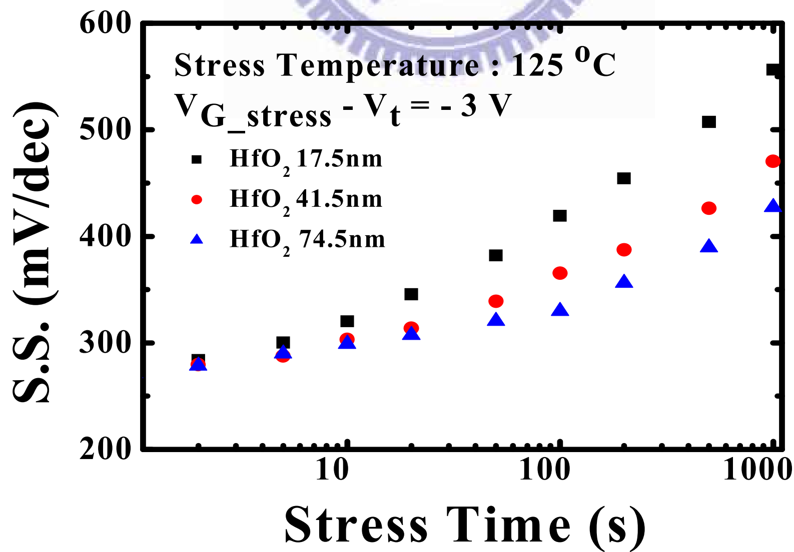


Fig. 4.6 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃.

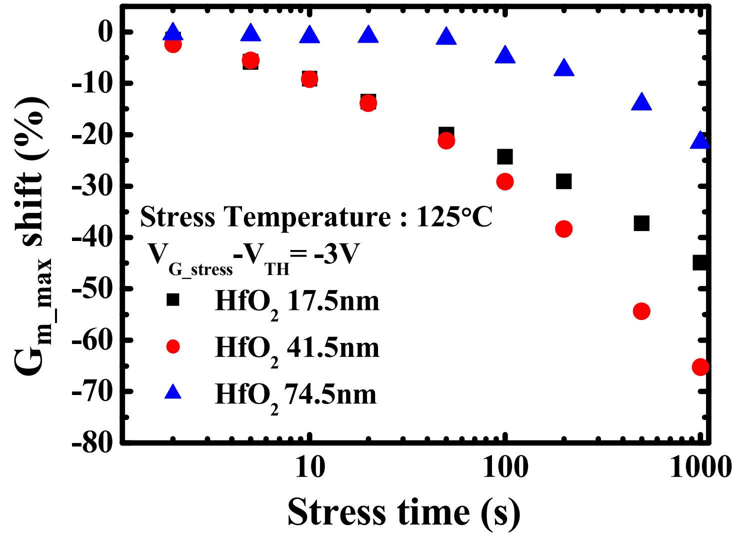


Fig. 4.6 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -3V from 2 to 1000 seconds at 125℃.

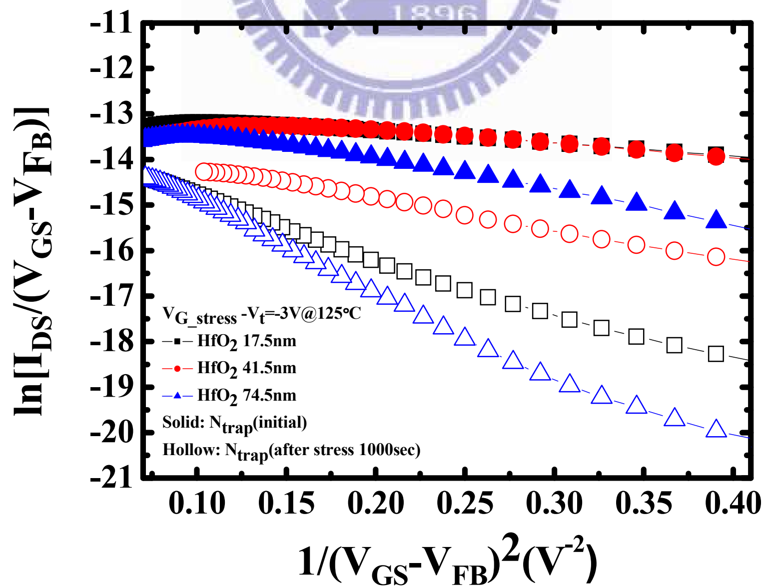


Fig. 4.6 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -3V after tress time of 1000 seconds at 125℃.

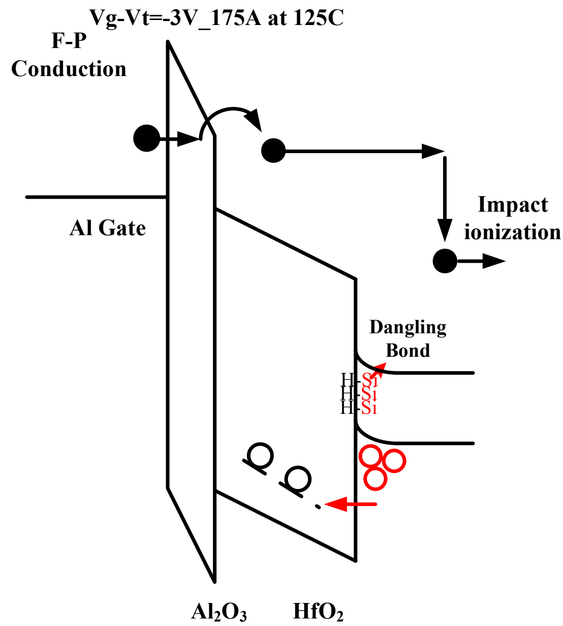


Fig. 4.6 (g) Schematic energy band diagram and the degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 125℃.

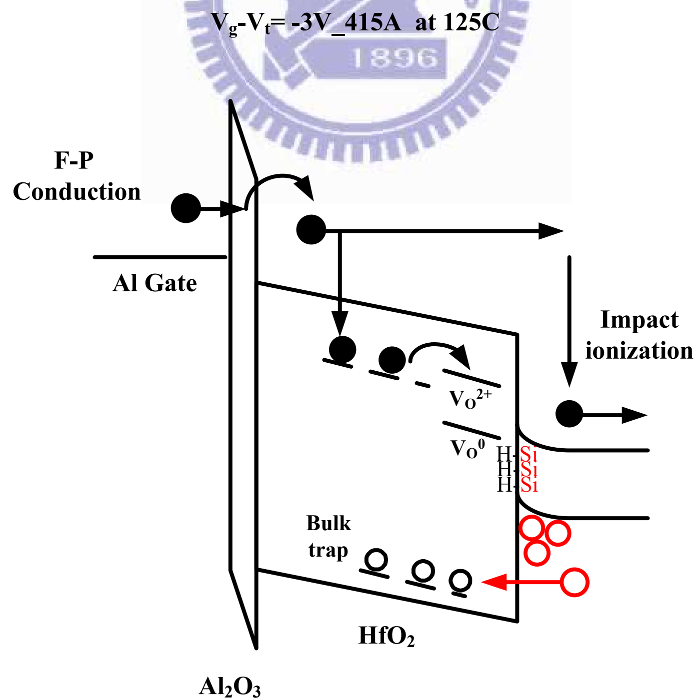


Fig. 4.6 (h) Schematic energy band diagram and the degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 125℃.

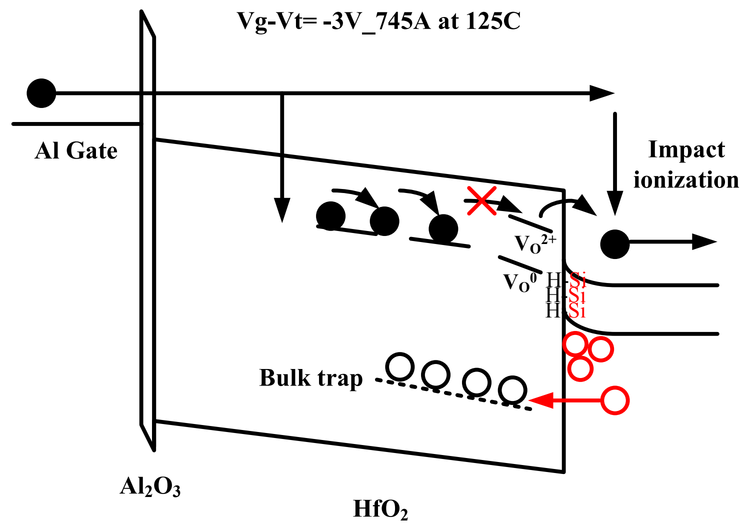


Fig. 4.6 (i) Schematic energy band diagram and the degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-3V at 125℃.

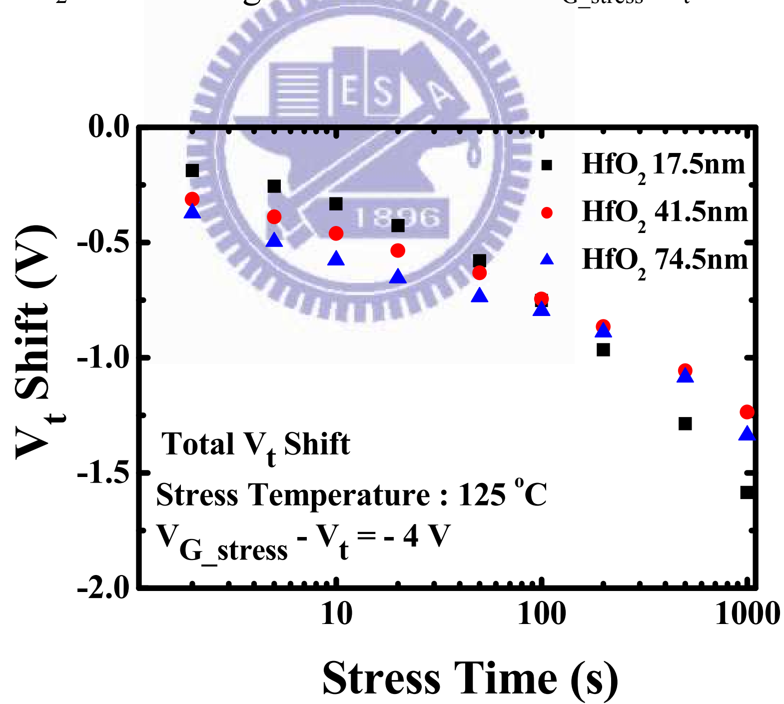


Fig. 4.7 (a) The total V_{th} shift of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃.

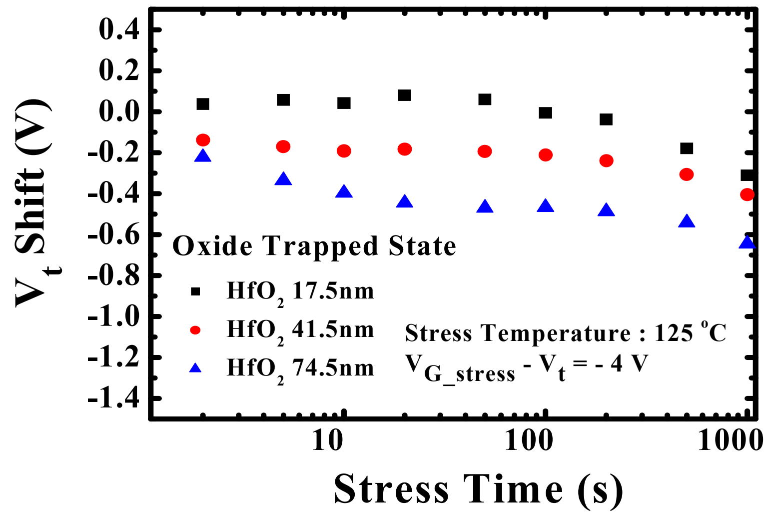


Fig. 4.7 (b) The V_{th} shift resulted from oxide trapping of TFTs with 175, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃.

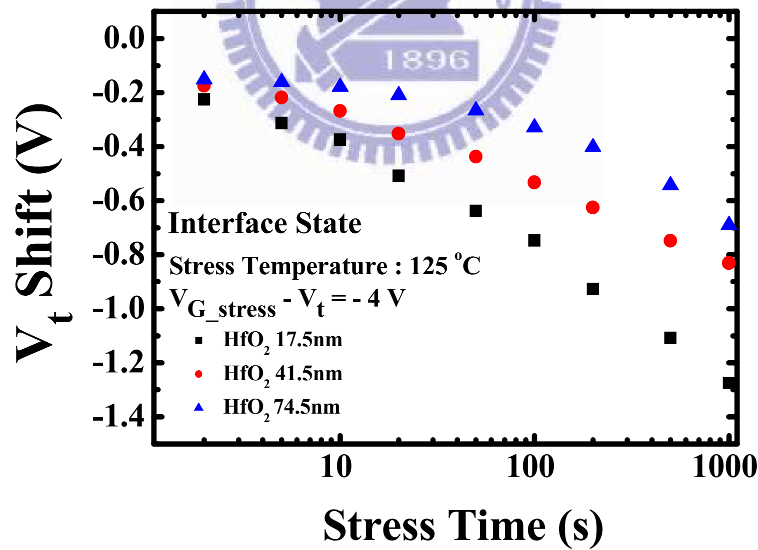


Fig. 4.7 (c) The V_{th} shift resulted from interface states of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃.

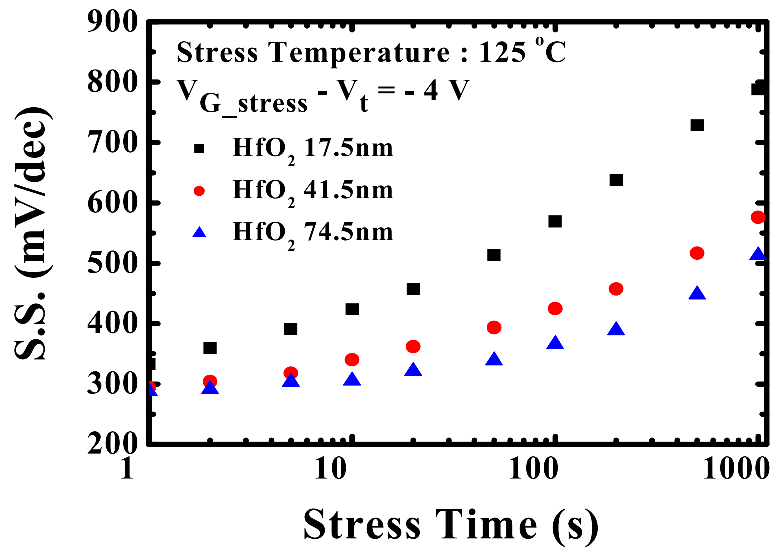


Fig. 4.7 (d) The S.S. degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃.

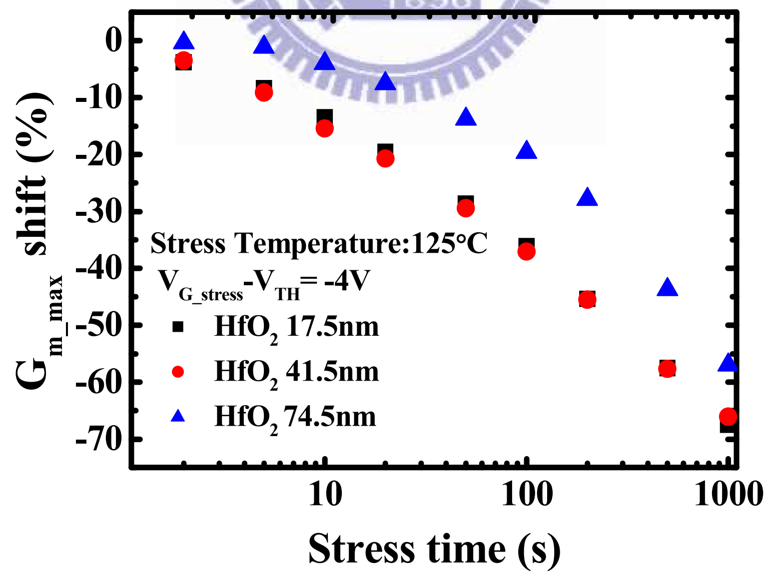


Fig. 4.7 (e) The G_{m_max} degradation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics versus stress time at V_{G_stress} - V_{th} = -4V from 2 to 1000 seconds at 125℃.

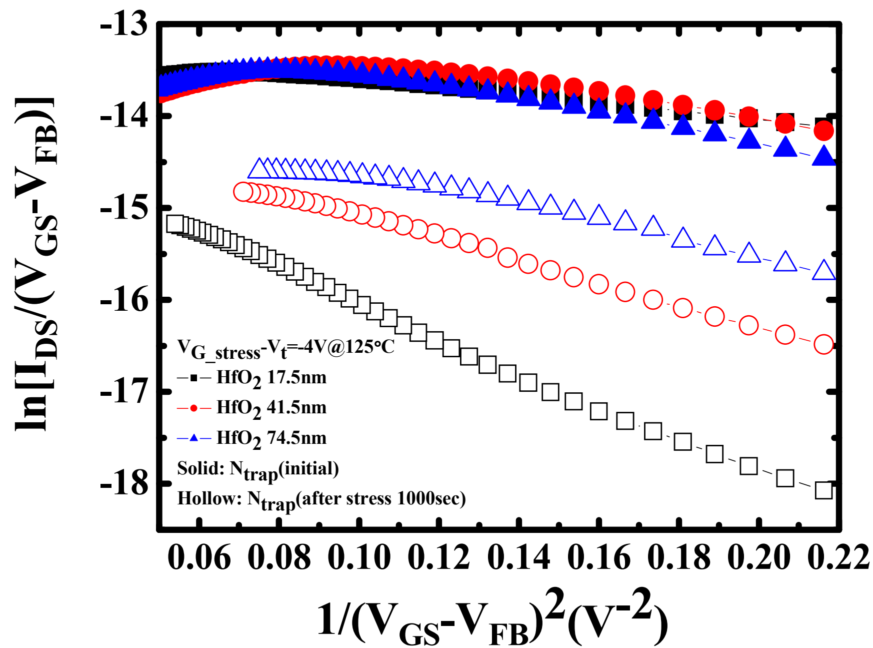


Fig. 4.7 (f) The trap state generation of TFTs with 175Å, 415Å and 745Å-thick HfO_2 gate dielectrics at V_{G_stress} - V_{th} = -4V after tress time of 1000 seconds at 125℃.

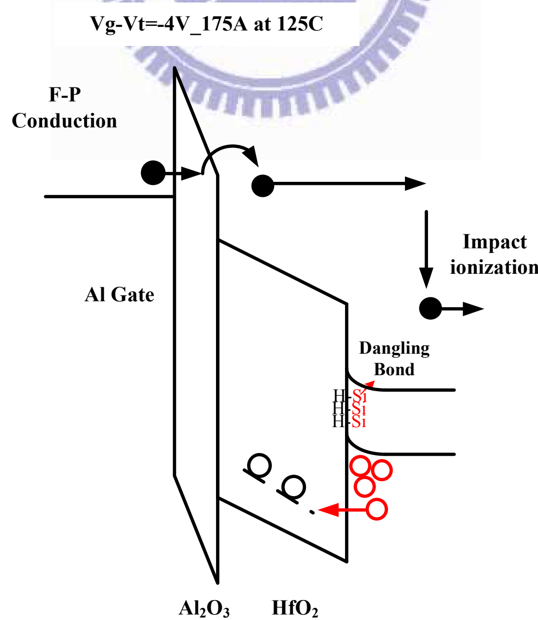


Fig. 4.7 (g) Schematic energy band diagram and the degradation mechanism of the 175Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-4V at 125℃.

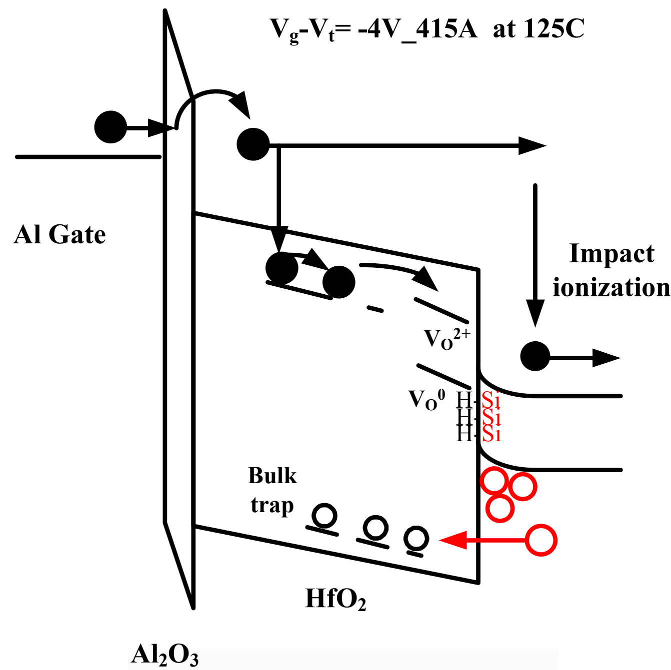


Fig. 4.7 (h) Schematic band diagram and the degradation mechanism of the 415Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-4V at 125℃.

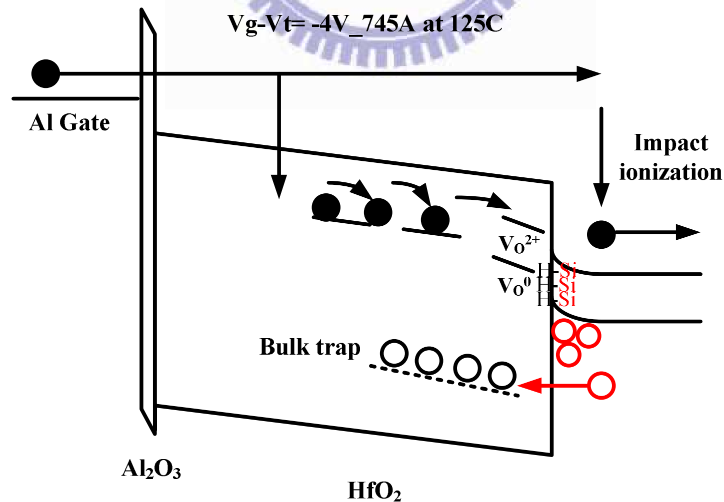


Fig. 4.7 (i) Schematic energy band diagram and the degradation mechanism of the 745Å-thick HfO_2 TFTs during NBTI stress with V_{G_stress}-V_t=-4V at 125℃.

Chapter 4

Reference

[1] D. J. DiMaria et al, E. Cartier, " Mechanism for stress-induced leakage currents in thin silicon dioxide films," *J. Appl. Phys*., vol. 78, pp.3883-3894, 1995.

[2] M. Houssa, L. Pantisano, L.-Å. Ragnarsson, R. Degraeve, T. Schram, G. Pourtois, S. De Gendt, G. Groeseneken, M.M. Heyns, "Electrical properties of high-κ gate dielectrics: Challenges, current issues, and possible solutions," *Materials Science and Engineering: R: Reports.,* vol. 51, pp. 37-85, Apr, 2006.

[3] Z. Xu, M. Houssa, S. D. Gendt, and M Heyns, " Polarity effect on the temperature dependence of leakage current through HfO_2/SiO_2 gate dielectric stacks, " *Appl. Phys. Lett.,* vol. 80, pp.1975-1978, 2002.

[4] K. Ohnishi, C. S. Kang, R. Choi, H,-J, Cho, S. Gopalan, R. Nieh, S. Krishnan, and J. C. Lee," Charging effects on reliability of HfO_2 devices with polysilicon gate electrode," in *Proc. IRPS.*, 2002, pp. 419-410.

[5] F. Fillot, B. Chenevierm S. Maitrejean, M. Audier, P. Chaudouet, B. Bochu, J. P. Senateur, A. Pisch, T. Mourier, H. Monchoix, B. Guillaumot, G. Passemard," Investigations of the interface stability in HfO_2-metal electrodes," *Micro. Electronic. Engineering.* vol. 70, pp. 384-391, 2003.

[6] W.J. Zhu, T. P. Ma, " Current transport in meta;/hafnium oxide/silicon structure," *IEEE, Electron, Device, Lett.,* vol. 23, pp.97-99, 2002.

[7] C. Y. Chen, J. W. Lee, S. D. Wang, M. S. Shieh, P.H. Lee, W. C. Chen, H. Y.

Lin, K. L. Yeh, T. F. Lei, "Negative Bias Temperature Instability on Low-Temperature Polycrystalline Silicon Thin-Film Transistors," *IEEE Trans. Electron Devices.*, vol. 53, no. 12, pp. 2993-3000, 2006.

[8] I.C. Chen, Holland, S.E, C. Hu," Electrical breakdown in thin gate and tunneling oxides," *IEEE Trans. Electron Devices*, vol. 32, pp. 413-422, 1985.

[9] F.V. Farmakis, J. Brini, G. Kamarinos, C.A. Dimitriadis, " Anomalous turn-on voltage degradation during hot-carrier stress in polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 22, pp. 74-76, 2001.

[10] J. Levinson, F. R. Shepherd, P. J. Scanlon, W. D. Westwood, G. Este, and M. Rider, " Conductivity behavior in polycrystalline semiconductor thin film transistors," *J. Appl. Phys*, vol. 53, pp.1193-1202, 1982.

[11] R. E. Proano, R. S. Misage, D. G. Ast, "Development and electrical properties of undoped polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices*, vol. 36, pp. 1915-1922, 1989.

[12] P. Samanta, T. Y. Man, Q. Zhang, C. Zhu, and M. Chan, " Direct tunneling stress-induced leakage current in ultrathin HfO_2/SiO_2 gate dielectric stacks," *J. Appl. Phys*, vol. 100, pp. 094507-094514, 2006.

[13] M. Houssa, V. V. Afanas'ev, A. Stesmans, and M. M. Heyns, "Variation in the fixed charge density of SiO_x/ZrO_2 gate dielectric stacks during post deposition oxidation," *Appl. Phys. Lett,* vol. 77, pp. 1885-1887, 2000.

[14] C. Hu, M. Wang, B. Zhang, M. Wong," Negative bias temperature

instability dominated degradation of metal-induced laterally crystallized p-Type polycrystalline silicon thin-film transistors," *IEEE Trans. Electron Devices,* vol. 56, pp. 587-594, 2009.

Chapter 5
Conclusion

5.1 Conclusion

In this work, the electrical performance and the reliability under the NBTI stress of the p-channel LTPS-TFTs with different thickness of the HfO_2 gate dielectric were compared. It is surprisingly that the G_{m_max} increases with the thickness of the HfO_2 layer. The main cause of this phenomenon can be divided into two parts: (1) Crystallization contributes to the field effect mobility degradation of the p-channel TFTs with the thin HfO_2 gate dielectric. Because enough thermal budget is required to crystallize the HfO_2 films, the thick HfO_2 layer may remain the amorphous phase even if the thin HfO_2 layers have been fully crystallize into the polycrystalline phase. As a result, the field effect mobility degradation of the p-channel TFTs with thin HfO_2 layer is attributed to the additional coulomb scattering resulted from the charges at the grain boundaries or the crystal/amorphous boundaries. (2) Positively charged oxygen vacancy induced grain boundary potential barrier height lowering of the p-channel TFTs: the positively charged oxygen vacancies resulted from the oxygen transfer from the ambient to the HfO_2/poly-Si interface will induce a voltage drop across the HfO_2 layer, which will lower the grain boundary barrier height of the p-channel TFTs and thus enhance the field effect mobility of the HfO_2-TFTs,. With the larger amount of oxygen vacancies in the thicker HfO_2 layer, the enhancement of the field effect mobility will be intensified so that the field effect mobility increases with the thickness of the HfO_2 layer.

The negative bias temperature instability (NBTI) stress of the p-channel LTPS-TFTs with different thickness of HfO_2 gate dielectric was also discussed.

We found that the mechanism contributes to the variation or the degradation of the electrical parameters depends on the thickness of the HfO_2 layers, stress temperature and the stress gate bias. Under the stress conditions at room temperature (25℃), the V_{th} variation is mainly attributed to oxide trapping. For the thin HfO_2 layer, electron trapping dominates the positive V_{th} shift because the interfacial Al_2O_3 layer at the Al/HfO_2 interface is thick for the 175Å sample. On the other hand, electron impact ionization induced hole trapping dominated the oxide trapping of the p-channel TFTs with the thick HfO_2 (415Å and 745Å) layer. Besides, the G_{m_max} degradation increases with the thickness of the HfO_2 layer at room temperature, the degradation of the 175Å and the 415Å sample is mainly attributed to the grain boundary trap states generation in the channel region during stress. However, the G_{m_max} degradation of the 745Å sample is mainly resulted from the neutralization of the positively charged oxygen vacancies. Under the stress conditions at high temperature (125℃), The V_{th} shift is both attributed to the interface states generation and oxide trapping. The interface states generation increases with the decreasing thickness of the HfO_2 layer, indicating that the electric field across the HfO_2 layer will accelerate the transport of the hydrogen-related species in the HfO_2 layer and thus reinforce the interface states generation. However, oxide trapping increases with the thickness of the HfO_2 layer, it is because of that the amount of the electrons tunnel through the Al_2O_3 layer from the Al gate depends on the thickness of the interfacial Al_2O_3 layer. With the high temperature, every electron tunnels through the Al_2O_3 layer must release protons. Therefore, the amount of charge trapping is Al_2O_3 thickness dependent rather than the electric field dependent of the impact ionization rate. As for the G_{m_max} degradation, the G_{m_max} degradation has the

same proportionality with the interface states generation, indicating that the Si-H bonds at either grain boundaries or the HfO_2 /poly-Si interface are damaged at the same time.

In conclusion, the 745Å sample exhibits the best field effect mobility among the three samples. As for the NBTI stress at room temperature, the 745Å Å sample exhibits the minimum V_{th} shift under stress at room temperature but the worst behavior of the G_{m_max} degradation. On the other hand, during the stress at high temperature, the 745Å sample exhibits the minimum interface states generation and G_{m_max} degradation but the worst oxide trapping due to the thin Al_2O_3 layer. Therefore, the V_{th} variation attributed to the NBTI stress at high temperature of the p-channel TFTs with thick HfO_2 layers will be enhanced if the thin Al_2O_3 layer at the HfO_2/poly-Si interface is removed. Above all, the thicker HfO_2 films is better to be utilized as the gate dielectrics for p-channel LTPS TFTs due to its larger field effect mobility and good reliability during NBTI stress.

簡 歷 (Vita)

姓名: 劉聿民

性別: 男

出生日: 1986 年 7 月 9 日

出身地: 台灣 台北市

學歷: 國立交通大學電子物理學系 學士班

2004 年 9 月- 2008 年 6 月

國立交通大學電子物理研究所 碩士班

2008 年 9 月- 2010 年 6 月

碩士論文題目:

具高介電常數閘極絕緣層之低溫複晶矽薄膜電晶體之研究

Investigation on LTPS-TFTs with High-κ Gate Dielectrics