國 立 交 通 大 學

電子物理研究所

碩士論文

利用尖角效應提高寫入電場於薄膜電晶體之記憶體元件應用

The Electrical Field Enhancement of Corner Effects on Thin-Film Transistor Nonvolatile Memories

指導教授 ： 趙天生 博士

研 究 生 ： 林岷臻

中華民國 一百 年 六 月

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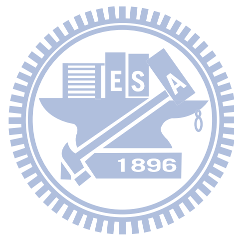
Abstract

For the first time, we propose a special structure to enhance the characteristic of TFT-SONOS memory devices. The memory process is not only simple but also compatible with 3D circuit integration. In this thesis, we investigate the effect of corners along channel width direction on TFT-SONOS memory. The experiments in this study used a local-oxidation of silicon (LOCOS) scheme to fabricate an M-shape in the width direction of TFT-SONOS memory. The programming and erasing operations are performed by the FN tunneling (FN) and Substrate transient hot-hole (STHH) injection, respectively. The improvement of M-shape TFT-SONOS memory is due to the locally electrical field enhancement at corners. On the other hand, the other advantage of this corner structure is the rounded corners improve the "Double Hump" situation. "Double Hump" would be caused by non-uniform charges injection.

Different oxidation thickness would make the platform and structure off-set of corners are different. The oxidation thicknesses are 100 nm and 150 nm, respectively. The more oxidation makes the higher structure off-set, but it is not direct related devices performance. We found out not the longer of effective width would depress the improvement of program/ erase speed.

The design exhibits superior electrical performance, including faster program/ erase speed, excellent data retention at high temperature, and width dependence. Thus, it has the larger application potential for flash memory market in the future.



利用尖角效應提高寫入電場於薄膜電晶體之記憶體元件應用

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摘要

我們提出一種新穎的結構來提高薄膜電晶體之非揮發性記憶體 SONOS 型記憶體的寫入與抹除特性。而這個方法不僅僅非常簡單也可運用於日後的三維結構製程技術中，且仍然能維持良好的可靠度；在此篇論文當中，我們成功的利用傳統元件的 LOCOS 的概念與方法，使在通道的寬度方向上尖角數量的增加，並對尖角數量的增加去做了更進一步的電性探討與可靠度的量測。在寫入與抹除操作的選擇上，我們分別選擇 FN 穿隧注入(FN tunneling) 與基板暫態熱電洞注入(Substrate transient hot-hole injection) ，利用局部電場在尖角二端的集中可提升其記憶體電子注入的速度與電洞的抹除。此結構的另外一個優點是其尖角為較圓滑的轉角，故可以改善由載子的不均

勻注入而產生的雙峰(Double Hump)。

不同的氧化厚度會使通道寬度方向的尖角有不同的平台寬度與高低差，而其氧化厚度分別為 100 nm、150 nm；我們發現並不是氧化厚度越厚所造成的尖角高低落差越大，對於記憶體特性的提升就越大，而是由有效通道寬度的長度去決定，較長的通道寬度會抑制對寫入/抹除速度的提升。

此結構擁有相當多的優點，包含了較快速的寫入速度、在高溫下仍有良好的可靠度特性以及對通道寬度有相當高的相依性。所以此技術有相當大的潛力於未來的記憶體市場。

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在新竹求學的三年中，因為有了許多人的照顧與關懷，讓第一次離開台南到新竹念書的我倍感溫暖，也因為有這麼多人的幫忙，讓岷臻能順利的完成學業。

在這一千多個日子中，我最感謝的就是我的指導教授–趙天生老師，謝謝老師給我機會在您的麾下學習，在您身上我學會的不僅是做研究的熱忱與多方嘗試的精神，更多的是老師對於人生的見解以及待人接物的態度，都讓我受益良多！所謂一日為師終身為父，老師您所教授的一切會是我最珍貴的寶藏。

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春杏小姐、趙子綾小姐、蕭明娟小姐;奈米中心:蘇俊榮博士以及倪月珍小姐，因為有你們的幫助岷臻才能順利完成實驗與論文,也因為有你們讓我在無塵室裡總是能獲得許多笑容。

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林岷臻　誌於　風城交通大學

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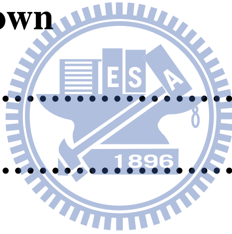

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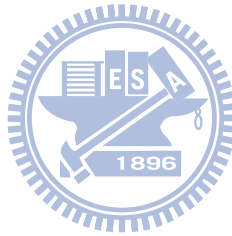

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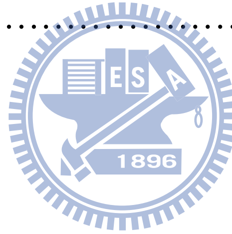

Chapter 1

Introduction

1.1 An Overview of Flash Memory Technologies

Recently, non-volatile memory (NVM) technologies which have extensive market requirement for computer, personal notebook, and electronic portable equipment (USB, MP3 audio player, digital camera, I Pad and so on). It has developed rapidly for a demand in the people's life [1.1]. The density of current storage media and the corresponding non-volatile memories technology for the some applications of the above is shown in Fig. 1.1 [1.2]. The non-volatile memory has been evolving the way from 16Mb and o.35μm of technology node in 1994 to 32Gb and 40 nm of technology node today [1.2]. In addition, the Moore's law accomplishment is the ultimate objective and impetus for scaling down the semiconductor logic devices. Fortunately, the process development of lithography helps us solve performance and number of transistors on chip. There are two major types of non-volatile memories: 1) the code storage application by the NOR architecture 2) the data storage application by the NAND architecture. The differences between NOR and NAND are that NAND has lower cell size, higher device density, fast programming speed, lower power consumption. The non-volatile memory revenues have reached > ＄22.2 billion dollars in 2008, nearly 40% of the total memory market, or 25% of the annual semiconductor market.

1.2 Brief Introduction of FG-type NVM Device

In 1976, *D. Kahng* and *S. M. Sze* invented the first floating gate (FG) structure non-volatile memory at Bell Labs [1.3]. The conventional floating gate NVM

structure as shown in Fig. 1.2, and electrons stored inside the floating gate is the mechanism of data storage in floating gate NVM. The electrons trapped inside floating gate isolated by the top side and bottom side oxide. The bottom oxide (tunneling oxide) is thinner which located between channel and floating gate of MOSFET device. The top oxide (blocking oxide) is thicker which located between control gate and floating gate of MOSFET device. A definition of memory window is the change of V_t (threshold voltage) between the programmed state and erased state as shown in Fig. 1.3.

If there is a point defect in the tunneling oxide, it has a huge chance that electrons can tunnel back to channel by Frenkel-Poole mechanism as shown in Fig. 1.4 [1.4]. Therefore, it has to fabricate defect free oxide. It is theoretical impossible, so the tunneling oxide must be thick enough to prevent electron tunneling back to channel by Frenkel-Poole mechanism as shown in Fig. 1.4 [1.4]. The floating gate NVM devices need thick tunneling oxide (8~11 nm) to keep excellent data retention and endurance characteristics. But there have some drawbacks for thick tunneling oxide: higher operation voltage and slower program/ erase speed.

The scaling down of conventional floating-gate memory devices has met limitations beyond 40-nm node technology [1.5]. According to the International Technology Roadmap for Semiconductors (ITRS), one of the challenges for floating gate NVM device is the scaling of the tunneling oxide, as shown in Table 1.1 and Table 1.2 [1.5]. Tunneling oxide thickness down to 7 nm must be faced with many challenges, such as large stress-induced-leakage-current (SILC), serious short-channel effect and floating gate coupling effect [1.6]-[1.11]. In addition, floating gate is conductive which electrons would leak easily through tunneling oxide by

Frenkel-Pool mechanism after programmed and erased cycles as shown in Fig. 1.5.

Recently, silicon-oxide-nitride-oxide-silicon (SONOS) non volatile memories catch a lot of attentions due to its possibility to overcome the limit of conventional floating gate memories [1.6]-[1.8].

1.3 Brief Introduction of SONOS-type NVM Device

The SONOS-type NVM device structure with discrete traps has been proposed in recent years. The electrons are stored in trapping layer – silicon nitride which located between tunneling oxides and blocking oxide as shown in Fig. 1.6. Due to the discrete trapped state, it can avoid severe stress-induced-leakage-current even at the thinner tunneling oxide of SONOS-type NVM device. Therefore, the SONOS-type NVM device shows many advantages than FG-type NVM device: 1) better data retention 2) lower voltage operation 3) faster program/ erase speed. Excluding better device performance, the SONOS-type NVM device offers some superiorities than FG-type NVM device: 1) simple fabrication process 2) compatible to the CMOS technologies 3) no floating gate coupling effect 4) elimination of the drain induced turn on effect [1.11]-[1.15].

1.3.1 Program Skills

The conventional flash memory devices change the characteristics of threshold voltage by injecting/ removing the electrons into/ from floating gate. The electrons in floating gate are isolated by insulator surrounding and the difference voltage between the initial and final voltage is defined as "Memory window". SONOS-type NVM device has two kinds of the major programming mechanism: Fowler-Nordheim (FN) tunneling, Channel-Hot-Electron (CHE) injection and Source-side injection.

I.   FN Tunneling Programming :

The positive bias is applied to control gate terminal during the programming and the voltage drop across the tunneling oxide make the electric field more than 6MV/cm. Electrons will be inject from channel into trapping layer and we called it Fowler-Nordheim (FN) tunneling as shown in Fig. 1.7. The main drawback of FN tunneling is slower program speed due to lower tunneling current [1.16]. In general, the order for FN tunneling current is about “pA”.

II.   Channel Hot Electron Injection :

The positive biases are applied to control gate terminal and drain terminal during the programming by Channel-Hot-Electron (CHE) injection. The carriers are accelerated by the high horizontal electric field in the channel and carriers would obtain high energy. For this reason, impact ionization would generate extra electron-hole pairs near drain side subsequently. At the same time, the high energy carriers could be inject into trapping layer by vertical electric field as shown in Fig. 1.8. Compared CHE and FN programming mechanisms, where CHE has faster program speed and smaller program voltage. The main drawback of CHE injection is it would damage the tunneling oxide near the drain side. This would be a problem for retention.

1.3.2 Erase Skills

SONOS-type NVM device has two kinds of the major erasing mechanism: Fowler-Nordheim (FN) tunneling and band to band hot hole (BTBHH) injection.

I.   FN Erasing :

The negative bias is applied to the control gate terminal during the erasing by FN tunneling and electron would distrapped from the trapping layer. It is owing to the electric field across to tunneling oxide as shown in Fig. 1.9. The main drawback of FN tunneling is slower erase speed due to lower tunneling current [1.16].

II. Band-to-Band Tunneling Hot-Hole (BTBTHH)

The negative bias and positive bias are applied to control gate terminal and drain terminal during the erasing by band to band hot hole injection. When the negative control gate bias is large enough, the depletion region at drain side under control gate would increase. Holes gain enough energy in depletion region due to high horizontally electrical field and holes would be accelerated to jump the tunneling oxide into storage layer as shown in Fig. 1.10 and Fig. 1.11. Compared FN and BTBHH erasing mechanism, where BTBHH has faster erase speed. However, BTBHH erasing has some oxide reliability issues which would degrade the charge retention ability.

III. Substrate Transient Hot-Hole (STHH) Injection

The source/ drain are N^+ doped compared to the P-type substrate. When we add positive bias to each side of source terminal and drain terminal, and the substrate terminal is ground. The PN junction between source/ substrate and drain/ substrate is both very serious reverse PN junctions. There are a lot of electron-hole pairs generations, because avalanche breakdown happened as shown in Fig. 1.12. Only a small negative bias adds to the gate terminal, a large number of holes would be attracted into the trapping layer at source/ drain side. [1.17]

1.4 Brief Introduction of TFT With SONOS NVM Device

Polysilicon thin-film transistors (ploy-Si TFTs) have attracted much attention for their use in active-matrix liquid crystal displays (AMLCDs). These TFTs can be integrated in driving circuits because of their high mobility and driving current [1.18]. Previous studies propose system-on-plane (SOP) display panels that incorporate various function devices on the display panel, including a controller [1.19] and memory [1.20]. These developments in display technology make displays more compact, reliable, and less expensive to produce. As a result, SOP technology is widely used in portable electronics.

Decreasing the power consumption of a device remains one of the most important challenges in portable electronics [1.21]. Nonvolatile memory (NVM) is often used in such devices because it has two outstanding features: (1) low power consumption, and (2) data preservation. Silicon-oxide-nitride-oxide-silicon (SONOS)-type memory has the greatest important advantage over conventional floating gate flash-memory due to its discrete storage node [1.22]. This node makes it possible to solve problems such as data loss, scaling down issues, and low operation voltage [1.23]. However, SONOS-type NVM still has some weaknesses, such as insufficient programming/erasing (P/E) efficiency, bad retention, and poor endurance [1.24].

Researchers recently fabricated SONOS-type TFT memory using different ways has tried to solve problems, such as: new structures, new materials for trapping/ blocking layer, and electric field enhancement to enhance P/ E speed. Electric field enhancement is easier to improve TFT-SONOS NVM device because electric field would focus at corners and protrusions.

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1.5 Motivation

Recently, system-on-plane (SOP) display panels that incorporate with SONOS-type NVM are very popular. Low power consumption, faster program/ erase speed and excellent data retention have become critical questions, and locally electric field enhancement seems to be the best way to solve those problems. Using new structures is not only difficult to fabricate but also not efficiency improve program/ erase speed. Using new materials (ex: high-κ) to replace trapping/ blocking layer also have some problems like: HfO_2 would crystalline after high temperature annealing and Al_2O_3 had much defect than oxide. Such these problems would be very serious problems for data retention and endurance.

How to enhance the locally electric field is a simple and direct way to improve program/ erase speed ,and not degrade the retention at the same time. Researchers recently fabricated SONOS-type TFT memory using sequential lateral solidified (SLS) [1.24][1.25] with Si protrusions in channel. This method can increase the P/E speed by peak field-enhanced tunneling [1.26]. However, the uniformity of the Si protrusions remains a critical issue for SLS laser annealing [1.27]. Thus, in this thesis we propose a simple way to optimize TFT-SONOS memory with an M-shape channel by locally electric field enhancement. This M-shape structure has not only improved P/E speed through a low cost process but also shown excellent reliability.

1.6 Organization of the thesis

In Chapter 1, an introduction about the general background of non-volatile

memory (ex: floating gate memory, SONOS-type memory and SONOS-type TFT memory) devices are described. SONOS-type TFT memory has got many attentions since system on panel (SOP) is very popular. According to the low power consumption, high program/ erase speed and excellent reliability issues, many novel structures and methods has been proposed. In chapter 2, we will demonstrate the process flow of TFT-SONOS devices and experimental measurement setup which shows schemes for programming/ erasing operation. The TEM cross-section would show to prove corners at each side of channel width direction was made. We will discuss the electric performance for different width dimension, and the devices reliability at different temperatures would also be talk here in chapter 3. In chapter 4, the same structure would make and we follow the EOT scaling down issue, the device performance and reliability both be discuss. Last, the conclusion and future work will be present in chapter 5.

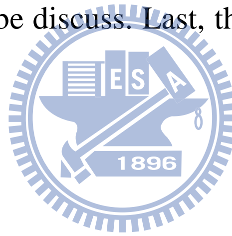
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Table 1.1 The non-volatile memory technology requirements for NAND Flash memory in ITRS 2010 [1.5]

Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
NAND Flash						
NAND Flash technology node – F(nm)	**32**	**28**	**25**	**22**	**20**	**19**
A. Floating Gate NAND Flash						
Tunnel oxide thickness(nm)	6-7	6-7	6-7	6-7	6-7	6-7
Interpoly dielectric material	ONO	ONO	High-K	High-K	High-K	High-K
Interpoly dielectric thickness (nm)	10--13	10-13	9-10	9-10	9-10	9-10
Highest W/E voltage (V)	17-19	17-19	15-17	15-17	15-17	15-17

Table 1.2 The non-volatile memory technology requirements for NAND Flash memory in ITRS 2010 [1.5]

Year of Production	*2010*	*2011*	*2012*	*2013*	*2014*	*2015*
NOR Flash						
NOR Flash technology node – F(nm)	**45**	**40**	**35**	**32**	**28**	**25**
A. Floating Gate NOR Flash						
Gate length Lg, physics (nm)	9-11	9-11	9-11	9-11	9-11	9-11
Tunnel oxide thickness(nm)	8-9	8-9	8-9	8	8	8
Interpoly dielectric material	ONO	ONO	ONO	High-K	High-K	High-K
Interpoly dielectric thickness (nm)	13-15	13-15	13-15	8-10	8-10	8-10
Highest W/E voltage (V)	7-9	7-9	7-9	6-8	6-8	6-8

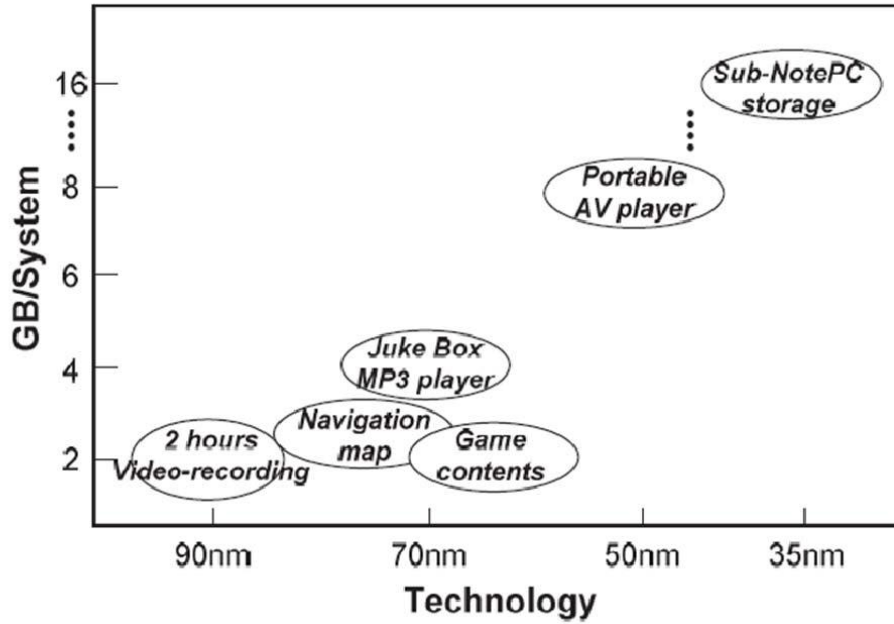

Fig. 1.1 Potential applications of NAND Flash memory comparing projected cost reductions with Flash capacitor by technology.[1.2]

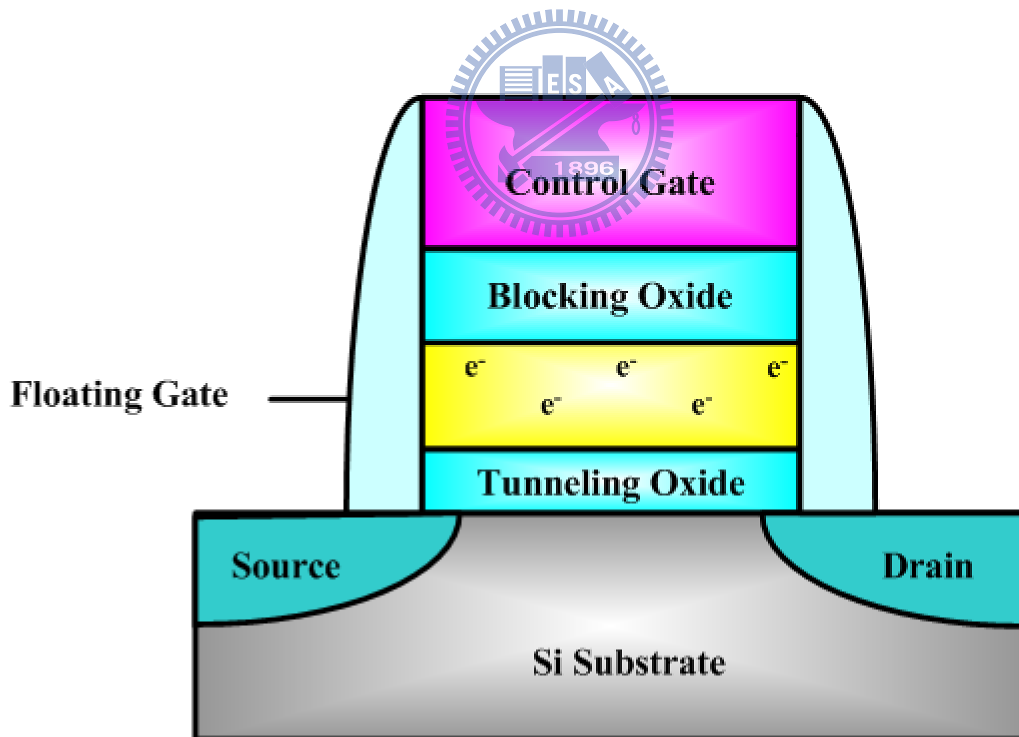

Fig. 1.2 The schematic of the conventional floating gate non-volatile memory devices.

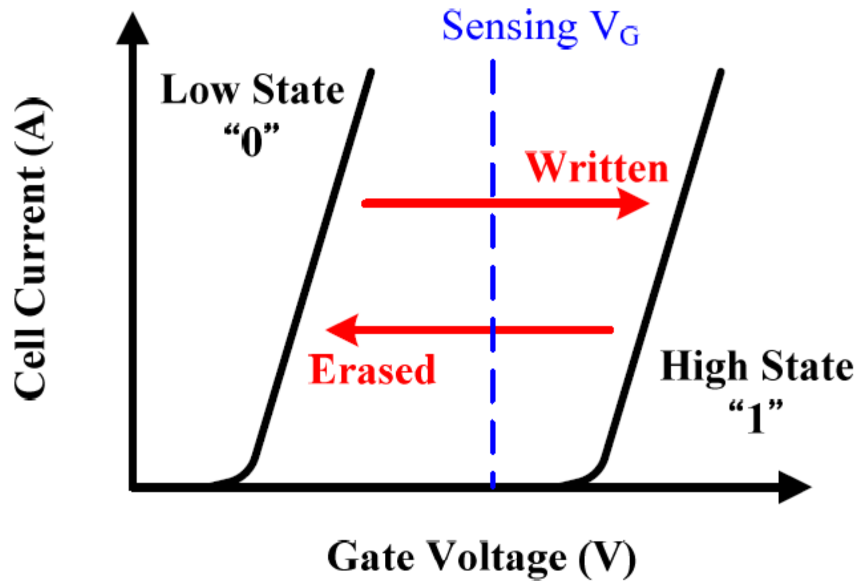

Fig. 1.3 The Id-Vg curves for the different program state "1" and erase state "0" ; showing the V_t shift and memory window.

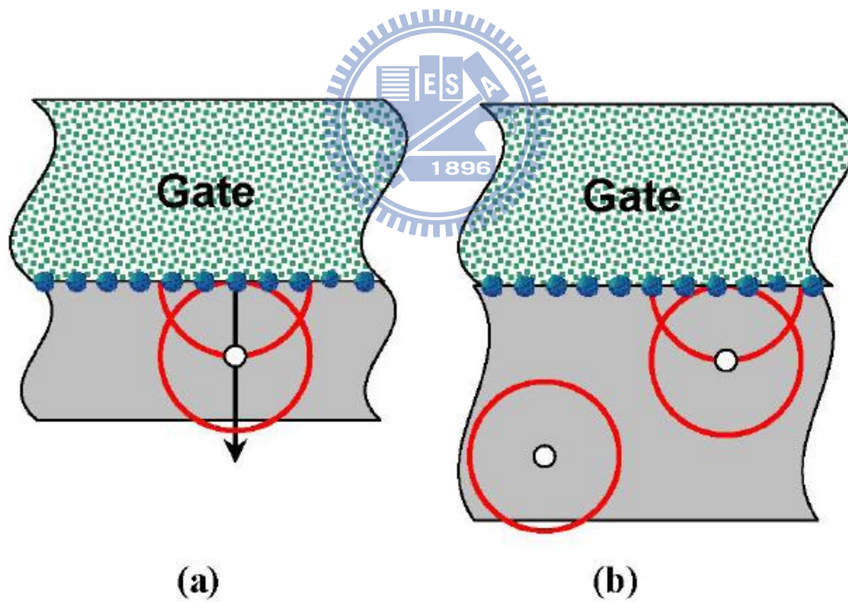

Fig. 1.4 Schematic of the electron loss by Frenkel-Poole mechanism (a) a single point defect in thin tunneling oxide may induce Frenkel-Poole tunneling (b) a single point defect in thick tunneling oxide is insufficient to cause Frenkel-Poole tunneling.

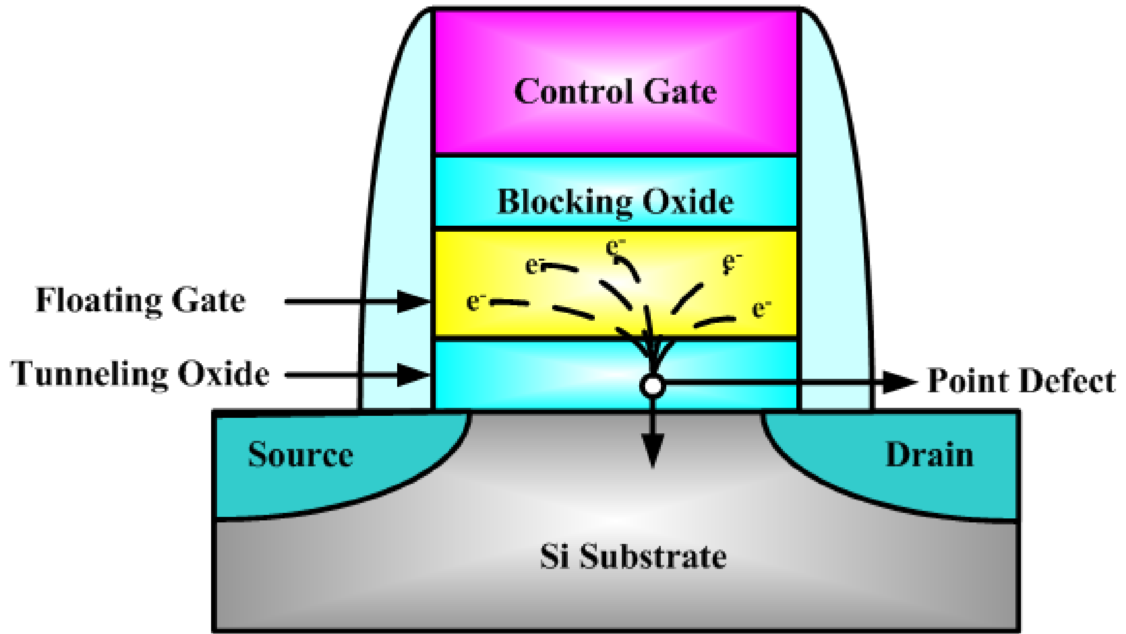

Fig. 1.5 Schematic of the total electron will be leaked through tunneling oxide by Frenkel-Pool mechanism due to floating gate is conductive.

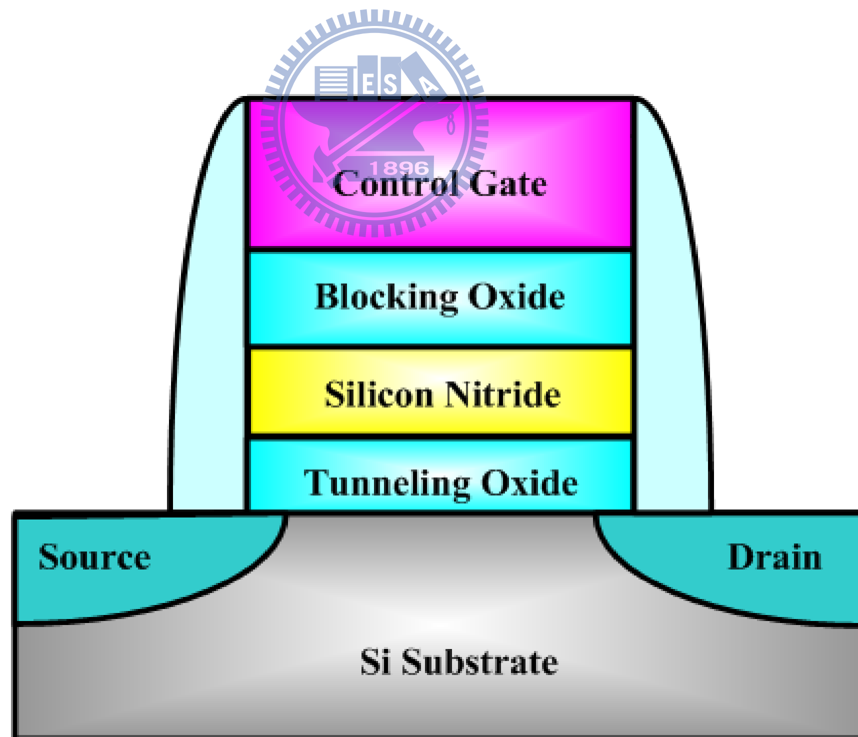

Fig. 1.6 Schematic of the conventional SONOS-type non-volatile memory devices.

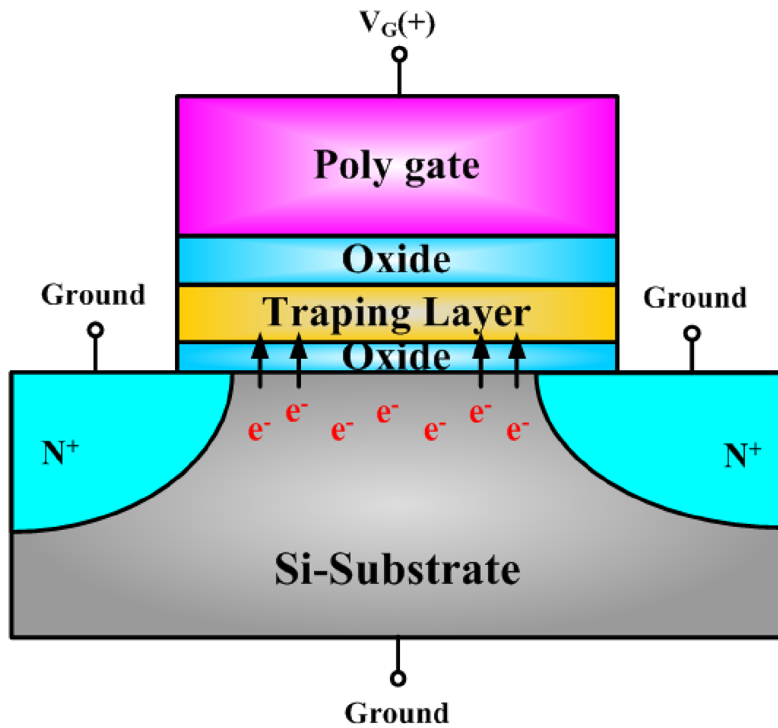

Fig. 1.7 The SONOS NVM devices were programmed by FN tunneling mechanism.

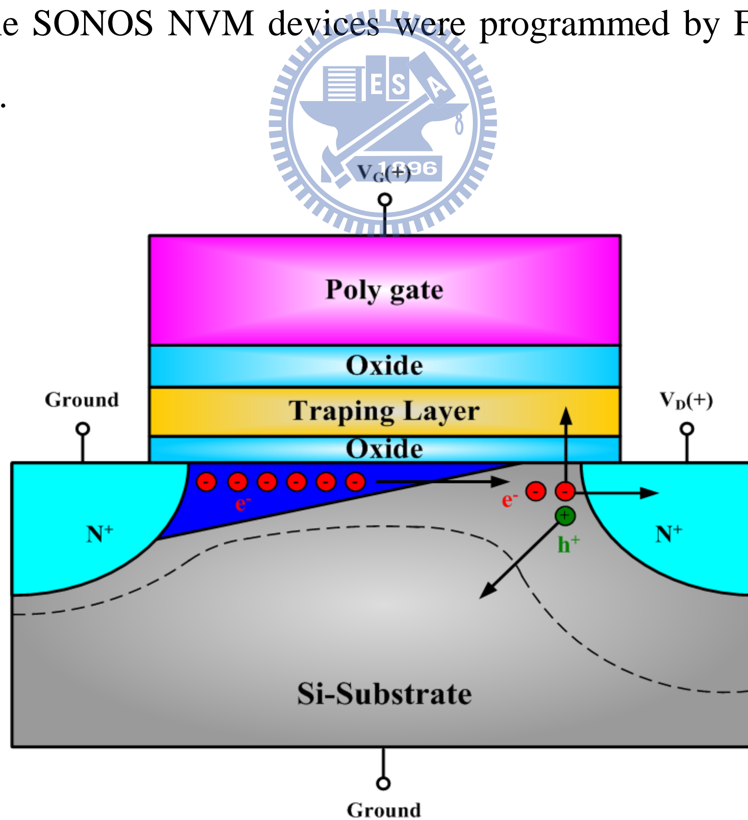

Fig. 1.8 The SONOS NVM devices were programmed by Channel Hot Carrier mechanism.

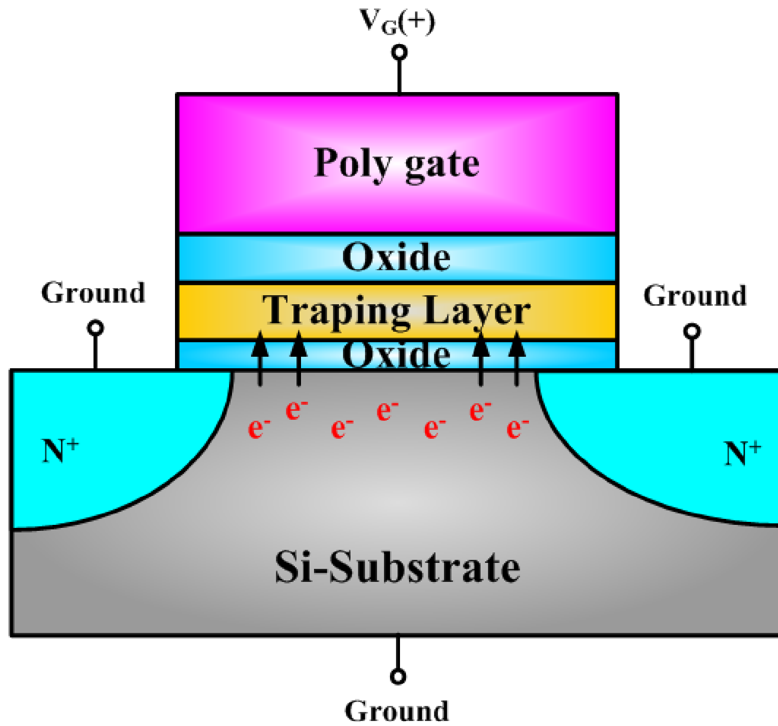

Fig. 1.9 The SONOS NVM devices were erased by FN tunneling mechanism.

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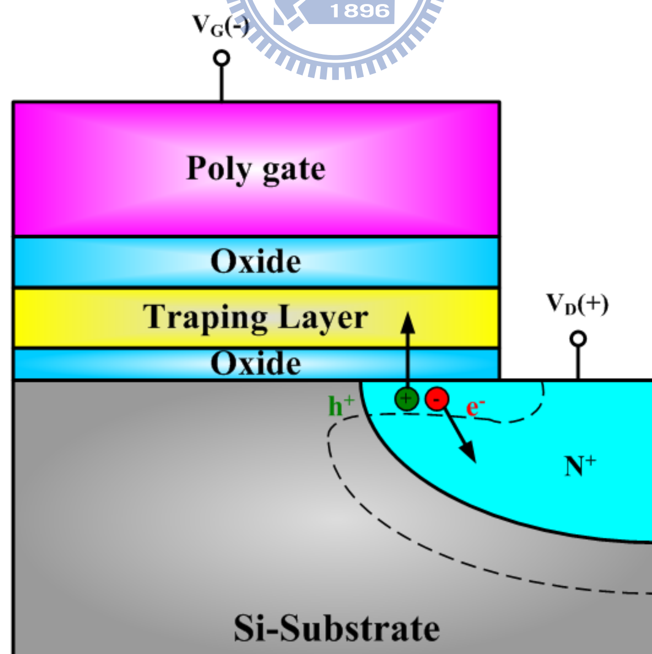


Fig. 1.10 The SONOS NVM devices were erased by BTBHH mechanism.

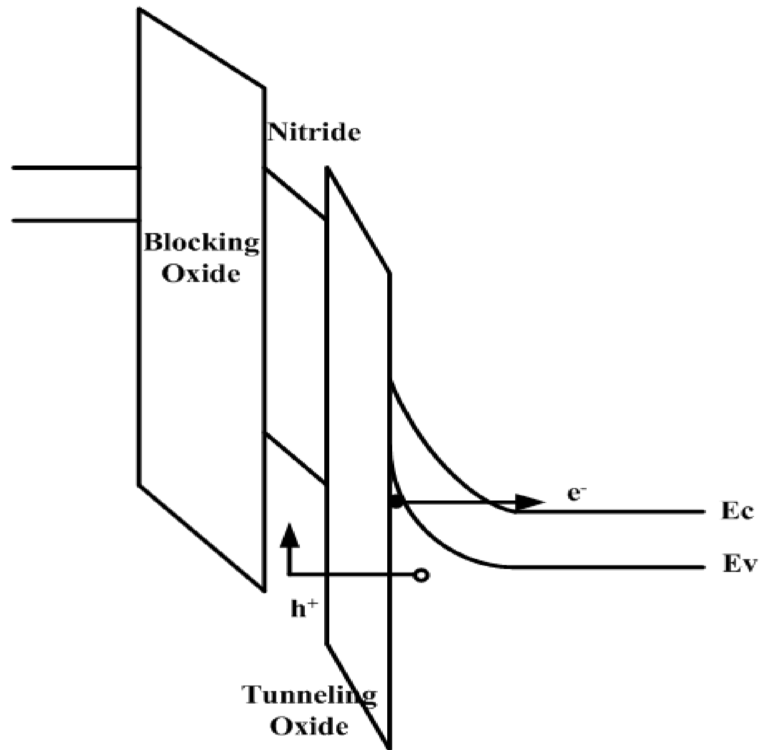


Fig. 1.11 The energy band diagram of the SONOS NVM device during erasing by BTBHH mechanism.

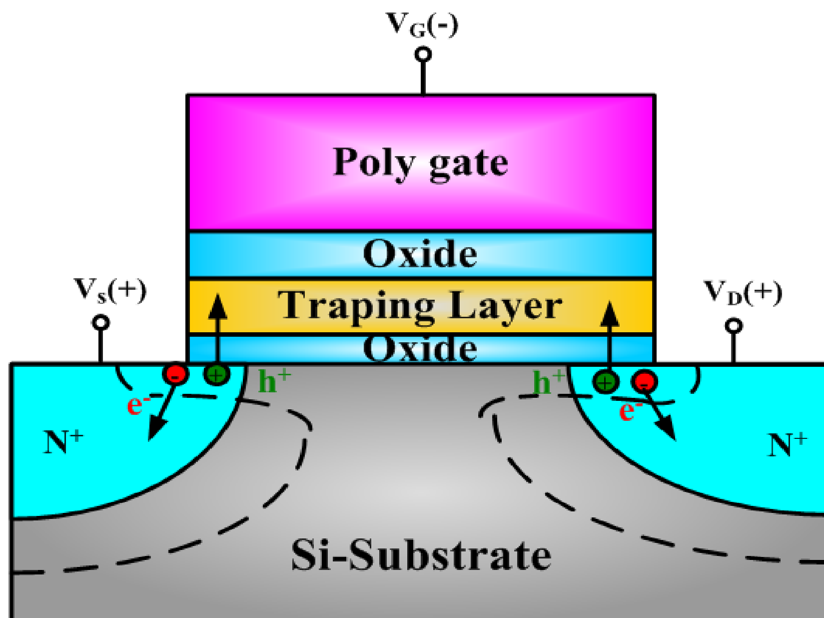


Fig. 1.12 The SONOS NVM devices were erased by STHH mechanism.

Chapter 2

Device Fabrication and Experimental Setup

2.1 Introduction

Since the traditional floating gate is replaced by the charge trapping layer [2.1], the tunneling oxide thickness can be scaled down to 3nm. Therefore, the programming and erasing speed is about the microsecond and millisecond range which is enhanced. Many studies point out the charge retention time would be related to the oxide thickness. As the oxide thickness decreased, the probability of charges detrapped by trap – assist – tunneling is multiplication [2.2]-[2.5]. In order to maintain the retention time over ten years, the oxide thickness is recovered to 4~5 nm to achieve the requirement of devices reliability. In this chapter, we will introduce a new structure to optimize TFT-SONOS memory with M-shape channel and this structure improves P/E speed through a low cost process. This TFT-SONOS memory with lower V_t, faster programming speed and longer retention can be obtained, highly promising for realization of 3D circuit integration. The performance and reliability of devices, including data retention, P/E cycling test, and gate/ drain disturbance were investigated.

2.2 Experimental Procedure

A 6-in (100) bulk silicon wafer was used as the base material substrate. First, a 500-nm thermal oxide layer was grown on the Si-substrate to form a glass substrate. A 150-nm amorphous silicon (α-Si) layer was then deposited using low-pressure chemical vapor deposition (LPCVD). The deposited α-Si layer was recrystallized by solid-phase crystallization (SPC) at 600℃ and annealed for 24 hr in N2 ambient.

Then, 35-nm wet oxide and 150-nm LPCVD nitride films were deposited on the wafers. Active regions were patterned by lithography and a dry etching process, as Fig. 2.1 (a) shows. Wafers were wet oxidized to obtain 140-nm wet oxide, forming a bird beak at the channel-width direction. This is similar to local oxidation of silicon (LOCOS) isolation in a MOSFET process, as Fig. 2.1 (b) shown. Using the 140-nm wet oxide as a hard mask to define TFT - island two corners were added to each side of the channel width direction as Fig. 2.1 (c) shows. The control samples excluded this LOCOS-step. All wafers underwent a BOE-dip to remove oxidation and simultaneously create an undercut under the poly-Si, creating two additional corners in the width direction, as Fig. 2.1 (d) shows. A 47-nm oxide-nitride-oxide (ONO) multilayer gate dielectric was deposited by LPCVD, including a 15-nm tunneling oxide, 12-nm nitride trapping layer, and 20-nm blocking oxide. A 200-nm undoped poly-Si layer was then deposited, and a gate defined by lithography. Fig. 2.1 (e) shows the control sample without an M-shape channel for comparison. The source, drain, and gate were then doped with self-aligned implantation of phosphorous. A 550-nm oxide passivation layer was deposited and contact holes were patterned. Finally, Al metallization was performed.

As shown in Fig. 2.2, we could assume our structure is composed by three transistors, like A-A', B-B' and C-C'. The A-A' and C-C' are the part of source and drain. Both of them also have additional corners at channel-width direction. The B-B' has oxide-nitride-oxide and poly-si gate and it also shows it has addition corners at channel-width direction. From Fig. 2.2, it helps us to understand our structure well through channel-width direction.

2.3 Measurement and Equipment Setup

The experimental setup for the I-V and threshold voltage characteristics measurement of this TFT-SONOS device is illustrated in Fig. As shown in Fig. 2.3, the main electrical characteristics measurement and control system here are Keithley 4200 which equipped with programmable source-monitor units (SMU) and a high resolution current amplifier with pico-ampere range to facilitate the device current measurement. The Agilent 81110A with two pulse channel could provide the high timing resolution for transient pulse level and P/E cycling endurance test for flash memory device. It's the main equipment to afford the programming and erasing pulse. For this reason, in order to precisely control the pulse level and pulse timing of Agilent 81110A memory device. It's the main equipment to afford the programming and erasing pulse. In addition, the C++ language is used to control different measurement instruments, such as the low leakage current machine Keithley 708A with 10-input and 12-output switching matrix switches the signals automatically to the device under test (DUT) immediately, the device reliability after P/E cycling stress and gate disturbance…etc.

2.4 Operation of Program/ Erase Mode

Memory devices are operated by variety principles, and major program mechanisms are Fowler-Nordheim (F-N) Injection [2.6]-[2.8] and channel-hot-electron (CHE) injection [2.9]-[2.11]. The programming mechanism of channel-hot-electron (CHE) injection requires high positive voltage connected to the gate and drain terminals. While the programming scheme switches on, as described as we mention before, the carriers are accelerated by high lateral electrical field that will produce the large amount of impact ionization. The lots of electron-hole pairs would redirect due to the high vertical electrical field in the neutral gap region which

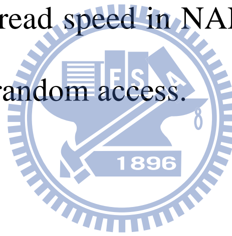
increases the probability of electrons injection into nitride trapping layer. The electron injection efficiency is lower and the high energy electrons would damage the tunneling oxide. Due to those reasons, we choose the programming mechanism of Fowler-Nordheim (F-N) injection as shown in Fig. 2.4. Only positive voltages connected to the gate terminal and Source/ Drain/ Well terminals are grounded. The voltage drop makes the electric field of tunneling oxide is more than 6 MV/cm, and electrons would be injected from channel into trapping layer owing to the electric field applied to tunneling oxide. The erase operation uses the substrate transient hot-hole (STHH) injection mechanism [2-12]. Fig. 2.5 shows the erase characteristic with negative bias connected to the gate terminal and huge positive bias connected to source/ drain terminals, where a huge reverse bias is added to the PN junction to cause the PN junction in breakdown. An avalanche breakdown in PN junction caused a lot of electron-hole pairs, and only added a small gate bias ($V_g > 0V$) a large number of holes will be attracted then injected into nitride layer to erase electrons.

2.5 Disturb Characteristics

Fig. 2.6 shows the possible disturbances phenomenon of equivalent circuit schematic in NAND architecture. In general, there are including program disturbance and read disturbance [2-13][2-14]. The disturbed phenomenon of programming process happened to the common word-line (WL) device in memory array is named gate disturbance. This is because the adjacent memory cells used the same word-line result in the electrical stress on the unselected cell. It may make slightly electrons tunneling into the trapping layer which to cause threshold voltage fluctuations. The serious program disturbance means that the unselected memory cell became high state from low state during the long time stress. Another program disturbance condition is

that electrons in nitride trapping layer may detrap by Frenkel-Poole emission and then tunneling to control gate through the blocking oxide by defects while applying the large positive bias at gate terminal. Such the excess leakage current will degrade the device reliability, too.

The second phenomenon is the read disturbance. Especially in NAND array, while the selected cell is reading, all of the memory cell in the string must be turned on to form the channel conduction. As a result, the unselected memory cell in NAND string will be stressed by the high pass voltage in reading mode. It will lead the electrons injecting into storage layer results in non-ideal effect of threshold voltage increase, called read disturbance. In addition, in the NAND architecture, the unselected memory cells act like the serial resistance in the circuit brings read current degradation. For this reason, the read speed in NAND architecture is slower than the NOR architecture and can’t read random access.



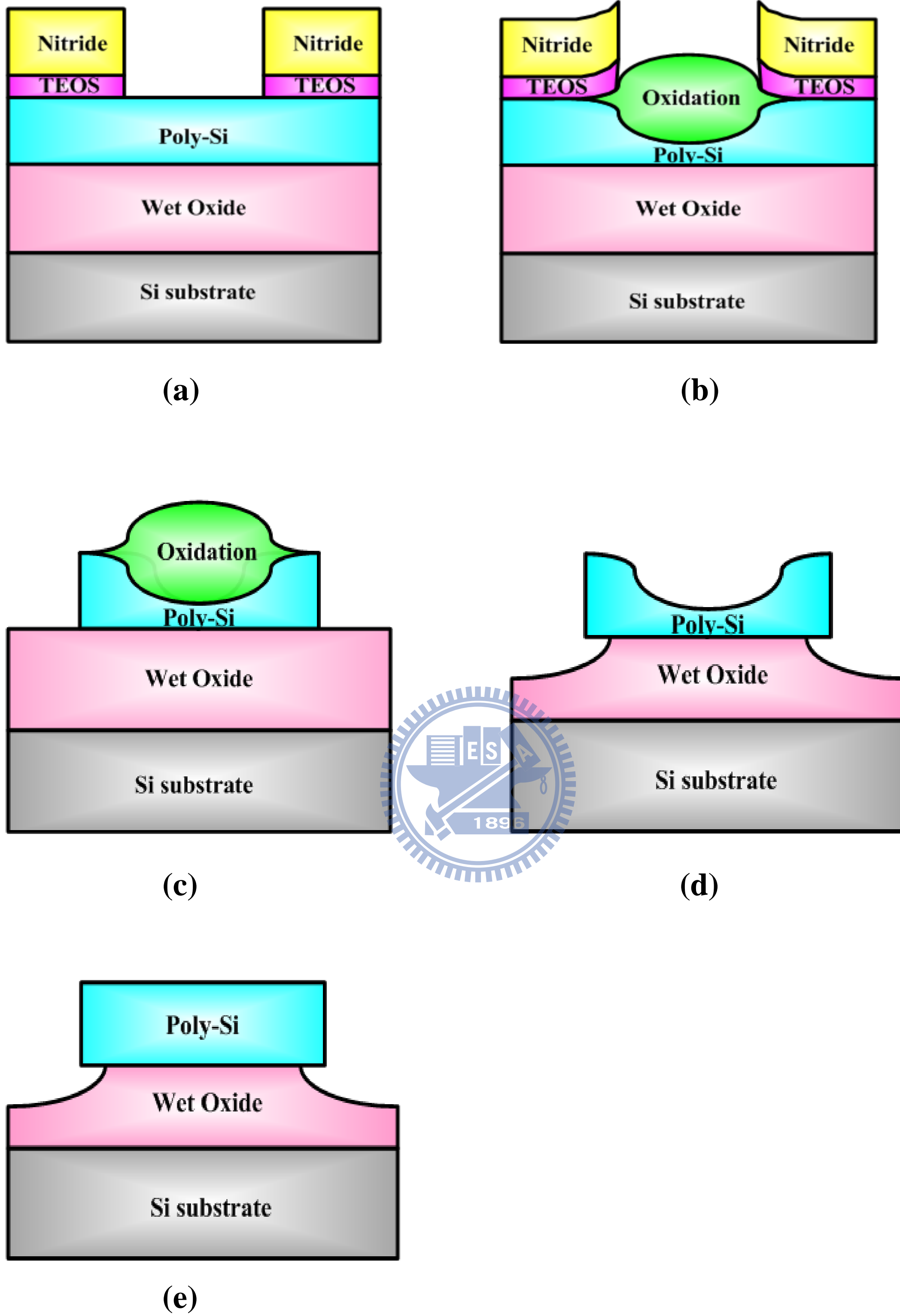


Fig. 2.1 (a) (b) (c) (d) Schematic view of an experimental process for fabricating an M-shape channel. (e) Schematic view for the control sample.

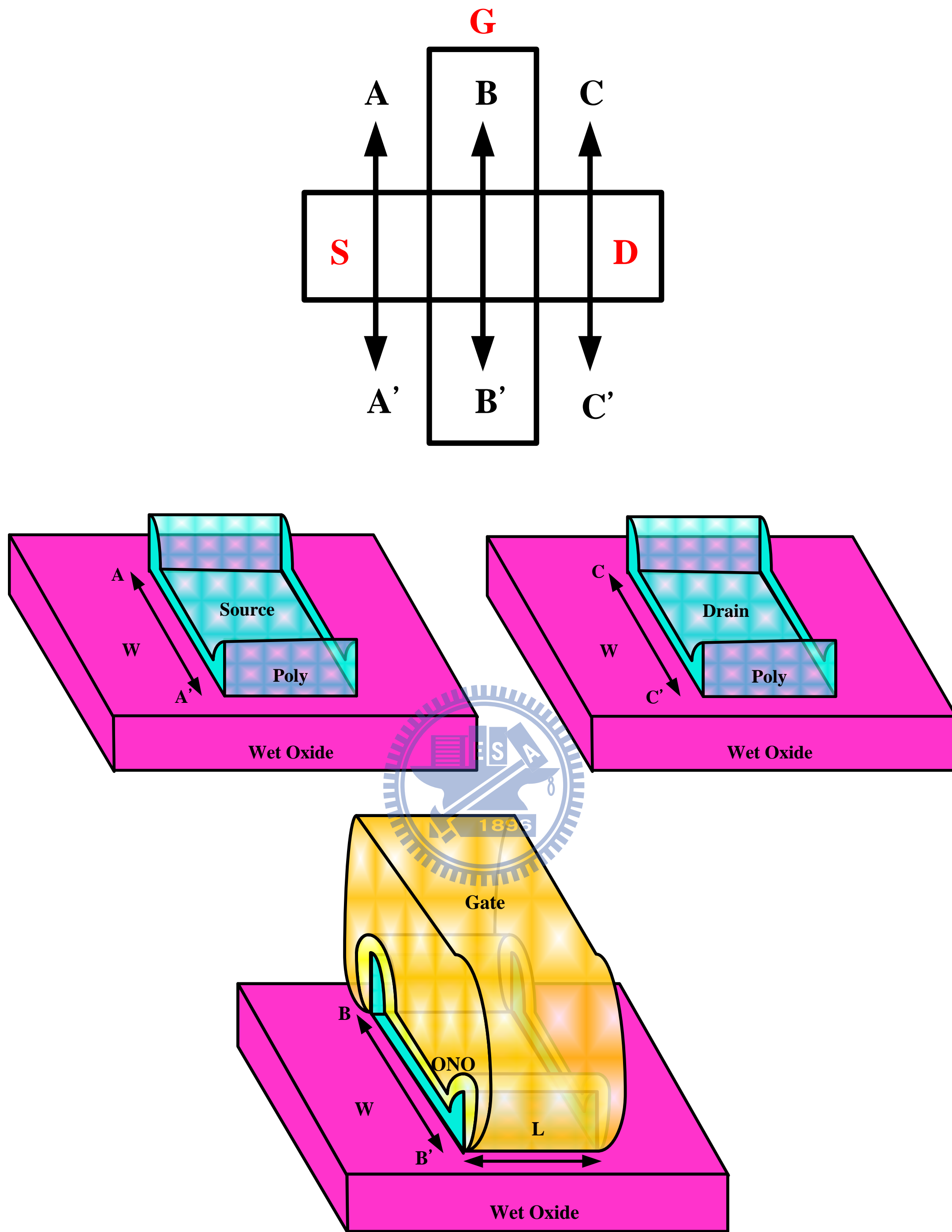


Fig. 2.2 Schematic view of this structure from channel-length direction. It is clearly shown the additional corners at channel-width direction.

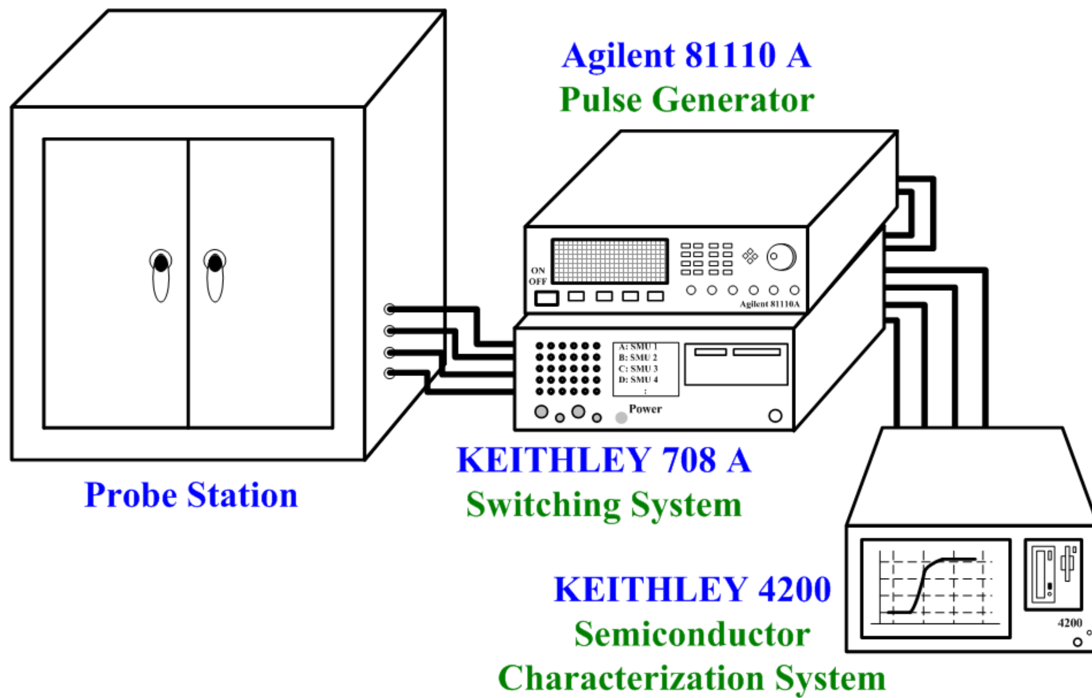


Fig. 2.3 The experimental setup of the I-V and threshold voltage characteristics measurement of the memory device.

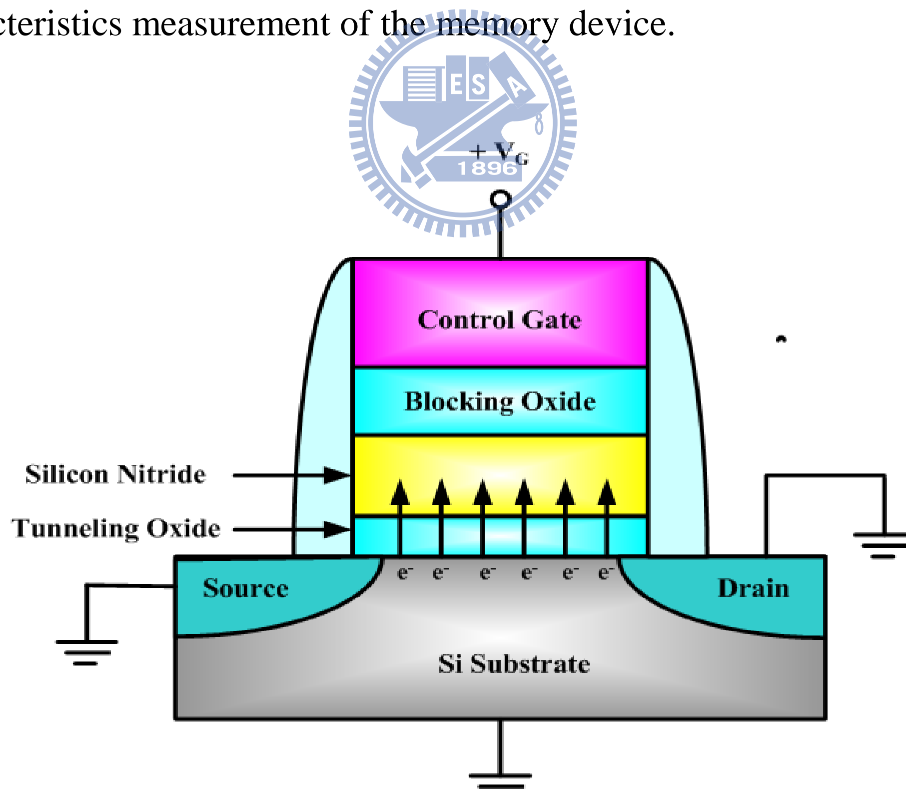


Fig. 2.4 The schematic mechanism of the FN tunneling for SONOS NVM devices programming.

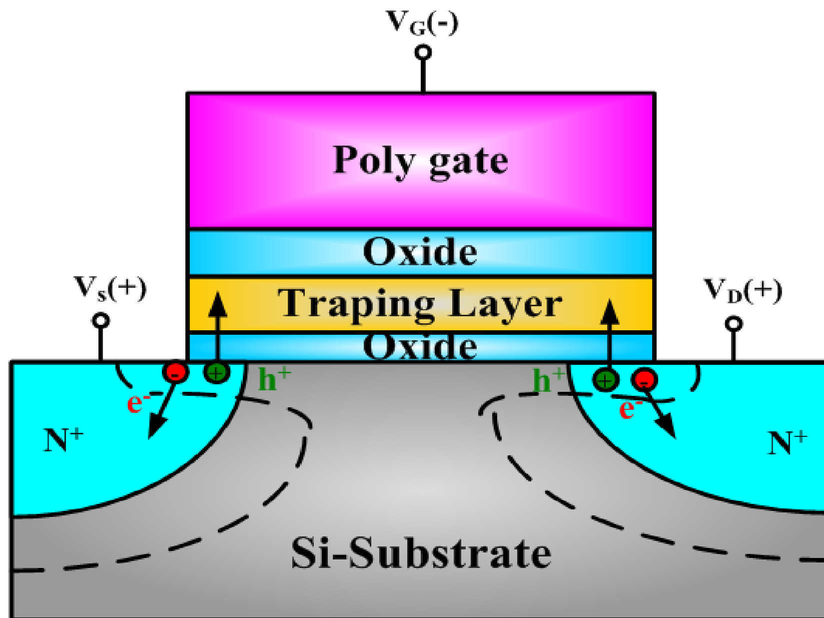


Fig. 2.5 The schematic mechanism of the substrate transient hot-hole (STHH) injection for SONOS NVM devices erasing.

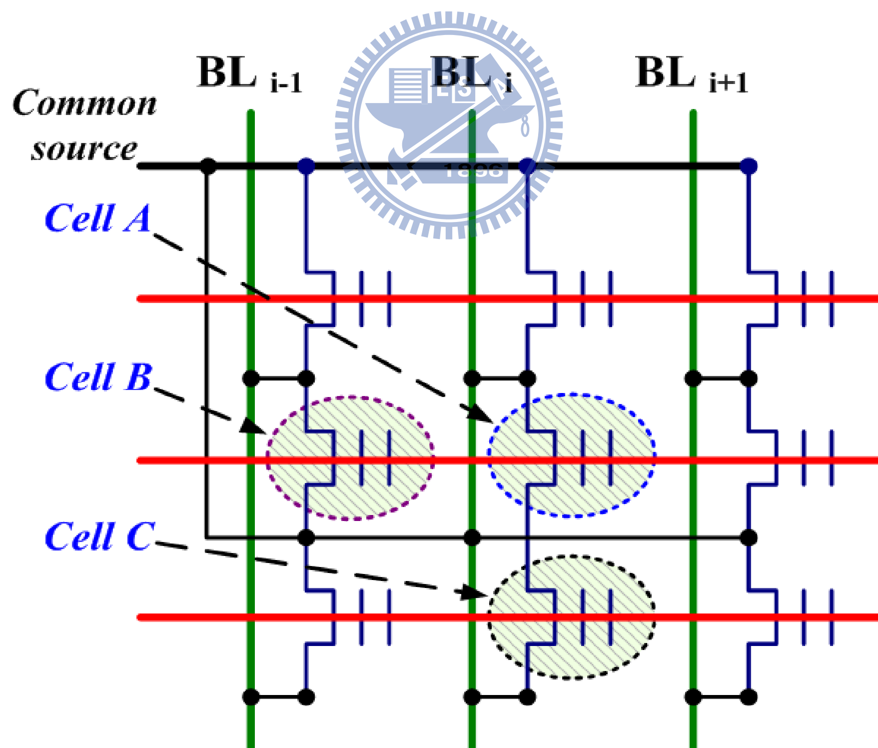


Fig. 2.6 The equivalent circuits schematic of the memory cell. During Cell A is programmed, the gate disturbance takes place in Cell B and the drain disturbance takes place in Cell C.

Chapter 3
Corner Effect of TFT-SONOS Memory Devices

3.1 Introduction

The most important demand of memory device is the performances of program/erase speed. We all hope the program/erase speed could as faster as possible. In addition, the cost per bit must be reduced in order for Flash technology to access the profitable market of mass storage for portable applications. The electric field enhancement is a good way to improve the program/erase speed and the efficiency was be proofed by many literatures [3-1][3-2]. In this chapter, we will introduce the experimental device of the Electric field enhancement memory cell with different corner number in NAND string. The program/erase speed and reliability issue would be discussed here. The programmed and erased of each sample were used Fowler-Nordheim (F-N) Injection and Substrate transient hot-hole (STHH) injection.

3.2 Results and Discussions

The structures of TFT-SONOS memory is as shown in Fig. 3.1 and Fig. 3.2. Fig. 31 is the TEM image of control sample and it could clearly show there are no adding corners at the channel width direction. As shown in Fig 3.2, channel film is look like "M" through the cross-section view of width direction. We called this structure is "M-shape" TFT-SONOS memory. And we also reinforce the topic of increasing number of corners, there were additive corners form undercut.

Fig 3.3 shows the program speed characteristics of the control sample and M-shape sample at Width/Length = 10um/ 10um, and the program voltages were at 35 V. The programming method is Fowler-Nordheim (FN) tunneling because the

voltage drop make the electric field of tunneling oxide is more than 6MV/cm. Using FN programming, a memory device without corners at the each side of channel shows a slow programming speed at a gate voltage (V_G) of 35 V comparable to the literatures [3-2][3-3]. On the other hand, M-shape sample (a memory device with corners) the programming V_{th} window of 7.06 V is obtained at V_G=35 V for 100-ms. Fig 3.4 shows the program speed characteristics of the control sample and M-shape sample at Width/Length = 5um/ 10um, and the program voltages were at 35 V. M-shape sample (a memory device with corners) the programming V_{th} window of 7.66 V is obtained at V_G=35 V for 100-ms. Fig 3.5 shows the program speed characteristics of the control sample and M-shape sample at Width/ Length = 2um/ 10um, and the program voltages were at 35 V. M-shape sample (a memory device with corners) the programming V_{th} window of 8.46 V is obtained at V_G=35 V for 100-ms. Fig 3.6 shows the program speed characteristics of the control sample and M-shape sample at Width/ Length = 5um/ 10um, and the program voltages were at 35 V. M-shape sample (a memory device with corners) the programming Vth window of 9.25 V is obtained at V_G=35 V for 100-ms.

From Fig 3.3 – 6, it is clearly shown that the programming speed is increased by local electric field enhancement. The electric field at corner region near the SiO2/poly-Si interface is much higher and the local enhancement of electric field can be achieved [3.4]. A higher electric field increases the likelihood of FN tunneling, allowing devices with corners to achieve a high program speed. Although the M-shape structures had locally field enhancement, it hadn't shown any double hump in Id-Vg characteristics as shown in Fig 3.11. It is because it had rounded corners. Rounded corner is not only reduced electric force lines crowding but also made induced free carriers more uniform [3.5].

Fig 3.7 shows the erase speed characteristics of the control sample and M-shape sample at Width/ Length = 10um/ 10um, and the erase voltages were at V_G= -7 V and V_S=V_D=18 V. The erasing method is substrate transient hot-hole (STHH) injection where a huge reverse bias is added to the PN junction to cause the PN junction in breakdown. An avalanche breakdown in PN junction caused a lot of electron-hole pairs, and only added a small VG of -7 V a large number of holes will be attracted then injected into nitride layer to erase electrons. On the other hand, M-shape sample (a memory device with corners) the erasing V_{th} window of 1.34 V is obtained at V_G= -7 V and V_S=V_D=18 V for 100-ms [3.6]. Fig 3.8 shows the program speed characteristics of the control sample and M-shape sample at Width/ Length = 5um/ 10um, and the program voltages were at V_G= -7 V and V_S=V_D=18 V. M-shape sample (a memory device with corners) the programming V_{th} window of 2.39 V is obtained at V_G= -7 V and V_S=V_D=18 V for 100-ms. Fig 3.9 shows the program speed characteristics of the control sample and M-shape sample at Width/ Length = 2um/ 10um, and the program voltages were at V_G= -7 V and V_S=V_D=18 V. M-shape sample (a memory device with corners) the programming V_{th} window of 3.3 V is obtained at at V_G= -7 V and V_S=V_D=18 V for 100-ms. Fig 3.10 shows the program speed characteristics of the control sample and M-shape sample at Width/Length = 1um/ 10um, and the program voltages were at V_G= -7 V and V_S=V_D=18 V. M-shape sample (a memory device with corners) the programming V_{th} window of 3.5 V is obtained at at V_G= -7 V and V_S=V_D=18 V for 100-ms.

From Fig 3.7 – 10, the programming efficiency is much higher than the erasing efficiency. This is because holes encounter a much higher barrier height (4.6eV) than electrons [3.6]. Although the erasing efficiency is not very well, as the width scaling

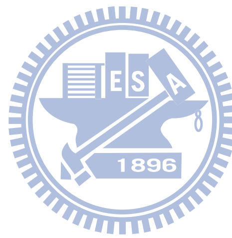
the erasing efficiency is improved.

From Fig 3.3 – 6 and Fig 3.7 – 10, we could find program window and erase window increase as channel width scaled down. There was an inverse proportion relationship between memory window and width as shown in Fig 3.12. As the channel width decreased, the V_{th} window of programming at a width of 1μm of M-shape TFT-SONOS increased by approximately 20% compared to the control sample. This kind of improvement also shows on erase window. In Fig 3.13, the V_{th} window of erasing at a width of 1μm of M-shape TFT-SONOS increased by approximately 57% compared to the control sample. Nevertheless, it still illustrates the retention performance of the M-shape TFT-SONOS memory at different temperatures. M-shape TFT-SONOS memory still has excellent reliability even at high-temperature of 100 ℃, resulting in a 5% data loss for 10^4-sec as shown in Fig 3.14. Results show that the addition of corners at each side of the channel in the width direction has no effect on data loss, even in short-width devices. Fig 3.15 shows the temperature activation energy (Ea) for the projection of retention lifetime. The data retention of the M-shape TFT-SONOS memory is well above ten years at 73 ℃, with an Ea of 1.604 eV [3.7].

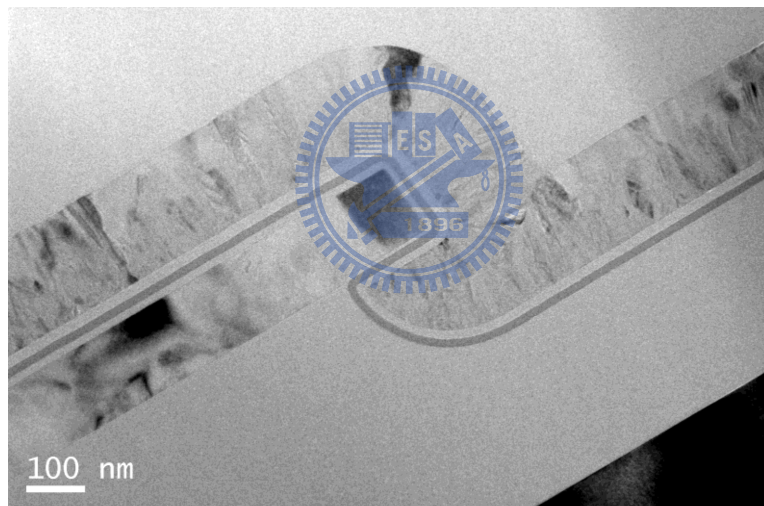
3.3 Summary

This study demonstrates structure-shape TFT-SONOS memory with sharp corners. This M-shape TFT-SONOS memory design improves the program/erase speed and program/erase window in contrast to the control sample. The enhanced electrical field in the corner regions generates a higher program current under FN programming. However, this corner effect does not decrease retention at room temperature. M-shape TFT-SONOS memory still has remarkable retention at different widths and high

temperature baking. The proposed M-shape TFT-SONOS memory significantly improves the memory window and achieves excellent retention. Thus, the proposed M-shape TFT-SONOS memory seems promising for future SOP designs.



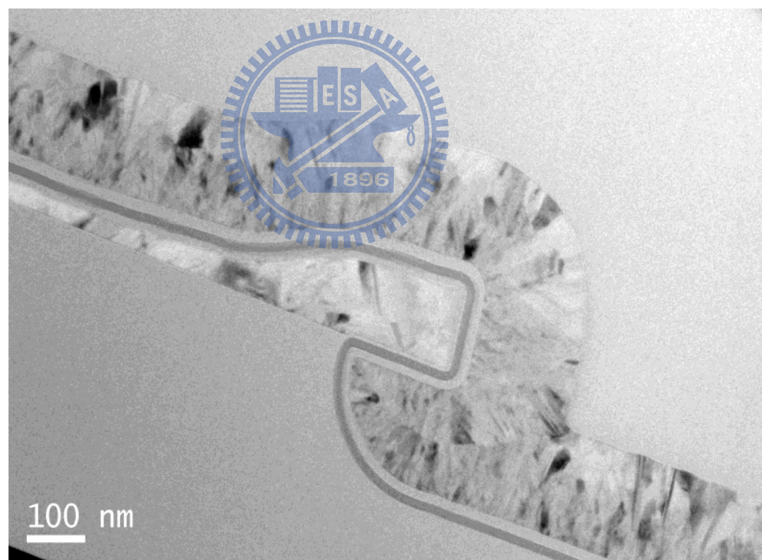
(a)



(b)

Fig. 3.1(a) The TEM images of control samples through width direction. There are no addition corners on each side of channel width direction (b) It is the enlarge drawing of corner.

(a)



(b)

Fig. 3.2(a) The TEM images of M-shape samples through width direction. There are addition corners on each side of channel width direction (b) It is the enlarge drawing of corner.

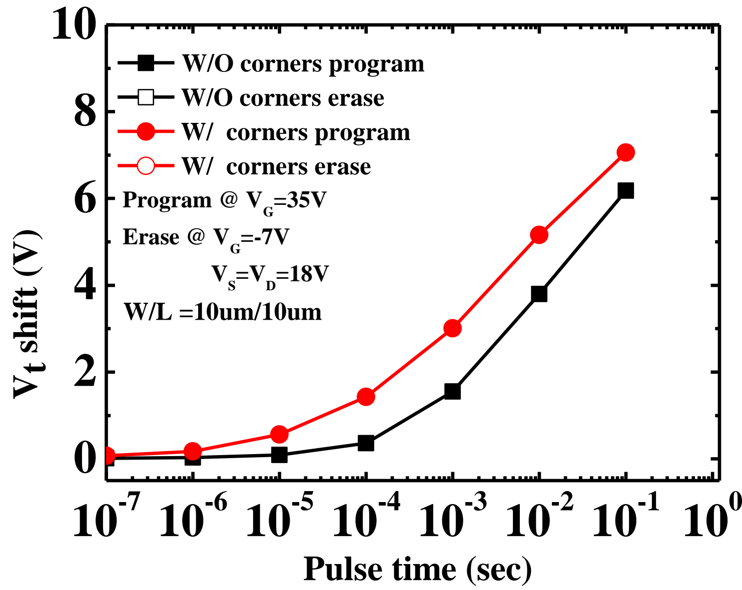


Fig 3.3 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=10μm.

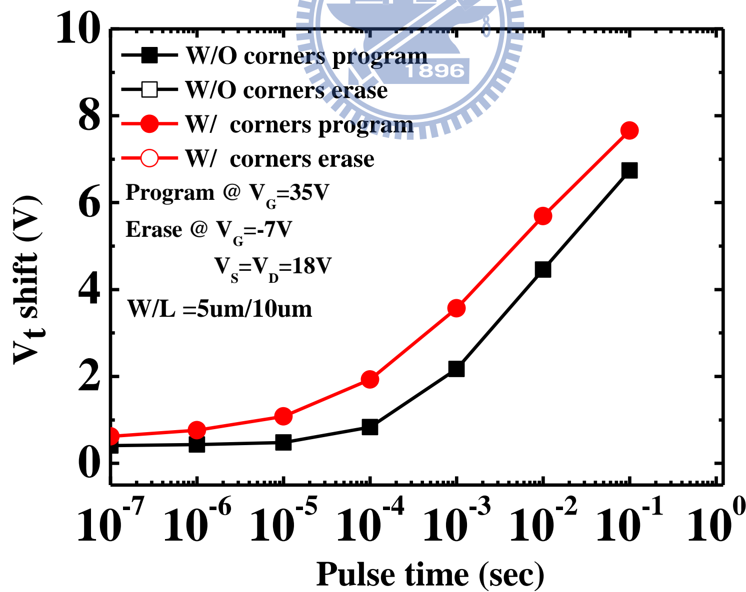


Fig 3.4 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=5μm.

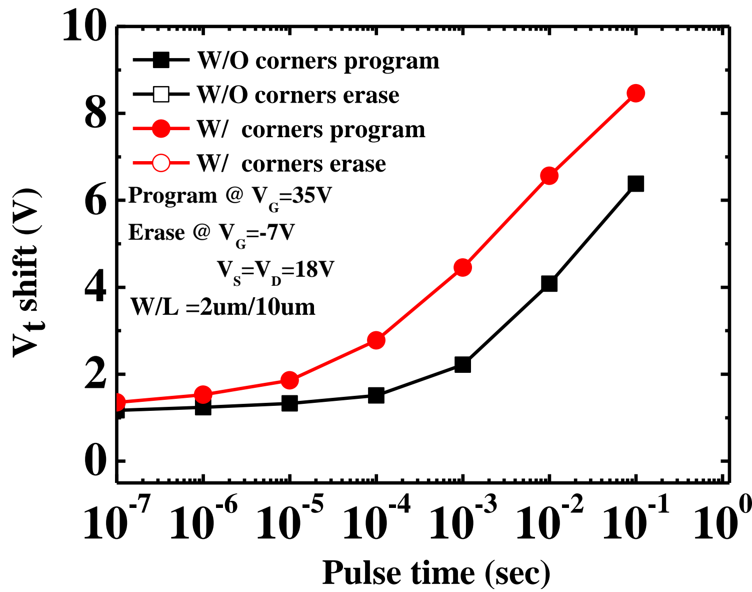


Fig 3.5 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=2μm.

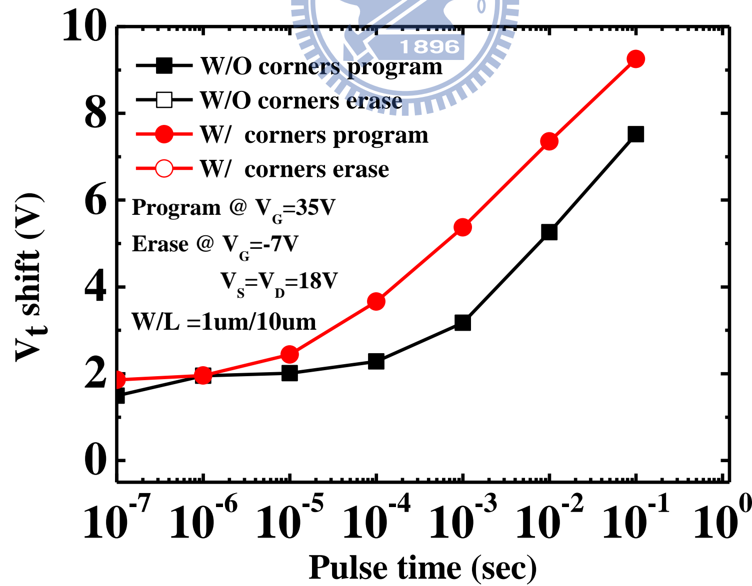


Fig 3.6 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=1μm.

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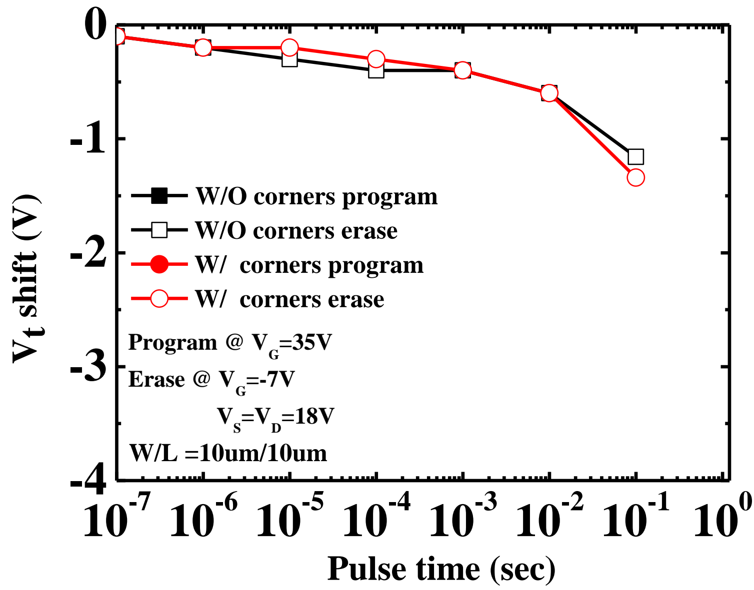


Fig 3.7 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=1μm

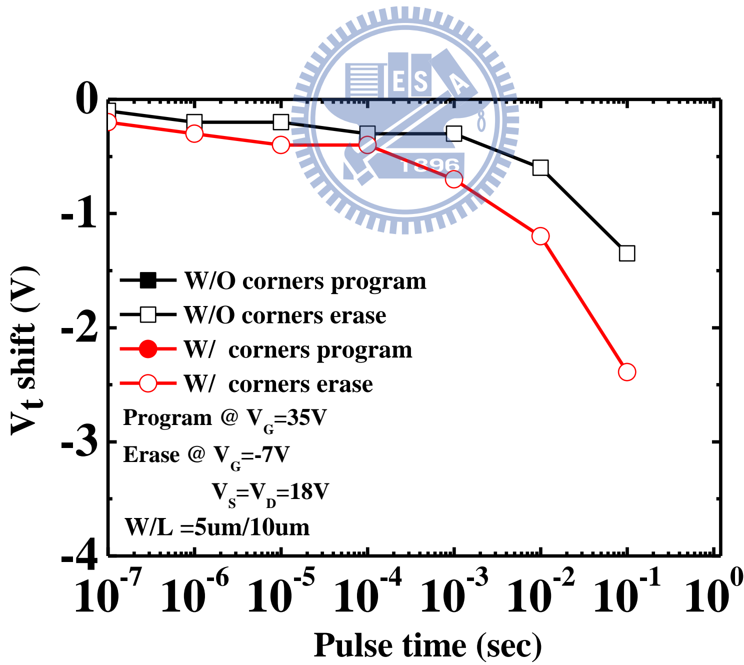


Fig 3.8 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width= 5μm

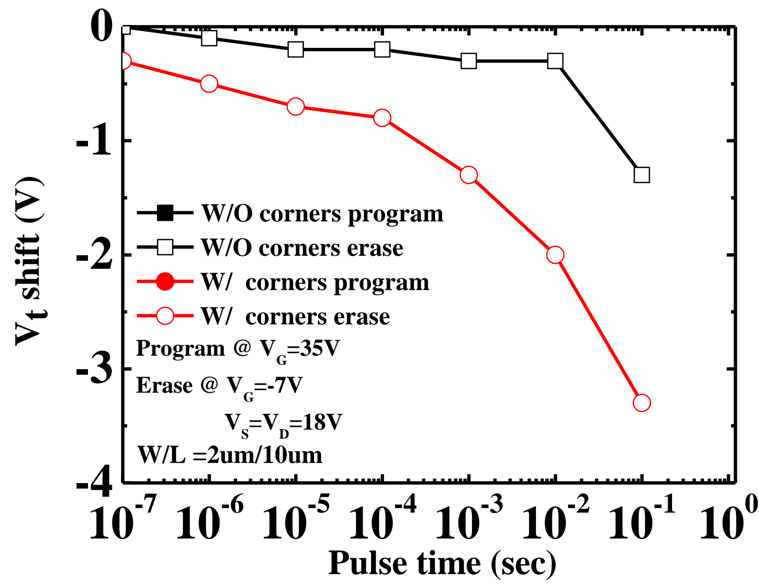


Fig 3.9 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=2μm.

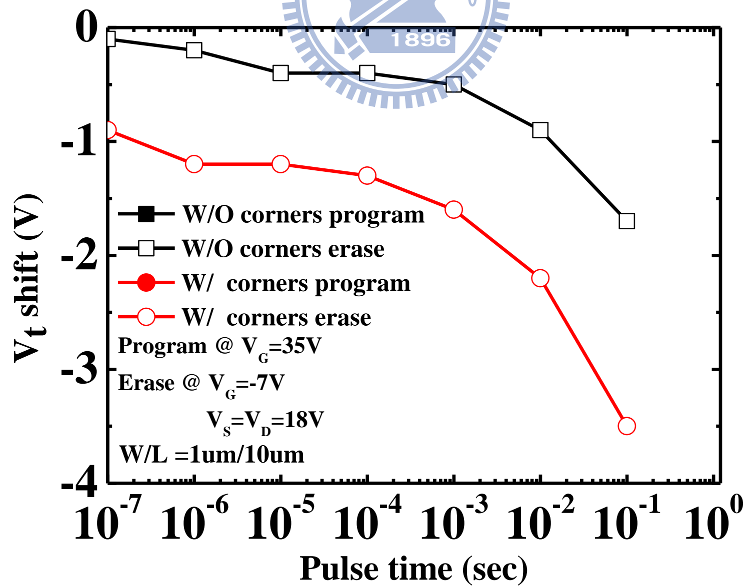


Fig 3.10 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=1μm.

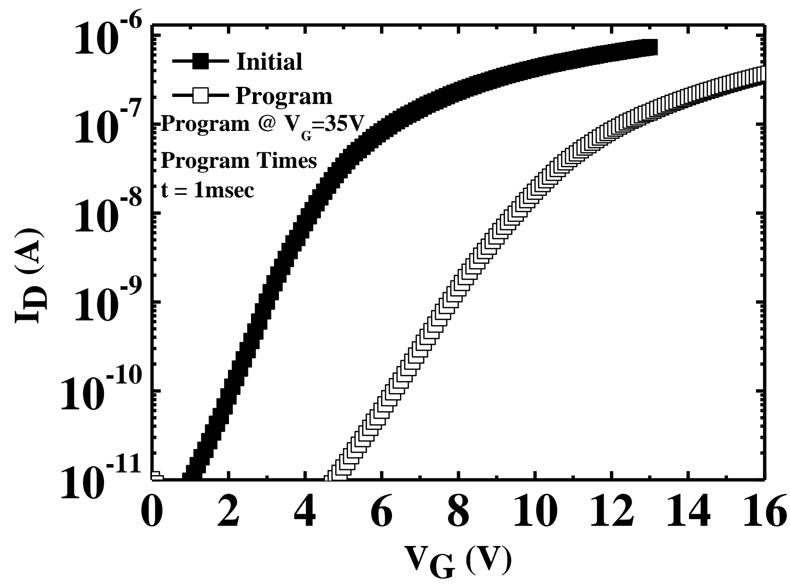


Fig. 3.11 The " double hump" was not shown here for ID-VG curves. The rounding corners help us solve the problem of hump.

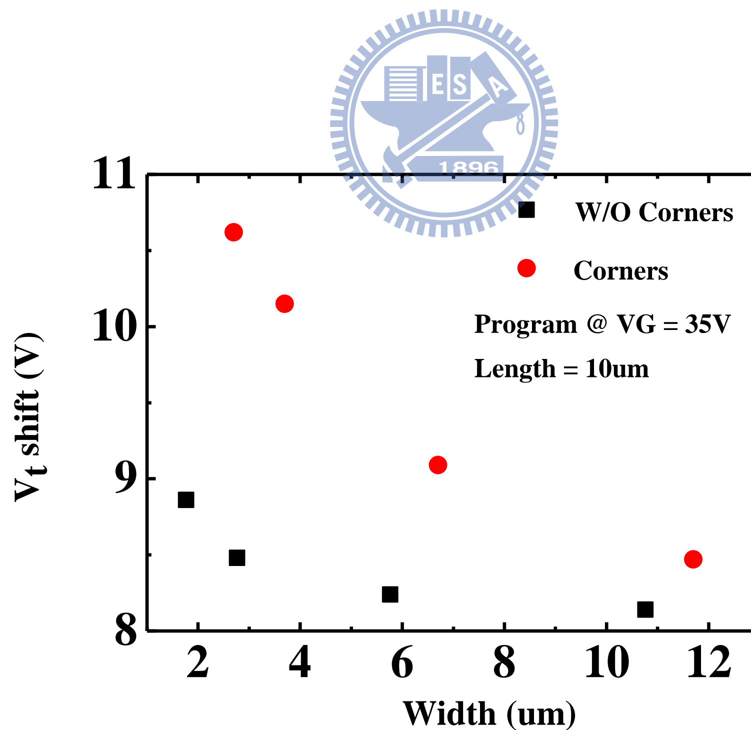


Fig. 3.12 M-shape TFT-SONOS memory has width dependence. Program windows increased significantly as the width decreased.

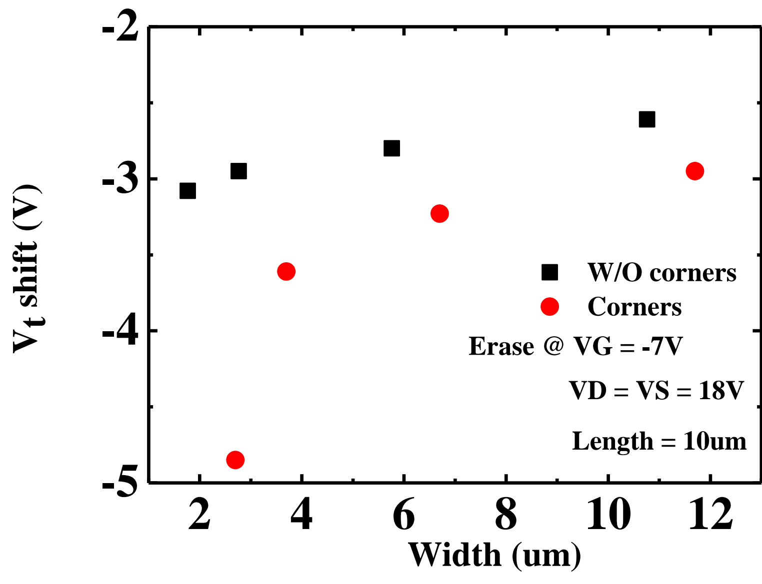


Fig. 3.13 M-shape TFT-SONOS memory has width dependence. Erase windows increased significantly as the width decreased.

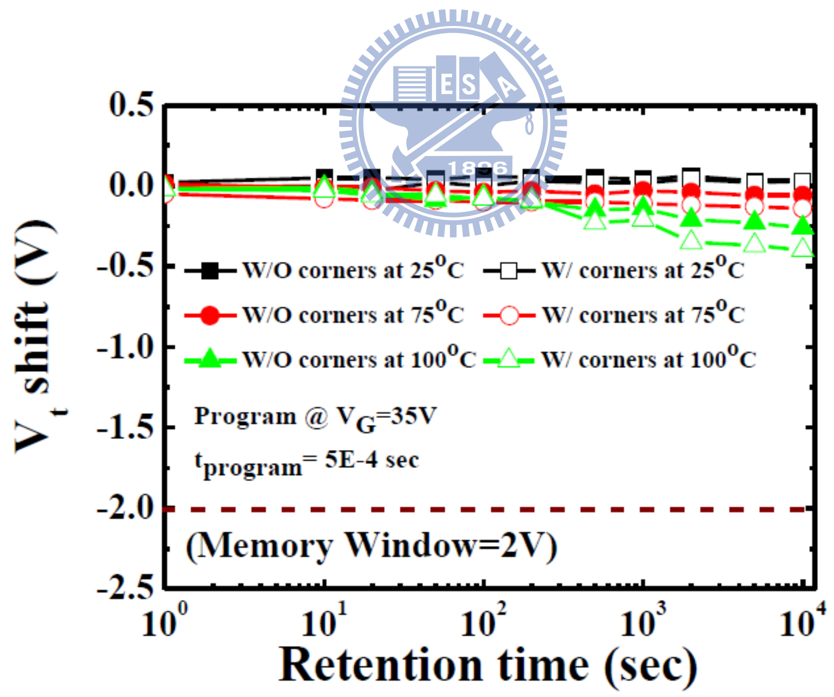


Fig. 3.14 Retention characteristics of M-shape TFT-SONOS memory window at different temperature 25℃, 75℃, and 100℃.

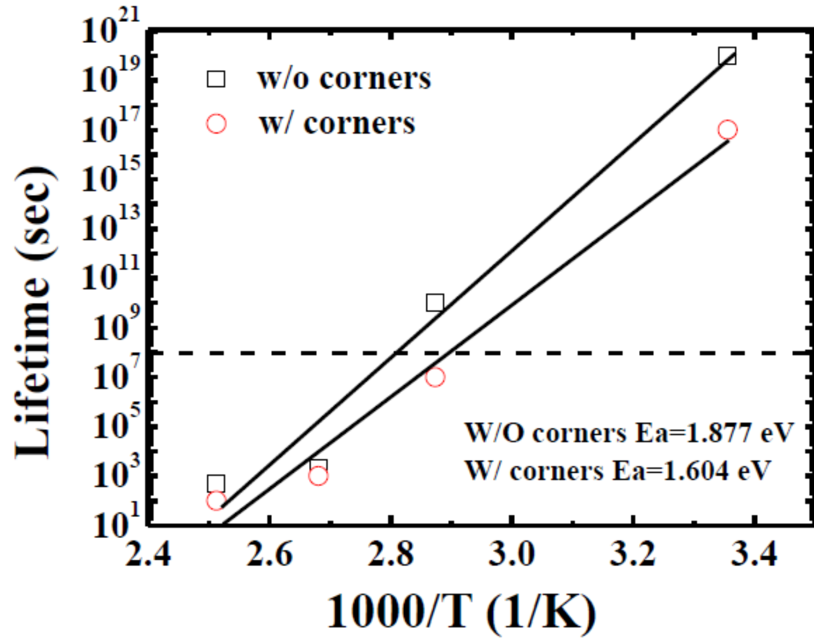
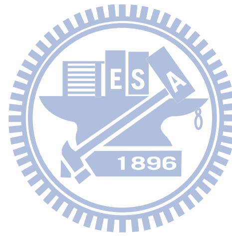


Fig. 3.15 Projection lifetime of data retention with an Ea of 1.604 eV.



Chapter 4

Corner Effect of TFT-SONOS Memory Devices Following EOT Scaled Down

4.1 Introduction

In 2007, the main flash memory market combined NOR and NAND array have reached above $22 billion US dollars, economic forecast of the Non-Volatile Memory (NVM) market almost occupy above 45 percent of memory market in 2010, nearly 22 percent of the total semiconductor market. According to the Moor's Law, the non-volatile memory has been leading the way from 16 Mb and 0.35 μm of technology node in 1994 to 32 Gb and 40 nm of technology node today [4.1]. Therefore, the density of Flash memory devices could be raised by scaling the design rule. As scaling the Flash memory device also to face the challenges for circuit design and reliability issues. First, in order to decrease the power consumption, the power supply voltage must be decreased. Second, the thickness of tunneling oxide in the flash memory device would be thinner than 3~4 nm as accompanies channel length scale-down [4.2]. Then, electrons would be easier to tunnel through the tunneling oxide defects into the silicon substrate. Equivalent oxide thickness (EOT) scaled down is easier than channel length scaled down. Because the channel length scaled down would suffer serious short channel effect. Hence, in this chapter, we will scale the oxide – nitride – oxide thickness and introduce different structure off-set. Following EOT scaling down issue, there is another problem of oxide – nitride – oxide thickness. According to references, the tunneling oxide thickness should be thick enough to prevent from a single point defect in the tunneling oxide induce Frenkel-Poole tunneling [4.3]. There is also a restriction of trapping layer. The thickness of nitride layer should be ≧ 7nm to ensure the charge capture rate [4.4].

The program/erase speed and reliability issue would also be discussed here. The programmed and erased each samples were used by Fowler-Nordheim (F-N) Injection and Substrate transient hot-hole (STHH) injection.

4.2 Result and Discussions

The structures of TFT-SONOS memory is as shown in Fig. 4.1, Fig. 4.2 and Fig. 4.2. Fig. 4.1 is the TEM image of control sample and it could clearly show there are no adding corners at the channel width direction. In Fig. 4.2 and Fig. 4.3, the difference between these is the oxidation thickness. By the different oxidation time and oxidation thickness, the poly-Si channel consumption was not alike. Due to this reason, we want to clarify the different oxidation time to bring about the structure off-set issue and it has any impact on TFT-SONOS memory performance.

Fig. 4.4 shows the program speed characteristics of the control sample and M-shape samples with different oxidation thickness at Width/ Length =10um/ 10um, and the program voltages were at 30 V. The programming method is Fowler-Nordheim (FN) tunneling because the voltage drop make the electric field of tunneling oxide is more than 6MV/cm. Using FN programming, a memory device without corners at the each side of channel shows a slow programming speed at a gate voltage (V_G) of 30 V comparable to the literatures [4-5][4-6]. In the meanwhile, we could fine M-shape samples (a memory device with corners) with different oxidation thickness they clearly show faster program speed compared with control sample. M-shape sample (a memory device with corners) the programming V_{th} window of 6.36 V is obtained at V_G=30 V for 1s for 100 nm oxidation, and the programming Vth window of 5.99 V is obtained at V_G=30 V for 1-s for 150 nm oxidation. As shown in

Fig. 4.5, M-shape samples also have better programming speed in contrast to the control sample. M-shape sample (a memory device with corners) the programming V_{th} window of 6.91 V is obtained at V_G=30 V for 1-s for 100 nm oxidation, and the programming Vth window of 6.26 V is obtained at V_G=30 V for 1-s for 150 nm oxidation. From Fig. 4.6, M-shape samples still have superior programming speed in contrast to the control sample. M-shape sample (a memory device with corners) the programming V_{th} window of 7.14 V is obtained at V_G=30 V for 1s for 100 nm oxidation, and the programming Vth window of 6.34 V is obtained at V_G=30 V for 1-s for 150 nm oxidation.

From Fig. 4.4 – 6, it is clearly shown that the programming speed is increased by local electric field enhancement. The electric field at corner region near the SiO_2/ Poly-Si interface is much higher and the local enhancement of electric field can be achieved [4.5]. A higher electric field increases the likelihood of FN tunneling, allowing devices with corners to achieve a high program speed.

Fig. 4.8 shows the erase speed characteristics of the control sample and M-shape sample at Width/ Length = 10um/ 10um, and the erase voltages were at V_G= -7 V and V_S=V_D=15 V. The erasing method is substrate transient hot-hole (STHH) injection where a huge reverse bias is added to the PN junction to cause the PN junction in breakdown [4.6]. An avalanche breakdown in PN junction caused a lot of electron-hole pairs, and only added a small VG of -7 V a large number of holes will be attracted then injected into nitride layer to erase electrons. In the meanwhile, we could fine M-shape samples (a memory device with corners) with different oxidation thickness they clearly show faster program speed compared with control sample. M-shape sample (a memory device with corners) the erasing V_{th} window of 1.61 V is

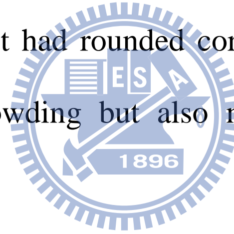
obtained at V_G= -7 V and V_S=V_D=15 V for 1s for 100 nm oxidation, and the erasing V_{th} window of 1.18 V is obtained at V_G= -7 V and V_S=V_D=15 V for 1-s for 150 nm oxidation. In Fig. 4.9, M-shape samples also have better erasing speed in contrast to the control sample. M-shape sample (a memory device with corners) the erasing V_{th} window of 2.49 V is obtained at V_G=30 V for 1-s for 100 nm oxidation, and the erasing Vth window of 1.33 V is obtained at V_G=30 V for 1-s for 150 nm oxidation. From Fig. 4.10, M-shape samples still have superior erasing speed in contrast to the control sample. M-shape sample (a memory device with corners) the erasing V_{th} window of 3.41 V is obtained at V_G=30 V for 1s for 100 nm oxidation, and the erasing V_{th} window of 1.65 V is obtained at V_G=30 V for 1s for 150 nm oxidation.

From Fig. 4.8 – 10, it is clearly shown that the erasing speed is increased by local electric field enhancement. The electric field at corner region near the SiO_2/ poly-Si interface is much higher and the local enhancement of electric field can be achieved [4.7]. The programming efficiency is much higher than the erasing efficiency. This is because holes encounter a much higher barrier height (4.6 eV) than electrons [4.8]. Although the erasing efficiency is not very well, as the width scaling the erasing efficiency is improved.

On the other hand, we find the programming speed is not direct proportion to the oxidation thickness. The sample with oxidation thickness 100nm has the optimum programming/ erasing speed and this is contrary to what we suppose initially. Due to we consider the higher oxidation thickness is, the higher structure off-set has. It would help the electric field enhance. As shown in Fig. 4.2, the corners of 100nm oxidation which have a platform and a slightly sharp curve. From Fig. 4.3, the corners of 150nm oxidation clearly showed which extremely round sliders are, and the center of channel

is much thinner than 100nm. From 100nm and 150nm oxidation samples, we obtained a conclusion that the programming/ erasing speed is both enhanced by this structure and the only one difference is the corner of platform. As we mention, the improvement is increasing as effective scaling down. The 150nm oxidation sample has much longer oxidation time, so it is possible the oxygen would be drill into poly – Si deeper. Due to this reason, the angles of platform corners are different. The more oxidation is, the more round corner is. Due to this reason, the 100nm oxidation sample is not only helps us improve the program/ erase speed but also help us prevent from double hump situation.

Although the M-shape structures had locally field enhancement, it hadn't shown any double hump in Id-Vg characteristics as shown in Fig 4.11(a)(b) for 100nm/ 150nm oxidation. It is because it had rounded corners. Rounded corner is not only reduced electric force lines crowding but also made induced free carriers more uniform.



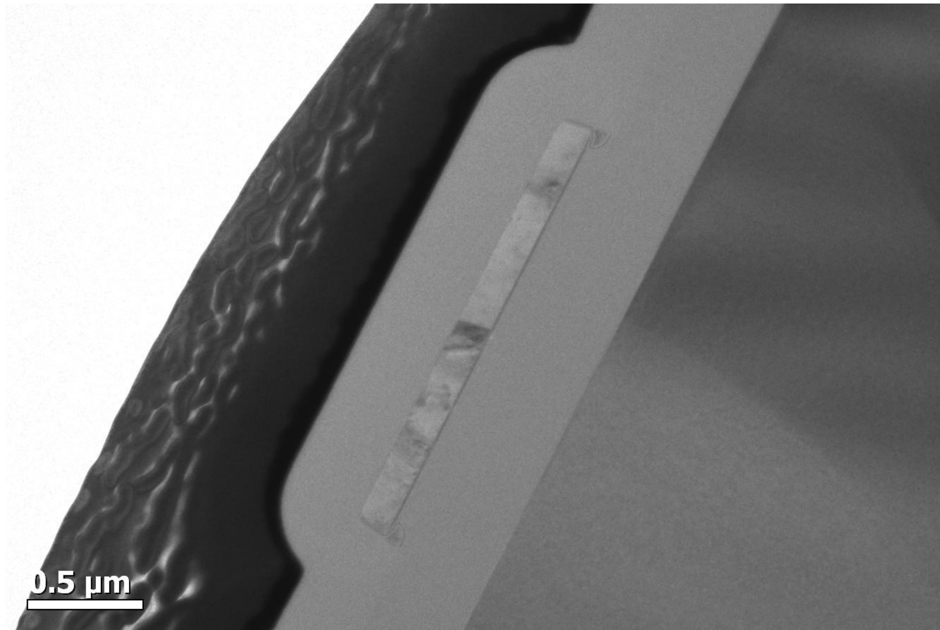
From Fig. 4.4 – 6 and Fig. 4.8 – 10, we could find program window and erase window increase as channel width scaled down. There was an inverse proportion relationship between memory window and width as shown in Fig. 4.12 (a)(b). As the channel width decreased, the V_{th} window of programming at a width of 2μm of M-shape TFT-SONOS increased by approximately 23.7% compared to the control sample of 100nm oxidation thickness. The V_{th} window of programming at a width of 2μm of M-shape TFT-SONOS increased by approximately 10% compared to the control sample of 150nm oxidation thickness. The program improvement is much less compared to the 100nm oxidation thickness. This kind of improvement also shows on erase window. In Fig. 4.13 (a)(b), the V_{th} window of erasing at a width of 2μm of

M-shape TFT-SONOS increased by approximately 120% compared to the control sample of 100nm oxidation thickness. The V_{th} window of erasing at a width of 2μm of M-shape TFT-SONOS increased by approximately 6.9% compared to the control sample of 150nm oxidation thickness. There is an obviously improvement of erasing window for 100nm oxidation thickness.

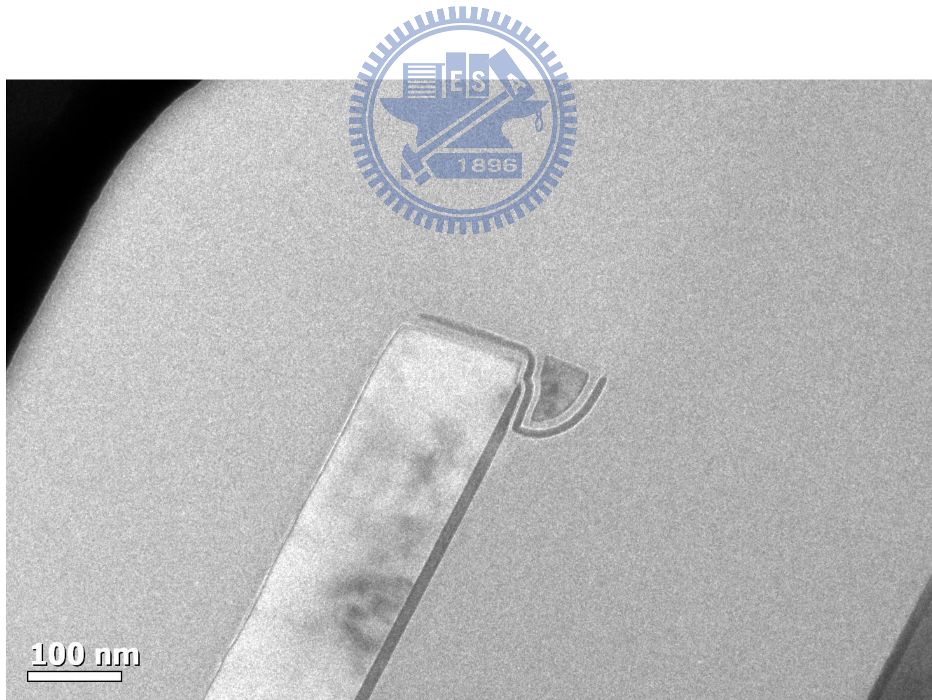
Even though the local field enhancement, it still illustrates the retention performance of the M-shape TFT-SONOS memory with different oxidation thickness at different temperatures. M-shape TFT-SONOS memory still has excellent reliability even at high - temperature of 125℃, resulting in a 6 % data loss for 104-sec with the 100nm/ 150nm oxidation thickness at width 10μ m as shown in Fig. 4.14-15. Results show that the addition of corners at each side of the channel in the width direction has no effect on data loss, even in short-width devices. Fig. 4.16 (a) shows the temperature activation energy (Ea) for the projection of retention lifetime. The data retention of the M-shape TFT-SONOS memory of 100nm oxidation is well above ten years at 102 ℃, with an Ea of 1.447 eV. And it also shown in Fig. 4.16 (b), the data retention of the M-shape TFT-SONOS memory of 150nm oxidation is well above ten years at 103 ℃, with an Ea of 1.387 eV [4.9]. Fig. 4.17 shows the gate disturb characteristic of TFT-SONOS memory devices for control sample, oxidation thickness 100nm and oxidation thickness 150nm. As the figure, we could see there are almost no threshold voltage shifts at different VG stress conditions (VG=15/ 17 /19 V).

4.3 Summary

In this chapter, we followed the issue of Equality oxide thickness (EOT) scaled down. This M-shape TFT-SONOS memory design improves the program/erase speed and program/erase window in contrast to the control sample. The enhanced electrical field in the corner regions generates a higher program current under FN programming. We obtained a relationship between program/ erase speed and different oxidation thickness. The oxidation thickness is not direct proportion to the TFT-SONOS memory performance, because the key point is the platform and the slightly sharp curve of corners. The more oxidation makes the corners are very round sliders, and it would lead the locally field enhance degrade. This structure has strong width among dependence and program/ erases speed. However, this corner effect does not decrease retention at room temperature. M-shape TFT-SONOS memory still has remarkable retention at different widths and high temperature baking. The proposed M-shape TFT-SONOS memory significantly improves the memory window and achieves excellent retention. On the other hand, gate disturbance characteristics also showed the reliability of M-shape TFT-SONOS memory is outstanding. Thus, the proposed M-shape TFT-SONOS memory seems promising for future SOP designs.

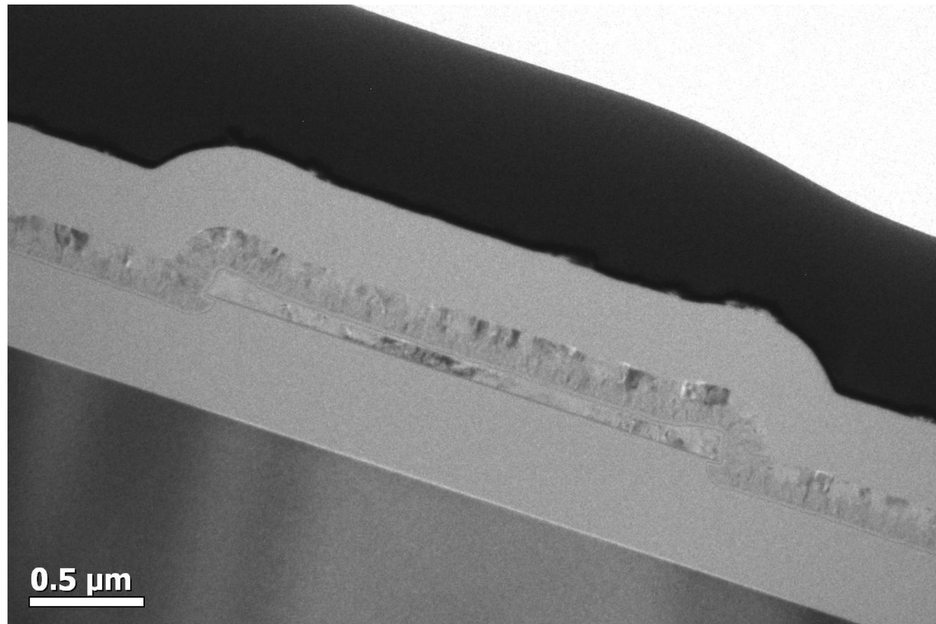


(a)

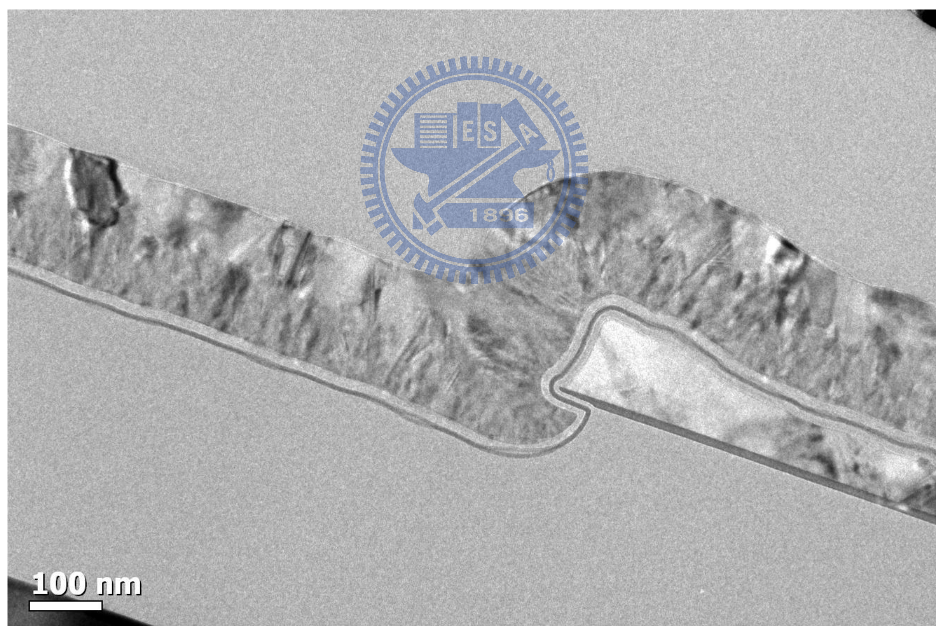


(b)

Fig. 4.1 (a) The TEM images of control samples through width direction. There are no addition corners on each side of channel width direction (b) It is the enlarge drawing of corner.

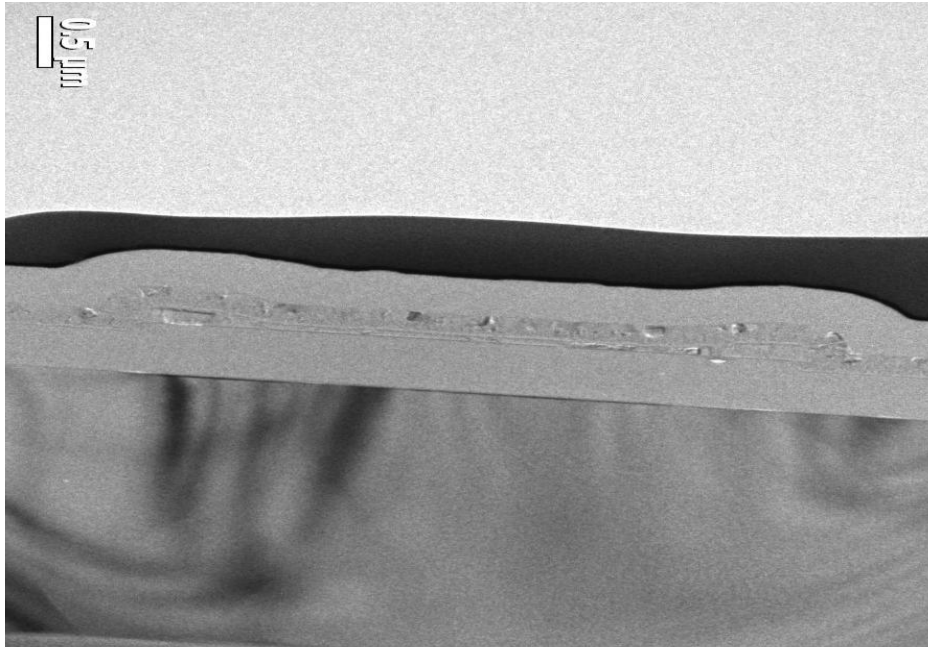


(a)

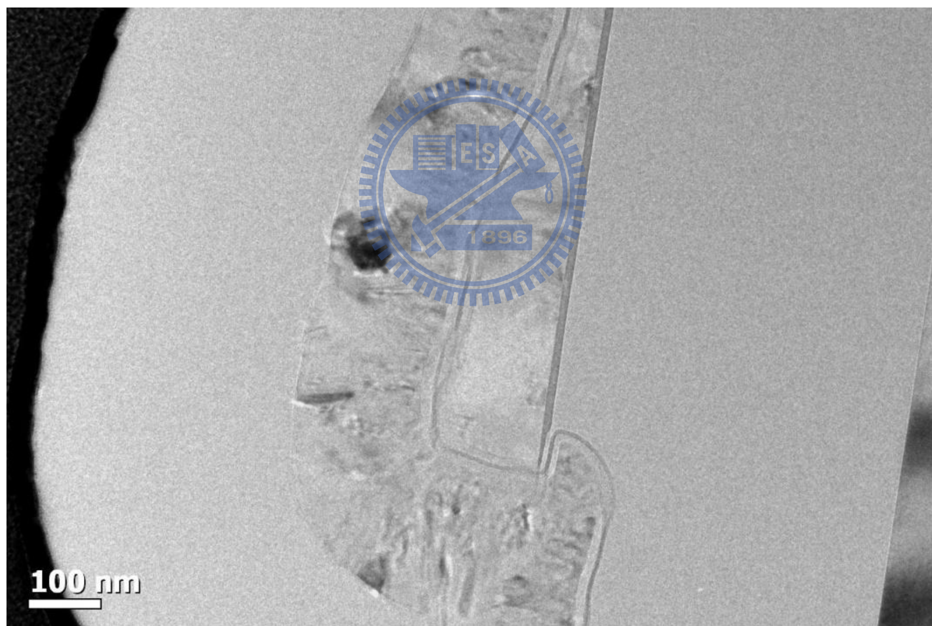


(b)

Fig. 4.2 (a) The TEM images of oxidation 100nm samples through width direction. There are addition corners on each side of channel width direction (b) It is the enlarge drawing of corner.



(a)



(b)

Fig. 4.3 (a) The TEM images of oxidation 150nm samples through width direction. There are addition corners on each side of channel width direction (b) It is the enlarge drawing of corner.

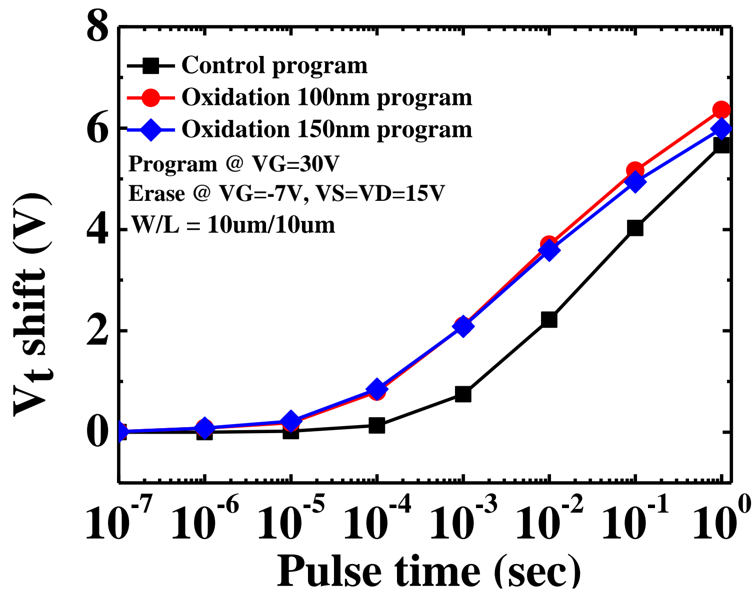


Fig. 4.4 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=10μm for both samples.

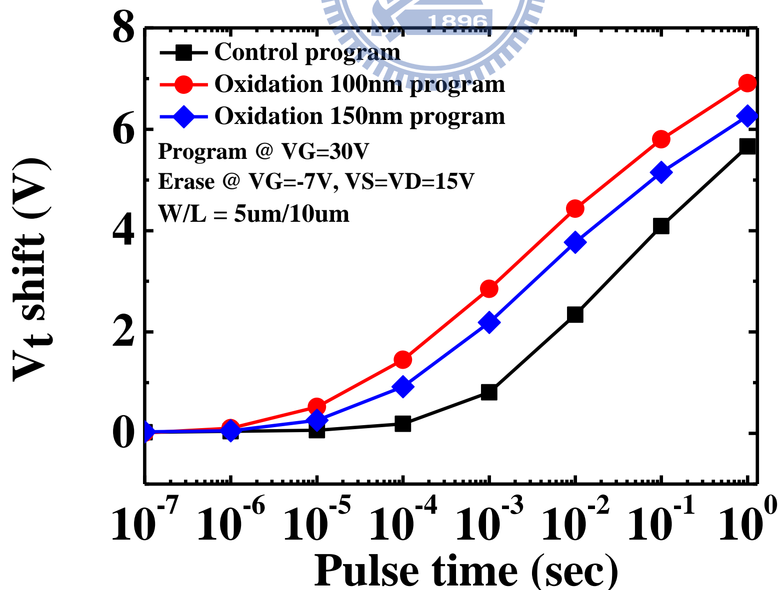


Fig. 4.5 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=5μm for both samples.

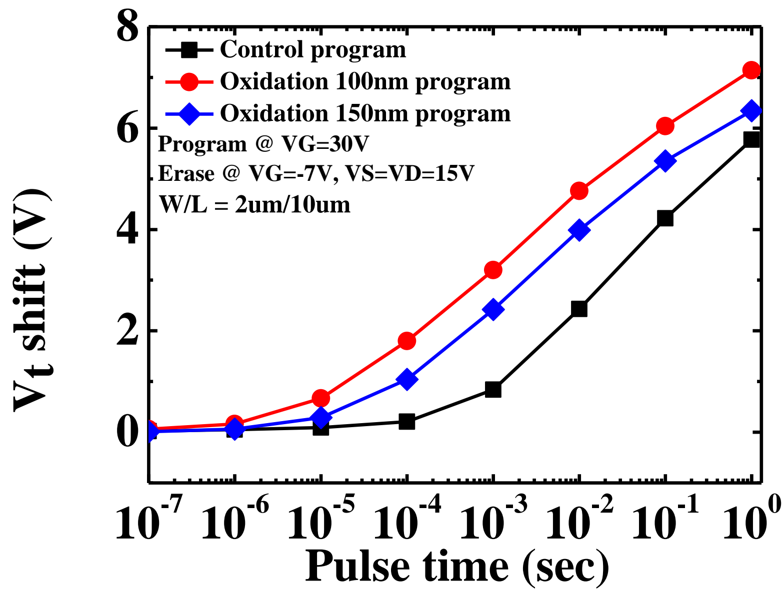
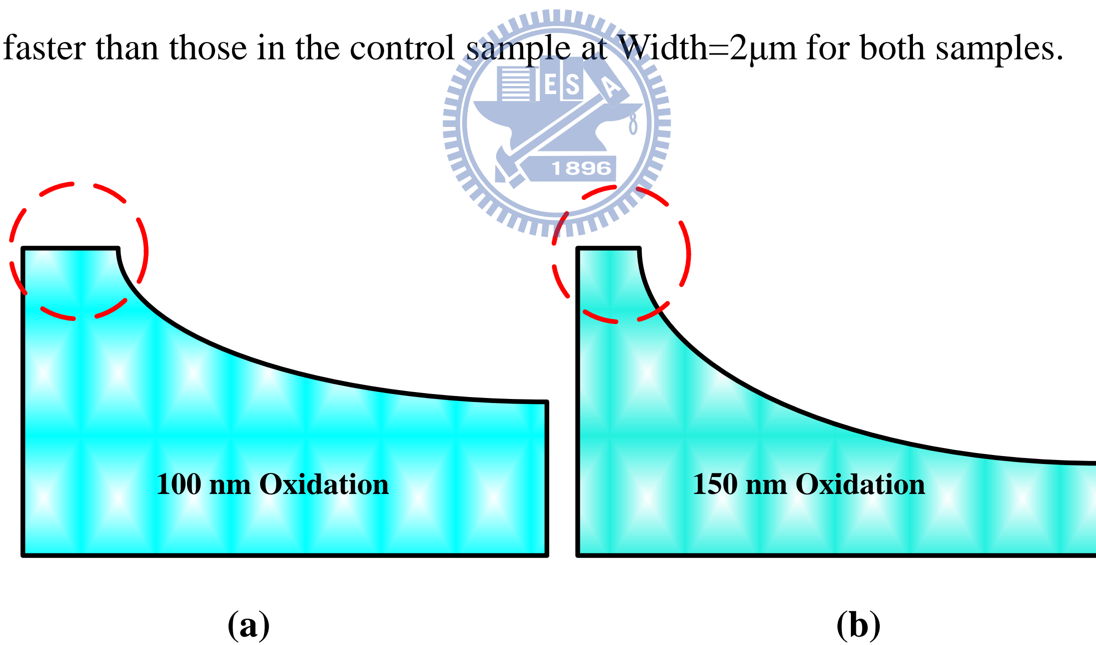


Fig. 4.6 Program characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=2μm for both samples.



(a) (b)

Fig. 4.7 (a) Schematic of 100nm oxidation thickness (b) Schematic of 150nm oxidation thickness. The angle of corner and the width of platform are different, and would be depress the improvement of program/ erase speed.

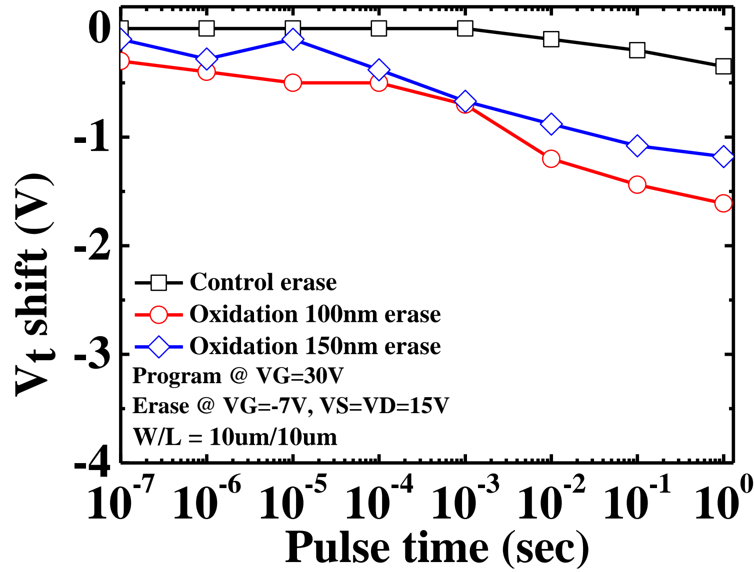


Fig. 4.8 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=10μm for both samples.

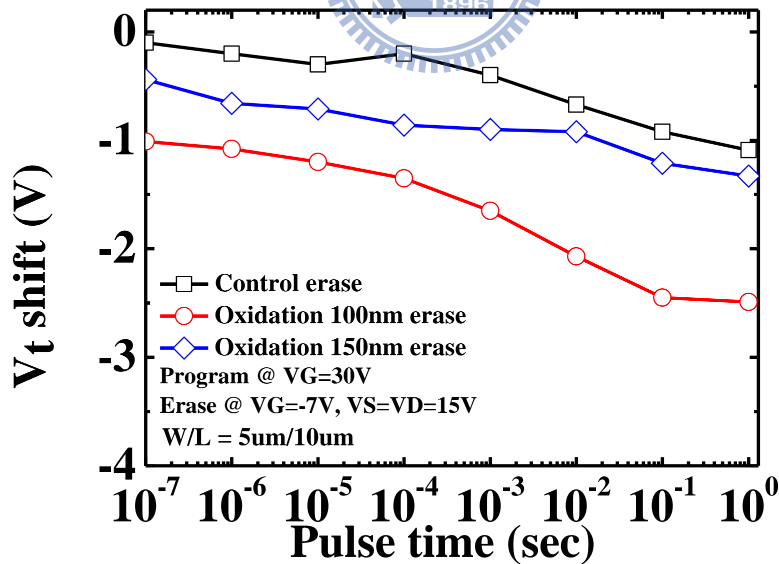


Fig. 4.9 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=5μm for both samples.

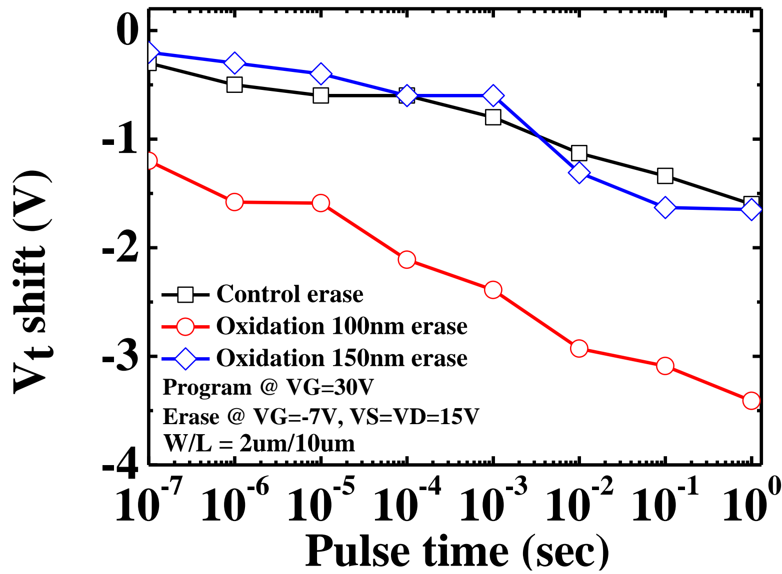
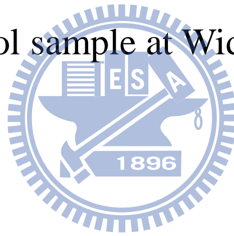


Fig. 4.10 Erase characteristic of M-shape TFT-SONOS memory. The program speed and memory window in TFT-SONOS memory increased faster than those in the control sample at Width=2μm for both samples.



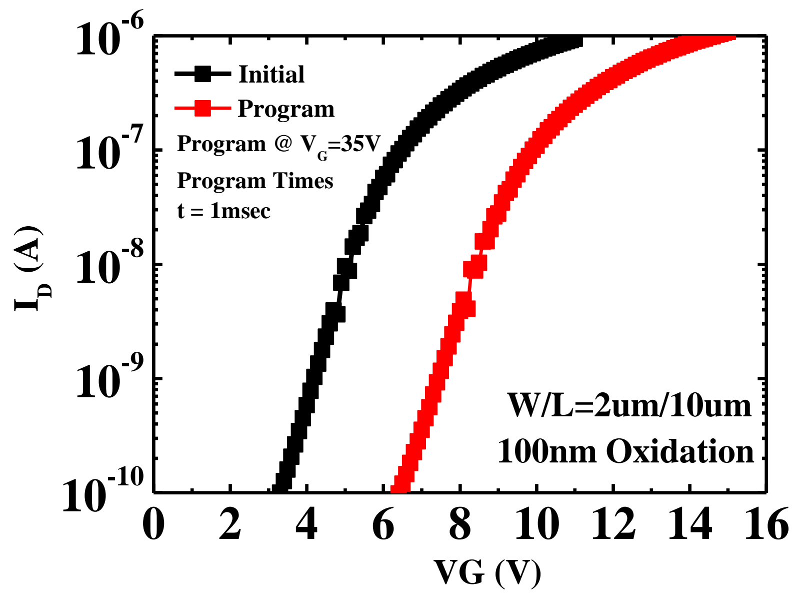


Fig. 4.11(a) The “ double hump” was not shown here for ID-VG curves of 100nm oxidation. The rounding corners help us solve the problem of hump.

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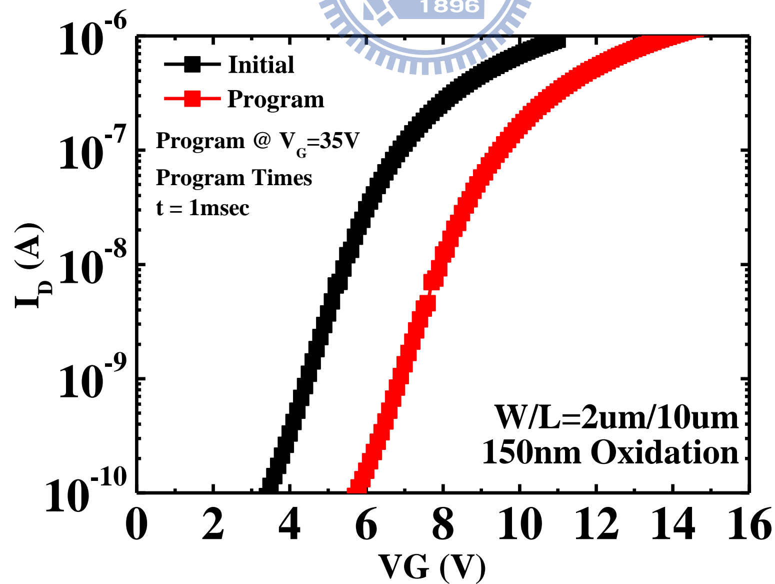
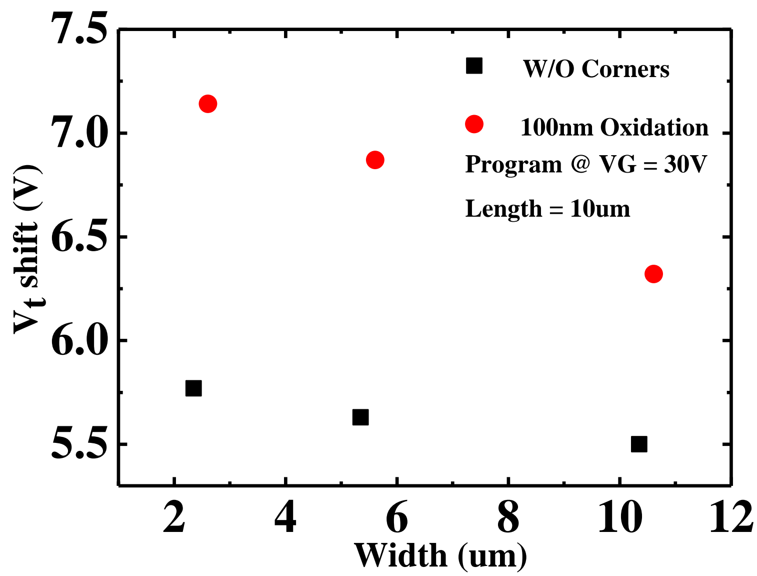
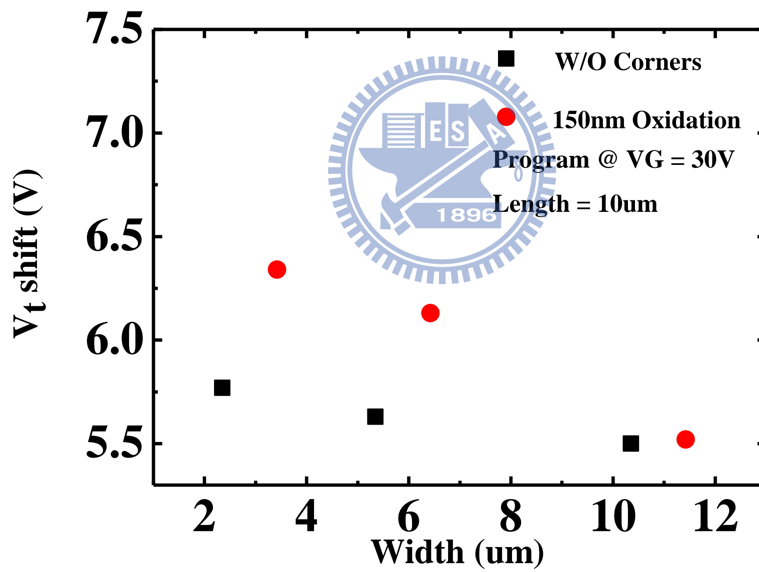


Fig. 4.11(b) The “ double hump” was not shown here for ID-VG curves of 150nm oxidation. The rounding corners help us solve the problem of hump.

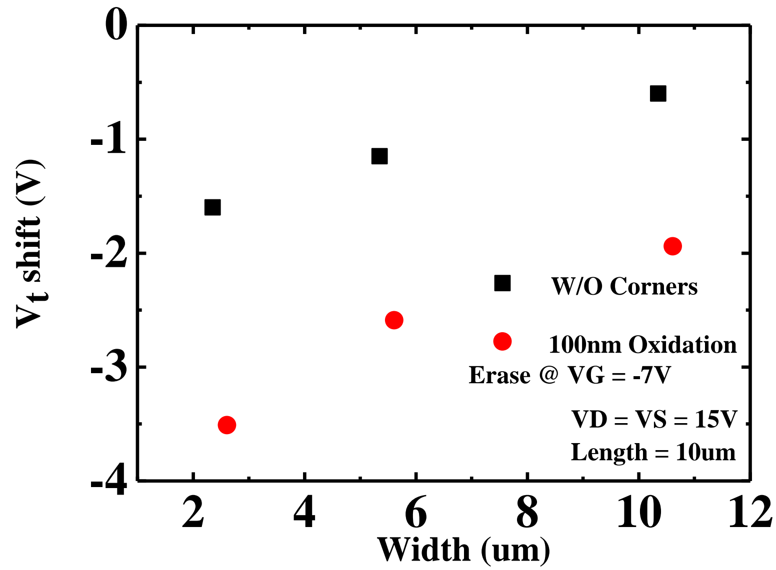


(a)

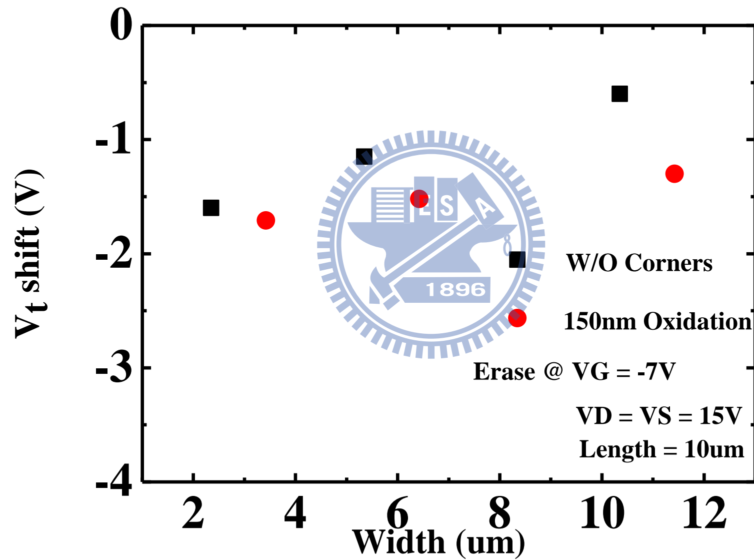


(b)

Fig. 4.12 (a)(b) TFT-SONOS memory has width dependence for both 100nm/150nm oxidation thickness. Program windows increased significantly as the width decreased, and 100nm oxidation thickness has much more improvement.



(a)



(b)

Fig. 4.13 (a)(b) TFT-SONOS memory has width dependence for both 100nm/150nm oxidation thickness. Erase windows increased significantly as the width decreased, and 100nm oxidation thickness has much more improvement.

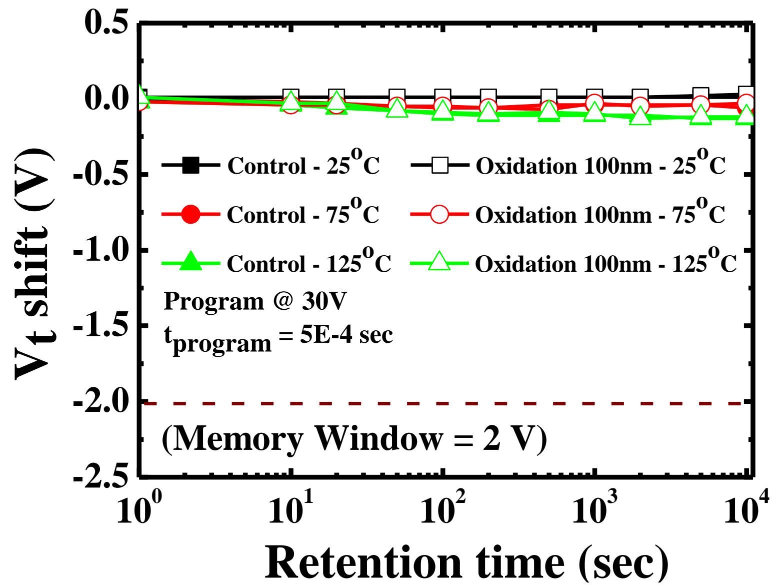


Fig. 4.14 Retention characteristics of M-shape TFT-SONOS memory window at different temperature 25℃, 75℃, and 125℃ for fresh devices with 100nm oxidation.

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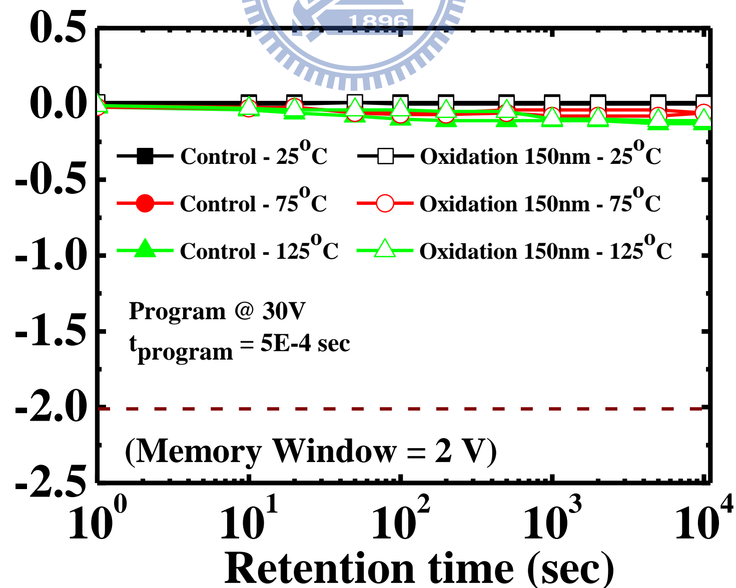
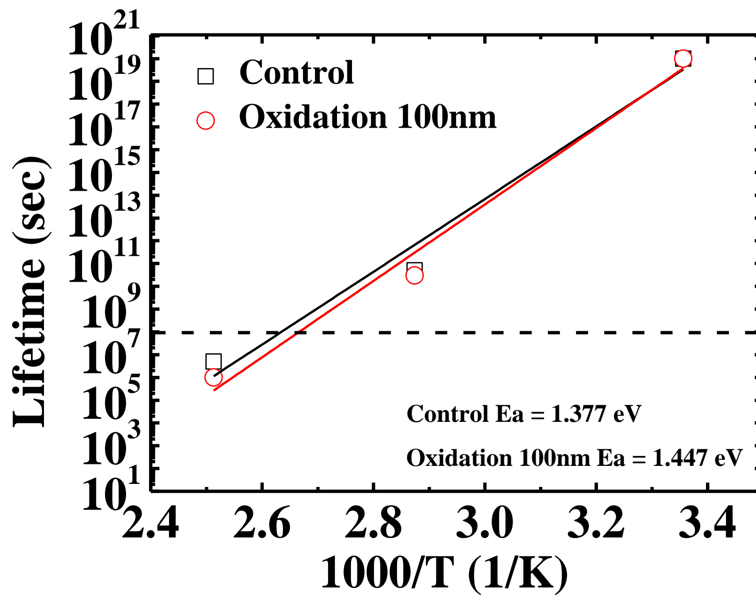
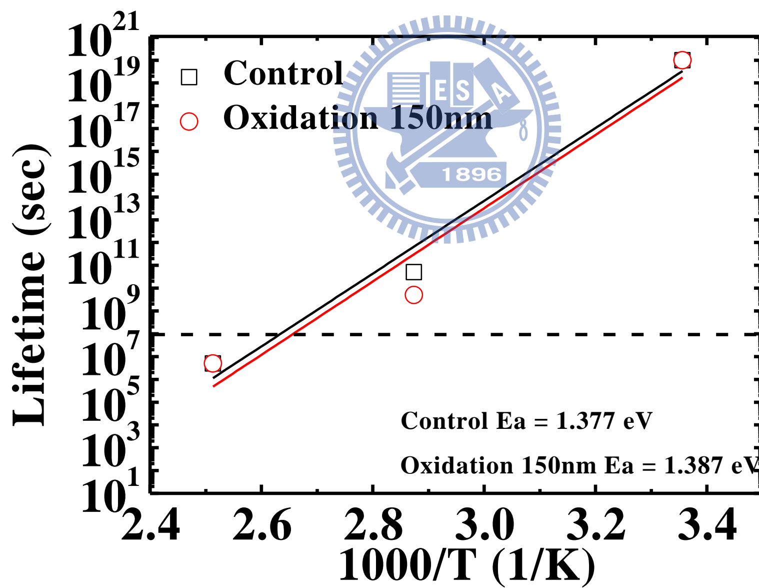


Fig. 4.15 Retention characteristics of M-shape TFT-SONOS memory window at different temperature 25℃, 75℃, and 125℃ for fresh devices with 150nm oxidation.



(a)



(b)

Fig. 4.16 (a) Projection lifetime of data retention with an Ea of 1.447 eV for 100nm oxidation thickness. (b) Projection lifetime of data retention with an Ea of 1.387 eV for 150nm oxidation thickness.

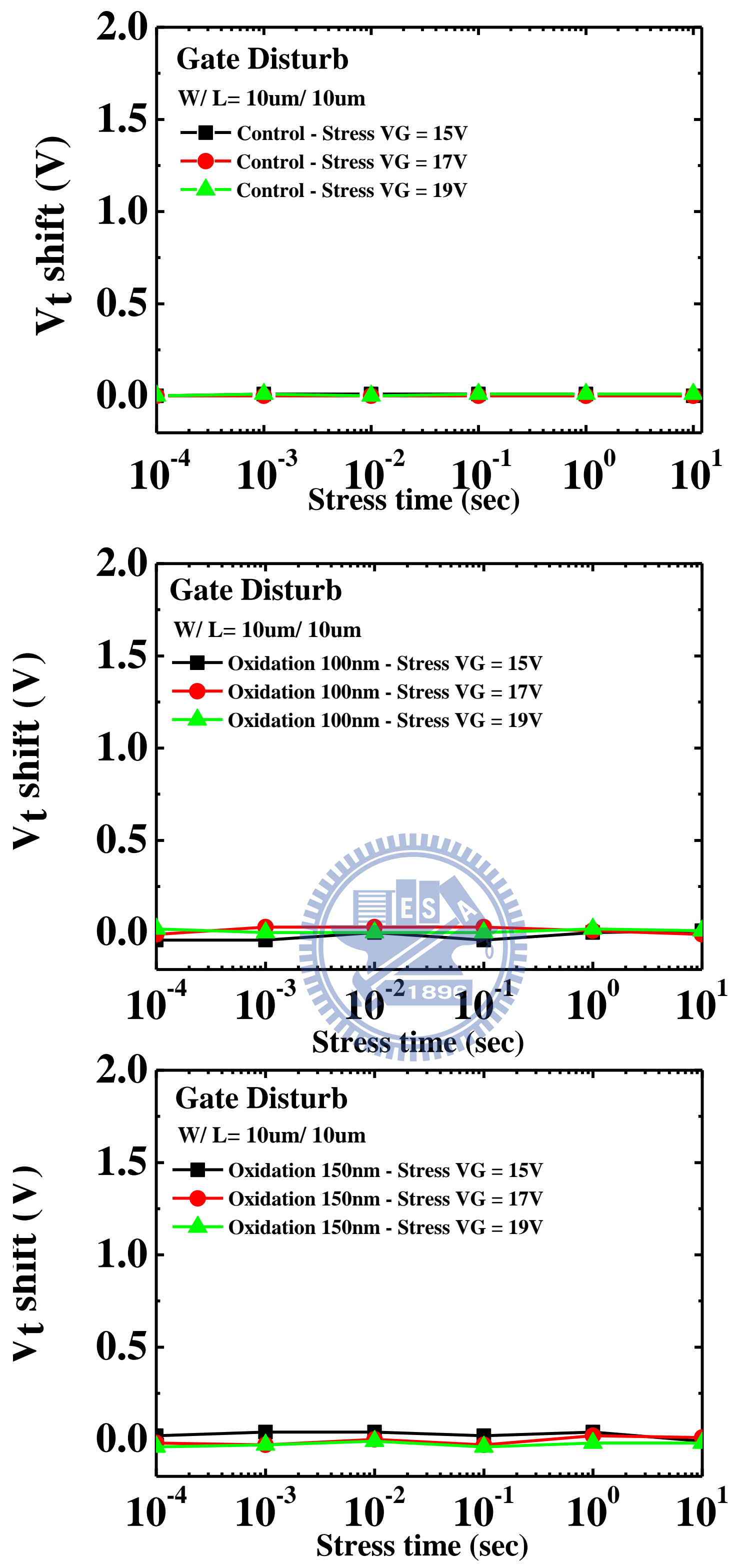


Fig. 4.17 Gate disturbance at W/ L = 10μ m/ 10μ m for stress bias VG = 15/ 17/ 19 V

Chapter 5
Conclusions and Future Work

5.1 Conclusions

In this thesis, for the first time, we propose the corner effect on TFT-SONOS memory. By using the bird beak of LOCOS, corners on each side of width direction was made. We have successfully demonstrated the feasibility of fabricating corners in channel width direction and using local electric field enhancement. In chapter 3, it is our first time attempt to demonstrate the local field enhancement to improve the program/erase speed. The results show the program/erase speed was improved and it still showed excellent reliability. The round corners also provided us another benefit was help us to avoid the problem of double hump. In addition, in chapter 4, we tried to figure out the oxidation thickness dependence with program/erase speed. According to the electric performance, we obtained a conclusion that the structure off-set of channel was not the key point. The platforms and slightly sharp curves of corners of channel width direction were the key factor. This structure was not only improving the program/erase speed but also maintain excellent reliability.

5.2 Challenges and Recommendable Solution

According to the international technology roadmap of semiconductor (ITRS) 2010 [5.1], the demands of non-volatile flash memory not only cheap but also high reliable. However, remaining the memory window after 1E6 P/E cycling numbers is a big challenge for the SONOS memory devices which often maintain endurance among 1E4~1E5 program/erase cycling times. It is due to the oxide degradation happened after many times program/erase stress operation. For our TFT-SONOS memory

devices also face the same reliability issue here. In order to solve the reliability issue, the novel erase method needs to invent for this TFT-SONOS memory to reduce damages in tunneling oxide and efficiency erasing in trapping layer. Moreover, follow the scaling trend of

flash memory cell, the thickness decrease of tunneling oxide and blocking oxide will result in the life time decrease of data retention. Due to this reason, the high dielectric constant materials has been used to substitute for the traditional blocking oxide such as HfO_2, Al_2O_3…etc [5.2]-[5.5]. The high-k materials not only increase the electrical field in tunneling oxide but also data retention time for thicker thickness of blocking layer. As a result, if we combine those novel ideas in this structure of TFT-SONOS memory in the future, it will be able to reach the goals in flash memory device with high performance, low power consumption and excellent reliability.

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5.3 Future Work

We have successfully created corners on each side of channel width direction and this really helps us to enhance the program/ erase window. The erasing is not very efficiency would be an extremely serious problem, because it would degrade the device reliability of program/ erase cycles. To develop an efficiency erasing method is the first important issue of our future work.

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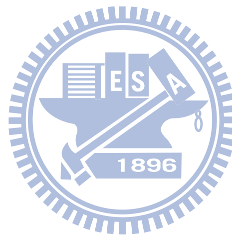

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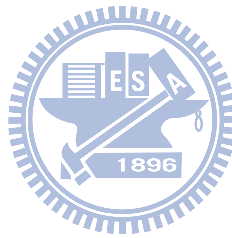

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利用尖角效應提高寫入電場於薄膜電晶體之記憶體元件應用

The Electrical Field Enhancement of Corner Effects on Thin-Film Transistor Nonvolatile Memories