建立二階多位元積分三角類比數位轉換器之設計模型與改進信號雜訊比公式估測之準確度

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摘　　要

在論文中，我們將以二階單迴路多位元積分三角類比數位轉換器架構為主，針對此架構建立出一個設計模型（Model），目的是讓設計者藉由此模型以及我們所建立的步驟來獲得相關重要的參數並快速完成電路的規劃；此外在我們要建立的模型中最關鍵的部份就在於信號雜訊比估算的精確度；在規劃的過程中，若是使用理想的公式來做估算將無法獲得準確的參數預估（如超取比、量化位元數）；另外我們當然可以使用軟體模擬來快速的得到結果，但卻無法獲得相關參數的物理意義，也就無法更深入的去探討問題所在；所以我們將從理論的分析上去研究何種原因導致理想的訊號雜訊比估算失真，並將其原因納入考量以求得到更準確的公式，另外也可觀察在電路設計上有何重要的考量點。

本論文最後提出積分三角類比數位轉換器二階多位元量化架構之設計模型，提供電路資訊如開關使用數目、電容使用數目、量化器之考量與參數之設計流程等等，另外提出信號雜訊比公式的改良，將電路的雜訊納入信號雜訊比公式估算的考量之中。

Build a Design Model and Improve the Peak SNR Equation of Sigma Delta A/D Converters in Single Loop Second Order Multi-Bit Architectures

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ABSTRACT

In the thesis, we focus on sigma delta modulator in single loop second order multi-bits architectures, and build a design model for one. There is a main objective which designer can obtain related parameter and accomplish scheme of circuitry faster. In addition, the most important part of design model is accurate estimation of SNR equation. During the scheme, designer will not obtain accurate parameter (ex. OSR, B) if designer use ideal SNR equation to estimate. We can also use simulation of software, but it can't obtain relation between devices and result of simulation; the problems in SNR equation are also discussed completely. We will modify the SNR equation by systematically analyzing the device noises and incorporate their effects into the SNR equation.

At lastly of the thesis, we present the design model of sigma delta in single loop second order multi-bits architecture which provide the information of numbers of switch, numbers of capacitor, considerations of quantizer and design flow; besides, modify the ideal SNR equation which incorporate the device noise.