

## Reference

- [1] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. John Wiley & Sons, Inc., 1997.
- [2] E. J. Morton, C. Y. Ng, T. Menezes, "Low noise integrating preamplifier with integral ADC," in *IEEE Nuclear Science Symposium Conf. Rec.*, pp. 352-355, Oct. 1999.
- [3] S. Mukherjee, C. Srinivasan, V. Pawar, S. Mathur, K. Godbole, "A 2.5V 10 bit SAR ADC," *VLSI Design, 1997. Proceedings., Tenth International Conference on*, pp. 525-526, Jan. 1997.
- [4] J. Yoo , K. Choi ,and A. Tangel, "A 1-GSPS CMOS Flash A/D Converter for System-on-Chip Applications", *VLSI, 2001. Proceedings. IEEE Computer Society Workshop on*, pp. 135 -139, April 2001.
- [5] S. M. Yoo, T. H. Oh, J. W. Moon, S. H. Lee, U. K. Moon, "A 2.5 V 10 b 120 MSamples/s CMOS pipelined ADC with high SFDR," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 441-444, May 2002.
- [6] M. Clara, A. Wiesbauer, F. Kuttner, "A 1.8V fully embedded 10b 160MS/s two-step ADC in  $0.18\text{ }\mu\text{m}$  CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 437-440, May 2002.
- [7] A. A. Hamoui, K. Martin, "A 1.8-V 3-MS/s 13-bit  $\Delta\Sigma$  A/D converter with pseudo data-weighted-averaging in  $0.18\text{- }\mu\text{m}$  digital CMOS," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 119-122, Sept. 2003.
- [8] Y. Yang, A. Chokhawala, M. Alexander, J. Melanson, and D. Hester, "A 114-dB 68-mW Chopper-stabilized stereo multibit audio ADC in  $5.62\text{ mm}^2$ ," *IEEE J. Solid-State Circuit*, vol. 38, pp. 2061-2068, Dec. 2003.
- [9] R. del Rio, J. M. de la Rosa, F. Medeiro, B. P'erez-Verd'u, and A. Rodriguez -V'azquez, "High-performance sigma-delta ADC for ADSL applications in 0.35

$\mu\text{m}$  CMOS digital technology," in *Proc. IEEE Int. Conf. Electronics, Circuits and Systems*, pp. 501-504, Sept. 2001.

- [10] R. Gaggl, A. Wiesbauer, G. Fritz, C. Schranz, P. Pessl, "A 85-dB Dynamic Range Multibit Delta-Sigma ADC for ADSL -CO Applications in  $0.18\mu\text{m}$  CMOS," *IEEE J. Solid-State Circuit*, vol. 38, pp. 1105-1114, July 2003.
- [11] M. R. Miller, C. S. Petrie, "A Multibit Sigma- Delta ADC for Multimode Receivers," *IEEE J. Solid-State Circuits*, vol. 38, pp. 475-482, Mar 2003.
- [12] K .Nguyen, B.Adams, K. Sweetland, "A 105 dB SNR multibit  $\Sigma\Delta$  ADC for digital audio applications," *IEEE Custom Integrated Circuits Conf.*, pp. 27-30, May 2001.
- [13] G. A. S. Machado, N. C. Battersby, and C. Tomazou, "On the Development of Analogue Sampled-Data Signal Processing," *Analog Integrated Circuits and Signal Processing*, 1996.
- [14] S. D. Norsworthy, R. Schreier, and G. C. Temes, *Delta-Sigma Data Converters—Theory, Design, and Simulation*. Piscataway, NJ : IEEE Press, 1997.
- [15] B. Razavi, *Design of Analog CMOS Integrated Circuit*. McGraw-Hill series in electrical and computer engineering, McGraw-Hill, c2001.
- [16] S. B. Nerurkar, K. H. Abed, R. E. Siferd, V. Venugopal, "Low power sigma delta decimation filter," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 1, pp. I-647—I-650, Aug. 2002.
- [17] K. Y. F. Mok, A. G. Constantinides, P. Y. K. Cheung, "A VLSI decimation filter for sigma-delta A/D Converters," in *Proc. IEEE Int. Conf. Advanced A-D and D-A Conversion Techniques and their Applications*, pp. 36-41, Jul 1994.
- [18] Chao, S. Nadeem, W. Lee, and C. Sodini, "A Higher Order Topology for Interpolative Modulators for Oversampling A/D Converters," *IEEE Transactions on Circuits and Systems*, Vol. 37, No 3, pp. 309–318, March 1990.

- [19] L. Williams and B. Wooley, "A Third-Order Sigma-Delta Modulator with Extended Dynamic Range," *IEEE J. Solid-State Circuits*, Vol. 29, pp. 193-202, March 1994.
- [20] M. R. Miller, C. S. Petrie, "A Multibit Sigma Delta ADC for Multimode Receivers ,," *IEEE J. Solid-State Circuits*, vol. 38, pp. 475-482, Mar 2003.
- [21] M. Rebeschini, N. R. Van Bavel, P. Rakers, R. Greene, J. Caldwell, and J. R. Haug, "A 16-b 160-kHz CMOS A/D Converter Using Sigma-Delta Modulation," *IEEE J. Solid-State Circuit*, vol. 25, pp. 431-440, April 1990.
- [22] F. Medeiro, A. P'erez-Verdu', and A. R. V'azquez, *TOP-DOWN DESIGN OF HIGH PERFORMANCE SIGMA DELTA MODULATOR*. Boston : Kluwer Academic Publishers,c1999.
- [23] B.P.Brandt, B.A.Wooley, "A 50-MHz multibit sigma-delta modulator for 12-b 2-MHz A/D conversion," *IEEE J. Solid-State Circuit*, vol. 26, pp. 1746-1756, Dec. 1991.
- 
- [24] I. Fujimori, L. Longo, A. Hairapetian, K. Seiyama, S. Kosic, J. Cao, S. L. Chan, "A 90-dB SNR 2.5-MHz output-rate ADC using cascaded multibit delta-sigma modulation at 8 $\times$  oversampling ratio," *IEEE J. Solid-State Circuit*, vol. 35, pp. 1820-1828, Dec. 2000.
- [25] J. Markus, G. C. Temes, "An Efficient  $\Delta\Sigma$  ADC Architecture for Low Oversampling Ratios," *IEEE Transaction Circuits and Systems*, vol. 51, pp. 63-71, Jan 2004.
- [26] D. B. Ribner, R. D. Bacrtsch, S. L. Garverick, D. T. McGrath, J. E. Krisciunas, T. F. Fujii, "A Third-Order Multistage Sigma-Delta Modulator with Reduced Sensitivity to Nonidealities," *IEEE J. Solid-State Circuit*, vol. 26, pp. 1764-1774, Dec 1991.
- [27] Beatriz, Olleta, L. Juffer, D. Chen, R. Geiger, "A DETERMINISTIC DYNAMIC

- ELEMENT MATCHING APROACH TO ADC TESTING," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. 5, pp. V-533—V-536, May 2003.
- [28] S. Tao, R. Schreier, F. Hudson, "Mismatch shaping for a current-mode multibit delta-sigma DAC," *IEEE J. Solid-State Circuits*, vol.34, pp. 331-338, March 1999.
- [29] R. Jacob Baker, *CMOS Mixed-Signal Circuit Design*. IEEE Press series on microelectronic systems, Wiley, 2002.
- [30] L. R. Carley, J. Kenney, "A 16-BIT 4' TH ORDER NOISE-SHAPING D/A CONVERTER," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 21.7/1-21.7/4, May 1988.
- [31] R. Jacob Baker, Harry W. Li and David E. Boyce, "CMOS Circuit Design, Layout, and Simulation," xxiv, 902 p. / ill. / 24 cm, IEEE Press 1998.
- [32] P. M. Aziz, H. V. Sorensen, and Jan Van Der Spiegel, "An Overview of Sigma-Delta Converters," *IEEE Signal Processing Magazine*, Jan 1996.
- [33] Paul R.Gray, Paul J.Hurst, Stephen H.Lewis and Robert G.Meyer, *Analysis and design of analog integrated circuits*. John Wiley & Sons, Inc., 2001.