國 立 交 通 大 學

電子物理學系

博士論文

動態臨界電晶體之精簡物理模型與應用

Compact Physical-Based Model and Applications of Dynamic-Threshold-Metal-Oxide-Semiconductor

研 究 生 ：王冠迪

指導教授 ：趙天生 博士

中華民國 一百年 七月

動態臨界電晶體之精簡物理模型與應用

Compact Physical-Based Model and Applications of Dynamic-Threshold-Metal-Oxide-Semiconductor

指導教授：趙天生 博士　　Advisor : Dr. Tien-Sheng Chao

研 究 生：王冠迪　　Student : Kuan-Ti Wang

國立交通大學

電子物理學系

博士論文

A Dissertation

Submitted to Department of Electrophysics

College of Science

National Chiao Tung University

in Partial Fulfillment of the Requirements

for the Degree of Doctor of Philosophy

in Electrophysics

July 2011

Hsinchu, Taiwan, Republic of China.

中華民國 一百年 七月

動態臨界電晶體之精簡物理模型與應用

指導教授 ： 趙天生 博士　　**研 究 生 ： 王冠迪**

國立交通大學

電子物理學系

摘要

首先，我們將傳統的最大電導外插法萃取臨界電壓值的方法應用在動態臨界電晶體上，成功的利用實驗結果證明此方法亦可應用在動態臨界電晶體上；接著利用等效電位的概念，我們用能帶模型來表示動態臨界電晶體藉由控制閘極與源極的電位而順利達到接近完美的通道電位控制；更進一步地，我們提出一種新穎的基板效應常數萃取方式—*m* 模型，相較於傳統必須量測不同基板電壓所呈現的臨界電壓變化來繪圖萃取曲線斜率的複雜方式，此新穎的方法可以快速的在單一元件上萃取出基板效應常數，並用來設計動態臨界電晶體臨界電壓。此外，動態臨界電晶體相對於傳統電晶體可以有更好的抵抗短通道效應的能力(~9%改進)，這是由於從源極與汲極端所產生的關鍵穿遂電場可以透過順向基板電壓的控制而降低；分離式電容電壓的量測方式則證明動態臨界電晶體在相同的反轉層電荷密度下，能夠使載子遷移率有 32%增進，主要原因是順向基板效應有效降低空乏區電荷；利用金屬閘極(TaC、TiN)取代傳統多晶矽閘極(Poly)來抑制閘極空乏區的效果可以有效降低等效氧化層厚度約 4 埃；彈道傳輸係數對順向基板電壓的特性結果則顯示動態臨界電晶體在抑制汲極端引起能障降低的效應過程中，亦將同時降低彈道傳輸係數；而射入速度則可以隨著載子遷移率的增加而上升。

此外，我們提出一種新穎的動態臨界源極射入法在具有隱藏式選擇性閘極之快閃記憶體元件於 NOR 電路陣列上，此元件不僅製程簡單也符合一般數位邏輯 CMOS 產品中的嵌入式非揮發性記憶體應用。在論文中，我們利用 ISE 電腦輔助設計模擬軟體結合記憶體製程與熱電子注入模型的研究成果來詳細的說明此動

態臨界源極射入法的寫入機制。模擬的結果顯示當隱藏式選擇性閘極記憶體操作在動態臨界源極射入法下將受幾個重要的因素所影響，其中包含了寫入電流量的大小與在隱藏式選擇性閘極記憶體中性區間的橫向電場與垂直電場。因此，我們比較在此記憶體結構中三種不同操作模式下的寫入效率，分別為：傳統源極射入法、基板偏壓增進源極射入法與動態臨界射入法。從量測實驗資料與電腦輔助模擬結果中可以發現，相較於傳統源極射入法，動態臨界射入法能同時大幅度的增加寫入電流量(~450%)與中性區間的最大橫向電場量值(~6%)，進而擁有較高的寫入效率。最後，我們利用動態臨界模式來完成具高效能(τ_{PGM}=200ns/τ_{ERS}=5ms)而低功率消耗(~25%降低)的單細胞二位元多層級操作，藉著利用動態臨界源極射入法的操作，多層級操作可以有更好的臨界電壓感測分佈區間、較低的單細胞二位元效應、優異的耐久力特性與良好的資料保存力。

最後，我們探討了操作溫度對動態臨界電晶體的影響，發現驅動電流對閘極偏壓變化中有一零溫度係數點(Zero-Temperature-Coefficient Point)，此零溫度係數點的發生，主要是因為臨界電壓與載子遷移率的互相補償結果；同時，當此動態臨界電晶體操作在低溫環境中，則可以降低關閉電流(off-current)，主要的原因是當元件隨著操作環境溫度降低時，本質載子密度會隨之下降(n_i)，造成臨界電壓值上升；而低溫下(-50^{o}C)的驅動電流則可以有 1.4 倍的提升。因此，正確的預測零溫度係數點將有助於操作動態臨界電晶體於不同環境溫度的應用，因此我們提出了一種新穎的動態臨界電晶體之零溫度係數模型來預測其操作點，可以非常準確的將誤差值降低在 2%左右，其中短通道元件必須考慮汲極端偏壓降低能障效應對溫度與臨界電壓變化的影響。從實驗結果與理論模型上，亦可發現從固定基板偏壓的零溫度係數模型延伸至動態臨界電晶體上的零溫度係數模型是有一致性的結果，藉著將元件物理參數對操作環境溫度的影響詳加考慮，可以藉由適當的調整金屬功函數、基板效應常數與動態基板電壓對閘極偏壓的變化值來設計出動態臨界電晶體所需要的零溫度係數點。

Compact Physical-Based Model and Applications of Dynamic-Threshold-Metal-Oxide-Semiconductor

Advisors：Dr. Tien-Sheng Chao **Student：Kuan-Ti Wang**

Department of Electrophysics

National Chiao Tung University

Abstract

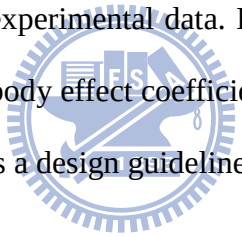
First, we use the maximum transconductance linear extrapolated method to extract V_{TH} of DTMOS. It can largely reduce drafting time of extracting V_{TH} of DTMOS by using this method. Furthermore, we lead the equivalent potential concept into DTMOS to indicate the channel potential control ability of both gate and source terminals with using band diagram, simultaneously. It deduces the *m*-model for extracting body effect coefficient without complicated variable substrate bias and fitting process. In addition, the penetration electric field from drain/source can be suppressed by the forward body bias of DTMOS, especially for short channel device. As a result, it improves the short channel effect (~9%) in DT technology due to decreasing of charge sharing effect. Then, we use split C-V to extract the effective mobility of DTMOS. Comparing to normal device, the higher mobility (~32%) of DTMOS can be attributed to the decreasing of normal electrical field for minor depletion region. The effect oxide thickness about 4 A of DTMOS can be reduced by using metal gate (TiN、TaC) to replace poly gate. It achieves by eliminating poly gate depletion. Besides, we prove that DTMOS owns the lower ballistic transport coefficient with higher injection velocity from source terminal due to its suppression of DIBL effect.

For the first time, high-performance with superior reliability characteristics is

demonstrated in a NOR-type architecture, using dynamic-threshold source-side injection (DTSSI) in a wrapped select-gate (WSG) silicon-oxide-nitride-oxide-silicon (SONOS) memory device, with multilevel and 2-bit/cell operation. The DTSSI programming mechanism was thoroughly investigated using the Integrated Systems Engineering (ISE) TCAD simulation tools combining the fabrication procedure and physical models. Results show the major factors affecting the DTSSI technique, including the supply current, and the lateral and vertical electric fields between the neutral-gap regions in the WSG-SONOS memory cell. Moreover, a programming mechanism for conventional source-side injection (Normal-mode), substrate-bias enhanced source-side injection (Body mode) and dynamic-threshold source-side injection (DT mode) of wrapped-select-gate SONOS (WSG-SONOS) memory is also developed with 2-D Possion equation and hot-electron simulation and programming characteristics measurement for NOR flash memory. Compared with traditional SSI, the DTSSI mechanisms are enhanced in terms of lateral acceleration electric field (~6%) and supply current (~450%) in the neutral gap region, resulting in high programming efficiency. It also provides lower power consumptions (~25% decrease). Finally, the high-performance (τ_{PGM}=200ns/τ_{ERS}=5ms) with low supply current in DT mode is used to achieve the multilevel and 2-bit/cell operation. Using the DTSSI enables easy extraction of the multilevel states with tight V_{TH} distribution, nearly negligible second-bit effect, superior endurance characteristics, and good data retention.

Finally, we discuss DTMOS with regard to operation temperature effect. We find a zero-temperature-coefficient point with no current variation at elevated temperature in DT mode operation. The main reason is that compensation between threshold voltage and mobility at elevated temperature. Once operating the device with higher

gate voltage than ZTC point, the phonon effect would degrade on current of device. On the contrary, the lower operation gate voltage than ZTC point would enhance the driving current due to its low threshold voltage at higher operation temperature. The decrease of threshold voltage is result from the increase of intrinsic density of material at elevated temperature. As a result, predicting the location of ZTC point precisely is very important to design device at different operation temperature. It can help to perform the circuit more stable and work well. Here, we propose a clear and simple ZTC point modeling of DTMOS with considering physical insights carefully. Using our DTMOS ZTC modeling, the mismatch value between our model and experimental data, no matter long channel or short channel device, can be reduced lower than 2%. Furthermore, the ZTC point of DTMOS can also be consistent by extracting from fixed body bias experimental data. It shows that optimum ZTC point of device can be adjusted by the body effect coefficient, work function and alpha ratio. Consequently, our model provides a design guideline for green DT technology.



誌 謝

畢業了！內心裡真的很開心且充滿激動，我最先要感謝的是雙親—王勝忠先生、林惠姝女士以及所有的親人們，因為有了你們長久以來對學生的細心呵護與鼓勵，我才能在做人處事與課業上有所進展與呈現，我在此要深深的向你們獻上最深摯的謝意與祝福，我愛你們！

然而，在這遠離家鄉在外求學的日子當中，最令我感謝的就是指導教授—趙天生老師。謝謝老師給予機會讓我能在實驗室中一起學習與成長；日常生活中老師常給予學生種種的指導與教誨，從老師日常的待人處事與學術研究的專業領域中，都讓我獲益匪淺；我也必將老師說過「取之於社會，必回饋於社會」的想法努力實踐，於此摯誠感謝老師的一切付出。

另外，我還要感謝博士生涯期間，實驗室眾多學長姐：郭柏儀學長、陳建豪學長、羅文政學長、吳偉成學長、馬鳴汶學長、呂宗宜學長、黃竣祥學長、高國興學長夫婦、呂宜憲學長、呂侑倫學長、林哲緯學長、賴妍心學姐、劉美君學姐、邱德馨學長...等的照顧，因為有各位學長姐幫實驗室打好基礎的緣故，才能讓後來的我們蒙受許多恩惠；特別是經過宜憲、侑倫與哲緯學長們平日對我幽默的夾擊，才讓我更能體會世道難行(笑)，接下來就要換你們了！加油！。此外，非常謝謝博士班同學宗育在我博士班的求學生涯給予我許多寶貴的意見，不論是實驗製程或生活經驗，都因為你而讓我提昇許多人生經驗，謝謝你一路不斷的付出，讓實驗室的運作一切正常。而有智盟(社會學博士)你在的地方就是充滿歡樂的地方，任何的大壓力都可以藉由你來快速排解，你在我心中是最強的 A 咖級娛樂界天王。同時，我也要謝謝博士班同學翊鴻在日本行對作為室友我的細心關照，讓我能順利帶回種種戰利品與美好回憶，為博士生涯畫下美好的句點。更有一同埋首專研論文與實驗的學弟妹：琬琦、芳昌，因為有你們的激勵與幫助，才能讓我順利畢業並使包容心不斷增大(笑)，特別的由衷感謝你們二位；其他不停增添我生活色彩的學弟妹們：士安、啟瑞、才民、時璟、聿民、政昌、立盈、昱璇、添舜、其儒、聖賢、繁達、邵軒、柔含、明慈、文馨、芳瑜...等，因為有了你們作為實驗室大家庭的成員，才能讓日常生活中充滿歡笑與淚水，使繁瑣的學術研究中增添了數分的色彩與寫意，謝謝你們的鼓勵與支持！還有謝謝同樣位於工六

內的系辦人員與其他實驗室同學的付出與包容：徐純妹小姐、黃明姿小姐、翁珮婷小姐、劉昇瓚小姐、黃偉德先生與張榮興學長、志宣、孟謙、妍君、小白熊…等，祝福你們都能順利通過種種人生關卡。

此外，我還要感謝的是圍繞在身邊的一群室友與好友們：老大菘宏、帥哥青宇還特別跑來參與我的口試過程，試圖想要擊垮我(笑)；悶燒男伯駿對我人生準備創業的默默支持與特別的環島禮物；新婚的翔耀與依淇夫婦帶來的幸福感；家駿與岷臻為我帶來另類的生活歡笑與人生建議；立堂與玉喬在星期五陪我一同探索新竹的美食地點與談論好笑的人生經驗，還有家群未來將要出生的小寶寶所帶來的好運…等，你們總是給我很多積極正面的鼓勵與支持，我真的很幸運，能與你們一同成長茁壯，祝願你們未來皆能平安健康喜樂。

在博士班研究生涯中，學生要感謝 NDL 內所有的服務人員與機台維護人員，因為有大家的耐心照顧，才能讓實驗順利完成。而要特別感謝的是鑫創科技股份有限公司與其經理李建興學長所提供於非揮發性快閃記憶體元件與量測技術上的建議與協助。

最後，學生要感謝在這短短的二十八年當中所遭遇的人事物，因為這些因緣的成就與佛菩薩的慈悲加被，才能有此時此刻的學生，摯誠感謝。阿彌陀佛！

學生：王冠迪 合十

誌於 風城交通大學

Contents

Table Captions

Chapter 2

Chapter 3

Chapter 4

Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 1

Introduction

1.1 Background

Recently, the concepts of “More Moore” and “More than Moore” have been discussed and refined in the International Technology Roadmap for Semiconductors (ITRS) 2009 [1.1], as shown in Fig. 1.1. According to the “More Moore” axis, the geometrical scaling refers to the continued shrinking of horizontal and vertical physical feature sizes on chip logic and memory storage functions in order to improve density (cost-down per area), performance (power and speed) and reliability abilities to the customers and application. However, it ensues the many grand technological challenges needed to be overcome from following the planar CMOS, Flash and DRAM devices’ continued scaled-down to submicron regime. Especially for the planar CMOS device’s scaling continues a 2.5 year cycle and flash device is 2 year cycle, respectively. Besides, the researches of “Parallel Paths” of traditional planar bulk metal-oxide-semiconductor field transistor such as: fully depleted silicon-on-insulator MOSFET (FD-SOI) and multiple gate structure (FinFET, Nanowire) are also very popular for advanced application in the “More Moore” future technological issues.

In order to enhance device performance, for the conventional constant field path of logic device scaling, that was accomplished by reducing the gate length, reducing the gate dielectric thickness and then increasing the channel doping concentration to avoid the un-ideal effect such as seriously short channel effect (SCE) and drain-induced barrier lowering (DIBL). Therefore, it results that the application requirements no longer both meet the performance and power consumption, simultaneously. Figure 1.2 shows the typical I_g-V_g characteristics of simulation and

measurement data under nMOSFET operation regime [1.2]. The results indicate the gate oxide leakage current will exceed more than the baseline limit of 1 A/cm^2 set for low stand-by power dissipation (LSTP) while the gate oxide scaled down to 1.5 nm for gate voltage biased at 0.5 V at 25°C. As a result, in order to break the scaling barriers, introducing a new material system (Silicon/High-k/Metal gate) for higher process control improvement with lower power consumption is as important as new device structure development. Particularly, using the high-k material, such as HfO_2, HfSiON, ZrO_2, Al_2O_3, Gd_2O_3 and HfZrO, to replace the oxynitride for suppressing the direct tunneling current with reducing the equivalent gate oxide thickness (EOT), has emerged the most difficult challenge associated with the future device scaling [1.3-1.6]. This is because the high-k materials don't like the traditional silicon dioxide with poly silicon gate device that has played the most reliable stack system for a long time. It encounters the seriously interfacial layer production, Fermi level pinning and reliability (soft breakdown and hard breakdown) issues [1.7-1.9]. In addition, the trade-offs of the high channel doping concentration to control short channel effect is to degrade the carrier mobility and increase the junction leakage of device. Particular in very short channel device beyond 45nm, the higher doping would also increase the fluctuation of threshold voltage results in the difficulty of circuit design while scaling the power supply voltage. As a result, the proposed solutions for these challenges should be considered to achieve concurrently with stable characteristics of device architecture and circuit design level.

On the other hand, similar to the traditional planar MOSFET, the flash memory device would also faces its specific challenges, such as non-scalability of interpoly dielectrics, dimensional control, non-scalability of tunnel dielectrics and dielectric material properties, beyond 2010. Either NOR and NAND in flash memory architecture, the difficult demands are that continually scale and reduce the

write/erase operation voltage with quiet thinner tunnel oxide and inter-poly blocking dielectrics for the smaller dimension device [1.10]. This is due to the tunnel oxide shrinks beyond 8 nm would result in the serious charge loss path, called stress-induced leakage-current (SILC), after cycling [1.11]. At the same time, the inter-poly dielectric stack system must be thin enough to keep an almost constant coupling ration but thick enough to assure the data retention to avoid the failure bit occurrence. As a result, these trade-off problems are suggested the need to introduce high-k material, 3D structure devices and silicon-oxide-nitride-oxide-polysilicon (SONOS) device into flash memory fabrication process [1.12-1.14].

Recently, the silicon-oxide-nitride-oxide-silicon (SONOS) memory device has become one of the most popular candidates for replacement of conventional FG memory when shrinking the tunneling-oxide thickness to 5 nm [1.15-1.16]. This is due to property of the material, which causes local trapping of silicon nitride, in turn helping the discrete electrons stored in the deep trap sites to resist tunneling-out processes through the tunneling-oxide. In addition, the density of flash memory devices can be doubled without increasing the die size, a phenomenon known as 2-bit/cell operation [1.17-1.18], under separated storage characteristics. This has been achieved by the well-known Channel Hot-Electrons Injection (CHEI) method for programming each side of a cell. The bit-1 and bit-2 can then be read-out using the highly reliable reverse-read scheme [1.19]. Furthermore, similar to 2-bit/cell operation, multi-level states in a cell (MLC) is another attractive approach for achieving high-density application in a flash memory device [1.20-1.21]. MLC operation entails construction of different levels of charge in the nitride trapping layer of a SONOS device. The different combination of charge states is then identified using a highly reliable method for distinguishing between each level of charge.

Now, the current mainstream types of non-volatile memory (NVM) is still charge

storage mechanism, both NOR and NAND flash architecture. Other, non-charge storage types of NVM are also developed, including phase change RAM (PRAM), ferroelertic RAM (FeRAM) and magnetic RAN (MRAM). All of them, the scaling difficulties are still the key issue with ensuring the very low levels of charge loss leakage [1.22-1.23].

1.2 Motivation

According to the International Technology Roadmap for Semiconductors (ITRS) 2010, as shown in Fig. 1.3, the power consumption of total chip power will be more than 4 w in 2015 [1.1]. The main driven factors of increased power consumption are the higher interconnect overall capacitance and resistance, the higher chip operating frequencies and the increasing of exponentially growing leakage of scaled transistor on chip. Normally, the maximum power trend can be presented in three categories, they are portable battery electronic operation, cost-performance and high performance PC application, respectively. As a result, selection of appropriate power supply voltage (V_{dd}) continues to be an important section to simultaneously optimize power and performance for integrated circuit products. On the other hand, in order to adapt the power consumptions to a reasonable value, the power supply voltage (V_{dd}) should be reduced down to less than 0.6 V in 2013. Other, the reduced transistor channel length and reliability of gate dielectrics are also the driven factors to reduce the power supply voltage. In addition, due to the gate delay increasing is proportional to the reduction of V_{dd}, the reduced power supply voltage would seriously degrade the circuit performance. Then, the threshold voltage of transistor must be simultaneously decreased as V_{dd}. However, it leads to the large increasing of exponentially growing leakage in subthreshold off-current of stand-by power again. Therefore, it is very hard

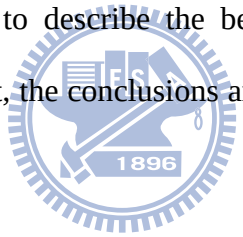
to reach both the high speed and low power consumption application.

For the reasons mentioned above, the main purpose of this research is to develop the concept of high performance with low power consumption with utilizing the dynamic threshold technique application. Figure 1.4 shows the dynamic threshold operation scheme, which is accomplished by connecting the gate to the well or body [1.24-1.26]. Owing to the parasitic n-p-n or p-n-p bipolar in CMOS circuit, the operation voltage should be maintained less than 0.7 V or junction leakage would increase violently. The feature of the Dynamic Threshold MOSFET (DTMOS) is a high threshold voltage (V_{th}) at stand-by scheme (V_{gs}=0V) and a low threshold voltage at transistor turn on (V_{gs}=V_{dd}). Then, the subthreshold leakage of off-state can remain a quiet low levels same as conventional MOSFET. On the other hand, due to the body-effect affection, the threshold voltage under DT-mode is dynamic variation which results in the almost idea subthreshold swing (S.S. = 60 mV/decade) and larger gate overdrive (V_{dd}-V_{th}) of transistor. Furthermore, the un-ideal short channel phenomenon, including V_{th} roll-off, drain-induced barrier lowering (DIBL) and mobility degradation could also be improved by using the dynamic threshold technique. Therefore, the author wants to use the concepts/merits of DT into these sub-micron advanced devices including WSG-SONOS memory device and high-k/metal gate planar devices. Finally, we want to simultaneously detail the DT mechanisms both in WSG-SONOS and high-k/metal gate planar devices in this thesis.

1.3 Organization of the thesis

The organization of the thesis is separated into five chapters. After a brief introduction of the relationships between device challenge issues and DT technique in chapter 1, we will detail *m*-model to extract body effect coefficient without complicated variable substrate bias and fitting process. It demonstrates the excellent

channel potential control ability of DTMOS. In addition, the detail physical insights of electrical characteristic are also measured and verified between normal and DT-modes for short channel device with HK/MG gate stack. It provides definite advantages of DT technology for advance scaled-down era in the chapter 2. Furthermore, we will demonstrate the characteristics of high-performance and high-reliability dynamic threshold source-side injection (DTSSI) for 2-bit/cell with MLC operation of wrapped-select-gate SONOS in NOR type flash memory. The DTSSI programming mechanism and programming efficiency among three modes (DT-mode, normal-mode and body-mode) would also be detailed in the chapter 3. In addition, the temperature effect would affect device characteristics is well known and want to clarify definitely for stable DT technology application. We introduce a compact and clear ZTC model to describe the behaviors of DTMOS at elevated temperature in the chapter 4. Last, the conclusions and future works will be presented in the chapter 5.



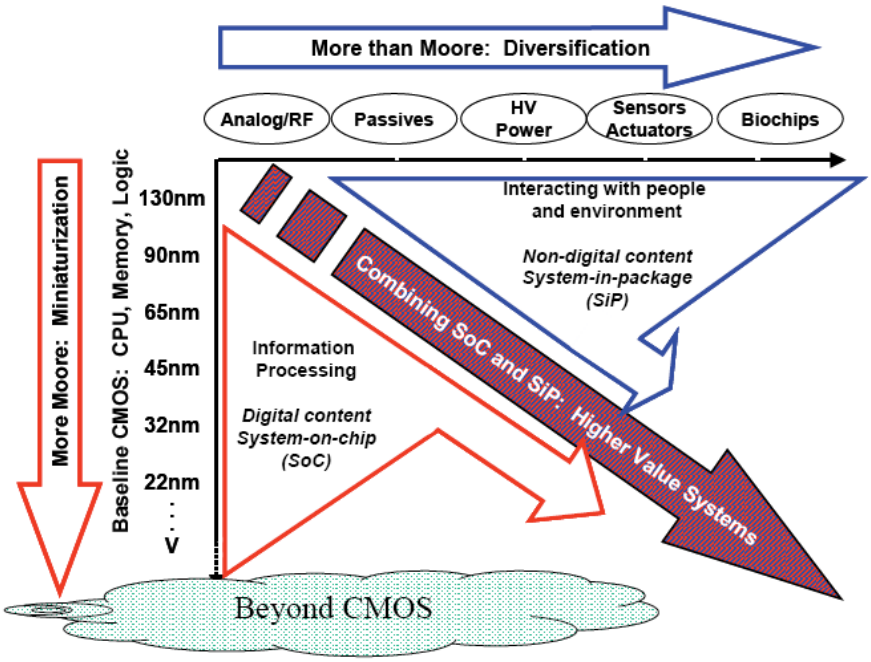


Fig 1.1 “More Moore” and “More than Moore” [1.1]

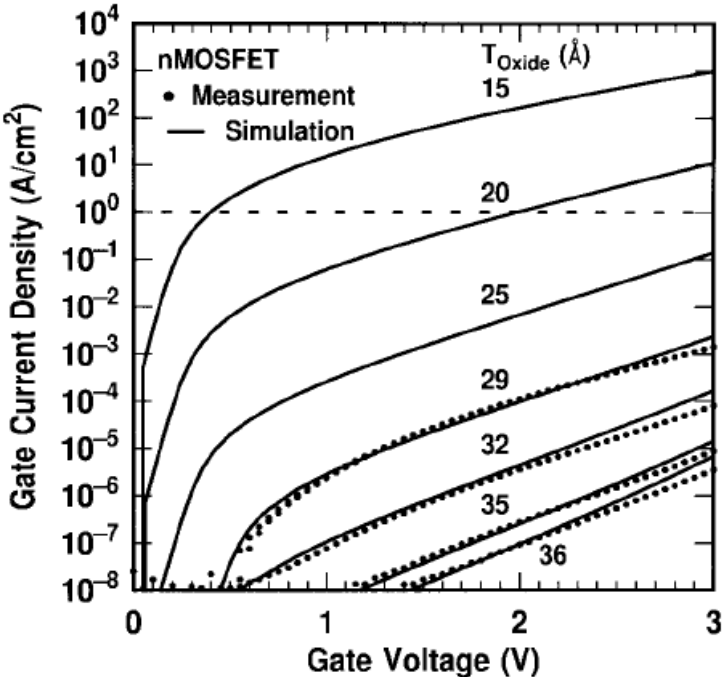


Fig 1.2 Measured and simulated I_g–V_g characteristics under nMOSFET operation regime. The baseline line indicates the 1 A/cm^2 limit for leakage current at 25^{o}C [1.2].

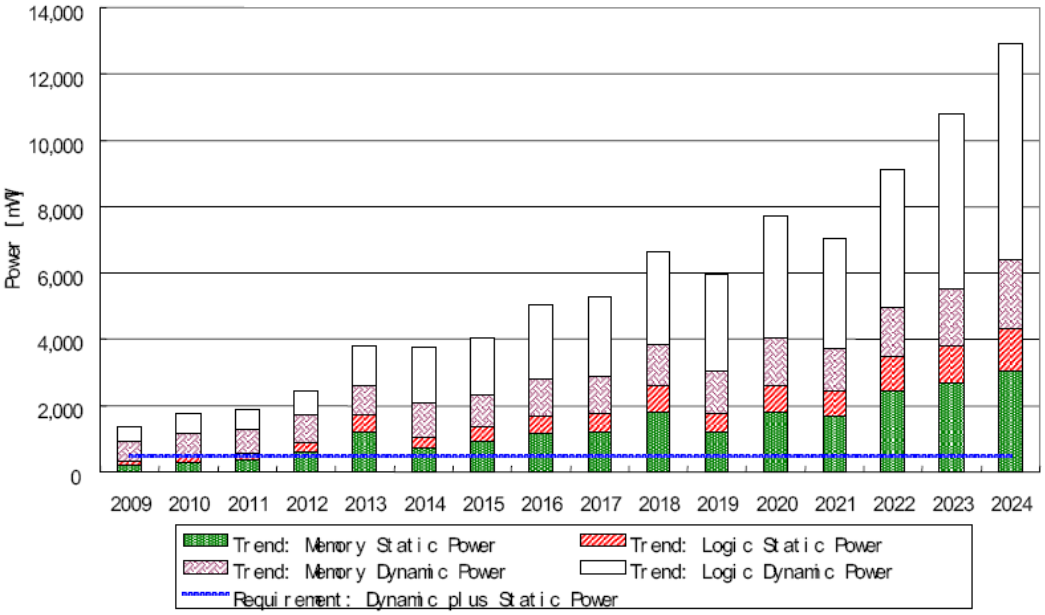


Fig 1.3 The SOC power dissipation anticipation of ITRS [1.1]

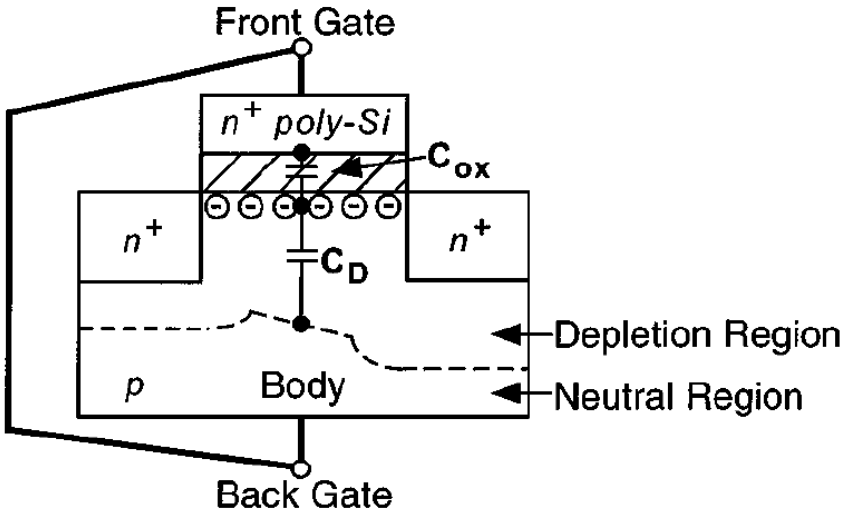


Fig 1.4 The interpretation of dynamic threshold scheme for planar transistor which n^+ poly-silicon gate is connected to the body [1.26].

Chapter 2

Basic Physical Insights and Electrical Characteristics of DTMOS with Different Gate Stack System

2.1 Introduction

Assaderaghi et al demonstrated the physical insights and design guidelines of dynamic threshold (DT) MOSFET, through both experimental and two-dimensional simulation approaches [2.1]. It shows the excellent subthreshold swing about 61mV/decade and quite low static power consumptions (low off-leakage) with higher overdrive. It also derives the gate voltage work point of DTMOS from subthreshold region to linear region by using traditional threshold voltage formulations with considering the body effect. It provides a lot of ideas for designing the DTMOS. For the reasons, using DT technique applications to attain high performance with low power consumption is a popular approach found in many MOS technologies, including 6T-SRAM, multiplier, RFID circuit and low voltage analog circuit [2.2-2.6]. According to [2.1] and [2.7], the V_{TH} value of the transistor should be less than three to four times the low power supply (V_{DD}) for high performance CMOS circuits. Generally, the V_{TH} of DTMOS can be defined by DC measurement by extracting V_{TH} in fixed substrate bias mode. However, this is not a straightforward method due to the complicated extraction and drawing process. In this thesis, to solve these problems, we show that the traditional maximum transconductance linearly extrapolated threshold voltage method with low drain bias (50~100mV) is still effective in DTMOS [2.8]. By using the maximum transconductance linear extrapolated method to extract V_{TH} of DTMOS, it can largely reduce the time of graphical fitting process. In addition, our proposed *m*-model directly extracts the threshold voltage (V_{TH}) and body effect coefficient (*m*) of DTMOS without complicated variable substrate bias and fitting processes under DC measurement. For the first time, we derive and verify the *m*-model with gate control ability for operations at typical room temperatures to military range (25℃-125℃) with different alpha ratios in DTMOS. We prove the gate control ability can be largely enhanced by DTMOS and derive the mathematical expression with physical insights clearly. Furthermore, we utilize the *m*-model with different substrate doping profile, including uniform, high-low and retrograde doping profile, to analysis and predict the important device characteristics of DTMOS.

Finally, we prove the device characteristics and short channel effect can be improved by using DTMOS with Metal gate/High-k systems [2.9-2-15].

2.2 Experiment

2.2.1 Device Fabrication

The Metal gate/High-k advanced transistors used in this work were fabricated by state-of-the-art 300 mm wafer with foundry technology. To reduce the low quality interaction between gate dielectric and silicon bulk, the interfacial layer was formed by chemical oxide. In turn, the gate dielectric with [Hf]/(Hf+Si) were deposited by atomic-layer deposition (ALD) techniques. N_2 ambient annealing was used to decrease the dielectric defects. It followed by a 100Å physical vapor deposition (PVD) metal film (including: TaC and TiN) and a 1000Å polysilicon gate capping layer. After gate patterning, halo implantation was used to optimize the short channel control for short channel devices. Eventually, BEOL process is following a high-temperature annealing to active the source/drain junction of device.

2.2.2 Measurement setup

In this thesis, the DTMOS are operated by connecting the gate with the substrate electrically. The substrate bias may thus be given as:

$$V_{BS} = \alpha V_G \quad (0 \le \alpha \le 1) \qquad (2.1)$$

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate. Due to the limitation of V_{BS} <0.7V under DT mode, the validation range of α is also defined in equation (2.1). Devices operated under normal and DT-modes while the $\alpha = 0$ and $\alpha > 0$, respectively. In our experiment, we compare the electrical characteristics of three different gate stack system (Poly/HfSiON, TaC/HfSiON and TiN/HfSiON) both under normal and DT-modes. For the third part of the chapter 2, to show the differences easily and effectively between normal and DT-modes, we use the constant current method (I_D=40(W/L) nA), which painstakingly makes drain current independent of device geometry, to define the V_{TH} of devices both under normal and DT-modes for NMOS and PMOS, respectively. In addition, we extract the drain induced barrier lowering (DIBL) effect and subthreshold swing as defined as following expressions:

$$DIBL \equiv \left.\frac{\Delta V_{TH}}{\Delta V_{DS}}\right|_{V_{DS}=0.1 and 0.7V} \tag{2.2}$$

and

$$S.S. \equiv \left(\frac{\partial \log I_D^{subthreshold}}{\partial V_{GS}}\right)^{-1} \tag{2.3}$$

,both electrical characteristics of DIBL and S.S. are referred to the short channel effect as device continued scaled-down. We extract them by DC measurement with using Keithley 4200 semiconductor parameter analyzer. Furthermore, we extract the effective mobility with using split C-V method for both under normal and DT-modes. The split C-V characteristics are measured at a frequency of 1 MHz with different metal gate devices to extract the gate to channel (C_{GC}) and gate to bulk capacitance (C_{GB}) by using HP 4284 LCR parameter analyzer [2.8]. Finally, we summarize the advantages of DTMOS in the conclusions of the chapter 2.

2.3 Results and Discussions

2.3.1 A Novel Threshold Voltage (V_{TH}) and Body Effect Coefficient (m) Extraction Method (m-model) of DTMOS

2.3.1.1 M-Modeling

Before starting to build our *m*-model, the V_{TH} of DTMOS here should be defined its meaning, due to its dynamical change of V_{TH}, as the gate voltage point which DTMOS works from subthreshold region to triode region. Figure 2.1 shows the V_{TH}-V_{BS} characteristics of transistor with fixed body bias mode. The decrease in the V_{TH} as the forward body bias increases may be considered a continued reduction of the depletion charge. The V_{TH} of device is extracted by the linearly extrapolated threshold voltage of the maximum transconductance method, where V_D=0.1V [2.8]. The straight lines demonstrate that the body bias varies dynamically with the gate bias. As same as mentioned before, because the DTMOS transistors are operated by connecting the gate with the substrate, the body bias may be given as:

$$V_{BS} = \alpha V_G \quad (0 < \alpha \leq 1) \tag{2.4}$$

The α is defined as a constant ratio of the dynamical biases between the gate and substrate. It should be noted that, the crossover points in Fig. 2.1 show the V_{TH} of

DTMOS. For the junction turn-on limitation of $V_{BS} < 0.7V$ in DTMOS, the validation range of α is also defined in equation (2.4). Devices are operated under normal and DT-modes in which $\alpha = 0$ and $\alpha > 0$, respectively.

The physical insight of V_{TH} is usually defined as the gate voltage when the surface potential (ψ_s) reaches $2\psi_{fp}$, where the potential ψ_{fp} is the difference between E_{Fi} and E_F. At the threshold condition, the total capacitance of MOSFET acts like the oxide capacitance (C_{ox}) and bulk depletion capacitance (C_{dm}) in series condition. Thus, the variation of surface potential may be expressed as a function of gate voltage [2.7]:

$$m \equiv \frac{\Delta V_G}{\Delta \psi_S} \tag{2.5}$$

where

$$m = 1 + \frac{C_{dm}}{C_{ox}} \tag{2.6}$$

The *m* factor is called the body effect coefficient, where $\Delta \psi_s$ is the incremental change of surface potential due to incremental change of gate voltage. While equation (2.6) is valid for both uniform and nonuniform bulk doping profiles, based on the physical concepts, by considering the surface potential (ψ_s) can be controlled by gate and source terminals under DT mode, simultaneously. The control capability of the channel potential in our *m*-model can be expressed as:

$$\frac{V_{TH,Normal}}{m} = \frac{(1-\alpha)V_{TH,DT}}{m} + \alpha V_{TH,DT} \qquad (0 < \alpha \le 1) \tag{2.7}$$

The left term of equation (2.7) exhibits the need of surface potential to achieve the $2\psi_{fp}$ band bending for the threshold voltage. By using the equivalent circuits to evaluate the effect of the body bias on DTMOS (keeping the substrate ground), the right term of equation (2.7) shows the $2\psi_{fp}$ band bending can be performed by the gate and source terminals under DT mode, simultaneously. When the boundary condition is α=1, the threshold voltage relationship between normal and DT-modes can be given as:

$$\frac{V_{TH,Normal}}{m} = V_{TH,DT} \tag{2.8}$$

This is directly referred to as the body effect coefficient (*m*), as a result, called it *m*-model. In advanced CMOS technology, the body effect coefficient (*m*) is a very important factor in short-channel-effect (SCE) control. It relates to the substrate doping profiles design, subthreshold slope and on/off current. Compared to the conventional body effect coefficient extraction method with its complicated variable substrate biases and fitting process, equation (2.8) provides a very fast and direct method to extract the body effect coefficient once the V_{TH} of normal and DT-modes is known. Further, equation (2.8) also provides a clear rule for designing the V_{TH} of DTMOS in deep-submicron device with a nonuniform doping profile. Unlike that of conventional devices, the body effect coefficient of DTMOS may be higher, with low gate work function material, for a high performance with low power consumption application.

2.3.1.2 MODELING VALIDATION

Figure 2.2 shows the I_D-V_G and G_m characteristics of NMOS under normal and DT-modes, respectively. It is obvious that the driving current of the DTMOS can be greatly enhanced by its lower threshold voltage and higher mobility resulting from the body effect. Unlike the conventional method as shown in Fig. 2.1, the V_{TH} of DTMOS is directly extracted by the linearly extrapolated threshold voltage of the maximum transconductance method. Figure 2.3 and Fig. 2.4 show comparisons of the V_{TH} extraction results of the conventional method and the $G_{m,max}$ extraction method for long channel and short channel devices, respectively. For both long channel (1μm) and short channel devices (0.16μm), the maximum errors are below 2.5% for different alpha ratios of devices under DT mode. Furthermore, from Fig. 2.5 to Fig. 2.8 show the extraction methods of the conventional method and the $G_{m,max}$ linearly extrapolated method for both Poly/SiO_2 and TaC/HfSiON devices with elevated temperature range from 298 K to 398 K, respectively. The gradual reduction in threshold voltage results from the increase in n_i with increasing measuring temperature. The maximum errors are lower than 1%, as shown in Fig. 2.9 and Fig. 2.10, in both Poly/SiO_2 and TaC/HfSiON gate stacks, confirming the good agreement between our method and the experimental data, respectively. Furthermore, the predicted values of the $V_{TH,DT}$ of the *m*-model and the experimental date extracted from the complicated variable substrate bias with fitting process are both shown in Fig.

2.11 and Fig. 2.12, respectively. For both long channel (1μm) and short channel devices (0.16μm), the maximum errors are less than 2% for different alpha ratios of devices under DT mode. It shows that our method can be still useful in short channel device. In addition, Fig. 2.13 and Fig. 2.14 shows the extraction results of the threshold voltage over the temperature range of 298 to 398K for the three methods under DT mode. The maximum errors are lower than 2% in both Poly/SiO_2 and TaC/HfSiON gate stacks, confirming the good agreement between our model and the experimental data, respectively. Furthermore, Fig. 2.15 details our *m*-model with using equivalent circuit for both normal and DT-modes, respectively. It demonstrates the surface potential can be controlled simultaneously under DT mode. The predicted values of the body effect coefficient of the *m*-model and the experimental date extracted from the complicated variable substrate bias with fitting process are both shown in Fig. 2.16. It includes the two different kinds of gate stack and bulk doping concentration with elevated temperatures range from 298 to 398K. The gradual increase in body effect coefficient results from the increase in n_i with increasing measuring temperature. Estimations of the disagreement between the *m*-model and the conventional method, roughly 2.5%, are obtained. These results show that our proposed *m*-model gives results that are sufficiently accurate to predict the V_{TH} and *m* of DTMOS.

2.3.2 Comparison with Performance and Short Channel Effect (SCE) for Different Gate Stacks between Normal and DT-modes

2.3.2.1 DTMOS Channel Surface Potential Control Modeling

As we mentioned before, the gate terminal connects to the substrate terminal while operating in DT mode. The threshold voltage of DTMOS is dynamical variation due to its body effect ($V_{BS}=\alpha V_G$). As a result, the theoretical threshold voltage for uniformly doped substrate with considering the body effect can be expressed as:

$$V_{TH,DT} = V_{FB} + 2\phi_{FP} + \frac{\sqrt{2\varepsilon_{Si} q N_a (2\phi_{FP} - \alpha V_G)}}{C_{OX}} \qquad (2.9)$$

As V_{FB} is the flat band voltage, ϕ_{fp} is the potential difference between Fermi level (E_F) and intrinsic Fermi level (E_{Fi}) of the silicon bulk, C_{ox} is the gate oxide capacitance and

N_a is the uniform substrate doping concentration. Fig. 2.17 shows the capacitance versus (V_G-V_{FB}) for three different poly, TaC and TiN gate stack, respectively. The effective oxide thickness among three different gate stacks is 25A, 17A and 18A, respectively. The gate depletion effect of poly gate stack about 4A can be calculated by the difference value of capacitance between inversion and accumulation region. Obviously, metal gate can resolve the of problem poly gate depletion effect for maintaining lower effective oxide thickness. The extraction results of substrate doping concentration for poly, TaC and TiN gate stacks are shown in Fig. 2.18. The substrate doping concentrations are almost the same value, 3.5E17, 3E17 and 2E17 cm^{-3} is obtained for TiN, TaC and poly gate stacks, respectively. By considering the N_a, C_{ox} and Q_{ss} (-4x10^{12} cm^{-2}), the effective gate work function is 4.1 e.V., 4.3 e.V. and 4.37 e.V. and the V_{TH} equals 0.43V, 0.53V and 0.63V can be obtained for poly, TaC and TiN, respectively. Figure 2.19 and Fig. 2.20 show the short channel effect of poly gate for both NMOS and PMOS under normal and DT-modes, respectively. Furthermore, to resolve the poly gate depletion effect, from Fig. 2.21 to Fig. 2.24 show the short channel effect of TaC and TiN gate for both NMOS and PMOS under normal and DT-modes, respectively. The V_{TH} roll-off phenomenon for both NMOS and PMOS can be found due to the charge sharing effect from source/drain junction to depletion region. For detailing the improvement of short channel effect for DTMOS, we need to use the equivalent circuit for both normal and DT-modes, again. As we known that, in subthreshold operating region of DTMOS, the V_{BS} may lower the potential barrier height between source and channel, and then the potential of source terminal can be expressed as following:

$$\psi'_{Source} = \psi_{Source,initial} - \alpha V_{BS} \qquad (2.10)$$

$\psi_{Source,initial}$ is the initial potential of source terminal. In addition, the building potential between channel and source terminal in the thermal equilibrium, can be described as following:

$$\psi_{bi} = \psi_{Source,initial} - \psi_S \qquad (2.11)$$

ψ_S is the channel surface potential and ψ_{bi} is the intrinsic building potential between channel and source junction. It should be noted that, due to the charge sheet of channel doesn't form before gate voltage higher than threshold voltage, the channel

surface potential can be negligible due to no inversion charge formation. As a result, we can define the gate control ability (CA_{GATE}) to channel surface as shown in following expression:

$$CA_{Gate}\Big|_{Subthreshold} \equiv \frac{\partial \psi_S}{\partial V_G} + \left(- \frac{\psi'_{Source}}{\partial V_G} \right) \tag{2.12}$$

In addition, due to the potential conservation, we can write the following relationship:

$$V_G - V_B - V_{FB} = \psi_S + \frac{\sqrt{2\varepsilon_{Si} q N_a \psi_S}}{C_{ox}} \tag{2.13}$$

Due to the $V_{BS}=\alpha V_G$ under DT-mode, the equation (2.13) can be rewritten as:

$$V_G - \alpha V_G - V_{FB} = \psi_S + \frac{\sqrt{2\varepsilon_{Si} q N_a \psi_S}}{C_{ox}} \tag{2.14}$$

Then by differentiation equation (2.14) with respect to V_G yields:

$$\frac{\partial \psi_S}{\partial V_G} + \frac{\partial \psi_S}{\partial V_G} \frac{\sqrt{\frac{\varepsilon_{Si} q N_a}{2\psi_S}}}{C_{ox}} = 1 - \alpha \tag{2.15}$$

Furthermore, by applying the depletion capacitance (C_d) concept to the equation, the relative change between ψ_S and V_G can be rewritten as:

$$\frac{\partial \psi_S}{\partial V_G} = \frac{(1-\alpha)}{\left(1 + \frac{C_d}{C_{ox}}\right)} \tag{2.16}$$

Relatively, the relative change of ψ'_{Source} and V_G can also be expressed as following:

$$- \frac{\partial \psi'_{Source}}{\partial V_G} = \frac{\partial \left(\psi'_{Source,initial} - \alpha V_G \right)}{\partial V_G} = \alpha \tag{2.17}$$

With substitute equation (5) and (5) into equation (5), the gate control ability (CA_{GATE}) to channel surface for DTMOS is shown as following formulation:

$$CA_{Gate}\big|_{Subthreshold} \equiv \frac{\partial \psi_S}{\partial V_G} + \left(-\frac{\psi'_{Source}}{\partial V_G} \right) = \frac{\left(1+\alpha \frac{C_d}{C_{ox}}\right)}{\left(1+\frac{C_d}{C_{ox}}\right)} = \frac{(1+\alpha\delta)}{(1+\delta)} \tag{2.18}$$

where

$$\delta = -\frac{dV_T}{dV_{BS}} = \frac{1}{C_{ox}} \sqrt{\frac{q\varepsilon_{Si} N_a}{2(2\phi_{fp} - V_{BS})}} \tag{2.19}$$

Comparing to normal mode, while $\alpha = 0$, the DT mode show its higher channel surface potential control ability with higher α ratios. We explain that why the DTMOS has lower V_{TH} roll-off effect with three different gate stack system for NMOS and PMOS, respectively. The experimental results of short channel effect are both shown in Fig. 2.25 to Fig. 2.26, respectively. Ideally, once α equals 1, the gate control ability would not be affected by body effect anymore, and it always equals 1 perfectly. However, in reality, there are some non-ideal factors, such as substrate parasitic resistance ($R_{parasitic}$) [2.16], and then the gate control ability wouldn't equal 1. Fortunately, the DT mode still improves much better than normal mode. In addition, the metal gate of TaC and TiN show the higher gate control ability result from with no poly gate depletion effect.

Furthermore, when the device continues scaled-down to sub-micron process, the source and drain junction would play an important role for capacitance coupling effect to channel, especially for short channel device. The electric field penetrates from larger drain voltage terminal would lower the potential barrier of channel which results a threshold voltage decrease and larger off-leakage, named DIBL effect [2.17-2-18]. The relationship between threshold voltage variation and device physical parameters can be expressed as [2.19]:

$$\Delta V_{TH} \propto V_D e^{\frac{-L}{l}} \tag{2.20}$$

where

$$l \propto T_{ox}^{\frac{1}{3}} W_{d,\max}^{\frac{1}{3}} X_j^{\frac{1}{3}} \tag{2.21}$$

T_{ox} is the gate oxide capacitance, $W_{d,max}$ is the maximum depletion width and is the X_j

source/drain junction depth. Obviously, the decrease value of all of the physical parameter can effectively decrease the DIBL effect. Fig. 2.27 and Fig. 2.28 show the DIBL characteristics of poly, TaC and TiN gate stacks for NMOS and PMOS, respectively. Due to the increase the effective oxide thickness of poly depletion, the poly gate stack shows the larger degradation of threshold voltage. On the other hand, the DIBL effect can be improved by DT-mode operation for all gate stacks result from its lower effective drain voltage and smaller maximum depletion width. It again proves the DTMOS has better gate control ability. Especially for short channel device, the DIBL effect would also increase the subthreshold swing degradation inducing high subthreshold leakage current ($I_{D,Subthreshold}$) as expressed:

$$I_{D,Subthreshold} \propto e^{\frac{q(\psi_s)}{KT}} \tag{2.22}$$

while the corresponding drain current named subthreshold current, due to the drain current is dominated by diffusion current in weak inversion. Furthermore, according to the initial definition of subthreshold swing, the subthreshold swing under DT-mode without considering DIBL effect can be expressed as:

$$I_{D,Subthreshold} \propto e^{\frac{q(\psi'_s)}{KT}} \tag{2.23}$$

where ψ'_s is the modulation surface potential under DT mode, and then:

$$S.S. \equiv \left(\frac{\partial \log I_{D,Subthreshold}}{\partial V_G}\right)^{-1} = \ln 10 \frac{kT}{q}\left(\frac{\partial \psi'_s}{\partial V_G}\right)^{-1} = 2.3\frac{kT}{q}\frac{(1+\delta)}{(1+\alpha\delta)} \tag{2.24}$$

The mathematical expressions show the higher alpha ratios can improve the subthreshold swing, ideally for α=1, the subthreshold swing can be only affected by the temperature factor with almost perfect swing. Figure 2.29 and Fig. 2.30 show the subthreshold characteristics of poly, TaC and TiN gate stacks for NMOS and PMOS at 223 K, respectively. The very excellent subthreshold swings are obtained under DT-modes which prove the quite high potential for applying in low stand-by power circuit.

Figure 2.31 shows the I_{cp} characteristics of poly, TaC and TiN gate stacks, respectively. The interface state of TiN gate is higher than the others. Furthermore, the effectively mobility extracted from split C-V among three different gate stacks are

also shown in Fig. 2.32. Due to the interaction between poly gate and gate dielectric, the additional defects and dipoles creation result in effective mobility of poly gate is obvious lower than the others. Figure 2.33 shows the capacitance versus gate voltage measured from split C-V under normal, fixed-body and DT-modes, respectively. It can be found that capacitance characteristic under DT mode is dynamical variation. In addition, Fig. 2.34 shows the effective mobility characteristics versus surface charge density of poly, TaC and TiN gate stacks under normal and DT-modes, respectively. The effective mobility of DT mode largely enhances than normal mode due to its lower normal electric field with higher charge screen effect for the larger inversion charges. The reason for lower normal electric field is attributed to the decrease of maximum depletion width. Furthermore, the Fig. 2.35 shows the injection velocity from source terminal as extracted from elementary scattering theory and temperature version of backscattering model [2.20-2.22]:

$$I_{D,Sat} = C_{ox} W V_{inj} B_{Sat} (V_G - V_{TH}) \tag{2.25}$$

Where V_{inj} is the injection velocity of carrier from source terminal and B_{Sat} is the ballistic coefficient. Where:

$$B = \left(\frac{1 - r_c}{1 + r_c} \right) \tag{2.26}$$

$$r_c = \frac{1}{1 + \frac{\lambda_0}{l_0}} \tag{2.27}$$

$$\frac{\lambda_0}{l_0} = \frac{4}{0.5 - \left(\sigma + \frac{\eta}{(V_G - V_{G,Sat})} \right) 298K} - 2 \tag{2.28}$$

$$\sigma = \frac{(I_{D,Sat1} - I_{D,Sat2})}{I_{D,Sat2}(T_1 - T_2)} \tag{2.29}$$

$$\eta = \frac{(V_{T,Sat1} - V_{T,Sat2})}{T_1 - T_2} \tag{2.30}$$

The results show the injection velocity versus forward body bias characteristics of poly, TaC and TiN gate stacks, respectively. Due to the reasons that injection velocity main affects by the DIBL effect and mobility, the TiN gate has better injection

velocity than poly gate for its high mobility for short channel device. Furthermore, while increasing the forward source-body bias, the injection velocity can also be improved by its higher injection mobility for decrease of depletion charge effect. In addition, the 65nm TiN gate device also shows its higher injection velocity than 85nm TiN gate device with lower ballistic coefficient for higher interface state, as shown in Fig. 2.36. Due to the higher barrier lowering effect at source across to channel in poly gate, the TiN gate shows lower ballistic transport coefficient than poly gate. However, the ballistic coefficient would also decrease as increasing forward body bias for reducing DIBL effect, simultaneously. Eventually, Fig. 2.38, Fig. 2.39 and Fig.2.40 show the on/off characteristics for poly, TaC and TiN gate stacks under both normal and DT-modes, respectively. Obviously, DTMOS may maintain the low off-leakage with accomplishing large enhancement of on current for low power device application.

2.4 Summary

In the chapter 2, analytical expressions with physical insights of *m*-model of DTMOS transistor are successfully presented in detail. The maximum errors lower than 2% and 2.6% in the threshold voltage (V_{TH}) and body effect coefficient (m) extraction at elevated temperature over 298 K to 398 K, respectively, confirms the good agreement between our *m*-model and experimental data. The proposed physical formulations are very useful for future deep-submicron integrated circuit design using DT technology. In addition, we also show the short channel effect improvement and high performance with low power consumption characteristics of DTMOS in this chapter. We give clear and simple physical insights to prove the advantages of DTMOS. Finally, we give a comparison table of physical parameters between DTMOS and MOSFET, as shown in Table. 2.1.

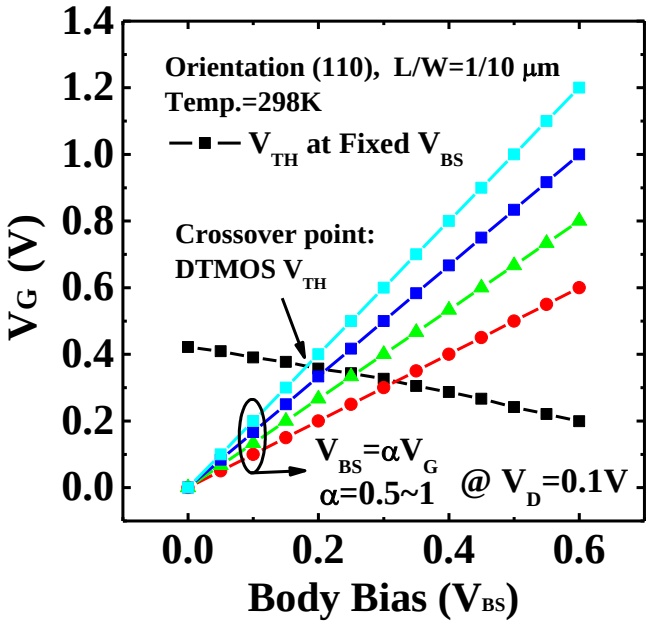


Fig. 2.1 Body bias dependence of the threshold voltage at 298K. The straight lines demonstrate that the body bias varies dynamically with the body bias. The crossover points show that the V_{TH} of DTMOS with the different alpha ration from 0.5 to 1.

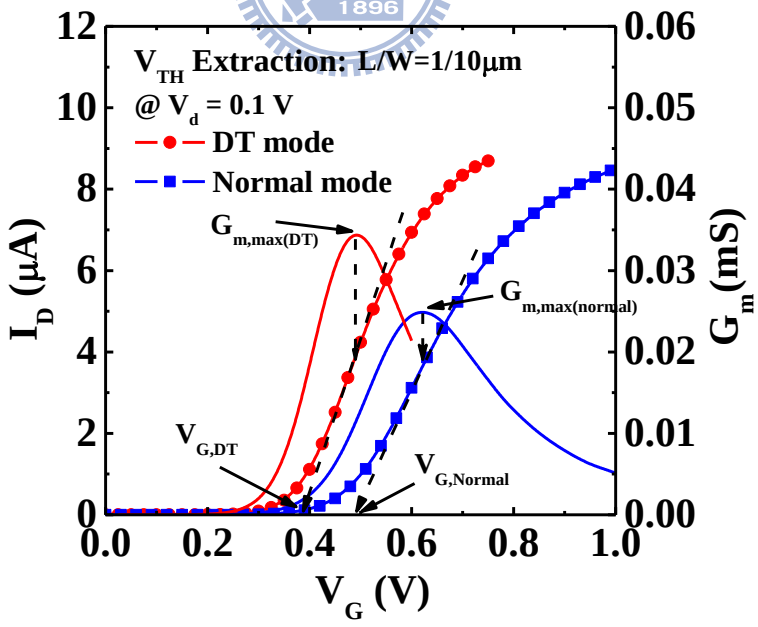


Fig. 2.2 Experimental I_D-V_G and G_m characteristics of both normal and DT-modes, respectively. The V_{TH} of both normal and DT-modes are extracted by linearly extrapolated of maximum transconductance method with low drain bias (50~100mV).

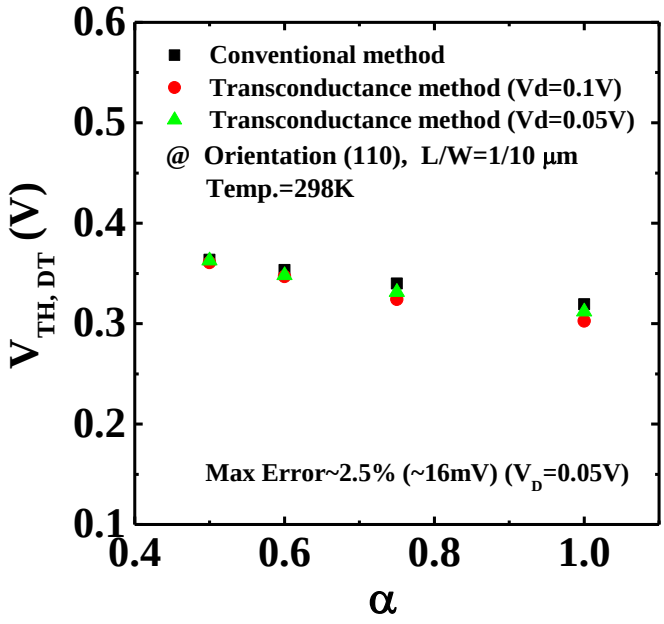


Fig. 2.3 The conventional method and maximum transconductance method experimental values of the V_{TH} of the DTMOS transistor with different alpha ration at long channel device. The channel length and width is 1 and 10 μm, respectively.

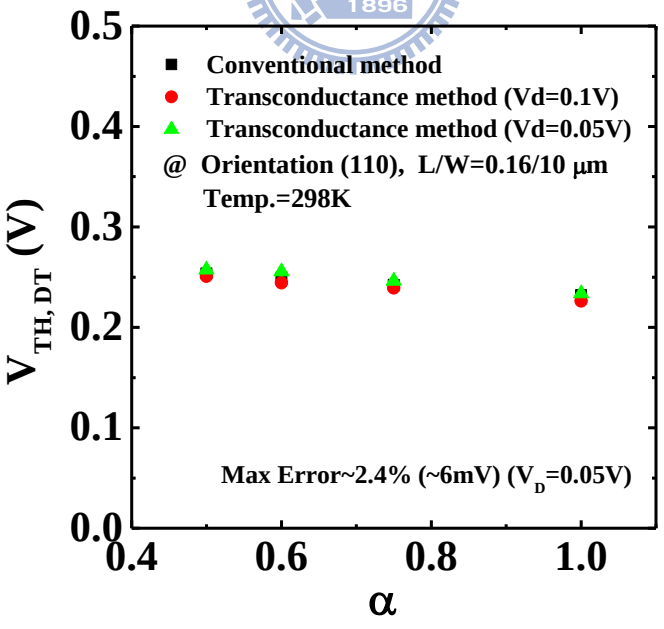


Fig. 2.4 The conventional method and maximum transconductance method experimental values of the V_{TH} of the DTMOS transistor with different alpha ration at short channel device. The channel length and width is 0.16 and 10 μm, respectively.

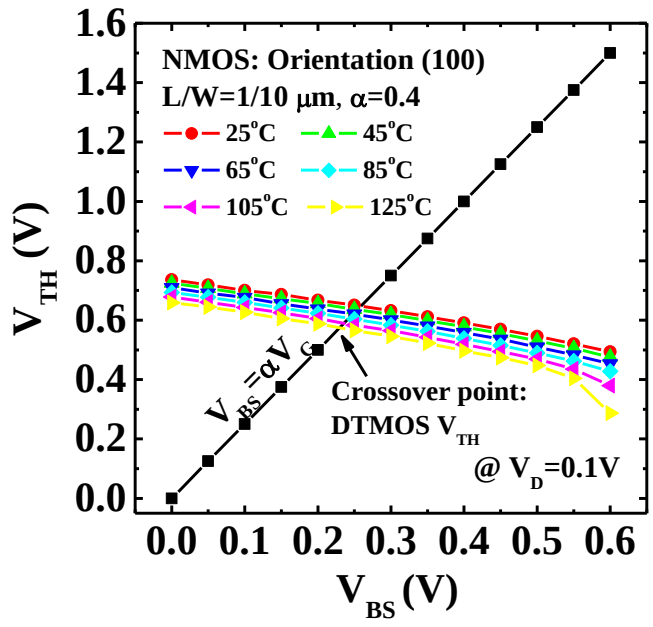


Fig. 2.5 Body bias dependence of the threshold voltage at elevated temperatures from 298K to 398K. The straight black line shows that the body bias varies dynamically with the gate bias. The crossover points show that the V_{TH} of Poly/SiO_2 DTMOS.

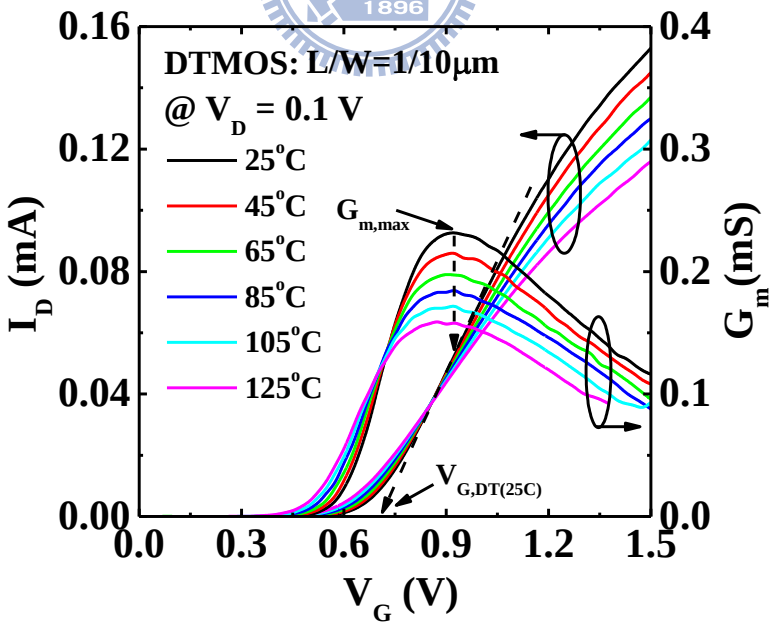


Fig. 2.6 Experimental Id-Vg and G_m characteristics of Poly/SiO_2 DTMOS in the linear region over a temperature range of 25℃ to 125℃. The V_{TH} of DTMOS is extracted by linearly extrapolated of maximum transconductance method.

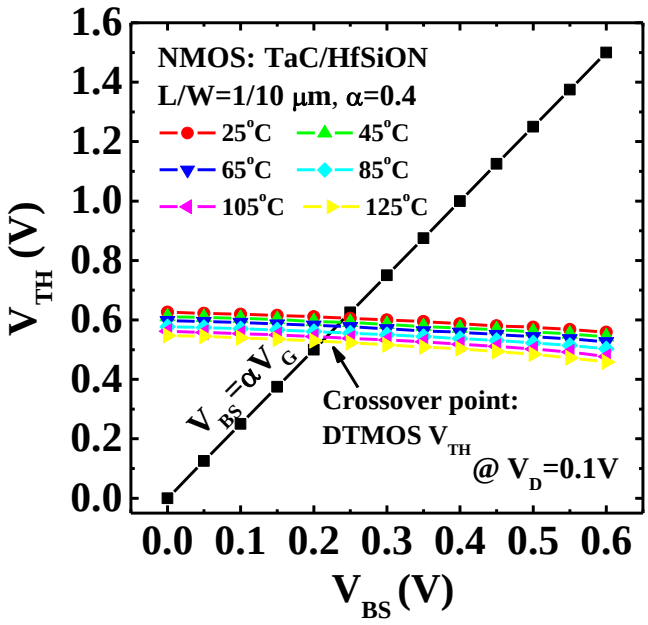


Fig. 2.7 Body bias dependence of the threshold voltage at elevated temperatures from 298K to 398K. The straight black line shows that the body bias varies dynamically with the gate bias. The crossover points show that the V_{TH} of TaC/HfSiON DTMOS.

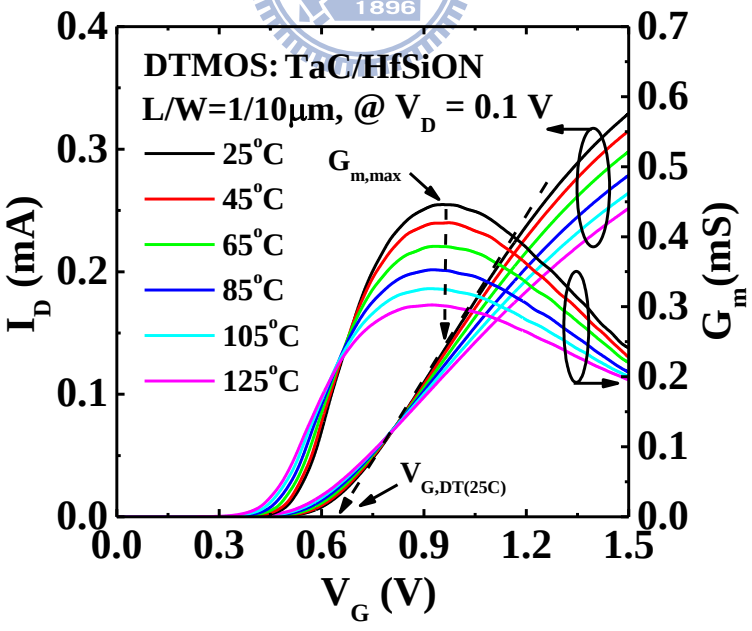


Fig. 2.8 Experimental Id-Vg and G_m characteristics of TaC/HfSiON DTMOS in the linear region over a temperature range of 25℃ to 125℃. The V_{TH} of DTMOS is extracted by linearly extrapolated of maximum transconductance method.

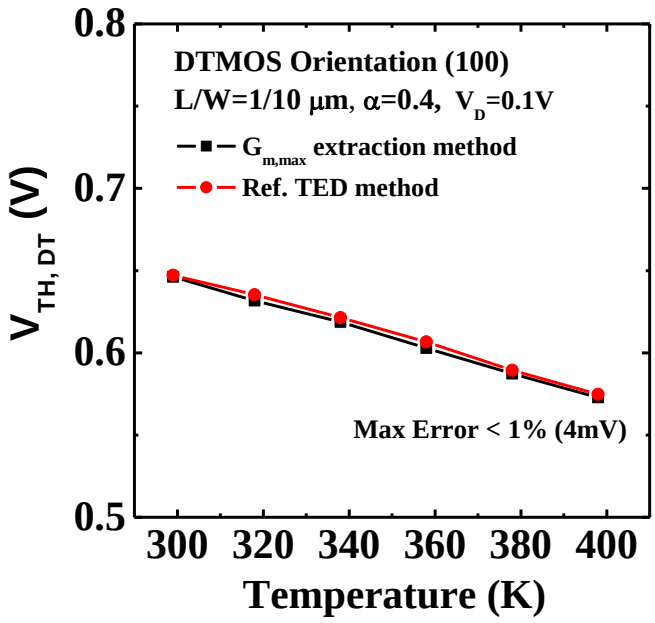


Fig. 2.9 The comparison results between conventional and maximum transconductance methods of the V_{TH} of the Poly/SiO_2 DTMOS transistor at elevated temperature.

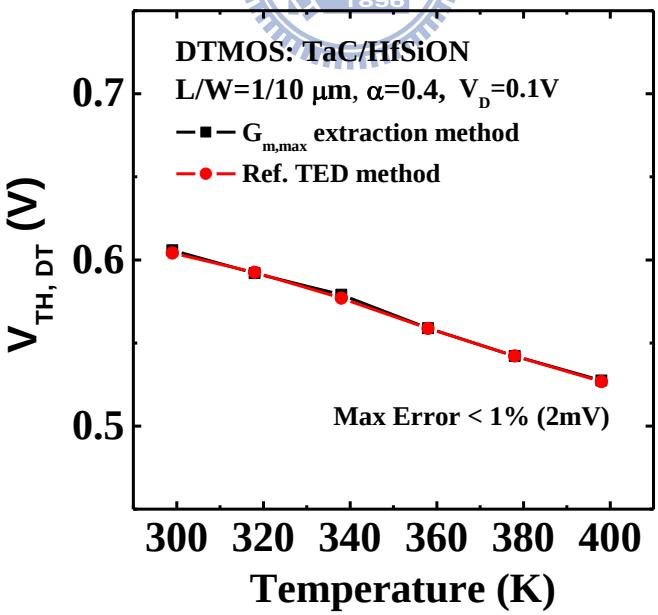


Fig. 2.10 The comparison results between conventional and maximum transconductance methods of the V_{TH} of the TaC/HfSiON DTMOS transistor at elevated temperature.

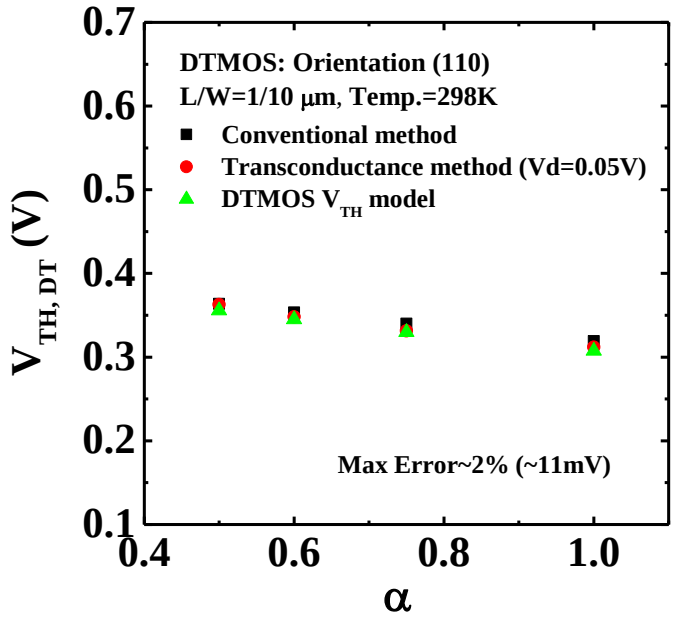


Fig. 2.11 Theoretical values and actual experimental data of the V_{TH} of the DTMOS transistor values with different alpha ration from 0.5 to 1 for long channel device.

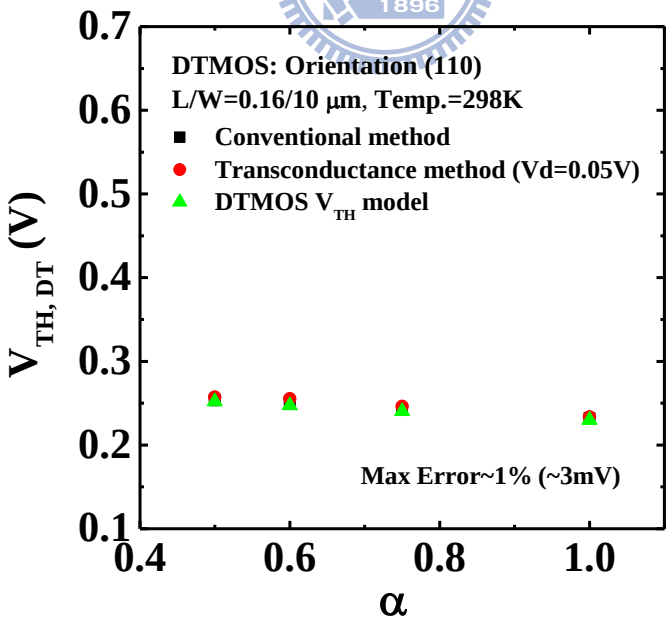


Fig. 2.12 Theoretical values and actual experimental data of the V_{TH} of the DTMOS transistor values with different alpha ration from 0.5 to 1 for short channel device.

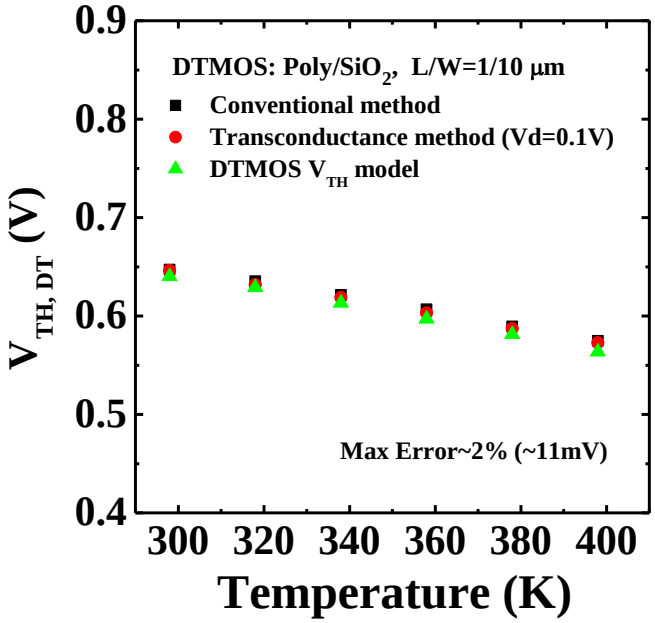


Fig. 2.13 Theoretical values and actual experimental data of the V_{TH} of the DTMOS transistor values at elevated temperature from 298 to 398 K for Poly/SiO_2 DTMOS.

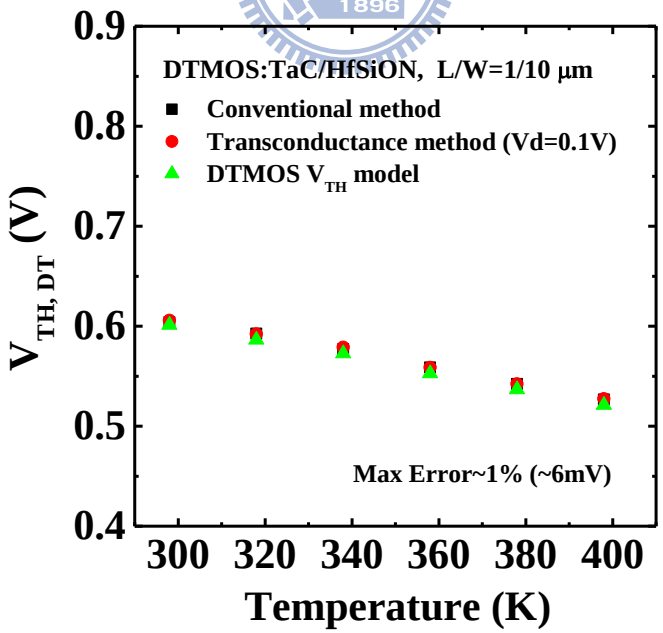


Fig. 2.14 Theoretical values and actual experimental data of the V_{TH} of the DTMOS transistor values at elevated temperature from 298 to 398 K for TaC/HfSiON DTMOS.

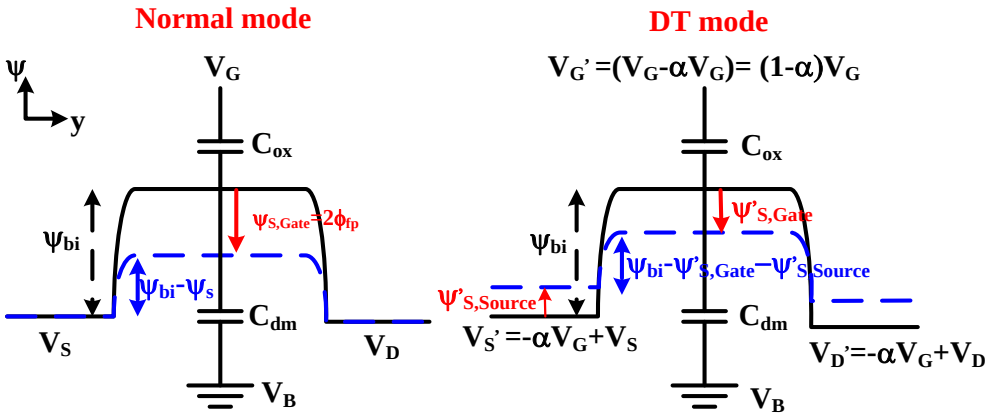


Fig. 2.15 Equivalent potential diagram and band diagram of our proposed *m*-model, including normal and DT-modes, respectively.

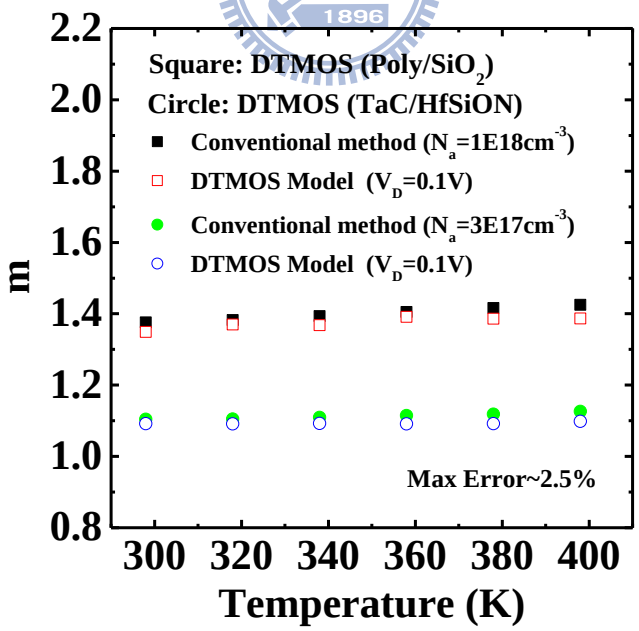


Fig. 2.16 Temperature dependence of the body bias coefficient at elevated temperatures from 298 to 398 K. Two different kinds of gate stack and body doping concentration are used to verify our proposed m-model.

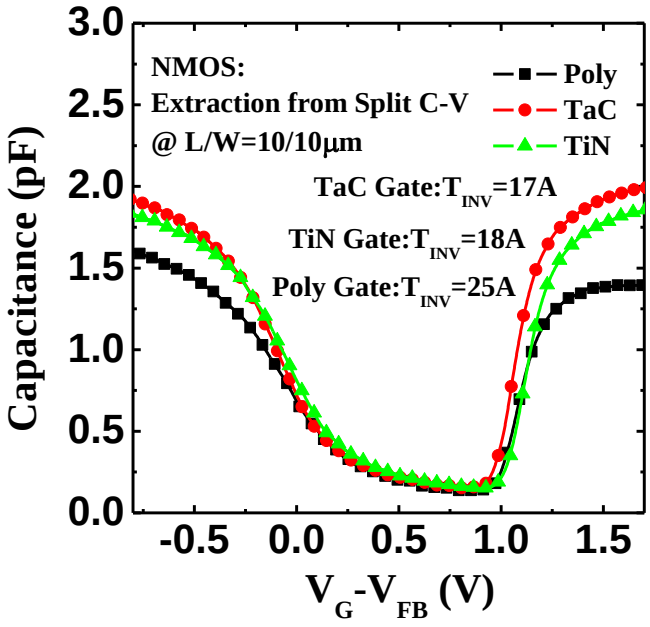


Fig. 2.17 Capacitance characteristics of poly, TaC and TiN gate NMOSFET, respectively.

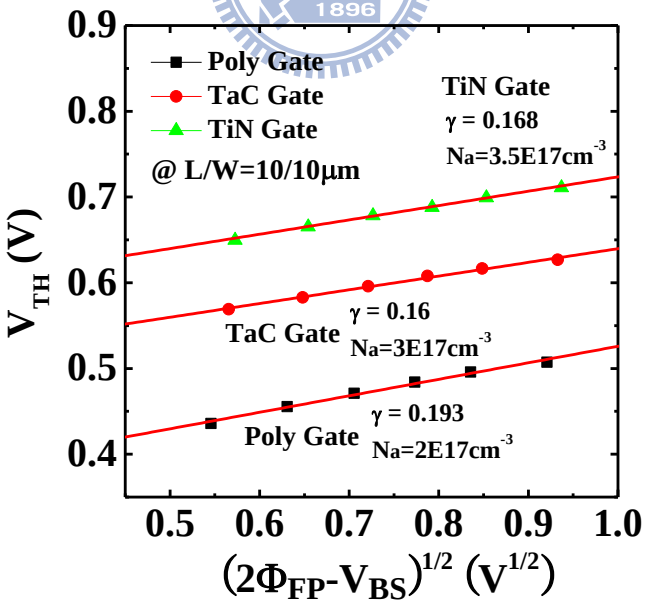


Fig. 2.18 Substrate doping concentration extraction of poly, TaC and TiN gate NMOSFET, respectively.

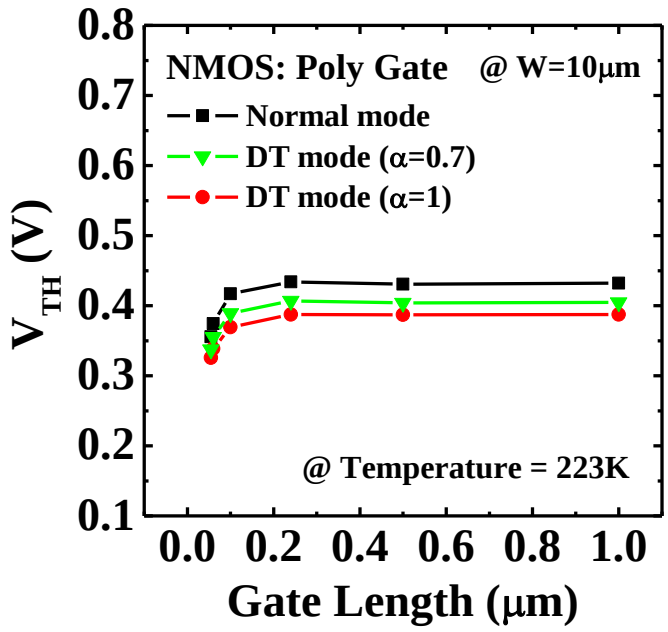


Fig. 2.19 Threshold voltage variation versus channel length between normal and DT-modes for poly gate NMOS.

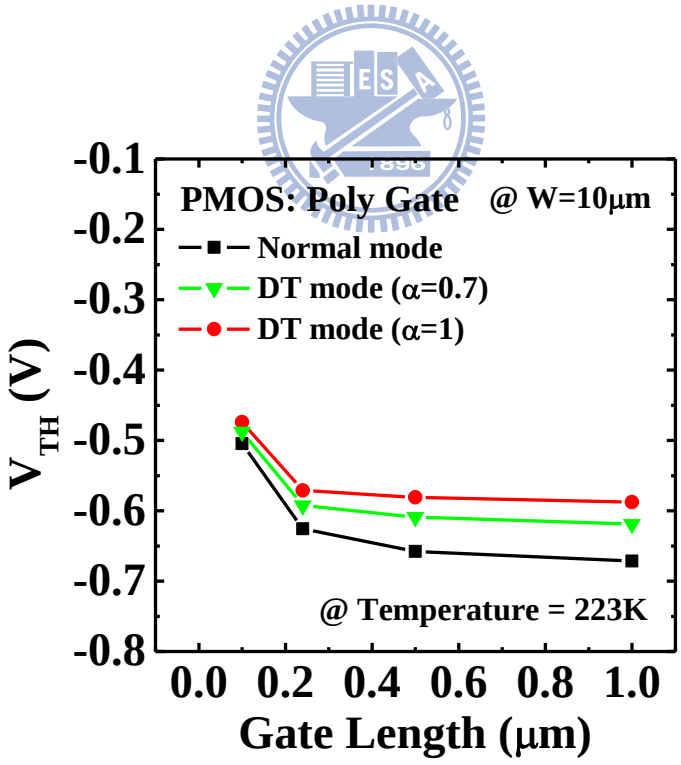


Fig. 2.20 Threshold voltage variation versus channel length between normal and DT-modes for poly gate PMOS.

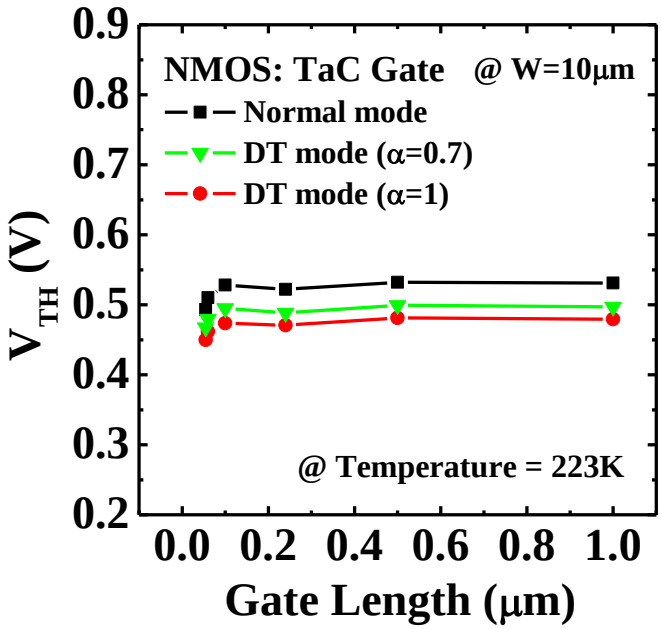


Fig. 2.21 Threshold voltage variation versus channel length between normal and DT-modes for TaC gate NMOS.

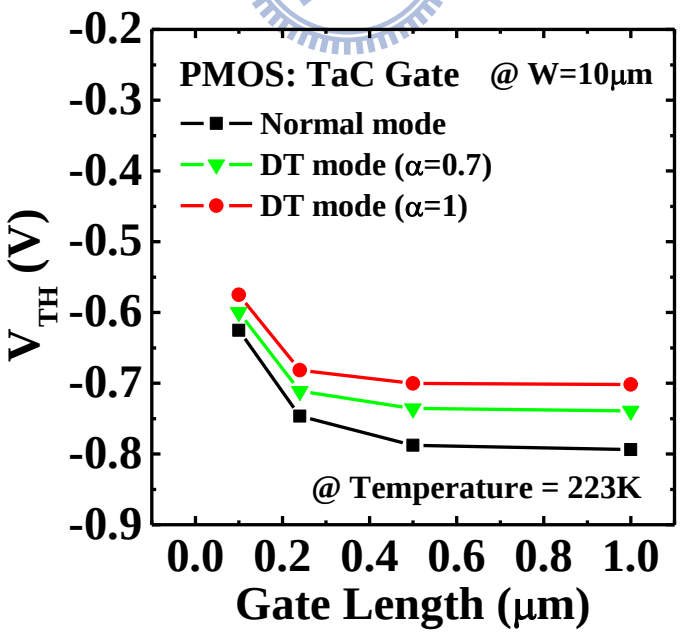


Fig. 2.22 Threshold voltage variation versus channel length between normal and DT-modes for TaC gate PMOS.

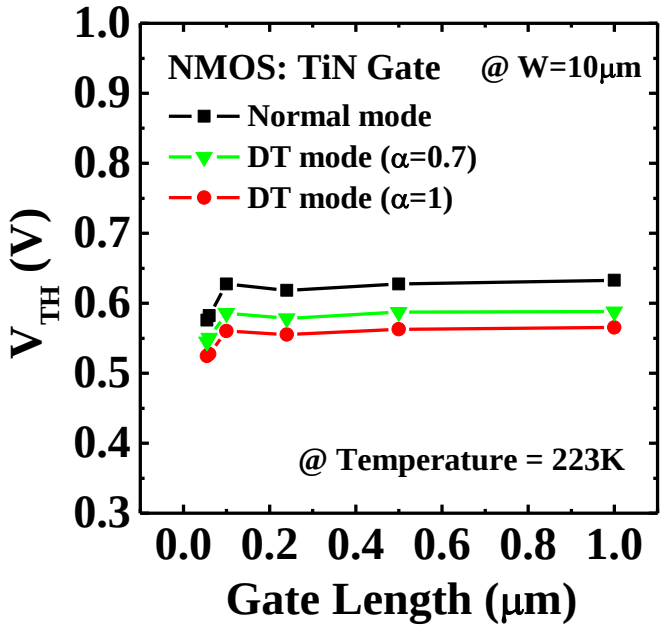


Fig. 2.23 Threshold voltage variation versus channel length between normal and DT-modes for TiN gate NMOS.

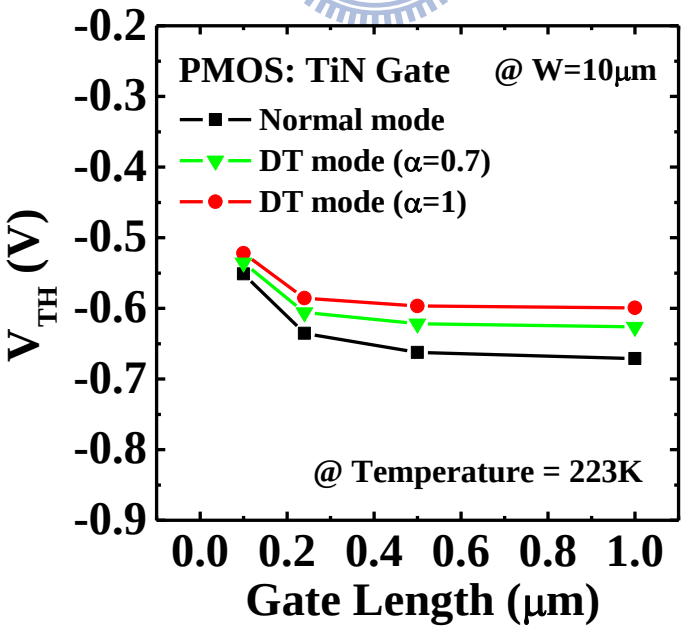


Fig. 2.24 Threshold voltage variation versus channel length between normal and DT-modes for TiN gate PMOS.

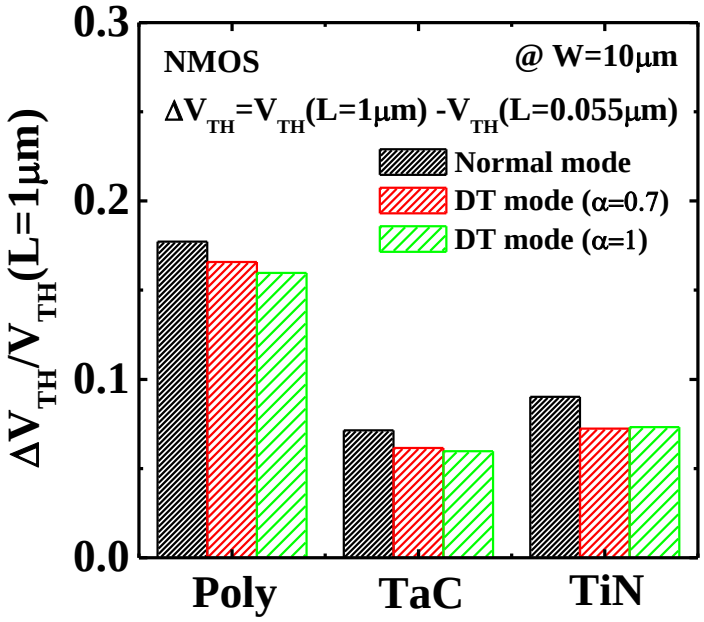


Fig. 2.25 Short channel effect between normal and DT-modes among poly, TaC and TiN gate NMOS.

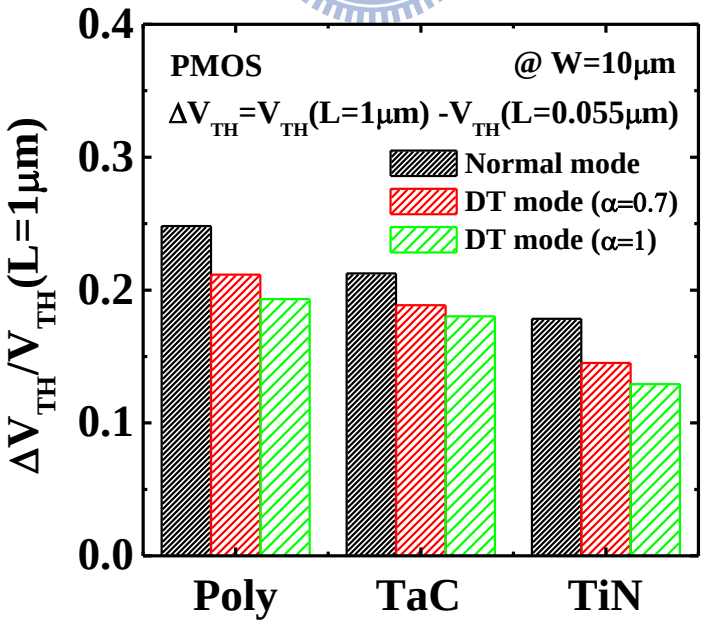


Fig. 2.26 Short channel effect between normal and DT-modes among poly, TaC and TiN gate PMOS.

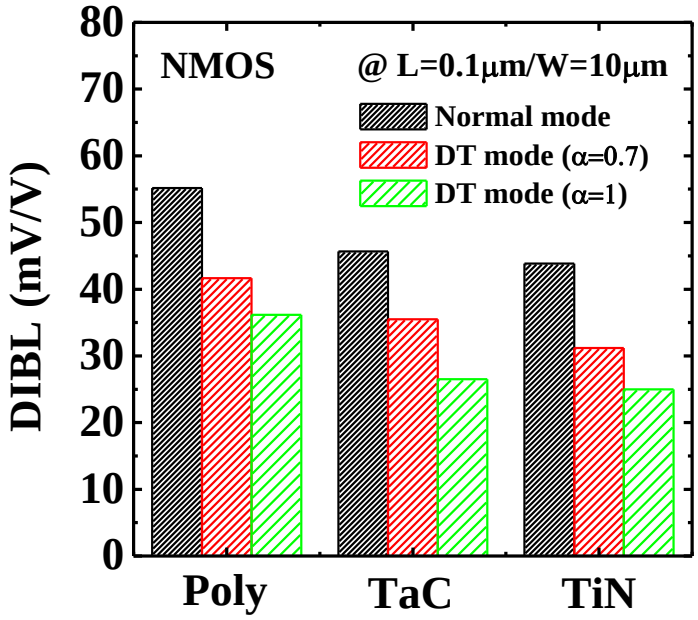


Fig. 2.27 DIBL effect between normal and DT-modes among poly, TaC and TiN gate NMOS.

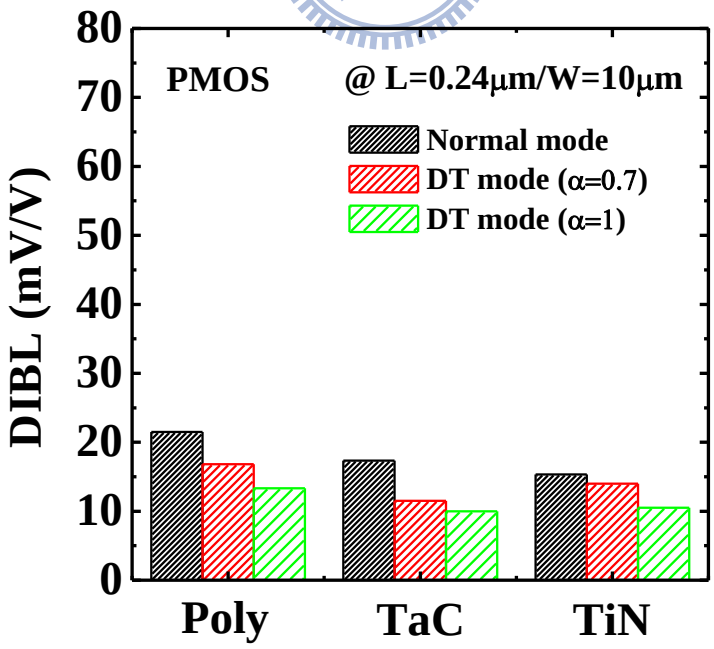


Fig. 2.28 DIBL effect between normal and DT-modes among poly, TaC and TiN gate PMOS.

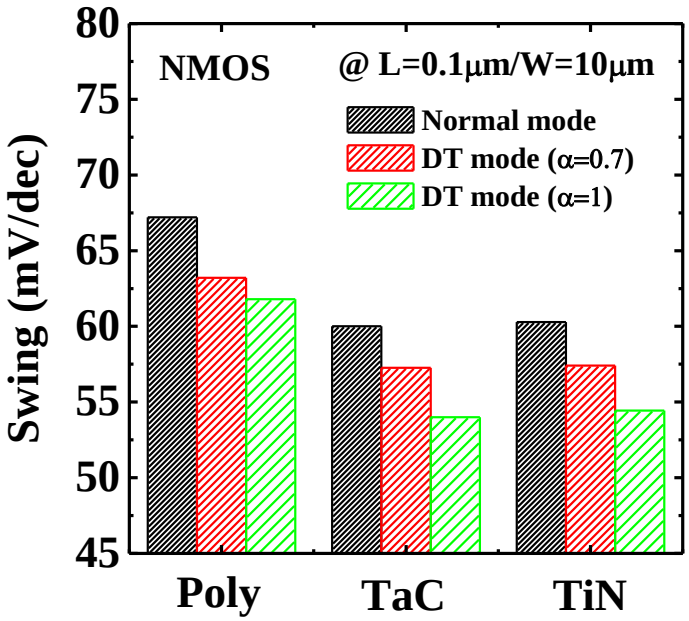


Fig. 2.29 Sub-threshold slope between normal and DT-modes among poly, TaC and TiN gate for NMOS.

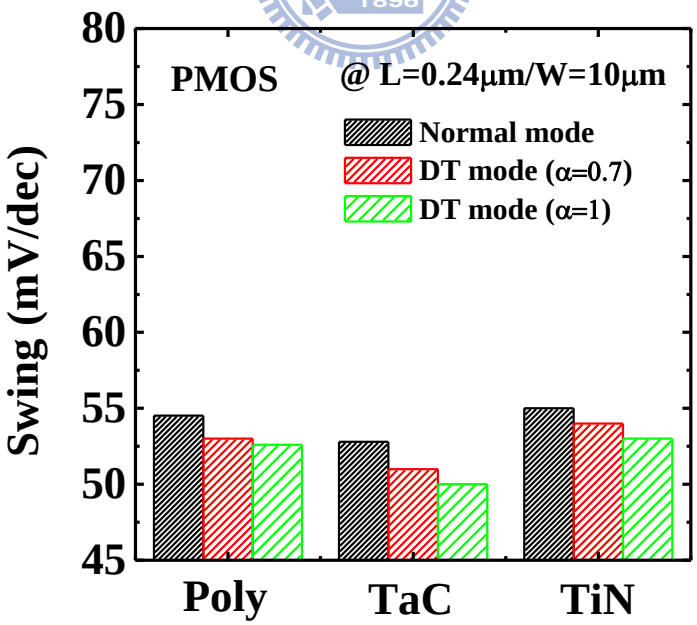


Fig. 2.30 Sub-threshold slope between normal and DT-modes among poly, TaC and TiN gate for PMOS.

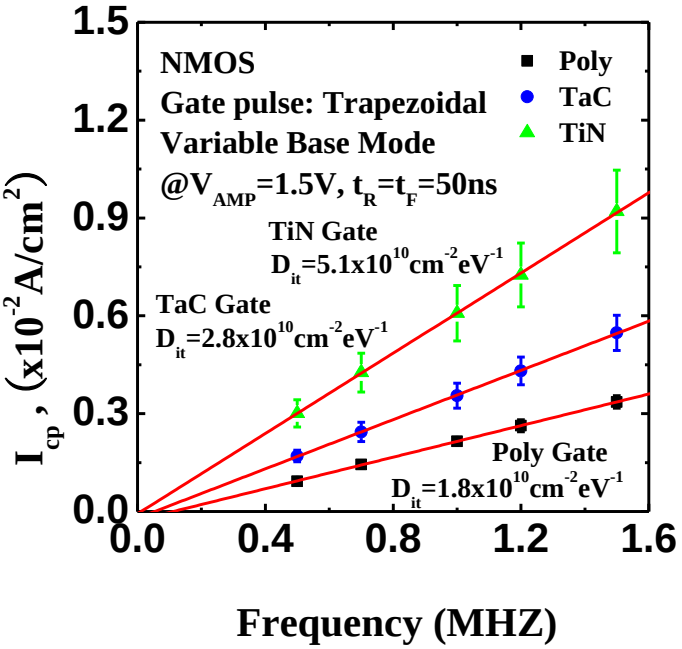


Fig. 2.31 Charge pumping characteristics of poly, TaC and TiN gate NMOSFET, respectively.

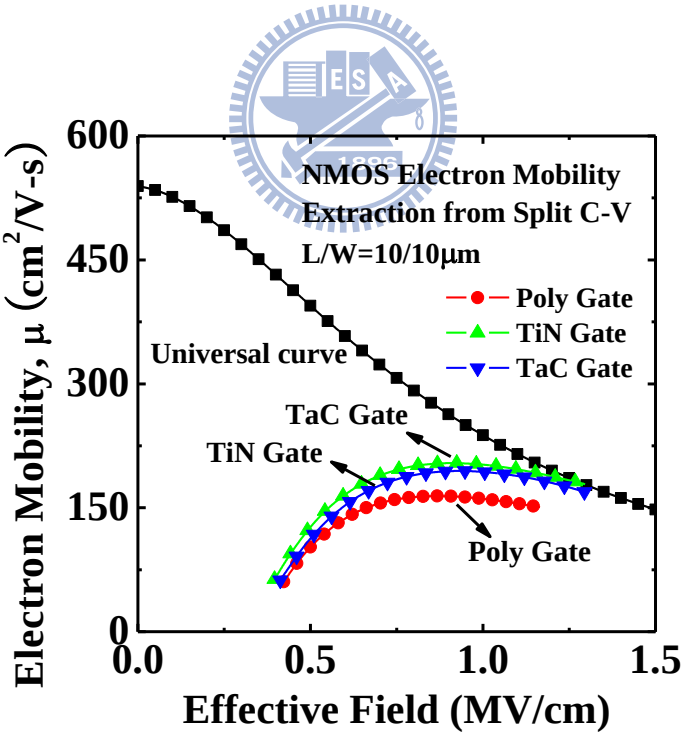


Fig. 2.32 Electron mobility characteristics of poly, TaC and TiN gate NMOSFET, respectively.

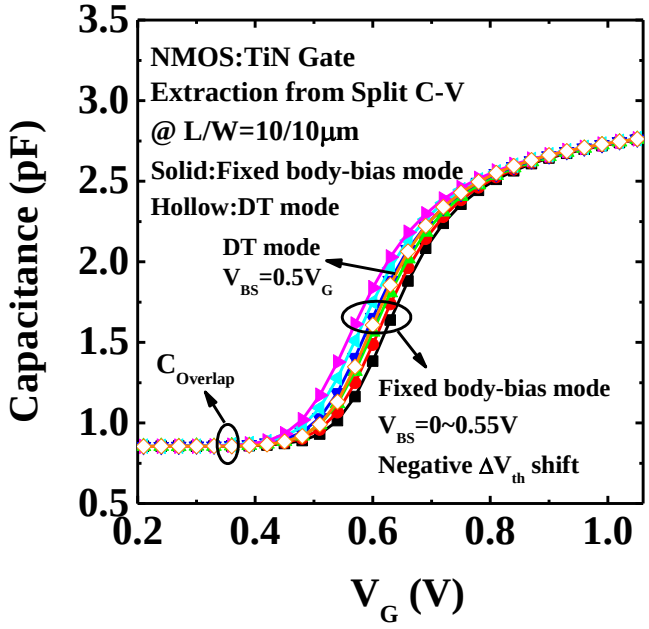


Fig. 2.33 Capacitance versus gate voltage characteristics with fixed body-bias and DT-modes for TiN gate NMOSFET, respectively.

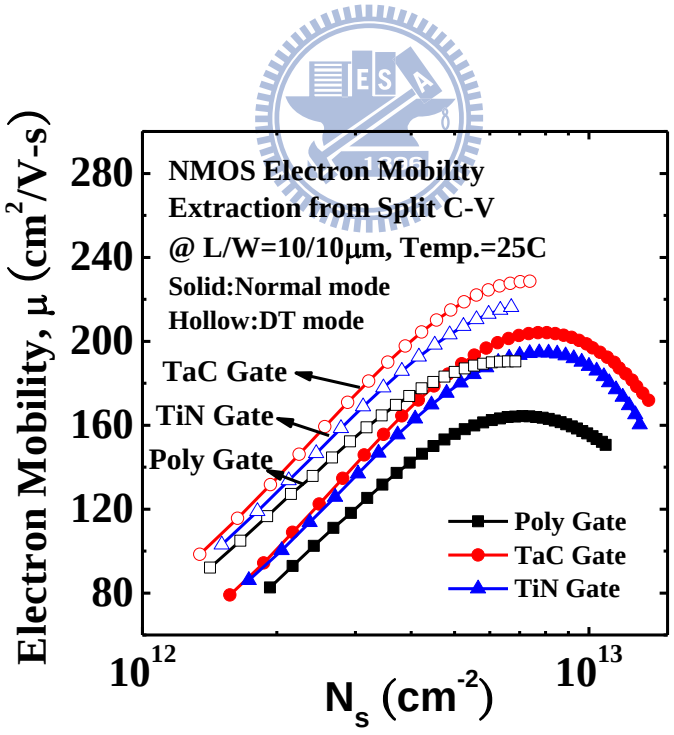


Fig. 2.34 Electrons mobility versus channel surface charge concentration characteristics between normal and DT-modes for three different gate NMOSFET.

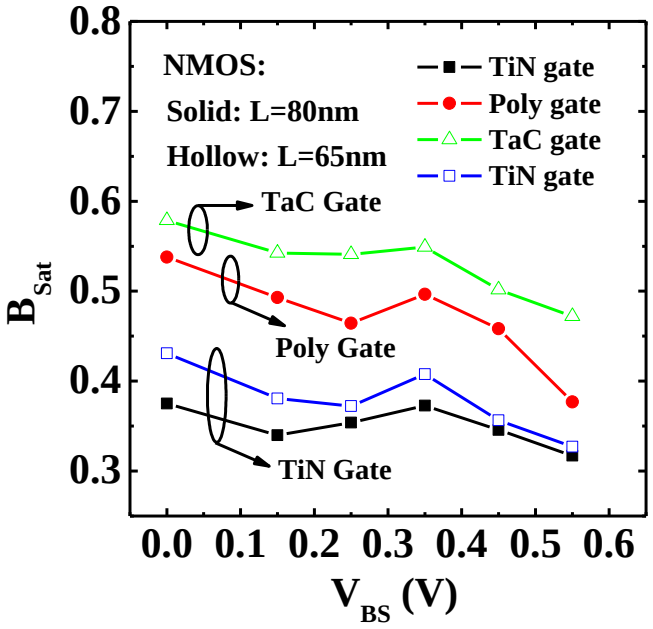


Fig. 2.35 Ballistic transport efficiency versus forward source-substrate bias characteristics for three different gates.

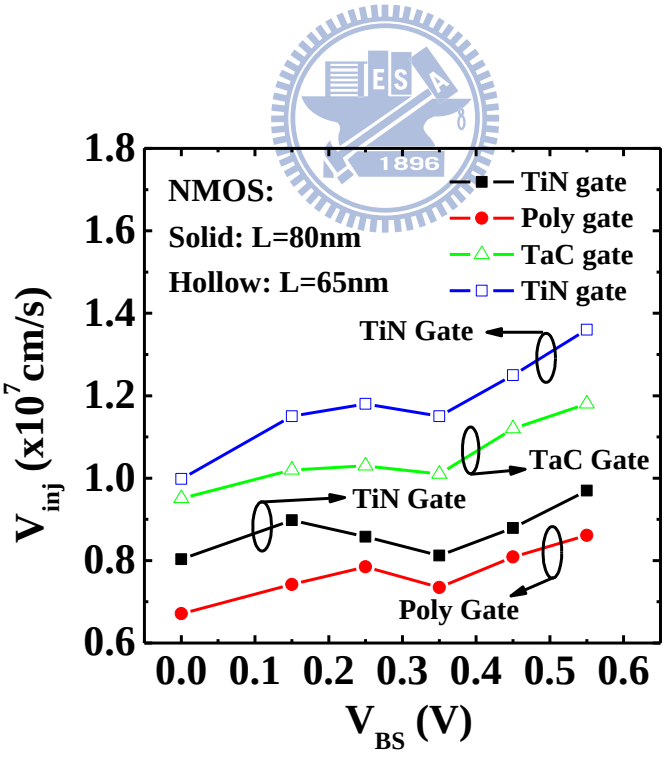


Fig. 2.36 Electron injection velocity versus forward source-substrate bias characteristics for three different gates.

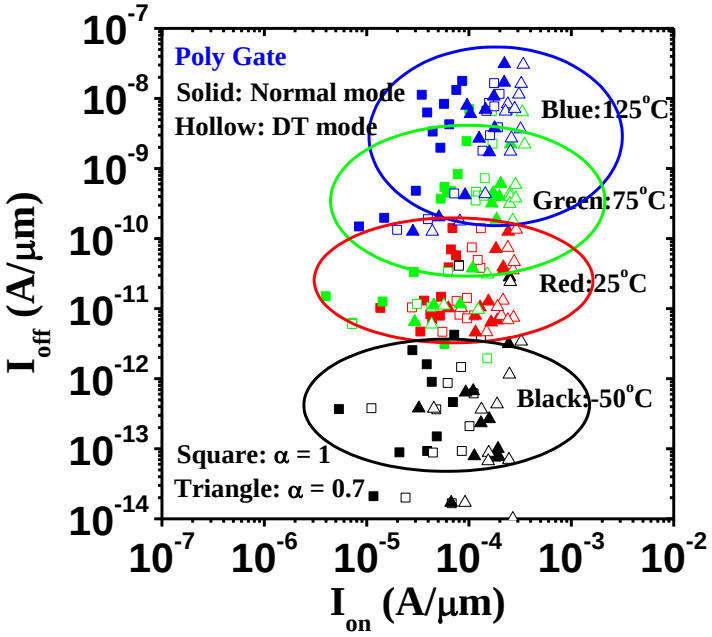


Fig. 2.37 On/off characteristics between normal and DT-modes for Poly gate.

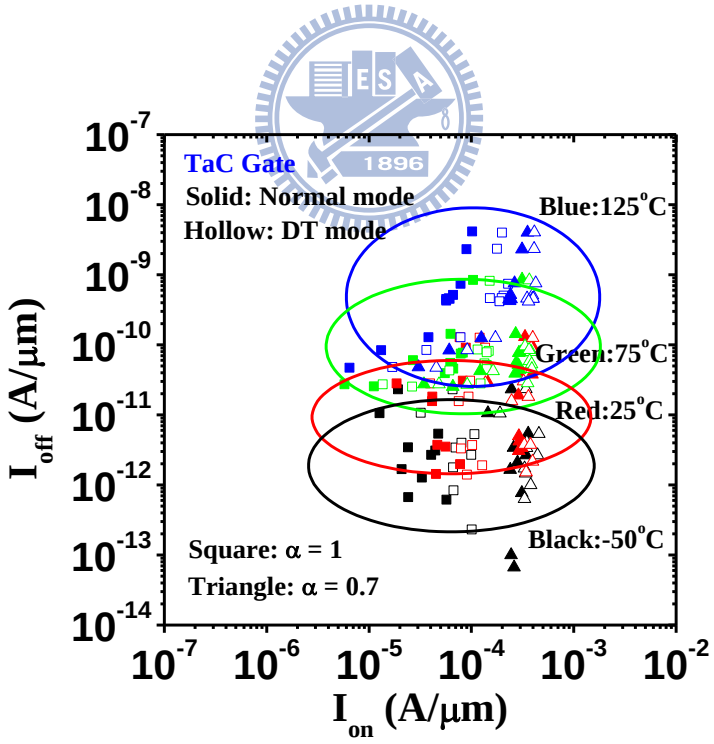


Fig. 2.38 On/off characteristics between normal and DT-modes for TaC gate.

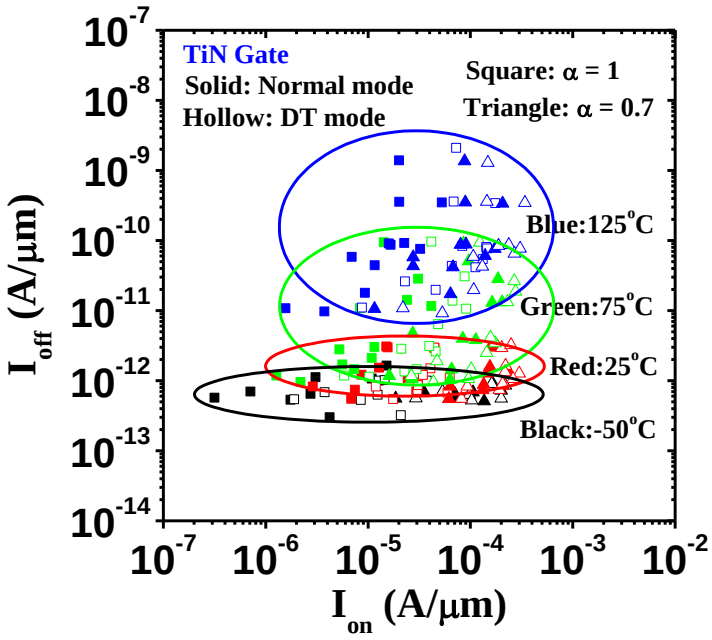


Fig. 2.39 On/off characteristics between normal and DT-modes for TiN gate.

Physical Parameters	V_{dd}	V_{TH}	C_{ox}	m	W_{dm}	N_a	u_{eff}
MOSFET	Normal	Normal	Normal	Normal	Normal	Normal	Normal
DTMOS	↓	↓	↑	↑	↓	↑	↑
Physical Parameters	$\Phi_{m,n}$	$\Phi_{m,p}$	ΔV_{TH}	DIBL	S.S.	I_{off}	I_{on}
MOSFET	Normal	Normal	Normal	Normal	Normal	Normal	Normal
DTMOS	↓	↓	↓	↓	↓	↓	↑

Table. 2.1 Comparison table of physical factors and electrical characteristics between MOSFET and DTMOS.

Chapter 3

High-Performance and High-Reliability Dynamic Threshold Source Side Injection (DTSSI) for 2-Bit/Cell with MLC Operation of Wrapped-Select-Gate SONOS (WSG-SONOS) in NOR-Type

3.1 Introduction

The floating-gate structure of traditional EEPROM devices has encountered a number of challenges as device sizes continue to shrink in scale. These include serious short-channel-effects [3.1], data retention degradation resulting from the stress-induced leakage current [3.2], and obvious gate injection and critical coupling effects [3.3] between the neighboring floating-gates (FG) in NOR and NAND type architectures. Among these factors, maintaining a tunneling oxide thickness of at least 8 nm in a very short channel device without simultaneous reliability degradation limits the process flexibility of FG devices, especially for the development of high performance FG device fabrication procedures [3.4].

The silicon-oxide-nitride-oxide-silicon (SONOS) memory device has become one of the most popular candidates for replacement of conventional FG memory when shrinking the tunneling-oxide thickness to 5 nm [3.5-3.6]. This is due to property of the material, which causes local trapping of silicon nitride, in turn helping the discrete electrons stored in the deep trap sites to resist tunneling-out processes through the tunneling-oxide.

The density of flash memory devices can be doubled without increasing the die size, a phenomenon known as 2-bit/cell operation [3.7-3.8], under separated storage characteristics. This has been achieved by the well-known Channel Hot-Electrons Injection (CHEI) method for programming each side of a cell. The bit-1 and bit-2 can then be read-out using the highly reliable reverse-read scheme [3.9].

Similar to 2-bit/cell operation, multi-level states in a cell (MLC) is another attractive approach for achieving high-density application in a flash memory device [3.10-3.11]. MLC operation entails construction of different levels of charge in the nitride trapping layer of a SONOS device. The different combination of charge states is then identified using a highly reliable method for distinguishing between each level of charge. However, owing to the larger sensor margin requirements required to precisely distinguish different charge levels, CHEI with lower programming

efficiency is not suitable for MLC operations due to its relatively high power consumption. However, the power-saving Source-Side-Injection (SSI) method, first published in 1986, has demonstrated high-performance with low operating voltages in EPROM [3.12-3.14]. Unlike the channel-hot-electron injection (CHEI), the major advantages of SSI injection are high-speed programming and high programming efficiency, due to its clever separation of the incompatibilities of optimal programming conditions of CHEI [3.15]. Therefore, SSI can generate and inject a sufficiently large number of hot electrons for multi-level operations. However, the most studies have focused only on drain field variations with increasing drain bias [3.16-3.17]. As a result, important pointers to improved efficiency for SSI may have been missed. Furthermore, substrate dopant concentration control for reducing drain bias becomes both more important and more difficult as devices are scaled down [3.18].

In this thesis, 2-bit/cell operation with MLC in a Wrapped-Select-Gate polysilicon-oxide-nitride-oxide-silicon (WSG-SONOS) memory is carried out using Dynamic Threshold Source-Side-Injection (DTSSI) [3.19]. A fast programming speed with quite low power consumption was easily achieved for MLC in a WSG-SONOS memory with the DTSSI programming technique in a NOR-type array. Moreover, we compare with programming efficiency among conventional SSI (normal mode), substrate-bias enhanced SSI (Body-mode) and dynamic threshold SSI (DTSSI). Finally, a highly reliable 2-bit/cell with MLC in a WSG-SONOS device is also presented in this thesis [3.20-3.22].

3.2 Experiment

Figure 3.1 shows a cross-section of the WSG-SONOS memory with 2-bit/cell operation in a NOR-type architecture. The equilibrium cell size is 3.5 F^2 for each bit, and 0.18 μm ground rule technology was used to fabricate the device. The channel length of the word gate is 0.65 F, defined by the distance between the select-gate and drain/source region. The channel length and width of the embedded MOSFET with in-situ n^+-doped Poly-Si select-gate are 1 F and 2 F respectively, as indicated in Fig. 3.1 To execute dynamic-threshold source-side injection (DTSSI) in a WSG-SONOS memory, the select-gate wrapped around the oxide/nitride/oxide layers is tied to the p-well electrically during programming. In our device, the V_{TH} of the embedded

MOSFET in DT mode is 0.4 V, defined by the constant current method (I_{PGM}=0.1 μA), as shown in Fig. 3.2. In general, the threshold voltage of the embedded MOSFET is designed to be lower than 0.7 V, otherwise the junction leakage will boost violently in DT mode, caused by the activation of a parasitic n-p-n bipolar structure. Figure 3.2 shows that I_{PGM} offers roughly a one order of magnitude improvement in DT mode due to the dynamic body-effect affection on the embedded MOSFET, resulting in a larger memory window for its higher supply charges as discussed later. Additionally, the clear 2-bit/cell and multilevel operation schemes of the WSG-SONOS memory with DTSSI are displayed in Table 1. The drain and source regions were defined as the bit-line in the WSG-SONOS memory to accomplish the two bit per cell operation in DT mode. Erasing and reading techniques were performed by band-to-band hot-holes injection (BTBHH) and reverse-read, respectively, as shown in Table 3.1.

In this device, the thickness of the blocking oxide/ silicon nitride/ tunneling oxide layers are 10.0 nm, 8.0nm and 5.0 nm, respectively and the distance between the nitride trapping layer and select-gate is 15 nm induced by the higher thermal growth rate on the side-wall of the poly-silicon select-gate than on the single-crystal silicon [3.21]. As a result, the two physical bits can be separated by the embedded MOSFET structure of the WSG-SONOS memory in the NOR-type array, resulting in better second-bit effect with using reverse-read scheme in a very short WSG-SONOS memory device. In addition, for the CMOS-integrated circuit, the simple fabrication procedure of the WSG-SONOS memory also shows its compatibility with conventional processes. In this chapter, the simulation tool Integrated Systems Engineering (ISE) TCAD was used to analyze the DTSSI programming mechanism in the WSG-SONOS memory in the first section of this chapter. Then, the comparisons of programming efficiency among conventional SSI (normal mode), substrate-bias enhanced SSI (Body-mode) and dynamic threshold SSI (DTSSI) are detailed clearly in the second section of this chapter. At the same time, the fabrication parameters and physical models, including the device doping concentration, the material properties, the Poisson equation, and the hot-electrons injection model were fed into the simulation tools. Finally, the high-performance and high-reliability DTSSI programming method for a WSG-SONOS memory with multilevel and 2-bit/cell operation is demonstrated in the third section of this chapter.

3.3 Results and Discussions

3.3.1 DTSSI Programming Mechanism for WSG-SONOS Memory

Figure 3.3 shows the programming characteristics of the WSG-SONOS memory using dynamic-threshold source-side injection (DT mode). The WSG-SONOS was programmed in DT mode by applying different word gate biases (9~12 V) and identical drain/source biases (4 V) for 100 ns in a NOR-type array. The junction leakage due to the low forward bias at well to source (p-n junction) in DT mode is also shown in Fig. 3.3. The results indicate that both the word gate (V_{WL}) and select-gate biases (V_{SG}) dominate the programming efficiency in DT mode. In order to understand the programming mechanism of the DTSSI for a WSG-SONOS memory in a NOR-type architecture, the Integrated Systems Engineering (ISE) TCAD simulation tools were used to analyze the fabrication parameters, hot-electrons injection model and Poisson equation in DT mode.

Figure 3.4 (a) shows that devices with larger V_{SG} exhibit a lower lateral electric field and almost no vertical electric field variation at V_{WL} = 12 V and V_{BL} = 4 V in DT mode. The neutral gap region is defined by the distance between the select-gate and the nitride trapping layer beneath the word gate. The reason for the degradation of the lateral electric field is primarily body effect, which increases the potential for overdrive in the embedded MOSFET, resulting in a decrease in the voltage drop in the neutral gap region. As a result, the programming efficiency of the WSG-SONOS is degraded in DT mode with higher V_{SG}. Fortunately, the higher V_{SG} also simultaneously enhances the supply current (I_{SG}) in DT mode, as indicated in Fig. 3.2. The threshold voltage shift may still be improved in DT mode for this reason. This research thus shows the trade-off between high performance and tolerance of power dissipation under increased V_{SG}. By the same token, the larger V_{WL} affects both the lateral and vertical electric fields in DT mode, as depicted in Fig. 3.4 (b) which also shows that the V_{SG} and V_{BL} were biased at 0.45 V and 4 V, respectively. The increase in the lateral electric field is attributed to the increased inversion charge density per area beneath the word gate in DT mode, resulting in higher potential drops between the virtual source/drain and the inversion layer of the embedded MOSFET. In other words, the generation rate of hot-electrons can be enhanced by the increase in the lateral electric field. In addition, the increase in the vertical electric field at the gap region redirects the movement path of the hot-electrons, resulting in more hot-electrons being injected through the tunneling oxide and becoming trapped in the

nitride. This explains the larger shift in threshold voltage in DT mode when the device biases at higher V_{WL} voltage (9~12 V) over a very short programming time (100 ns). Further, Fig. 3.4 (c) shows the simulation results of the electric field dependences on V_{BL}. The drain and source regions are defined as the bit-line of the WSG-SONOS memory in the NOR-type architecture for performance of the 2-bit/cell operation. In this figure, the V_{WL} and V_{SG} were biased at 12 V and 0.45 V in DT mode, respectively. As in previous research [3.12-3.13], the larger V_{BL} exhibits higher lateral electric field in the gap region, resulting in the higher hot-electrons generation efficiency in our WSG-SONOS memory.

Further, figures 3.5 (a) and Fig. 3.5 (b) show the dependence of V_{WL} and V_{BL} on the programming efficiency characteristics of the WSG-SONOS memory in DT mode using an identical supply charge in a NOR-type array. The V_{WL} and V_{BL} are biased at 10 V and 4 V at 100ns in DT mode, respectively. The linear dependence between the delta V_{TH} and V_{WL}/V_{BL} shows the excellent performance with high programming efficiency in DT mode. The results can be explained by our simulation analysis of DT mode in Figures 3.4 (a) and Fig. 3.4 (b).

In sum, this section shows that the programming mechanism of our WSG-SONOS memory device in DT mode in a NOR-type architecture depends on the V_{SG}, V_{BL}, and V_{WL} bias. Optimizing the operating conditions of the WSG-SONOS memory in DT mode enables both high performance application (high speed with larger programming window) and LSTP (low stand-by power).

3.3.2 Comparison with Programming Efficiency among Conventional SSI (normal mode), Substrate-Bias enhanced SSI (Body-mode) and Dynamic Threshold SSI (DTSSI)

Unlike single gate channel-hot-electron programming SONOS devices, the I_{PGM} induced by wrapped-MOSFET can maintain a high value due to the structural separation between the left-bit and the right-bit. Therefore, the electrical effects of the nitride-trapping charges can be as low as possible. Based on these concepts, there are three kinds of programming methods for WSG-SONOS devices: normal, DT, and body mode, as illustrated in Fig. 3.6. Figure. 3.7 shows the effect of V_{SG} with 100ns of programming for each mode of WSG-SONOS memory under the same programming conditions (V_{WL}= 9~12 V, V_{BL}= 4V). A typical bell-shaped distribution

is observed in both normal and body modes, but not in DT mode. Here the DTSSI must be operated below V_{SG}=0.65V, otherwise the junction diode of the well and source will activate. In our device, the V_{th} of embedded select-gate MOSFET is only 0.4V, which is defined by the constant current method I_{PGM}=0.1 μA, in WSG-SONOS memory under DT-mode by appropriately adjusting device process. Across all three modes, the higher V_{WL} exhibits a larger programming window. This is because high V_{WL} not only enhances the collection ability with increasing normal electric field but also raises the hot electron generation rate by increasing the voltage drop across the gap region. To understand the SSI mechanism, we simulate the dependence of V_{WL} and V_{SG} on the electrical field. Both lateral and vertical electrical fields increase exponentially from the pinch-off point to the end of the neutral gap region, as shown in Fig. 3.8. The higher V_{WL} increases the maximum field peak due to the higher potential transmission from the drain terminal by increasing the inversion charge density beneath the word gate. By the same token, the higher V_{SG}, though it sufficiently enhances I_{PGM}, degrades the electric field peaks at the same time. This is because as the wrapped-MOSFET overdrive becomes higher, the voltage drop across the neutral gap region decreases, decreasing the efficiency of programming. This explains the typical bell-shaped distribution found in Fig. 3.7.

Further, the DT mode exhibits different behaviors from those of the normal and body modes, as shown in Fig. 3.7. The typical programming characteristic of the DTSSI has a higher memory window while V_{SG} is still at a low voltage. To detail this phenomenon, we simulate the electrical field dependence of each mode, as shown in Fig. 3.8. Compared to the normal and body modes, the DT mode possesses a larger acceleration electrical field between the wrapped-select gate and the word gate. Therefore, the hot-electron generation rate can be enhanced. By contrast, the body mode improves only the I_{PGM}, and degrades the lateral electrical field because of the higher V_{SG}. As a result, the body mode produces a traditional bell-shaped distribution (Fig. 3.7).

In sum, there are two major enhancing mechanisms for high programming speed of WSG-SONOS under DTSSI operation. First, the I_{PGM} increases in DT mode [3.19]; second, the maximum lateral electrical field enhancement occurs at the same time in the gap region. Owing to the body effect in DT mode, the equivalent oxide capacitance is increased by decreasing the depletion region under wrapped-MOSFET.

The increase of inversion charge density per area leads to the strong I_{PGM} injection into the gap region. Furthermore, the charge reduction of the depletion width can effectively increase the lateral electric field by decreasing the vertical electric field effects, further resulting in better gate disturbance in the WSG-SONOS. The hot electron generation efficiency can be enhanced due to the tradeoff between the lateral and vertical electric fields in the gap region.

Figure 3.8 also shows that the crossover point of both electrical fields indeed occurs near the end of the gap region close to the word-gate in all three modes. Since DTSSI is used for programming, the slight reduction of potential differences between the word gate and the well, due to the positive body bias, can induce the hot-electron injection point to move toward to drain terminal. This phenomenon is similar to a slight decrease in the word-gate voltage. This improves the band-to-band hot-hole erasing process [3.19] without degrading the programming speed. In other words, the crossover point pointed out the most possible electrons injection place due to its maximum vertical electrical field. It also implies the charge storage spatial distribution in the nitride storage layer will vary with the applied program bias [3.23] across different SSI mechanisms, when the hot electron injection point is beneath the word gate, not beside it.

Figure 3.9 displays comparisons of programming efficiency for WSG-SONOS memory using different SSI modes under the same programming conditions (V_{WL}= 9~11 V, V_{BL}= 4 V), where the supply charge is defined as $Q_{Supply\ charge} = I_{PGM} \times \tau_{PGM}$. We found that at the same supply charge, the DT mode exhibits a lower word gate bias with lower V_{SG}, resulting in higher programming efficiency. Similar to the simulation results in Fig. 3.9, the very high programming speed with improvement of programming efficiency can be attributed to the simultaneous enhancement of I_{PGM} and the lateral electrical field in the gap region. In addition, in body mode, there is still a larger threshold voltage shift even with the lower lateral field. The drawback of body mode is its greater power consumption for the higher supply charge due to its lower programming efficiency.

In sum, this section shows the source-side-injection mechanism under normal, body, and DT modes of WSG-SONOS memories. Under DT mode, devices exhibited increased lateral electric field and I_{PGM}. These changes enhanced the programming efficiency of wrapped-select-gate SONOS for NOR-type flash memory.

3.3.3 High-Performance and High-Reliability DTSSI Method for 2 Bit/Cell Operations with MLC in a WSG-SONOS Memory

Figure 3.10 shows the programming characteristics of the WSG-SONOS memory with optimum ONO thickness (10/8/5nm) programmed by the dynamic-threshold source-side injection (DT mode) method. To realize high performance multilevel operations with the WSG-SONOS memory in DT mode, 9 V, 10 V, and 11 V were applied to the word gate while the drain and source were biased at 4 V and 0 V, respectively. Further, 0.45 V was applied to the select-gate which was electrically tied to the p-well in DT mode.

Due to the high programming efficiency of DTSSI, the programming time (τ_{PGM}) is only 200 ns when applying V_{WL}= 9 V, 10 V, and 11 V in a NOR-type array. The "10", "01", and "00" states (V_{TH} shift more than 1 V, 2 V and 3 V) can thus be easily obtained, as shown in Fig. 3.10. Here, the constant sensing current method (I_{PGM}=0.1 μA) was used in reverse-read mode (V_{BL} = 1.8 V and V_{SG} = 1.6 V) to distinguish between each state, and the "11" state was defined as the initial state in our memory device. Fig. 3.11 shows the erasing characteristics of the WSG-SONOS memory for the different multilevel states in the NOR-type array, as programmed by DTSSI. In our device, the band-to-band hot-holes erasing method was used to recombine the trapping charge in the nitride storage layer. The erasing time for multilevel operation at different programming levels ("10", "01", and "00" states) is easily faster than 5 ms when - 4 V and 6 V were applied at the word-line and bit-line, respectively. Using DTSSI, our results show that the erasing characteristics of WSG-SONOS were easily controlled in multilevel application.

The I_{BL}-V_{WL} transfer characteristics and excellent margin distribution of multilevel states in our device are shown in Fig. 3.12 (a) and Fig. 3.12 (b), respectively. The threshold voltage shift exceeds 1 V ("10" state), 2 V ("01" state), and 3V ("00" state) at a very fast-speed (τ_{PGM}=200ns) in DT mode in our device. Constant current (0.1 μA) was used to define the threshold voltage of the WSG-SONOS memory, while the device was reverse-read at V_{BL} = 1.8 V and V_{SG} = 1.6 V.

In this work, a tight distribution of the threshold voltage was observed. The large

margin of each state between the neighboring programming levels is 0.87 V, 0.9 V, and 0.93V in DT mode, respectively. The memory window of more than 0.85 V relaxes the high accuracy demands of circuit design and provides the ability to precisely distinguish each state of the WSG-SONOS memory when DTSSI is used. As discussed above, the multilevel states of the WSG-SONOS memory are programmed using dynamic-threshold source-side injection technique.

The characteristics of two bit operation in a WSG-SONOS memory cell are shown in Fig. 3.13. In Fig. 3.13 only the right bit was programmed by DTSSI, while the left bit was maintained in the initial state. The inset figure shows the I_{BL}-V_{WL} transfer characteristics programmed by DTSSI for both forward-read (FR) and reverse-read (RR) modes, respectively. Forward-read mode for the WSG-SONOS memory is a common measurement method involving sweeping V_{WL} at V_D=1.8 V and V_S =0 V. The results show that the storage characteristics of these two physical bits in a cell can be reliably distinguished from the differences in threshold voltage in our WSG-SONOS. Further, crosstalk immunity can be easily obtained between the two physical bits for different multilevel states in the WSG-SONOS memory under reverse-read mode, as shown in Fig. 3.14. The bit-1 (neighboring the drain side, as indicated in Fig. 3.13) was programmed to different multilevel states (“10”, “01”, and “00” states) in DT mode, while bit-2 was kept in various multilevel states. In general, the more electrons injected into the nitride trapping layer (bit-1), the more serious the V_{TH} variation of bit-2, called second-bit effect. This phenomenon can be explained by the larger amount of the electrons stored in bit-1, resulting in potential increases beneath the word-gate. To avoid this less-than-ideal effect, with increased V_{BL}, the “screen effect” induced by extending the drain/source depletion region under bit-1 effectively decreases the second-bit effect. In our WSG-SONOS device, if using V_{BL} =1.8 V and V_{SG} =1.6 V to discriminate the exact state in our device, there is almost no crosstalk between these two bits in the WSG-SONOS memory. Briefly, the bit-line and select-gate biases should be optimized to avoid serious short channel effects in a very short channel WSG-SONOS device, and then highly reliable multilevel operations with 2 bits/cell operation in DT mode can be achieved in a scaled-down WSG-SONOS memory cell.

Figure 3.15 and Fig. 3.16 show the endurance characteristics and data retention behaviors of the WSG-SONOS memory with multilevel application under DT and normal mode, respectively. The multilevel states are programmed at the same V_{WL} = 9

V, 10 V, and 11 V in both modes with different programming times for DT mode (τ_{PGM}=200 ns) and normal mode (τ_{PGM}=1us). In this cycling test, the bit-line and select-gate were biased at 4 V and 0.45 V, respectively. Furthermore, an erasing time of 5 ms using band-to-band hot-holes was selected for the recombination process with the word-line and bit-line biased at – 4 V and 6 V, respectively. The results demonstrate that the sensing margin between each bit can still remain highly accurate with almost no V_{TH} variation even after 10^4 P/E cycles.

Charge loss behavior in the WSG-SONOS with different multilevel states at 250^{o}C high baking temperature was observed. As the baking temperature gradually increases, the thermal temperature increases the activation energy of the trapping charges in the silicon nitride, and these high-energy electrons may then tunnel-out from the trapping center or migrate and redistribute in the nitride trapping layer, resulting in variations in the threshold voltage for each state. Fortunately, the memory window is preserved, remaining large enough to enable highly reliable distinguishing of the different states in the WSG-SONOS memory device at such high baking temperatures.

Figure 3.17 demonstrates the gate disturbance (word-line) and drain/source (bit-line) disturbance for different multilevel states programmed by DTSSI in our WSG-SONOS memory. In gate disturbance, neighboring un-selected memory cells which share a common select-gate and word gate with the programming cell, were biased at 0.45 V and 12 V in DT mode, respectively. We can see that the thick top oxide (10nm) in this device creates almost no gate disturbance using DTSSI. By the same token, the bit-line disturbance (V_{BL}=4 V and V_{SG}=0.45 V) is comparatively serious in the “00” state due to the drain field inducing hole injection into the silicon nitride through the thinner tunneling oxide (5nm), resulting in recombination taking place in the nitride trapping layer.

Similar to the previous work [3.22], this result shows that an optimized ONO thickness of 10/8/5 nm in this device in DT mode still performs with excellent reliability for multilevel application even after the long stressing time of 100 seconds. In sum, our results demonstrate that our WSG-SONOS device in a NOR-type array simultaneously achieves both superior performance and high reliability for 2-bit/cell and multilevel applications using DTSSI.

3.4 Summary

A novel dynamic-threshold source-side injection (DTSSI) in WSG-SONOS memory with high performance and reliable multilevel application for 2-bit/cell operations is successfully demonstrated in this work, for the first time. We have investigated the programming mechanism of DTSSI in detail using the Integrated Systems Engineering (ISE) TCAD simulation tools. It shows that the supply current (I_{SG}), and the lateral and vertical electric fields are the three major factors affecting programming efficiency when programming WSG-SONOS memory in DT mode. Our results show that appropriate operating voltages for the WSG-SONOS memory in DT mode enable higher programming efficiency to support high-speed multilevel operation with low power consumption. Further, we obtained high performance (τ_{PGM}=200ns/τ_{ERS}=5ms) for highly reliable multilevel operation using DTSSI to program our WSG-SONOS memory. The greater noise margin between each state also provides higher flexibility for sensor amplification in circuit design. Moreover, we also found that the interferences of second bit effect and program inhibit may be almost ignored when operating 2-bit/cell using DT mode in our device. The excellent endurance characteristics and superior data retention also indicate the high potential of the WSG-SONOS memory programmed with DTSSI for high-reliability and high-performance flash applications in the future.

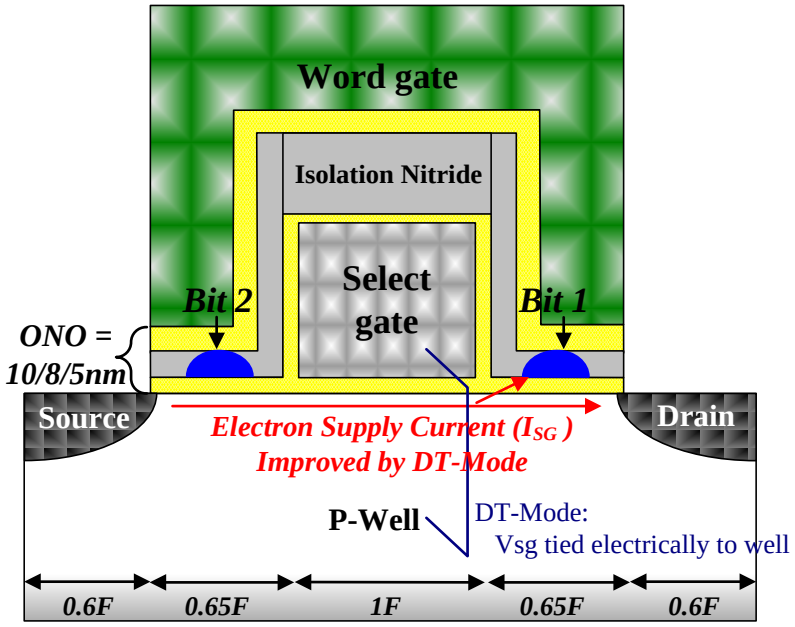


Fig. 3.1 Cross-section scheme of a 2-bit/cell WSG-SONOS memory device in DT mode. DTSSI is used to tie the select-gate to the p-well electrically. The two physical bits are separated by the embedded MOSFET.

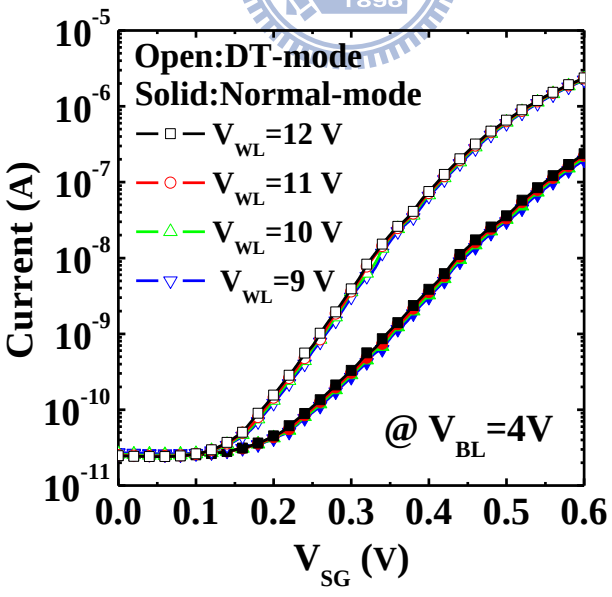


Fig. 3.2 Supply current (I_{SG}) characteristics of the embedded-MOSFET under DT and normal modes at different V_{WL} (9 V, 10 V, 11 V, and 12 V) in a WSG-SONOS memory cell, respectively.

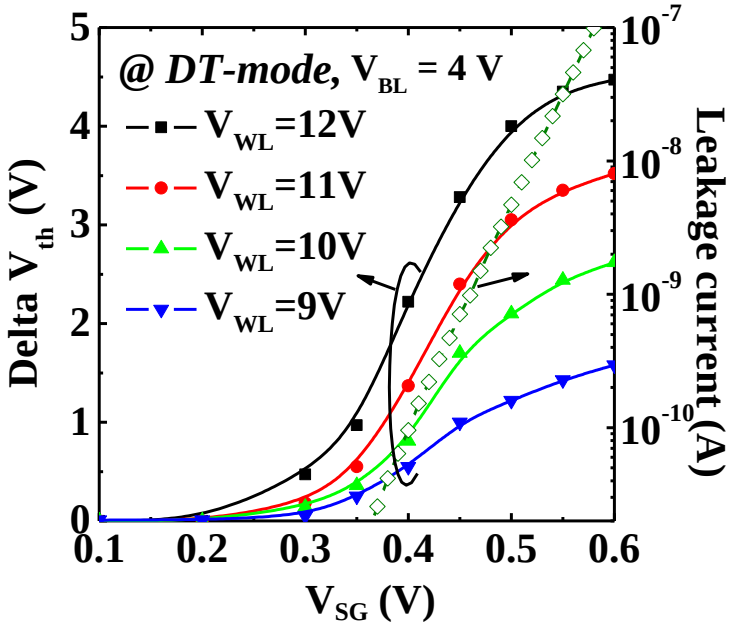


Fig. 3.3 Programming characteristics of the WSG-SONOS memory device in DT mode at different V_{WL} (9 V, 10 V, 11 V, and 12 V) and the same V_{BL} =4 V, τ_{PGM} = 100 ns for various applied select-gate biases. The junction leakage is also shown in this figure.

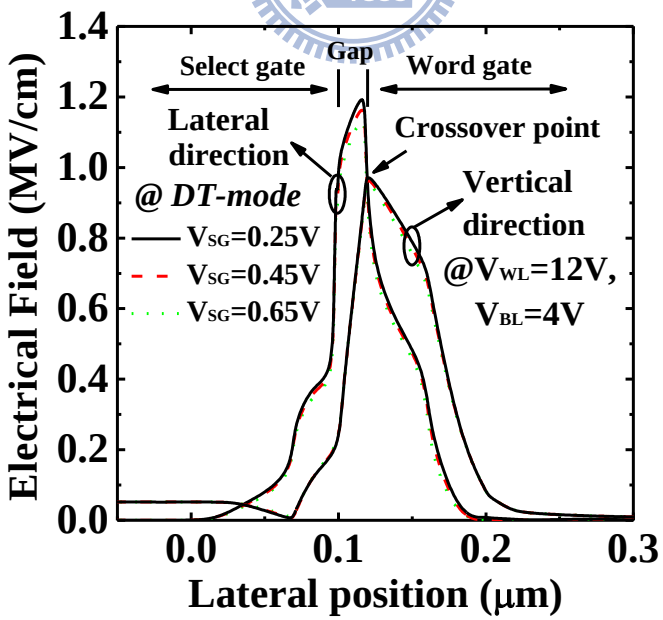


Fig. 3.4 (a) Simulation results for different applied select-gate biased dependence on the lateral and vertical electric fields in the neutral-gap region of WSG-SONOS memory in DT mode.

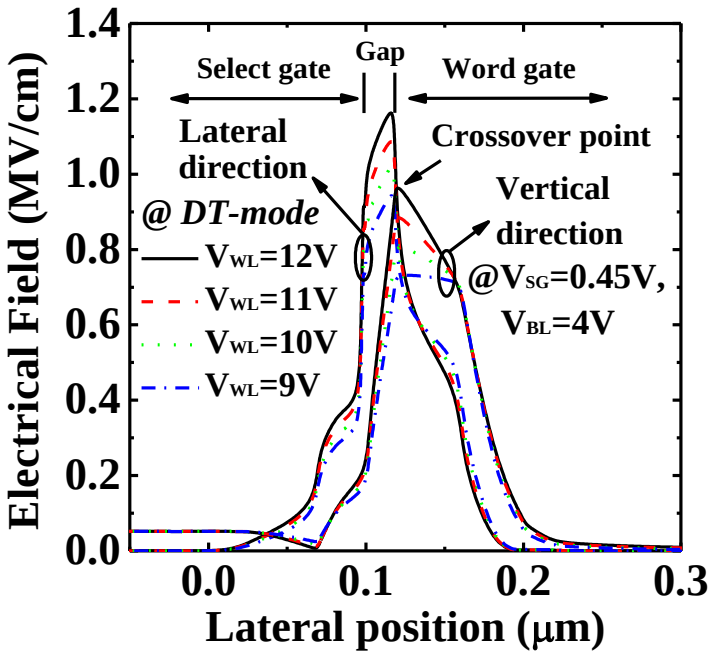


Fig. 3.4 (b) Simulation results for different applied word-line biased dependence on the lateral and vertical electric fields in the neutral-gap region of WSG-SONOS memory in DT mode.

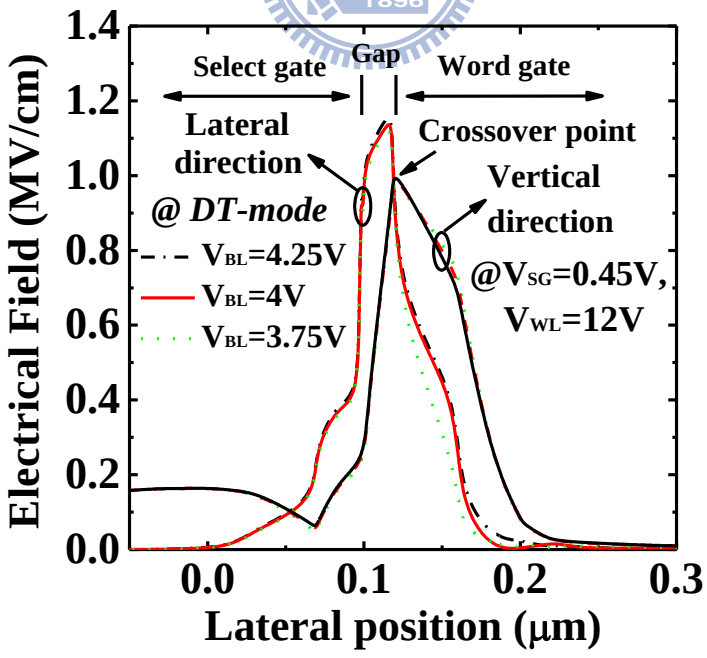


Fig. 3.4 (c) Simulation results for different applied bit-line biased dependence on the lateral and vertical electric fields in the neutral-gap region of WSG-SONOS memory in DT mode.

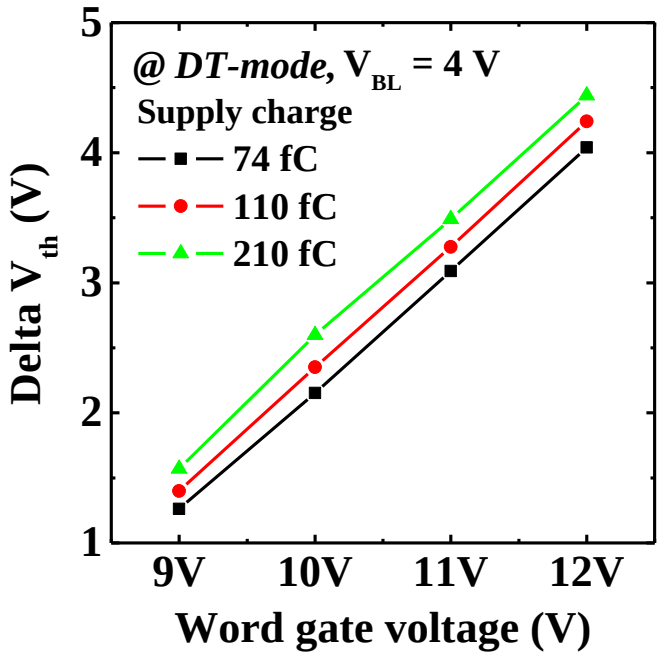


Fig. 3.5 (a) The linear dependence between delta V_{TH} and word-line biased in DT mode of the WSG-SONOS memory at different supply charges ($Q_{Supply\ charge} = I_{PGM} \times \tau_{PGM}$).

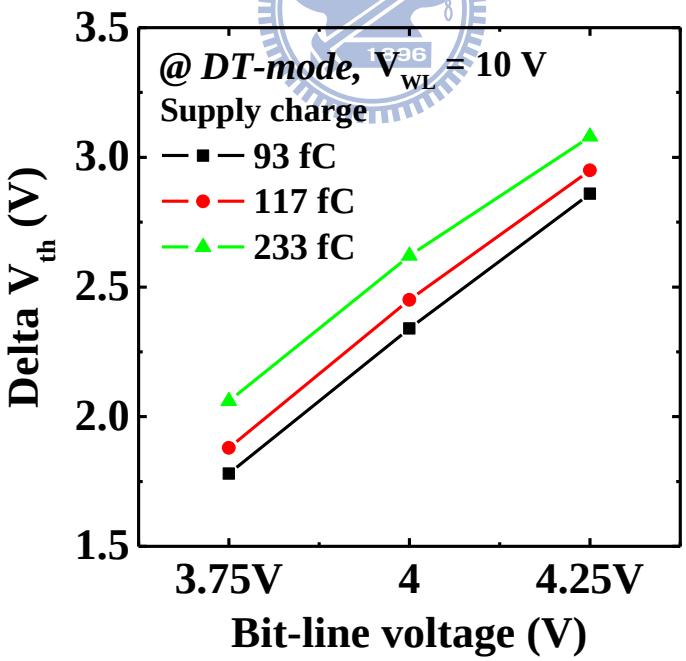


Fig. 3.5 (b) The linear dependence between delta V_{TH} and bit-line biased in DT mode of the WSG-SONOS memory at different supply charges ($Q_{Supply\ charge} = I_{PGM} \times \tau_{PGM}$).

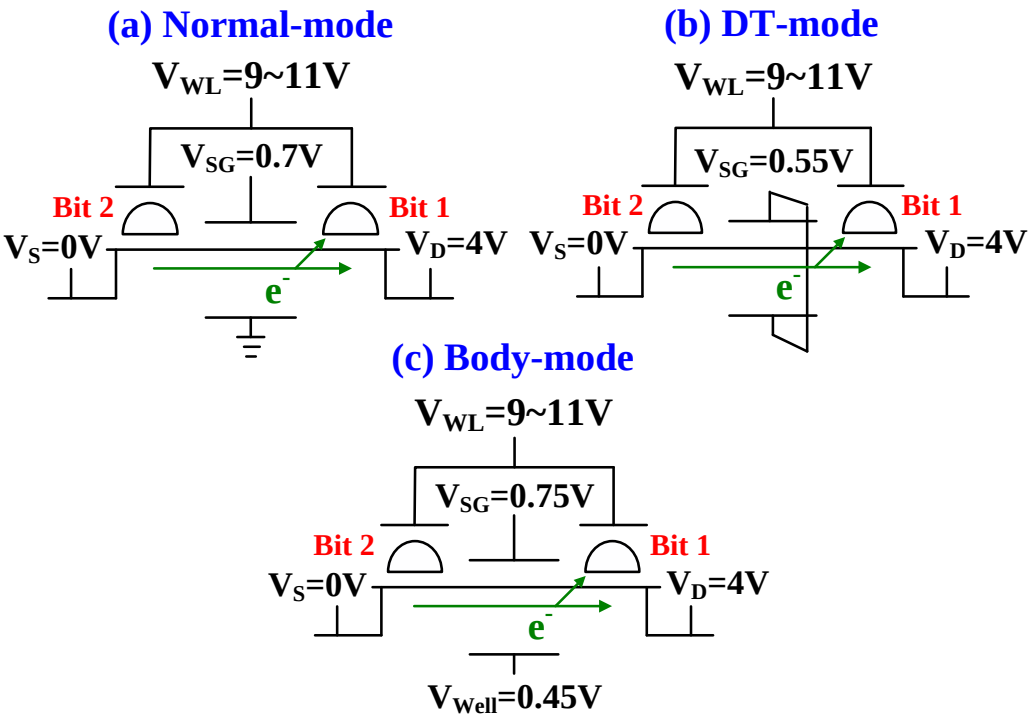


Fig. 3.6 Comparison of (a) traditional SSI (b) dynamic-threshold SSI (c) body-bias enhanced SSI programming schemes.

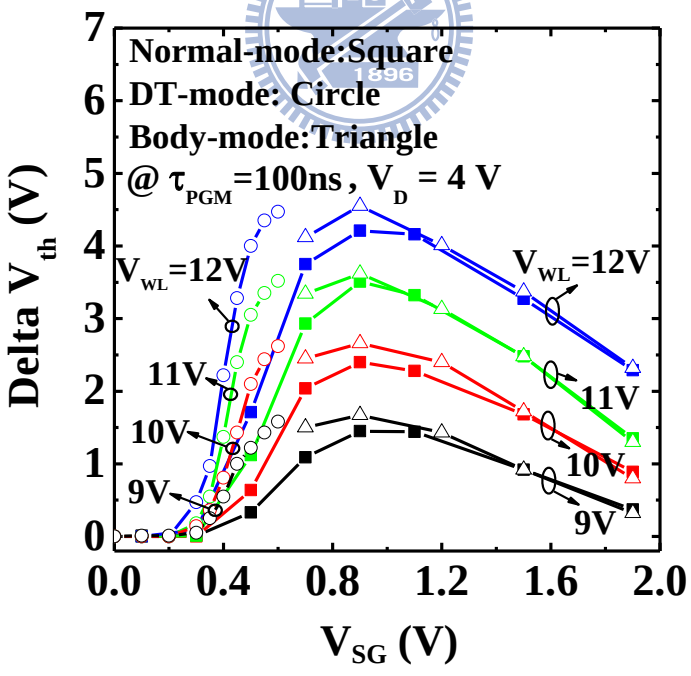


Fig. 3.7 Programming characteristics of WSG-SONOS memory as a function of V_{SG} and V_{WL} at fixed V_{BL}=4V with τ_{PGM}=100ns for each mode. Typical bell-shaped distribution of the threshold voltage shift is observed in normal and body modes (V_{Well}=0.45 V).

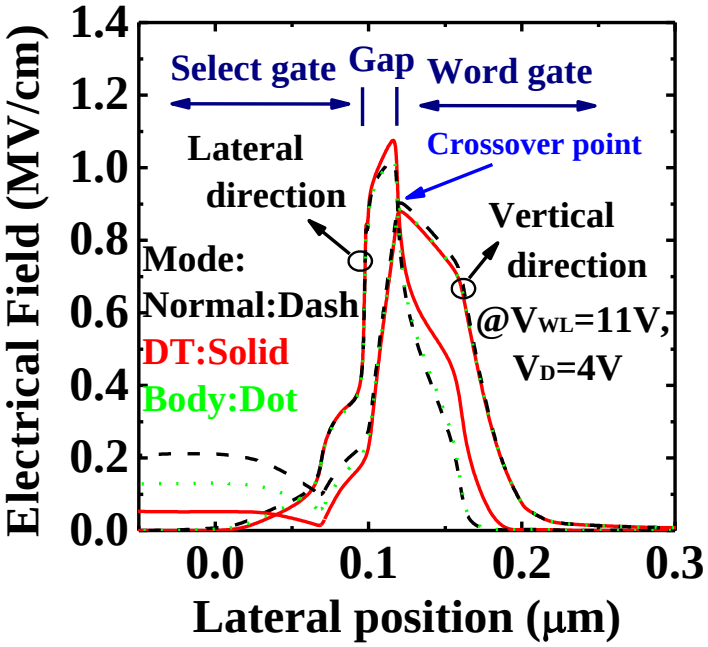


Fig. 3.8 Comparison of electrical field variations for each mode. (Normal-mode: V_{SG}=0.7 V、DT mode: V_{SG}=V_{Well}=0.55 V、Body mode: V_{SG}=0.75, V_{Well}=0.45 V)

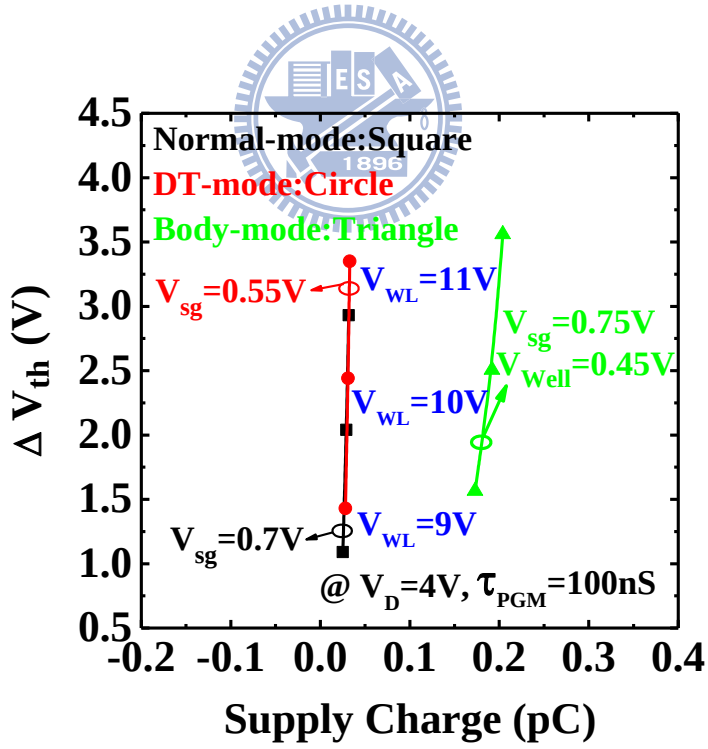


Fig. 3.9 Programming efficiency with the same supply charge ($Q_{Supply\ charge}$ =I_{PGM} x τ_{PGM}) under V_{WL}=9V, V_{WL}=10V and V_{WL}=11V for each mode, respectively.

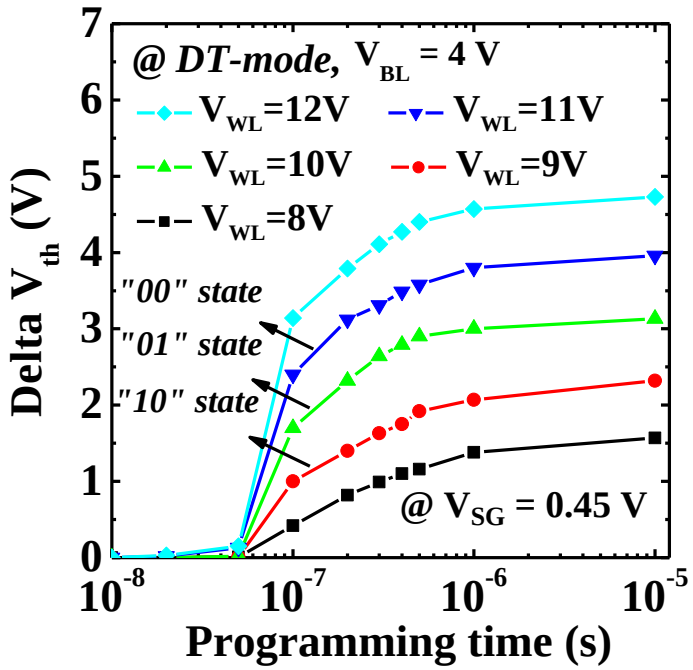


Fig. 3.10 Programming characteristics of the WSG-SONOS memory with multilevel operation in DT mode.

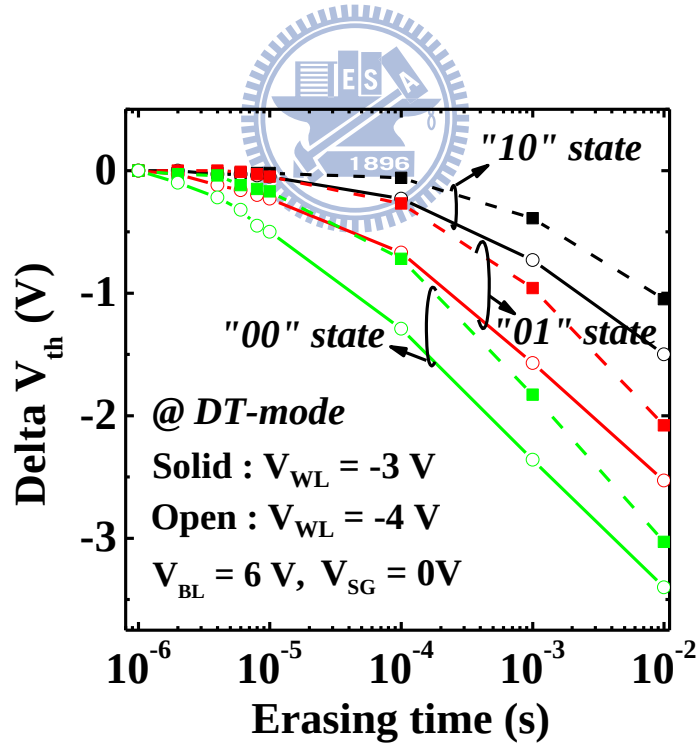


Fig. 3.11 Erasing characteristics of the WSG-SONOS memory across different multilevel states. The different initial multilevel states were erased using the same V_{BL}, while the erasing time is lower than 5 ms programming in DT mode.

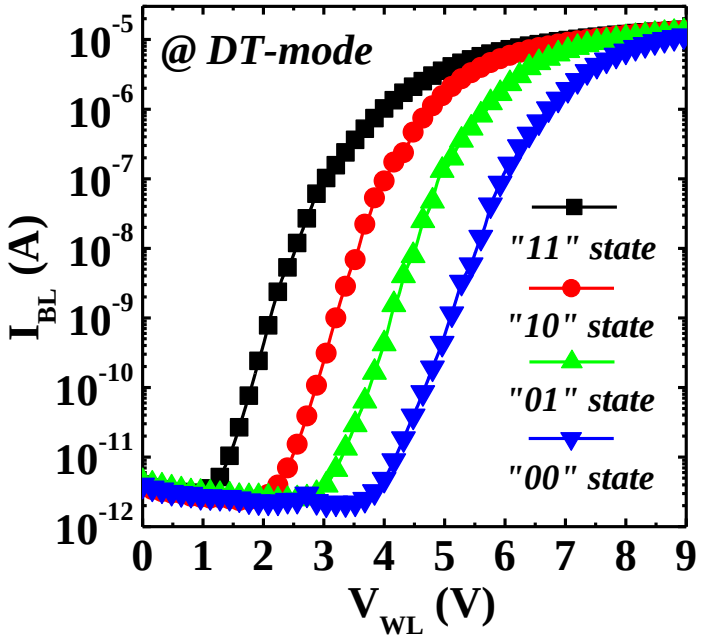


Fig. 3.12 (a) The I_D-V_G characteristics of different multilevel states programmed by DTSSI

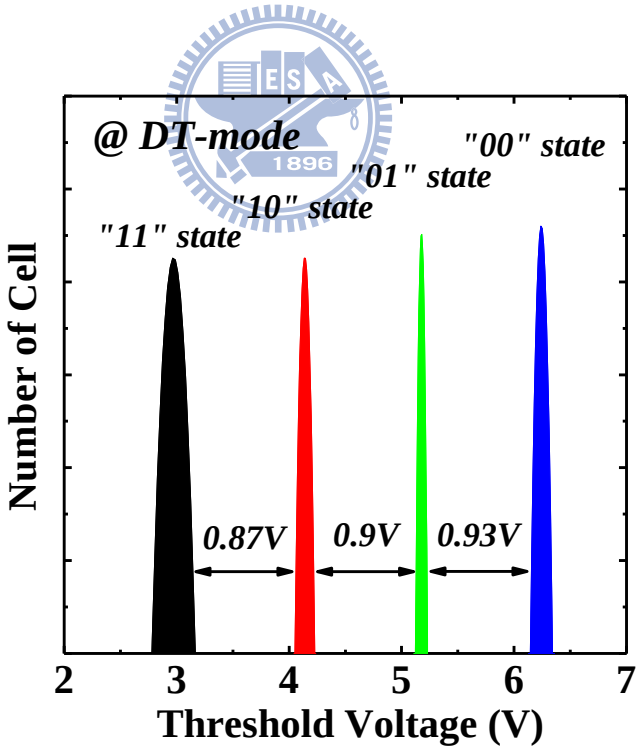


Fig. 3.12 (b) The V_{TH} distribution of the WSG-SONOS memory at different programming levels under DT-mode.

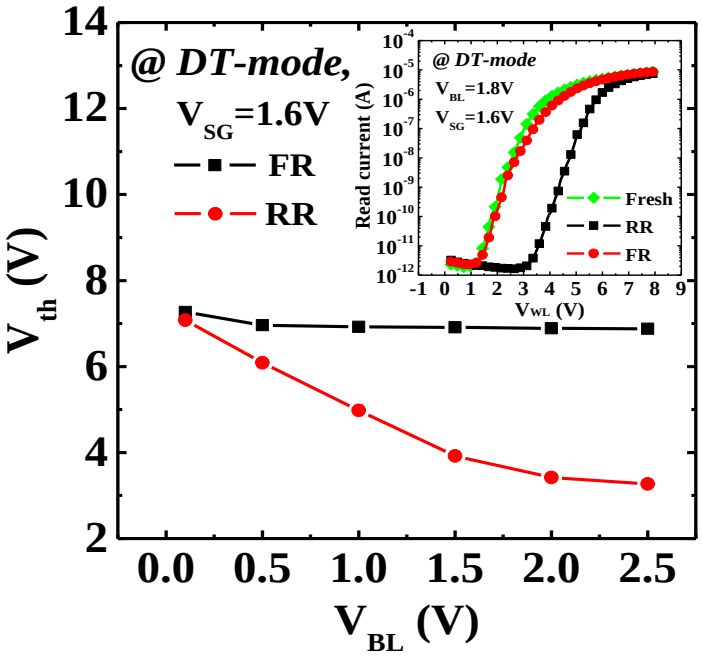


Fig. 3.13 2-bit/cell characteristics of WSG-SONOS memory programmed using DTSSI under forward-read (FR) and reverse-read (RR), respectively. The inset figure shows the good I_D-V_G curves of reading bit-1 and bit-2 for WSG-SONOS memory.

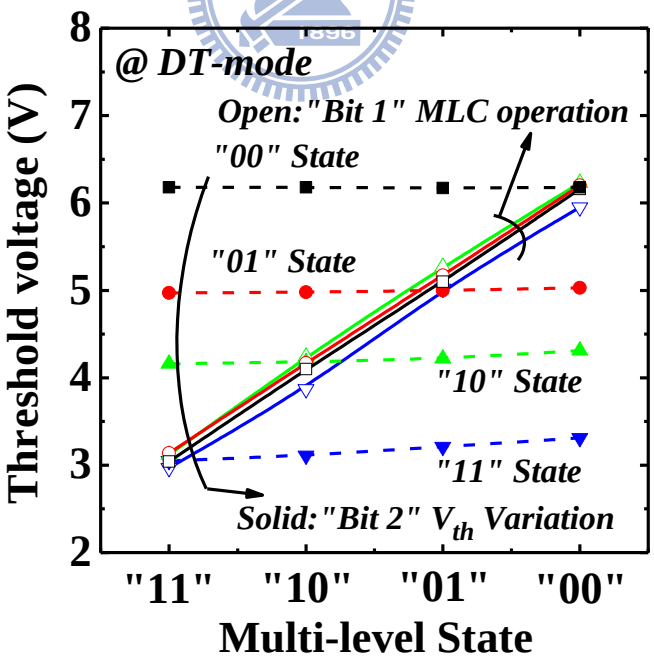


Fig. 3.14 The superior second bit effect characteristics of WSG-SONOS memory for different multilevel states programmed using DTSSI.

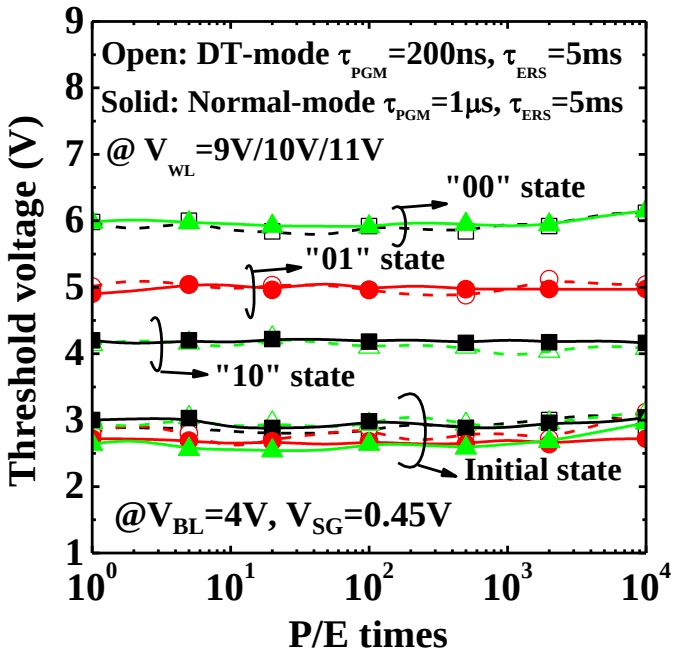


Fig. 3.15 Endurance characteristics across different multilevel states of the WSG-SONOS memory for DT and normal modes with the same V_{WL}, V_{BL} and V_{SG}, respectively.

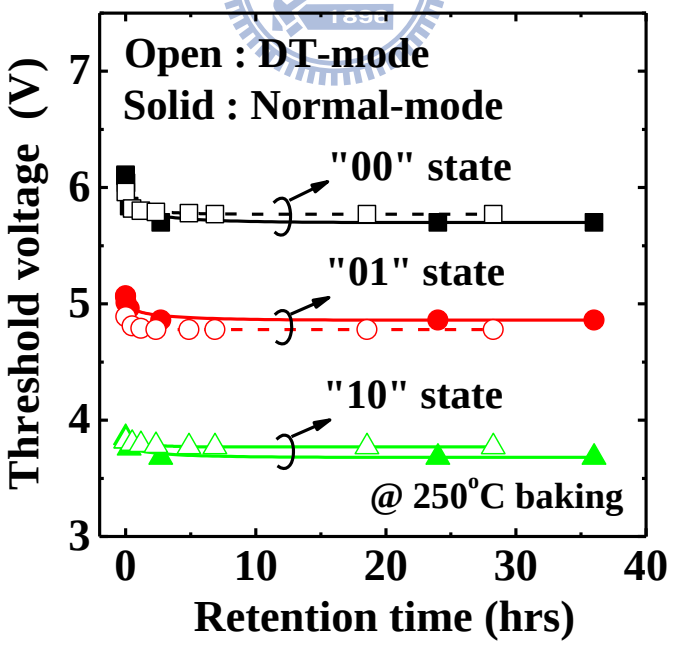


Fig. 3.16 Data retention characteristics for different multilevel states obtained from the WSG-SONOS memory under both programming modes at high baking temperature (250°C).

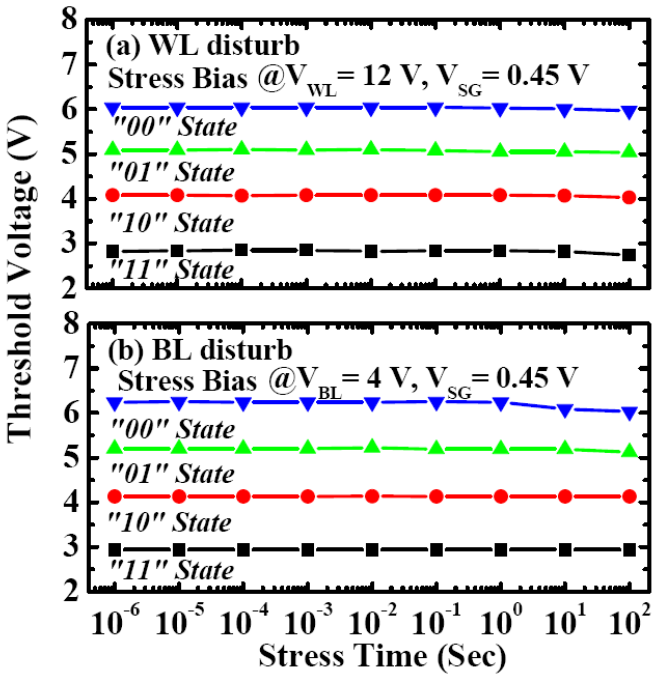


Fig. 3.17 (a) Word-line and (b) bit-line disturbances of WSG-SONOS memory with ONO layers (5/8/10 nm) in DT mode in NOR-type architecture.

Multi-level states: “10” state、 “01” state 、 “00” state DT-Mode: V_{WL}=9V、 V_{WL}=10V 、 V_{WL}=11V							
Bit-1 operation	**Mode**	**Time**	**V_{WL}**	**V_D**	**V_S**	**V_{SG}**	**V_{Well}**
Program	**DT**	**200ns**	**9~11V**	**4V**	**0V**	**0.45V**	**0.45V**
Erase	**BTBT**	**5ms**	**-4V**	**6V**	**0V**	**0V**	**0V**
Read	**Reverse**	**Sweep time**	**Sweep 0-8V**	**1.8V**	**0V**	**1.6V**	**0V**

Table 3.1 Multilevel operating conditions for the WSG-SONOS memory in a NOR-type architecture.

Write/Erase/Read Performance for Multi-level Operation

MLC State	“11” State	“10” State	“01” State	“00” State
Programe Voltage	Initial State	V_{WL}=9V	V_{WL}=10V	V_{WL}=11V
Programming Time	N.A	110nS	140nS	200nS
Erase Voltage	Initial State	V_{WL}=-4V	V_{WL}=-4V	V_{WL}=-4V
Erasing Time	N.A	3mS	4mS	5mS
Programming Current (@Vsg=0.45V)	0.25uA			
Read Current	1.2uA			

Reliability for Multi-level Operation

MLC State	**“11” State**	**“10” State**	**“01” State**	**“00” State**
Gate Disturbance	0.01V	0.01V	0.01V	0.01V
Drain Disturbance	0.01V	0.01V	0.08V	0.11V
2nd Bit Effect	0.18V	0.15V	0.06V	0.01V
Endurance 1E4 Times	0.17V	0.05V	0.05V	0.14V
250°C (28hours)	0.02V	0.05V	0.11V	0.18V

Table 3.2 High-performance and high-reliability of multilevel operation for the WSG-SONOS memory in a NOR-type architecture.

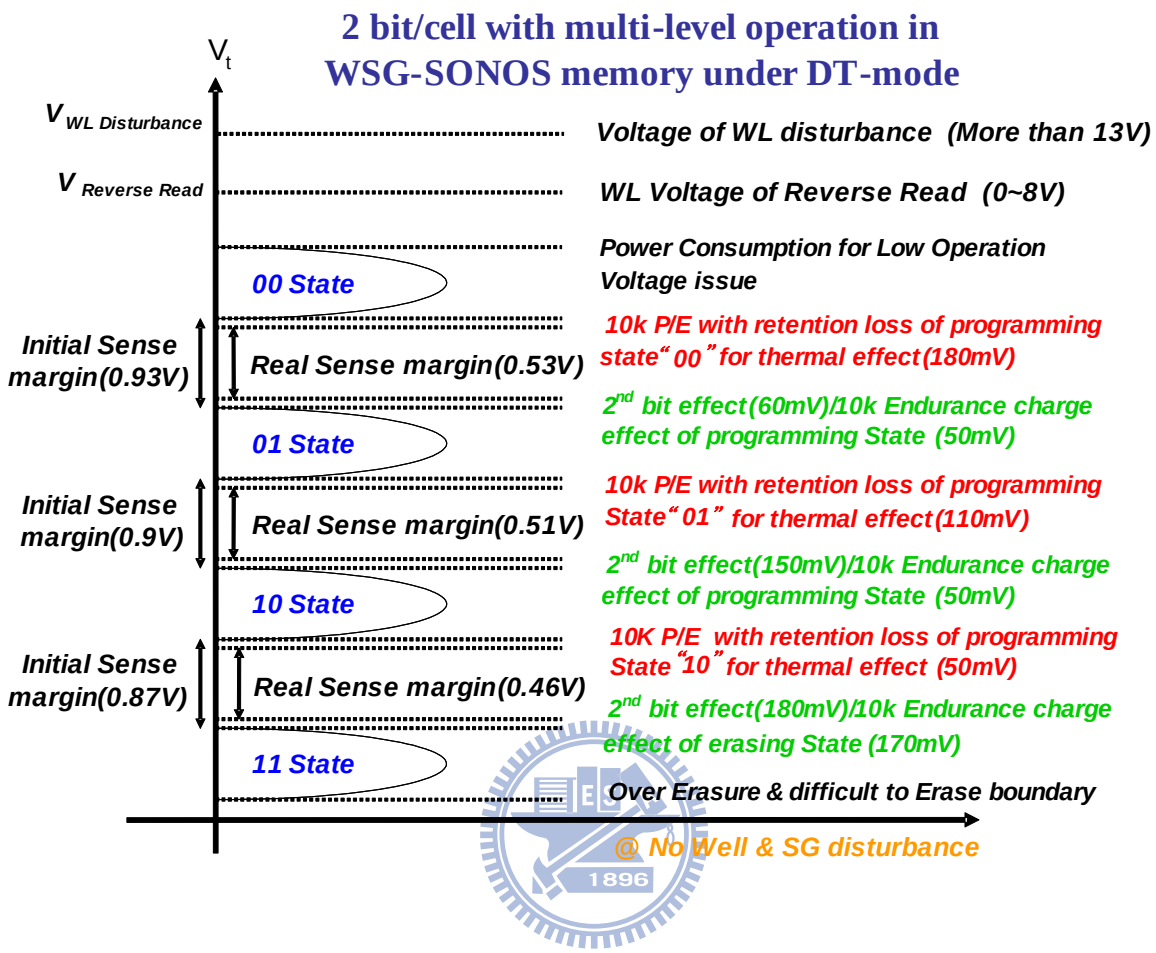


Table 3.3 Sense margin of 2 bit/cell with multilevel operation for the WSG-SONOS memory in a NOR-type architecture.

Chapter 4

The Zero-Temperature-Coefficient Point Modeling of DTMOS

4.1 Introduction

According to the general CMOS technology application in our life, it has been a growing interest in designing circuits and devices that operate reliably with low power consumption over a widespread temperature range from 298 K to 398 K. As a result, it is desirable to operate circuits designed at zero-temperature-coefficient (ZTC) point where the driving current must be insensitive to the temperature in the extreme environment. Generally, the existence of ZTC point is due to its reciprocal compensation between the effective mobility (μ_{eff}) and threshold voltage (V_{TH}) at elevated operated temperature in MOSFET [4.1-4.3]. There are also many published paper to confirm the existence and advanced to derive the theory of ZTC point by combining the experimental data, the error values between the theoretical predicted results and row data are lower than 5% and 14% in the linear and saturation region, respectively [4.4-4.5]. From the results of these ZTC point model, it can be found that while more physical factors are considered would effectively reduce the error values between the theoretical modeling and experiment data. As a result, we try to develop a ZTC point modeling for both long channel and short channel devices with detailing physical insights in CMOS integration. In the thesis, the definition of ZTC point can be expressed as:

$$\frac{\partial I_D}{\partial T} = 0 \tag{4.1}$$

And the ZTC point means that gate voltage value of device while driving current (I_D) wouldn't vary with temperature. It should be noted that, the developed modeling of ZTC point is obtained by the least squares method which minimizes the differences between the left and right-hand sides of the initial definition over a specified operating temperature range T_i to T_f [4.1-4.3]. Combining the method with clear physical insights, it leads the ZTC model to be more accurate. Besides, the idea of attaining high performance with low power consumption by using dynamic threshold (DT) technique [4.6-4.8] applications has become popular in the development of a number of MOS technologies, including 6T-SRAM, RFID circuit, multiplier, and low voltage analog circuit [4.9-4.11]. However, the DT technique operated at elevated temperature

should seriously degrade the performance, caused by the phonon scattering, which results in some of the reference circuit failures. To solve these unstable temperature problems, the zero-temperature-coefficient (ZTC) point which is an important parameter for stable CMOS integrated circuit work over an operated temperature is applied [4.4-4.5], as mentioned before. In the thesis, the ZTC design criterion for a stable integrated circuit under consideration of elevated temperature DT operation means that to drive circuits at an optimal gate voltage with temperature independence is desired. Based on these concepts [4.4-4.5] and [4.12], for the first time, we derived and verified the zero temperature coefficient (ZTC) point model of a DTMOS transistor for operations at typical room temperatures to military range (25℃ to 125℃).

4.2 Experiment

4.2.1 Device Fabrication

The Metal gate/High-k advanced transistors used in this work were fabricated by state-of-the-art 300 mm wafer with foundry technology. To reduce the low quality interaction between gate dielectric and silicon bulk, the interfacial layer was formed by chemical oxide. In turn, the gate dielectric with [Hf]/(Hf+Si) were deposited by atomic-layer deposition (ALD) techniques. N_2 ambient annealing was used to decrease the dielectric defects. It followed by a 100Å physical vapor deposition (PVD) metal film (including: TaC and TiN) and a 1000Å polysilicon gate capping layer. After gate patterning, halo implantation was used to optimize the short channel control for short channel devices. Eventually, BEOL process is following a high-temperature annealing to active the source/drain junction of device.

2.2.2 Measurement setup

The DTMOS are operated by connecting the gate with the substrate electrically by using keithley 708A. The substrate bias may thus be given as:

$$V_{BS} = \alpha V_G \quad (0 \le \alpha \le 1) \tag{4.2}$$

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate. Due to the limitation of V_{BS} <0.7V under DT mode, the validation range of α is also defined in equation (4.2). Devices operated under normal and DT-modes

while the $\alpha = 0$ and $\alpha > 0$, respectively. In our experiment, we compare the ZTC point characteristics of three different gate stack system (Poly/HfSiON, TaC/HfSiON and TiN/HfSiON) both under normal and DT-modes. For the third part of the chapter 4, we define the V_{TH} of devices by using the maximum transconductance linear extrapolate method. The DC measurement with using Keithley 4200 semiconductor parameter analyzer is at different operated temperature over 298 K to 398 K. Furthermore, we extract the effective mobility with using split C-V method for both under normal and DT-modes. The split C-V characteristics are measured at a frequency of 1 MHz with different metal gate devices to extract the gate to channel (C_{GC}) and gate to bulk capacitance (C_{GB}) by using HP 4284 LCR parameter analyzer [4.13]. Finally, we summarize the advantages of DTMOS in the conclusions of the chapter 4.

4.3 Results and Discussions

4.3.1 The Zero-Temperature-Coefficient Point Modeling of DTMOS

Figure 4.1 shows the I_D-V_G characteristics of NMOS transistor with ZTC for both under normal and DT-modes at elevated temperature over 298 K to 398 K, respectively. The ZTC point is 0.85 V of DT-mode which shows the higher driving current with low operation voltage than normal-mode. Figure 4.2 shows the C_{GC} characteristics extracted from split C-V measurement with fixed body-bias mode. Figure 4.3 and Fig. 4.4 show the effective mobility versus surface charge density characteristics with elevated temperature over 298 K to 398 K and fixed body-bias mode, respectively. The effective mobility largely enhances due to its reduction of depletion charge. On the other hand, the effective mobility would also decrease resulting from phonon scattering as increasing of temperature. Figure 4.5 shows the G_m characteristics similar to the effectively mobility while continue increase the operated temperature under DT mode. For easily to discuss the affects of phonon scattering, we use G_m characteristics to extract the degradation factor K_1 dependence of temperature. In addition, in order to accurately express the ZTC point analytical solutions for DTMOS, employing an appropriate analytical drain current model is important. As a result, our DTMOS ZTC point theory is based on the simple and accurate charge sheet approximation of the MOSFET drain current model with depletion approximation which considers both the linear and saturate regions by

simultaneously including the channel potential and body effect [4.14]. For DTMOS, the drain current expressions may be expressed as

Linear region:

$$I_{DS} = \frac{W}{L} C_{ox} \mu_n \left\{ \left(V_G - V_T \left(T, V_{BS}, V_{DS} \right) \right) V_{DS} - \frac{m}{2} {V_{DS}}^2 \right\} \tag{4.3}$$

Saturation region:

$$I_{DS} = \frac{W}{L} C_{ox} \mu_n \frac{\left(V_G - V_T \left(T, V_{BS}, V_{DS} \right) \right)^2}{m} \tag{4.4}$$

Where

$$m = 1 + \delta \tag{4.5}$$

$$\delta = -\frac{dV_T}{dV_{BS}} = \frac{1}{C_{ox}} \sqrt{\frac{q \varepsilon_{Si} N_a}{2 \left(2\phi_{fp} - V_{BS} \right)}} \tag{4.6}$$

m is the body effect coefficient, C_{ox} is the gate oxide capacitance per unit area, μ_n is the effective channel mobility, uniform channel doping N_a is assumed here, and W and L are the channel width and length, respectively. As same as mentioned before, because the DTMOS transistors are operated by connecting the gate with the substrate, the substrate bias may thus be given as:

$$V_{BS} = \alpha V_G \quad (0 \le \alpha \le 1) \tag{4.7}$$

The α is defined as a constant ratio of the dynamical biases between the gate and the substrate. Due to the limitation of $V_{P\text{-}Well}$<0.7V under DT mode, the validation range of α is also defined in equation (4.7). Devices operated under normal and DT-modes while the $\alpha = 0$ and $\alpha > 0$, respectively.

Furthermore, the effective mobility dependence on operation temperature, for an ideal MOS transistor, is usually given as:

Linear region:

$$\frac{\mu_n \left(T_f \right)}{\mu_n \left(T_i \right)} = \frac{G_{m,\max} \left(T_f \right)}{G_{m,\max} \left(T_i \right)} = \left(\frac{T_f}{T_i} \right)^{-K_1} \tag{4.8}$$

Saturation region:

$$\frac{\mu_n \left(T_f \right)}{\mu_n \left(T_i \right)} = \frac{G_m \left(T_f \right) \left(V_{G,(ZTC)} - V_{T,i} \right) m \left(T_f \right)}{G_m \left(T_i \right) \left(V_{G,(ZTC)} - V_{T,f} \right) m \left(T_i \right)} = \left(\frac{T_f}{T_i} \right)^{-K_1} \tag{4.9}$$

Where T_i is the initial room absolute temperature and K_1 is the corresponding constant, smaller than the previous reports, which is extracted from the transconductance

degradation of ZTC point at elevated operation temperature, as shown in Fig. 4.5. By using the method, the mobility variations of DTMOS caused by the threshold voltage decrease with different temperature have also been included.

As we known that: $I_D^{Sat.} \propto (V_{GS} - V_T)^X$. To increase the accuracy of DTMOS ZTC modeling, especially for sub-micron device, we may correct the power dependence of square term under saturation mode by following extraction:

$$\frac{I_{D,Sat.}(V_{GS2})}{I_{D,Sat.}(V_{GS1})} = \left(\frac{V_{GS2} - V_T}{V_{GS1} - V_T} \right)^X \Bigg|_{@V_{GS2} > V_{GS1} > V_{G,(ZTC)}} \tag{4.10}$$

Generally, in published papers, the value of X equals 2, corresponding to the ideal square law for long channel device. However, the theoretical value under saturation region always brings about quite notable error more than 10%. Therefore, we try to estimate the actual power dependence with using the experiment data in behalf of reducing the prediction errors [4.4-4.5].

In this chapter, the V_{TH} is extracted by the maximum transconductance linear extrapolation method [4.13]. The assumptions of V_{TH} dependence on temperature and body bias are modeled simultaneously in the following approximate expressions:

$$V_T(T, V_{BS}, V_{DS}) \cong p_0 T + r_0 V_{BS} + \eta V_{DS} + q_0 \tag{4.11}$$

where

$$p_0 = \left. \frac{dV_T}{dT} \right|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average} \tag{4.12}$$

$$r_0 = \left. \frac{(V_{T2}(T, V_{BS2}, V_{DS}) - V_{T1}(T, V_{BS1}, V_{DS}))}{V_{BS2} - V_{BS1}} \right|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average} \tag{4.13}$$

$$\eta = \left. \frac{(V_{T2}(T, V_{BS}, V_{DS2}) - V_{T1}(T, V_{BS}, V_{DS1}))}{V_{DS2} - V_{DS1}} \right|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average} \tag{4.14}$$

$$q_0 = V_T(T_i, V_{BS}, V_{DS}) - r_0 V_{BS} - p_0 T_i - \eta V_{DS} \Big|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average} \tag{4.15}$$

The p_0, q_0, η and r_0 are average values extracted from the experimental data. P_0 is affect by the temperature effect, q_0 is affect by the body effect and η is affect by the DIBL effect, especially for short channel device. Further, the temperature dependence of the body effect coefficient may be approximated by the expression:

$$m = 1 + \delta \cong 1 + sT + t \tag{4.16}$$

where

$$s = \left.\frac{d\delta}{dT}\right|_{T_i \sim T_f} \tag{4.17}$$

$$t = \delta(T_i) - T_i \left.\frac{d\delta}{dT}\right|_{T=T_i} \tag{4.18}$$

A main reason is increasing of n_i while increases operated temperature. In addition, the DIBL effect may also be approximated by the following expression:

$$\eta \cong uT + v \tag{4.19}$$

where

$$u = \left.\frac{d\eta}{dT}\right|_{T_i \sim T_f} \tag{4.20}$$

$$v = \eta(T_i) - T_i \left.\frac{d\eta}{dT}\right|_{T=T_i} \tag{4.21}$$

The detailed physical expressions of dV_T/dT and $d\delta/dT$ may also be found in the reference [4.14].

After deriving the initial definition of $dI_{DS}/dT=0$ under DTMOS ZTC model, and using the least-squares method to ensure drain current independence over the temperature range T_i to T_f [4.4-4.5], the expression of both linear and saturate regions can be obtained as following:

Linear region:

$$\frac{d}{dV_G}\int_{T_i}^{T_f}\left[V_G(ZTC) - V_T + \frac{T}{K_1}\left(\frac{V_{DS}}{2}\frac{d\delta}{dT} + \frac{dV_T}{dT}\right) - \frac{mV_{DS}}{2}\right]^2 dT = 0 \tag{4.22}$$

Saturation region:

$$\frac{d}{dV_G}\int_{T_i}^{T_f}\left[V_G(ZTC) - V_T + \frac{2mT\dfrac{dV_T}{dT}}{\left(mK_1 + T\dfrac{d\delta}{dT}\right)}\right]^2 dT = 0 \tag{4.23}$$

As a consequence, by substituting the assumptions described by equations (4.7)-(4.21) into the results, the expression (4.22) and (4.23) can be rewritten as:

Linear region:

$$\frac{d}{dV_G}\int_{T_i}^{T_f}\left[\begin{array}{l} V_G(ZTC)-\left(p_0T+r_0\alpha V_g+\eta V_{DS}+q_0\right)+\dfrac{T}{K_1}\left(\dfrac{sV_{DS}}{2}+p_0\right) \\ -\dfrac{V_{DS}}{2}(1+sT+t)\end{array}\right]^2 dT=0 \qquad (4.24)$$

Saturation region:

$$\frac{d}{dV_G}\int_{T_i}^{T_f}\left[V_G(ZTC)-\left(p_0T+r_0\alpha V_g+\eta V_{DS}+q_0\right)+\frac{2p_0T(1+sT+t)}{K_1(1+sT+t)+sT}\right]^2 dT=0 \qquad (4.25)$$

Consequently, by solving the equations, we propose formulations for the linear and saturation region of the ZTC point model of the DTMOS transistor, respectively:

Linear region:

$$V_G{}^{Lin}(ZTC)\cong\frac{\left(p_0+uV_{DS}+\dfrac{sV_{DS}}{2}\right)\left(1-\dfrac{1}{K_1}\right)(T_i+T_f)+V_{DS}(1+t)+2(q_0+vV_{DS})}{2(1-\alpha r_0)} \qquad (4.26)$$

Saturation region:

$$V_G{}^{Sat}(ZTC)\cong\frac{(p_0+uV_{DS})\left(1-\dfrac{x}{K_1+1}\right)(T_i+T_f)+2(q_0+vV_{DS})-\dfrac{(p_0+uV_{DS})T_\delta}{K_1}\left(\dfrac{2x}{K_1+1}\right)\left[1-\dfrac{T_\delta}{(T_f-T_i)}\ln\left(\dfrac{T_f+T_\delta}{T_i+T_\delta}\right)\right]}{2(1-\alpha r_0)} \qquad (4.27)$$

where

$$T_\delta = \frac{K_1(1+t)}{s(1+K_1)} \qquad (4.28)$$

4.3.2 The Validation of Zero-Temperature-Coefficient Point Modeling of DTMOS

The proposed model is verified using the experimental data obtained from our DTMOS device in which channel length and width is 1 and 10 μm for long channel device and 0.1 and 10 μm for short channel device, respectively. Figure 4.6 shows the threshold voltage dependences on the temperature from 25℃ to 125℃ with different body biases. The physical parameters p_0, q_0, and r_0 of the ZTC point model for DTMOS can be extracted easily from our model. In general, the threshold voltage decrease with increasing body bias can be considered a continued reduction of the depletion region in DTMOS, as shown in Fig. 4.7. The straight black line shows that the body bias varies dynamically with gate bias under different alpha ratios and the crossover points shows a gradual reduction in threshold voltage, due to the increase in

n_i with increasing operating temperature. The inset of Fig. 4.8 shows the temperature dependence of the body effect coefficient over the temperature range of 298K to 398K. The characteristic features s_0 and t_0 in our ZTC point model of DTMOS are extracted from the slope and extrapolated point of a body effect coefficient versus absolute temperature curve, simultaneously. Figure 4.9 and Fig. 4.10 show the K_1 degradation factors dependence of temperature with different alpha ratios under linear and saturation regions, respectively. The higher carrier energy results in the lower values of K_1 degradation factors. It can also prove the large enhancement of mobility while operated under DT mode, indirectly. At the same time, the error between our model and experiment is almost neglected, proving our G_m extraction method for K_1 degradation factors is feasible. The $V_{G, (ZTC)}$ and K_1 dependence of body bias are both shown in Fig. 4.11. It can be found that our fixed body bias mode of ZTC model can still perform excellent prediction results with quite low mismatch to the row data at elevated temperature environment. The detail expressions of fixed body bias ZTC model both under linear and saturation are shown in Table. 4.1. Furthermore, Fig. 4.12 shows the ZTC point of DTMOS can be determinate by row data with different alpha ratios condition under fixed body-bias mode. The maximum error can be reduced smaller than 1% for Poly/SiO_2 NMOS. The clear comparison results between our DTMOS ZTC model and experimental data under linear and saturation regions are both shown in Fig. 4.13. The maximum error about 1.5% happens at the transition region through linear region to saturation region. Different alpha ratios prove the good agreement between our model and experimental values. In addition, the variation characteristics of ZTC point operation after stress 2000 sec demonstrate the excellent reliability for DTMOS due to its low operation voltage, as shown in Fig. 4.14. Similar to the silicon dioxide device, the HK/MG devices also show the ZTC point characterization as shown in Fig. 4.15. The V_{TH} and K_1 degradation factor dependence of body bias are both shown in Fig. 4.16 and Fig. 4.17. Unlike long channel device, the short channel device shows the smaller K_1 degradation factor both under linear and saturation regions in Fig. 4.18 due to its higher carrier transport energy. Then, the temperature effects of body effect coefficient can be extracted from Fig. 4.19. Different to long channel device, the DIBL effect couldn't be neglected in short channel device. The temperature effects of DIBL concern parameter can also be extracted from Fig. 4.20 at elevated temperature from 298 K to 398 K. Finally, we demonstrate that ZTC point of both long channel and short channel devices for

traditional or advanced gate stacks can be precise prediction by our DTMOS ZTC model, for maximum error smaller than 1%, with different behaviors of ZTC point under saturation region resulting from DIBL effect. The large improvement for precisely predicted ZTC point can be attracted to the detailed temperature dependence of physical parameters effect, respectively. The detail physical insights and expressions of DTMOS ZTC modeling both under linear and saturation are shown in Table. 4.1, simultaneously. Figure 4.23 and Fig. 4.24 show a clear chart to illustrate the ZTC point position at an I_D-V_G curve. It locates after the V_{TH} about 0.2 V at linear region and 0.3 V at saturation, respectively. As we know that DTMOS shows the more excellent electrical characteristics at low temperature operation, for predicting ZTC precisely now, the DTMOS operated at quite low temperature can also be performed more reliable. A design window for different DT technology application now can be depicted precisely by utilizing our ZTC modeling, as shown in Fig. 4.25. For high performance operation, the ZTC point would be higher due to increase of power supply voltage. In addition, the higher alpha ratio provides better subthreshold swing and DIBL effect for device characteristics. As a result, we give results sufficiently accurate to predict the ZTC behaviors of DTMOS.

4.4 Summary

Analytical expressions of zero-temperature-coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail. The maximum error smaller than 1% are obtained in the linear and saturation regions, respectively, confirms the good agreement between our DTMOS ZTC point model and experimental data. In addition, we also establish the fixed body-bias ZTC modeling, simultaneously. The detail physical insights and expressions are also summarized in Table 4.1. The proposed formulations are useful for future integrated circuit design using DT technology.

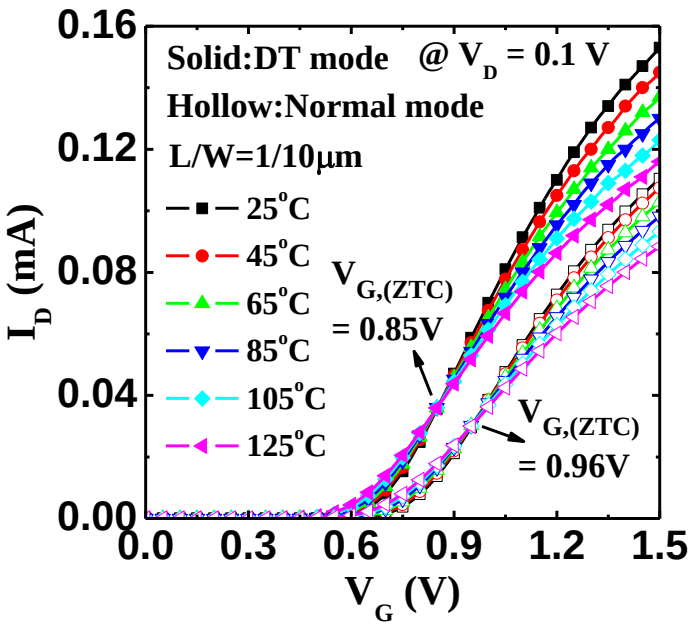


Fig. 4.1 I_D-V_G characteristics and ZTC point of NMOS under normal and DT-modes at elevated temperature from 298 K to 398 K, respectively.

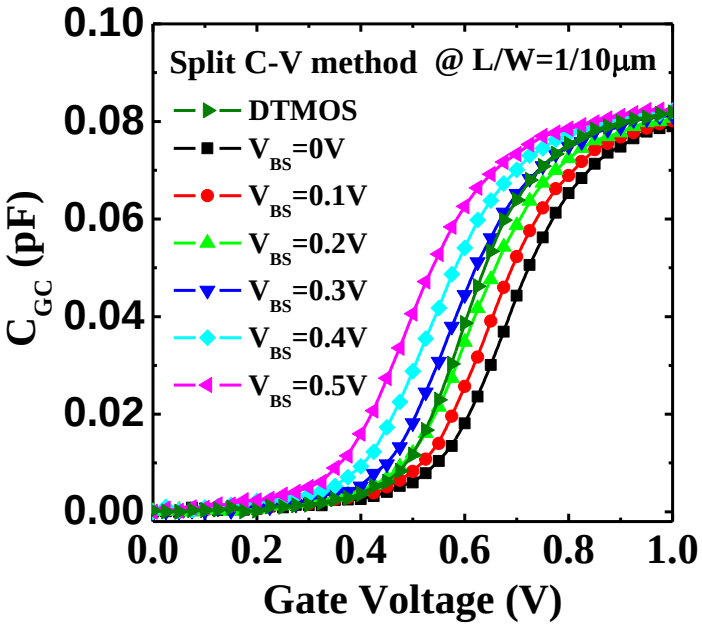


Fig. 4.2 C_{GC} characteristics of NMOS extracted from split C-V method under fixed body-bias and DT-modes at 298 K, respectively.

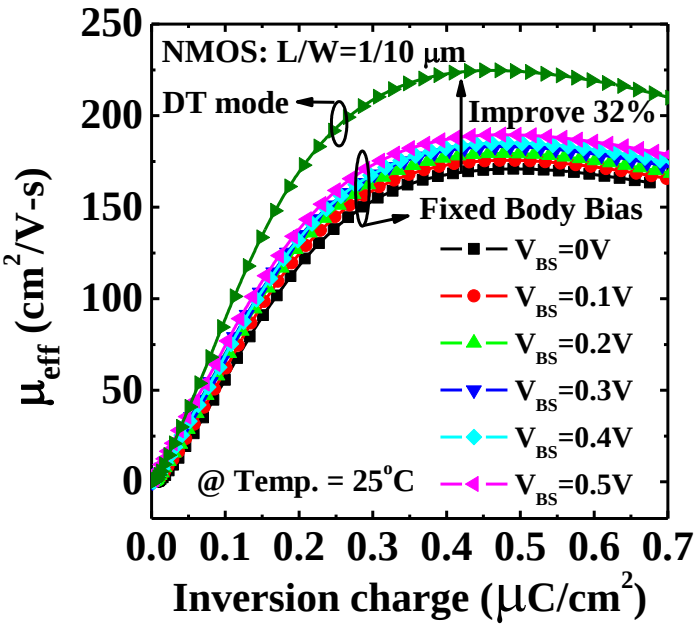


Fig. 4.3 Effective mobility versus surface charge density of NMOS under fixed body-bias and DT-modes at 298 K, respectively.

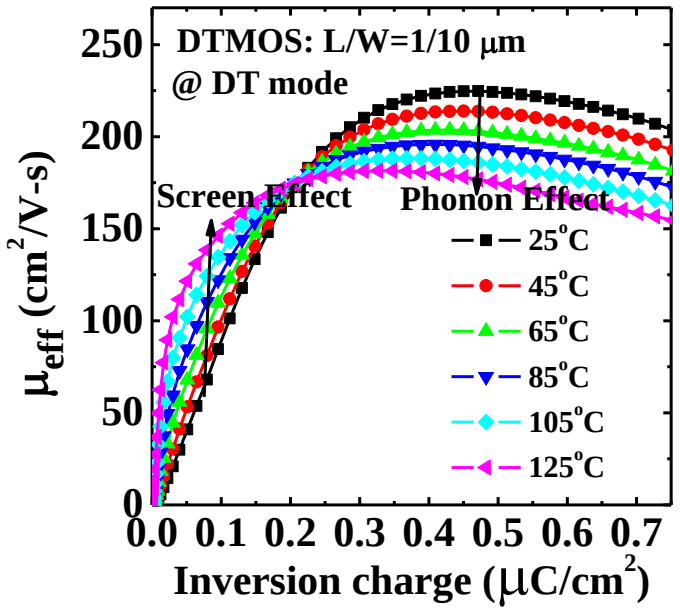


Fig. 4.4 Effective mobility versus surface charge density of NMOS under DT-mode at elevated temperature from 298 K to 398 K, respectively.

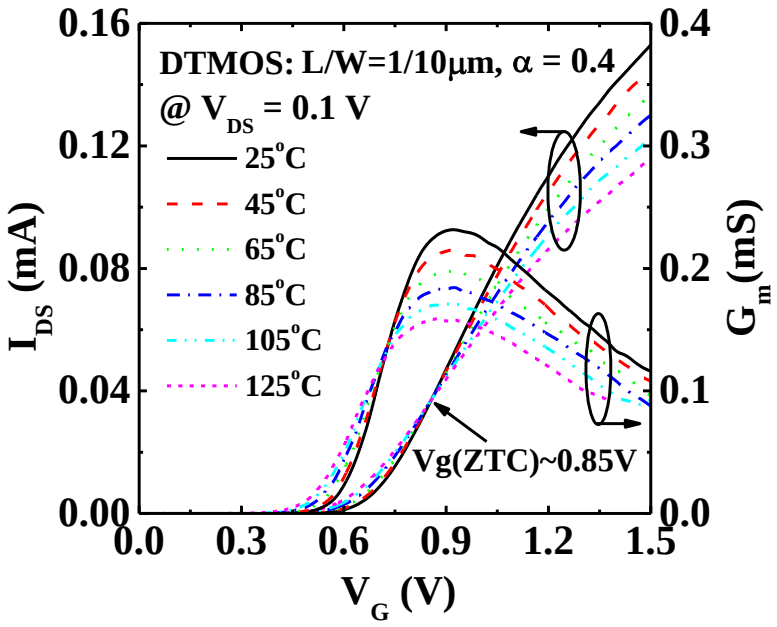


Fig. 4.5 I_D-V_G, G_m characteristics and ZTC point of Poly/SiO_2 DTMOS under DT-mode at elevated temperature from 298 K to 398 K, respectively.

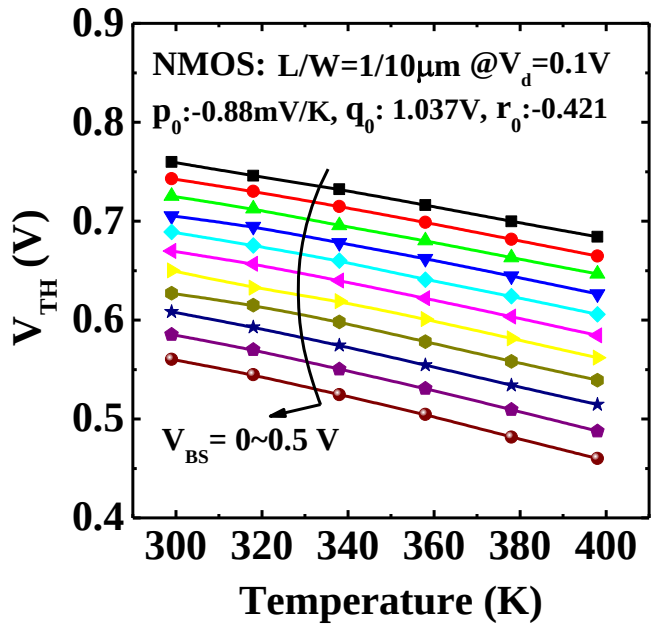


Fig. 4.6 Temperature dependence of V_{TH} under fixed body-bias mode at elevated temperature from 298K to 398K.

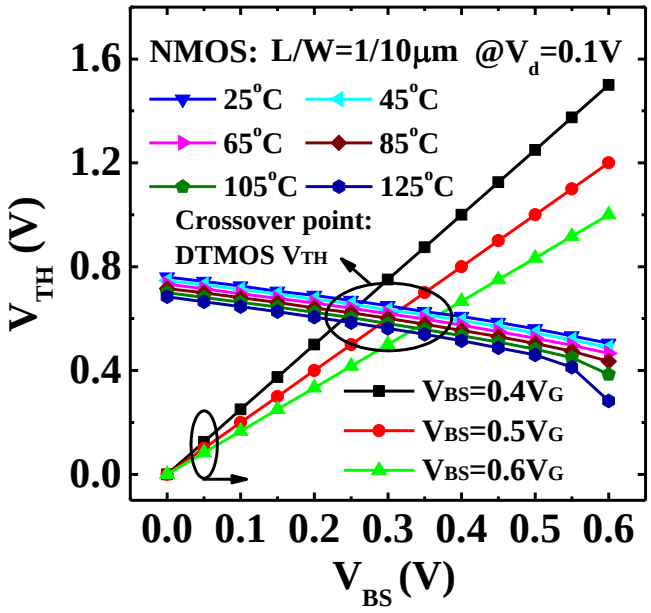


Fig. 4.7 Body bias dependence of V_{TH} with different temperature from 298K to 398K under fixed body-bias mode, respectively.

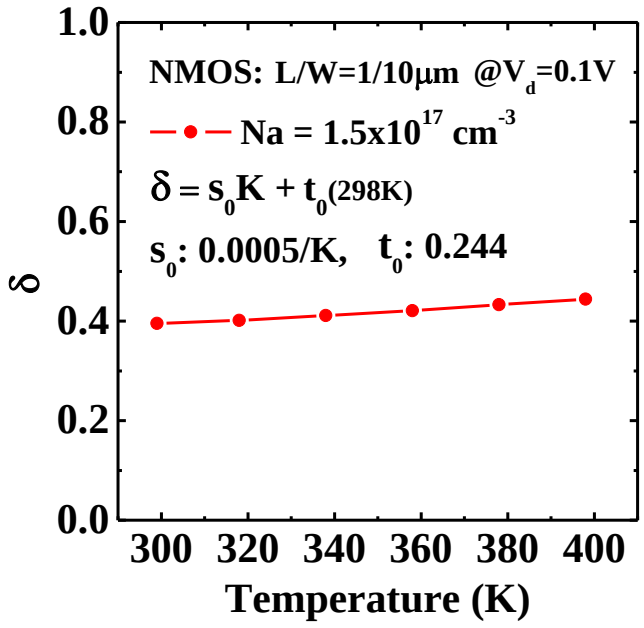


Fig. 4.8 Temperature dependence of body factor of Poly/SiO_2 NMOS at elevated temperature from 298K to 398K.

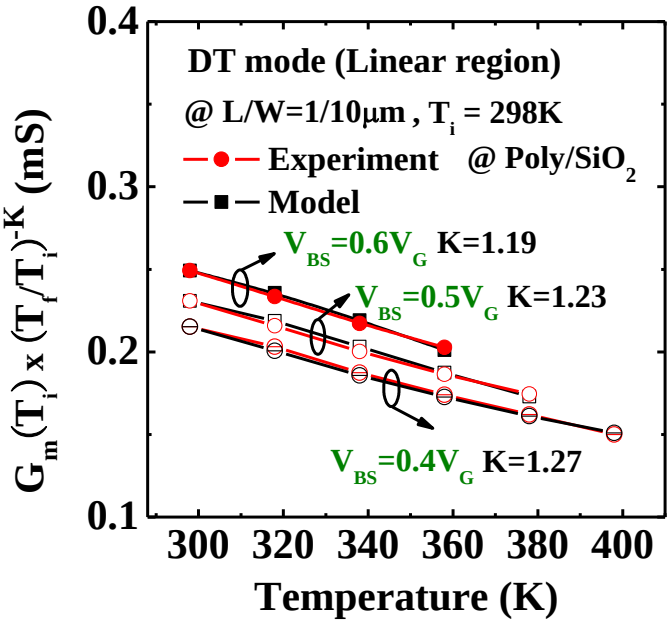


Fig. 4.9 Extraction of mobility degradation factor K_1 and our prediction model of Poly/SiO_2 with different alpha ratios in linear region.

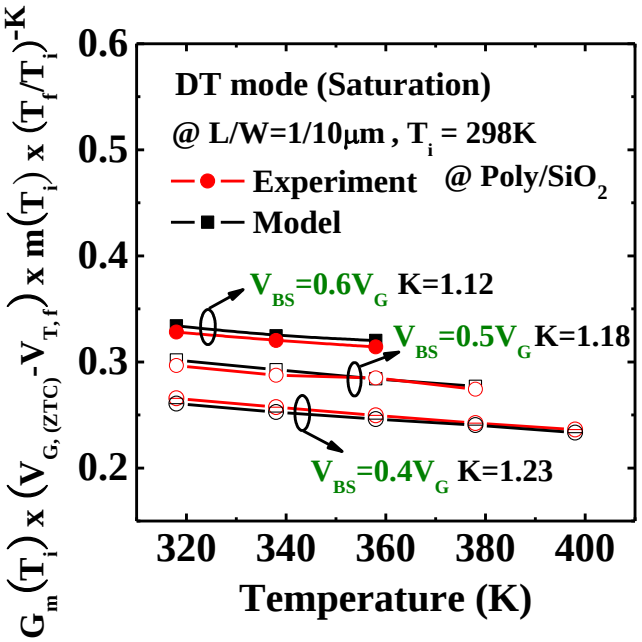


Fig. 4.10 Extraction of mobility degradation factor K_1 and our prediction model of Poly/SiO_2 with different alpha ratios in saturation region.

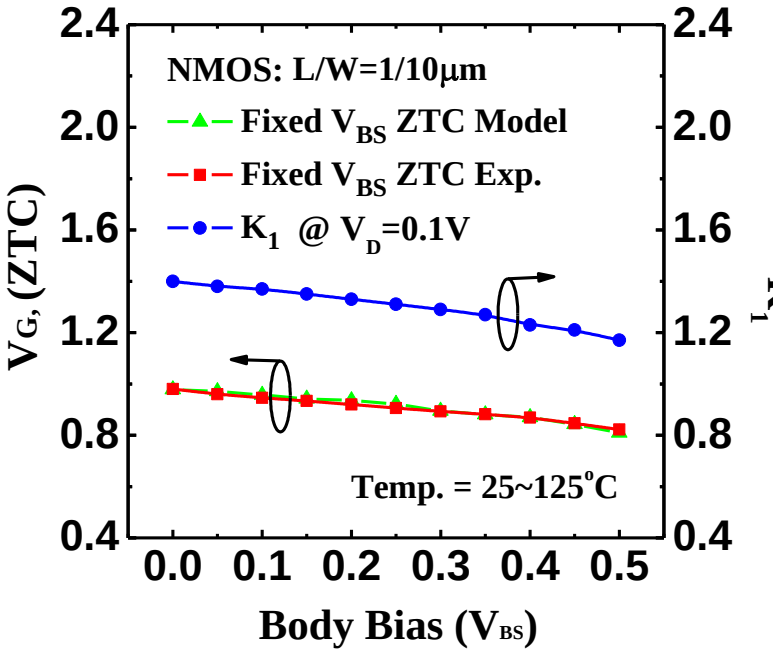


Fig. 4.11 Both $V_{G,(ZTC)}$ point of fixed body-bias mode and mobility degradation factor K_1 dependence of forward body-bias at elevated temperature from 298K to 398K.

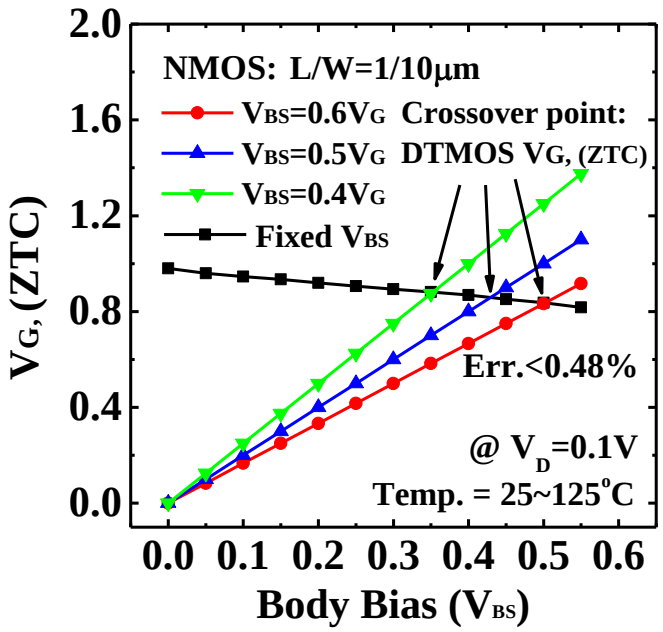


Fig. 4.12 The $V_{G,(ZTC)}$ point dependence of forward body-bias of Poly/SiO_2 NMOS with different alpha ratios at elevated temperature from 298K to 398K. Crossover points shows the of $V_{G,(ZTC)}$ point DTMOS.

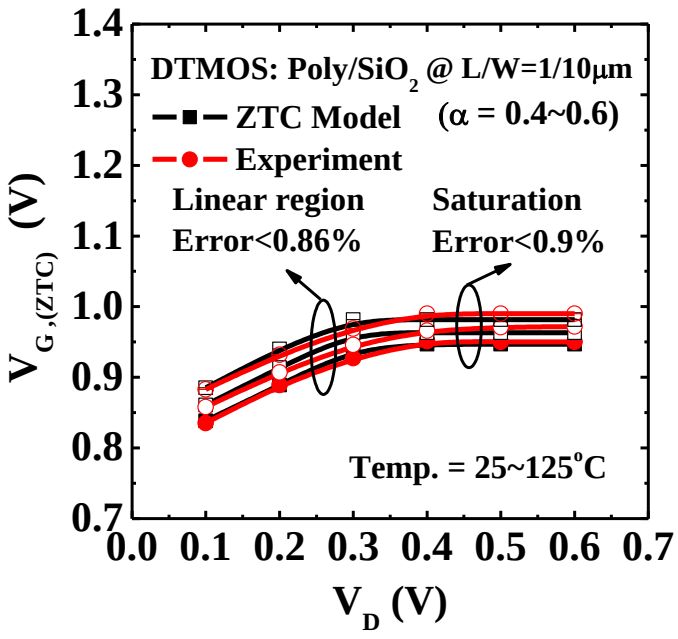


Fig. 4.13 The theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor with different alpha ratios in both the linear and saturation regions, respectively.

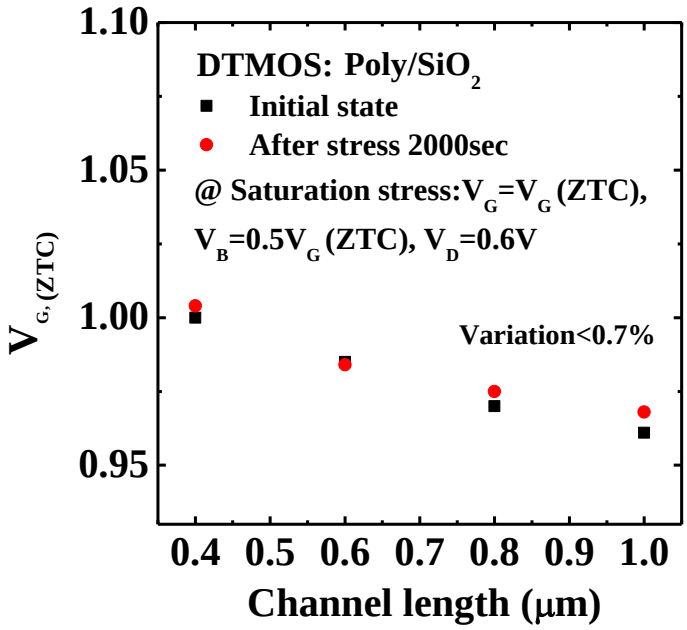


Fig. 4.14 Reliability characteristics of NMOS ZTC point under DT mode with different channel length after 2000sec stress.

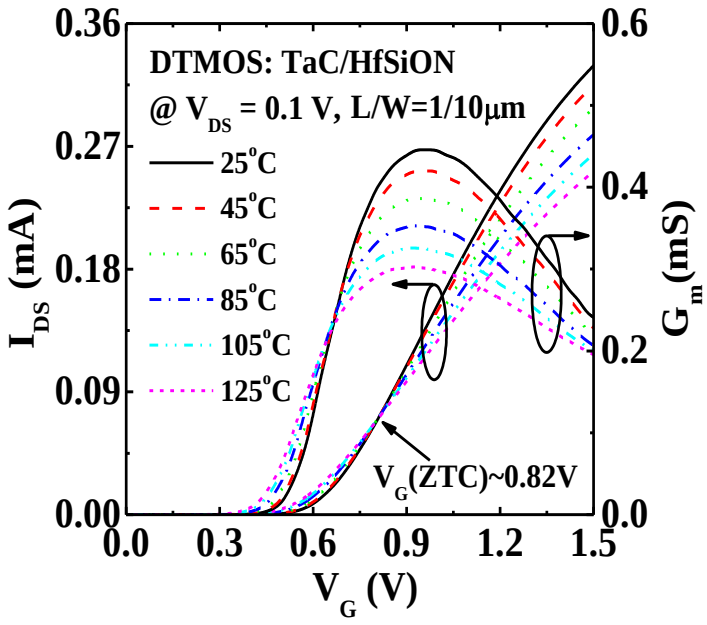


Fig. 4.15 I_D-V_G, G_m characteristics and ZTC point of TaC/HfSiON NMOS under DT-mode at elevated temperature from 298 K to 398 K, respectively.

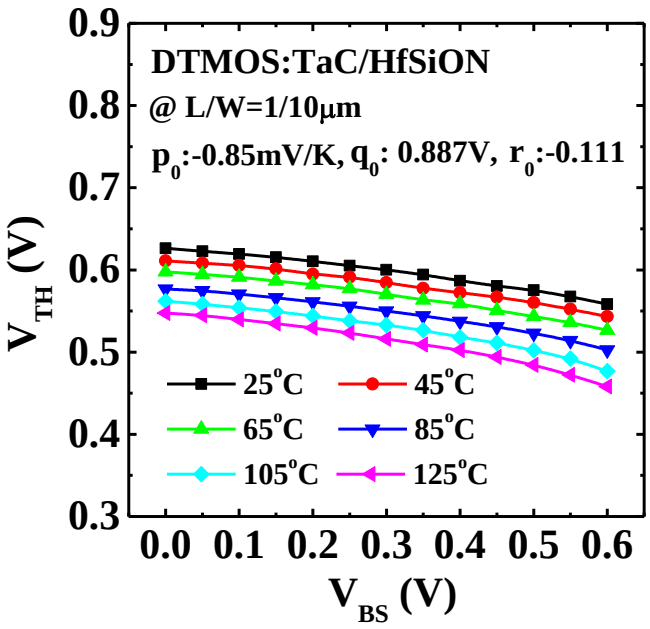


Fig. 4.16 Body bias dependence of V_{TH} of TaC/HfSiON NMOS with different temperature from 298K to 398K under fixed body-bias mode, respectively.

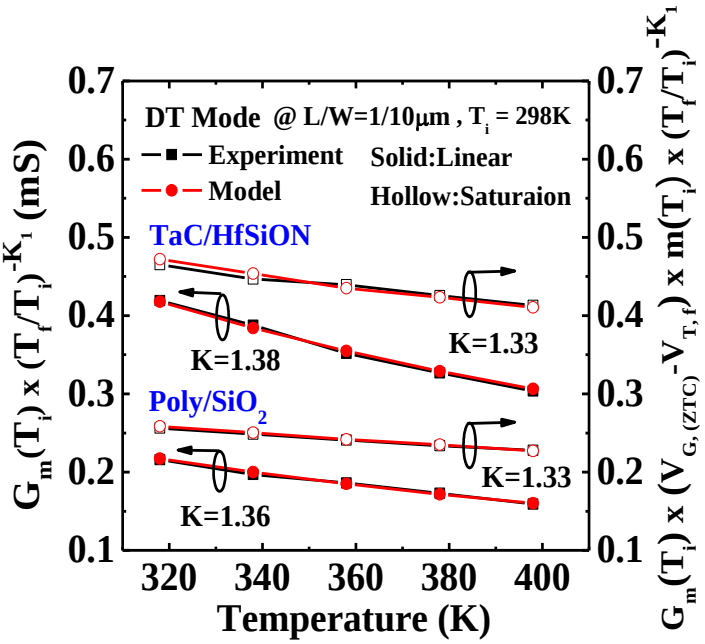


Fig. 4.17 Extraction of mobility degradation factor K_1 and our prediction model of TaC/HfSiON and Poly/SiO_2 gate stacks for long channel device in linear and saturation region, respectively.

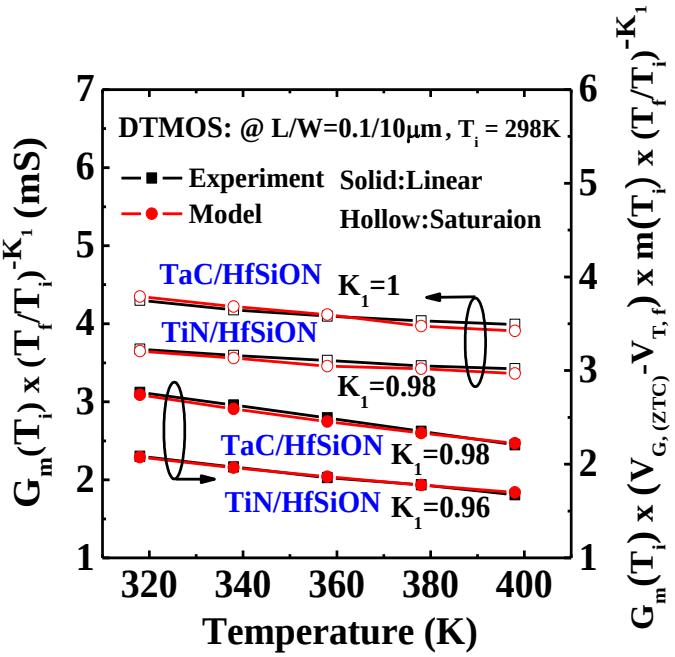


Fig. 4.18 Extraction of mobility degradation factor K_1 and our prediction model of TaC/HfSiON and TiN/HfSiON gate stacks for short channel device in linear and saturation region, respectively.

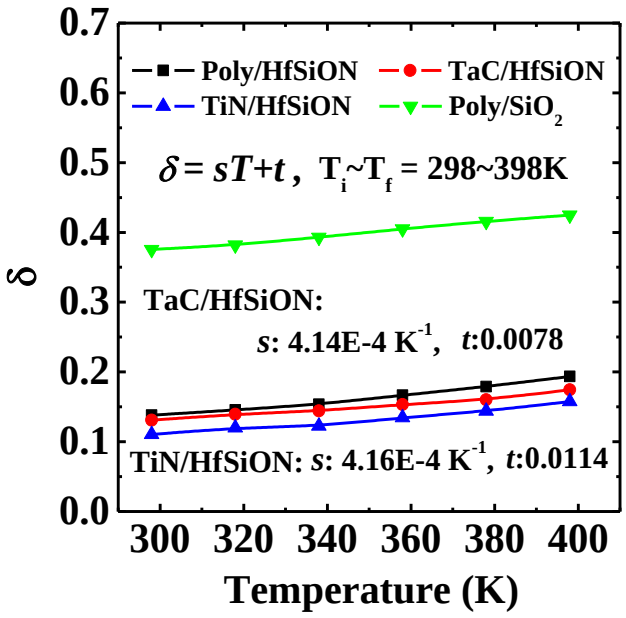


Fig. 4.19 Temperature dependence of body factor of poly/HfSiON, TaC/HfSiON and TiN/HfSiON gate stacks at elevated temperature from 298K to 398K.

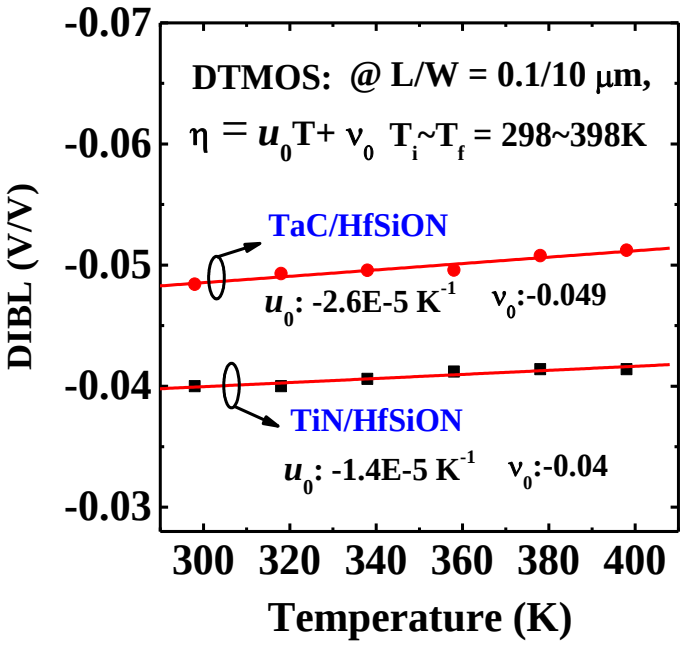


Fig. 4.20 Temperature dependence of DIBL effect of TaC/HfSiON and TiN/HfSiON gate stacks at elevated temperature from 298K to 398K.

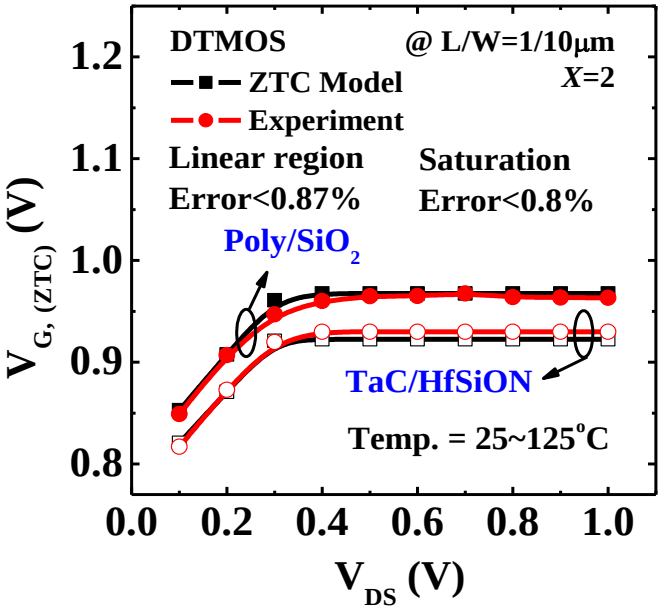


Fig. 4.21 The theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor for long channel device in both the linear and saturation regions, respectively.

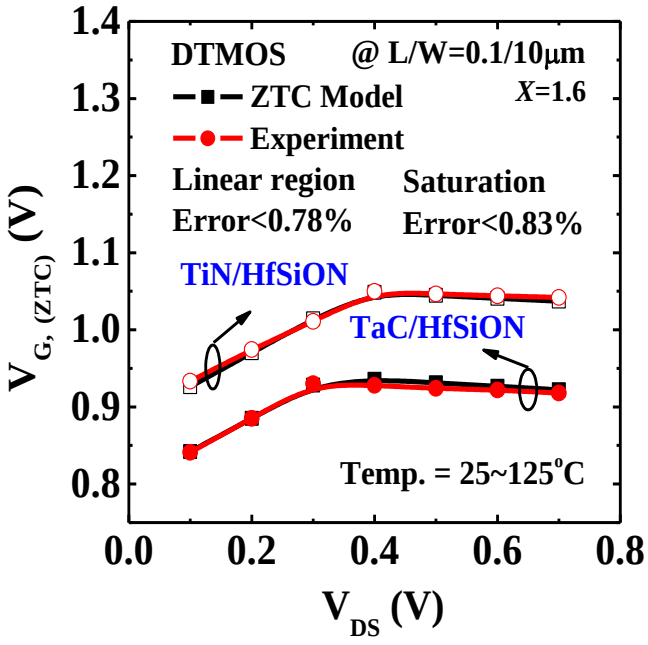


Fig. 4.22 The theoretical values of the ZTC point model and actual experimental data of the DTMOS transistor for short channel device in both the linear and saturation regions, respectively.

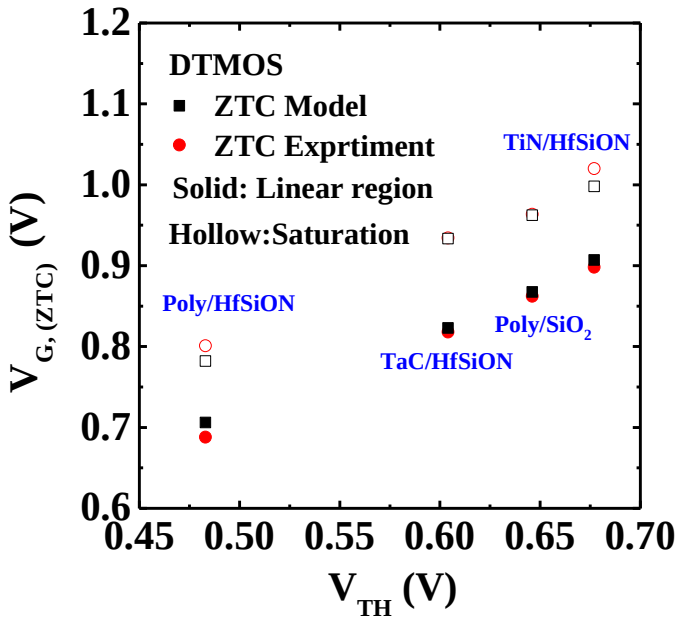


Fig. 4.23 Threshold voltage dependence of ZTC point of four gate-stacks system in linear and saturation region, respectively.

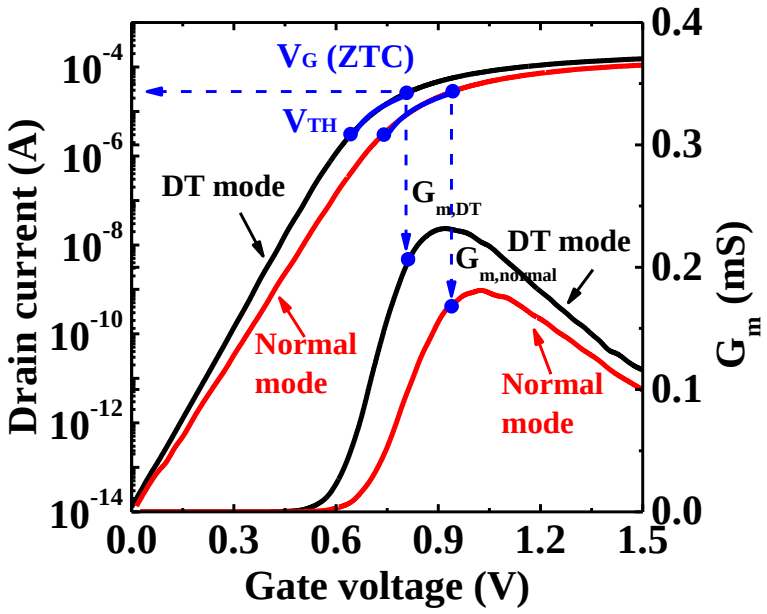


Fig. 4.24 A chart to demonstrate the differences and positions of ZTC point between normal and DT-modes.

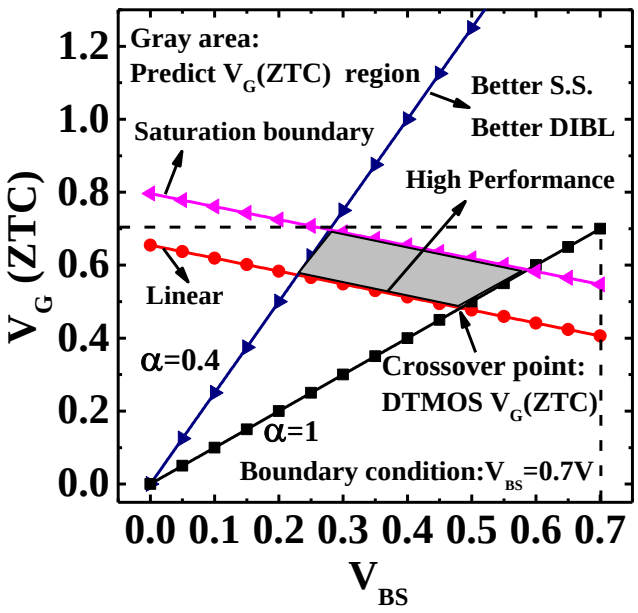


Fig. 4.25 The design windows of ZTC point of DTMOS with low stand-by power and high- performance characteristics.

Table 1. Drain current expressions:

Linear Regine: $I_{DS} = \frac{W}{L} C_{ox}\mu_n \left\{ (V_G - V_T(T, V_{BS}, V_{DS}))V_{DS} - \frac{m}{2} V_{DS}^{\ 2} \right\}$ Saturation Regine: $I_{DS} = \frac{W}{L} C_{ox}\mu_n \frac{(V_G - V_T(T, V_{BS}, V_{DS}))^2}{m}$

Body Effect Coefficient: $m = 1 + \delta, \ \delta = -\frac{dV_T}{dV_{BS}} = \frac{1}{C_{ox}} \sqrt{\frac{q\varepsilon_{Si}N_a}{2(2\phi_{fp} - V_{BS})}}$

Table 2.

A. Fixed Body Bias Mode: $|V_{BS}| \geq 0$

Linear Regine: $V_G^{\ Llin}(ZTC) \cong \frac{\left(p_0 + uV_{DS} + \frac{sV_{DS}}{2}\right)\left(1 - \frac{1}{K_1}\right)(T_i + T_f) + V_{DS}(1 + t) + 2(q_0 + vV_{DS} + r_0V_{BS})}{2}$, $T_\delta = \frac{K_1(1 + t)}{s(1 + K_1)}$

Saturation Regine: $V_G^{\ Sat}(ZTC) \cong \frac{(p_0 + uV_{DS})\left(1 - \frac{x}{K_1 + 1}\right)(T_i + T_f) + 2(q_0 + vV_{DS} + r_0V_{BS}) - \frac{(p_0 + uV_{DS})T_\delta}{K_1}\left(\frac{2x}{K_1 + 1}\right)\left[1 - \frac{T_\delta}{(T_f - T_i)} \ln\left(\frac{T_f + T_\delta}{T_i + T_\delta}\right)\right]}{2}$

B. DT Mode: $V_{BS} = \alpha V_G \quad (0 < \alpha \leq 1)$

Linear Regine: $V_G^{\ Llin}(ZTC) \cong \frac{\left(p_0 + uV_{DS} + \frac{sV_{DS}}{2}\right)\left(1 - \frac{1}{K_1}\right)(T_i + T_f) + V_{DS}(1 + t) + 2(q_0 + vV_{DS})}{2(1 - \alpha r_0)}$, $T_\delta = \frac{K_1(1 + t)}{s(1 + K_1)}$

Saturation Regine: $V_G^{\ Sat}(ZTC) \cong \frac{(p_0 + uV_{DS})\left(1 - \frac{x}{K_1 + 1}\right)(T_i + T_f) + 2(q_0 + vV_{DS}) - \frac{(p_0 + uV_{DS})T_\delta}{K_1}\left(\frac{2x}{K_1 + 1}\right)\left[1 - \frac{T_\delta}{(T_f - T_i)} \ln\left(\frac{T_f + T_\delta}{T_i + T_\delta}\right)\right]}{2(1 - \alpha r_0)}$

Table. 4.1 The drain current expressions with ZTC point modeling under fixed body-bias and DT-modes in the linear and saturation, respectively.

Table 3.

Physical Insight: $V_T(T, V_{BS}, V_{DS}) \cong p_0 T + r_0 V_{BS} + \eta V_{DS} + q_0$ V_T variation induced by Temp. Effect, Body Effect, and DIBL Effect.

$I_D^{Sat.} \propto (V_{GS} - V_T)^X$ X: Power dependence term of ZTC point in saturation region

$\mu_n(T_f) = \mu_n(T_i)\left(\frac{T_f}{T_i}\right)^{-K_1}$ K_1: Mobility degradation factor induced by phonon scattering

Physical parameter extraction:

Temp. dependence parameter:

$p_0 = \left.\frac{dV_T}{dT}\right|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average}$ Temp. Effect $\delta \cong sT + t$ Body Factor, $\eta \cong uT + v$ DIBL Effect

$r_0 = \left.\frac{(V_{T2}(T, V_{BS2}, V_{DS}) - V_{T1}(T, V_{BS1}, V_{DS}))}{V_{BS2} - V_{BS1}}\right|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average}$ Body Effect $s = \left.\frac{d\delta}{dT}\right|_{T_i \sim T_f}$ $u = \left.\frac{d\eta}{dT}\right|_{T_i \sim T_f}$

$\eta = \left.\frac{(V_{T2}(T, V_{BS}, V_{DS2}) - V_{T1}(T, V_{BS}, V_{DS1}))}{V_{DS2} - V_{DS1}}\right|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average}$ DIBL Effect $t = \delta(T_i) - T_i \left.\frac{d\delta}{dT}\right|_{T=T_i}$ $v = \eta(T_i) - T_i \left.\frac{d\eta}{dT}\right|_{T=T_i}$

$q_0 = V_T(T_i, V_{BS}, V_{DS}) - r_0 V_{BS} - p_0 T_i - \eta V_{DS}\Big|_{T_i \sim T_f, V_{BS} < 0.6V}^{Average}$ Const. Term

Mobility degradation K_1 parameter:

$\frac{\mu_n(T_f)}{\mu_n(T_i)} = \frac{G_{m,\max}(T_f)}{G_{m,\max}(T_i)} = \left(\frac{T_f}{T_i}\right)^{-K_1}$ Linear Regine, $\frac{\mu_n(T_f)}{\mu_n(T_i)} = \frac{G_m(T_f)(V_{G,(ZTC)} - V_{T,f})m(T_f)}{G_m(T_i)(V_{G,(ZTC)} - V_{T,i})m(T_i)} = \left(\frac{T_f}{T_i}\right)^{-K_1}$ Saturation Regine.

Power dependence X parameter:

$\frac{I_{D,Sat.}(V_{GS2})}{I_{D,Sat.}(V_{GS1})} = \left(\frac{V_{GS2} - V_T}{V_{GS1} - V_T}\right)^X\Bigg|_{@\, V_{GS2} > V_{GS1} > V_{G,(ZTC)}}$

Table. 4.2 The detail physical insights of ZTC point modeling both under fixed body-bias and DT-modes.

Chapter 5

Conclusions and Recommendations for Future Research

5.1 Conclusions

Briefly, the dissertation has involved physical concept of DT technology with HK/MG MOSFET, WSG-SONOS memory and ZTC model. We describe the merits of DT technology with using experimental data and ISE simulation tool. Moreover, the definite physical insight dependence of elevated temperature is also discussed. Major contributions of each section in thus thesis are summarized as following:

First, the linearly extrapolated threshold voltage of the maximum transconductance method to extract V_{TH} of DTMOS is proposed and then a body effect coefficient extraction analytical expression of DTMOS called *m*-model includes physical insights is successfully presented in detail. It explains why the DTMOS shows very excellent gate control ability and quite low off-leakage from energy band diagram variation. By using our *m*-model, it provides an important physical meaning including threshold voltage and body effect coefficient factors for designing body doping profile and work function adjustment for advanced HK/MG short channel device. The different alpha ratio between gate and substrate can be used to achieve our requirement of circuit. In addition, we prove the channel effective mobility can be enhanced by reducing depletion charge under DT mode using split C-V method. The un-ideal short channel including V_{TH} roll-off and DIBL effect would also be improved resulting in lower carrier ballistic transport coefficient and higher injection velocity from source terminal. The higher overdrive of HK/MG device can be still achieved by DTMOS.

Second, a novel dynamic-threshold source-side injection (DTSSI) in WSG-SONOS memory with high performance and reliable multilevel application for 2-bit/cell operation is successfully demonstrated, for the first time. We have investigated the programming mechanism of DTSSI in detail using the experimental data and Integrated Systems Engineering (ISE) TCAD simulation tools. It shows that the supply current (I_{SG}), and the lateral and vertical electric fields adjacent to neutral gap region are the three major factors affecting programming efficiency under DTSSI programming mode. We prove the higher programming efficiency to support high-speed multilevel operation with quite low power consumption can be performed

by appropriate operating voltages for the WSG-SONOS memory. Moreover, the greater noise margin between each level state provides higher flexibility for sensor amplification in circuit design with using DTSSI to achieve programming process. Further, we also found that the interferences of second bit effect may be almost ignored when operating 2-bit/cell utilizing DT mode in our device. The superior data retention and excellent endurance characteristics indicate the high potential of the WSG-SONOS memory programmed with DTSSI for high-reliability and high-performance embedded memory applications in the green technology.

Finally, for the first time, the new analytical expressions of zero-temperature-coefficient (ZTC) point modeling of DTMOS transistor are successfully presented in detail for both long and short channel device. The maximum error lower than 1% is obtained in the linear and saturation regions, respectively, confirms the good agreement between our DTMOS ZTC point model and experimental data. Moreover, we also establish the fixed body-bias ZTC modeling, simultaneously. The detail physical insights and expressions are also summarized in Table 4.1. The proposed formulations are useful for future integrated circuit design using DT technology.

5.2 Recommendation for Future Research

There are some still unknown physical insights to be studied for future work. Here are some suggestions as shown as following:

As detailed in our work, the body effect coefficient and metal gate work function choosing are the key factors for high performance with low power consumption application. To enhance the overdrive current for higher body effect coefficient factor, the body doping concentration and profile need to be controlled carefully. However, the doping fluctuation effect in very short channel device is a critical issue due to its depletion charge effect dependence of threshold voltage. Although the retrograde doping profile is used to improve the phenomenon, the threshold voltage variation affects in deep sub-micron DTMOS is still unclear. As a result, the detail process effect for discrete doping effect on V_{TH} is suggested to study with using simulation tools. Furthermore, the adjustment of lower metal work function in DTMOS for very short channel device is also need to be collocated at the same time.

Besides, the mechanism of WSG-SONOS memory with using DTSSI

programming method to achieve multi-level with 2-bits/cell application is described clearly. However, the reliability effect of charge storage lateral spatial distribution with utilizing DTSSI programming method is still needed to be considered. Especially, after cycling effect stress, the serious damage both for tunnel oxide and interface would degrade the reliability resulting from trap-assist-tunneling effect. Once we can prove the lateral spatial distribution of electron injection is different to hot-hole injection by utilizing charge pumping method under different programming mode under, the excellent endurance and good retention of WSG-SONOS memory can be explained clearly. Moreover, the charge storage vertical spatial distribution with utilizing DTSSI programming method is needed to be considered, too. It concerns to the scaled-down issue for good control ability of short channel effect with decreasing charge trapping layer and oxide thickness. The storage nitride layer with silicon-dots has demonstrated its excellent reliability and performance for scaling device. Therefore, it can be predicted that charge storage layer of WSG-SONOS memory uses nitride layer with silicon-dots can further enhance its electrical characteristics. Moreover, replacing traditional blocking silicon dioxide layer with high-k material, such as Al_2O_3, HfO_2 and Gd_2O_3, is suggested to enhance electrical characteristic and reducing power supply voltage. Finally, the performance and reliability of WSG-SONOS memory operates at elevated temperature is suggested to study for its special wrapped-select-gate transistor in its structure. We proposed the DTMOS ZTC point modeling and detailed the physical insights may help WSG-SONOS memory to be more stable at different operation temperature in circuit level. Summary, our recommendations provide the feasibility of DT technology for future green MOSFET era.

References

Chapter 1

[1.1] "International Technology Roadmap for Semiconductors" 2010 update, published by the Semiconductor Industry Association.

[1.2] S. H. Lo, D. A. Buchanan, Y. Taur and W. Wang, "Quantum-Mechanical Modeling of Electron Tunneling Current from the Inversion Layer of Ultra-Thin-Oxide nMOSFET's," IEEE Electron Device Lett., vol. 18, no. 5, pp. 209-211, 1997.

[1.3] R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros and M. Metz, "High-K/Meta-Gate Stack and Its MOSFET Characteristics," IEEE Electron Device Lett., vol. 25, no. 6, pp. 408-410, 2004.

[1.4] I. S. Han, W. H. Choi, H. M. Kwon, M. K. Na, Y. Y. Zhang, Y. G. Kim, J. S. Wang, C. Y. Kang, G. Bersuker, B. H. Lee, Y. H. Jeong, H. D.Lee and R. Jammy. "Time-Dependent Dielectric Breakdown of La_2O_3-Doped High-k Metal Gate Stacked NMOSFETs," IEEE Electron Device Lett., vol. 30, no. 3, pp. 298-301, 2009.

[1.5] M. Yamaguchi, T. Sakoda, H. Minakata, S. Xiao, Y. Morisaki, K. Ikeda and Y. Mishima. "Formation of HfSiON/SiO_2/Si-Substrate Gate Stack With Low Leakage Current for High-Performance High-k MISFETs," IEEE Trans. Electron Devices, vol. 53, no. 4, pp. 923-925, 2006.

[1.6] S. Agrawal and J. G.. Fossum. "On the Suitability of a High-k Gate Dielectric in Nanoscale FinFET CMOS Technology", IEEE Trans. Electron Devices, vol. 55, no. 7, pp. 1714-1719, 2008.

[1.7] H. H. Tseng, P. J. Tobin, S. Kalpat, J. K. Schaeffer, M. E. Ramon, L. R. C. Fonseca, Z. X. Jiang, R. I. Hegde, D. H. Triyoso and S. Semavedam. "Defect

Passivation with Fluorine and Interface Engineering for Hf-Based High-k Metal Gate Stack Device Reliability and Performance Enhancement", IEEE Trans. Electron Devices, vol. 54, no. 12, pp. 3267-3275, 2007.

[1.8] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Sanavedam, W. J. Taylor, J. M. Grant, L. G. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H. H. Tseng, S. G.H. Anderson, B. E. White and P. J. Tobin. "Fermi-Level Pinning at The Polysilicon Metal Oxide Interface-Part I", IEEE Trans. Electron Devices, vol. 51, no. 6, pp. 971-977, 2004.

[1.9] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Sanavedam, W. J. Taylor, J. M. Grant, L. G. G. Dip, D. H. Triyoso, R. I. Hegde, D. C. Gilmer, R. Garcia, D. Roan, M. L. Lovejoy, R. S. Rai, E. A. Hebert, H. H. Tseng, S. G.H. Anderson, B. E. White and P. J. Tobin. "Fermi-Level Pinning at the Polysilicon Metal Oxide Interface-Part II", IEEE Trans. Electron Devices, vol. 51, no. 6, pp. 978-984, 2004.

[1.10] C. Y. Lu, T. C. Lu and R. Liu. "Non-Volatile Memory Technology-Today and Tomorrow", Proceedings of 13th IPFA, Singapore, pp. 18-23, 2006.

[1.11] K. Naruke, S. Taguchi, and M. Wada "Stress Induced Leakage Current Limiting to Scale Down EEPROM Tunnel Oxide Thickness," *IEDM Tech. Dig.*, pp. 424-427, 1988.

[1.12] G. Zhang, W. J. Yoo and C. H. Ling " Hot-Electron Capture for CHEI Programming in SONOS-Type Flash Memory Using High-k Trapping Layer", IEEE Trans. Electron Devices, vol. 55, no. 6, pp. 1502-1510, 2008.

[1.13] Y. Q. Wang, W. S. Hwang, G. Zhang, G. Samuda, Y. C. Yeo and W. J. Yoo. "Electrical Characteristics of Memory Devices With a High-k HfO_2 Trapping

Layer and Dual SiO_2/Si_3N_4 Tunneling Layer", IEEE Trans. Electron Devices, vol. 54, no. 10, pp. 2699-2705, 2007.

[1.14] S. J. Choi, J. W. Han, M. G. Jang, J. S. Kim, K. H. Kim, G. S. Lee, J. S. Oh, M. H. Song, Y. C. Park, J. W. Kim and Y. K. Choi. "High Injection Efficiency and Low-Voltage Programming in a Dopant-Segregated Schottky Barrier (DSSB) FinFET SONOS for nor-type Flash memory", IEEE Trans. Electron Devices, vol. 30, no. 3, pp. 265-268, 2009.

[1.15] H.T. Lue, S.Y. Wang, E.K. Lai, Y.H. Shih, S.C. Lai, L.W. Yang, K.C. Chen, J. Ku, K.Y. Hsieh, R. Liu and C.Y. Lu "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," *IEDM Tech. Dig.*, pp. 547-550, 2005.

[1.16] H.T. Lue, S.Y. Wang, E.K. La, K.Y. Hsieh, R. Liu and C. Y. Lu. "A BE-SONOS (Bandgap Engineered SONOS) NAND for Post-Floating Gate Era Flash Memory," *VLSI Tech. Dig.*, pp. 1-2, 2007.

[1.17] B. Eitan, P.Pavan, I. Bloom, E. Aloni, A. Frommer and D. Finzi. "NROM: A Novel Localized Trapping, 2-bit Nonvolatile Memory Cell," *IEEE Electron Device Lett.*, vol. 21, no. 11, pp. 543-545, 2000.

[1.18] Y. W. Chang, T.C. Lu, S. P. and C.Y. Lu. "Modeling for the 2nd-bit effect of a Nitride-Based Trapping Storage Flash EEPROM Cell under Two-Bit Operation," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 95-97, 2004.

[1.19] H. T. Lue, T. H. Hsu, M. T. Wu, K. Y. Hsieh, R. Liu and C. Y. Lu. "Studies of the Reverse Read Method and Second-Bit Effect of 2-Bit/Cell Nitride-Trapping Device by Quasi-Two-Dimensional Model," *IEEE Trans. Electron Devices*, vol. 53, no. 1, pp. 119-125, 2006.

[1.20] Z. L. Huo, J. K. Yang, S. H. Lim, S. J. Baik, J. Lee, J. H. Han, I. S. Yeo, U. I.

Chung, J. T. Moon, B. I. Ryu “Band Engineered Charge Trap Layer for Highly Reliable MLC Flash Memory,” *VLSI Tech. Dig.*, pp. 138-139, 2007.

[1.21] M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, M. Ishac, J. Javanifard, M. Landgraf, D. Leak, K. Loe, D. Mills, P. Ruby, R. Rozman, S. Sweha, S. Talreja and K. Wojciechowski. “A Multilevel-Cell 32 Mb Flash Memory,” *IEEE Solid-State Circuit Conference, Tech. Dig*, pp 132-133, 1995.

[1.22] Y. H. Ha, J. H. Yi, H. Horii, J. H. Park, S. H. Joo, S. O. Park, U. I. Chung, J. T. and Moon “An Edge Contact Type Cell for Phase Change RAM Featuring Very Low Power Consumption”, *VLSI Tech. Dig.*, pp. 175-176, 2003.

[1.23] S. Tehrani, J. M. Slaughter, E. Chen, M. Durlam, J. Shi, and M. DeHerrera. “Progress and Outlook for MRAM Technology”, *IEEE Trans. Magnetics*, vol. 35, no. 5, pp. 2814-2819, 1999.

[1.24] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko and C. Hu. “Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI”, *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414-422, 1997.

[1.25] J. B. Kuo, K. H. Yuan and S. C. Lin. “Compact Threshold-Voltage Model for Short-Channel Partially-Depleted (PD) SOI Dynamic-Threshold MOS (DTMOS) Devices”, *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 190-196,. 2002.

[1.26] M. Takamiya and T. Hiramoto. “High Drive-Current Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body Effect and Low Threshold Voltage”, *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1633-1640, 2001.

Chapter 2

[2.1] F. Assaderaghi, D. Sinitsky, S.A. Parke, J. Bokor, P.K. Ko and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414-422, 1997.

[2.2] M. E. Hwang and K. Roy "A 135mV 0.13μW Process Tolerant 6T Subthreshold DTMOS SRAM in 90nm Technology," *in proceeding of IEEE Custom Integrated Circuit Conference (CICC)*, pp. 419-422, Sep. 2008.

[2.3] F. M. Yasin, Y. K. Teh, M. B. I. Reaz and A. Kordesch "Developing Designs For RFID Transponder Using DTMOS," *Microwaves and RF*, pp. 70-80, 2007.

[2.4] M. Maymandi-Nejad and M. Sachdev "DTMOS Technique for Low-Voltage Analog Circuits," *IEEE Trans. on Very Large Scale Integration (VLSI) systems*, vol. 14, no. 10, pp. 1151-1156, 2006.

[2.5] K. T. Wang, W. C. Lin and T. S. Chao, "The Zero-Temperature-Coefficient Point Modeling of DTMOS in CMOS Integration," *IEEE. Electron Device Lett.*, vol. 31, no. 10, pp. 1071-1073, 2010.

[2.6] Y. Momiyama, T. Hirose, H. Kurata, K. Goto, Y. Watanabe and T. Sugii "A 140 GHz ft and 60 GHz fmax DTMOS Integrated with High-Performance SOI Logic Technolgy," *IEDM Tech. Dig.*, pp. 451-454, 2000.

[2.7] Y. Taur and T. H. Ning "Fundamentals of Modern VLSI Devices," Cambridge University Press, 2009.

[2.8] D. K. Schroder "Semiconductor Material and Device Characterization," Wiley-Interscience publication, third edition, 2005.

[2.9] J. Li. And T. P. Ma, "Scattering of Silicon Inversion Layer Electrons by Metal/Oxide Interface Roughness," *Journal of Applied Physics*, vol. 62, no.

10, pp. 4212-4215, 1987.

[2.10] S. Saito, K. Torii, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, T. Mine, D. Hisamoto, T. Onai, J. Yugami, M. Hiratani and S. Kimura, "Effects of Remote-Surface-Roughness Scattering on Carrier Mobility in Field-Effect-Transistors with Ultrathin Gate Dielectrics," *Appl. Phys. Lett.*, vol. 84, no. 8, pp. 1395-1397, 2004.

[2.11] F. Y. Yen, C. L. Hung, Y. T. Hou, P. F. Hsu, V. S. Chang, P. S. Lim, L. G. Yao, J. C. Jiang, H. J. Lin, C. C. Chen, Y. Jin, S. M. Jang, H. J. Tao, S. C. Chen and M. S. Liang, "Effective Work Function Engineering of TaxCy Metal Gate on Hf-based Dielectrics", *IEEE, Electron Device Lett.*, vol. 28, no. 3, pp. 201-203, 2007.

[2.12] Y. T. Hou, F. Y. Yen, P. F. Hsu, V. S. Chang, P. S. Lim, C. L. Hung, L. G. Yao, J. C. Jiang, H. J. Lin, Y. Jin, S. M. Jang, H. J. Tao, S. C. Chen and M. S. Liang, "High Performance Tantalum Carbide Metal Gate Stacks for NMOS Application", *IEDM Tec. Dig*.,pp. 31-34, 2005.

[2.13] P. F. Hsu, Y.T. Hou, F.Y. Yen, V.S. Chang, P.S. Lim, C.L. Hung, L.G. Yao, J.C. Jiang, H.J. Lin, J.M. Chiou, K.M. Yin, J.J. Lee, R.L. Hwang, Y. Jin, S.M. Chang, H.J. Tao, S.C. Chen, M.S. Liang and T.P. Ma, "Advanced Dual Metal Gate MOSs with High-k Dielectric for CMOS Application", *IEDM Tec. Dig*., pp. 11-12, 2006.

[2.14] P. D. Kirsch, J. H. Song, S. Krishnan, J. Peterson, H. J. Li, M. Q. Lopez, C. D. Young, R. Choi, N. Moumen, P. Majhi, Q. Wang, J. G. Ekerdt, G. Bersuker and B. H. Lee, "Mobility Enhancement of High-k Gate Stacks Through Reduced Transient Charging", *Proceedings of Solid-State Device Research Conference, ESSDERC*., pp. 367-370, 2005.

[2.15] K. Tatsumural, M. Goto, S. Kawanaka, K. Nakajima, T. Schimizu, T. Ishihatal and M. Koyamal, “Clarification of Additional Mobility Components Associated with TaC and TiN Metal Gates in Scaled HfSiON MOSFETs Down to Sub-1.0nm EOT”, *IEDM Tec. Dig*.,pp. 349-352, 2007.

[2.16] M. Takamiya. and T. Hiramoto, “High Drive-Current Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body Effect and Low Threshold Voltage,” *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1633-1640, 2001.

[2.17] R. R. Troutman, “VLSI Limitation from Drain-Induced Barrier Lowering,” *IEEE Journal of Solid-State Circuits*, vol. 14, no. 2, pp. 383-391, 1979.

[2.18] A. A. Mutlu and M. Rahmud, “Two-Dimensional Analytical Model for Drain-Induced Barrier Lowering (DIBL) in Short Channel MOSFETs,” *in proceeding of IEEE Southeast Conference*, pp. 340-344, Sep. 2000..

[2.19] Z. H. Liu, C. Hu, J. H. Huang, T. Y. Chan, M. C. Jeng, P. K. Ko and Y. C. Cheng, “Threshold Voltage Model for Deep-Submicrometer MOSFET’s ,” *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 86-95, Jan. 1993.

[2.20] M. Lundstorm, “Elementary Scattering Theory of the Silicon MOSFET ,” *IEEE Electron Devices Lett.*, vol. 18, no. 7, pp. 361-363, 1997.

[2.21] M. J. Chen, H. T. Huang, K. C. Huang, P. N. Chen, C. S. Chang and C. H. Diaz, “Temperature Dependence Channel Backscattering Coefficients in Nanoscale MOSFETs,” *IEDM Tech. Dig.*, pp. 39-42, 2002.

[2.22] A. Lochtefeld and D. A. Antoniadis, “On Experimental Determination of Carrier Velocity in Deeply Scaled NMOS:How Close to the Thermal Limit? ,” *IEEE Trans. Electron Devices*, vol. 22, no. 2, pp. 95-97, 2001.

Chapter 3

[3.1] C. Y. Lu, T. C. Lu, and R. Liu "Non-Volatile Memory Technology - Today and Tomorrow," *IPFA Proc.*, PP 18-23, 2006.

[3.2] K. Naruke, S. Taguchi, and M. Wada "Stress Induced Leakage Current Limiting to Scale Down EEPROM Tunnel Oxide Thickness," *IEDM Tech. Dig.*, pp. 424-427, 1988.

[3.3] J. H. Park, S. H. Hur, J. H. Leex, J. T. Park, J.S. Sel, J. W. Kim, S. B. Song, J. Y. Lee, J. H. Lee, S. J. Son, Y. S. Kim, M. C. Park, S. J. Chai, J. D. Choi, U. I. Chung, J. T. Moon, K. T. Kim, K. Kim and B. I. Ryu "8 Gb MLC (multi-level cell) NAND Flash Memory Using 63 nm Process Technology," *IEDM Tech. Dig.*, pp. 873-876, 2004.

[3.4] R. Degraeve, F. Schuler, B. Kaczer, M. Lorenzini, D. Wellekens, P. Hendrickx, M.V. Duuren, G.J.M. Dormans, J.V. Houdt, L. Haspeslagh, G. Groeseneken and Tempel, G. "Analytical Percolation Model for Predicting Anomalous Charge Loss in Flash Memories," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1392-1400, Sep. 2004.

[3.5] H. T. Lue, S. Y. Wang, E. K. Lai, Y. H. Shih, S. C. Lai, L. W. Yang, K. C. Chen, J. Ku, K. Y. Hsieh, R. Liu and C. Y. Lu "BE-SONOS: A Bandgap Engineered SONOS with Excellent Performance and Reliability," *IEDM Tech. Dig.*, pp. 547-550, 2005.

[3.6] H. T. Lue, S. Y. Wang, E. K. La, K. Y. Hsieh, R. Liu and C. Y. Lu. "A BE-SONOS (Bandgap Engineered SONOS) NAND for Post-Floating Gate Era Flash Memory," *VLSI Tech. Dig.*, pp. 1-2, 2007.

[3.7] B. Eitan, P.Pavan, I. Bloom, E. Aloni, A. Frommer and D. Finzi. "NROM: A Novel Localized Trapping, 2-bit Nonvolatile Memory Cell," *IEEE Electron*

Device Lett., vol. 21, no. 11, pp. 543-545, Nov. 2000.

[3.8] Y. W. Chang, T. C. Lu, S. P. and C. Y. Lu. "Modeling for the 2nd-bit Effect of a Nitride-Based Trapping Storage Flash EEPROM Cell Under Two-Bit Operation," *IEEE Electron Device Lett.*, vol. 25, no. 2, pp. 95-97, 2004.

[3.9] H. T. Lue, T. H. Hsu, M. T. Wu, K. Y. Hsieh, R. Liu and C.Y. Lu. "Studies of the Reverse Read Method and Second-Bit Effect of 2-Bit/Cell Nitride-Trapping Device by Quasi-Two-Dimensional Model," *IEEE Trans. Electron Devices*, vol. 53, no. 1, pp. 119-125, 2006.

[3.10] Z. L. Huo, J. K. Yang, S. H. Lim, S. J. Baik, J. Lee, J. H. Han, I. S. Yeo, U. I. Chung, J. T. Moon, B. I. Ryu "Band Engineered Charge Trap Layer for highly Reliable MLC Flash Memory," *VLSI Tech. Dig.*, pp. 138-139, 2007.

[3.11] M. Bauer, R. Alexis, G. Atwood, B. Baltar, A. Fazio, K. Frary, M. Hensel, M. Ishac, J. Javanifard, M. Landgraf, D. Leak, K. Loe, D. Mills, P. Ruby, R. Rozman, S. Sweha, S. Talreja and K. Wojciechowski. "A Multilevel-Cell 32 Mb Flash Memory," *IEEE Solid-State Circuit Conference, Tech. Dig*, pp 132-133, 1995.

[3.12] A. T. Wu, T. Y. Chan, P. K. Ko and C. Hu "A Novel High-Speed, 5-Volt Programming EPROM Structure with Source-Side Injection," *IEDM Tech. Dig.*, pp. 584-587, 1986.

[3.13] K. T. Chang, W. M. Chen, C. Swift, J. M. Higman, W. M. Paulson, and K. M. Chang "A New SONOS Memory Using Source-Side Injection for Programming," *IEEE Electron Device Lett.*, vol. 19, no. 7, pp. 253-255, 1998.

[3.14] L. Breuil, L. Haspeslagh, P. Blomme, D. Wellekens, J.D. Vos, M. Lorenzini, and J.V. Houdt "A New Scalable Self-Aligned Dual-Bit Split-Gate Charge-Trapping Memory Device," *IEEE Trans. Electron Devices*, vol. 52, no.

10, pp. 2250-2257, Oct. 2005.

[3.15] J. F. V. Houdt, G. Groeseneken and H. E. Maes “An Analytical Model for the Optimization of Source-Side Injection Flash EEPROM Devices,” *IEEE Trans. Electron Devices*, vol. 42, no. 7, pp. 1314-1320, Oct. 1995.

[3.16] A. T. Wu, T. Y. Chan, P. K. Ko and C. Hu “A Novel High-Speed, 5-Volt Programming EPROM Structure with Source-Side Injection,” *IEDM Tech. Dig.*, pp. 584-587, 1986.

[3.17] H. Tomiye, T. Terano, K. Nomoto and T. Kobayashi “A Novel 2-bit/cell MONOS Memory Device with a Wrapped-Control-Gate Structure that Applies Source-Side Hot-Electron Injection,” *VLSI Tech. Dig.*, pp. 206-207, 2002.

[3.18] C. Y. Lu, T. C. Lu, and R. Liu “Non-Volatile Memory Technology - Today and Tomorrow,” *IPFA Proc.*, PP 18-23, 2006.

[3.19] K. T. Wang, T. S. Chao, W. C. Wu, T. Y. Chiang, Y. H. Wu, W. L. Yang, C. H. Lee, T. M. Hsieh, J. C. Liou, S. D. Wang, T. P. Chen, C. H. Chen, C. H. Lin and H. H. Chen. “High-Speed Multilevel Wrapped-Select-Gate SONOS Memory Using a Novel Dynamic Threshold Source-Side-Injection (DTSSI) Programming Method,” *IEEE Electron Device Lett.*, vol. 30, no. 6, pp. 659-661, 2009.

[3.20] W. C. Wu, T. S. Chao, W. C. Peng, W. L. Yang, J. C. Wang, J. H. Chen, C. S. Lai, T. Y. Yang, C. H. Lee, T. M. Hsieh and J. C. Liou. “Highly Reliable Multilevel and 2-Bit/Cell Operation of Wrapped Select Gate (WSG) SONOS memory,” *IEEE Electron Device Lett.*, vol. 28, no. 3, pp. 214-216, 2007.

[3.21] K. T. Wang, T. S. Chao, W. C. Wu, and C. S. Lai. “The Polarity Dependence of ONO Thickness for Wrapped-Select-Gate (WSG) SONOS Memory,” *IEEE MTDT Proc.*, pp. 51-54, 2007.

[3.22] W. C. Wu, T. S. Chao, W. C. Peng, W. L. Yang, J. H. Chen, M. W. Ma, C. S. Lai, T. Y. Yang, C. H. Lee, T. M. Hsieh, J. C. Liou, T. P. Chen, C. H. Chen, C. H. Lin, H. H. Chen and J. Ko "Optimized ONO Thickness for Multi-Level and 2-Bit/Cell Operation for Wrapped Select-Gate (WSG) SONOS Memory," *Semicond. Sci. Technol.* vol. 23, no. 1, 015004, 2008.

[3.23] Y. Okuyama, T. Furukawa, T. Saito, Y. Nonaka, T. Ishimaru, K. Yasui, D. Hisamoto, Y. Shimamoto, S. Kimura, M. Mizuno, K. Toba, D. Okada, T. Hashimoto and K. Okuyama "Determination of Lateral Charge Distributions of Split-gate SONOS Memories Using Experimental Devices with Nanometer-size Nitride Piece," *NVSMW Proc.* , pp. 85, 2007.

Chapter 4

[4.1] I. M. Filanovsky and A. Allam, "Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits", *IEEE Trans. Circuits and Systems*, vol. 48, no. 7, pp. 876-884, 2001.

[4.2] F. S. Shoucair, "Design Consideration in High Temperature Analog CMOS Integrated Circuits", *IEEE Trans. Components, Hybrids, and Manufacturing Tec*., vol. 9, no. 3, pp. 242-251, 1986.

[4.3] F. S. Shoucair, "Analytical and Experimental Methods For Zero-Temperature-Coefficient Biasing of MOS Transistors", *IEEE Electronics Lett*., vol. 25, no. 17, pp. 1196-1198, 1989.

[4.4] F. Shoucair and W. Hwang, "Electrical Characteristics of Large Scale Integration (LSI) MOSFETs at Very High Temperature. (Part I: Theory)", *Microelectron. Reliab*, vol. 24, no. 3, pp. 465-485, 1984.

[4.5] F. Shoucair and W. Hwang, "Electrical Characteristics of Large Scale Integration (LSI) MOSs at Very High Temperature. (Part Π: Experiment)", *Microelectron. Reliab*, vol. 24, no. 3, pp. 465-485, 1984.

[4.6] F. Assaderaghi, D. Sinitsky, S. A. Parke, J. Bokor, P. K. Ko and C. Hu, "Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI," *IEEE Trans. Electron Devices*, vol. 44, no. 3, pp. 414-422, 1997.

[4.7] S. J. Chang, C. Y. Chang, C. Chen, T. S. Chao, Y. J. Lee and T. Y. Huang, "High-Performance and High-Reliability 80-nm Gate-Length DTMOS with Indium Super Steep Retrograde Channel," *IEEE Trans. Electron Devices*, vol. 47, no. 12, pp. 2379-2384, Dec. 2000.

[4.8] M. Takamiya. and T. Hiramoto, "High Drive-Current Electrically Induced Body Dynamic Threshold SOI MOSFET (EIB-DTMOS) with Large Body

Effect and Low Threshold Voltage," *IEEE Trans. Electron Devices*, vol. 48, no. 8, pp. 1633-1640, 2001.

[4.9] M. E. Hwang and K. Roy "A 135mV 0.13μW Process Tolerant 6T Subthreshold DTMOS SRAM in 90nm Technology," *in proceeding of IEEE Custom Integrated Circuit Conference (CICC)*, pp. 419-422, 2008.

[4.10] F. Mohd,-Yasin, Y. K. Teh, M. B. I. Reaz and A. Kordesch "Developing Designs For RFID Transponder Using DTMOS," *Microwaves and RF*, pp. 70-80, 2007.

[4.11] M. Maymandi-Nejad and M. Sachdev "DTMOS Technique for Low-Voltage Analog Circuits," *IEEE Trans. on Very Large Scale Integration (VLSI) systems*, vol. 14, no. 10, pp. 1151-1156, 2006.

[4.12] Z. D. Prijic, S. S. Dimitrijev and N. D. Stojadinovic, "The Determination of Zero Temperature Coefficient Point in CMOS Transistors," *Microelectron. Reliab.* vol. 32, no. 6, pp. 769-773, 1992.

[4.13] D. K. Schroder "Semiconductor Material and Device Characterization," Wiley-Interscience publication, third edition, 2005.

[4.14] Y. Taur and T. H. Ning "Fundamentals of Modern VLSI Devices," Cambridge University Press, 2009.

Publication List

International Journal:

[1] **Kuan-Ti Wang**, Tien-Sheng Chao, Woei-Cherng Wu, Wen-Luh Yang, Chien-Hsing Lee, Tsung-Min Hsieh, Jhyy-Cheng Liou, Shen-De Wang, Tzu-Ping Chen, Chien-Hung Chen, Chih-Hung Lin, and Hwi-Huang Chen, "High-Reliability Dynamic Threshold Source Side Injection (DTSSI) for 2-Bit/Cell with MLC Operation of Wrapped-Select-Gate SONOS (WSG-SONOS) in NOR-Type Flash Memory," *IEEE Transactions on Electron Devices*, Vol. 57, No. 9, pp. 2335-2338, September 2010.

International Letter:

[2] **Kuan-Ti Wang**, Tien-Sheng Chao, Woei-Cherng Wu, Tsung-Yu Chiang, Yi-Hong Wu, Wen-Luh Yang, Chien-Hsing Lee, Tsung-Min Hsieh, Jhyy-Cheng Liou, Shen-De Wang, Tzu-Ping Chen, Chien-Hung Chen, Chih-Hung Lin, and Hwi-Huang Chen "High-Speed Multi-level Wrapped-Select-Gate SONOS Memory Using A Novel Dynamic Threshold Source Side Injection (DTSSI) Programming Method" , *IEEE Electron Device Letter*, Vol. 30, No. 6, pp. 659-661, June 2009.

[3] **Kuan-Ti Wang,** Tien-Sheng Chao, Tsung-Yu Chiang, Woei-Cherng Wu, Po-Yi Kuo, Yi-Hong Wu, Yu-Lun Lu, Chia-Chun Liao, Wen-Luh Yang, Chien-Hsing Lee, Tsung-Min Hsieh, Jhyy-Cheng Liou, Shen-De Wang, Tzu-Ping Chen, Chien-Hung Chen, Chih-Hung Lin, and Hwi-Huang Chen "Physical Mechanism of High Programming Efficiency Dynamic Threshold Source Side Injection (DTSSI) in Wrapped-Select-Gate SONOS (WSG-SONOS) for NOR-Type Flash Memory", *IEEE Electron Device Letter,*

Vol. 30, No. 11, pp. 1206-1208, November, 2009.

[4] **Kuan-Ti Wang,** Wan-Chyi Lin and Tien-Sheng Chao "The Zero Temperature Coefficient (ZTC) Point Modeling of DTMOS in CMOS Integration", *IEEE Electron Device Letter*, No. 31, pp. 1071-1073, October. 2010.

International Conference:

[1] **Kuan-Ti Wang**, Tien-Sheng Chao, Woei-Cherng Wu and Chao-Sung Lai. " The Polarity Dependence of ONO Thickness for Wrapped-Select-Gate (WSG) SONOS Memory," *IEEE International Workshop on Memory Technology, Design and Testing*, December 3-5, 2007 (MTDT).

[2] **Kuan-Ti Wang,** Wan-Chyi Lin, and Tien Sheng-Chao. "The Compact Modeling of Zero Temperature Coefficient (ZTC) Point of DTMOS," *International Conference on Solid State Device and Material*, September 22-24, 2010 (SSDM).

Local Conference:

[1] **Kuan-Ti Wang,** Tien-Sheng Chao, Woei-Cherng Wu, Tsung-Yu Chiang, Yi-Hong Wu, Wen-Luh Yang, Chien-Hsing Lee, Tsung-Min Hsieh, Jhyy Cheng Liou, Shen De Wang, Tzu Ping Chen, Chien Hung Chen, Chih Hung Lin, and Hwi Huang Chen "High-Speed (100-ns) Multi-level Cell Wrapped-Select-Gate SONOS Memory Using Dynamic Threshold Source-Side-Injection (DTSSI) Programming Method" , *16th Symposium on Nano Device Technology*, April 29-30, 2008 (SNDT).

[2] **Kuan-Ti Wang,** Wan-Chyi Lin, and Tien-Sheng Chao, "The Zero-Temperature-Coefficient Point Modeling of DTMOS" , *18th Symposium on Nano Device Technology*, April 21-22, 2011 (SNDT).

簡 歷 (Vita)

姓名: 王冠迪

性別: 男

出生日: 1983 年 10 月 24 日

籍貫: 台灣 台南市

出生地: 台灣 高雄市

學歷: 私立長庚電子工程學系 學士班

2002 年 9 月-2006 年 6 月

國立交通大學電子物理學系 碩士班

2006 年 9 月-2008 年 6 月

國立交通大學電子物理學系 博士班

2008 年 9 月-2011 年 7 月

博士論文題目:

動態臨界電晶體之精簡物理模型與應用

Compact Physical-Based Model and Applications of Dynamic-Threshold-Metal-Oxide-Semiconductor