國　立　交　通　大　學

電機與控制工程研究所

碩　士　論　文

內建自我測試電路之管線化類比數位轉換器

Built-in Self-test Circuits For Pipeline Analog-to-Digital Converters

研究生：楊為朋

指導教授：蘇朝琴 教授

中華民國九十三年七月

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電機與控制工程學系

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內建自我測試電路之管線化類比數位轉換器

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摘　　要

在本論文中，主要的目標是設計管線化類比數位轉換器的內建自我測試電路。我們提出一新的測試方，依照每一級的取樣保持電路的輸出信號的機率統計，去計算出管線化類比數位轉換器每一級的抵補誤差和增益誤差。首先，設計一 8 位元,50 MS/s,四級的管線化類比數位轉換器。並測量其靜態行為，積分型非線性誤差，微分型非線性誤差,抵補誤差和增益誤差。然後，我們設計內建自我測試電路去量測管線化類比數位轉換器每一級的抵補誤差和增益誤差。把內建自我測試電路所測得的值和實際上管線化類比數位轉換器所量測的結果做比較。

Built-in Self-test Circuits for Pipeline Analog-to-Digital Converters

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ABSTRACT

In this thesis, our target is to design a built-in self-test circuit for the pipeline analog-to-digital converters. We propose a new approach. According to the probability of each stage sample-and-hold output signals, we can test the voltage offset error of each stage in pipeline analog-to-digital converters. First, we design a 8-bit, 50 MS/s and four stages pipeline analog-to-digital converters. And we measure the static characteristics which include differential nonlinearity error, integral nonlinearity error, offset error and gain error. Then, we measure offset error and gain error of each stage in pipeline analog-to-digital converters by built-in self-test circuits. Finally, we compare the result from built-in self-test circuits with the real value by measuring the pipeline analog-to-digital converters.

誌　　謝

由衷的感謝恩師蘇朝琴教授，指導著我兩年的研究生生涯。充實專業領域的知識，與及待人處事應有的方法。還有學得以嚴謹的態度從事科學研究，使我獲益良多。

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同時，我要感謝我的父母，一直支持著我，鼓勵著我，讓我可以專心完成我的學業。

楊為朋

2004/07

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Chapter 1

Introduction

1.1 Motivation

Due to development of *system-on-chip* (SOC), mixed-mode circuits are wildly used in many applications. Testing in the mixed-mode circuits are a big challenge. The main challenge derives from the fact that testing in the mixed-mode circuits is very expensive and time-consuming. Hence, we propose a *built-in self-test* (BIST) approach to solve the above difficulty. And, BIST can increases controllability and observability of testing.

As the VLSI technology advances, digital system operational and signals procession capability is more popularly. Analog circuits are more easily affected by noise, operational voltage, and manufacture than digital circuits. But in the environment, analog signals are touched, heard, and looked by human . For this reason, the *analog-to-digital* (A/D) interface is needed. The key technology in the analog-to-digital interface is high-resolution and high-speed analog-to-digital converters. The high-resolution *analog-to-digital converters* (ADC) are applied in many field, such as communication product, medical treatment instrument and so on.

First, we design a 8-bits, 50 MHz, pipeline ADC. It has the flash ADC advantage, high speed. And pipeline ADC can reduce chip area and power consumption.

Second, we propose a new idea for BIST circuits in the ADC. It uses probability to gather statistics to test the pipeline ADC. It can test each stage's voltage offset, Gain error.

1.2 Organization

This thesis is composed of six chapters. We introduced research motivation for ADC BIST in this chapter. In chapter 2, ADC are classified into three categories. We discuss their structure, operational and characteristics. BIST circuits of ADC are also discussed briefly. In chapter 3, we design a pipeline ADC. That includes sample-and-hold circuits, 3-bit flash ADC, 3-bit DAC, residue amplifier and digital error correction circuits. In chapter 4, we bring up new idea of BIST of ADC. It uses probability to collect statistics to test the pipeline ADC. In chapter 5, the circuits schemes of building block and their simulation results are presented. In chapter 6, conclusion and future work are given.

Chapter 2

Brief introduction of ADC and BIST

2.1 ADC Review

Analog-to-digital converters transforms analog signals to digital ones. In the analog input dynamic range, ADC transform it related digital output code. It is shown in Fig. 2-1. As shows in Fig. 2-1(a), it is a simple diagram of ADC. As shows in Fig. 2-1(b), it is a simple transfer curve of an ADC.

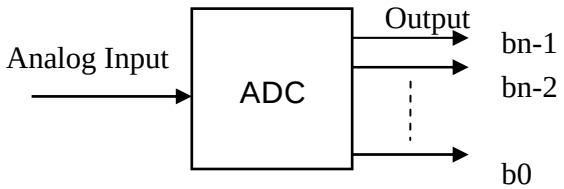


Fig. 2-1(a)

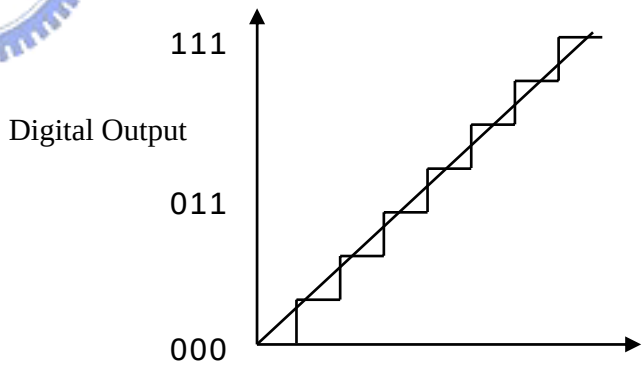


Fig. 2-1(b)

Fig. 2-1, Simple ADC circuits

There are four important parameters for static characteristics of ADC, *differential nonlinearity* (DNL), *integral nonlinearity* (INL), *offset error* (V_{os}) and *gain error* (G_e). By

testing the DNL, INL, offset error and gain error, the basic functionality of ADC can be verified.

Fig. 2-2 is an example for 2-bit ADC. It illustrates the actual and ideal transfer curves of 2-bit ADC with V_{ref+} and V_{ref-} the specified upper and lower bounds of the ADC input range.

The $V_{at(i)}$ means the actual transfer value at code i, and the $V_{it(i)}$ means the ideal transfer value at code i. The $V_{aw(i)}$ is the actual width between two adjacent codes at code i. Every (i) defines the value at code i in DNL and INL.

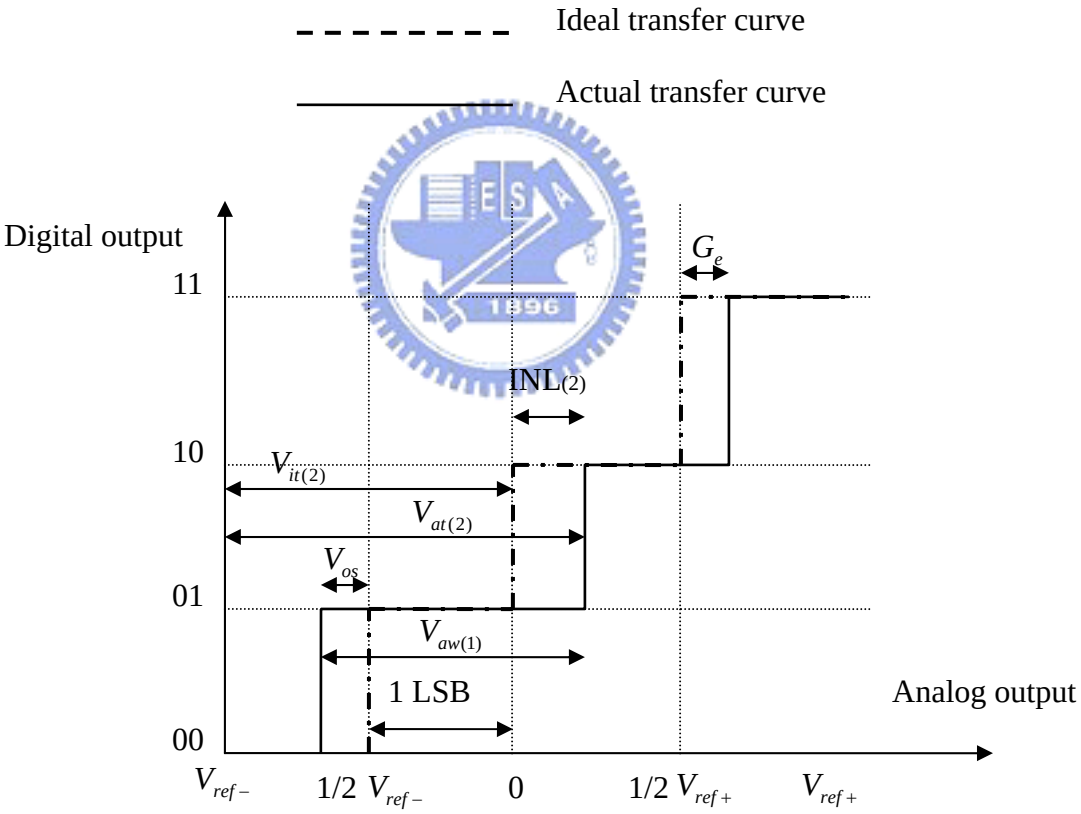


Fig. 2-2, Illustration of ADC parameter

(a) *Ddifferential nonlinearity error* (DNL) :

The DNL is the deviation of actual step width from the ideal value of 1 LSB. For example in Fig. 2-2, $DNL_{(1)} = V_{aw(1)}$ -1LSB.

(b) *Integral nonlinearity error* (INL) :

The INL is the deviation of actual step transition point from the ideal step transition point. For example in Fig. 2-2, $INL_{(2)} = V_{at(2)} - V_{it(2)}$.

(c) *offset error* (Vos) :

The offset error is the difference between the ideal and actual voltage at the lowest code as shown in Fig. 2-2.

(d) *gain error* (Ge) :

The gain error is the difference between the ideal and actual voltage at the highst code as shown in Fig. 2-2.

2.2 Three Architectures of ADC

2.2.1 Flash Architecture

Flash ADC architecture is shown in Fig. 2-3. The flash architecture consists of $2^N - 1$ comparators, a resistor string, and a decoder. The flash architecture does not need explicit front-end *sample-and-hold* (S/H) circuits. Only one clock cycle is needed to perform data conversion. The flash architecture is the simplest and fastest A/D converters. The number of comparators and reference voltages grow exponentially with the resolution. So the chip size and power consumption will become excessively large for the resolution above 6 bits.

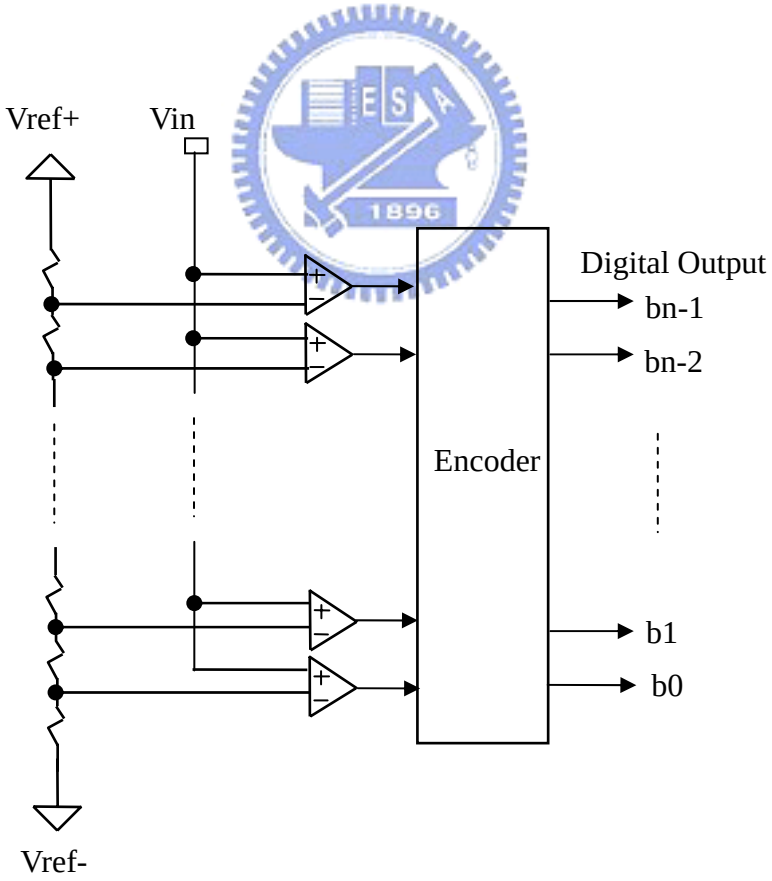


Fig. 2-3, Flash ADC

2.2.2 Two-step Architecture

Because flash architecture use many comparators and resistor, two-step architecture improve its disadvantage. It can reduce comparators and resistor. The block diagram of a two-step architecture is shown in Fig. 2-4. It is include a coarse flash MSB ADC section , a fine flash LSB ADC section, S/H circuits, *digital -to- analog data converters* (DAC) and residue amplifier. As the Fig. 2-4, it is N+M bits of two-step ADC. First, the N-bit MSB ADC determines the first N-bits. Secondly, we use DAC to transfer N-bits digital signals to an analog one. Then, input signals is subtracted off that value, called residue value. Finally, the residue value is amplified 2^N and the LSB are determined using the m-bit LSB ADC.

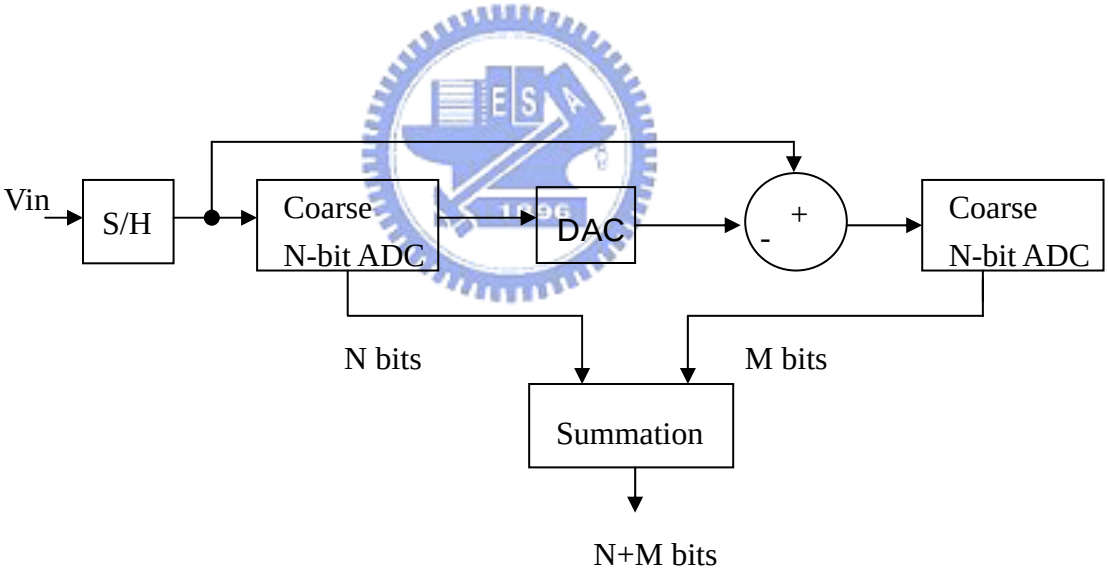


Fig. 2-4, Two-step ADC

2.2.3 Pipeline Architecture

In the pipeline architecture, it is like two-step architecture. But the pipeline architecture needs more stages. Each stage has a S/H circuits, a low-resolution ADC, a DAC, a residue amplifier. Input signal is ampled S/H circuits. Then low-resolution ADC transform digital outputs of this stage. The output signals of DAC are subtracted out of the hold voltage in residue amplifier. The residue signals is transmitted to next stage where the process is repeated. The pipeline architecture is shown in Fig. 2-5. Add all digital output of each stage in digital error correction circuits to produce final outputs.

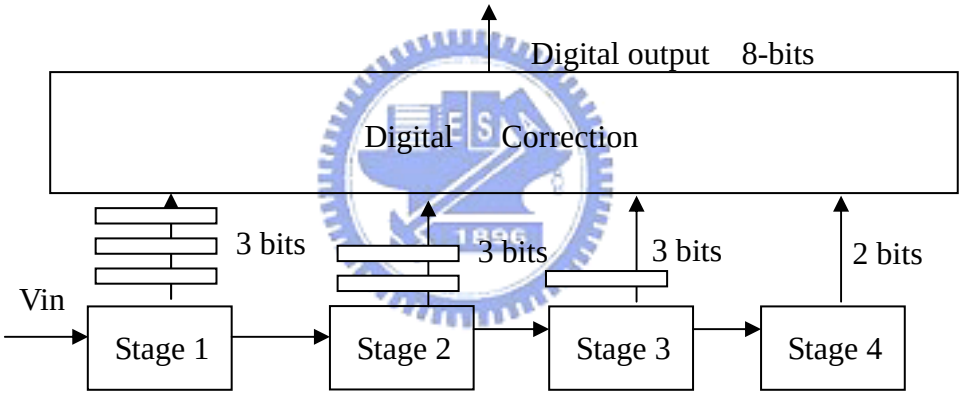


Fig 2-5, Pipeline ADC

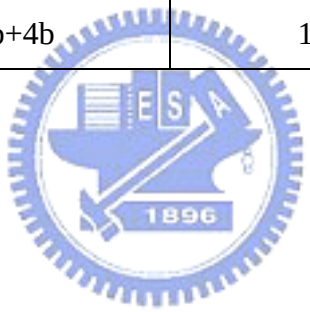
Pipeline architecture has the advantage of flash ADC. It can reduce chip area and power construction. But, how many stages in the pipeline architecture and how many bits in each stage require careful design. For example of an 8-bit ADC, first situation is two stage (5-4 bits). Second situation is seven stages (2-2-2-2-2-2-2 bits). For first design, the residue amplifier must amplify 16 times. But residue amplifier must amplify 2 times of second design. Because of settling time, The second design is faster than first situation. But the second

design must has higher resolution because of there are more bits in the next stage.

As shown in the Table 2-1, It is to compare the more stage and less stage which is better. With more stages, it has high speed potential, high latency, small cap array and large operational amplifier size. With less stages, it has high resolution potential, low latency, high scale down ratio and large cap array.

Table 2-1, Number of stage of pipeline ADC

Number of stage	Structure	Gain per stage	Number of comparator
7	2b*7	2	14
4	3b*3+2b	4	21
2	5b+4b	16	45



2.3 BIST Review

Built-in self-test circuits builds in the chip with device-under test. BIST circuits allows the DUT to evaluate its own quality without elaborate automatic test equipment. The DUT also can be tested in parallel by BIST circuits and automatic test equipment. BIST circuits requires a little more power consumption. There are some advantages and disadvantages in the Table 2-2.

Table 2-2, Advantage and disadvantage of BIST

Advantage	Build test circuits on chip Reduce input/output pin signals traffic Permit testing easily Reduce test cost Reduce test time At-speed testing
Disadvantage	Area overhead Capability for system test

2.4 Two Works for BIST

2.4.1 Huertas's Work

Fig. 2-6 shows the BIST scheme for structural testing of pipeline ADC. The strategies relies on reconfigured as A/D-D/A block, and tests each of ADC stages by applying a set of analog values. These values are DC stimuli giving a simple output signature. The technique is intended for being used in pipeline converters of arbitrary number of conversion stages and with a digital self-correction mechanism. It sends specific analog signals and digital count to each stage. Then, it compares the analog value and digital count with signals from the stages. If they are all equal, anatest and digtest are set pass. If they are one or all are not equal, anatest and signals are set fail [1].

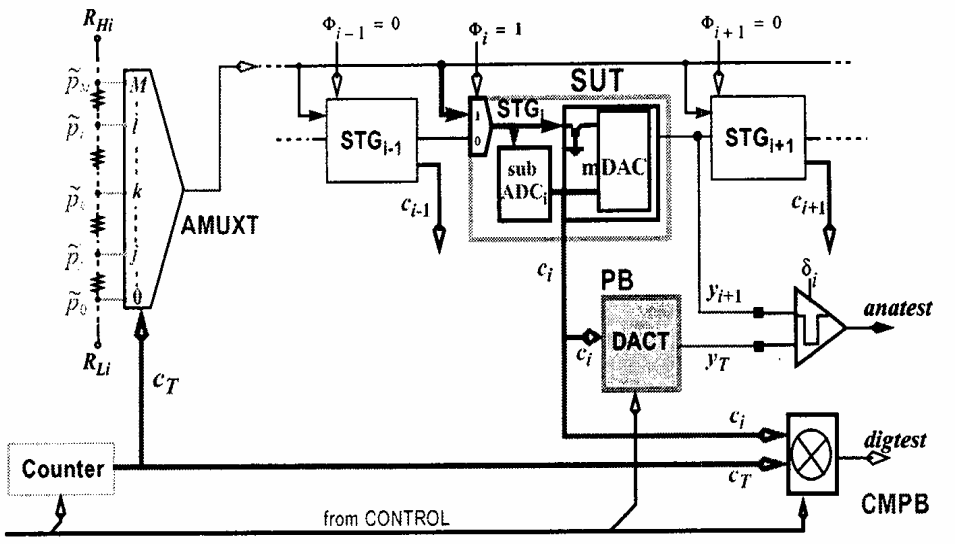


Fig. 2-6, Huertas's work

2.4.2 Lee's Work

Fig. 2-7 shows a BIST structure to test the static specification of ADC. A ramp signals generated by integrator serves as a test input signals. A specific range of this signals is divided into 2^{N+1} segments, with each segment corresponding to one output combination of n+1-bit counter, where n is the number of bits of ADC under test. The testing process is done with digital data processing by comparing the output of ADC under test with output of the n+1-bit counter [2].

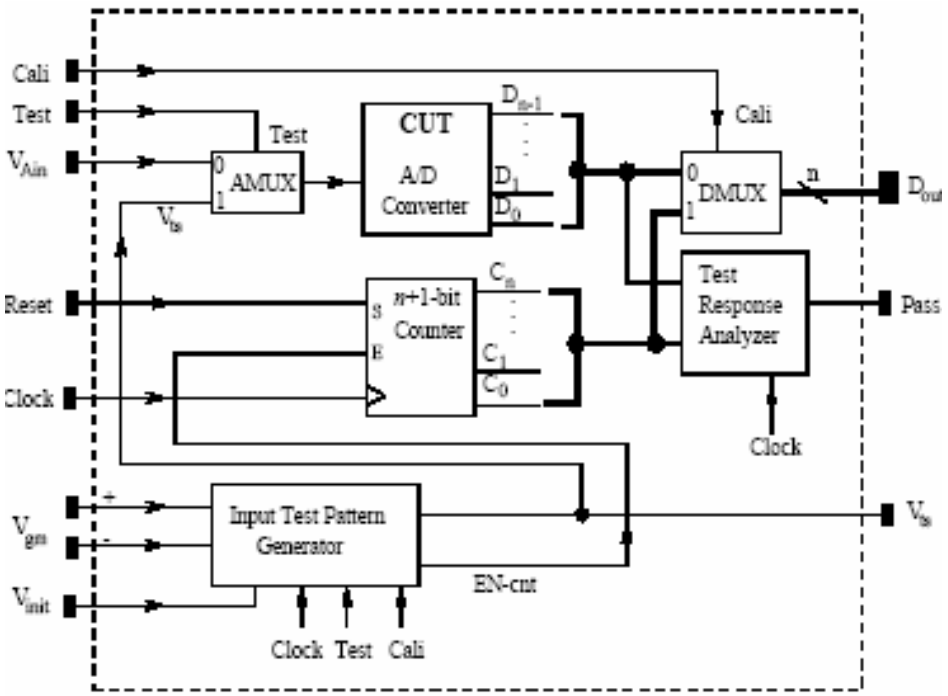


Fig. 2-7, Lee's work

Chapter 3

50 MHz / 8-bits Pipeline ADC

3.1 Abstract

In the chapter, we propose to design a 8-bit, 50 MHz pipeline ADC. We select four stages (3-3-3-2 bits structure), as shown in Fig. 3-1. Each stage has a S/H circuits, a low-resolution ADC, a DAC and a residue amplifier. With digital error correction circuits, it can reduce offset error and increase resolution. Clock generator generates different clock signals for the internal circuits. The S/H circuits uses double-sampling architecture. It can sample two times in an unit time than traditional S/H circuits.

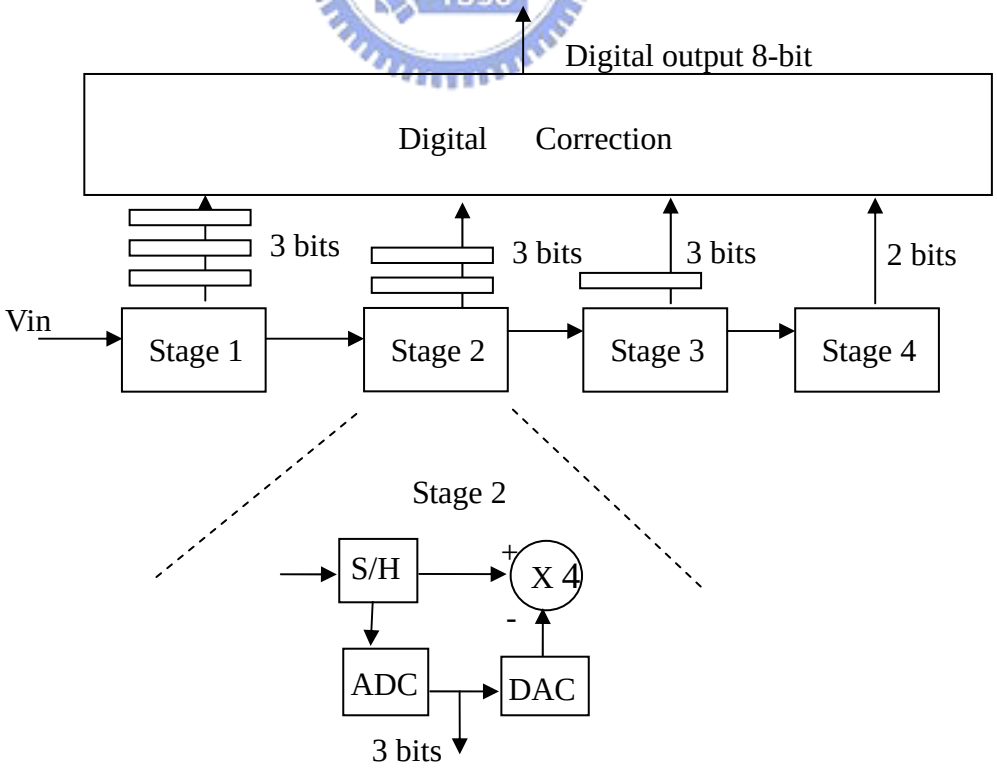


Fig. 3-1, Four stages of pipeline ADC

3.2 ADC Architecture Overview

All circuits of pipeline ADC which we design are shown as the flow.

a. 50MS/s S/H circuits:

- Folded-cascode Op.
- Double Sample S/H circuits.

b. 3-bits A/D converters:

- Pre Amplifier.
- Comparator.
- Encoder.
- Bubble correction.

c. 3-bits D/A converters:

- Resistor D/A converters.

d. Residue amplifier:

- Residue amplifier.

e. Digital Error Correction:

- Digital Error Correction.
- D flip-flop.

f. Clock Generator:

- Clock Generator.

3.3 Sample-and-Hold circuits

3.3.1 Double-sampling S/H

In the analog-to-digital converters， the sample-and-hold circuits is very important. It is a key module in designing an ADC. The double-sampling architecture is shown in Fig. 3-2. Switches of transistor M5/M6/M7/M8/M13/M14/M15/M16 control the capacitor to sample or hold signals. Our goal is 50 Mega Sample per second with a resolution of 8 bits and error is less than 1.5625mV (1/2 LSB). It's dynamic range is 0.8 V (peak-to-peak).

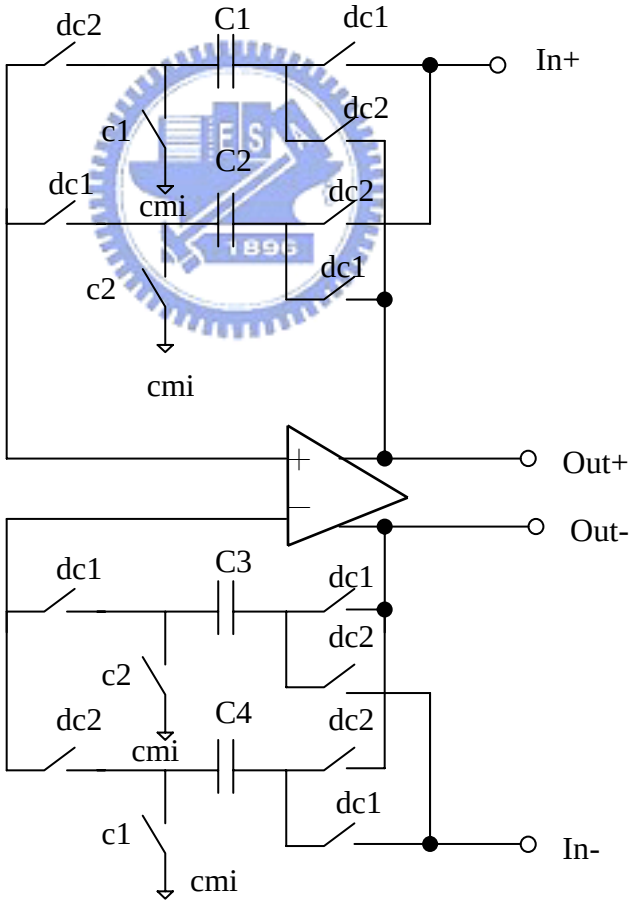


Fig. 3-2, Double-sampling S/H circuits

The double-sampling S/H, uses two pairs capacitors to sample and hold in turns. When one pair is sampling input signals, another hold previous input signals. As shown in Fig. 3-3, C1/C4 sample input signals and C2/C3 and OPA become close-loop to hold previous input signals. In the next clock phase, the two pairs capacitors exchange their work. C1/C4 holds signals and C2/C3 sample signals. It has two times of sample output in unit time.

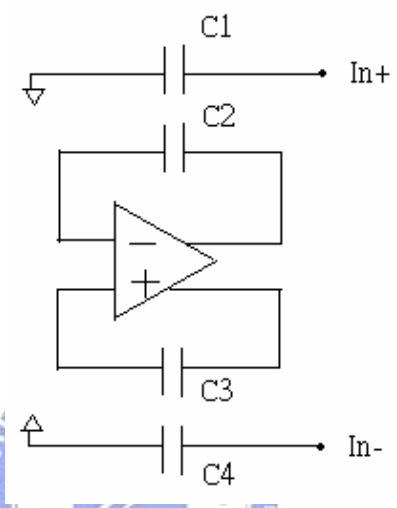


Fig. 3-3, Operational of double-sampling architecture

Because of double-sampling, it has two outputs in one clock. But traditional S/H only has one outputs in one clock. That is shown in Fig. 3-4.

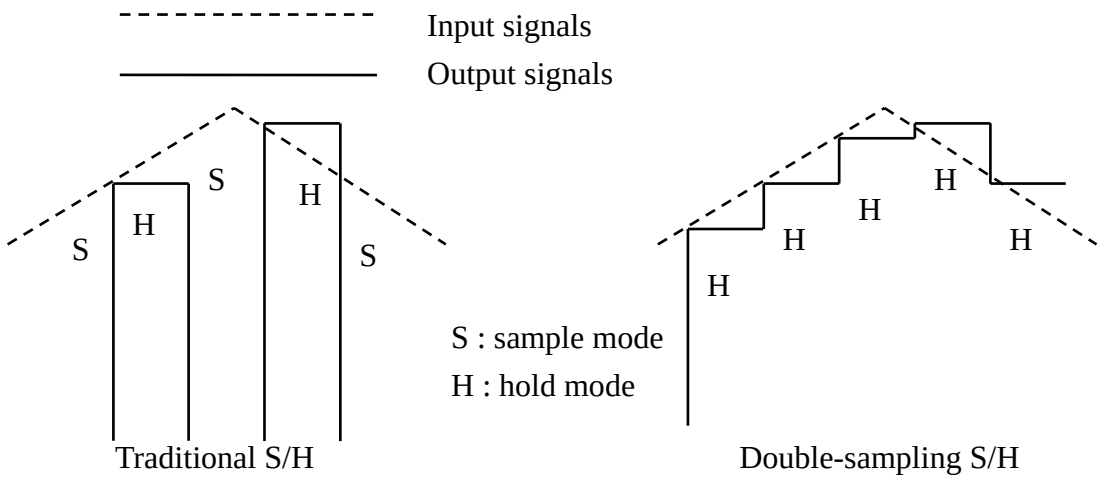


Fig. 3-4, Compare traditional S/H and double sampling S/H

3.3.2 Operational Amplifier

In the sample-and-hold circuits, the operational amplifier is very important. It is the key point to design S/H circuits. The unit-gain frequency and slew-rate decides the speed of the S/H circuits. The gain decides the gain error of the S/H circuits. Output swing decides the dynamic range of the S/H circuits.

a. 8-bits resolution, 0.8 mV dynamic range (peak-to-peak).

$\frac{1}{2}\text{LSB} = 0.5 \times 800\text{mV} \div 256 \geq \frac{1}{A}$, so $A \geq 640 = 56\text{dB}$.

b. 8-bits resolution, settling time is less than 10ns (half of 20ns).

$20\,\text{ns} = \frac{A}{f_t} \times \ln 256$, so $f_t \geq 320\,\text{MHz}$.

We use folded-cascode operational amplifiers, shown in Fig. 3-5. Its advantage is large output swing. Output and input can have the same common-mode level.

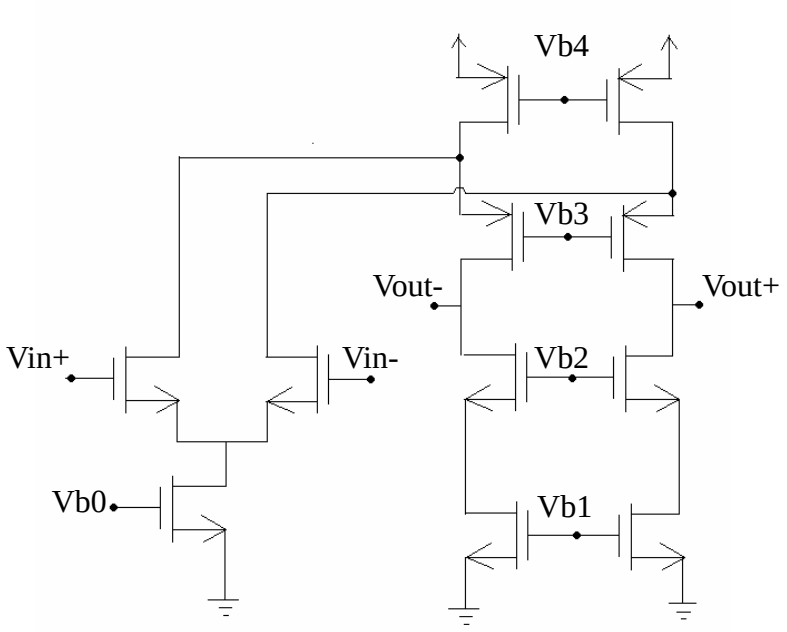


Fig. 3-5, Folded-cascode operational amplifier

In the fully-differential operational amplifier, we need *common-mode feedback* (CMFB) circuits to hold on the voltage of common-mode output. It lets the output swing of operational amplifier to have the same datum point. We use dynamic CMFB circuits. In coordination to the double-sampling architecture, two pairs capacitor work to take turns. It is shown in Fig. 3-6.

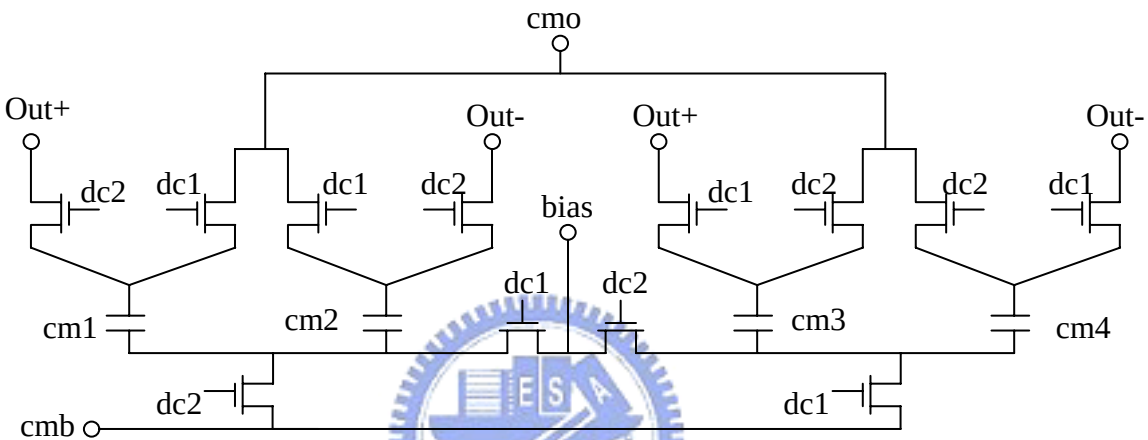


Fig. 3-6, Common-mode feedback circuits

There are two pairs of CMFB circuits, left side is the one and right side is another. They are feedback in turns. So, we only analysis the right hand side, M3/M4. When dclk2 is high, MC6/MC7/MC11 are open, CM3/CM4 charge the difference of CMO and Bias. When dclk1 is high, MC5/MC8/MC12 are open, the charge of CM3/CM4 share the charge with $Out+/Out-$ and Cmb. If the common-mode voltage of $Out+/Out-$ have offset, the voltage difference will be feedback to the operational amplifier to calibrate $Out+/Out-$ level.

As shown in Fig. 3-7, it is the simulation results of folded-cascode operational amplifier. We calculate that the gain of operational amplifier must be 56dB and unit-gain frequency must higher than 310 MHz. The parameters are shown in Table 3-1.

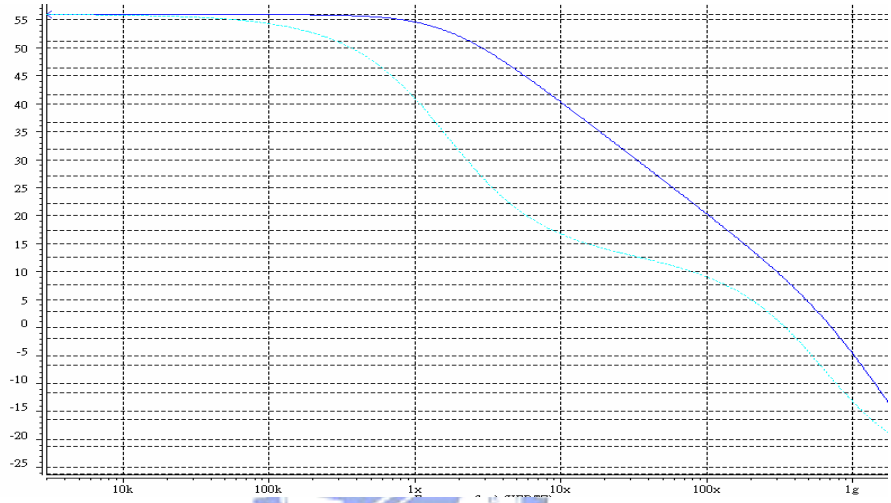


Fig. 3-7, Simulation of folded-cascode operational amplifier

Table 3-1, Parameters of folded-cascode operational amplifier

DC Gain	Unit-Gain frequency	Phase Margin	I/P CM	O/P CM	Dynamic Range
56 dB	570 MHz	60 deg	0.9 v	0.9 v	0.8 v

3.4 3-bit Flash ADC

In the flash 3-bit ADC, it includes Pre-Amplifier, Comparator, Encoder and Bubble correction circuits. It is shown in Fig. 3-8. First, input signal (V_{in}) compares with eight reference voltages levels respectively. And then, the comparison results are corrected by bubble correction circuits. The correction circuits can reduce effect of meta-stability. Finally, the improved thermometer will be transferred to binary code by encoder.

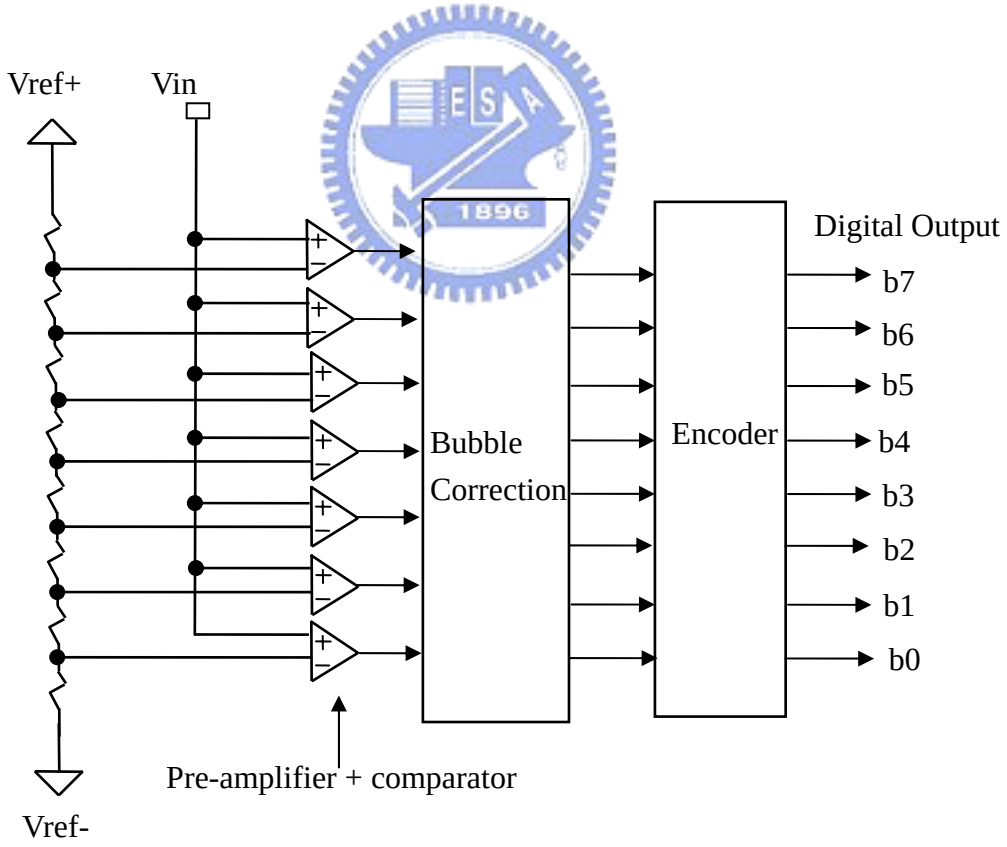


Fig. 3-8, 3-bit flash ADC

3.4.1 Pre-Amplifier

The voltage offset error of comparator will cause error during comparing process. It is an important factor to affect the resolution of ADC. So, the pre-amplifier can amplify the input signals to reduce the affect of offset error for comparator. As shown in Fig. 3-9, it is differential difference component. The first stage amplifies the difference between input signals and reference signals. Then the difference will be transfer to the second stage. We hope the gain of pre-amplifier is bigger then eight times. Then, we look the offset voltage is become 1/8 of the original in the comparator. For example, if the voltage offset error is 24 mV in the comparator, it is 3 mV in pre-amplifier forward. If the difference between input signals and reference signals are too small, it will affect the meta-stability. The pre-amplifier can reduce the affect of meta-stability.

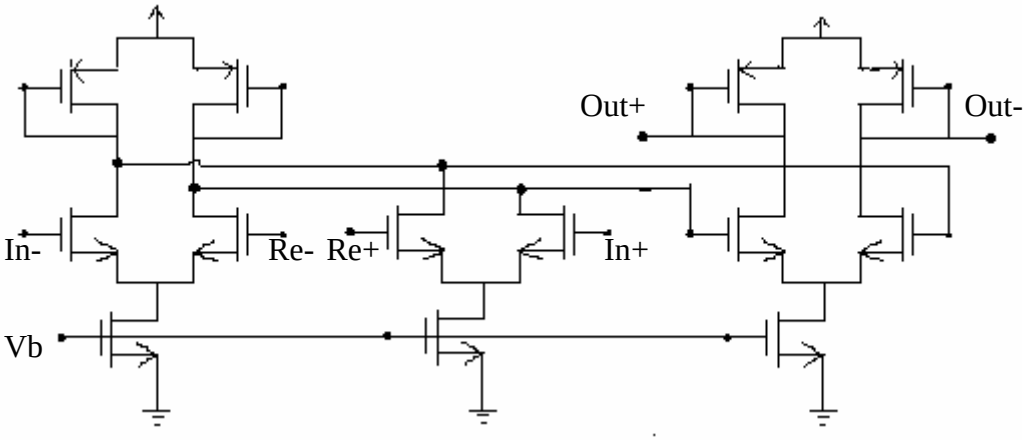


Fig. 3-9, Pre-amplifier circuits

3.4.2 Comparator

As shown in Fig. 3-10, it is a latch type comparator. When the clock C_n is low, it is in the reset mode. $Out+$ and $Out-$ reset to vdd. When the clock C_n is high, it is in the latch mode. A comparator compares the difference between I_n and R_{ef} signals. When one of $Out+$ and $Out-$ sets to high level, the other will set to low level.

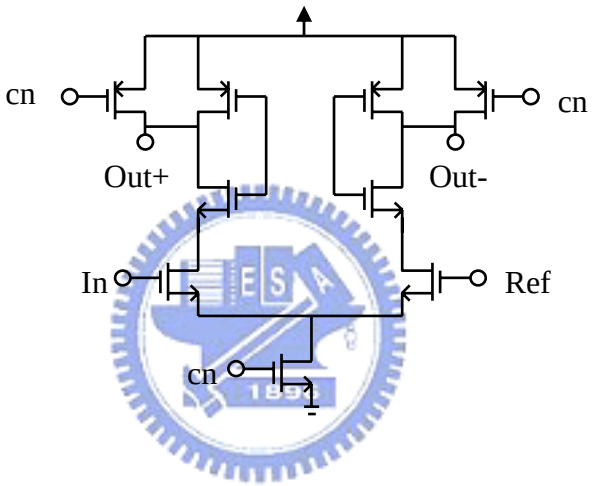


Fig. 3-10, Comparator

3.4.3 Bubble correction

Because of meta-stability, there is an error code in a group codes. For example, it is shown in Fig. 3-11. Left side is correct input. Input is 0-0-1-1-1 and output is 0-0-1-0-0-0. In right side, input is not correct 0-0-1-0-1. But we use the bubble-correction to calibrate it. Therefore the output is also correct.

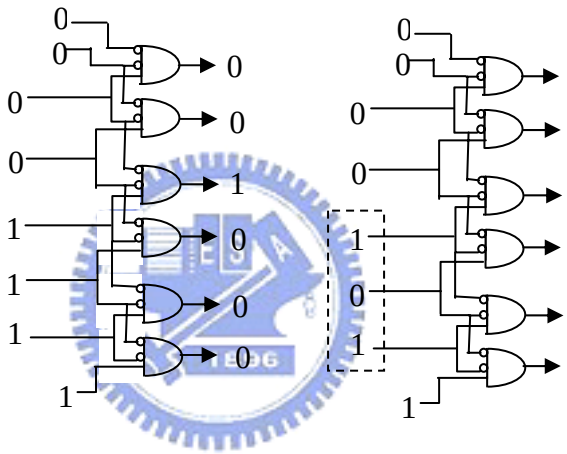


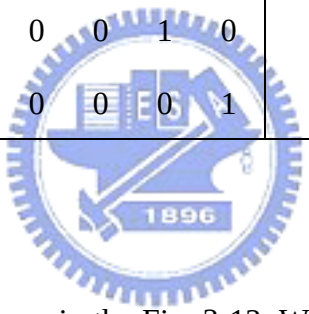
Fig. 3-11, Bubble correction circuits

3.4.4 Encoder

We want to transfer the thermometer to output code of 3-bit. It is shown in the Table 3-2.

Table 3-2, Encode to 3-bit output

a6	a5	a4	a3	a2	a1	a0	d2	d1	d0
1	0	0	0	0	0	0	1	1	0
0	1	0	0	0	0	0	1	0	1
0	0	1	0	0	0	0	1	0	0
0	0	0	1	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0
0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	0	1	0	0	0



Encoder architecture is shown in the Fig. 3-12. We use three 3-input OR-gate to encode the input code.

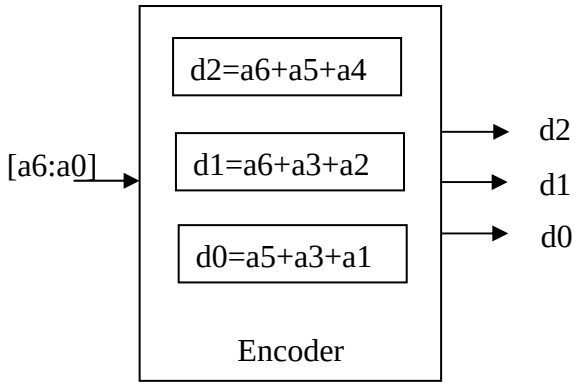


Fig. 3-12, Encoder

3.5 3-bit DAC

Digital-to-analog converters uses serial resistors to divid the reference voltage into several voltage value. Da+ and Da- select output of +3/4V_{ref}, +1/2 V_{ref}, +1/4 V_{ref}, -3/4 V_{ref}, -1/2 V_{ref}, -1/4 V_{ref} and 0. We must decide the size of switch carefully. It considers turn-on resistor of switch. Da+ and Da- signals must to be steady-state as fast aswell. It is shown in Fig. 3-13.

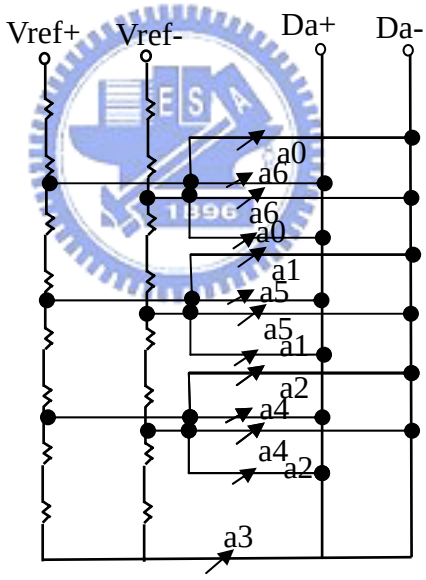


Fig. 3-13, Series resistor DAC

3.6 Residue Amplifier

As shown in Fig. 3-14，it is residue amplifier circuits. It must operate in overall range. It must auto zero to reduce the offset error of operational amplifier.

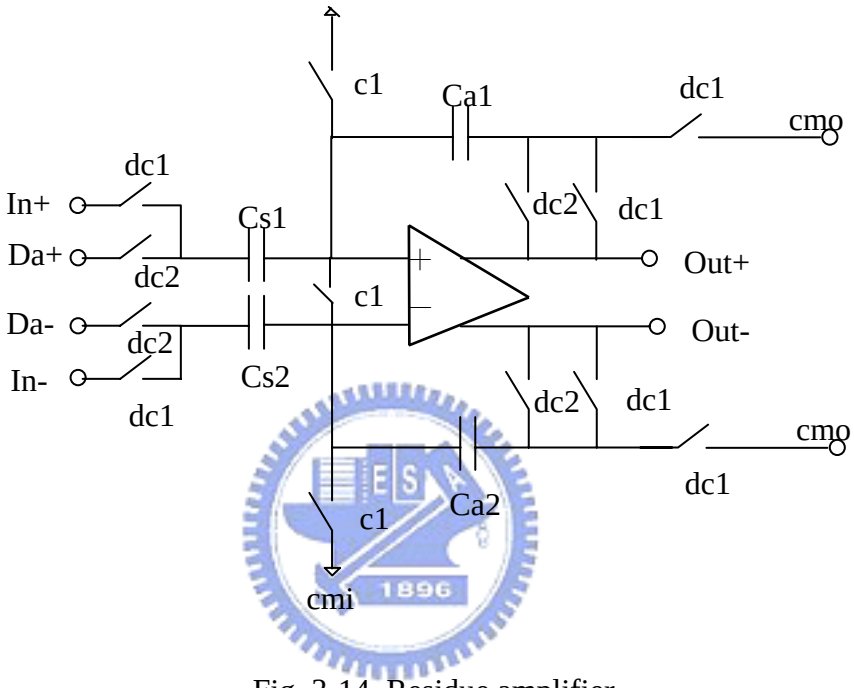


Fig. 3-14, Residue amplifier

In order tohold the charge of capacitors，dc1 and dc2 is non-overlapping. We use a skip named bottom-plate sampling. Before dc1 set to low，c1 has already turned to low. It lets charge injection and input signals are not correspond. There is no offset error from operational amplifier. Because the offset error is cancel by the virtual short. The clocks are shown in Fig. 3-15.

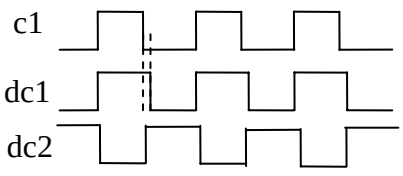


Fig. 3-15, Non-overlapping clock

First，when dc1/c1 is high，it is shown in Fig. 3-16. Cs1/Cs2 charges the input signals. Input and output of operational amplifier connect the common-mode voltage of in and out. Second，when dc2 is high，it is shown in Fig. 3-17. Cs1/Cs2 connects Da+/Da- to charge. The difference charge of In and Da transfer to Ca1/Ca2. When Cs=4Ca，then *Out*=4*(In-Da).

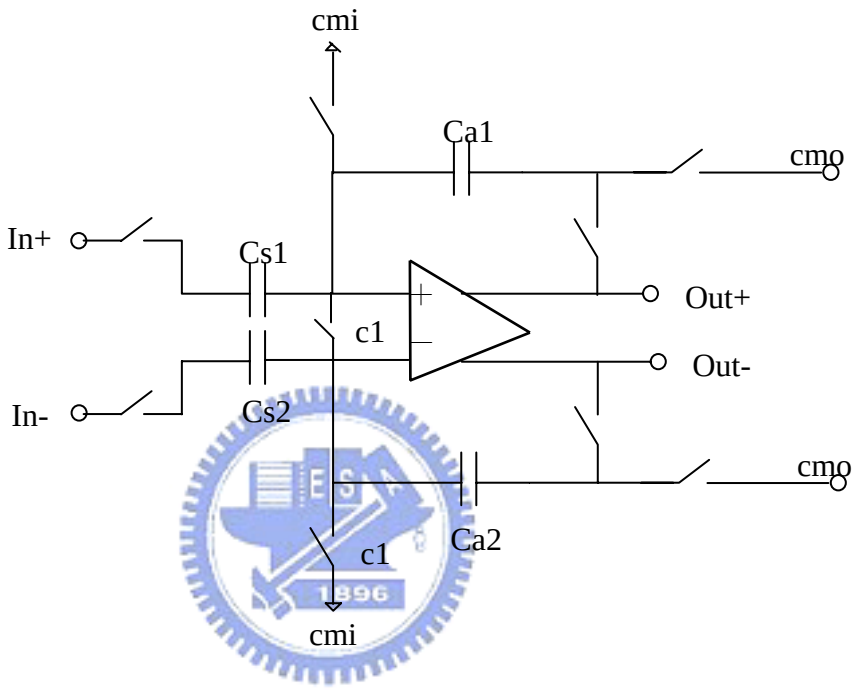


Fig. 3-16, Sample mode of residue amplifier

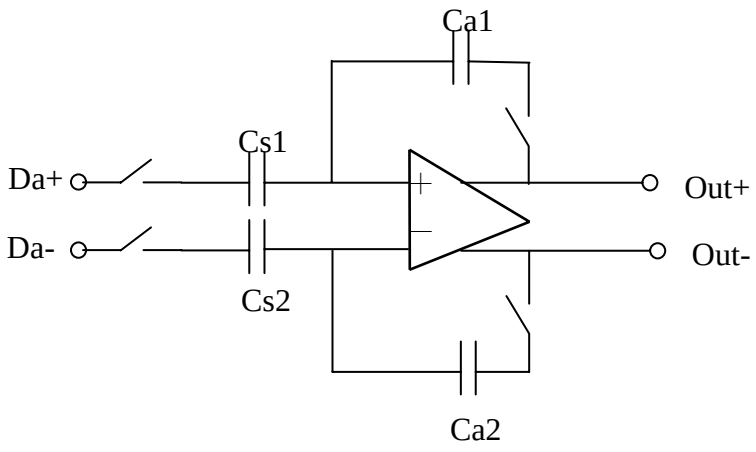


Fig. 3-17, Residue mode of residue amplifier

3.7 Digital Error Correction

Digital error correction circuits can reduce offset error and increase resolution. The principle is the MSB of next stage to calibrate the LSB of this stage. The final output value is the sum of each stage's output， it is shown in Fig 3-18.

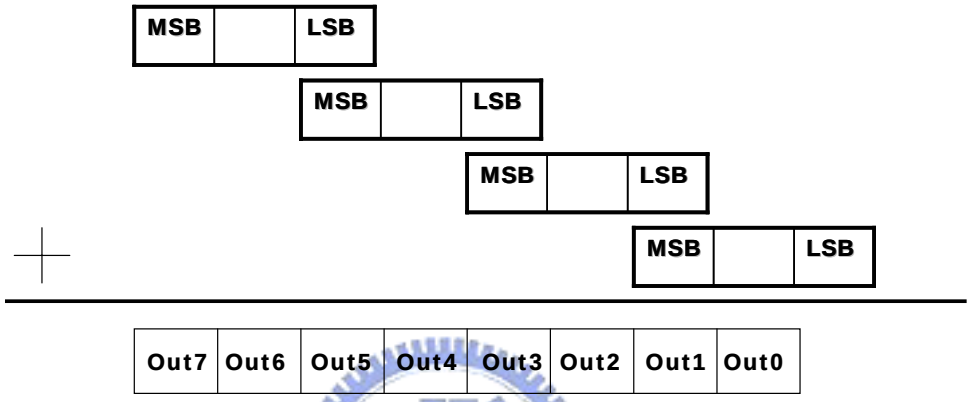


Fig. 3-18, Final output of digital error correction

There are two steps. First，Keep the compare level to shift right 1/2LSB. Second，reduce the gain of amplifier two times. Originally we amplify the gain is 8. But now， we amplify only 4. Fig. 3-19 is traditional transfer curve of 3-bit ADC. Fig. 3-20 is shift transfer curve of 3-bit ADC.

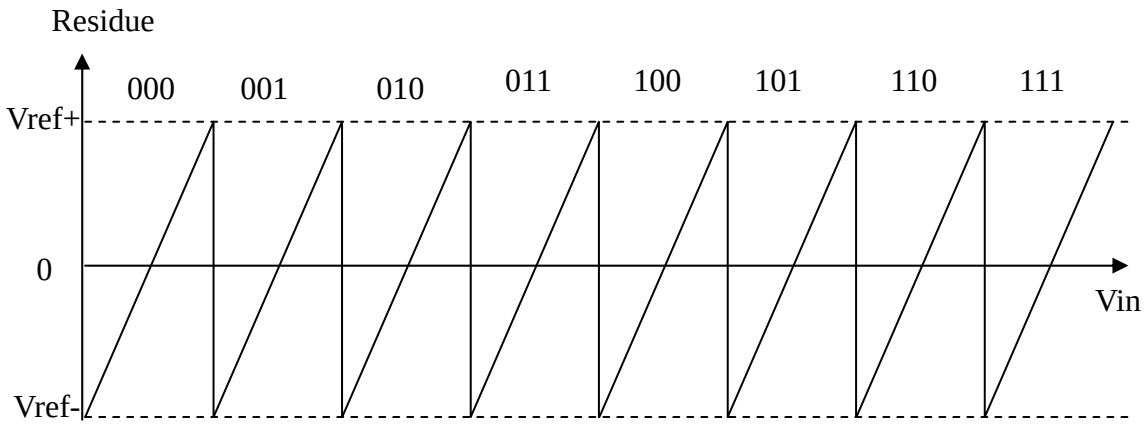


Fig. 3-19, Traditional transfer curve

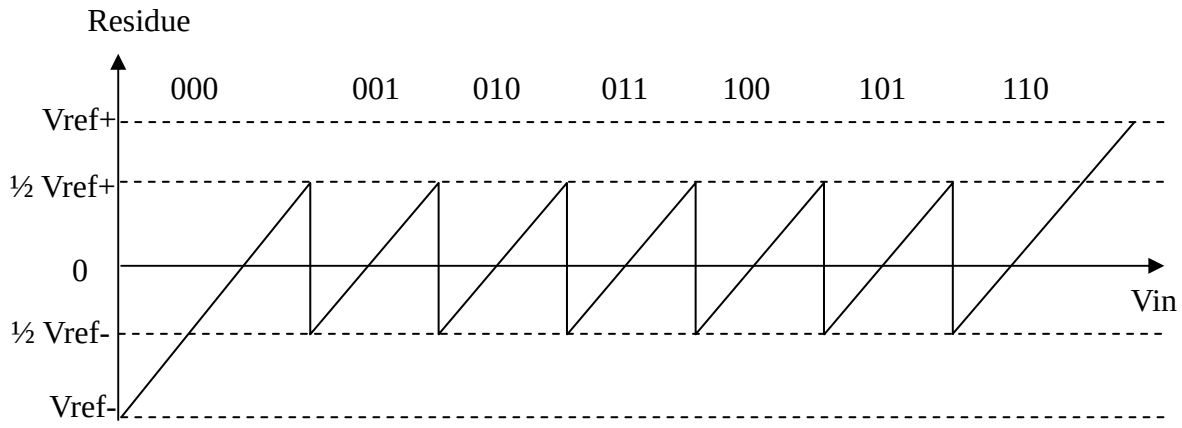


Fig. 3-20, Shift transfer curve

3.8 Clock Generator

Clock generator is shown in Fig. 3-21. In the switch capacitor circuits， all switchs are controlled by internal clock which is generated by clock generator. It has two modes. One is sample mode and the other is hold mode. The clocks must be non-overlapping in order to guarantee charge is not inadvertently lost. It is shown in Fig. 3-22. Dc1 and dc2 are non-overlapping.

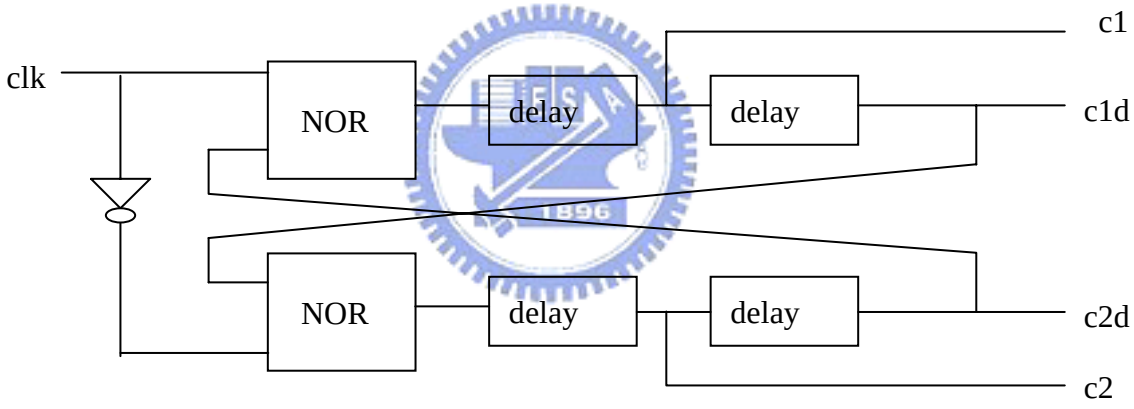


Fig. 3-21, Clock generator

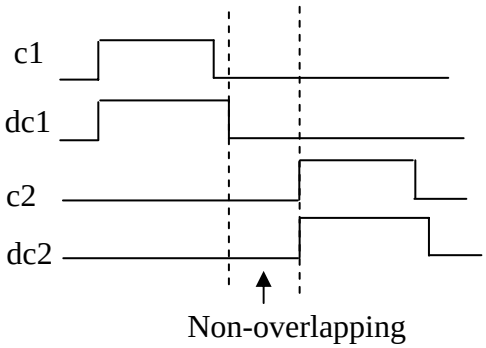


Fig. 3-22, Clocks of clock generator

Chapter 4

Built-In Self-Test of ADC

4.1 Overview

In the chapter, we propose a new approach to test pipeline ADC. It gathers statistic about probability to test pipeline ADC. We test the offset error and gain error by the output signals of the S/H in each stage. Then, we design the BIST circuits. We realize the BIST circuits and pipeline ADC on the same chip.

4.2 Ideal Analysis for ADC

We design the four stages pipeline ADC. Output code of first, second and third stage is 3-bit. Output code of fourth stage is 2-bit. They are shown in Fig.4-1.

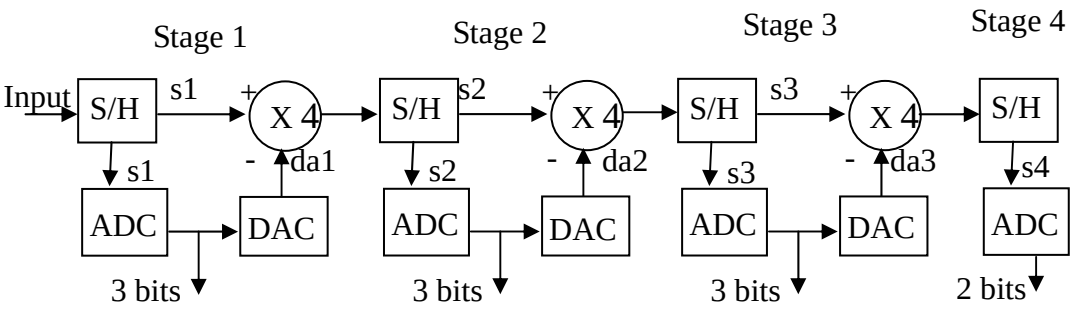


Fig. 4-1, Four stages of pipeline ADC.

If pipeline ADC is ideal, the equation of s1, s2, s3 and s4 is as the follow:

$$s1 = in. \quad (1)$$

$$s2 = (s1 - da1) \times 4. \quad (2)$$

$$s3 = (s2 - da2) \times 4. \quad (3)$$

$$s4 = (s3 - da3) \times 4. \quad (4)$$

$$\text{where} \quad dai = \tfrac{1}{4} \times Vref \times N \quad (5)$$

$$\text{N} = -3: \quad -Vref \le s_{i-1} \le -\tfrac{5}{8} Vref.$$

$$-2: -\tfrac{5}{8} Vref \le s_{i-1} \le -\tfrac{3}{8} Vref.$$

$$-1: -\tfrac{3}{8} Vref \le s_{i-1} \le -\tfrac{1}{8} Vref.$$

$$0: -\tfrac{1}{8} Vref \le s_{i-1} \le \tfrac{1}{8} Vref.$$

$$1: \tfrac{1}{8} Vref \le s_{i-1} \le \tfrac{3}{8} Vref.$$

$$2: \tfrac{3}{8} Vref \le s_{i-1} \le \tfrac{5}{8} Vref.$$

$$3: \quad \tfrac{5}{8} Vref \le s_{i-1} \le Vref.$$

The overall range of input signals is +400 mV ~ -400 mV. We divide the overall range into three parts. *Part-A* (Pa) is -400 mV ~ -150 mV. *Part-B* (Pb) is -150 mV ~ +150 mV. *Part-C* (Pc) is +150 mV ~ +400 mV. It is shown in Fig. 4-2.

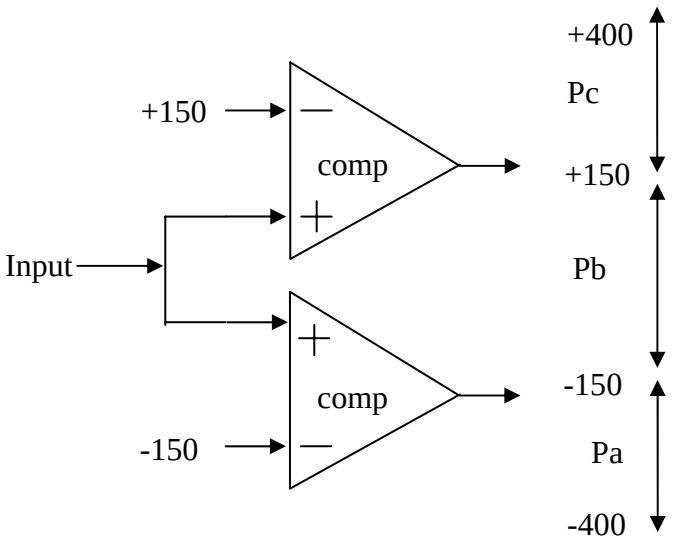


Fig. 4-2, Distribution of Pa and Pb and PC.

If we send ramp signals to the input of the pipeline ADC, we can get the four signals.

The signals s1 is the stage 1 output of the S/H, as shown in Fig. 4-3. The signals s2 is the stage 2 output of the S/H, as shown in Fig. 4-4. The signals s3 is the stage 3 output of the S/H, as shown in Fig. 4-5. The signals s4 is the stage 4 output of the S/H, as shown in Fig. 4-6. All of s1, s2, s3 and s4 are triangle signals. The frequency of the following stage is higher than the pervious stage. Frequency of s2 is four times s1. Frequency of s3 is four times s2， and so on. The overall range is +400 mV ~ -400 mV. We divide the full range into three parts. Part-A is -400 mV ~ -150 mV. Part-B is -150 mV ~ +150 mV. Part-C is +150 mV ~ +400 mV. We can calculate probability of Part-A, Part-B and Part-C in each stage. Stage 1 is Pa1 and Pb1 and Pc1 shown in equation (6), (7) and (8). Stage 2 is Pa2 and Pb2 and Pc2 shown in equation (9), (10) and (11). Stage 3 is Pa3and Pb3 and Pc3 shown in equation (12), (13) and (14). Stage 4 is Pa4 and Pb4 and Pc4 shown in equation (15), (16) and (17).

4.2.1 Ideal Probability of Stage 1

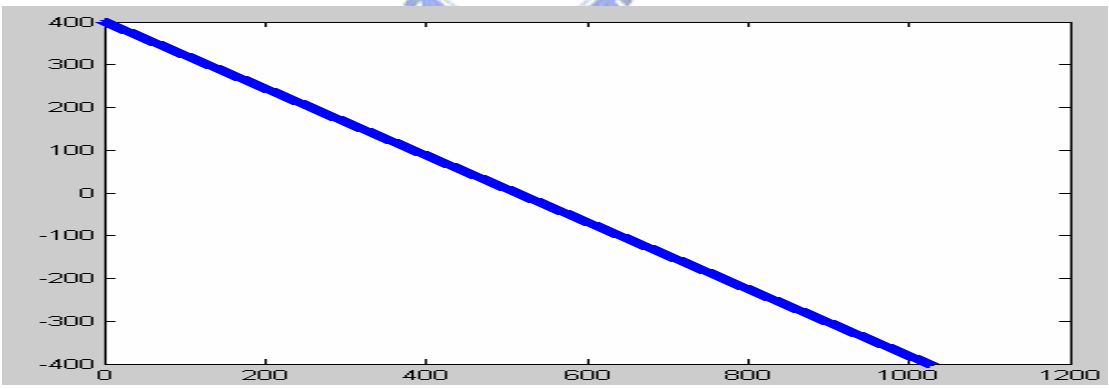


Fig. 4-3, Ideal signals of S/H for stage 1.

$$all = 800. \tag{6}$$

$$Pc1 = Pa1 = \frac{250}{all} = 0.3125. \tag{7}$$

$$Pb1 = \frac{300}{all} = 0.375. \tag{8}$$

4.2.2 Ideal Probability of Stage 2

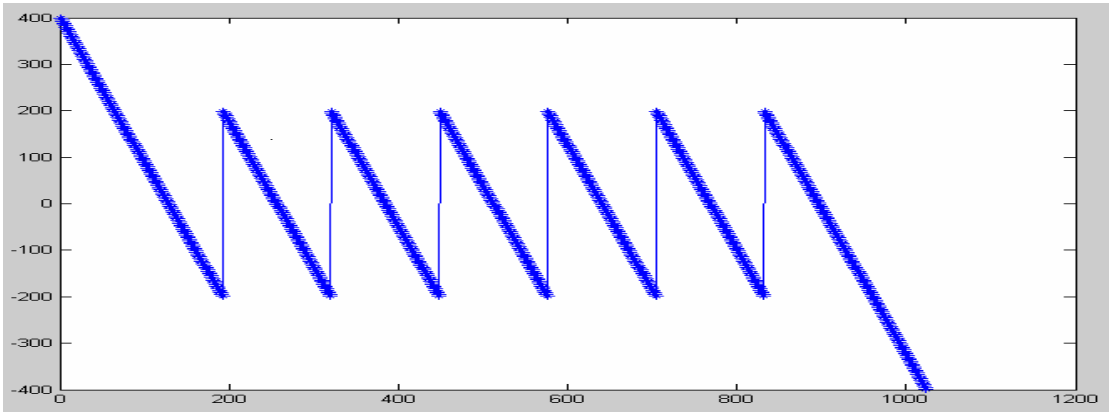


Fig. 4-4, Ideal signals of S/H for stage 2.

$$all = 400*8. \tag{9}$$

$$Pc2 = Pa2 = \frac{200+50*7}{all} = 0.171825. \tag{10}$$

$$Pb2 = \frac{300*8}{all} = 0.65625. \tag{11}$$

4.2.3 Ideal Probability of Stage 3

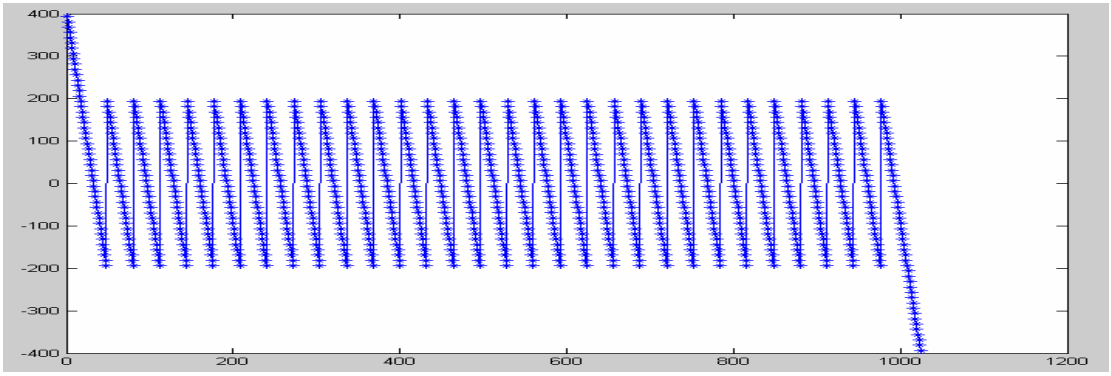


Fig. 4-5, Ideal signals of S/H for stage 3.

$$all = 400*32. \tag{12}$$

$$Pc3 = Pa3 = \frac{200+50*31}{all} = 0.13671875. \tag{13}$$

$$Pb3 = \frac{300*8}{all} = 0.7265625. \tag{14}$$

4.2.4 Ideal Probability of Stage 4

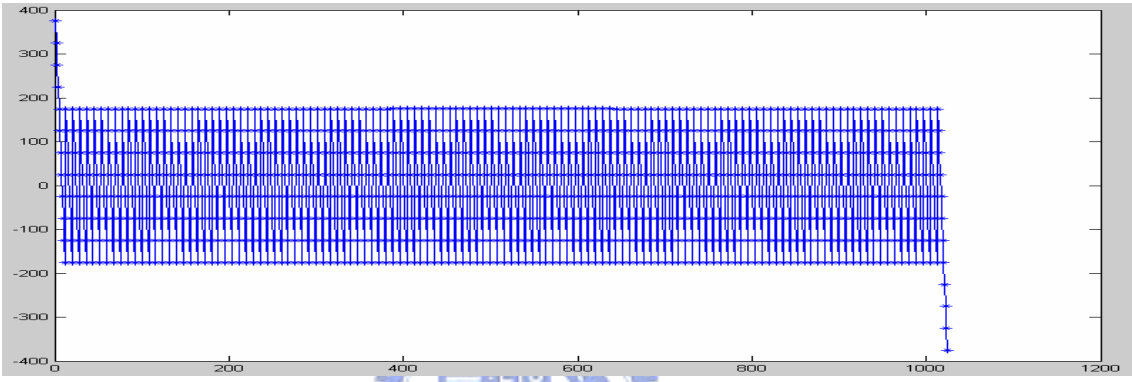


Fig. 4-6, Ideal signals of S/H for stage 4.

$$all = 400*128. \tag{15}$$

$$Pc4 = Pa4 = \frac{200+50*127}{all} = 0.1279296875. \tag{16}$$

$$Pb4 = \frac{300*127}{all} = 0.744140625. \tag{17}$$

4.3 Actual Probability with Offset and Gain error

In the actual ADC, there are voltage offset error and gain error in each stage. Operational amplifiers and comparators have voltage offset error. Residue amplifier has gain error. We suppose that each stage has *voltage offset error* (V_{os}) and *gain error* (G_e). The equations are as follow.

$$s1 = in + V_{OS1}. \quad (1)$$

$$s2 = (s1 - da1) \times (4 + G_{e1}) + V_{OS2}. \quad (2)$$

$$s3 = (s2 - da2) \times (4 + G_{e2}) + V_{OS3}. \quad (3)$$

$$s4 = (s3 - da3) \times (4 + G_{e3}) + V_{OS4}. \quad (4)$$

where $dai = \frac{1}{4} \times Vref \times N$ (5)

$$\mathrm{N} = -3: \quad -Vref \le s_{i-1} \le -\frac{5}{8}Vref.$$

$$-2: -\frac{5}{8}Vref \le s_{i-1} \le -\frac{3}{8}Vref.$$

$$-1: -\frac{3}{8}Vref \le s_{i-1} \le -\frac{1}{8}Vref.$$

$$0: -\frac{1}{8}Vref \le s_{i-1} \le \frac{1}{8}Vref.$$

$$1: \frac{1}{8}Vref \le s_{i-1} \le \frac{3}{8}Vref.$$

$$2: \frac{3}{8}Vref \le s_{i-1} \le \frac{5}{8}Vref.$$

$$3: \quad \frac{5}{8}Vref \le s_{i-1} \le Vref.$$

Therefore, we measure the probability distribution of the four signals s1, s2, s3 and s4. From the probability distribution, we can calculate probability of Part-A, Part-B and Part-C in each stage. We define that Pi is the probability in ideal case, and we also define that Pi' is the probability in actual case when there are gain error and offset error in pipeline ADC. Stage 1 is Pa1' and Pb1' and Pc1' of actual case. Stage 2 is Pa2' and Pb2' and Pc2' of actual case. Stage 3 is Pa3' and Pb3' and Pc3' of actual case. Stage 4 is Pa4' and Pb4' and Pc4' of actual case. Then, we compare Pai' and Pbi' and Pci' with Pai and Pbi and Pci. Pai, Pbi and Pci are

ideal probability. From section 4.2, Pai, Pbi and Pci are shown in Table 4-1.

We define :

Pi is ideal probability.

Pi' is actual probability.

$\Delta P = Pi' - Pi.$ (23)

Table 4-1, Ideal probability

Stage 1	Pa1	31.25 %
	Pb1	37.5 %
	Pc1	31.25 %
Stage 2	Pa2	17.1825 %
	Pb2	65.625 %
	Pc2	17.1825 %
Stage 3	Pa3	13.671875 %
	Pb3	72.65625 %
	Pc3	13.671875 %
Stage 4	Pa4	12.79296875 %
	Pb4	74.4140625 %
	Pc4	12.79296875 %

4.3.1 Offset error

Fig. 4-7 shows that the offset error happens in a stage. The Pb' is equal Pb in Part-B. If Pc' increase x%, Pa' decrease x%. It is shown as follow.

$$Pb' = Pb. \qquad (24)$$

$$Pc' = Pc + x\%. \qquad (25)$$

$$Pa' = Pa - x\%. \qquad (26)$$

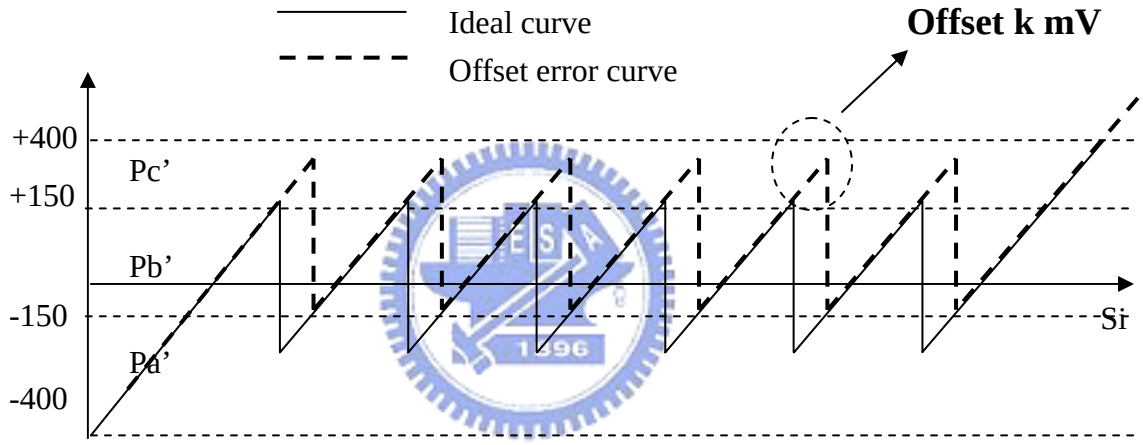


Fig. 4-7, Offset error curve and ideal curve of S/H signals

As shown in the Fig. 4-3 and Fig. 4-7, if there are k1 mV offset error, we can gather Pa1' or Pc1' to calculate the offset error of the stage 1. The equation is shown as follow.

$$k_1 \text{ mV Offset }, Pc'_1 \text{ is actual }, Pc_1 \text{ is ideal }, \text{all} = 800 \qquad (27)$$

$$\Delta Pc_1 = Pc'_1 - Pc_1 = \frac{250 + k}{all} - \frac{250}{all} = \frac{k}{800} \ . \qquad (28)$$

$$\therefore k_1 = \Delta Pc_1 * 400 * 2 \ . \qquad (29)$$

As shown in Fig. 4-4 and Fig. 4-7, if there are k2 mV offset error. We can gather Pa2' or Pc2' to calculate offset error of stage 2. The equation is shown as follow.

k_2 mV Offset , Pc'_2 is actual, Pc_2 is ideal, all $= 400*8$ (30)

$$\Delta Pc_2 = Pc'_2 - Pc_2 = \frac{250+(50+k)*7}{all} - \frac{250+50*7}{all} = \frac{7*k}{8*400} \quad . \quad (31)$$

$$\therefore k_2 = \Delta Pc_2 * 400 * {}^{8}\!/_{7} \quad . \quad (32)$$

As shown in Fig. 4-5 and Fig. 4-7, if there are k3 mV offset error. We can gather Pa3' or Pc3' to calculate offset error of stage 3. The equation is shown as follow.

k_3 mV Offset , Pc'_3 is actual, Pc_3 is ideal, all $= 400*32$ (33)

$$\Delta Pc_3 = Pc'_3 - Pc_3 = \frac{250+(50+k)*31}{all} - \frac{250+50*31}{all} = \frac{31*k}{32*400} \quad . \quad (34)$$

$$\therefore k_3 = \Delta Pc_3 * 400 * {}^{32}\!/_{31} \quad . \quad (35)$$

As shown in Fig. 4-6 and Fig. 4-7, if there are k4 mV offset error. We can gather Pa4' or Pc4' to calculate offset error of stage 4. The equation is shown as follow.

k_4 mV Offset , Pc'_4 is actual, Pc_4 is ideal, all $= 400*128$ (36)

$$\Delta Pc_4 = Pc'_4 - Pc_4 = \frac{250+(50+k)*127}{all} - \frac{250+50*127}{all} = \frac{127*k}{128*400} \quad . \quad (37)$$

$$\therefore k_4 = \Delta Pc_4 * 400 * {}^{128}\!/_{127} \quad . \quad (38)$$

4.3.2 Gain error

When there is gain error happen， it is shown in Fig. 4-8. If Pb’ is increase 2y%, Pa’ and Pc’ is decrease y%. It is shown as follow.

$$Pb' = Pb + 2y\%. \quad (39)$$

$$Pc' = Pc - y\%. \quad (40)$$

$$Pa' = Pa - y\%. \quad (41)$$

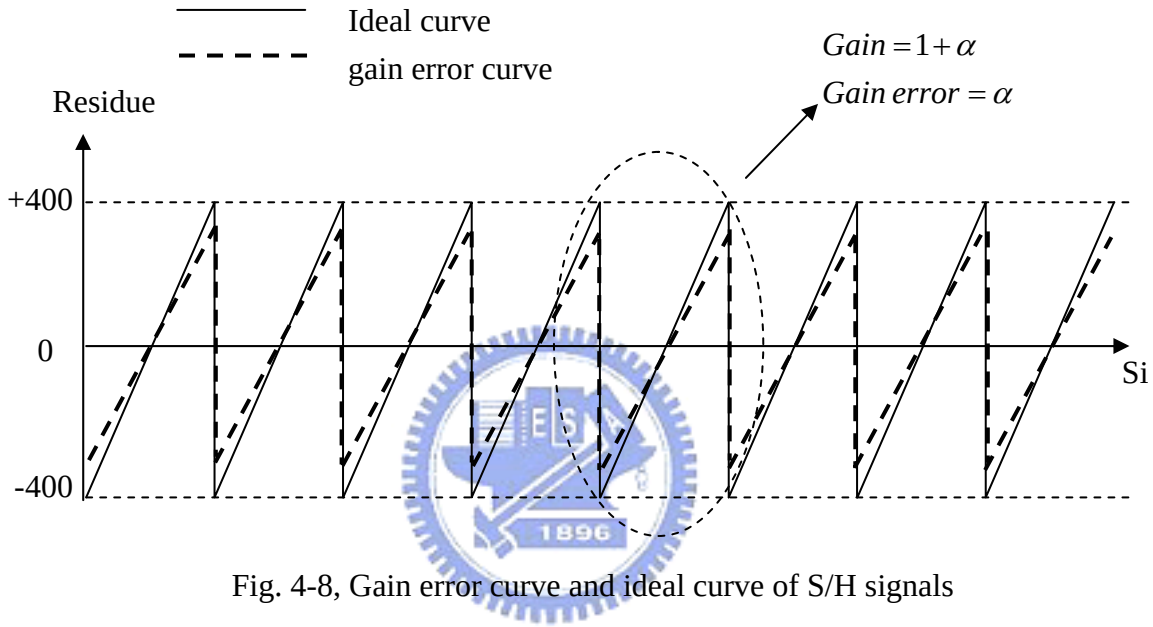


Fig. 4-8, Gain error curve and ideal curve of S/H signals

See the Fig. 4-4 and Fig. 4-8, if there are α_1 gain error. We can gather Pb1’ to calculate gain error of stage 1. The equation is shown as follow. Stage 2 and stage 3 are the same as stage 1.

α is Gain error , Pb' is actual , Pb is ideal

$$Pc'_1 = \frac{Pc_1 * (1+\alpha) + Pb * 0.5 * \alpha_1}{1+\alpha_1} \quad (42)$$

$$Pb'_1 = \frac{Pb_1}{1+\alpha_1} \quad (43)$$

$$\Delta Pb = Pb'_1 - Pb_1 \quad (44)$$

$$\therefore \alpha_1 = -\Delta Pb_1 / Pb'_1 \quad (45)$$

$$\alpha_2 = -\Delta Pb_2 / Pb'_2 \quad (46)$$

$$\alpha_3 = -\Delta Pb_3 / Pb'_3 \quad (47)$$

4.3.3 Conclusion of Offset error and Gain error

If there are offset error and gain error in each stage, we can separate the probability of the offset error from the probability of the gain error. From section 4.3.1, when the offset error happens， the Pb' equal Pb and it is not change. If Pc' increase x%, Pa' decrease x%. From section 4.3.2, if Pb' is increase 2y%, Pa' and Pc' is decrease y%. The relation of the gain error and the offset error is shown in Table 4-2. Therefore, we calculate $\triangle$Pb which is about gain error. Then, we can calculate the offset error from $\triangle$Pc or $\triangle$Pa minus half of $\triangle$Pb. The conclusion is shown in Table 4-3.

Table 4-2, Difference of probability for offset error and gain error

	$\triangle$Pa	$\triangle$Pb	$\triangle$Pc
Offset error	-x%	0	x%
Gain error	-y%	2y%	-y%
Offset error and gain error	-x-y%	2y%	x-y%

Table 4-3, Conclusion of probability for offset error and gain error

Offset error (k mV offset)	Stage 1	$k_1 = \Delta Pc_1 * 400 * 2$
	Stage 2	$k_2 = \Delta Pc_2 * 400 * 8/7$
	Stage 3	$k_3 = \Delta Pc_3 * 400 * 32/31$
	Stage 4	$k_4 = \Delta Pc_4 * 400 * 128/127$
Gain error (α gain error)	Stage 1	$\alpha_1 = -\Delta Pb_1 / Pb'_1$
	Stage 2	$\alpha_2 = -\Delta Pb_2 / Pb'_2$
	Stage 3	$\alpha_3 = -\Delta Pb_3 / Pb'_3$

4.4 BIST Circuits

In the section, we propose a BIST circuits. BIST circuits and ADC circuits are shown in Fig. 4-9. BIST circuits has two circuits which are triangle wave generator circuits and analyzer circuits. When mode in the Fig. 4-9 is high, the ADC is in normal mode and input signals of the ADC is sent from the Analog Input. When mode is low, ADC is in test mode and input signals of the ADC is sent from the Triangle Wave.

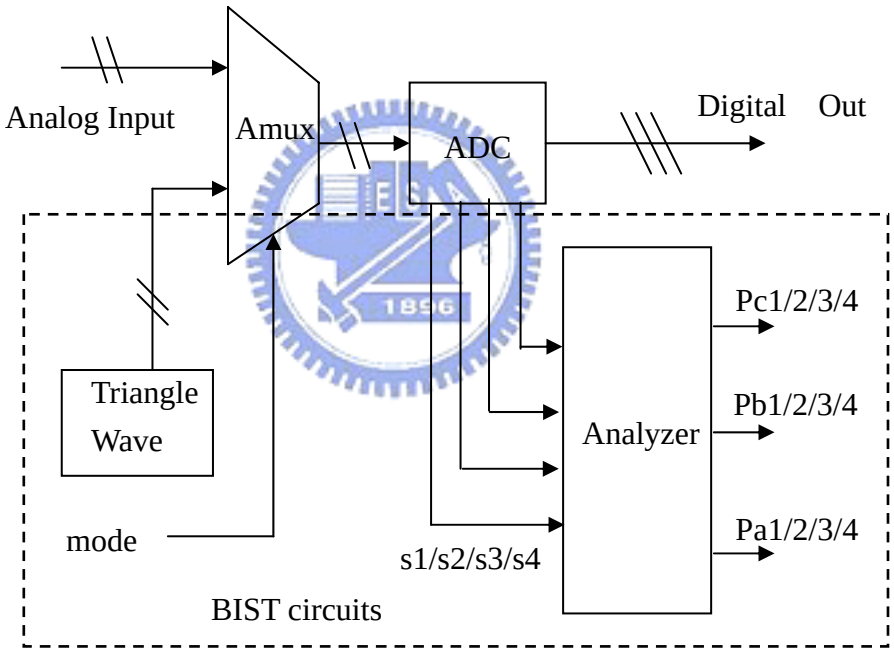


Fig. 4-9, BIST circuits and ADC circuits

From previous section, we want to gather statistics and calculate probability Pa and Pb and Pc. The signals s1, s2, s3 and s4 are the input signals of the Analyzer. There are four Comparison Circuits in Analyzer in Fig. 4-9. Comparison Circuits is shown in Fig. 4-10. The signals s1, s2, s3 and s4 are sent into the Comparison Circuits and the Comparison Circuits

compares the signals with 150 mV and -150 mV. The output signals of comp1 and comp2 are sent into logic circuits. Then, the logic circuits transfers the output signals of comp1 and comp2 to Pa and Pb and Pc. The relation of si and Pa and Pb and Pc is shown in Table 4-4.

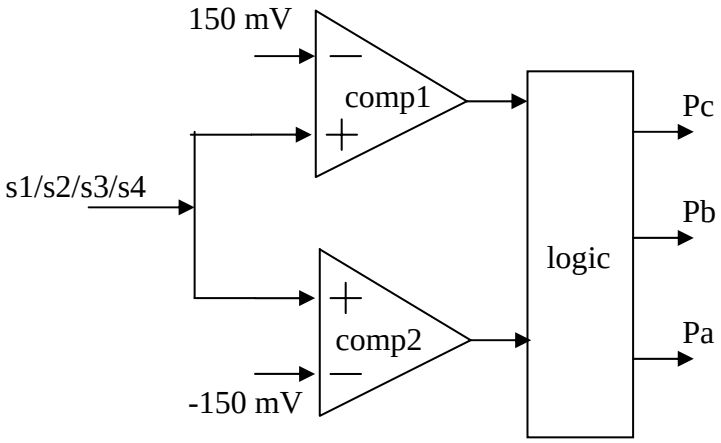


Fig. 4-10, Comparison Circuits

Table 4-4, Logic function of analyzer

Input : si	comp1	comp2	Pa	Pb	Pc	Logic circuits
+400 ~ +150 mV	1	1	0	0	1	Pc=comp1*comp2
+150 ~ -150 mV	0	1	0	1	0	Pb=com1'*comp2
-150 ~ -400 mV	0	0	1	0	0	Pa=(comp1+comp2)'

As triangle wave generator, we use a simple circuits shown in Fig. 4-11. The circuits has operational amplifier, resistor, capacitor, switch, comparator and S-R latch. It uses resistor and capacitor to charge and discharge. There are two states in Fig. 4-11. First, Vout+ is charged to the voltage of Vr+ and Vout- is discharged to the voltage of Vr- at the same time. Second, Vout+ is discharged to the voltage of Vr- and Vout- is charged to the voltage of Vr+ at the

same time For example, if Vout+ is charged to reach the value of Vr+ and Vout- is discharged to reach the value of Vr-, S-R latch send signals to sw1 and sw2. Then Vout+ become to discharge and Vout- become to charge.

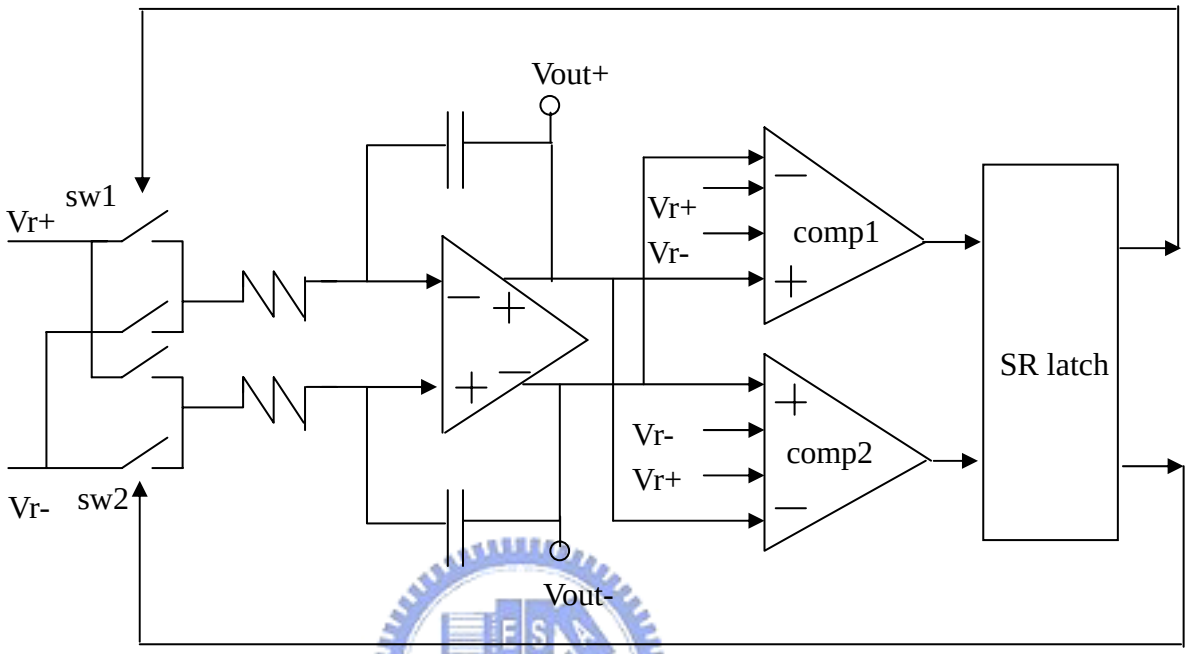


Fig. 4-11, Triangle wave generator

The simulation of triangle wave generator is shown in Fig. 4-12. One signals is Vout+ and another is Vout-. The full rang is in 0.7 mV and 1.1 mV.

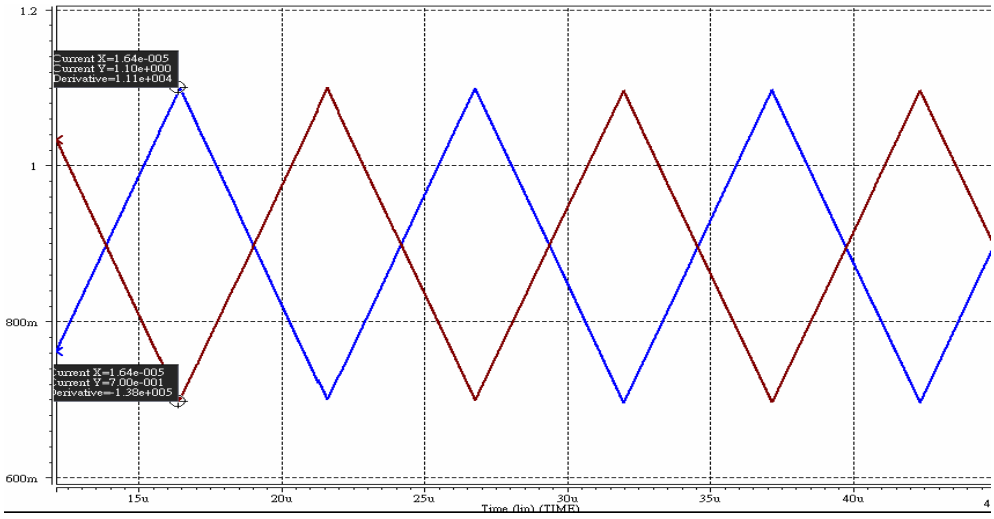


Fig. 4-12, Simulation of triangle wave generator

Chapter 5

Experimental Results and Layout

5.1 Simulation Results of ADC

In the section, we show the simulation of ADC. We generate a ramp signal of input to the input of pipeline ADC. And, we send 50 MHz clock. Then, we use matlab to calculate DNL and INL from digital output code. The ramp signal is shown in Fig. 5-1. The digital output codes are shown in Fig. 5-2. The relation of real output value and digital output code are as (48). The real output value is decrease from 255 to 0. Every value must emerge from 255 to 0 one time.

$$Output = out7*128 + out6*64 + out5*32 + out4*16 + out3*8 + out2*4 + out1*2 + out0*1. \quad (48)$$

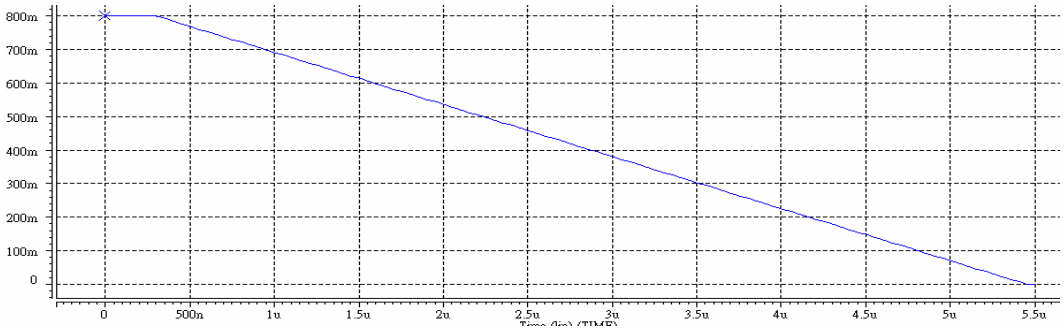


Fig. 5-1, Ramp signals

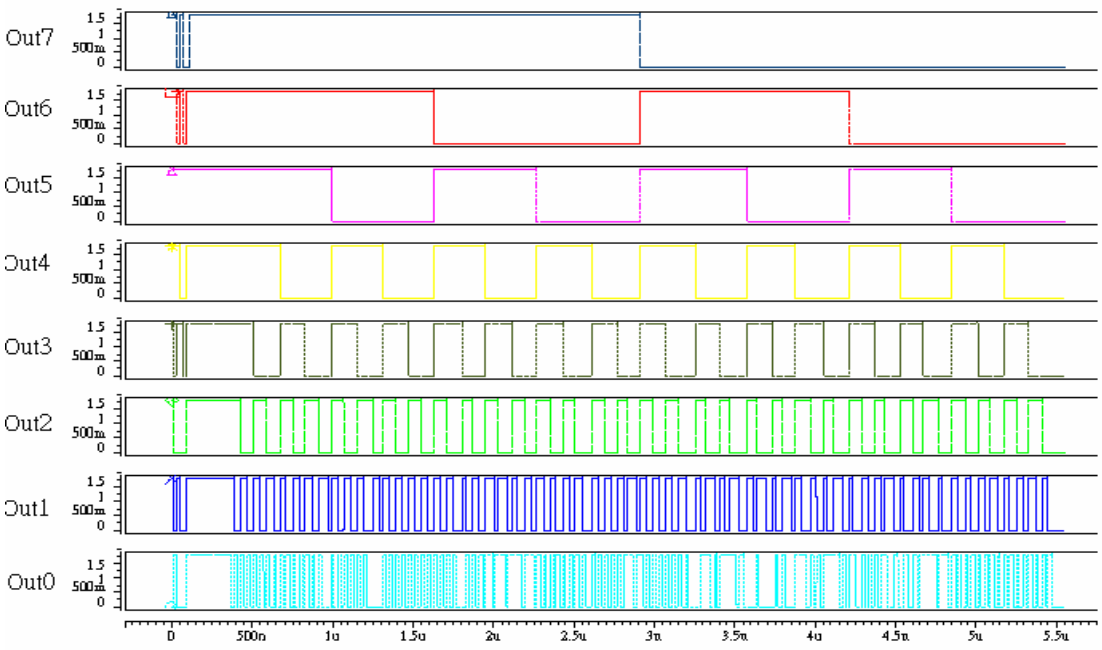


Fig. 5-2, Digital output codes

We send a slow ramp signals to the pipeline ADC. The output value decreases from 255 to 0. Every value must occur ten times ideally. We use matlab to calculate DNL and INL from digital output code. DNL is shown in Fig. 5-3. IDNL is shown in Fig. 5-4

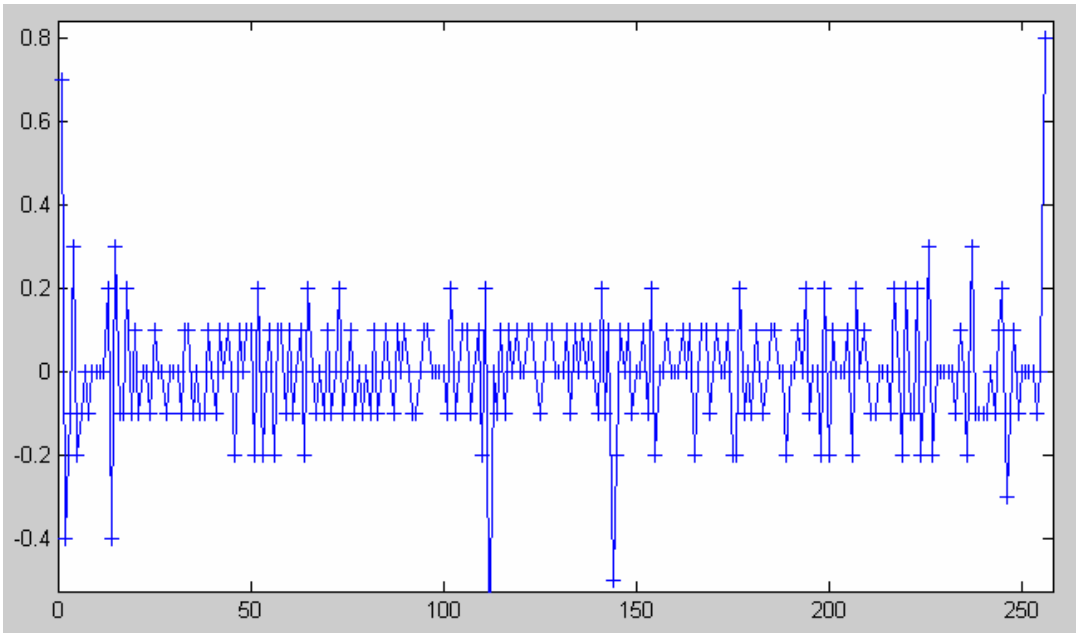


Fig. 5-3, DNL

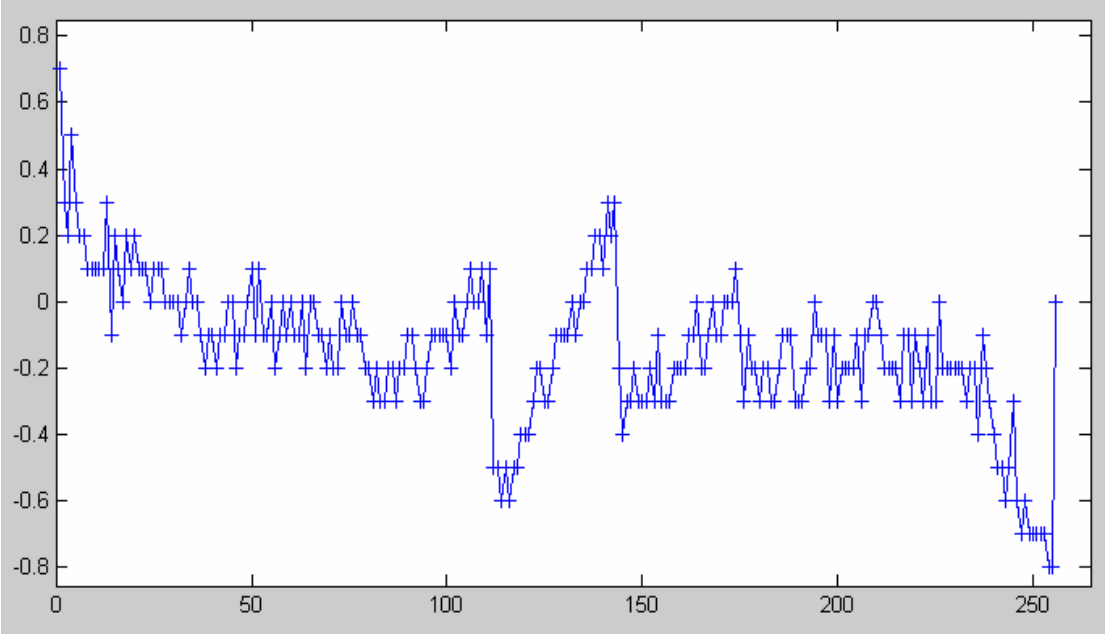


Fig. 5-4, INL

The characters of ADC are shown in Table 5-1.

Table 5-1, Characters of ADC

Supply Voltage	1.8 V
Resolution	8 bit
Sampling rate	50 MS/s
I/P dynamic range	0.8 V (p-p)
1 LSB	3.125 mV
DNL	0.8 LSB
INL	0.8 LSB
Offset error	0.7 LSB
Gain error	0.8 LSB

5.2 Simulation Results of BIST

In the section, we simulate the result that offset error or gain error happen in one stage. For example, we suppose that stage 1 has offset error (k mV) and other stages are ideal. We calculate probability of Pa1' and Pb1' and Pc1'. Then, we use Table 4-3 to calculate it's offset error and compare it with our suppose.

Therefore, there are seven simulations. Offset error of stage 1 is shown in Table 5-2. Offset error of stage 2 is shown in Table 5-3. Offset error of stage 3 is shown in Table 5-4. Offset error of stage 4 is shown in Table 5-5. Gain error of stage 1 is shown in Table 5-6. Gain error of stage 2 is shown in Table 5-7. Gain error of stage 3 is shown in Table 5-8.

Table 5-2, Compare offset error of stage 1

K mV Offset we suppose	2	4	6	8	10
Offset for probability	2.0313	4.0625	5.9375	7.9688	10

Table 5-3, Compare offset error of stage 2

K mV Offset we suppose	2	4	6	8	10
Offset for probability	1.875	3.75	6.25	8.125	10

Table 5-4, Compare offset error of stage 3

K mV Offset we suppose	4	8	12	16	20
Offset for probability	5	7.5	12.5	15	20

Table 5-5, Compare offset error of stage 4

K mV Offset we suppose	20	40	60	80	100
Offset for probability	20	40	60	80	100

Table 5-6, Compare gain error of stage 1

α gain error we suppose	0.2	0.4	0.6	0.8	1
α gain error for probability	0.19214	0.40367	0.5933	0.8	1

Table 5-7, Compare gain error of stage 2

α gain error we suppose	0.2	0.4	0.6	0.8	1
α gain error for probability	0.21053	0.36364	0.61538	0.8	1

Table 5-8, Compare gain error of stage 3

α gain error we suppose	0.2	0.4	0.6	0.8	1
α gain error for probability	0.28571	0.28571	0.61538	0.8	1

From Table 5-2 ~5-8, the offset error that we suppose and the offset error that calculate from probability are very approximate. They have a little difference which are because of sample point not enough.

5.3 Compare Simulation of BIST and ADC

We send a slow ramp signals to the 50 MHz pipeline ADC. First, we gather statistics which are signals of S/H, signals of DAC, signals of residue amplifier from each stage. Then we can calculate offset error and gain error of each stage, called it actual offset error and gain error.

Second, we gather statistical values Pai, Pbi and Pci from each stage. We can use Table 4-3 to calculate offset error and gain error called it probability offset error and gain error. Probability of ΔPai and ΔPbi and ΔPci from each stage are shown in Table 5-9.

Table 5-9, ΔPai and ΔPbi and ΔPci from each stage

Δ Pi	Probability	About offset error	About gain error
ΔPa1	-0.15625 %	-0.11719	
ΔPb1	0.078125 %		0.078125
ΔPc1	0.078125 %	0.11719	
ΔPa2	0.15625 %	0.097656	
ΔPb2	-0.11719 %		-0.11719
ΔPc2	-0.039063 %	-0.097656	
ΔPa3	0.15625 %	0.17578	
ΔPb3	0.039063 %		0.039063
ΔPc3	-0.19531 %	-0.17578	
ΔPa4	0.41016 %	0.35156	
ΔPb4	-0.11719 %		-0.11719
ΔPc4	-0.29297 %	-0.35156	

Use Table 4-2, we can separate △Probability from offset error and gain error. Then, we can calculate offset error and gain error from probability. Therefore, we compare actual offset error and gain error with probability offset error and gain error. It is shown in Table 5-10 and 5-11.

Table 5-10, Compare actual offset error and probability offset error

	Stage 1	Stage 2	Stage 3	Stage 41
Probability offset error	0.9375 mV	-0.44643 mV	-0.72581 mV	-1.4173 mV
Actual offset error	0.80327 mV	-0.15892 mV	-0.41373 mV	-1.2126 mV

Table 5-11, Compare actual gain error and probability gain error

	Stage 1	Stage 2	Stage 3
Probability gain error	-0.019082	0.025793	-0.0084122
Actual gain error	-0.013811	-0.013792	-0.1282

The difference of actual offset error from and probability offset error is less then 0.3 mV. We can accept this value.

The difference of actual gain error from and probability gain error from stage 1 is about 0.006. The difference actual gain error from and probability gain error from stage 2 is about 0.039. But the difference of actual gain error from and probability gain error from stage 3 is about 0.12. This larger error could be introduced by accumulative of previous two stages.

5.4 Layout Consideration

5.4.1 Capacitor Array

In S/H circuits and residue amplifier circuits, we need high accuracy capacitor. We use MIM structure to realize the capacitor. It is shown in Fig 5-5.

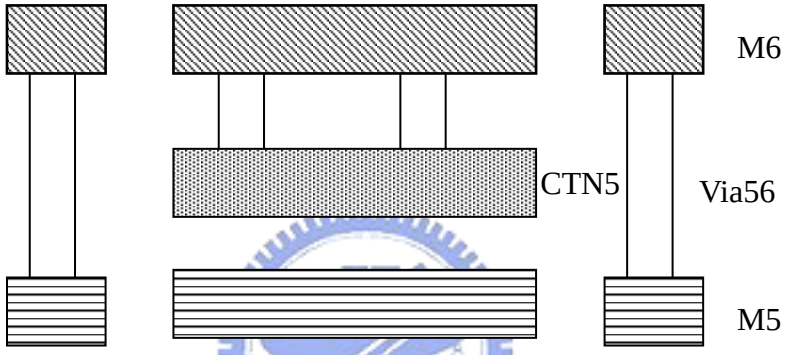


Fig 5-5, MIM capacitor

5.4.2 Consideration Operational Amplifier

Operational amplifier is very sensitive the mismatch of size. Therefore, the differential pair must layout transistor matching. It is shown in Fig. 5-6.

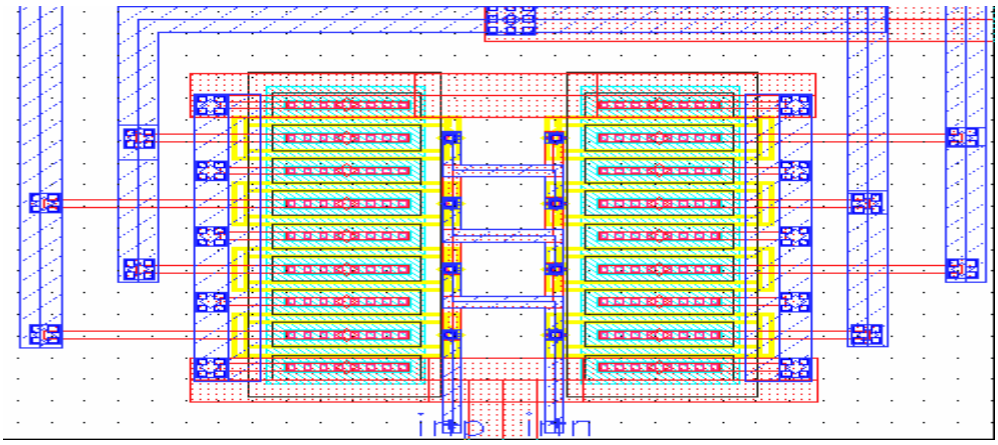


Fig. 5-6, Differential pair layout

5.4.3 Layout and Pad

The simple graph of layout is shown in Fig.5-7. We place ADC circuits on the left side. Clock generator, digital error correction and BIST circuits are on the right side. The area of layout is 2000u*1400u. There are 30 pads, six of input, twenty of output, two of gnd and two of vdd. They are in Table 5-12. The layout is shown in Fig.5-8.

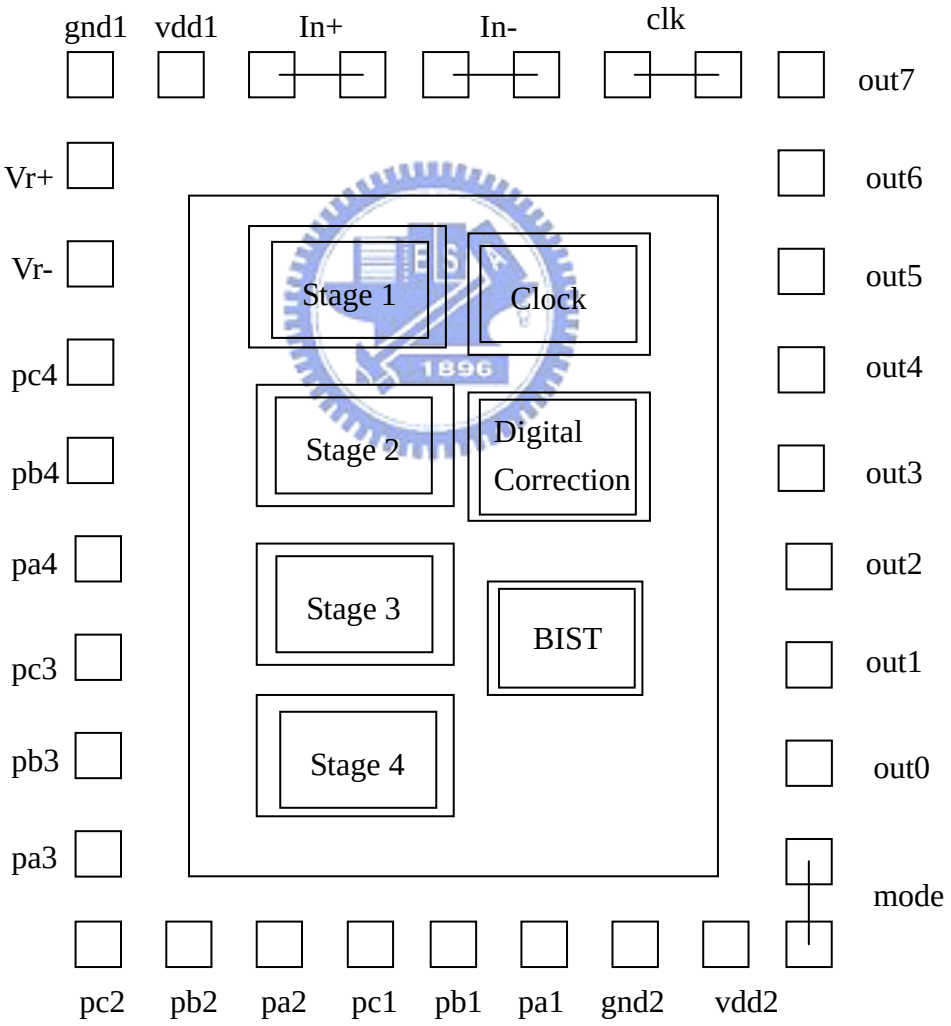
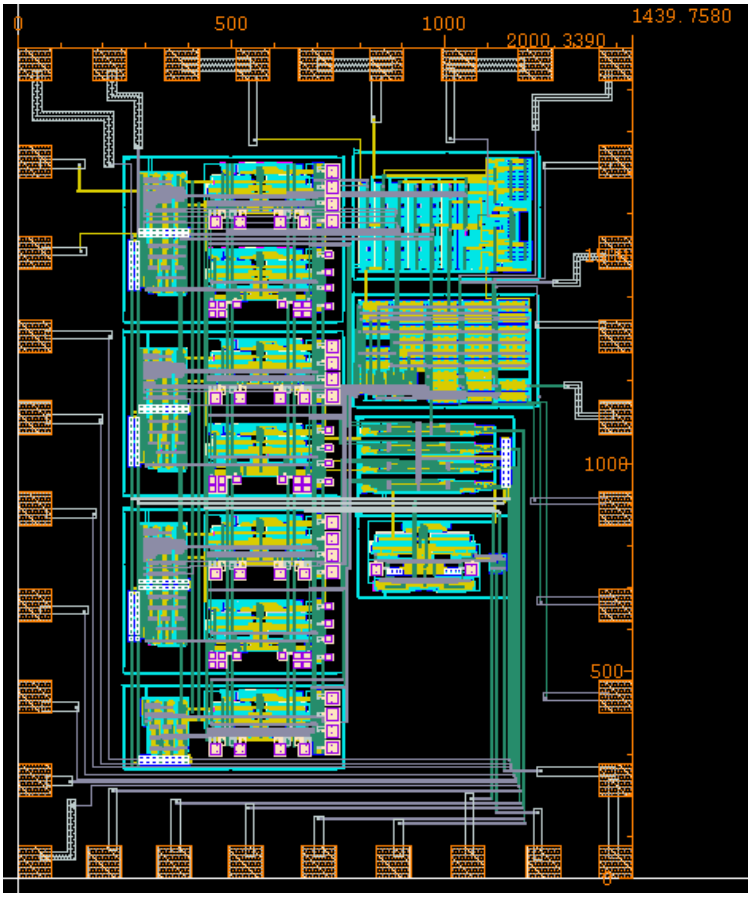


Fig. 5-7, Simple graph of layout

Table 5-12, Pad of layout

6 input	Iin+, In-, clkin, mode, Vref+, Vref-.
20 output	Out7 ,Out 6 ,Out 5 ,Out 4 Out 3 ,Out 2 ,Out 1 ,Out0, pa1 ,pb1 ,pc1, pa2, pb2, pc2, pa3 ,pb3, pc3, pa4, pb4,pc4
4 vdd/gnd	vdd1, gnd1, vdd2, gnd2

Fig.5-8, Layout of chip



Chapter 6

Conclusion and Future Work

6.1 Conclusion

This paper is propose a built-in self-test to test the pipeline ADC. We design a 8-bit, 50 MS/s pipeline ADC first. The DNL of ADC is 0.8LSB and INL of ADC is 0.7LSB. Second, we bring up new a approach about BIST circuits to test pipeline ADC. We use probability to gather statistical values to test offset error and gain error in each stage. The chip of ADC and BIST circuits is realize by TSMC 0.18 um 1p6M. The simulation result of BIST can meet our requirement.

6.2 Future Work

For the analysis of BIST circuits, we can calculate probability to calculate offset error and gain error in each stage. We suggest the follower can calculate probability to calculate the DNL and INL of ADC to use the BIST architecture. Improve the analysis for BIST and get better performance.

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