國 立 交 通 大 學

光電工程研究所

博士 論 文

閘極介電層於矽通道與鍺通道金氧半場效電晶體之研究

Study of Thin Gate Dielectrics on Silicon and Germanium MOSFETs

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摘要

本論文探討閘極介電層於矽型與鍺型場校電晶體的應用。本文首先討論氮輪廓分佈(Nitrogen profile)與記憶應力記憶技術(stress memorization technique, SMT)於超薄氮氧化矽介電層於 45 奈米矽型場效電晶體之影響。在氮輪廓分佈於超薄氮氧化矽介電層的研究中，發現即使具有相同等效氧化層厚度的氮氧化矽介電層，其氮輪廓分佈仍會對閘極穿隧漏電流造成影響。而且閘極穿隧漏電流隨著氮輪廓分佈越傾斜而越大。另外相較於負型(n-type)場效電晶體，正型(p-type)場效電晶體增加的幅度更大。本文以 WKB 近似為理論基礎，建立一直接穿隧漏電流物理模型。此模型透過建立介電常數、能帶彎曲程度與有效載子穿隧質量對於氮輪廓分佈變化而得以合理解釋氮輪廓分佈對於正負型場效電晶體的影響。另外在記憶應力記憶技術於超薄氮氧化矽介電層研究中，本文發現異常

的閘極漏電流因記憶應力記憶技術增加。本文利用載子分離量測法，鑑定出異常的閘極漏電流來自於載子經由閘極流向源極/汲極區。另外本文亦發現記憶應力記憶技術會導致閘極與源極/汲極的耦合電容增加的現象。實驗結果顯示高伸張應力導致源極/汲極的輕摻雜區(LDD)因而延伸與邊際閘極區域破壞，並引起異常高閘極穿隧漏電流。

在閘極介電層於鍺型場校電晶體的研究中，本文提出以高壓水方式對鍺型元件施予處理。為了清楚釐清高壓水對於鍺型元件中的各層薄膜的影響，本文逐步在二氧化矽於鍺基板研究高壓水對鍺基板的影響；在二氧化鋯於矽基板中研究高壓水對二氧化鋯的影響；最終實現高壓水對二氧化鋯於鍺基板處理。在二氧化矽於鍺基板研究中，經高壓水處理後的元件顯示出較平坦的表面特性與抑制電容-電壓中頻率發散(frequency dispersion)現象。而且本文發現以高壓水處理經高溫退火後的元件可以降低其漏電流。在二氧化鋯於矽基板的研究中，經高溫退火處理後的元件會因二氧化鋯結晶而導致漏電上升。經過高壓水處理後的元件，其閘極漏電流、電容遲滯現象(hysteresis)和等效電容厚度(capacitance-equivalent thickness, CET)明顯下降。其推斷源自於二氧化鋯中晶粒的缺陷與靠近矽基板的邊緣缺陷(border traps)經高壓水處理而被修復。最後研究高壓水對二氧化鋯於鍺基板上的影響。本研究發現以高壓水處理二氧化鋯於鍺基板的元件，可消除介於二氧化鋯和鍺基板中間層形成物-低氧化鍺(Ge suboxide)。在沉積或熱製程所形成的低氧化鍺會造成閘極漏電增加，也會使閘極控制能力下降。電子能譜儀(X-ray photoelectron spectroscopy)和高解析度場效電子顯微鏡(high-resolution transmission electron microscopy)的分析也驗證高壓水處理可以消除低氧化鍺。經研究發現此物理機

制主要由於水氧化未完全氧化的氧化鋯，並其所生成的氫進一步與低氧化鍺還原成鍺。而且經高壓水處理後，二氧化鋯-鍺電容元件的閘極漏電流下降 1000 倍。

除此之外，本論文也在快速爐管退火製程中添加水和氫氣，並研究其對二氧化鋯於鍺基板的影響。實驗結果顯示，在適當的退火溫度下添加水與氫氣可有效地抑制低氧化鍺的生成並抑制閘極漏電流。但是當快速退火爐管製成達到 500 度時，氫氣會因劇烈的氧化還原反應造成鍺表面不平整，甚至出現孔洞現象。

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Abstract

This work focuses on characterization of thin gate dielectrics on silicon (Si) and germanium-based (Ge-based) metal-oxide-semiconductor field-effect transistor (MOSFET). First, the impacts of nitrogen profile (N profile) and stress memorization technique (SMT) on ultrathin oxynitride (SiON) for 45-nm Si-based MOSFETs application are investigated. The dependence of the gate tunneling current (J_G) on N profile within an ultrathin SiON film was observed. It was found that gate tunneling current is dependent on N profile, even with equal oxide thickness and nitrogen dosage. Gate tunneling current increased with steeper N profile, and it had higher sensitivity for p-type MOSFET than n-type MOSFET. A direct tunneling model based on Wentzel-Kramers-Brillouin approximation has been proposed. The model

described the influence of N profiles on gate tunneling current through local change of dielectric constant, band bending, and effective mass. Also, it reasonably explained the different J_G sensitivity in n-/p-MOSFETs, a phenomenon that has not been addressed in earlier publications. Then, anomalously high gate tunneling current, induced by high tensile SMT is reported in this work. Carrier-separation measurement method shows the increased gate tunneling current is originated from the higher gate-to-source/drain tunneling current, which worsens when channel length is getting shorter. Also, the device with enhanced tensile strain exhibits 9% higher gate-to-source/drain overlapping capacitance. These data indicate the anomalously high gate tunneling current could be attributed to the high tensile strain that induces the effects of excessive lightly-doped drain-source (LDD) dopant diffusion and higher gate edge damage. The proposed inference is confirmed by channel hot electron stress.

Then, high-pressure (HP) H_2O treatment at low temperature (100~150 ℃) has been proposed to treat Ge MOS devices. The effect of high-pressure H_2O treatment on Ge MOS devices is examined step-by-step to discriminate the influence on individual layer within Ge MOS capacitor. The HP H_2O treatment was respectively performed on SiO_2/Ge stack for exploration of Ge substrate, on ZrO_2/Si for exploration of ZrO_2 thin film and finally realized on ZrO_2/Ge capacitors. In the investigation of SiO_2/Ge MOS devices, a smooth interfacial GeO_2 layer between gate SiO_2 and Ge is formed after H_2O treatment, and the frequency dispersion of capacitance-voltage characteristics is also effectively alleviated. Furthermore,

the electrical degradation of Ge-MOS after a post-gate dielectric annealing at 450 ℃ can be restored to an extent similar to the initial state. In the investigation of ZrO_2/Si MOS devices, the dramatic increase of J_G for ZrO_2 dielectrics after rapid thermal annealing (RTA) at 500 ℃ was found and attributed to defective grain boundaries induced by thermal crystallization. After high-pressure H_2O treatment, the hysteresis, gate leakage current and capacitance-equivalent thickness (CET) reduces in ZrO_2/Si capacitor. It is inferred that the HP H_2O treatment passivates the border traps in ZrO_2 nearby Si substrate and defective grain boundary regions in the bulk of ZrO_2. The HP H_2O treatment was finally realized on the sputtered ZrO_2 upon Ge substrate. This investigation demonstrates the effect of HP H_2O treatment on the elimination of the interfacial germanium suboxide (GeO_X) layer between ZrO_2 and Ge. The formation of GeO_X interlayer increases the gate leakage current and worsen the controllability of the gate during deposition or thermal cycles. X-ray photoelectron spectroscopy and high-resolution transmission electron microscopy reveal that HP H_2O treatment eliminates the interfacial GeO_X layer. The physical mechanism involves the oxidation of non-oxidized Zr with H_2O and the reduction of GeO_X by H_2. Treatment with H_2O reduces the gate-leakage current of a ZrO_2/Ge capacitor by a factor of 1000.

In the other way, the effects of H_2O and H_2 ambiences for RTA system on sputtered ZrO_2 upon Ge substrate are reported in this work. The experimental results reveal that H_2O or H_2 in RTA process effectively suppress GeO_X formation and release degradation of gate leakage

current at appropriate process temperature. However, when the temperature of RTA treatment reaches at 500 ℃, the aggressive oxidation-reduction reaction in H_2 ambience cloud cause uneven surface and voids at the interface between ZrO_2 and Ge substrate.

誌謝

在此篇論文完成之際，我開始回想所經歷過的研究生涯。回想當初繼續攻讀博士學位的原因，只是一個簡單的理由:因為我還有許多不懂，想再多了解一些。而在經過這些年後，再度檢驗自己，覺得自己好像多懂了一些，但是好像又發掘更多不明瞭之處，這才知道原來科學是這麼深奧與廣大，而自己的研究只是眾多領域中之小小一處，更體悟到一人之力難成大事。首先，感謝多年來細心指導我的劉柏村教授，感謝劉老師在學術上的指導，總是在學涯迷惘時給予適當貼切的提攜；感謝劉老師給予相當大的空間，能盡情發揮所學，讓學生勇敢嘗試;感謝劉老師提供許多機會，讓學生具有業界實務經驗，了解業界與學界差異性，並提供平台讓兩者融合；另外，因劉老師而所聚集的實驗室大家庭，形成的舒適研究環境，使得學生能快樂在這個地方學習。

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Chapter 1

Introduction

1.1 Revolution and challenges of gate dielectric on Si-MOSFETs

Scaling solid-state devices has great benefits to the cost, performance, and power consumption for electronic products application. In order to achieve this purpose, the microelectronics industry has driven transistor feature size scaling from 10 μm to about 30 nm during the past 40 years [1], as shown in Fig. 1-1. According to empirical observation by Moore, the component density and performance of integrated circuits doubles every year and then was revised to doubling every two years [2]. The scaling of electronic solid-state devices seems to never stop and the physical limitations are being continuously broken with great effort.

Device downscaling for gate dielectric was initially achieved by simply reducing the physical thickness of SiO_2. The downscaling of device thickness causes gate tunneling-current to increase exponentially. Additionally, poor barrier of thin SiO_2 gate dielectric can't prvent boron penetration from heavy p-type doping of polycrystalline-silicon gate electrode to channel region and further results in performance degradation [3]. This poses incredible challenge to continue with device scaling. To overcome these issues, SiON was firstly adopted. Downscaling continues with the scaling of physical thickness and increasing nitrogen concentration within SiON. Nevertheless, the excessive nitrogen concentration poses

several issues to device and reliability, such as severe threshold voltage shift, degraded mobility and reliability of Negative-Bias-Temperature-Instability (NBTI).[4] Hence, the need to control N-profile in ultra-thin SiON becomes more and more critical [5]. Successful N-profile engineering will definitely alleviate the issues mentioned [6].

With aggressive scaling of gate dielectric, the physical limitation of the conventional SiO_2 or oxynitride as gate dielectric has reached the point where films thickness are only a few atomic layers thick. Below the physical thickness of 1.5 nm, the gate leakage current exceeds the 1 A/cm^2 and can't follow to demand of International Technology Roadmap for Semiconductors (ITRS) in 2011, namely 1.2 nm for effective-oxide thickness (EOT) and 0.9 A/cm^2 for gate leakage current. To solve this critical issue, the high-κ gate dielectric have been introduced, such as hafnium, zirconium and aluminum based oxide, as shown in Fig. 1-3 [7]. Although, a large amount of effort has been paid to integrate high-κ dielectric to Si-based MOSFETs, many critical issues still remain. Besides having a sufficiently large dielectric constant, there are also several critical requirements must be taken into consideration. Those involves (i) thermodynamic stability in contact with Si and gate electrode; (ii) kinetic stability against Si and the gate electrode during thermal process; (iii) appropriate band offset with Si, as shown in Fig. 1-4 [8]; (iv) low interface states between dielectric and Si ; (v) low bulk defects in high-κ dielectric itself to prevent flat-band (V_{FB}) and threshold (V_{TH}) shift and (vi) hysteresis free during device operation [9, 10].

The integrity of gate dielectric involves not only issue of gate dielectric but also external mechanical strain. Furthermore, introduction of stressors to boost mobility has received a lot of attention in recent years. Therefore, the impact of stressors on gate dielectric should be taken into consideration. Stressors can be introduced in two key forms, the substrate-strain based and the process-induced strain based. The substrate-strain based makes use of material with different lattice spacing, such as SiGe/Si epitaxial stack, to generate biaxial strain in the channel. This method introduces a global strain to the substrate. It boosts mobility effectively, at the expense of higher cost [11]. On the other hand, the process-induced strain based method provides a lower cost solution. They could appear in the forms of shallow trench isolation (STI), contact etching stop layer (CESL) and stress memorization technique (SMT), which introduce uniaxial strain to boost mobility [12-15]. The mechanical strain not only enhance the mobility of carries in channel region, but also results in changes the gate tunneling current by altering the out-plane mass and SiO_2/Si barrier height. Moreover, the change of strain will make a great impact on the gate tunneling current [11]. Previous articles have reported the reduction of gate tunneling current by introducing the tensile strain in nMOSFETs [13, 16].

Although the mechanical strain improves the Si-MOSFET performance by boosting carriers' mobility, the mobility enhancement by stain is subject to limitation. Alternative channel materials, such as Ge, GaAs, InSb and InP, are therefore investigated to obtaining high mobility device. Among high mobility material, Ge is the most promising candidate for

next generation devices [17].

1.2 Revolution and challenges of gate dielectric on Ge-MOSFETs

Germanium (Ge) semiconductor has been considered as a new channel material in replace of silicon (Si) for future high-performance CMOS technology, because its higher carrier mobility for both electrons and holes, lower dopant thermal activation energies for shallower junction formation and compatible fabrication processes with existing silicon manufacturing infrastructure. However, the Ge-MOS technology still has many challenges and not been widely deployed due to (1) high defect states at the interface between high-k dielectric and Ge channel, (2) Ge diffusion and incorporation into high-K dielectric during thermal process, (3) low solid solubility of n-type dopant, (4) high diffusibility of source/drain (S/D) dopant and (5) high drain junction leakage current [17].

The most critical issue hindering the development of gate dielectric on Ge is lack of high quality and stable Ge insulation oxide comparable to silicon dioxide (SiO_2) for silicon. In fact, the poor native Ge oxide has been formed immediately after wet chemical pre-clean or exposure to thermal oxygen ambient, such as thermal dielectrics deposition process. The native Ge oxide consists of GeO_2 and GeO. The GeO_2 exhibits excellent interface quality and non-volatility. Unfortunately, the GeO is easy sublimation up to about 400 ℃ and the transformation of GeO_2 to GeO proceeds by thermal annealing. ($GeO_2+Ge \rightarrow 2GeO_{(g)}$ at about 400 ℃) The other serious problem is Ge thermal diffusion into gate dielectric insulators

resulting in gate leakage current increase. These issues cause it to be difficult to implement the gate-first process in Ge-MOS technology.

The engineering of gate dielectric on Ge substrate can be classified into several categories for different purposes. For pre-gate clean, one of the effective methods to decrease the amount of Ge oxide is HF pretreatment at high concentration (about 20%). However, a certain Ge suboxide (GeO_X, X<2) remains even after the pretreatment. More investigations have reported in previous articles [18-20].

Various pre-gate surface modification techniques, such as surface nitridation or Si passivation, have been developed to improve the quality of gate dielectric/Ge interface [17]. It was also reported that high-performance Ge MOSFET could be realized by careful control of interfacial GeO_2 formation [21]. Whether GeO_2 interlayer improves the electric performance of high-k/Ge substrate or not depends on the sequent process. Decomposition of GeO_2 after high thermal process even causes poor interface quality and higher leakage current in Ge-based MOS. Additionally, the physical property of high-k dielectric could be alternated through intentional incorporation, such as Si, N, Ge and La. The thermal stability of Hf or Zr-related dielectric could be improved through silicate formation or nitridation to prevent degradation of gate leakage from Ge diffusion. It has also be reported the phase of crystalline for ZrO_2 transform into tetragonal phase by Ge or La incorporation and corresponding dielectric constant reached around 44 [22-24].

1.3 Motivation

With aggressive scaling for high performance Si-MOSFETs application, the SiON was adopted to replace SiO_2 as gate dielectric until to 45-nm generation. The control of nitrogen profile in SiON is necessary to prevent reliability issue from excessive nitrogen concentration at the interface of dielectric and Si substrate. Numerous models have been proposed to explain the dependence of nitrogen dosage on gate tunneling current [25-27]. However, little attention has been paid to study the influence of N-profile on the gate tunneling current. In this article, the effect of different N-profiles within an ultra-thin SiON on the eventual gate tunneling-current will be investigated and a model based on WKB approximation[28] will be proposed to explain the impact of N-profiles. For mechanical strain on SiON for 45-nm generation, previous articles have reported the reduction of gate tunneling current by introducing the tensile strain in nMOSFET [13, 16]. However, boosting nMOSFET mobility using SMT with high tensile strain, the gate tunneling current was also found to be increased in our work. In order to explore mechanism of gate current increase by SMT, a series of experiment had been examined in this thesis.

Ge semiconductor has been considered as an alternate channel material in replace of Si for future high-performance CMOS technology. However, the poor Ge native oxide hinders the application of Ge. Additionally, the thermal decomposition of GeO_2 at low temperature ($GeO_2+Ge \rightarrow GeO_{(g)}$ at about 400 ℃),[17] resulting in a high gate leakage current and a thick

effective oxide thickness (EOT) during thermal deposition or post-dielectric annealing. In this article, a high-pressure H_2O treatment is proposed at low temperature (100~150 ℃) to improve the interface of dielectric/Ge and release the degradation of gate leakage current after high PDA process. Base on the finding of high-pressure H_2O treatment, the H_2O and H_2 are added in rapid thermal annealing to suppress the GeO_X formation and lower gate leakage current.

1.4 Organization of the thesis

In this thesis, six chapters are organized to present the detail of aforementioned works. First the revolutions and challenges of gate dielectric on Si and Ge-based MOSFETs are introduced in the Chapter 1. The experimental instrument, analysis method and parameter extraction are described in Chapter 2. Then, the impacts of nitrogen profile and high tensile mechanical stress on ultra-thin SiON for 45-nm generation (Si-MOSFETs) are investigated in Chapter 3. Next, the Chapter 4 focuses on high-pressure H_2O treatment of gate dielectric on Ge substrate. After examination of high-pressure H_2O treatment, the effects of water vapor and hydrogen annealing on gate dielectric upon Ge substrate are also investigated in Chapter 5. Finally, the Chapter 6 gives the summaries and future work. The structure is in the other way listed below for indexing:

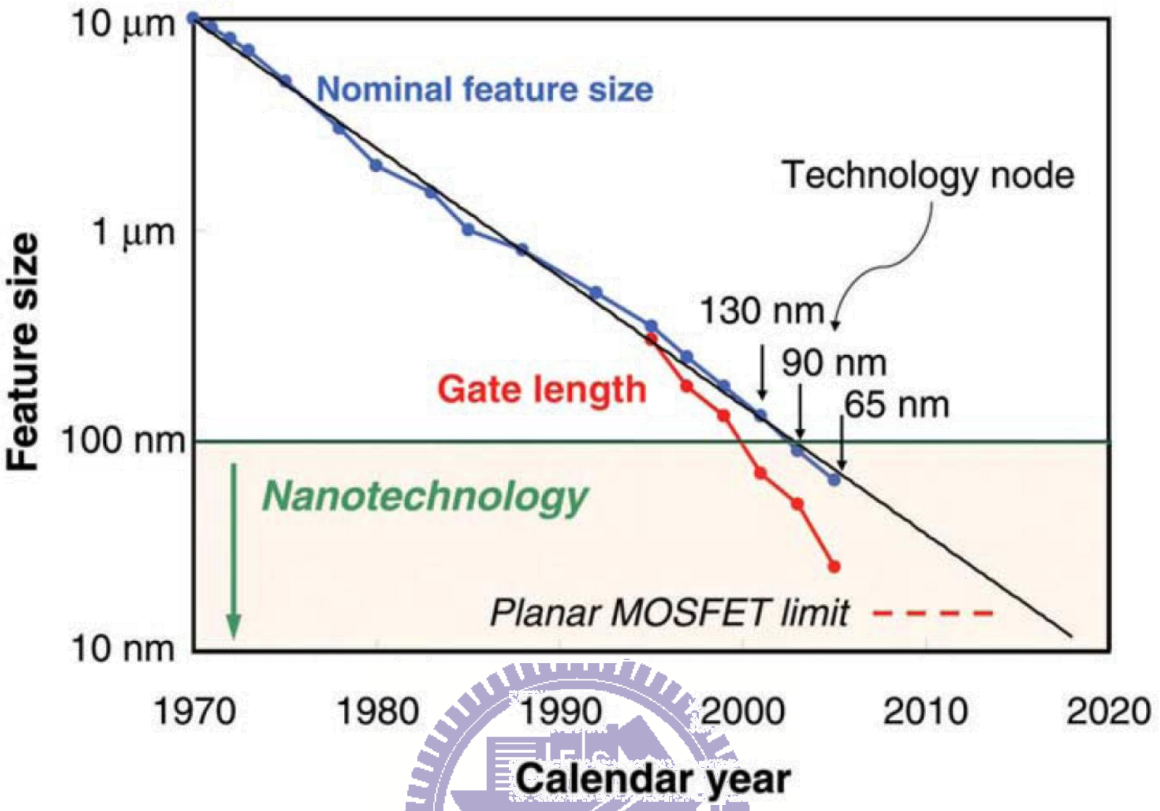

Figure 1-1 Logic technology node and transistor gate length versus calendar year.[1]

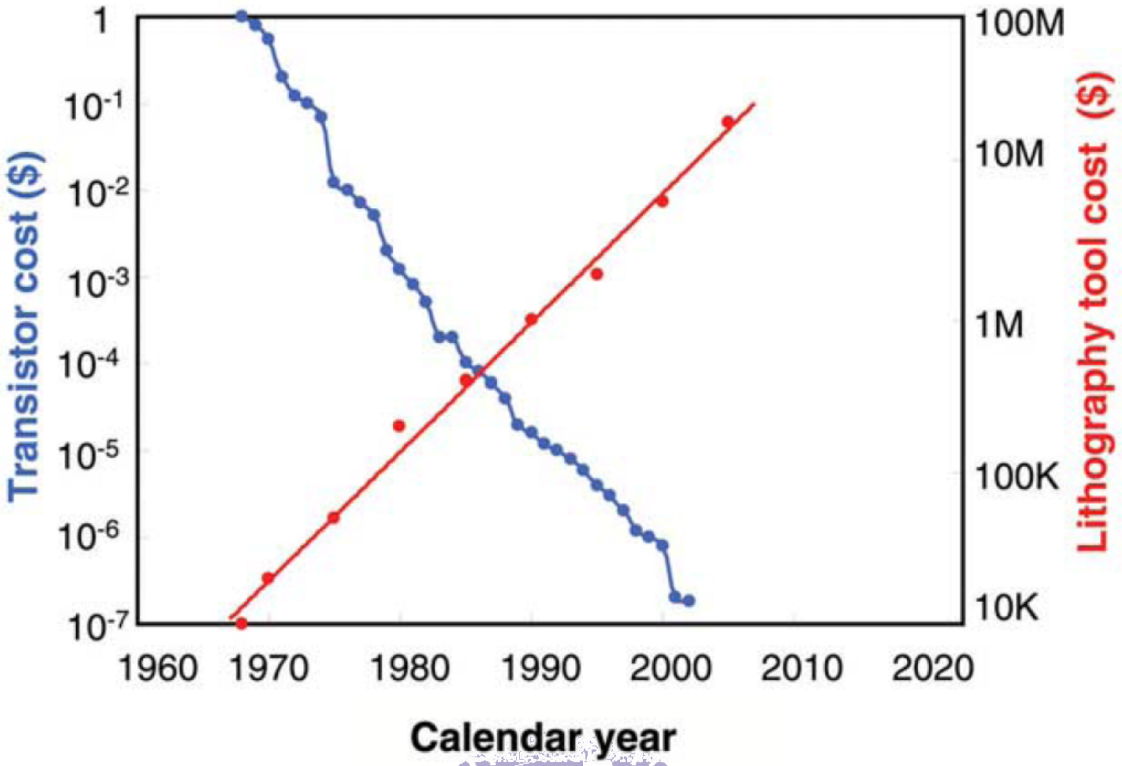

Figure 1-2 Transistor cost and lithographic tool cost versus years.[1]

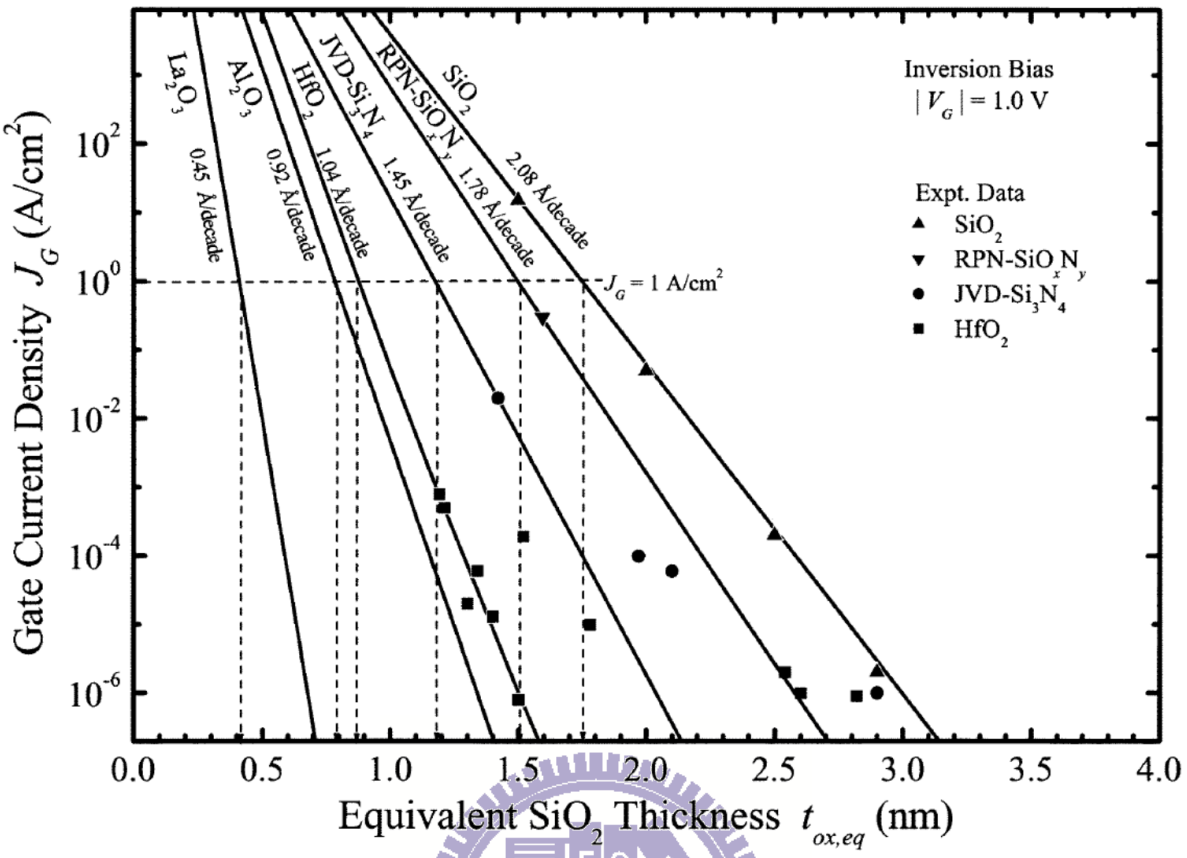

Figure 1-3 Gate-current density against effective-oxide thickness with various gate materials.[7]

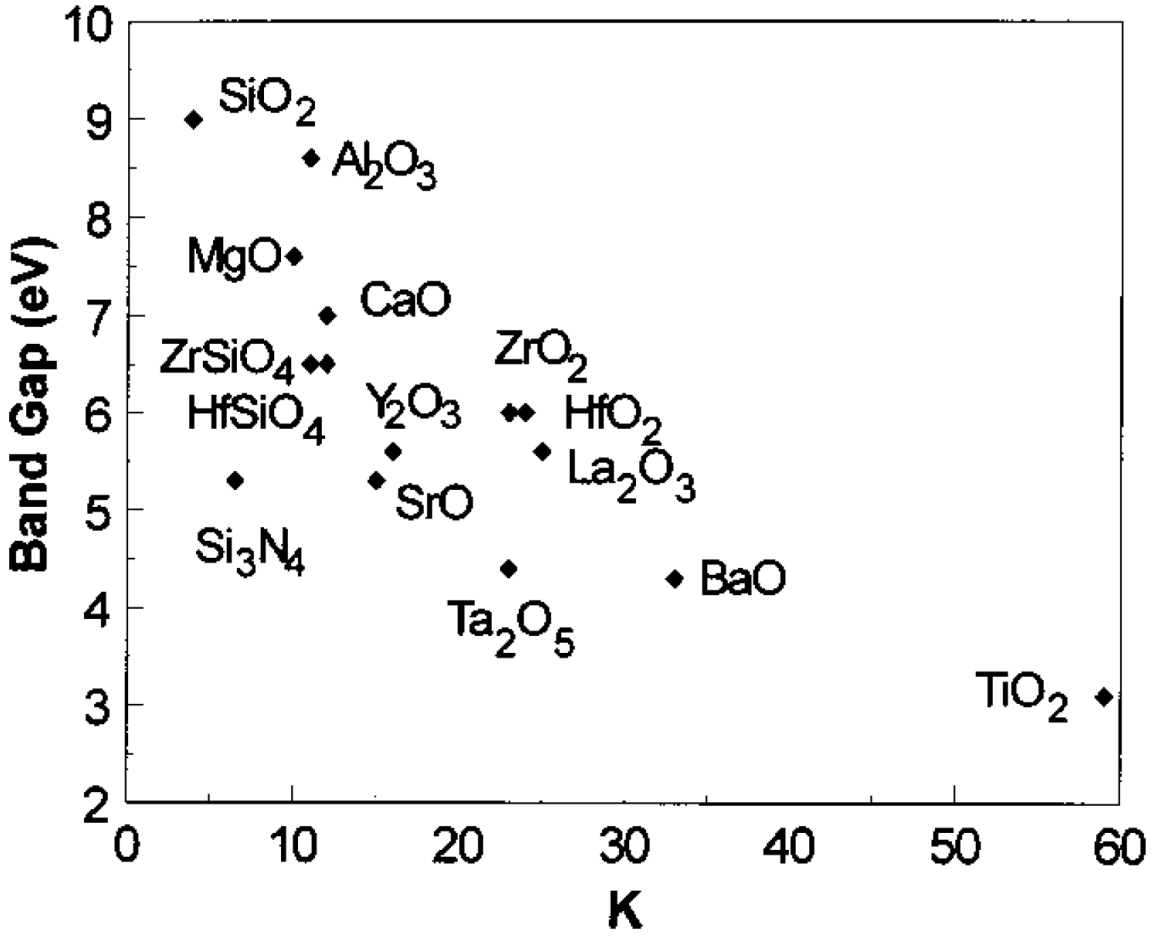

Figure 1-4 Correlation of dielectric constant with band gap of candidate [8].

	Ge	Si	GaAs	InSb	InP
Bandgap (eV)	0.66	1.12	1.42	0.17	1.35
Electron affinity (eV)	4.05	4.0	4.07	4.59	4.38
μ_h ($cm^2V^{-1}s^{-1}$)	1900	450	400	1250	150
μ_e ($cm^2V^{-1}s^{-1}$)	3900	1500	8500	80000	4600
N_V (cm^{-3})	6.0×10^{18}	1.04×10^{19}	7.0×10^{18}	7.3×10^{18}	1.1×10^{19}
N_C (cm^{-3})	1.04×10^{19}	2.8×10^{19}	4.7×10^{17}	4.2×10^{16}	5.7×10^{17}
Lattice constant (nm)	0.565	0.543	0.565	0.648	0.587
Dielectric constant, k	16.0	11.9	13.1	17.7	12.4
Melting point, T_m (°C)	937	1412	1240	527	1060

Table 1-1 Material characteristics of alternative channel materials.[17]

Chapter 2

Experiments

Before going deep into the characterization of gate dielectric on Si and Ge MOSFETs, The experimental instrument, analysis method and parameter extraction are described in this chapter.

2.1 High-pressure H_2O system

In this work, a high-pressure H_2O treatment is proposed as a post-gate dielectric treatment at 100~150℃ to improve the electrical performance of gate dielectric on Ge substrate. Figure 2-1 shows the proposed high-pressure system. High-pressure H_2O treatment was conducted using supercritical carbon dioxide ($SCCO_2$) fluid that was mixed with 10 volume % of propyl alcohol and 10 volume % of pure H_2O at 100~150 ℃ for 1 hour. In this section, author will introduce the properties of $SCCO_2$ and high-pressure H_2O.

A supercritical fluid can be defined as a substance heated above its critical temperature (T_C), and which is also compressed above its critical pressure (p_C). At the critical point, the fluid phase boundary between liquid and gaseous phase vanishes, and the properties of the new single “supercritical” phase are best described as a combination of those of liquid and gaseous phase.[29] Therefore, supercritical fluid provides good liquid-like solvency and high gas-like diffusivity, giving it excellent transport capacity.

In this work, author used $SCCO_2$ for carrier of H_2O due to its low T_C (30 ℃), p_C (1072

psi) and environmental benefits, such as no waste, no damage of ozone layer, non-carcinogenic, non-toxic and non-flammable. The properties of $SCCO_2$ are shown in Figs. 2-2 and 2-3. The solubility of H_2O rises with increasing the CO_2 pressure due to the density increase, as shown in Fig. 2-3. The propyl alcohol was used as a modifier to enhance the solubility of the polar H_2O molecules in nonpolar CO_2. The water was dissolved as small H_2O molecule clusters with propyl alcohol assistance and uniformly mixed in $SCCO_2$ fluid. The $SCCO_2$ fluid exhibited a liquid-like property, giving it an excellent transport capacity. Also, supercritical fluid has gas-like properties and efficiently diffuses into nanoscale structures without damage. Therefore, the H_2O effectively reacts with the thin film when dissolved in $SCCO_2$.

It is also noted that high-pressure H_2O has quit different properties to ambient. Figure 2-4 shows the ionic product of water at high temperature and high pressure.[29] The amounts of ionic products, $H3O^+$ and OH^+ radicals, in H_2O at high pressure may be orders of magnitude higher than those obtained in ambient water. The higher amounts of free radicals are associated with a strengthened oxidation reaction between H_2O and non-oxidized thin film owing to the higher collision frequency.

2.2 X-ray photoelectron spectroscopy

Of all the contemporary surface characterization methods, X-ray photoelectron spectroscopy (XPS) is the most widely used. XPS is also called electron spectroscopy for

chemical analysis (ESCA), and the two acronyms can be used interchangeably. The popularity of XPS as a surface analysis technique is attributed to its high information content, its flexibility in addressing a wide variety of samples, and its sound the sound theoretical basis. XPS analysis provides useful information such as composition, chemical state, and thickness etc. of thin films. In this article, author used XPS analysis to exanimate the composition-depth profile and chemical states of gate dielectric on Ge substrate with various post gate treatment and further discriminate the chemical reaction within gate dielectric. The brief principle and main functions of XPS used in this article will be introduced as following content.

The principle of XPS is based on the photoelectric effect outlined by Einstein in 1905 where the concept of the photon was used to describe the ejection of electrons from a surface when photons impinge upon it. This process can be expressed by the following equation,[30]

$$E_B^{vac} = hv - KE + \phi_e \quad (1)$$

Where E_B is the binding energy of the electron in the atom, hv is the photon energy of X-ray source, KE is the kinetic energy of the emitted electron that is measured in the XPS spectrometer and ϕ_e is the spectrometer work function. The energy of the photoelectrons leaving the sample is determined using an analyzer and this gives a spectrum with a series of photoelectron peaks. The binding energy of the peaks is characteristic of each element. The peak areas can be used to determine the composition of the materials surface. The shape of each peak and the binding energy can be slightly altered by the chemical state of the emitting

atom. Hence XPS can provide chemical bonding information as well.[30]

In this article, the XPS analysis is mainly used to identify the oxidation state, such as ZrO_2 and GeO_X. Figure 2-5 shows the example of oxidation for Ge resulting in binding energy shift to high energy level. The shift of binding energy is attributed to higher electronegativity of oxygen, comparing to the other element. When oxygen atoms bond to other elements, electron of element will be drawn by oxygen and become more positively charged, resulting in an increase in binding energy.[31]

2.3 Parameter extraction

There are three parameters were presented in characteristics of MOS capacitors, namely capacitance-equivalent thickness, flat-band voltage and hysteresis.

The capacitance-equivalent thickness (CET) is defined as following formula,

$$C_{acc} = \frac{\varepsilon_{SiO_2}}{CET} = \frac{\varepsilon_{Dielectric}}{d_{PHY}} \quad (2)$$

Where C_{acc} is measuring capacitance of per cm^2 at accumulation region, ε_{SiO2} is the permittivity of SiO_2, and $\varepsilon_{Dielectric}$ is the permittivity of gate dielectric deposited on Si or Ge substrate and d_{PHY} is the physical thickness of gate dielectric.

The flat-band voltage (V_{FB}) was extracted at flat-band capacitance (C_{FB}) given as following formula,

$$C_{FB} = \left(\frac{1}{C_{acc}} + \frac{1}{C_{D,FB}}\right)^{-1}, where\ C_{D,FB} = \frac{\varepsilon_{Substrate}}{L_D}\ and\ L_D = \sqrt{\frac{k\varepsilon_{Substrate}}{q^2 N_{Sub}}} \quad (3)$$

Where $C_{D,FB}$ is the capacitance at depletion region, $\varepsilon_{Sbustrate}$ is the permittivity of substrate, L_D

is Debye length and N_{sub} is the substrate doping concentration.

The value of hysteresis (ΔV_{FB}) was defined as difference of V_{FB} for forward and reverse gate bias sweeping. The hysteresis is related to border traps in gate dielectric. The border traps in near-interfacial oxide are in charged or discharged state by rapid electrical communication with Si or Ge substrate, causing hysteresis behavior during forward and reverse C-V sweeping.

2.4 Experimental Designs

In the Chapter 3, different nitrogen profiles (N-profile) within SiON were fabricated to explore the N-profile effect on gate tunneling current. The buffer oxide layer was firstly growth by dry-oxidation and nitridation was performed by plasma method. After nitridaion of gate dielectric, the re-oxidation process was performed and oxygen-rich nearly Si substrate was therefore formed. The shapes of N-profile within SiON can be modulated through control thickness of buffer oxide layer and process of re-oxidation. Additionally, the effect of stress memorization technique (SMT) on SiON for Si-MOSFETs was also examined in Chapter 3. Two NMOSFETs with different strain level were compared to investigate the effect of strain on gate tunneling current. The different strain level of SMT transported in channel region were modulated by control thickness of buffer oxide under strain nitride capping films.

In the Chapter 4, the effect of high-pressure (HP) H_2O treatment on gate dielectric upon Ge substrate was systematically investigated. The HP H_2O treatment was respectively

performed on SiO_2/Ge stack for exploration of Ge substrate, on ZrO_2/Si for exploration of ZrO_2 thin film and finally realized on ZrO_2/Ge capacitors. Additionally, the thermal stability of gate dielectric on was examined by rapid thermal annealing system and vacuum annealing system. After investigate the effect of high-pressure H_2O treatment, it is observed that the H_2O and H_2 were helpful to eliminated GeO_X formation and reduce gate leakage current after thermal annealing. Further, the H_2O and H_2 were added into RTA system and presented in Chapter 5 to verify the suppression of GeO_X formation with H_2O and H_2 ambiences.

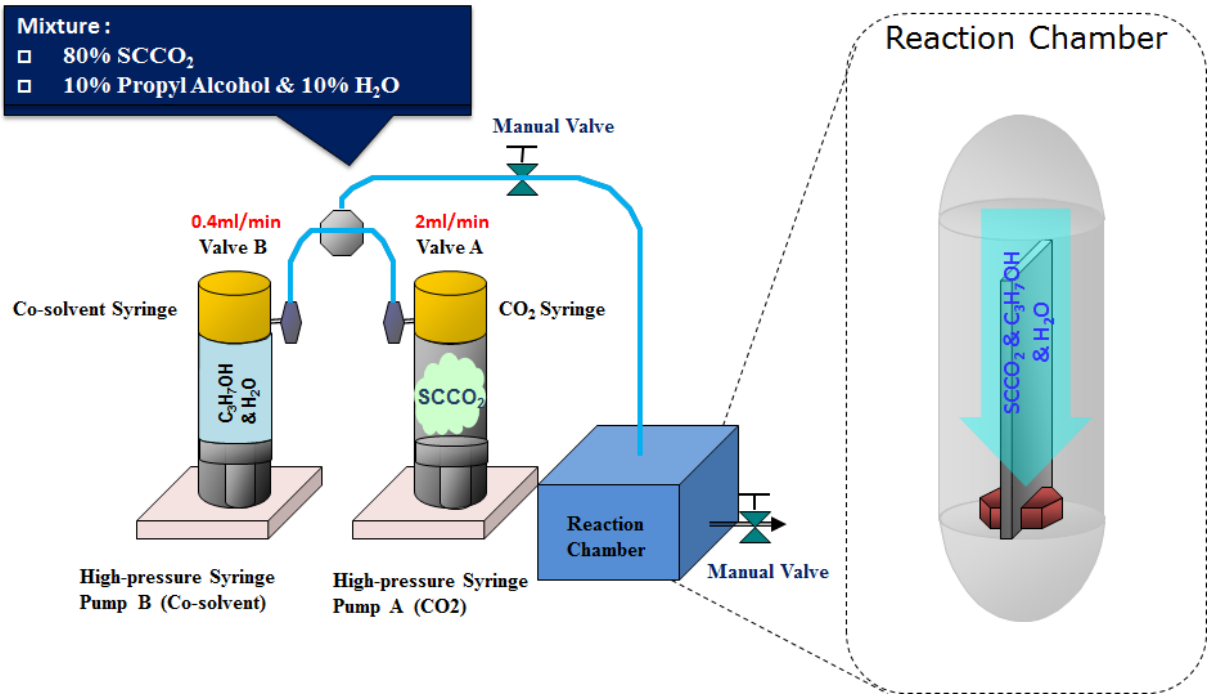

Figure 2-1 The high-pressure H_2O system.

Fluid	Critical Temperature(℃)	Critical Pressure (Psi) (1atm=14.7psi)
Heliu (He)	-268	33
Neon (Ne)	-229	400
Argon (Ar)	-122	706
Nitrogen (N_2)	-147	492
Oxygen (O_2)	-119	731
Carbon dioxide (CO_2)	31	1072
Sulfur hexafluoride (SF_6)	46	545
Ammonia (NH_3)	133	1654
Water (H_2O)	374	3209

Table 2-1 The critical temperature and pressure of various substances.

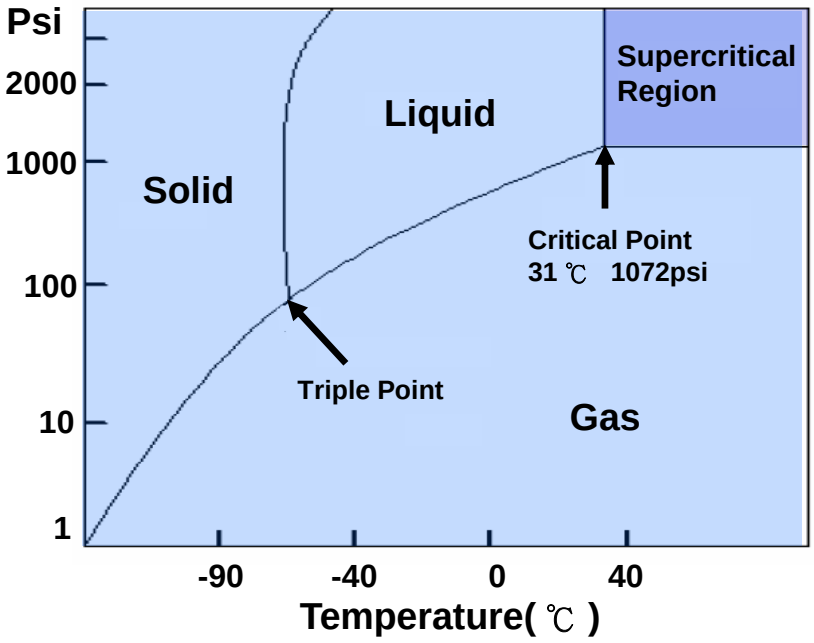

Figure 2-2 The pressure and temperature phase diagram of CO_2.

	Liquid	Supercritical Fluid	Vapor
Density (g/cm^3)	1.0	0.3 ~ 0.7	~ 10^{-3}
Diffusivity (cm^2/sec)	< 10^{-5}	10^{-2} ~ 10^{-5}	~ 10^{-1}
Viscosity (g/cm-sec)	~ 10^{-2}	10^{-3} ~ 10^{-6}	~ 10^{-6}

Table 2-2 The density, diffusivity and viscosity of CO_2 at various phases.

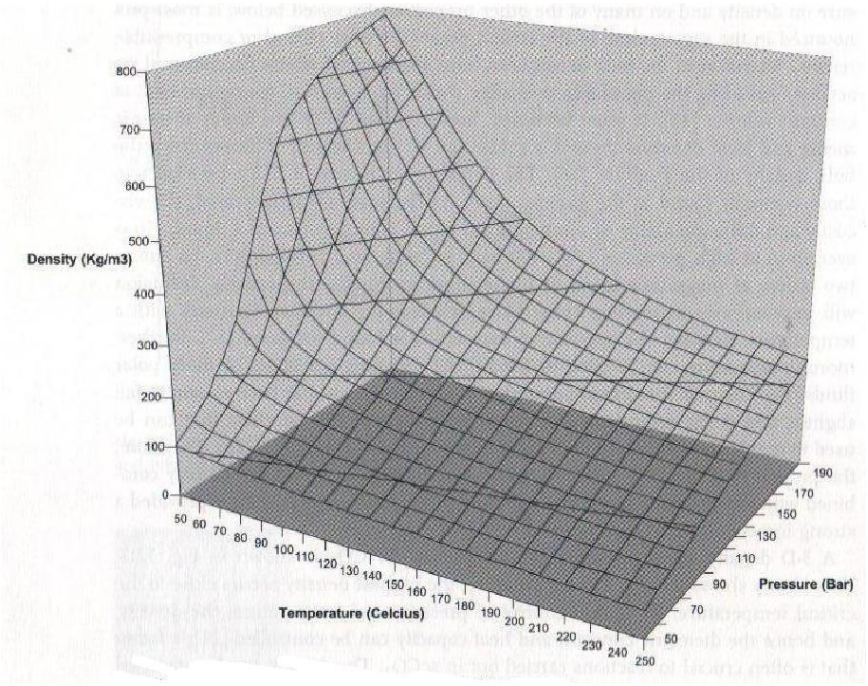

Figure 2-3 The plot of density variation with respect to pressure and temperature for CO_2.[29]

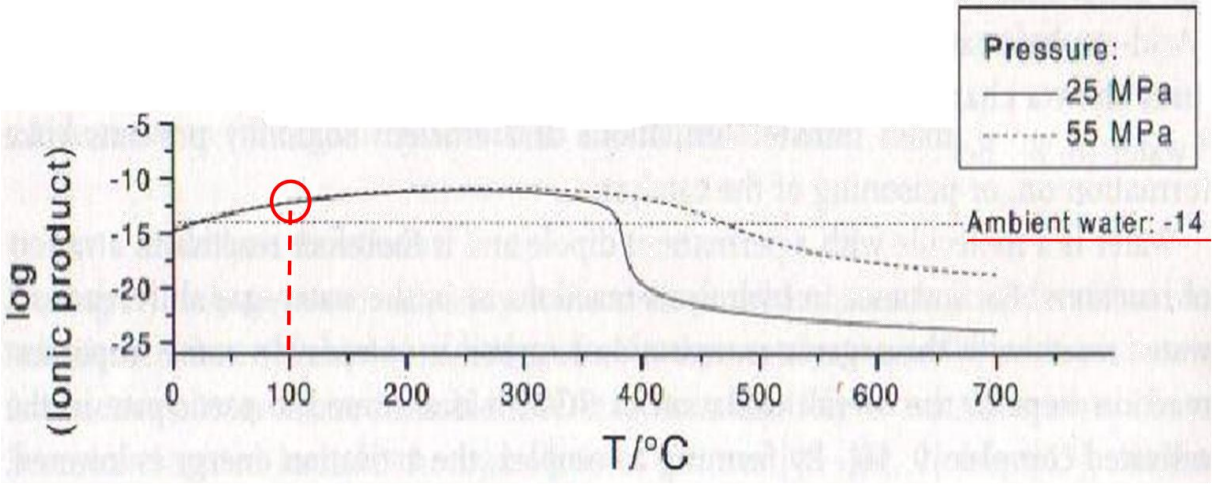

Figure 2-4 The ionic product of water at high temperature and high pressure.[29]

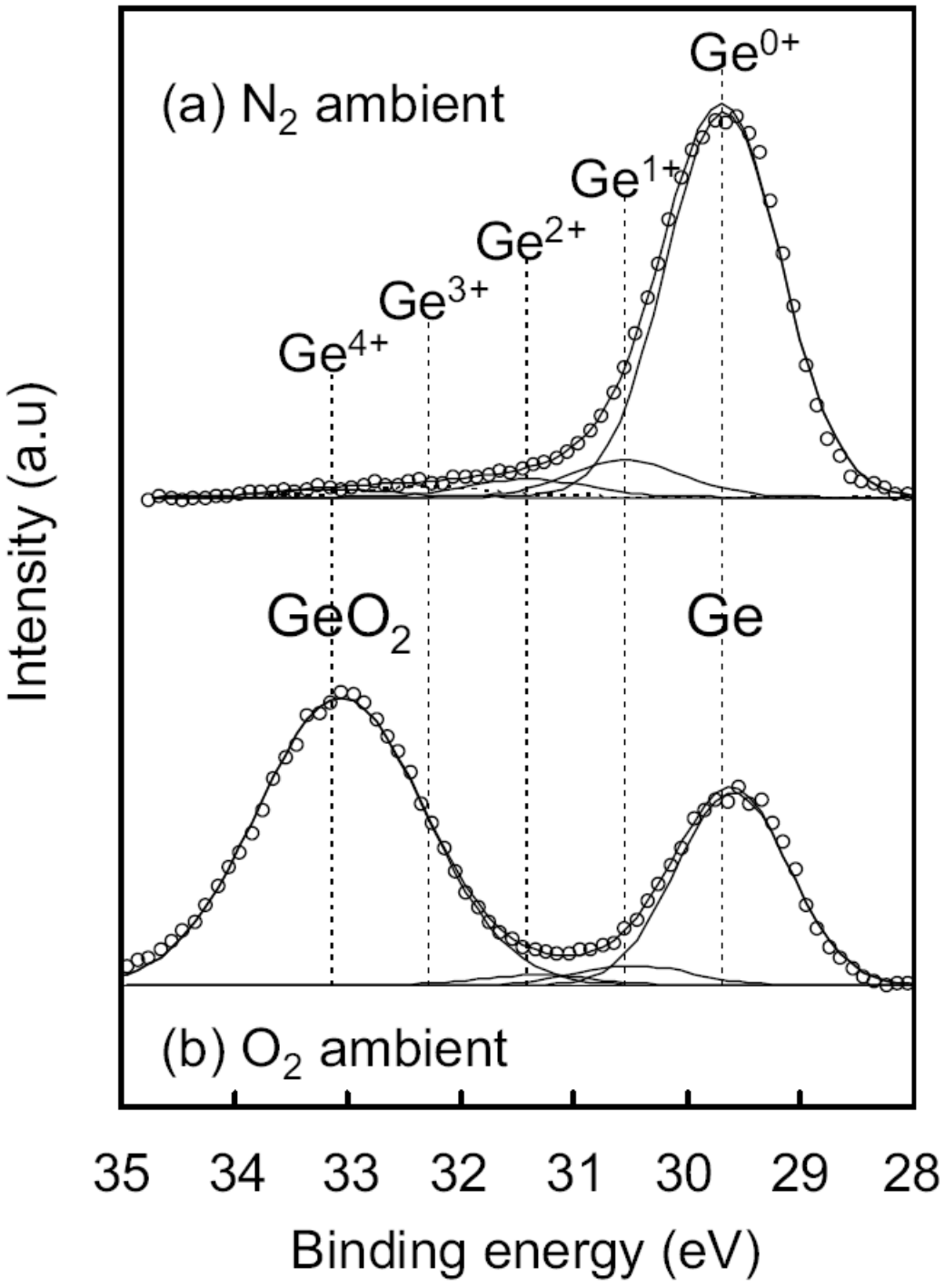

Figure 2-5 The example of binding energy shift with oxide formation.[32]

Chapter 3

Ultrathin Nitrided Oxides for Si-based MOSFET

3.1 Review and motivation

Improvement of Si-based MOSFETs was initially achieved by simply reducing the physical thickness of SiO_2 as gate dielectric layer. The downscaling of dielectric thickness causes gate tunneling-current (J_g) to increase exponentially and boron penetration issue to emerge. This poses incredible challenge to continue with device scaling. To overcome these issues, silicon oxinitride (SiON) was firstly adopted. Downscaling continues with the scaling of physical thickness and increasing nitrogen concentration within SiON. Nevertheless, excessive nitrogen concentration poses several issues of device and reliability, such as severe threshold voltage shift, lower mobility and degraded Negative Bias Temperature Instability (NBTI) [33]. Hence, the need to control N-profile in ultra-thin SiON becomes more and more critical [5]. Successful N-profile engineering will definitely alleviate these issues mentioned [6].

Additionally, the introduction of stressors to boost mobility has received a lot of attention in recent years. Stressors can be introduced in two key forms, the bases of the substrate strain and the process-induced strain. The substrate-strain based makes use of material with different lattice spacing, such as SiGe/Si epitaxial stack, to generate biaxial strain in the channel. This method introduces a global strain to the substrate. It boosts mobility effectively, at the

expense of higher cost [11]. On the other hand, the process-induced strain based method provides a lower cost solution. They could appear in the forms of shallow trench isolation (STI), contact etching stop layer (CESL) and stress memorization technique (SMT), which introduce uniaxial strain to boost mobility [12-15]. Both nMOSFET and pMOSFET have different requirements in strain. N-type MOSFET performed better under the presence of tensile strain, while p-type MOSFET performs better under the compressive strain.

In this chapter, we explored the effects of N-profile and high tensile mechanical stress on ultra-thin SiON for 45-nm generation. Firstly, experimental results show that N-profile within SiON has different impact of gate tunneling current on nMOSFETs and pMOSFETs. A model based on Wentzel-Kramers-Brillouin (WKB) approximation was proposed to expound effect of N-profiles on gate leakage current. Secondly, although high tensile mechanical stress boots the channel electron mobility, experimental results show that mechanical stress causes higher gate leakage current for nMOSFT owing to induced damage in gate dielectric edge.

3.2 Modeling of nitrogen profile effects on ultrathin nitrided oxides

There are numerous publications on how gate tunneling-current could be suppressed through nitrogen incorporation. For the same effective oxide thickness (EOT), a lower tunneling-current is possible by increasing the nitrogen concentration. Numerous models have been proposed to explain the dependence of nitrogen dosage on gate-tunneling current [25-27]. In these models, uniformly distributed N-profile is normally assumed. Little attention has

been paid to study the influence of N-profile. Typically, the nitrogen profile is intentionally engineered to optimize the benefits in both device and reliability. In this article, the effect of different N-profiles within an ultra-thin SiON on the eventual gate tunneling-current will be investigated. A model based on WKB approximation[28] will be proposed to answer why steeper N-profile produces higher J_g. Also, it will well explain the change of tunneling current by taking into consideration of the local variations in dielectric constant, band profile and effective mass.

To investigate the impact of N-profile to gate tunneling current, two kinds of SiON samples ("Sample-A" and "Sample-B") with different N-profiles were fabricated. Sample-A had a steeper N-profile than Sample-B, as illustrated in Fig. 3-1. The N-profile was measured using high resolution angle-resolved XPS. To have a fair comparison, both thickness and N-dosage were kept equal. The corresponding electrical data in terms of EOT, inversion gate tunneling-current (J_g), and J_g-ratio (defined as $J_{g\text{-}A}/J_{g\text{-}B}$) are shown in the Fig. 3-2. Two key observations were made from the experimental data: firstly, Sample-A is having a higher J_g than Sample-B, for both n- and pMOSFET. Secondly, J_g-ratio (defined as $J_{g\text{-}A}/J_{g\text{-}B}$) is higher in pMOSFET than nMOSFET, indicating pMOSFET has a higher sensitivity in J_g towards N-profile change. A model, based on the change of tunneling probability, arising from localized band bending, is proposed to explain these experimental data. This model was built based on Wentzel-Kramers-Brillouin (WKB) approximation,[28] as will be explained as

follows.

In this model, WKB approximation is adopted to calculate the change of tunneling probability under various biasing conditions. The tunneling probability (T_t) could be expressed by:

$$T_t = exp\left[-2\int_0^{T_{phy}} \sqrt{\frac{2m^*(x)}{\hbar}[\varphi_{SiON}(x) - E]}dx\right] \quad (1)$$

where T_t ≡ tunneling probability, φ_{SiON}≡ SiON/Si potential barrier and m*≡ carrier's effective mass and x≡distance into SiON, determined from Poly/SiON interface.

To solve T_t, two parameters: $\varphi_{SiON}(x)$ and m*(x), under different biases must first be extracted. To simplify the model, several assumptions were made in this model. Firstly, the nitrogen concentration is assumed to vary linearly within the bulk of SiON. Secondly, the bulk of SiON is assumed to consist of "n" number of very thin SiON strips, with uniformly distributed nitrogen in each strip. Thirdly, the energy barrier height (φ), dielectric constant (ε) and effective tunneling mass (m*) for SiON are assumed to vary linearly with nitrogen dosage between oxide material constants and those for nitride, as reference to Philip A. et al.[27, 34] Following that, the various input parameters could be simplified to:

$$N(x) = a_1 x + a_2 \quad (2)$$

$$\varphi(N) = \varphi_{ox} + (\varphi_{SiN} - \varphi_{ox})\frac{N}{57} \quad (3)$$

$$\varepsilon(N) = \varepsilon_{ox} + (\varepsilon_{SiN} - \varepsilon_{ox})\frac{N}{57} \quad (4)$$

$$m^*(N) = m^*_{ox} + (m^*_{SiN} - m^*_{ox})\frac{N}{57} \quad (5)$$

where a_1 and a_2 are constants, and we can obtain a variety of linear N profile shapes by modifying those values. The N and N_{SiN} are nitrogen concentrations (atom %) in the oxynitride film and the pure nitride film, respectively. The other used constants are summarized in the Table 3- 1 and Fig. 3-3. Substituting these parameters [$\varphi(x)$, $\varepsilon(x)$ and $m^*(x)$] into the main expression in Eq. (1), we could simulate the tunneling probability through the different potential barriers. Figure 3-4 and Figure 3-5 respectively shows the simulated N-profiles and corresponding band diagram under a bias (V_{OX}) of 0 V.

For $V_{OX} \neq 0$, Poisson's equation shall be adopted to describe the non-homogeneous change of dielectric constant within SiON:

$$\frac{d}{dx}\left(\varepsilon(x)\frac{dV_{SiON}(x)}{dx}\right) = \rho = 0 \qquad (6)$$

Where $V_{SiON}(x)$ and ρ are representing the potential and free charge density within SiON, respectively. Solving for Poisson Equation, we are able to simulate the band diagram for SiON with different N-profiles, as shown in Fig. 3-6. Therefore, the corresponding tunneling probability nMOSFET under $V_{OX} > 0$ V and for pMOSFET under $V_{OX} < 0$ V can be simulated.

To examine our model, the case of two SiON samples with different N-profiles is considered, as depicted in Fig. 3-4. Both samples are having the equal nitrogen concentrations and thickness. Under zero bias (i.e., $V_{OX} = 0$V), the simulated energy band diagram are shown in Fig. 3-5 and Fig. 3-6. The SiON sample with steeper N-profile exhibits a steeper conduction band (CB) and valence band (VB) bending. Take note that the degree of VB

bending is steeper than that of CB. This is attributed to the greater VB offset (than CB offset) difference comparing SiO_2 to Si_3N_4, as shown in the Table 3- 1.

Under nonzero biasing (i.e., $V_{OX} \neq 0$), there will be an additional voltage drops across the silicon oxinitride (V_{SiON}). Hence, it is necessary to consider both $\varphi(x)$ and $V_{SiON}(x)$ for constructing the potential barrier, while simulating the energy band diagrams. Considering minority carriers under operation mode (at low electric field),[35] the simulated tunneling probability for electrons (in nMOSFET) under positive biasing, and holes (in pMOSFET) under negative biasing are plotted in Fig. 3-7. These experimental results are also shown in Fig. 3-8. These I-V curves in Fig. 3-8 are the average results of five devices for each kind of samples. The gate current density (J_g) ratios of the steep profile to the smooth profile for n/pMOSFETs are also presented. The range of gate bias for measuring Jg ratios is just shown between -1.25 to -0.5V for pMOSFET and between 0.5 to 1.5 V for nMOSFET. The carrier transport mechanism in the bias range can be attributed to the direct tunneling behavior, which is verified by conduction processes fitting.[28]

According to simulated results, it shows that sample with steeper N-profile exhibits a higher tunneling probability, valid for both n- and pMOSFETs. This result agrees well with our experimental data in Fig. 3-8. On the other hand, defining the tunneling probability ratio (TP-ratio) as TP_{steep}/TP_{smooth}, it is observed holes (in the pMOSFET) have a higher TP-ratio than electrons (in the nMOSFET). In other words, SiON with steeper N-profile gives rise to a

higher J_G increase. This is particularly true for pMOSFET because VB bending is more sensitive to N-profile change than CB bending, as predicted by our model.

3.3 Effect of high tensile stress on ultrathin nitrided oxides

The introduction of strain into the channel region does not only enhance the mobility of electrons and holes by altering the in-plane mass, it also changes the gate tunneling current by altering the out-plane mass and SiO_2/Si barrier height. However, the change of strain will make a great impact on the gate tunneling current.[11] Previous articles have reported the reduction of gate tunneling current by introducing the tensile strain in nMOSFET.[13, 16] In the course of boosting nMOSFET mobility using SMT with high tensile strain, the gate tunneling current was also found to be increased at the same time. This is particularly evident when the channel is driven into accumulation mode. This observation is rather different from previous reports. In this study, two possible factors will be investigated to analyze the anomalously high gate tunneling currents. One is the strain-induced excessive lateral dopant diffusion, and the other is the strain-induced polysilicon gate damage at the edges.

The nMOSFET used in this work was fabricated using state-of-the-art CMOS processes. The device went through the gate dielectric, gate poly, spacer and source/drain (S/D) formation.[36-38] The lightly-doped drain-source (LDD) and S/D regions were implanted with arsenic and phosphorous, respectively. High tensile SMT film is then deposited and followed by high temperature activation treatment. Process details can be found elsewhere.[15]

Two NMOSFETs (sample-A and sample-B) with different strain level were compared to investigate the effect of strain on gate tunneling current. Sample-A is having a higher tensile strain than Sample-B. Keithely 4200 Semiconductor Characterization System and Agilent 4294 Precision Impedance Analyzer are the key instruments used to extract various device parameters.

In Fig. 3-9 and Fig. 3-10, the electrical characteristics of nMOSFET devices show that Sample-A (with higher tensile strain) has approximately 4% higher mobility than Sample-B (with lower tensile strain). Figure 3-9 also shows that the sample with higher strain also exhibits a higher drain leakage current (I_d-off) at off states. This is particularly evident when the device is biased at a linear mode (V_d=0.05V). Electrical measurement shows that the higher I_d-off is mainly contributed from the higher gate tunneling current.

Carrier separation measurement was performed to identify the source and the type of carriers tunneling through the gate dielectric.[39] The gate tunneling current is plotted as a function of gate bias (V_g) in Fig. 3-11.The measured gate current could be divided into two distinctive regions. For the low V_g region, Sample-A exhibits a much higher J_g than Sample-B. As V_g increases, the difference in J_g diminishes. Carrier-separation measurement shows electron and hole tunneling currents dominate at a low and a high gate biasing regions, as respectively shown in Fig. 3-12 and Fig. 3-13. At the low biasing region, the gate tunneling current flows primarily to the S/D regions. Sample-A is found to exhibit a higher gate

tunneling current than Sample-B. This could be originated from the different tensile strain. It has been reported that tensile strain from a SMT is huge at the gate edge.[16, 40] Therefore, it is reasonable to deduce that the anomalously high gate tunneling current in Sample-A is a result of higher tensile strain.

Figure 3-14 examines the gate tunneling current of nMOSFET devices with gate bias at -0.75 V for various channel lengths. The results show that the gate tunneling current is a function of channel length. As the channel length is decreased, the impact from strain becomes more evident. The mechanical stress induced by SMT is not only originated from the vertical compressive strain or restraining polysilicon gate from re-growth, it also comes from the tensile strain experienced by the S/D regime (SMT). This explains the dependence to channel length [41, 42]. In other words, the tensile strain experienced from SMT will be increased with the reduction of channel length, resulting in the increased gate tunneling current.

On the other hand, it is also observed that Sample-A is having approximately 9% higher gate-to-S/D overlapping capacitance than Sample-B, as shown in the Fig. 3-15. Excessive strain was reported to induce point defects, such as interstitials and vacancies in silicon. The presence of these defects assists dopant diffusion. Hence, both the tensile and compressive strain would influence the dopant diffusion behavior.[43] In our samples, the LDD was implanted with arsenic. The presence of higher tensile strain in Sample-A could enhance the

lateral arsenic diffusion. This explains Sample-A is having a higher gate-to-S/D overlapping capacitance. In addition, the change in overlapping capacitance increases gate tunneling current at gate edge.

Figure 3-16 shows transfer characteristics of Sample-A and Sample-B in the linear mode, at a drain voltage of 0.05V. The drain current of Sample-A is higher than that of Sample-B in the off state. The threshold voltage of Sample-A is slightly lower than Sample-B. These results could be attributed to the effects of strain-induced mobility increment and strain-induced lateral LDD dopant diffusion, which shortens the effective channel length further. In Fig. 3, Sample-B was also intentionally subjected to 1000 sec channel hot electron (CHE) stress to create damage at the proximity of gate edge. Following the channel hot electron stresses, threshold voltage shifts positively with degradation in sub-threshold swing. During hot carrier stress, hot electrons were injected into the gate dielectric and create interface traps.[12, 44] Compared with fresh Sample-A without stress, the stressed device produces an increased off-state drain current (I_d-off), indicating that I_d-off increases when the gate edge is damaged. This verifies our inference that an excessive tensile strain at gate edge may damage gate edge, and causes the higher I_d-off current.

3.4 Summaries

In summary, we have proposed a model based on WKB that could well explain the gate tunneling-current through thin SiON with different N-profile. The change in N-profile influences the band shape of SiON, causing the change in tunneling probability. The SiON film with steeper N-profile will exhibit a higher gate tunneling-current. Also, the phenomenon is more apparent in pMOSFET than in nMOSFET. The higher sensitivity of VB bending towards N-profile change explains why pMOSFET is showing a larger current increment than nMOSFET.

This article shows that SMT boosts the electrical performance of nMOSFET, but the gain was achieved at the expense of a higher off-state gate tunneling current. Carrier separation measurement shows the increased gate tunneling current is originated from the higher gate-to-S/D tunneling current, which worsens when channel length gets shorter. Excessive strain degrades gate tunneling current via two approaches: (1) excessive LDD dopant diffusion and (2) gate edge damage. This was verified from the higher gate-to-S/D overlapping capacitance and the hot carrier stress study.

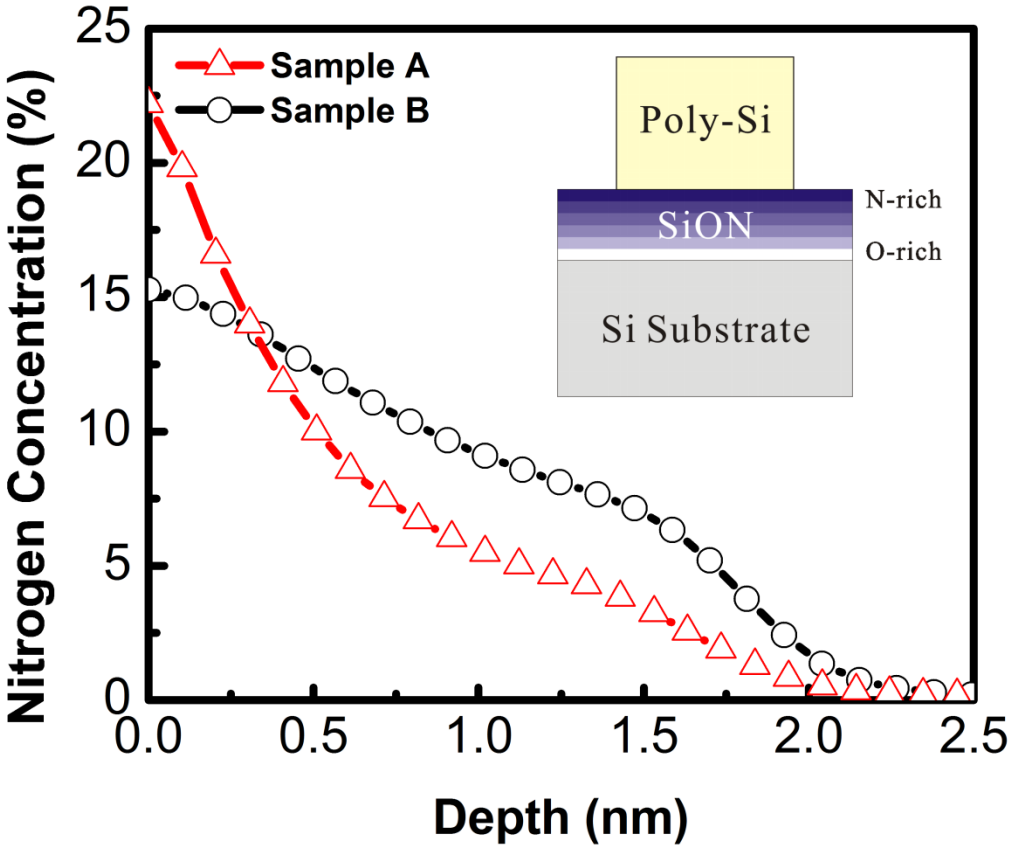

Figure 3-1 Comparison of nitrogen depth profile for two kinds of SiON films with similar thicknesses and nitrogen concentrations.

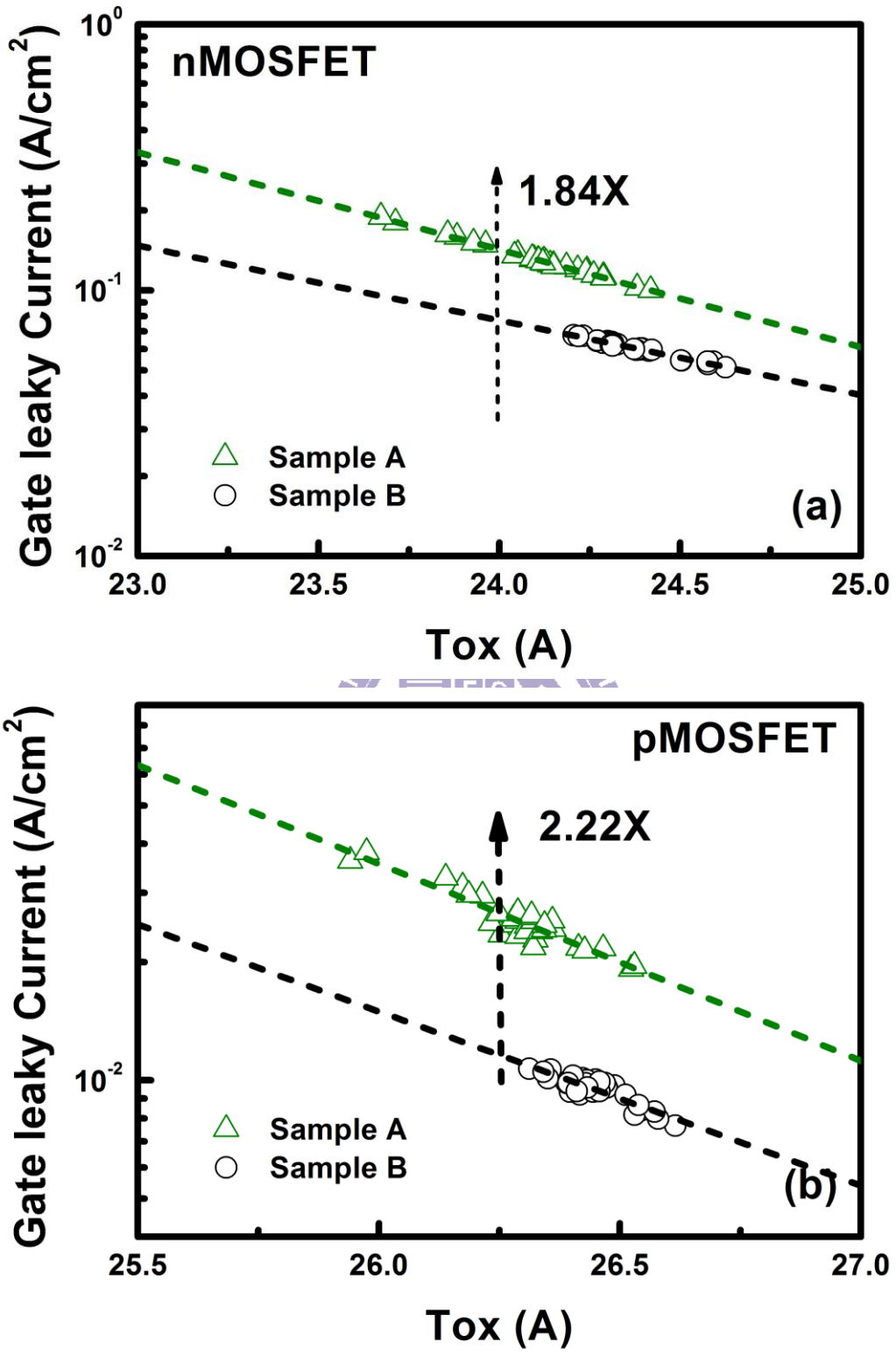

Figure 3-2 Gate current density against capacitance effective thickness with different N-profile for (a) nMOSFET and (b) pMOSFET.

	SiO_2		Si_3N_4	
Permittivity	ε_{ox}		ε_{SiN}	
	3.9		7	
	φ_{ox}	m^*_{OX}	φ_{SiN}	m^*_{SiN}
CBO	3.5eV [9]	$0.5m_0$ [10]	2.4eV [9]	$0.25m_0$ [6]
VBO	4.4eV [9]	$0.6m_0$ [6]	1.8eV [9]	$0.3m_0$ [6]

Table 3- 1 The various constants used in simulations

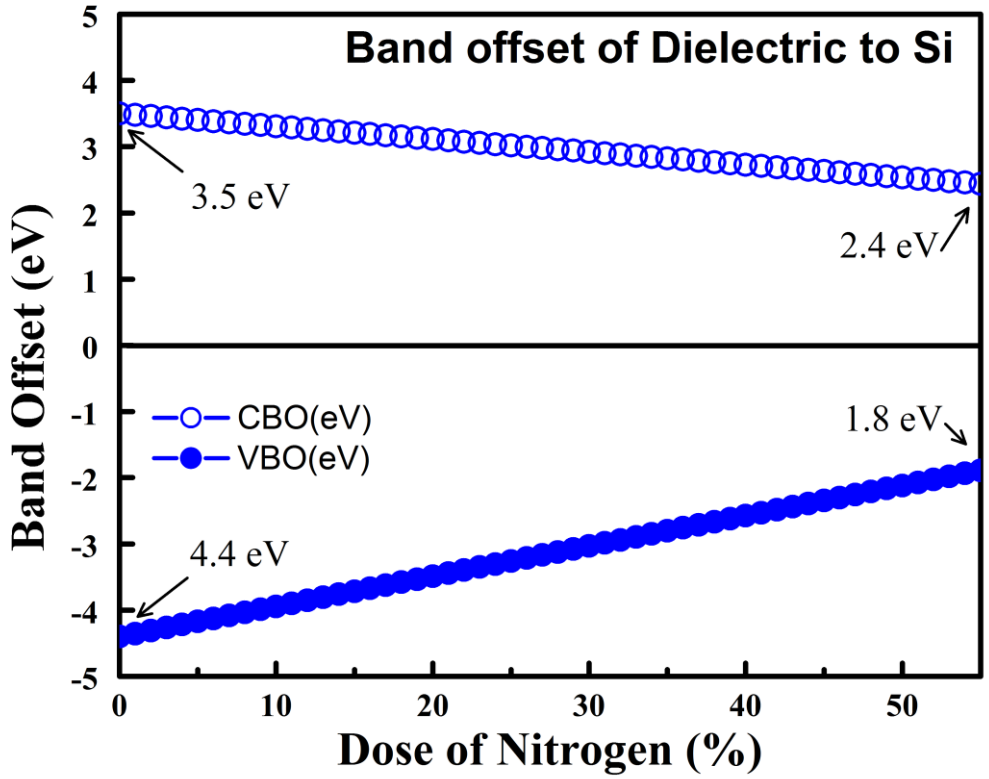

Figure 3-3 Band offset of SiON to Si with various dose of nitrogen.

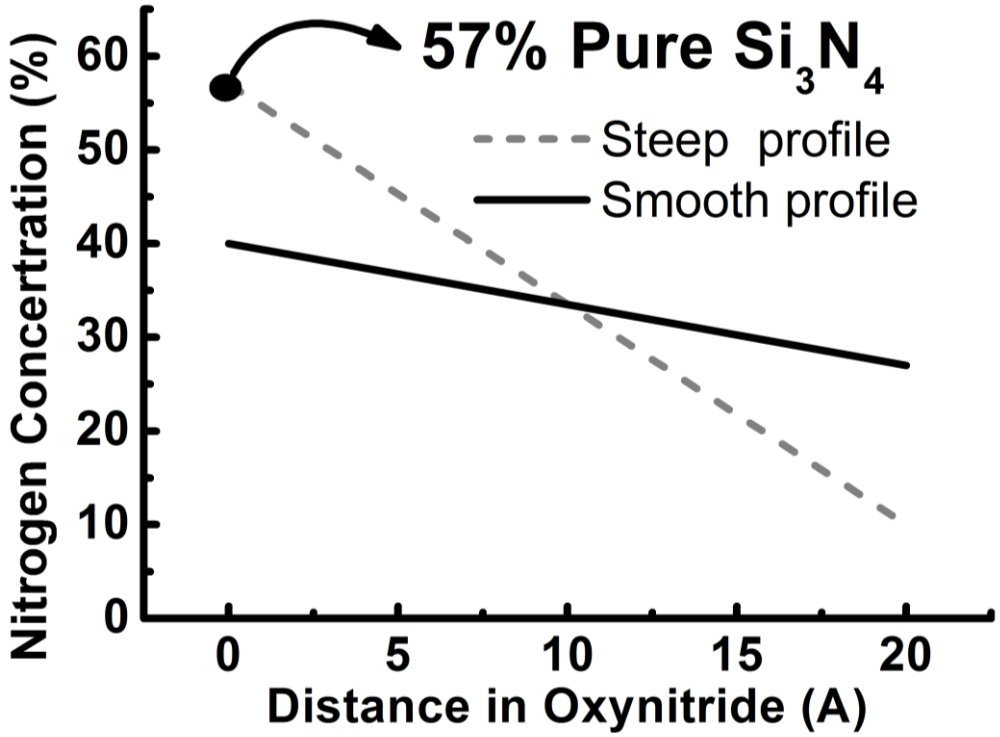

Figure 3-4 Schematic showing for two kinds of N profiles: the steep vs. the smooth profile.

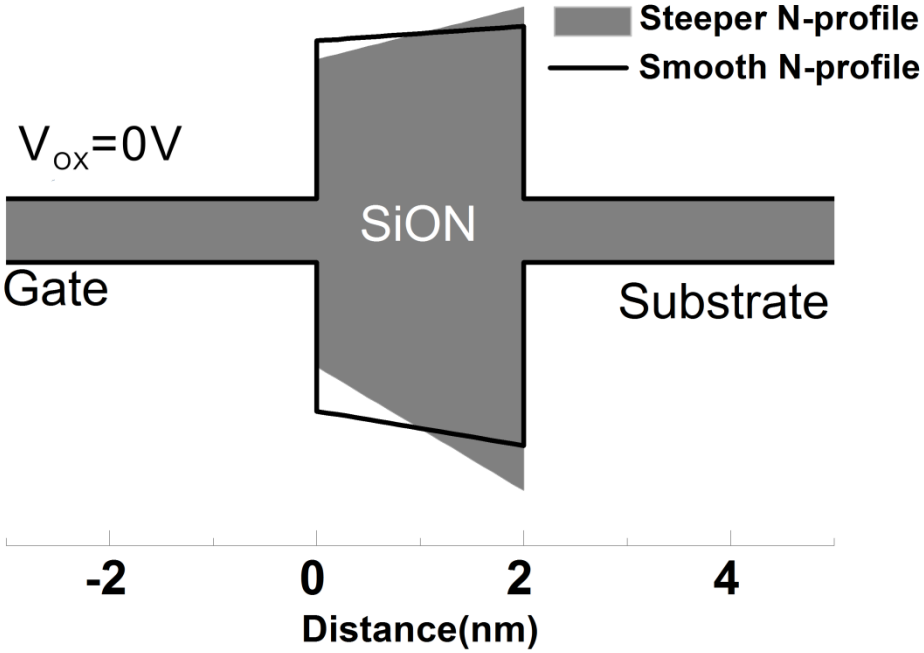

Figure 3-5 Simulated energy band diagram for steeper and smooth N-profile without gate bias.

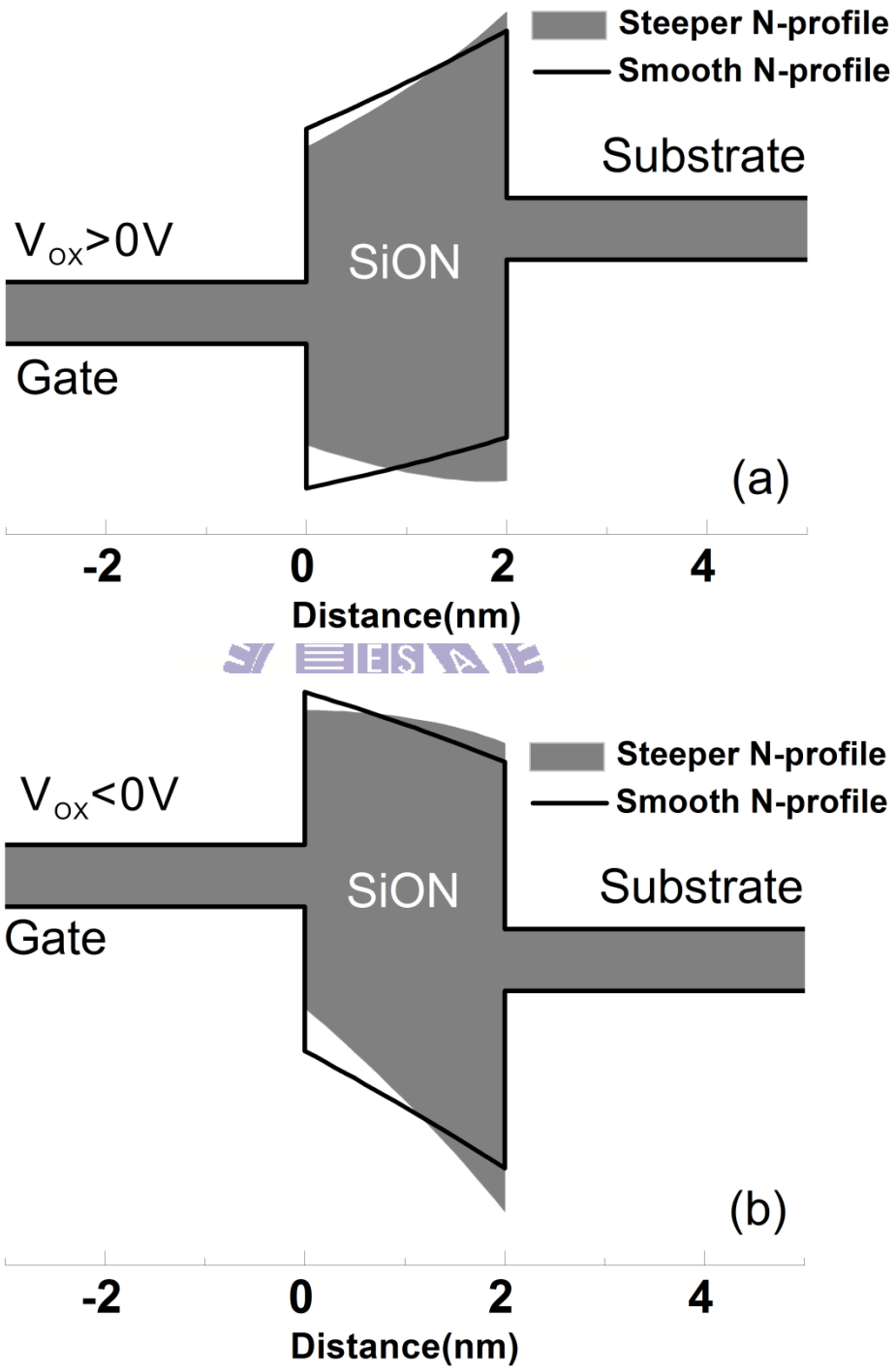

Figure 3-6 Simulated energy band diagram for steeper and smooth N-profile with (a) positive and (b) negative gate bias.

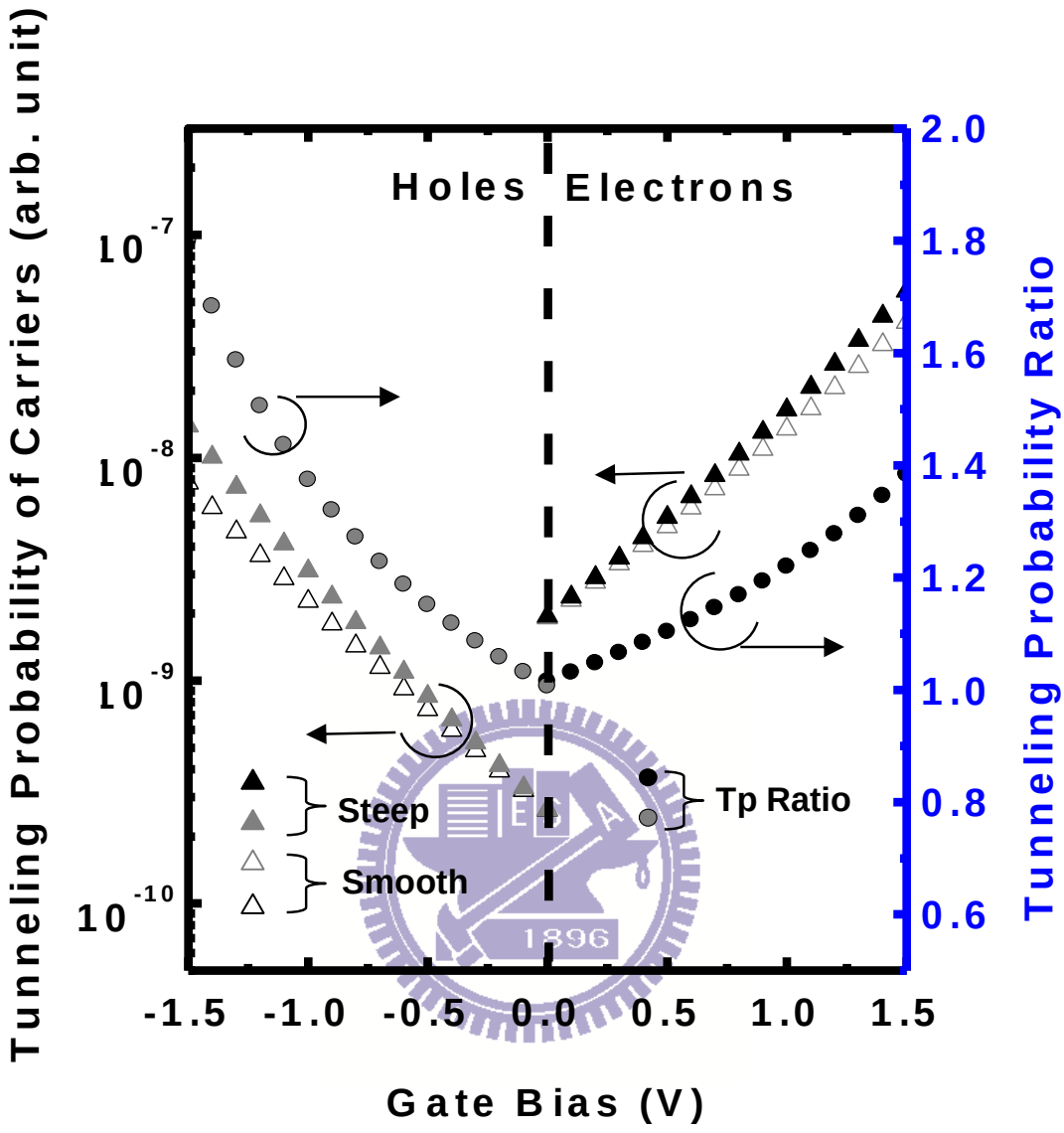

Figure 3-7 Tunneling probability and tunneling probability ratio for electrons and holes under various biasing conditions across SiON.

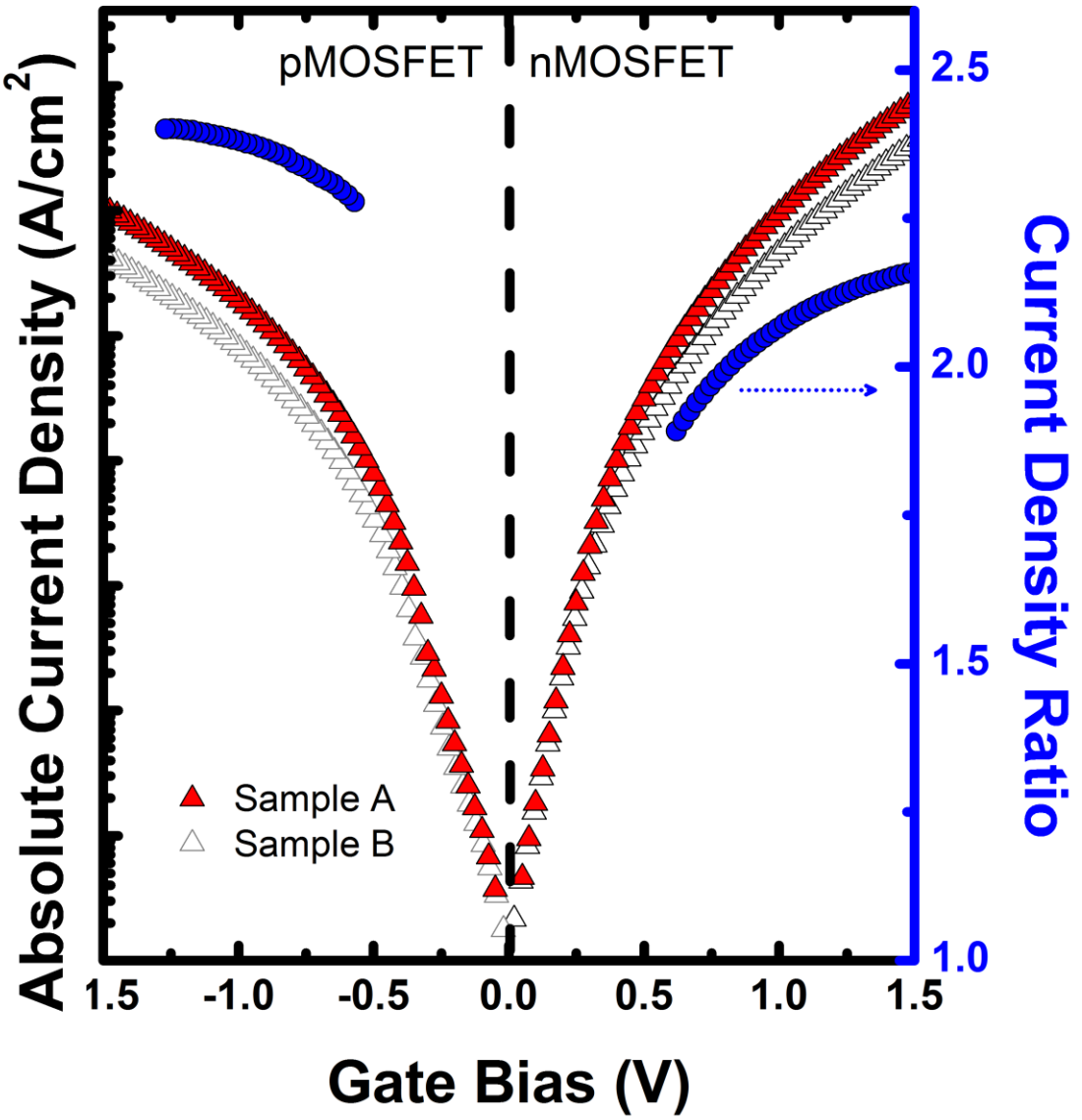

Figure 3-8 The gate leakage current density for nMOSFET and pMOSFET under various bias conditions.

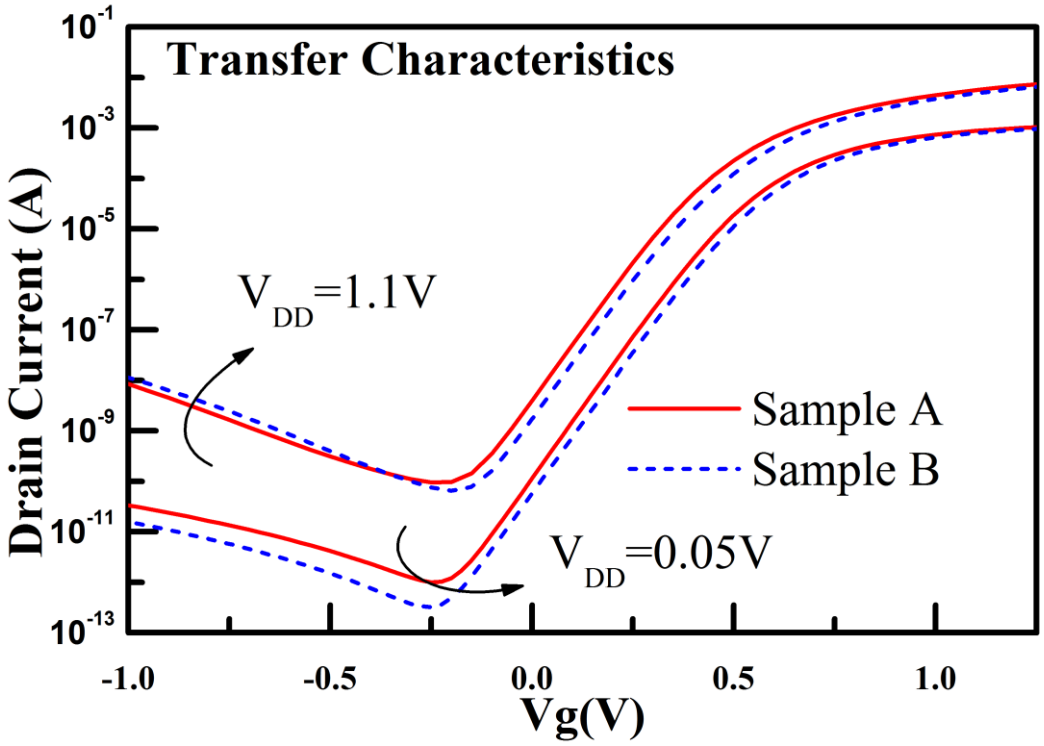

Figure 3-9 The transfer characteristics of nMOSFET with high and low tensile strain.

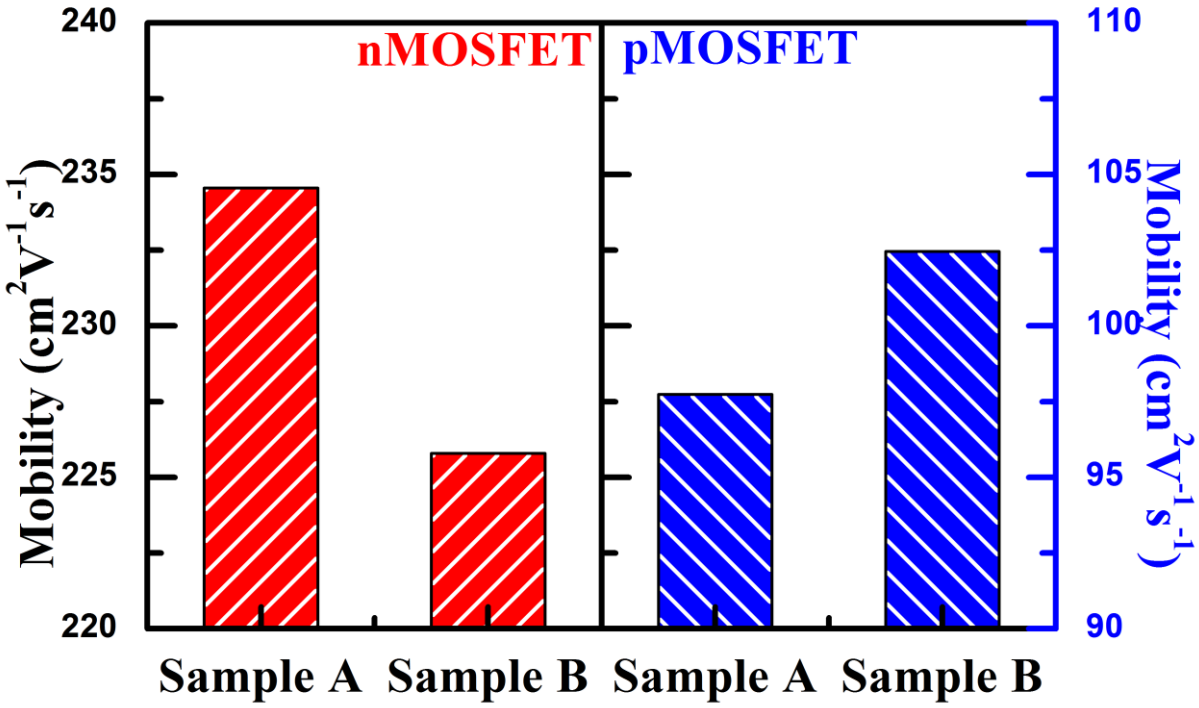

Figure 3-10 The mobility of n/pMOSFET with different tensile strain.

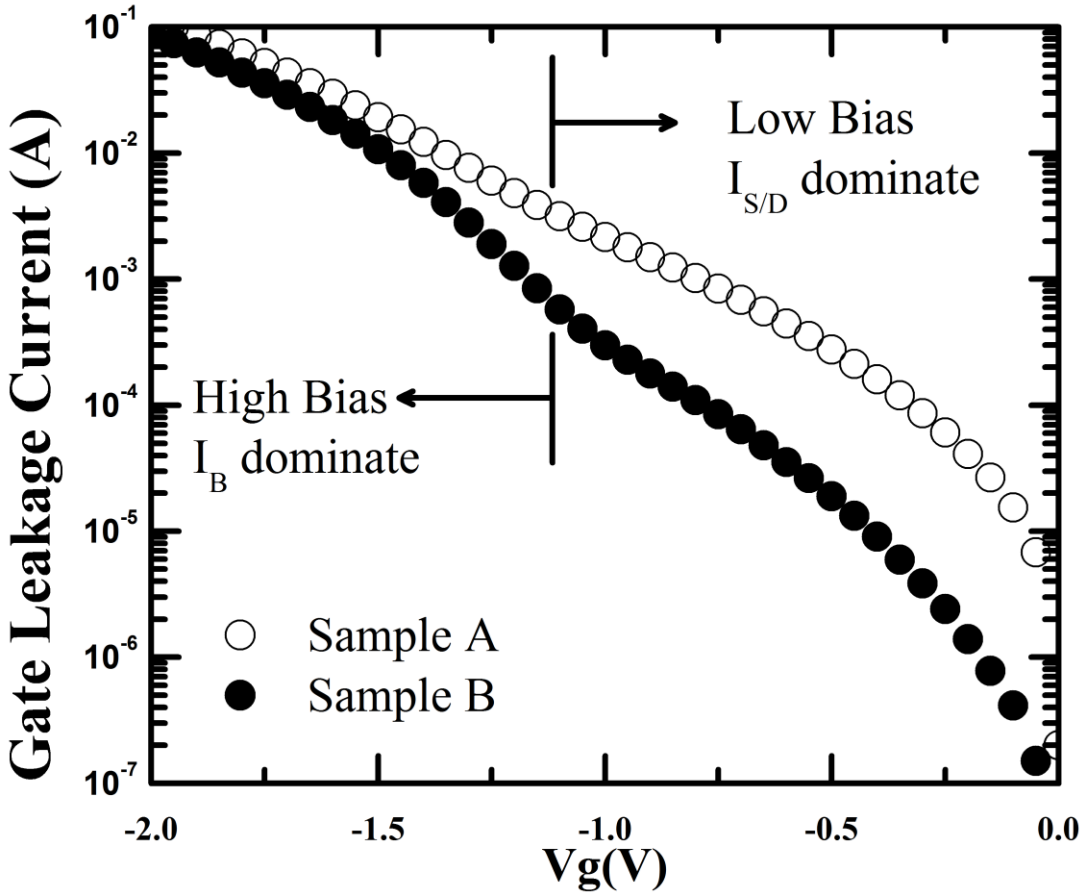

Figure 3-11 The plot of gate current density (J_g) against the gate biases.

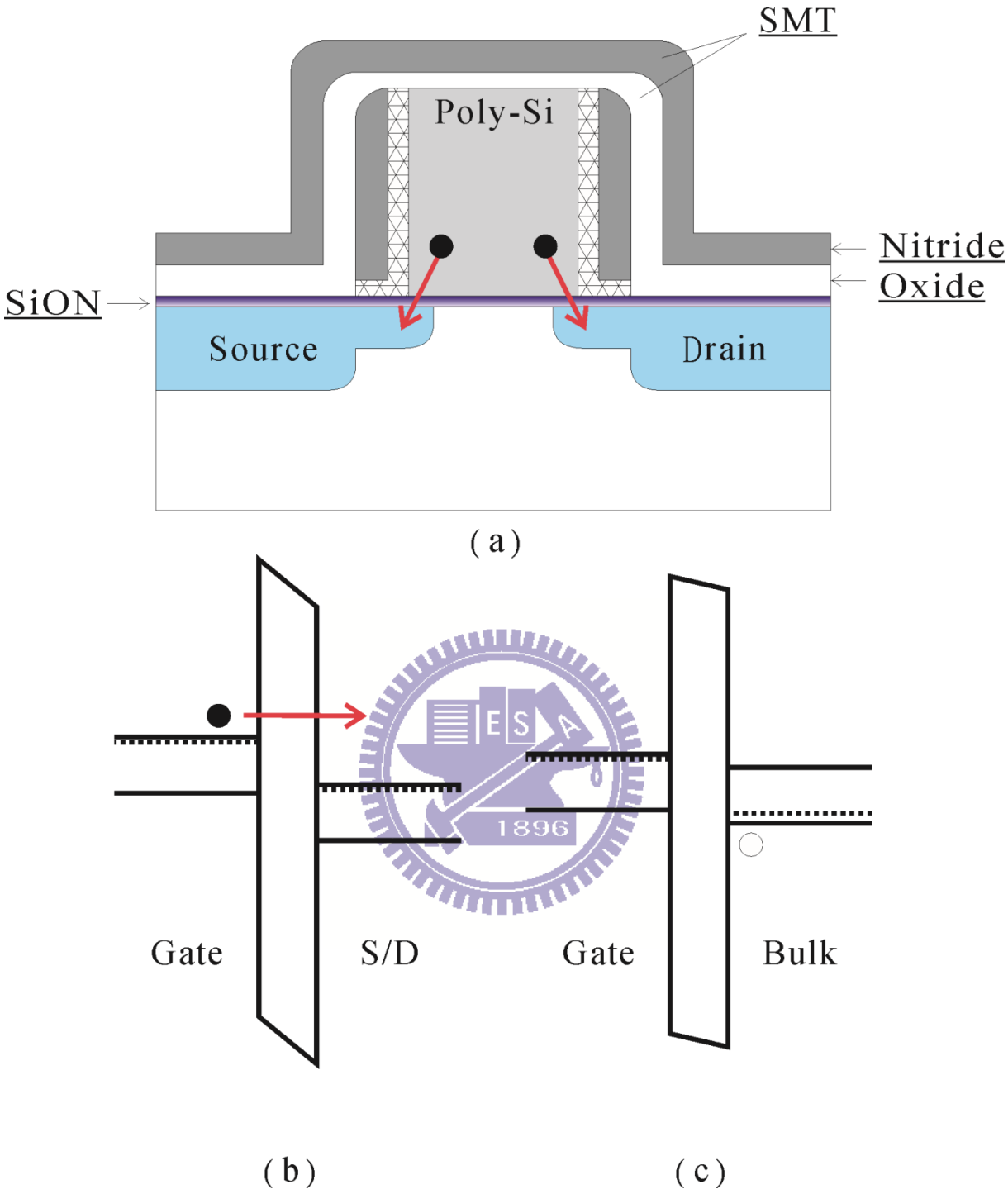

Figure 3-12 (a) Schematic diagram of leakage path, (b) band diagram of gate to S/D and (c) band diagram of gate to substrate under low negative gate bias..

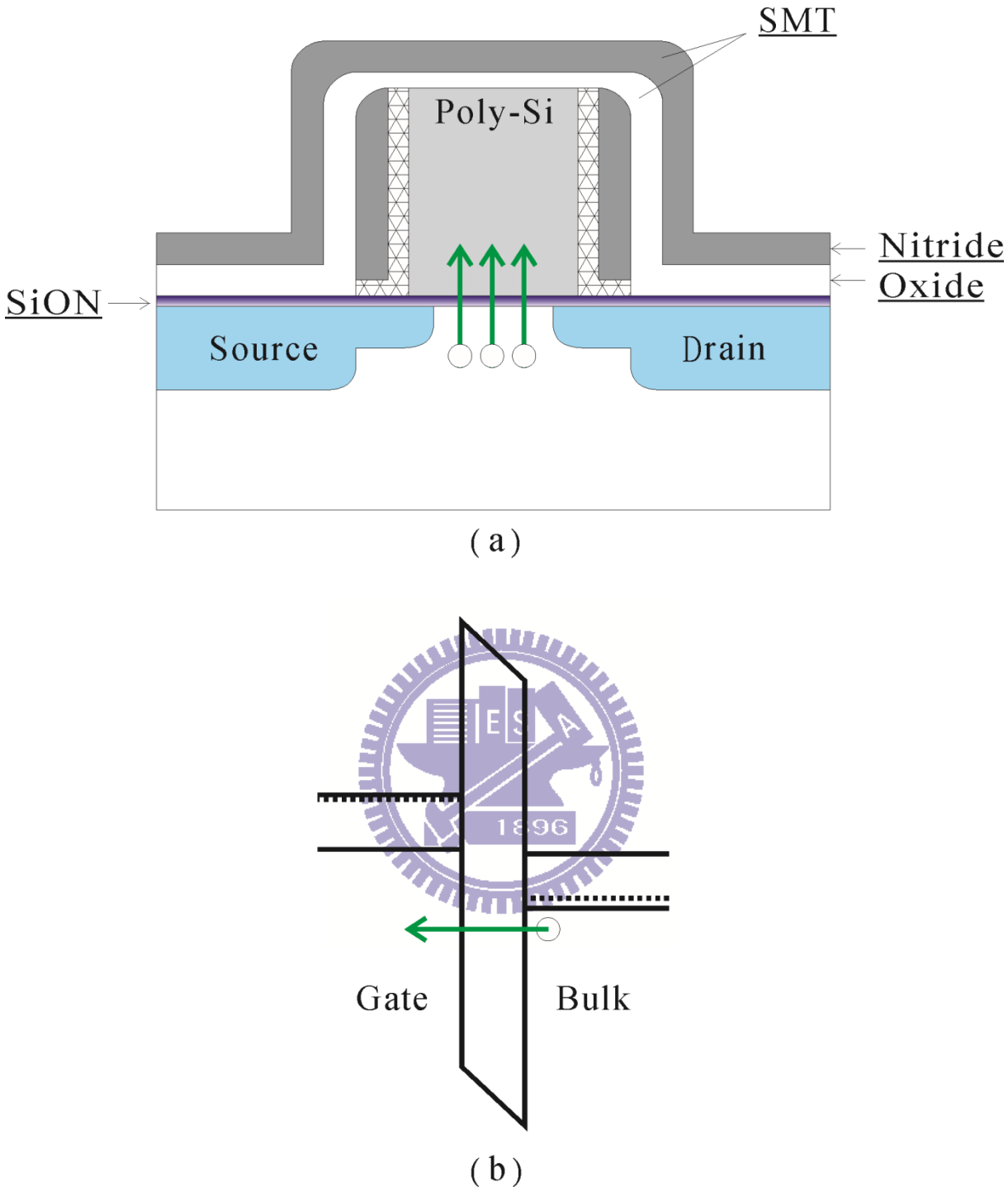

Figure 3-13 (a) Schematic diagram of leakage path and (b) band diagram of gate to substrate under high negative gate bias.

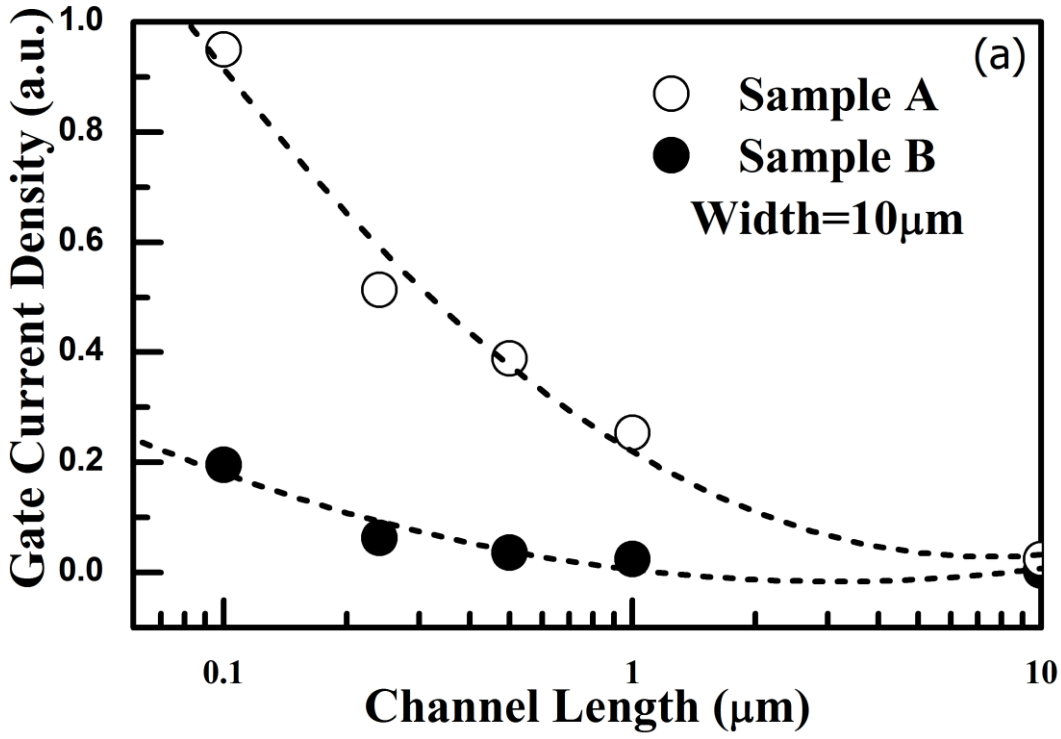

Figure 3-14 Dependence of J_G on device channel length.

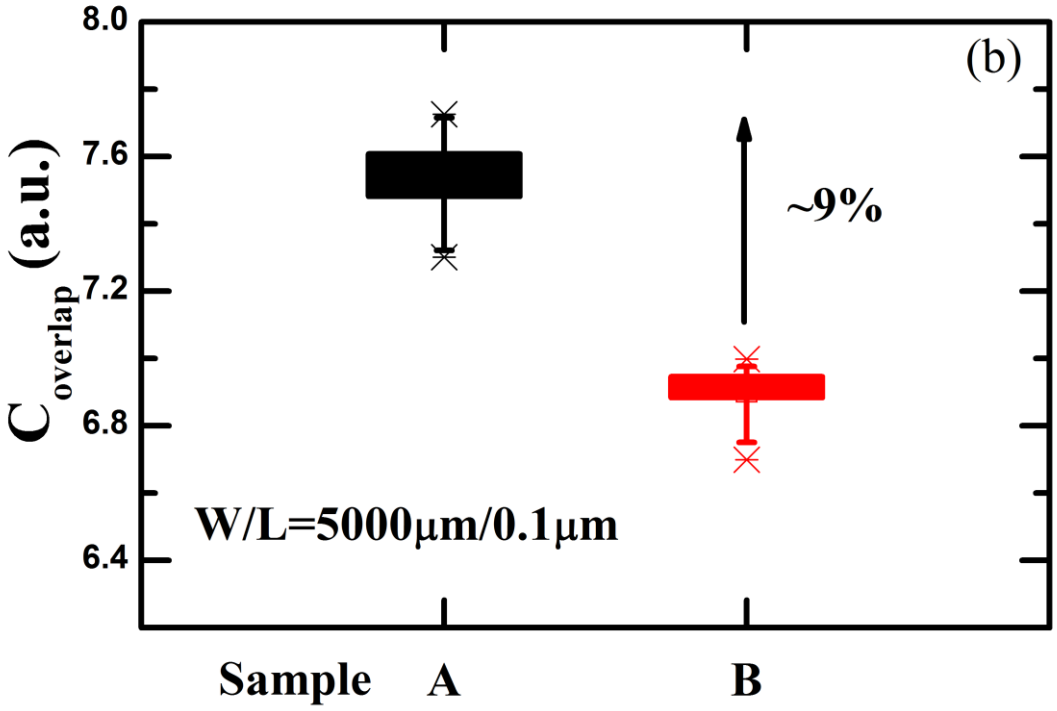

Figure 3-15 Gate-to-S/D overlap capacitance.

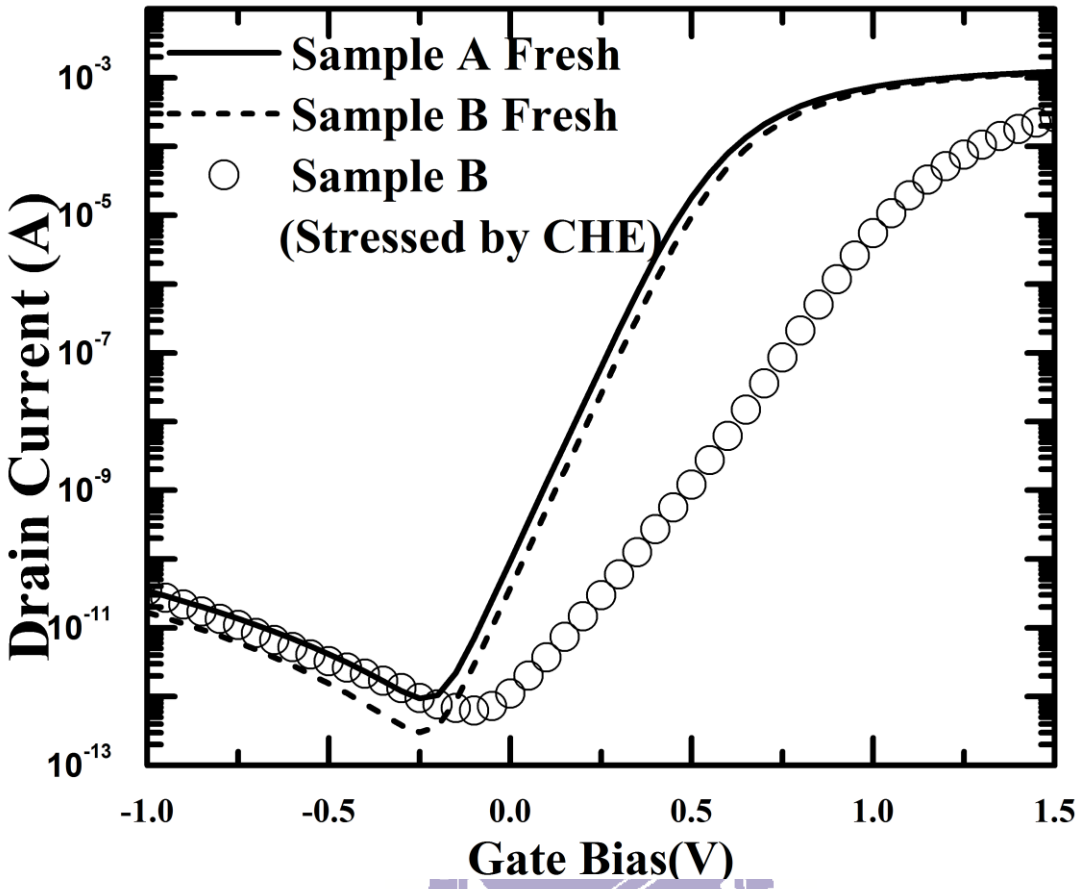

Figure 3-16 Linear-mode transfer characteristics for both Sample A and Sample B.

Chapter 4

Effect of High pressure H_2O on Gate Dielectric for Ge MOSC

4.1 Review and Motivation

Ge semiconductor has been considered as an alternate channel material in replace of Si for future high-performance CMOS technology, because its higher carrier mobility for both electrons and holes, lower dopant thermal activation energies for shallower junction formation and compatible fabrication processes with existing silicon manufacturing infrastructure.[21, 32] Recently, appropriate high-dielectric-constant (high-k) gate dielectrics on Ge channels have been examined for aggressive Ge MOSFETs scaling. These include Hf, Zr and Al-based metal oxide. Among the various high-k dielectric materials, ZrO_2 has received considerable interest owing to its high breakdown field, its large band gap and its very high dielectric permittivity when Ge or La is incorporated into it.[23, 45]

However, the most critical issue that hinders the application of Ge is the lack of a high-quality and stable Ge-insulating oxide that is similar to silicon dioxide (SiO_2) for silicon. A poor Ge suboxide (GeO_X) layer may be formed from native oxide or by the thermal decomposition of GeO_2 at low temperature ($GeO_2+Ge \rightarrow GeO_{(g)}$ at about 400 ℃),[17] resulting in a high gate leakage current and a thick effective oxide thickness (EOT) during thermal deposition or post-dielectric annealing [46-49].

The investigations of interfacial layer for GeO_2 between gate dielectric and Ge substrate can be classified into several categories for different purposes. Various pre-gate surface modification techniques, such as surface nitridation or Si passivation, have been developed to improve the quality of gate dielectric/Ge interface [17]. It was also reported that high-performance Ge MOSFET could be realized by careful control of interfacial GeO_2 formation [21]. Whether GeO_2 interlayer improves the electric performance of high-k/Ge substrate or not depends on the sequent process. Decomposition of GeO_2 after high thermal process even causes poor interface quality and higher leakage current in Ge-base MOS.

Additionally, numerous approaches have been developed to eliminate interfacial Ge native oxide between the gate dielectric and Ge. Wet chemical cleaning, such as with deionized (DI) water, diluted HF or diluted HCl, is generally performed as a pre-gate treatment to remove existing native oxide on Ge substrate [50]. However, the pre-gate cleaning can't prevent GeO_X formation after gate dielectric deposition or thermal cycles. Therefore, the development of post-gate treatment to suppress the growth of the GeO_X interlayer is essential for Ge technology. Although water vapor annealing and Al-gate oxidation after gate dielectric deposition have been reported to suppress the growth of the GeO_X interlayer, the relative studies are still not widely developed [51, 52]. Moreover, the high thermal budget of water vapor annealing at 500 ℃ could induce the incorporation of Ge into gate dielectric [53], and the thin Al_2O_3 layer formation for Al-gate oxidation technology

also could increase EOT owing to its low permittivity (about 9).

4.2 Effect of high-pressure H_2O treatment on SiO_2/Ge stack

Fitstly, a high-pressure H_2O treatment is proposed as a post-gate dielectric treatment at 100~150℃ to improve the SiO_2/Ge interface after high-temperature PDA process by dissolved H_2O in supercritical CO_2 ($SCCO_2$) fluid. The $SCCO_2$, which exists above its critical pressure (1170 psi) and temperature (30 ℃), provides good liquid-like solvency and high gas-like diffusivity, giving it excellent transport capacity. The oxidant is also easily dissolved in $SCCO_2$ fluid with specific surfactants. It is thereby allowed for $SCCO_2$ fluid to transport the oxidant and penetrates the dielectric layer for trap passivation and interface oxidation at low temperature. The $SCCO_2$ fluid mixed with oxidant is proposed in this work for the formation of interfacial GeO_2 layer after gate-dielectric SiO_2 deposition to prevent interfacial decomposition from subsequent thermal processes.

4.2.1 Device fabrication

An epitaxial Ge (epi-Ge) layer on Si substrate was taken as Ge channel in this study. A 0.5 Ω cm p-type (100) Si wafer was cleaned with standard RCA clean process and immediately loaded into the Applied Materials reduced-pressure chemical vapor deposition (RP-CVD) reactor. The initial 600 nm-thick Ge film was grown at 400 ℃ with a GeH_4 partial pressure of 8 Pa. Annealing under H_2 ambient was then performed at 825 ℃ for 40 min. The growth temperature was ramped to 600 ℃ for the deposition of another 1.4 μm-thick Ge layer

at 8 Pa, followed by a 15-min H_2 bake at 750 ℃. This epi-Ge layer is p-type with an electrically activated concentration of 4×10^{15} cm^{-3}. The wafer was immediately loaded into a low-pressure chemical vapor deposition (LPCVD) furnace with 300 mTorr and a thin silicon dioxide (SiO_2) layer was deposited at 300 ℃ on top of the epi-Ge layer, as the gate insulator of the following Ge-MOS device. It was followed that the samples were divided into two groups for study in this work. In the first group, the high-pressure H_2O treatment was performed right after the gate SiO_2 deposition to enhance the Ge-MOS device performance. The sample was placed in a $SCCO_2$ system at 150 ℃ for 1 hour, where was injected with 2000~3000 psi of $SCCO_2$ fluid that were mixed with 5 vol.% of propyl alcohol and 5 vol.% of pure H_2O. The propyl alcohol was used as a modifier to enhance the solubility of the polar H_2O molecules in nopolar CO_2. The water was dissolved as small H_2O molecule clusters and uniformly mixed in $SCCO_2$ fluid. The $SCCO_2$ fluid exhibited a liquid-like property, giving it an excellent transport capacity. Also, supercritical fluid has gas-like properties and efficiently diffuses into nanoscale structures without damage.[54] Therefore, H_2O molecules are uniformly distributed in $SCCO_2$ fluid and delivered into the gate SiO_2 film to passivate defect states. In the second group, the influence of PDA on the Ge MOS device characteristics was studied further. The sample after the gate SiO_2 deposition was subjected to a PDA process at 450 ℃ for 30 min in a vacuum furnace with 1×10^{-7} torr, and then the SCF pos-treatment was implemented with the same conditions as mentioned above. Finally, aluminum electrodes

were thermally evaporated on the top surface of SiO_2 film with an electrode area of 7.07×10^{-4} cm^2 and the back side of silicon wafer to fabricate Ge-MOS capacitors. The material analysis of X-ray photoelectron spectroscopy (XPS) on epi-Ge channel layer was also performed to examine the evolution of chemical bonding before and after $SCCO_2$ treatment. In order to clearly distinguish the gate insulator/epi-Ge interface for signal collection, the $SCCO_2$ process was applied to a stack structure of 13nm-thick HfO_2/epi-Ge layers. It is noted that the HfO_2 layer was in-situ removed by Ar^+ sputtering process before XPS spectra collection. Therefore, the information of chemical bonding at the epi-Ge surface can be obtained after SCF treatment.

4.2.2 Results and discussions

Figures 4-1(a) and (b) show the cross-sectional high-resolution transmission electron microscopy (HRTEM) images for the LPCVD-SiO_2 film deposited on epi-Ge layer, before and after the high-pressure H_2O post-gate dielectric treatment, respectively. In Fig. 4-1(a), the thickness of as-deposited SiO_2 film is observed to be about 13.5 nm. After immersion of high-pressure H_2O at 150 ℃ for 1 hour, the dielectric thickness above the Ge layer is increased to about 16.6 nm in total, and a clear and even interface is exhibited, as shown in Fig. 4-1(b). It is inferred that the increase of dielectric thickness and the even interface formed are originated from the formation of interfacial germanium oxide (GeO_x) during the SCF treatment with excellent permeability. The following XPS analysis results will support the

inference.

The frequency dependence of capacitance-voltage (C-V) curves for the Ge-MOS device with various post-treatments is studied at 300K, as depicted in Fig. 4-2. It is observed that the inversion capacitance which occurs at positive gate bias for p-type Ge exhibits frequency dispersion in different levels. The frequency dispersion behavior is attributed to the response of minority carrier thermal generation from interface defect states to measuring frequencies. The fast minority-carrier response can be achieved at low frequency.[32] When ambient temperature decreases to 80K, the generation rate of minority carriers is obviously suppressed, as shown in Fig. 4-3. Therefore, the observation of frequency dispersion at inversion region can be used to evaluate the interface quality of Ge-MOS capacitor.

Compared with the case of lower interface state densities, the Ge-MOS capacitor with higher interface state densities also will present a larger inversion capacitance, and the gap of the inversion capacitances between both cases shrinks as the increase of measuring frequencies. In this work, the inversion capacitance of Ge-MOS device with HP H_2O treatment declines fastest and approaches to an ideal minimum capacitance as compared to the one without HP H_2O treatment, especially in the high measuring frequency of 500 KHz. In addition, it was shown that the C-V frequency dispersion decreased with increasing the processing pressure. It is reasonably believed that the solubility of oxidant (H_2O) and modifier (propyl alcohol) is increased with increasing the $SCCO_2$ pressure.[55] The increased pressure

can also enhance the penetration of $SCCO_2$ to the interface between gate dielectric film and epi-Ge layer. Additionally, the amounts of ionic products, H_3O^+ and OH^- radicals, in H_2O at high pressure may be orders of magnitude higher than those obtained in ambient water. The higher amounts of free radicals are associated with a strengthened oxidation reaction between H_2O and thin film owing to the higher collision frequency.[29]

Figure 4-4 shows XPS spectra of Ge 3*d* signal on the interface between gate dielectric (HfO_2) layer and epi-Ge before and after SCF treatment. The detected signal of Ge 3*d* spectra primarily comes from the surface of epi-Ge channel layer, since the HfO_2 layer was in-situ removed previously by Ar^+ sputtering before XPS spectra collection. The signals of GeO_x and GeO_2 bonding were observed for both samples from the XPS analysis. For the sample without HP H_2O treatment, it is inferred that the species of oxygen will oxidize the Ge surface to form loose native oxide layer during the early stage of gate dielectric film deposition. After SCF treatment, higher signal intensity of GeO_2 bonding at the epi-Ge surface is observed obviously. The results reasonably explain that the oxidation at the epi-Ge/gate dielectric interface has occurred by dissolving H_2O oxidant into the $SCCO_2$ fluid with excellent transport capacity. The formation of interfacial GeO_2 layer can smoothen the epi-Ge surface and alleviate frequency dispersion of inversion capacitance.

The thermal stability and the effects of HP H_2O treatment on PDA-treated Ge-MOS device are investigated further for realistic Ge-MOSFET fabrication consideration. Figure 4-5

shows C-V characteristics of 450 ℃ PDA-treated Ge-MOS devices before and after HP H_2O post-treatment. Figure 4-6 also depicts the leakage current characteristics of the PDA-treated Ge-MOS devices before and after HP H_2O post-treatment. The least accumulation capacitance is observed in the PDA-treated Ge-MOS device, about a 66% reduction compared with the control sample (without PDA process). The significant reduction of the accumulation capacitance due to poor charge holding capability can be attributed to the large leakage current of PDA-treated Ge MOS device, as shown as Fig. 4-6. It was reported that thermal process induces Ge decomposition and desorption into gate dielectric layer. The incorporation of Ge in dielectric insulator is believed to act as defect traps and thereby causes an increased gate leakage current.[17, 21, 56] In this study, the implementation of HP H_2O treatment after PDA process significantly reduces leakage current of gate insulator and recovers the C-V characteristic to a similar state as the initial Ge-MOS device without PDA process (control sample). This indicates again that H_2O oxidant is effectively transported into SiO_2 film by the high-pressure $SCCO_2$ and passivates the defect states generated in the Ge-MOS device during high-temperature thermal PDA process.

4.2.3 Summaries

In summary, a low-temperature and high-pressure H_2O treatment at 150 ℃ has been proposed to treat the SiO_2/epi-Ge interface and restore Ge-MOS device degradation after a high-temperature PDA process. It is observed that the uneven and poor interface was easily

formed during thermal deposition processes on epi-Ge layer. After the high-pressure H_2O treatment, a smooth GeO_2 interface layer is formed and the frequency dispersion of inversion capacitance is alleviated. Furthermore, electrical degradation of Ge-MOS device after 450℃ PDA process leads to the reduction of accumulation capacitance and the increase of gate leakage current. The high-pressure H_2O treatment also can transport the oxidant into the gate dielectric layer and passivate the Ge-related defect states generated by PDA process. Electrical characteristics of Ge-MOS device are effectively recovered to an extent similar to the one before PDA process.

4.3 Characteristics of ZrO_2 thin film on Si substrate

In order to characterize and optimize the sputtered-ZrO_2 dielectric layer without interruption by semiconductor substrate, the preliminary investigations of thermal treatment and high-pressure H_2O treatment for ZrO_2 dielectric layer were performed on silicon (Si) substrate firstly.

4.3.1 Device fabrication

P-type (100) Si wafers with 0.5 ohm-cm were cleaned by standard RCA clean process. After drying, the ZrO_2 thin film was deposited by radio-frequency sputtering in Ar ambient with a highly pure ZrO_2 (99.99%) target at 100 W and a chamber pressure of 3×10^{-3} Torr. Following the deposition of ZrO_2, vacuum annealing was performed at 250 ℃ under a pressure of 5×10^{-6} torr for 30 minutes to improve the quality of ZrO_2. Rapid thermal

annealing (RTA) was also carried out at 300 ℃ to 500 ℃ for 1 minute to study effect of thermal stability on the ZrO_2/Si stack. High-pressure H_2O treatment was conducted using 3000 psi (about 200 atm) of supercritical CO_2 fluid that was mixed with 5 vol.% of propyl alcohol and 5 vol.% of pure H_2O at 100 ℃ for one hour. Finally, 100 nm-thick sputtered TaN and 500 nm-thick thermally evaporated aluminum were deposited on the top surface of the ZrO_2 film with an electrode area of 7.07×10^{-4} cm^2, for use in MOS devices. The backside was also thermally evaporated aluminum as electrode.

4.3.2 Result and discussions

Figure 4-7 depicts the gate leakage current density (J_G) of sputtered-ZrO_2 dielectric layer on Si substrate with various thermal treatments. The results show that the J_G for thermal annealing changes slightly until the temperature at 400 ℃. However, the dramatic increment of J_G is observed in 500 ℃ RTA-treated sample. The increase of leakage current for high-k dielectrics after thermal process is generally considered as the result of film crystallization.[57] The J_G may be higher in polycrystalline dielectrics than in amorphous films because defective grain boundary regions may enhance electronic conduction. The high-pressure H_2O treatment was performed on ZrO_2/Si stack after 500 ℃ RTA and shown in Fig. 4-8. The J_G of RTA-treated ZrO_2/Si stack reduces about three orders of magnitude after high-pressure H_2O treatment, and is comparable to ZrO_2/Si device without RTA. It is inferred that the defective grain boundaries of ZrO_2 were effectively passivated by high-pressure H_2O treatment at low

temperature.

The C-V characteristics of ZrO_2/Si with various thermal treatments are shown in Fig. 4-9 and are summarized in Table 4-1. The V_{fb}, ΔV_{fb}, THK, CET and ε_{eff} present flat-band voltage, shift of flat-band voltage, thickness of ZrO_2 measured by n-k instrument, capacitance effective thickness and effective dielectric permittivity, respectively. The decrease of $V_{fb,}$ observed in 500 ℃ RTA-treated sample, is attributed to change of effective metal work function with crystallization of ZrO_2. Additionally, the ΔV_{fb} is the index of hysteresis and related to border traps.[58] The border traps in near-interfacial oxide are in charged or discharged states, causing hysteresis behavior during forward and reverse C-V sweeping. Therefore, the decline of ΔV_{fb} after 500 ℃ RTA is attributed to reduction of border traps by thermal annealing. Although the higher RTA temperature reduces hysteresis behavior of ZrO_2/Si device, it also has a penalty of CET, as shown in Table 4-1. The CET increases from 3.92 nm to 4.76 nm after 500 ℃ RTA. One of factors in increment of CET is resulted from ZrO_2 layer thickened by 500 ℃ RTA. In other way, the significant reduction of the CET due to poor charge holding capability can be attributed to the large leakage current of 500 ℃ RTA-treated ZrO_2/Si device, as shown as Fig. 4-7.

Figure 4-10 and Table 4-2 show and summarize the C-V characteristics of ZrO_2/Si stack with 500 ℃ RTA after high-pressure H_2O treatment, respectively. After high-pressure H_2O treatment, the hysteresis behavior vanishes and CET decrease from 4.76 nm to 4.11 nm. It

is inferred that the high-pressure H_2O treatment passivates the border traps in ZrO_2 nearby Si substrate and defective grain boundary regions in the bulk of ZrO_2.

4.3.3 Summaries

In summary, the preliminary investigations of thermal treatment and high-pressure H_2O treatment for ZrO_2 dielectric layer were performed on Si substrate to prevent interruption of Ge. After thermal annealing, the J_G of ZrO_2 dielectric changes slightly until temperature at 400 ℃. However, the dramatic increment of J_G is observed in the 500 ℃ RTA-treated sample. The increase of J_G for ZrO_2 dielectrics is attributed to defective grain boundaries induced by thermal crystallization. Moreover, increase of J_G also worsens the charge holding capability of ZrO_2 layer and results in increment of CET. After high-pressure H_2O treatment, the hysteresis behavior vanishes and CET reduces in ZrO_2/Si capacitor. It is inferred that the high-pressure H_2O treatment passivates the border traps in ZrO_2 nearby Si substrate and defective grain boundary regions in the bulk of ZrO_2.

4.4 Effect of High-Pressure H_2O Treatment on ZrO_2/Ge Stack

4.4.1 Device fabrication

The Ge substrate was a (100) Ga-doped p-type wafer with a resistivity of 1-10 Ω cm. The wafers were cleaned with diluted HF (1:50) and rinsed deionized water for several cycles to remove the unstable native oxide. After drying, the ZrO_2 thin film was deposited by radio-frequency sputtering in Ar ambient with a highly pure ZrO_2 (99.99%) target at 100 W

and a chamber pressure of 3×10^{-3} Torr. Following the deposition of ZrO_2, vacuum annealing was performed at 250 ℃ under a pressure of 5×10^{-6} torr for 30 min to improve the quality of ZrO_2. Generally, thermal annealing is performed at 400-500℃ to activate source/drain dopants after gate dielectric deposition. Therefore, rapid thermal annealing (RTA) was carried out at 500 ℃ for 1 min to explore thermal stability of the ZrO_2/Ge stack. High-pressure H_2O treatment was conducted using supercritical CO_2 ($SCCO_2$) fluid that was mixed with 5 vol.% of propyl alcohol and 5 vol.% of pure H_2O at 100 ℃ for one hour. The $SCCO_2$ exists above its critical pressure (1170 psi) and temperature (30 ℃). Moreover, the solubility of H_2O also rises with increasing the CO_2 pressure.[59] With optimization of high-pressure H_2O treatment, the processing pressure was adopted at 3000 psi. The propyl alcohol was used as a modifier to enhance the solubility of the polar H_2O molecules in nopolar CO_2. The water was dissolved as small H_2O molecule clusters and uniformly mixed in $SCCO_2$ fluid. The $SCCO_2$ fluid exhibited a liquid-like property, giving it an excellent transport capacity. Also, supercritical fluid has gas-like properties and efficiently diffuses into nanoscale structures without damage.[54] Therefore, the H_2O effectively reacts with the thin film when dissolved in $SCCO_2$. Finally, 100 nm-thick sputtered TaN and 500 nm-thick thermally evaporated aluminum were deposited on the top surface of the ZrO_2 film with an electrode area of 7.07×10^{-4} cm^2, for use in MOS devices. The backside was also thermally evaporated aluminum as electrode.

4.4.2 Results and discussion

Figure 4-11 depicts the evolution of J_G for ZrO_2 on Ge substrate with various thermal treatments. Compared to Fig. 4-8, the behavior of J_G for ZrO_2 on Ge substrate is quite different to those on Si substrate. The symmetrical J_G of ZrO_2 on p-type Ge substrate at negative and positive electrical field is attributed to fast generation rate of minority carrier for Ge substrate. Additionally, the J_G of ZrO_2/Ge capacitor with standard condition has six orders of magnitude higher than ZrO_2/Si capacitor. Furthermore, the J_G of ZrO_2/Ge capacitor first decreases until 400 ℃ and then dramatically increases at 500 ℃, as shown in Fig. 4-11(b). The high and unstable J_G of ZrO_2/Ge capacitor may be related to formation, decomposition and incorporation of the Ge oxide during thermal process. The C-V characteristics of ZrO_2/Ge capacitor with various thermal treatments are shown in Fig. 4-12 and summarized in Table 4-3. The lower accumulation capacitance for standard condition and 500 ℃ RTA-treated samples is attributed to poor charge holding in leaky ZrO_2 layer, as shown in Fig. 4-11. Additionally, the inversion capacitance at positive bias for 500 ℃ RTA-treated samples is responded to poor interface quality between ZrO_2 and Ge substrate. Accordingly, appropriate thermal annealing (below 400 ℃) is helpful to improve the electrical performance of ZrO_2/Ge capacitor. While electrical degradation of ZrO_2/Ge capacitor was observed at 500 ℃ RTA, thermal annealing is usually adopted above 500 ℃ to activate dopant of source and drain. Therefore, repair of thermal damage in gate dielectric for Ge-based MOS device is essential.

Figure 4-13 presents the composition-depth profiling analysis for ZrO_2/Ge stack with vacuum annealing at 250 ℃ as standard process condition. The composition-depth profiling was analyzed by collecting XPS signals with various Ar^+ sputtering time. Singnals of O 1*s*, Zr $3p_{3/2}$ and Ge $2p_{3/2}$ were adopted to evaluate atom % without significant singnals interruption. An interfacial GeO_X signal was observed between ZrO_2 film and Ge substrate. Additionally, a high dosage of GeO_X is observed in the ZrO_2 thin film, and may have become incorporated during deposition and the thermal process. The following RTA was carried out in N_2 ambient at 500 ℃ for one min to explore thermal effect on Ge-MOS, as shown in Fig. 4-14. The intensity and incorporated dosage of GeO_X slightly decrease but still very high. The reduction of GeO_X after thermal RTA is attributed to vaporization of GeO_X.[60] Figure 4-15 shows composition-depth profile for ZrO_2/Ge after high-pressure H_2O post-gate treatment. High-pressure H_2O post-gate treatment caused the interfacial GeO_X signal to vanish and reduced the amount of GeO_X that was incorporated into the ZrO_2 thin film.

The cross-sectional HRTEM images in Fig. 4-16 show the sputtered ZrO_2 on Ge substrate with vacuum annealing at 250 ^oC before and after RTA at 500 ^oC. It indicates that both samples have a ZrO_2 film with a thickness of approximately 5.3 nm. Upon thermal annealing, the ZrO_2 films clearly underwent crystallization. Additionally, the 3.67 and 2.9 nm-thickness GeO_X layers are observed before and after RTA, respectively. The reduction of thickness for GeO_X is consistent with the results of composition-depth profiling in Fig. 4-14

and Fig. 4-15. The high-pressure H_2O treatment was further explored by examining HRTEM images in Fig. 4-17. Figure 4-17(a) depicts a 2.9 nm-thick interfacial GeO_X layer between ZrO_2 and Ge substrate following RTA. However, high-pressure H_2O treatment, as shown in Fig. 4-17(b) eliminated the interfacial GeO_X layer. This phenomenon reveals that the high-pressure H_2O post-gate treatment helps to eliminate the interfacial GeO_X layer in the ZrO_2/Ge stack.

The XPS spectra of Zr $3p_{3/2}$ and Ge $2p_{3/2}$ signals were carefully analyzed in Fig. 4-18 and Fig. 4-19, respectively, to explore further the reaction between ZrO_2 and GeO_x films during RTA and high-pressure H_2O post-gate treatment. The Zr $3p_{3/2}$ signal at a binding energy of around 333.2 eV is associated with ZrO_2, and is shown in Fig. 4-18. In the inset in Fig. 4-18, the peak value of the Zr $3p_{3/2}$ signal from the high-pressure H_2O-treated sample is shifted to a higher binding energy as the ion sputtering time increases, whereas the shift in the peak of the RTA-treated sample is negligible. The high binding energy shift of Zr $3p_{3/2}$ signal indicates that zirconia is further oxidized upon high-pressure H_2O treatment. Notably, oxidation is favored at the interface between ZrO_2 and Ge. In Fig. 4-19, the Ge $2p_{3/2}$ signals at binding energies of around 1217.26 eV and 1219.5 eV are associated with non-oxidized Ge and GeO_X, respectively.[61] The interfacial Ge oxide layer of the RTA treated sample is mostly GeO_X, and is eliminated by high-pressure H_2O treatment. Restated, the interfacial GeO_X layer is formed during deposition or a thermal process and is eliminated by high-pressure H_2O

treatment with Zr oxidation. Moreover, the elimination of GeO_X helps to reduce the gate leakage current, as shown in the Fig. 4-20.

While GeO_2 is hydrolyzable in H_2O, the GeO_X layer isn't directly dissoluble in H_2O.[62] In Fig. 3, it is observed that GeO_X layer is eliminated with further oxidation of Zr, occurred at the interface between ZrO_2 and Ge. Therefore, it is reasonably inferred that oxidation and reduction reactions may occur at the interface between ZrO_2 and GeO_X during high-pressure H_2O treatment and are as follows.

$$Zr+2H_2O \rightarrow ZrO_2+2H_2 \quad (1)$$

$$GeO+H_2 \rightarrow Ge+H_2O \quad (2)$$

According to the previous findings, it is inferred that the H_2O is taken as oxidant and reacts with the non-oxidized Zr film close to the GeO_X interlayer by dissolving in supercritical fluid. The amounts of ionic products, H_3O^+ and OH^- radicals, in H_2O at high pressure may be orders of magnitude higher than those obtained in ambient water. The higher amounts of free radicals are associated with a strengthened oxidation reaction between H_2O and non-oxidized Zr owing to the higher collision frequency.[29] Moreover, the generation of hydrogen using Zr and H_2O has also been reported elsewhere.[63] In the presence of H_2, the reaction of Eq. (2) proceeds spontaneously (ΔG=-42.96 kJ/mol at 100 ℃) and GeO_X is reduced by H_2.[64] Therefore, high-pressure H_2O treatment effectively eliminates the undesired interfacial GeO_X layer in the ZrO_2/Ge stack. Additionally, Zr oxidation is favored at

the interface between ZrO_2 and Ge because H_2 is effectively consumed by GeO_X.

4.4.3 Summaries

In summary, this investigation studied the effect of high-pressure H_2O treatment on the sputter-deposition of ZrO_2 on Ge substrate. The H_2O oxidant is carried into the ZrO_2 thin film by supercritical CO_2 fluid in which H_2O oxidant is dissolved. According to the composition-depth profiles from the analyses of XPS and HRTEM images, a GeO_X layer is formed at the interface between ZrO_2 and Ge during deposition and thermal cycles, and eliminated by high-pressure H_2O treatment. The analysis of XPS spectra reveals that the H_2O oxidant reacts with non-oxidized Zr film close to the GeO_X interlayer and produced H_2 further reduces GeO_X. Additionally, the elimination of GeO_X helps to reduce the gate leakage current.

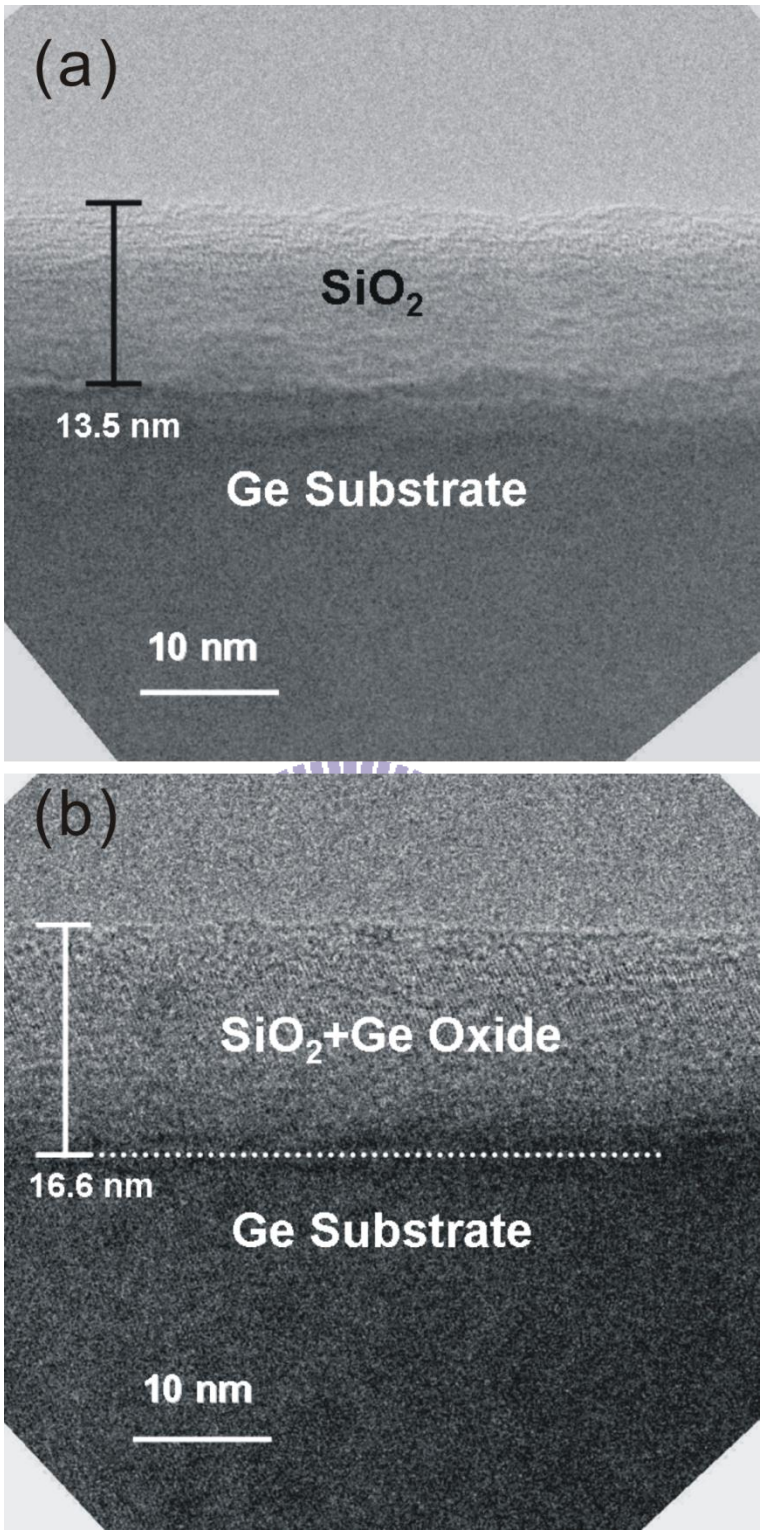

Figure 4-1 The cross-sectional HRTEM images of LPCVD-SiO_2 on epi-Ge substrate (a) before and (b) after high-pressure H_2O treatment.

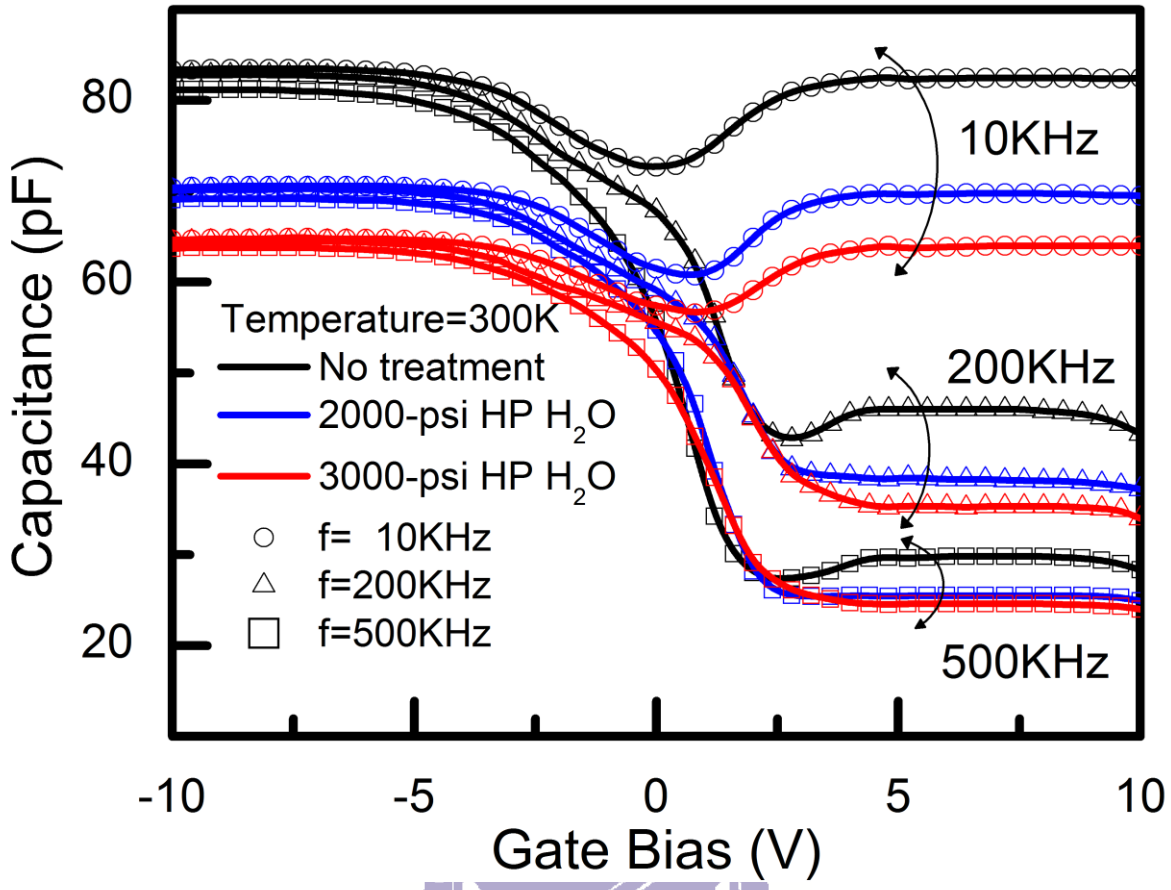

Figure 4-2 The C-V characteristics of Ge-MOS devices with various pressure H_2O treatments at temperature=300K.

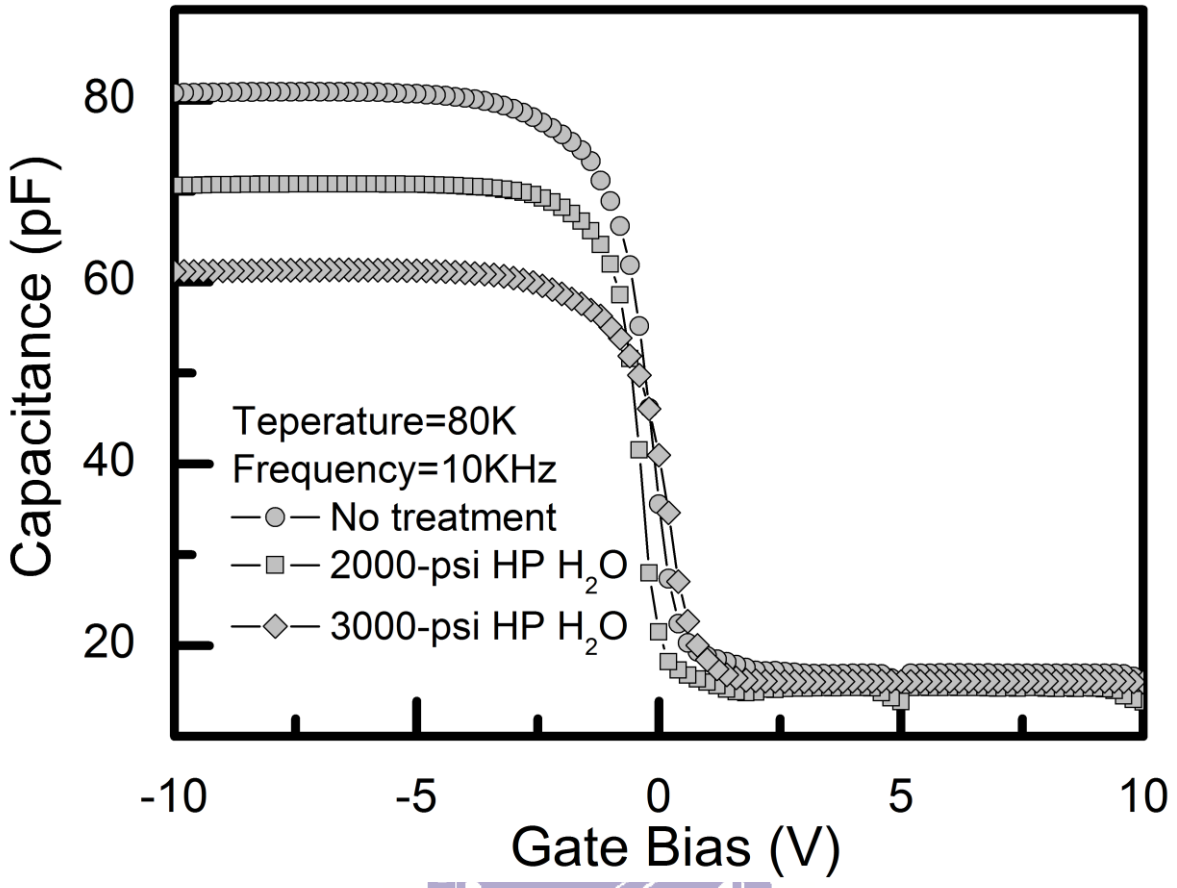

Figure 4-3 The C-V characteristics of Ge-MOS devices with various pressure H_2O treatments at temperature=80K.

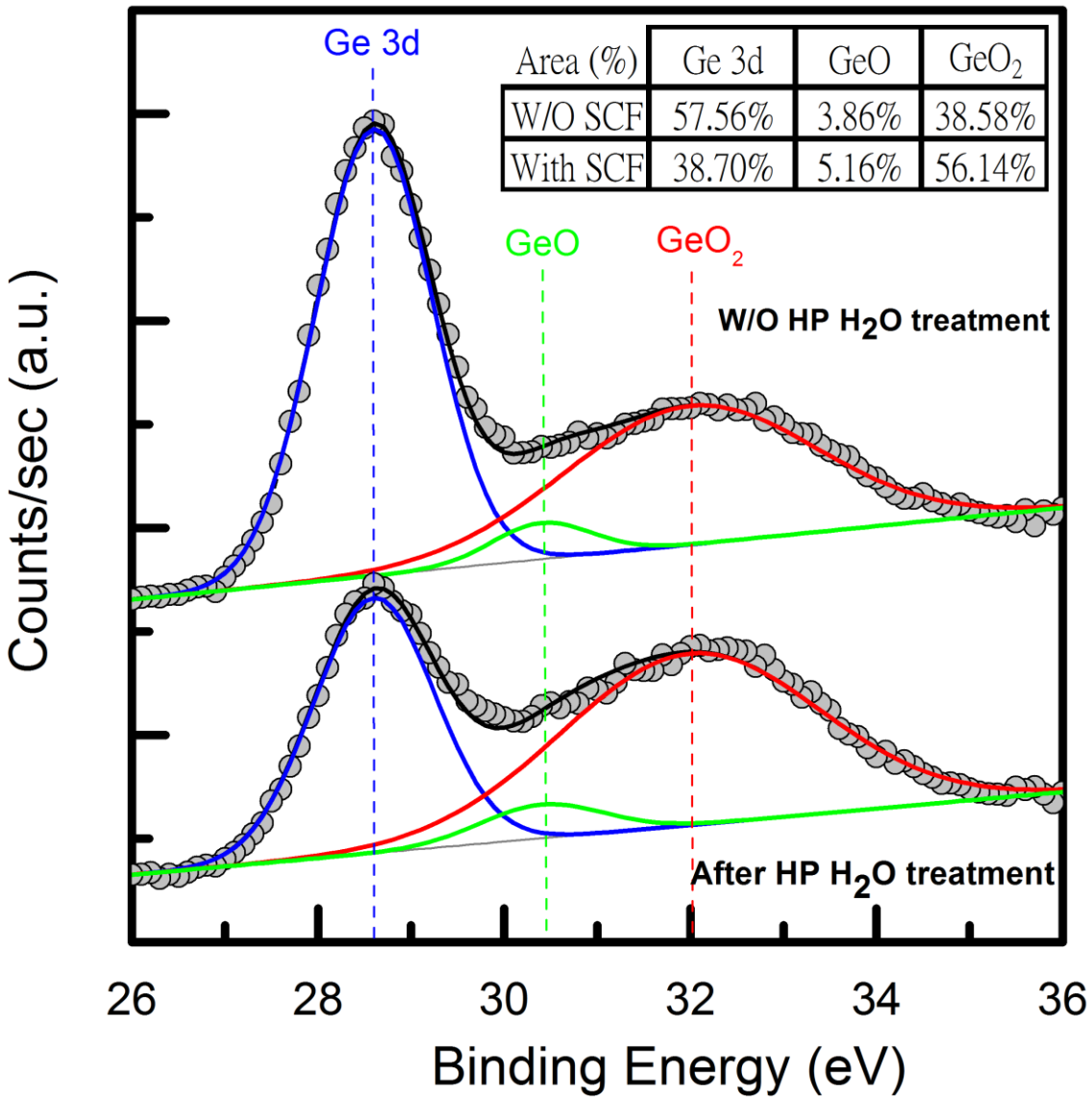

Figure 4-4 XPS spectra of Ge 3d signal of HfO_2 on the epi-Ge channel layer with and without HP H_2O treatment.

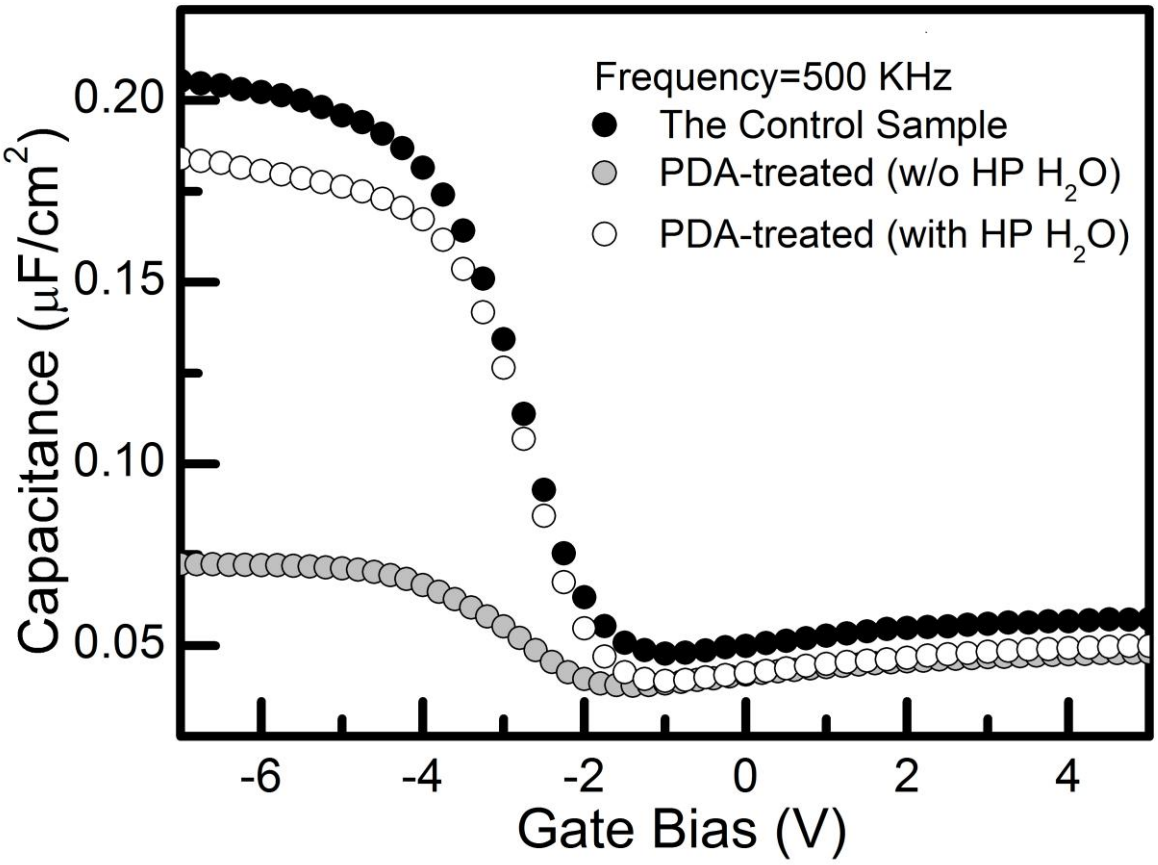

Figure 4-5 The C-V characteristics of 450 °C PDA-treated Ge-MOS devices before and after HP H_2O treatment.

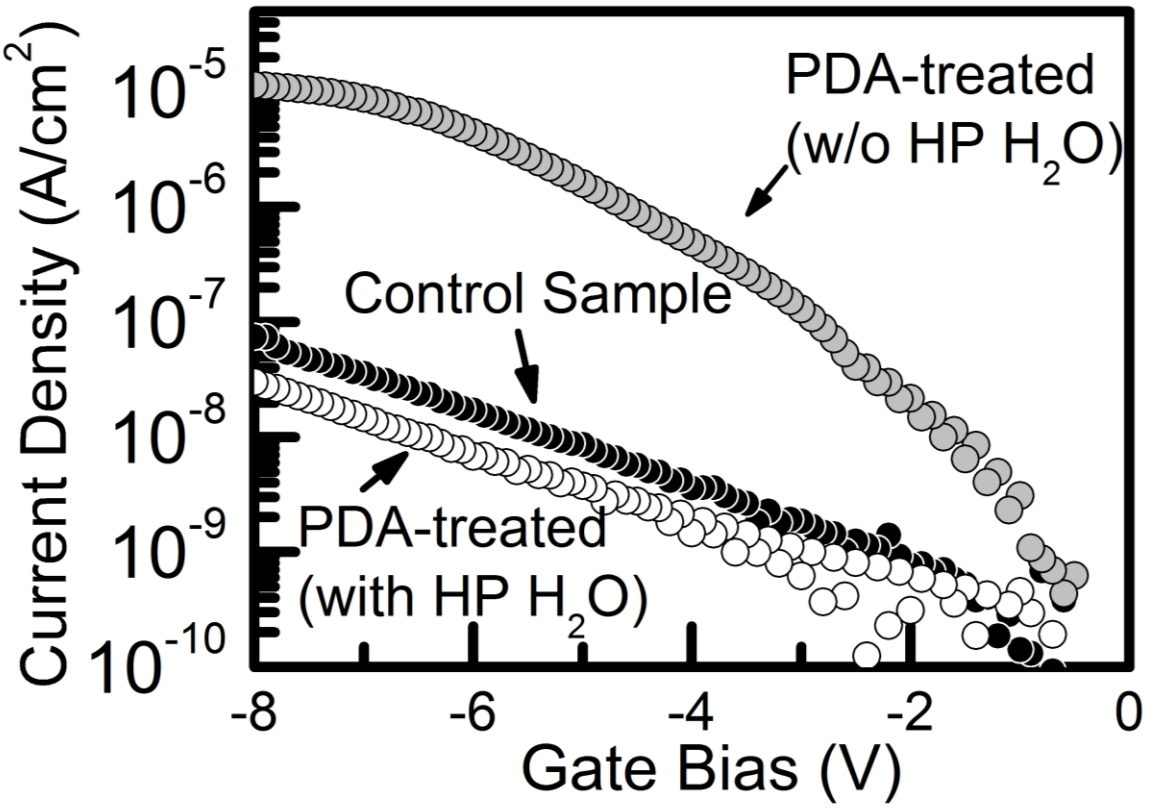

Figure 4-6 The gate leakage current density of PDA-treated Ge-MOS devices before and after HP H_2O treatment.

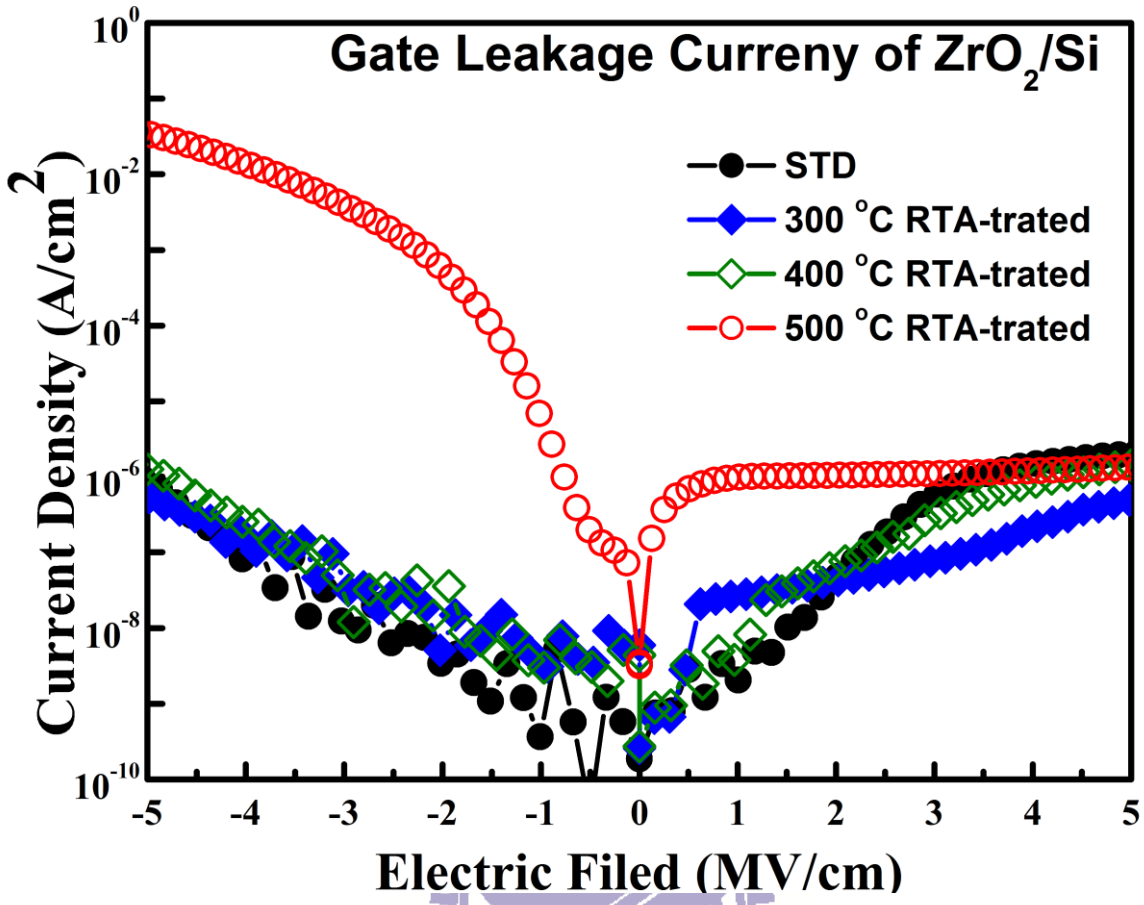

Figure 4-7 The gate leakage current density of sputtered-ZrO_2 on Si with various thermal treatments.

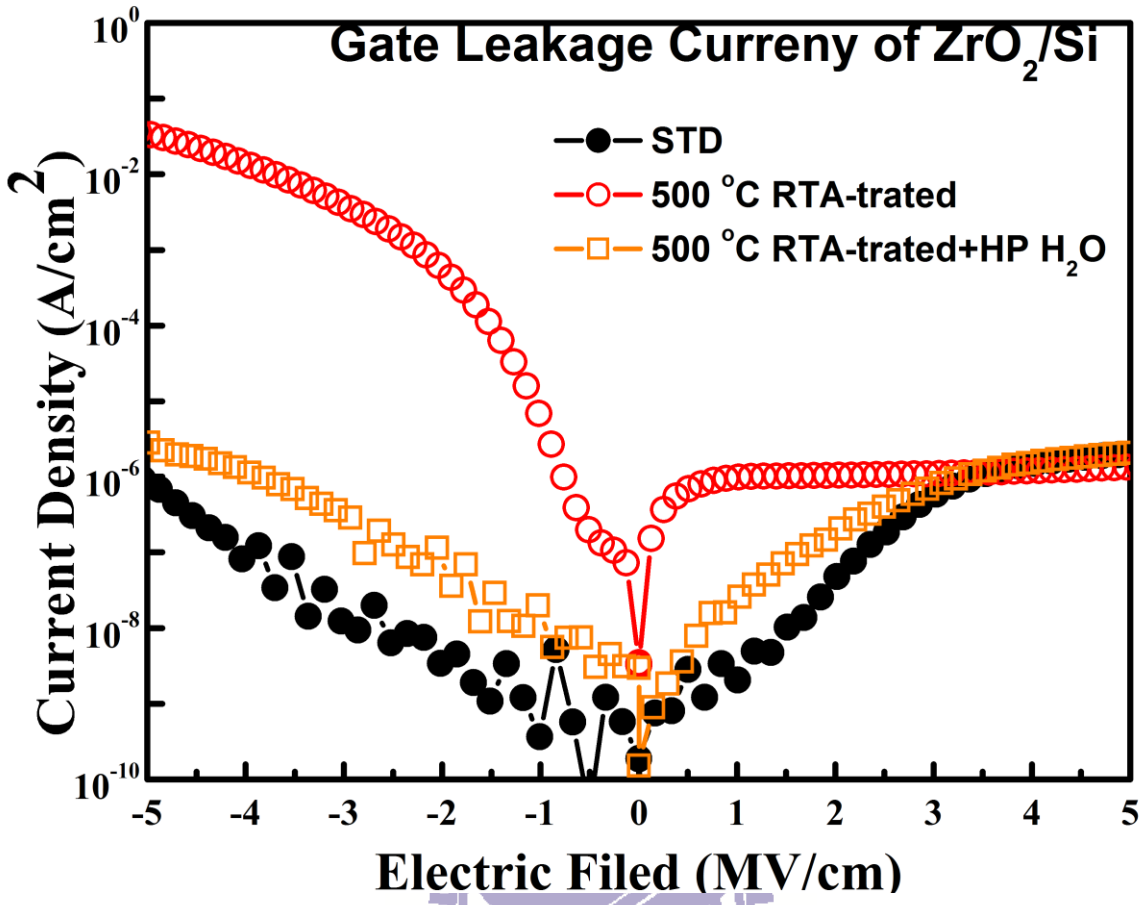

Figure 4-8 The gate leakage current density of sputtered-ZrO_2 on Si with 500 °C RTA before and after HP H_2O treatment.

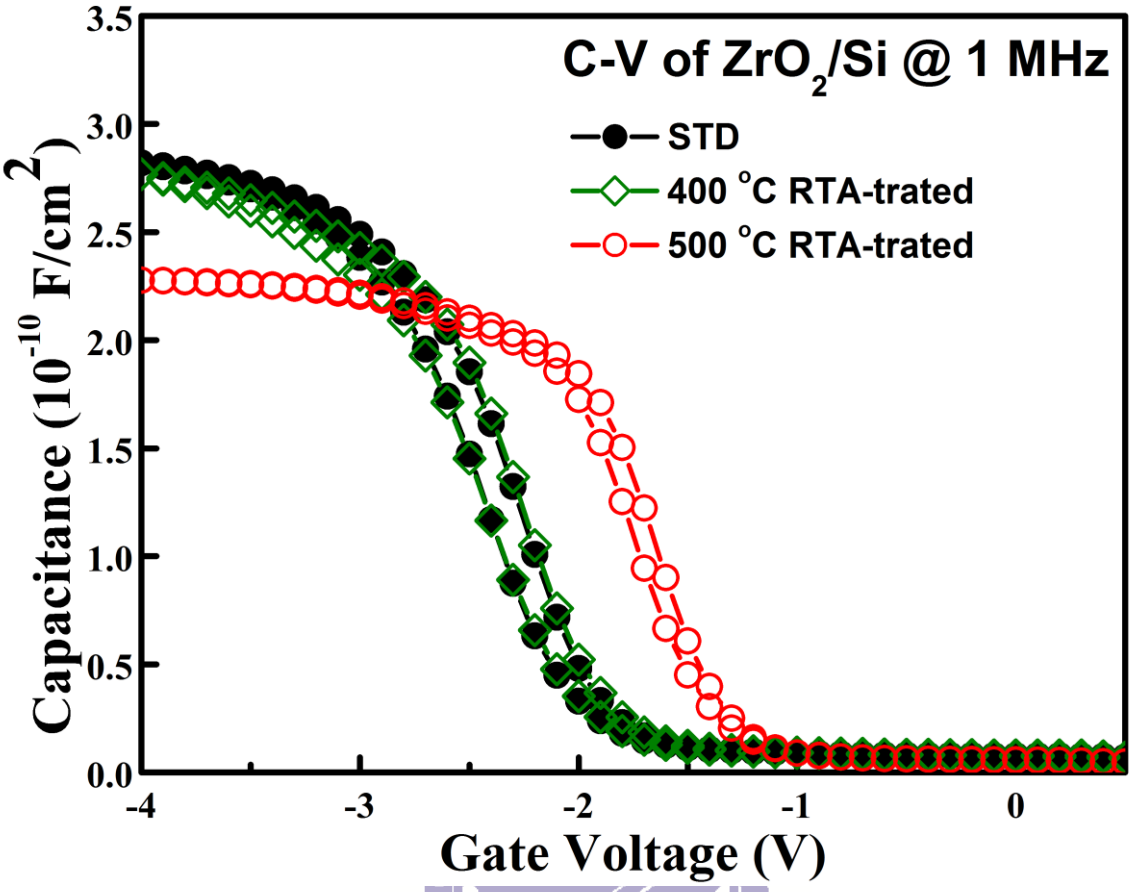

Figure 4-9 The C-V characteristics of sputtered-ZrO_2 on Si with various thermal treatments.

	STD	RTA Treated	
		400 ℃	500 ℃
V_{fb} (V)	-2.33	-2.46	-1.78
ΔV_{fb} (V)	0.15	0.17	0.09
THK (nm)	10.5	12.0	12.5
CET (nm)	3.85	3.92	4.76
ε_{eff}	10.64	11.94	10.24

Table 4-1 The summary of C-V characteristics for sputtered-ZrO_2 on Si with various thermal treatments.

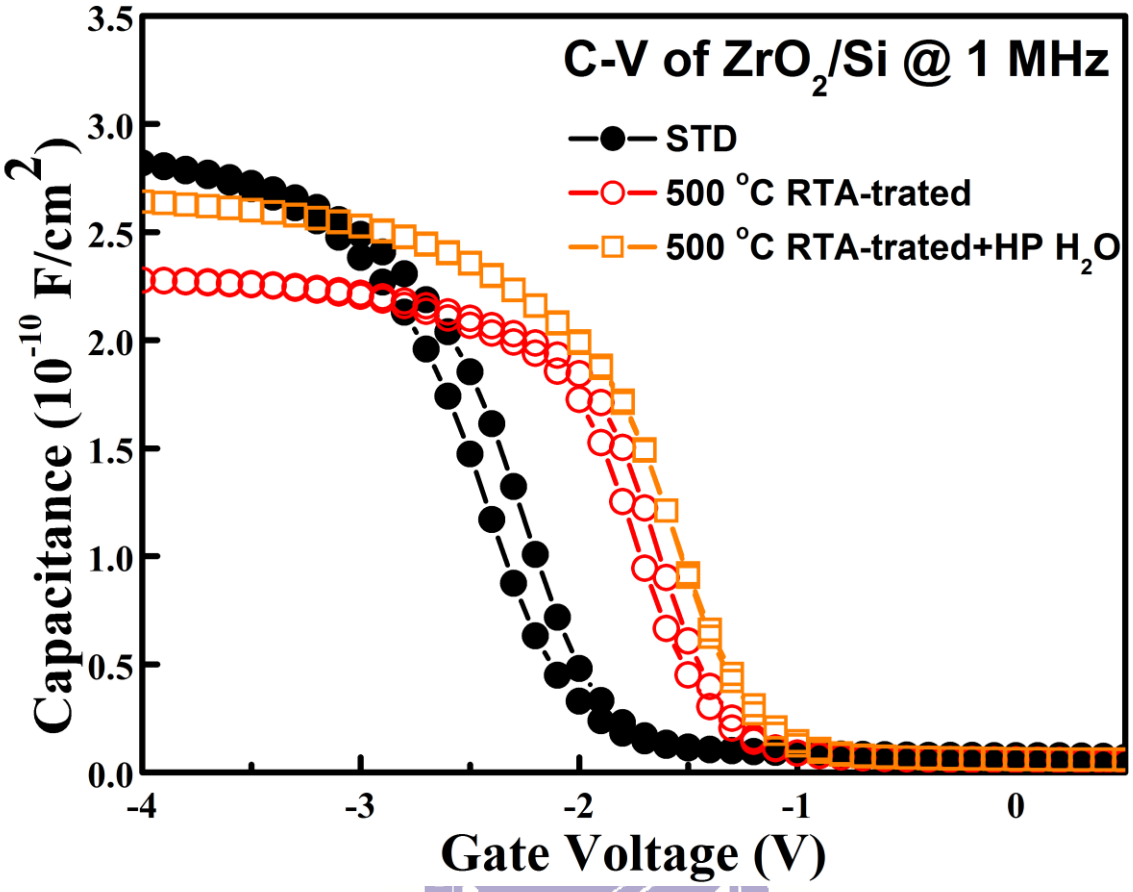

Figure 4-10 The C-V characteristics of sputtered-ZrO_2 on Si with 500 °C RTA before and after HP H_2O treatment.

	STD	RTA Treated 500 °C	HP H_2O
V_{fb} (V)	-2.33	-1.78	-1.63
ΔV_{fb} (V)	0.15	0.09	0
THK (nm)	10.5	12.5	12.5
CET (nm)	3.85	4.76	4.11
ε_{eff}	10.64	10.24	11.87

Table 4-2 The summary of C-V characteristics for sputtered-ZrO_2 on Si with 500 °C RTA before and after HP H_2O treatment.

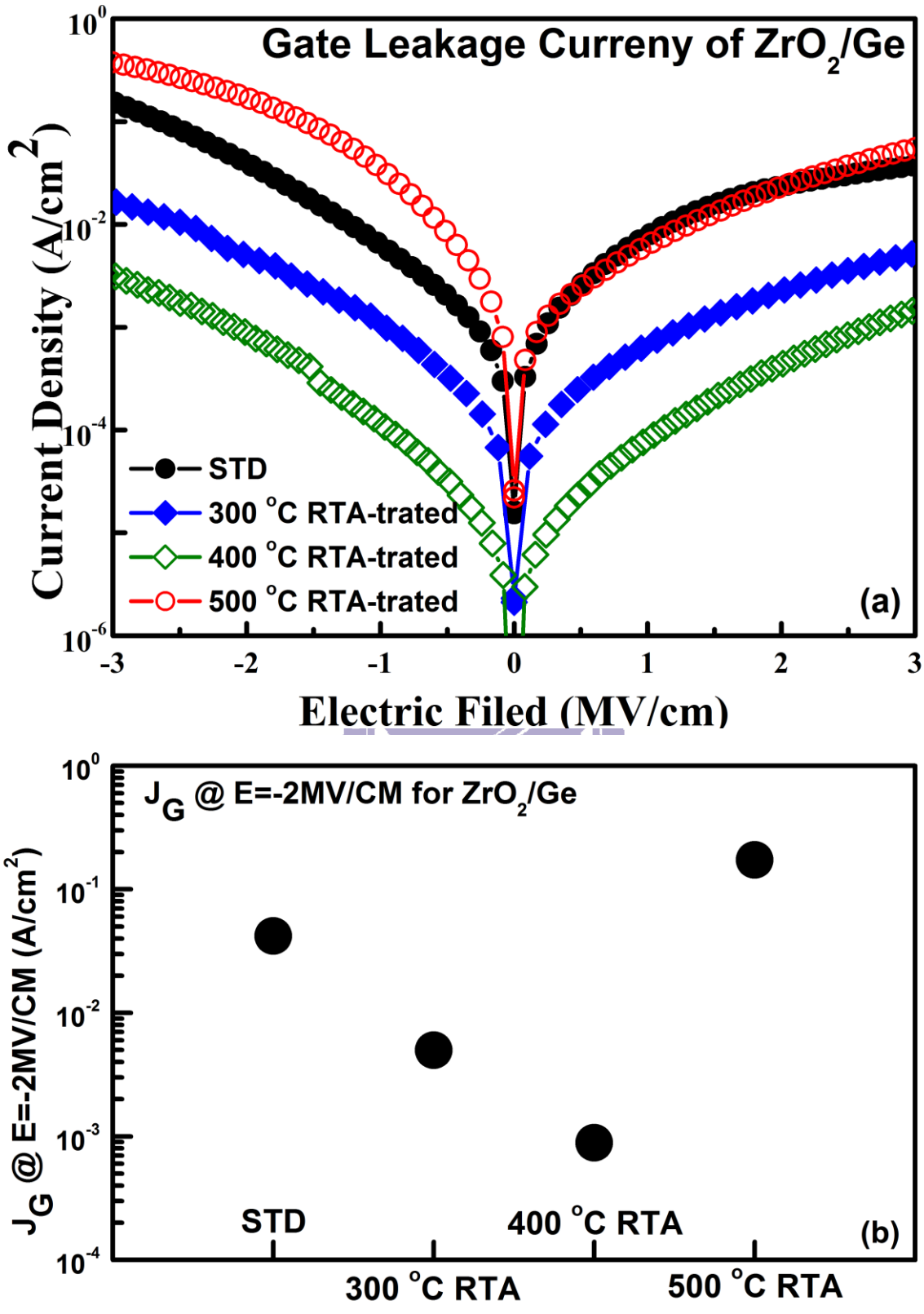

Figure 4-11 The gate leakage current density of ZrO_2/Ge capacitor with various thermal treatments.

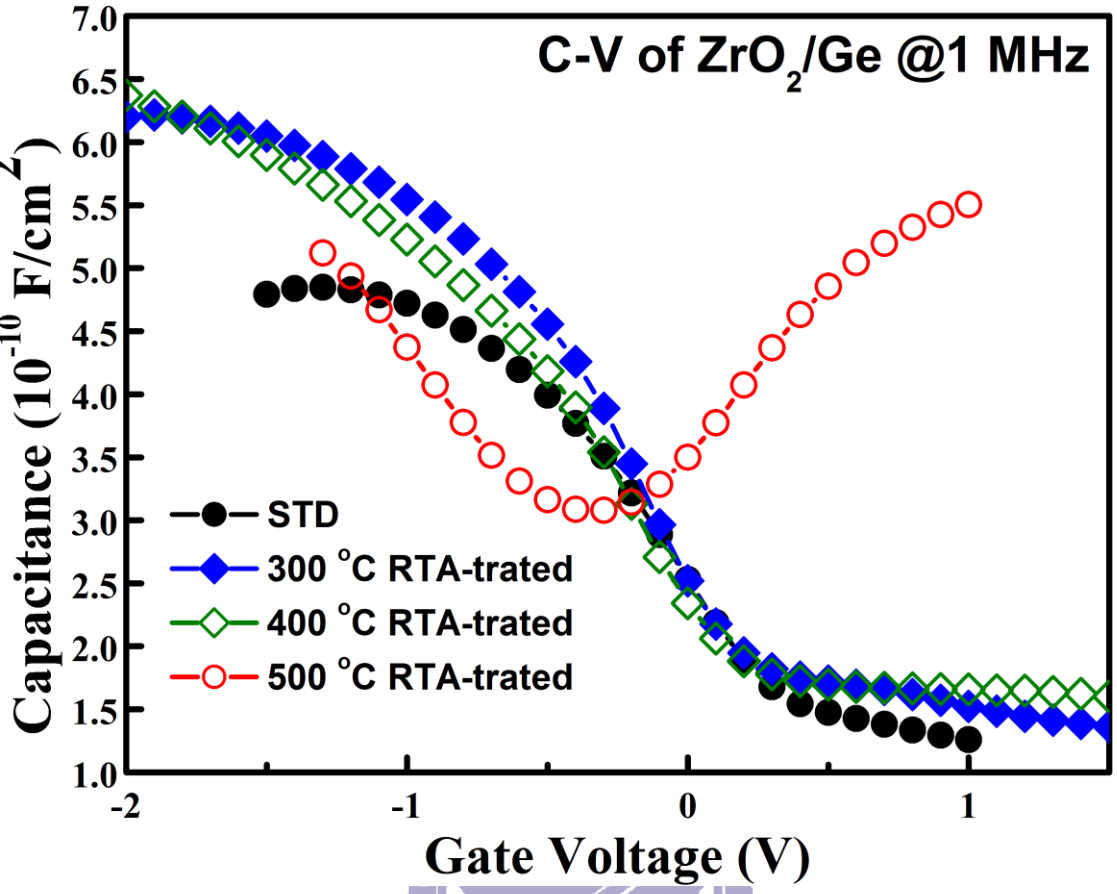

Figure 4-12 The C-V characteristics of ZrO_2/Ge with various thermal treatments.

	STD	RTA Treated		
		300 ℃	400 ℃	500 ℃
CET (nm)	2.23	1.7	1.74	1.97
THK (nm)	8.98	N/A	N/A	8.21
ε_{eff}	15.7	N/A	N/A	16.3

Table 4-3 The summary of C-V characteristics for sputtered-ZrO_2 on Ge with various thermal treatments.

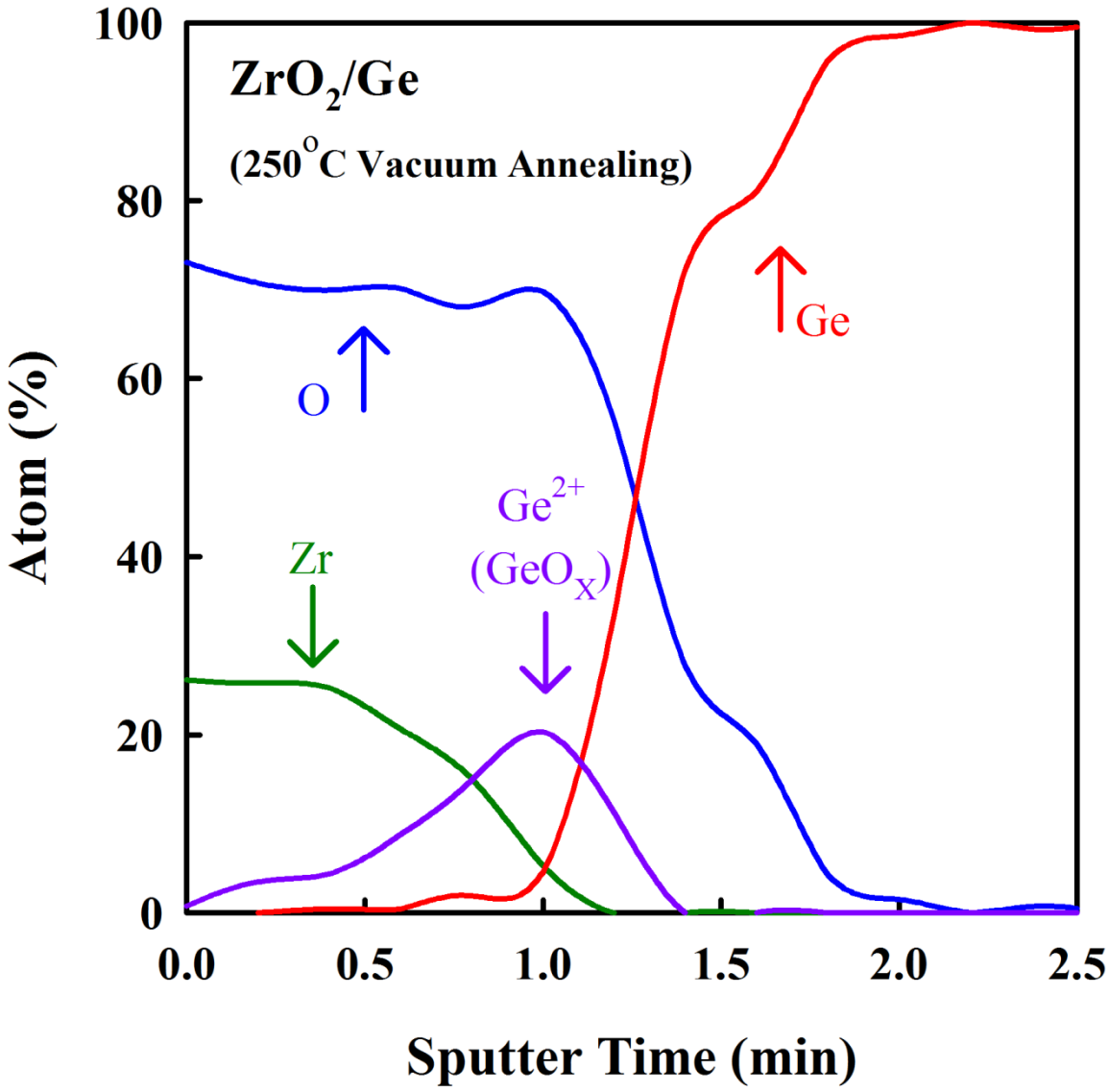

Figure 4-13 The composition-depth profiling analysis of XPS with vacuum annealing at 250 °C for 30 mins.

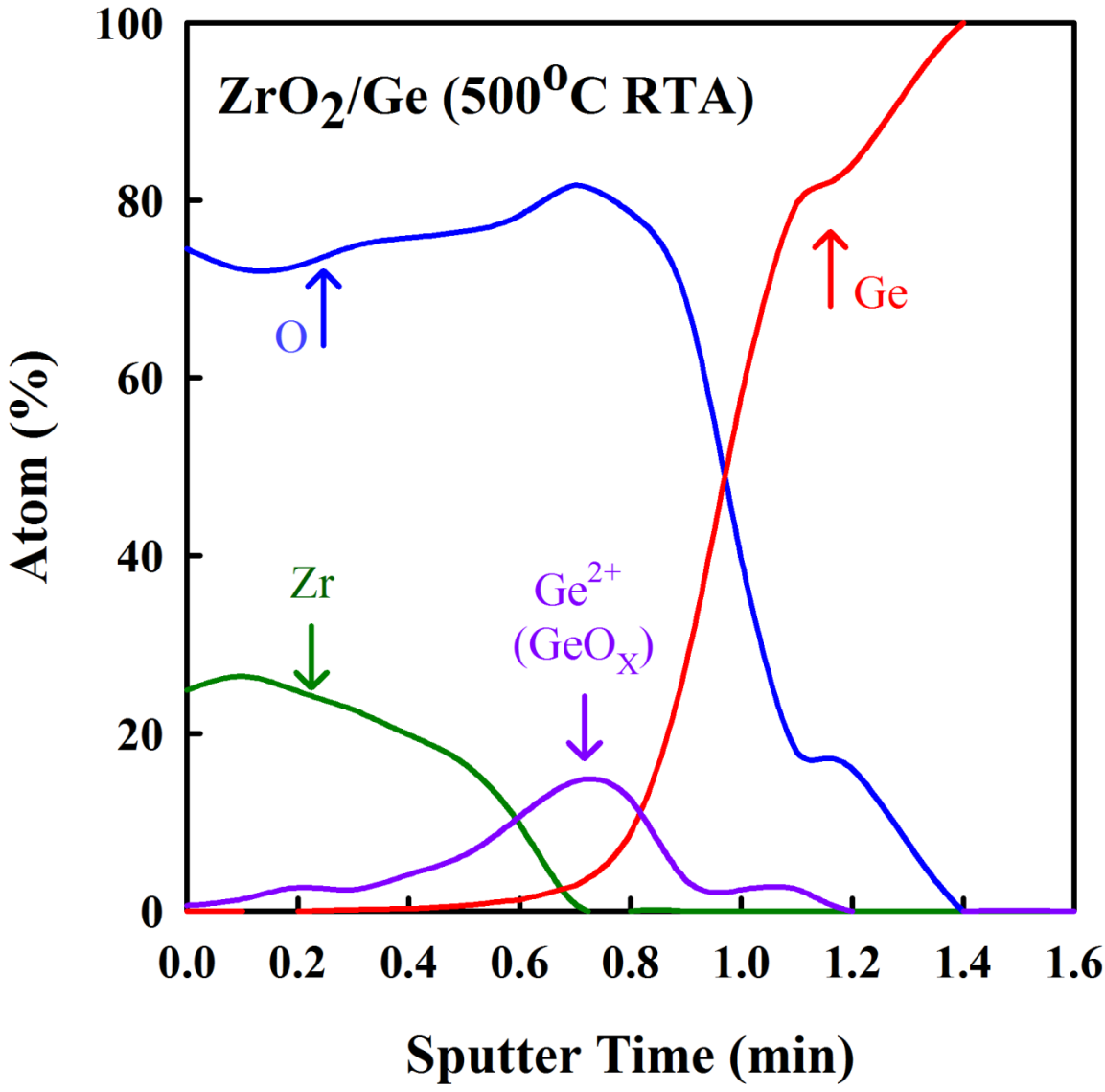

Figure 4-14 The Composition-depth profiling analysis of XPS with RTA at at 500 °C before HP H_2O treatment.

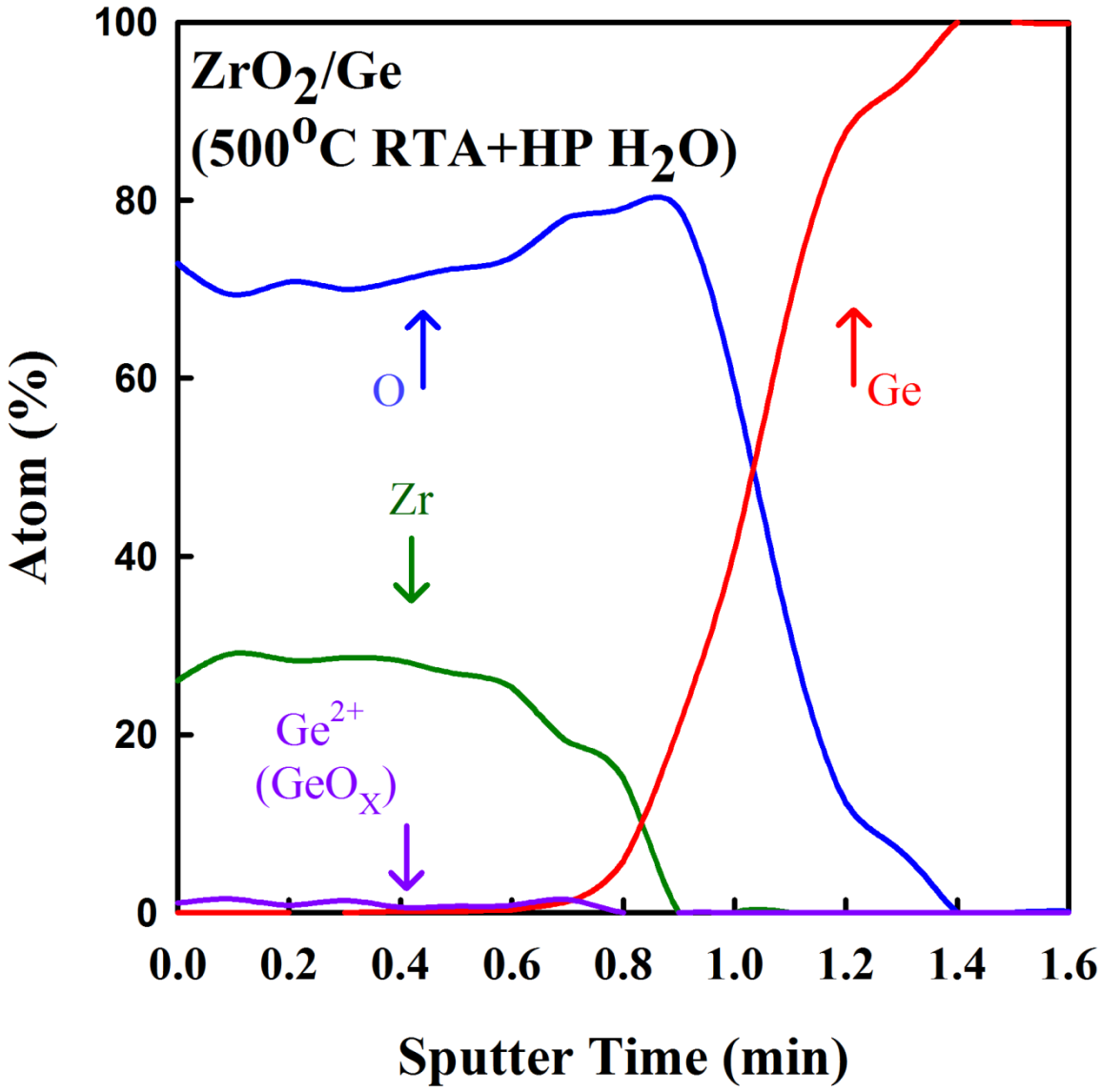

Figure 4-15 The Composition-depth profiling analysis of XPS with RTA at at 500 °C after HP H_2O treatment.

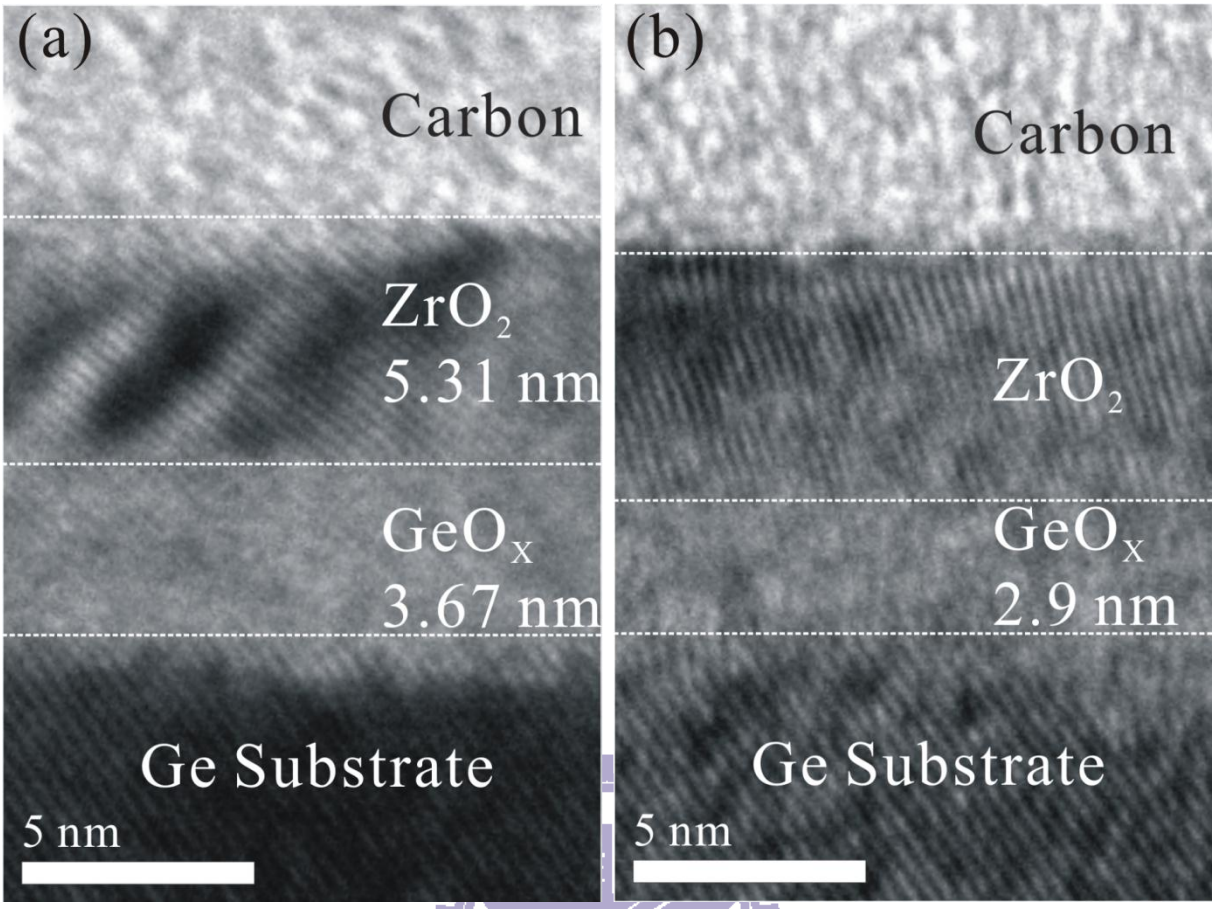

Figure 4-16 The cross-sectional HRTEM images of sputtered ZrO_2 on Ge substrate with vacuum annealing at 250 ^{o}C (a) before and (b) after RTA at 500 ^{o}C

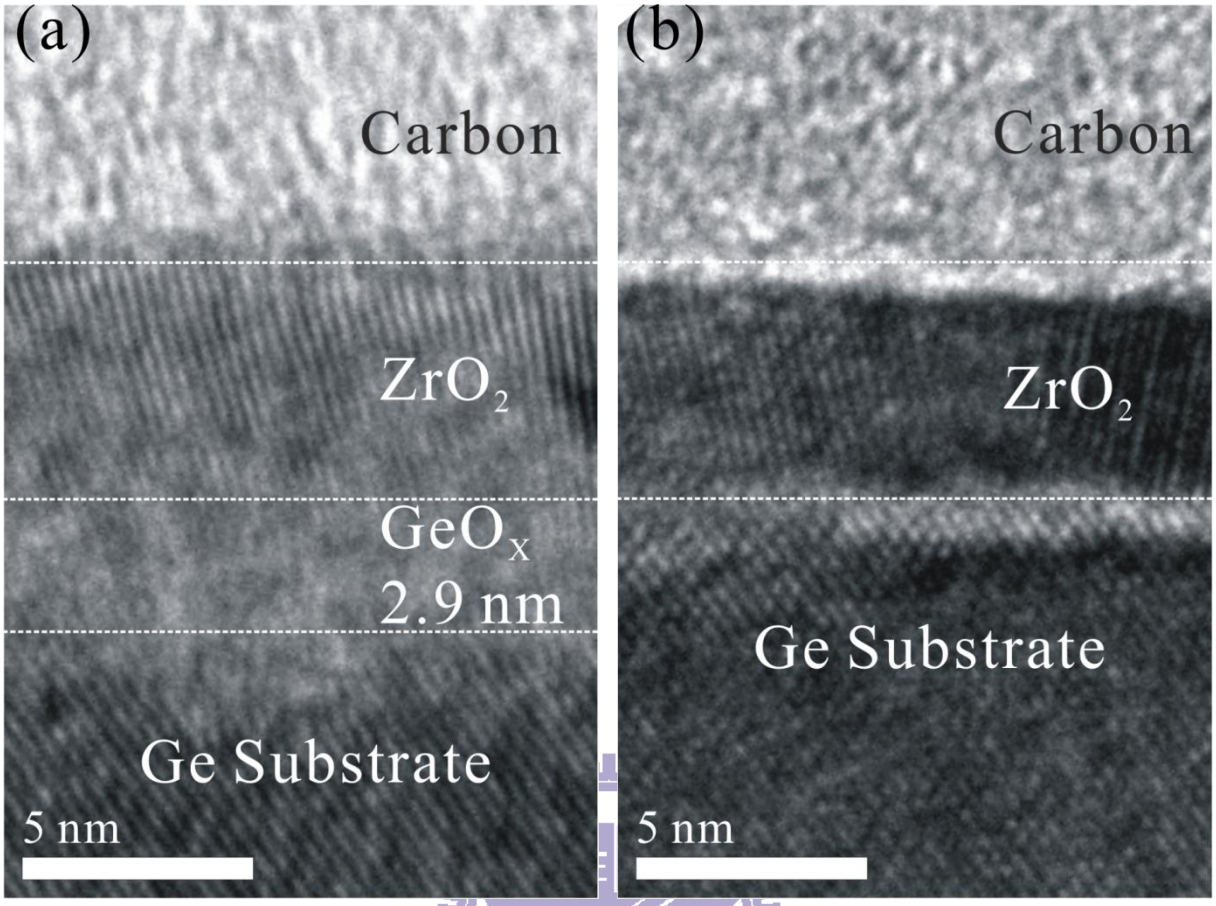

Figure 4-17 The cross-sectional HRTEM images of sputtered ZrO_2 on Ge substrate with vacuum annealing and RTA (a) before and (b) after HP H_2O treatment.

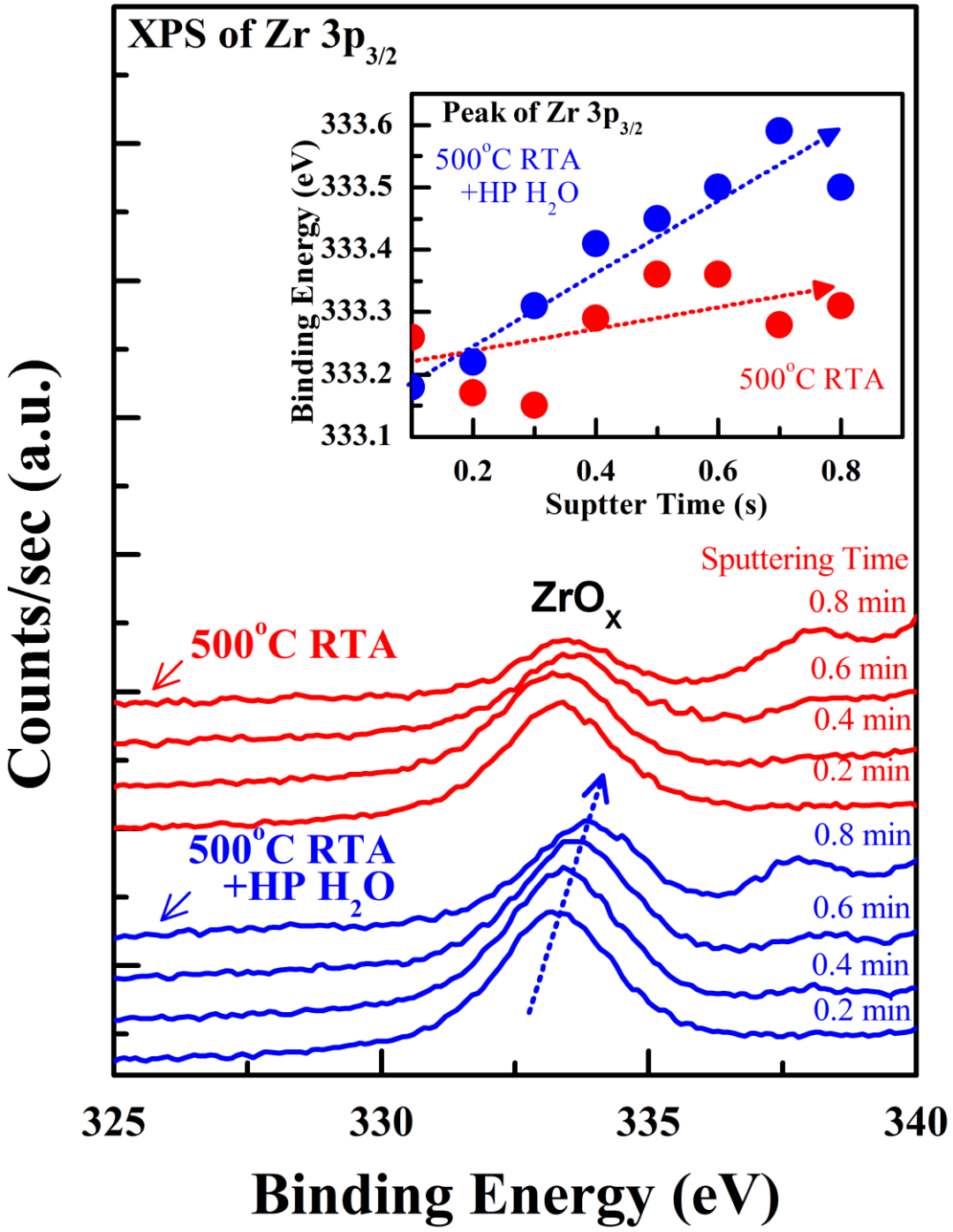

Figure 4-18 XPS spectra of Zr $3p_{3/2}$ signals with various treatments.

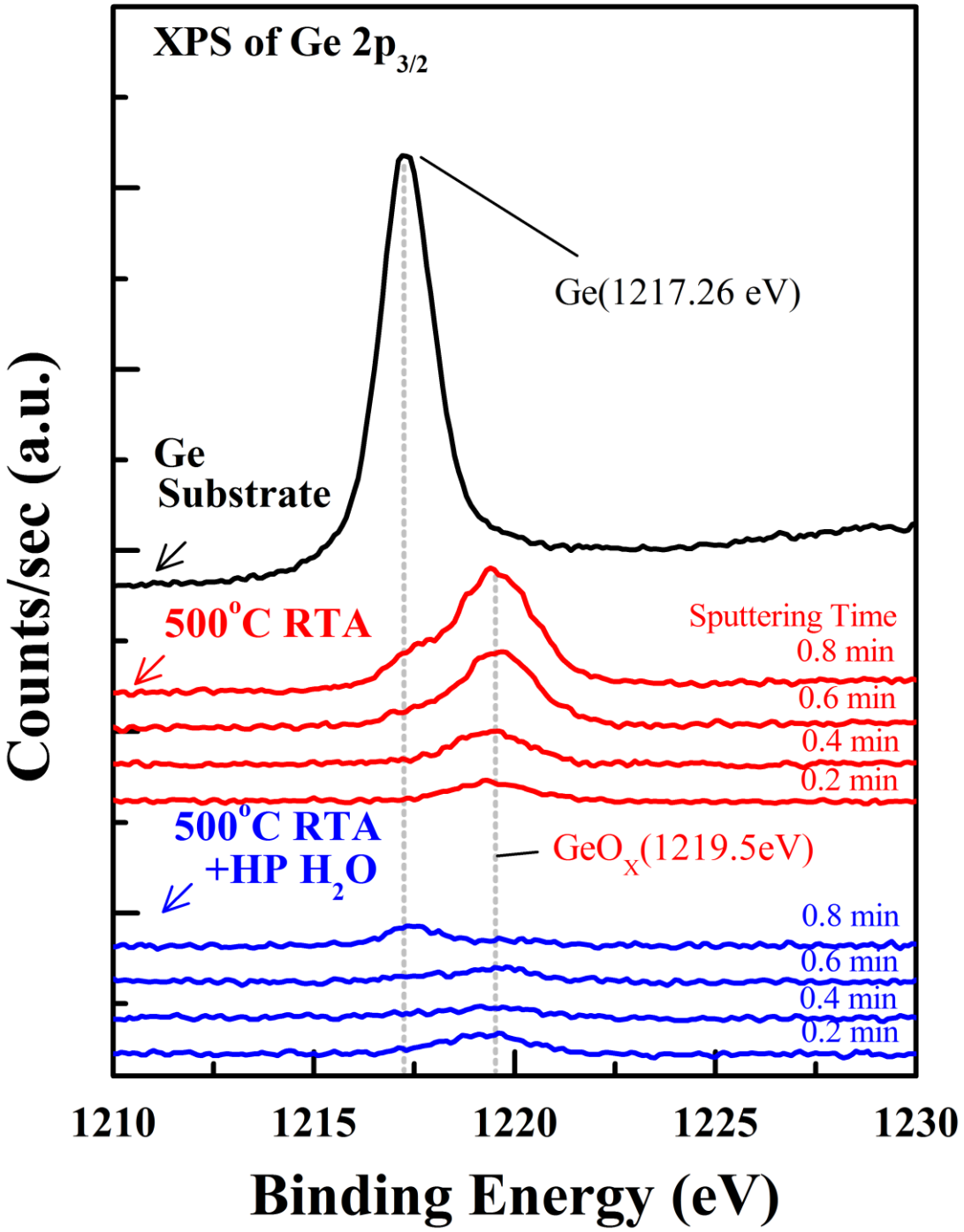

Figure 4-19 XPS spectra of Ge $2p_{3/2}$ signals with various treatments.

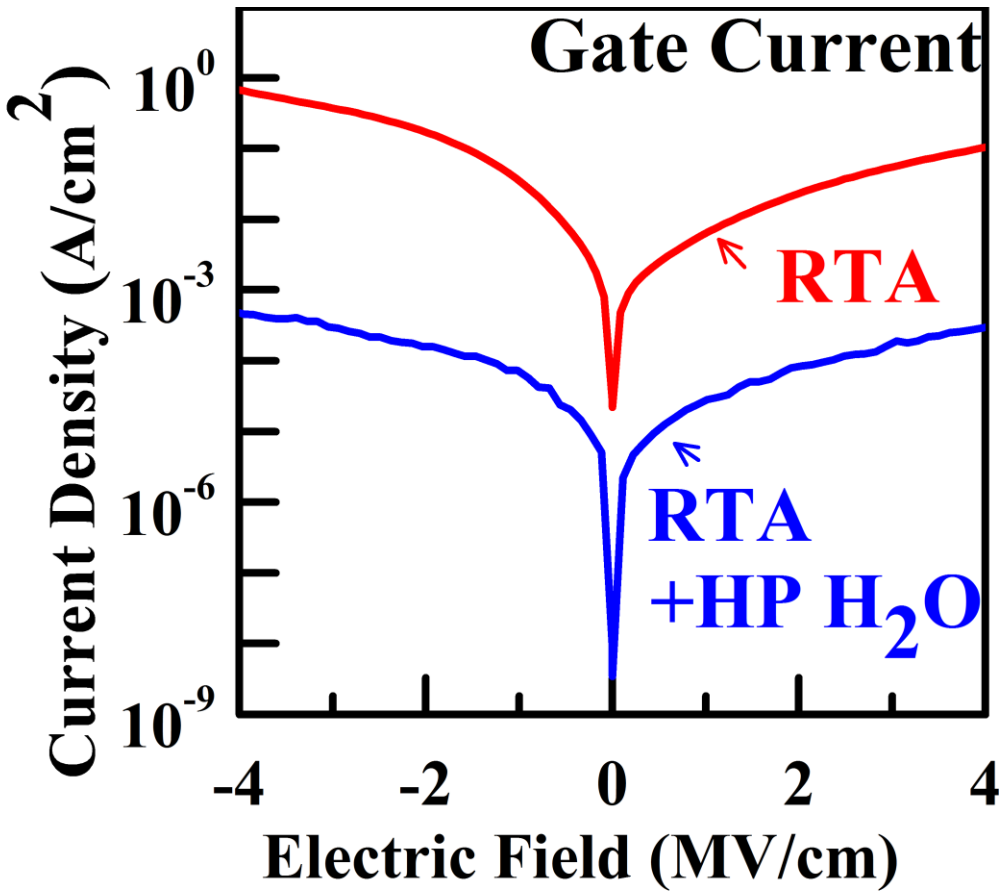

Figure 4-20 The gate leakage current of RTA-treated sample before and after HP H_2O treatment.

Chapter 5

Effect of Water Vapor and Hydrogen Annealing on ZrO_2/Ge Stack

5.1 Review and motivation

In the previous chapter, it is observed that the H_2O and H_2 play important roles in high-pressure H_2O treatment to eliminate GeO_X interlayer and suppress the degradation of gate leakage current. The main mechanisms involve the oxidation of non-oxidized Zr with H_2O and the reduction of GeO_X by H_2. Although the high-pressure H_2O treatment effectively eliminates the GeO_X interlayer, the high-pressure system has not been widely employed in manufacture facilities. X. Zou et al. has reported the effect of water vapor annealing for HfTiON on suppressed growth of unstable GeO_X.[51] However, the water vapor annealing of ZrO_2 has not been reported before. In this chapter, rapid thermal annealing of ZrO_2 on Ge substrate was investigated in H_2O, H_2 and N_2 to clarify the influence of ambient gas on ZrO_2/Ge capacitor.

5.2 Device fabrication

The Ge substrate was a (100) Ga-doped *p*-type wafer with a resistivity of 1-10 Ω cm. The wafers were cleaned with diluted HF (1:50) and rinsed DI water for several cycles to remove the unstable native oxide. After drying, the ZrO_2 thin film was deposited by radio-frequency sputtering in Ar ambient with a highly pure ZrO_2 (99.99%) target at 100 W.

During sputtering, the chamber pressure was set at 3×10^{-3} Torr. Following the deposition of ZrO_2, RTA was carried out at 300 ℃ and 500 ℃ for 3 minute in N_2/H_2O, H_2 and N_2 to investigate the influence of annealing ambience on ZrO_2/Ge stack. The N_2/H_2O annealing was realized by bubbling pure N_2 through de-ionized water at 75 ℃ with a flow rate of 50 sccm. Finally, 100 nm-thick sputtered TaN and 500 nm-thick thermally evaporated aluminum were deposited on the top surface of the ZrO_2 film with an electrode area of 7.07×10^{-4} cm^2, for use in MOS devices. The backside was also thermally evaporated aluminum as electrode.

5.3 Results and discussion

Figure 5-1 depicts the C-V characteristics of ZrO_2 on Ge substrate with RTA at 300 ℃ in N_2/H_2O, H_2 and N_2 ambiences. Additionally, the values of CET, V_{FB} and hysteresis for C-V characteristics are summarized in Figs. 5-2 and 5-3. Although the CET of standard-sample without any thermal treatment has the smallest value about 1.7 nm, the positive V_{FB} and hysteresis relate to negative fixed charge and large amount of border traps existing in transition layer between ZrO_2 and Ge substrate. After N_2-RTA treatment at 300 ℃, the reduction of V_{FB}, hysteresis and increment of CET imply formation of GeO_X interlayer during thermal annealing. The roll-off of C-V at accumulation region (negative bias region) is relative to high gate leakage current and also causes overestimation of CET. After N_2/H_2O and H_2 RTA at 300 ℃, the values of CET apparently decrease to 2.9 nm and 2.6 nm, respectively. The phenomena of CET reduction are attributed to suppression of GeO_X

formation by adding H_2O and H_2 gas during thermal annealing. The further material analysis will be examined later.

The gate leakage currents of ZrO_2 on Ge substrate with RTA at 300 ℃ in N_2/H_2O, H_2 and N_2 ambiences are shown in Fig. 5-4. It is observed that the RTA treatment, especially for N_2-RTA, causes gate leakage currents increasing. With the same thermal budget, ZrO_2/Ge capacitors annealing in the N_2/H_2O and H_2 corresponsively have lower gate leakage current. Further transportation mechanisms of carriers in ZrO_2/Ge stack were analyzed by using Poole-Frenkel emission (P-F), Ohmic and trap-assisted tunneling (TAT) model. [65, 66]

The P-F emission is due to the emission of trapped election into the dielectric conduction band. The supply of electron from the traps is through thermal emission. The current due to P-F emission is given by

$$J_{PF} \propto V \exp\left[\frac{q}{k_B T}\left(2a\sqrt{V} - \Phi_{PF}\right)\right] \quad (1)$$

$$Slope_{1/T} = \left(\frac{2qa}{k_B}\right)\sqrt{V} - \frac{\Phi_{PF}}{k_B} \quad (2)$$

$$a = \sqrt{q/4\pi\varepsilon_i d} \quad (3)$$

where J_{PF}, q, k_B, V, ϕ_{PF}, ε_i and d are gate leakage current density, electron charge, Boltzmann constant, barrier height of P-F emission, dielectric permittivity and dielectric thickness, respectively. The dependence of gate leakage current on measuring temperature are displayed in Fig. 5-5. The $slope_{1/T}$ of J_G versus 1/T is a function of gate bias and show in Fig. 5-6. The trap barrier heights of P-F emission are shown in Table 5-1. However, the extracted

dielectric constants of N_2/H_2O, H_2 and N_2 are given unacceptably values. This indicates to some other dominant mechanism in low electrical fields.

The results of Ohmic conduction fitting are shown in Fig. 5-7. The power law dependence of J_G and V_G ($J_G=AV_G^n$) is observed at low gate bias region and the values of n are about 1. It indicates an Ohmic type conduction at low electrical field. This type of low field current conduction may be due to a hopping mechanism where current is carried by thermal excited electrons moving between isolated discrete defect states in gate dielectric. However, it is hard to determinate the impact of RTA ambiences on ZrO_2/Ge capacitor.

The TAT model presents a two-step tunneling process via traps generated in the dielectric. The tunneling current J_{TAT} is given (approximately) by

$$J_{TAT} \propto \exp\left[-\frac{8\pi\sqrt{2qm_{ZrO_2}}}{3hE}\Phi_{TAT}^{3/2}\right] \quad (4)$$

where m_{ZrO2}, h and ϕ_{TAT} are the effective mass of tunneling electron in ZrO_2, Plank constant and the trapping energy level below dielectric conduction band, respectively. The plot of ln(J_G) versus 1/E in Fig. 5-8 shows a linear relationship indicating that gate leakage current at high electrical field is due to TAT mechanism. It is noted that TAT of N_2-RTA treated sample, comparing to others, occurs at lower electrical field. Additionally, the corresponding extracted parameters are listed in Table 5-2. The derived trapping energy level of N_2-RTA is apparently shallower than standard sample. The result indicates that thermal treatment of ZrO_2/Ge capacitor, even at such low temperature, worsen gate leakage current.

Comparing to N_2-RTA, the H_2O and H_2 have deeper trapping energy level and greatly suppress degradation of gate leakage current during thermal process, especially for H_2 ambience.

In order to further explore the thermal effect on GeO_X, the composition-depth profiling analysis of ZrO_2 on Ge substrate with RTA treatment in various ambiences at 300 ℃ and 500 ℃ are examined in Figs. 5-9, 5-10 and 5-11. In the Fig. 5-9, the sputtered-ZrO_2 on Ge without thermal treatment shows that GeO_X is incorporated and can't be clearly discriminated from ZrO_2 and Ge layers. The existence of defective GeO_X interlayer is associated with larger hysteresis of C-V characteristic in Fig. 5-1. After N_2-RTA at 300 ℃, the GeO_X interlayer is clearly formed and interfacial Ge content increases, as shown in Fig. 5-11 (a). The GeO_X formation and interfacial Ge increment are attributed to thermal oxidation and diffusion during N_2-RTA at 300 ℃, respectively. However, when the RTA is performed in N_2/H_2O ambience, atom % of GeO_X decreases from 11.34% to 7.45%, as shown in Fig. 5-10 (b). The thermal annealing temperature was further elevated to 500 ℃, as shown in Fig. 5-11. In Fig. 5-11 (a), GeO_X interlayer is also formed, but the amount slightly decreases in comparison with standard sample. It could be originated from the decomposition of GeO_2 above 420 ℃ ($GeO_2+Ge \rightarrow GeO_{(g)}$). Moreover, the Fig. 5-11(b) shows that atom % of GeO_X with N_2/H_2O-RTA further decrease by elevating temperature at 500 ℃. The experimental results indicate that adding H_2O vapor in RTA treatment effectively suppresses the formation of

GeO_X interlayer.

The XPS spectra of Zr $3p_{3/2}$ and Ge $2p_{3/2}$ signals were carefully analyzed in Fig. 5-12 to explore further the reaction between ZrO_2 and GeO_x films during N_2 and N_2/H_2O-RTA at 300 ℃ and 500 ℃. The Zr $3p_{3/2}$ signal at a binding energy of around 333.2 eV is associated with ZrO_2. The Fig. 5-12(a) shows that the peak values of the Zr $3p_{3/2}$ signal from N_2/H_2O RTA-treated samples are shifted to a higher binding energy as the ion sputtering time increases, whereas the shifts in the peak of the standard and N_2 RTA-treated samples are negligible. The results are similar previous findings in Section 4.4. The high binding energy shift of Zr $3p_{3/2}$ signal indicates that zirconia is further oxidized upon N_2/H_2O-RTA. Notably, oxidation is also favored at the interface between ZrO_2 and Ge. In Fig. 5-12(b), the Ge $2p_{3/2}$ signals at binding energies of around 1217.26 eV and 1219.5 eV are associated with non-oxidized Ge and GeO_X, respectively. The interfacial Ge oxide layers of the standard and N_2-RTA samples are mostly GeO_X, are suppressed with adding H_2O ambience. The results are consistent with Figs. 5-1, 5-10 and 5-11. Restated, the interfacial GeO_X layer is formed during RTA process and is suppressed by adding H_2O ambience with Zr oxidation.

Since suppression of GeO_X formation by N_2/H_2O RTA treatment was enhanced with elevating RTA temperature, the C-V characteristics of ZrO_2/Ge capacitor with RTA treatment were therefore examined in N_2 and N_2/H_2O at 500 ℃, as shown in Figs. 5-13, 5-14 and 5.15. The C-V curves show that CET of N_2-RTA and N_2/H_2O-RTA treated samples decrease from

4.3 nm to 3.1 nm and from 2.6 nm to 2.2 nm, respectively. Moreover, the CET of N_2/H_2O-RTA is smaller than N_2-RTA. According to the results in Figs. 5-12 and 5-13, the GeO_X interlayer thermally decomposes when temperature reaching at 500 ℃ and CET with N_2/H_2O-RTA further decreases owing to H_2O additive. However, the high annealing temperature worsens transition of C-V characteristic in Fig. 5-13. It could be attributed to formation of poor interface upon Ge substrate by aggressive thermal decomposition of germanium oxide and germanium at 500 ℃.

The cross-sectional HRTEM images of ZrO_2 on Ge substrate with RTA in N_2/H_2O and H_2 ambiences at 500 ℃ for 3 min are shown in Figs. 5-16 and 5-17, respectively. Figure 5-16 (a) shows that the deposited ZrO_2 on Ge substrate without RTA treatment has 7.9-nm thin layer on Ge substrate. Upper thin layer exhibits crystalline structure and is considered as ZrO_2. The middle amorphous layer is regarded as GeO_X. However, the interface of ZrO_2 and GeO_X can't be clearly discriminated duo to intermixing with each other. After N_2/H_2O RTA at 500 ℃, the total thickness of thin layer upon Ge substrate decrease from 7.9 nm to 6.2 nm, as shown in Fig. 5-16 (b). The evidence of thickness reduction is attributed to suppression GeO_X formation by adding H_2O. The deposited ZrO_2 on Ge substrate with RTA was also examined in H_2 ambience, as shown in Fig. 5-17. The different amplification of cross-sectional images show that uneven surface and voids have been observed between ZrO_2 and Ge substrate after H_2-RTA treatment. It is noted that the thickness of ZrO_2 was further decreased to 2.5 nm with

vanishing of GeO_X.

According to previous observations of XPS analysis and HRTEM images for RTA treatment in N_2, N_2/H_2O and H_2 ambience, those evidences demonstrate that oxidation and reduction reactions occur at the interface between ZrO_2 and GeO_X by adding H_2O or H_2 ambience. The oxidation-reduction reaction are recalled as following,

$$Zr+2H_2O \rightarrow ZrO_2+2H_2 \quad (1)$$

$$GeO+H_2 \rightarrow Ge+H_2O \quad (2)$$

It reasonably explains that CET decreases and gate leakage current reduces with adding H_2O or H_2 ambiences due to suppression of GeO_X during RTA. Comparing to H_2O, directly adding H_2 ambience at 300 ℃ have superior suppression of GeO_X formation exhibited in smaller CET and lower gate leakage current. When the temperature of RTA treatment reaches at 500 ℃, the aggressive oxidation-reduction reaction in H_2 ambience cloud cause uneven surface and voids at the interface between ZrO_2 and Ge substrate. At 500 ℃, the oxygen could actively react with Ge substrate to form GeO_X. The capability reduction of GeO_X by H_2 is simultaneously booted at high temperature. Cycles of oxidation and reduction result in voids formation. However, since the concentration of H_2 has not been optimized, the degradation of surface morphology could be avoid with diminishing H_2 content.

5.4 Summaries

The rapid thermal annealing of sputtered ZrO_2 on Ge substrate was investigated in N_2,

N_2/H_2O and H_2 ambiences. The capacitor for sputtered ZrO_2 on Ge substrate without thermal treatment has larger hysteresis due to defective transition interlayer. While appropriate thermal annealing eliminates the hysteresis, the ZrO_2/Ge capacitor has GeO_X interlayer resulting in thicker CET and gate leakage current degradation. Adding H_2O or H_2 in RTA process effectively suppress GeO_X formation and release degradation of gate leakage current. Experimental results show that suppression of GeO_X is owing to oxidation and reduction reactions occur at the interface between ZrO_2 and GeO_X by adding H_2O or H_2 ambience. Compare to N_2/H_2O additive, directly adding H_2 ambience at 300 ℃ have superior suppression of GeO_X formation resulting in smaller CET and lower gate leakage current. However, when the temperature of RTA treatment reaches at 500 ℃, the aggressive oxidation-reduction reaction in H_2 ambience cloud cause uneven surface and voids at the interface between ZrO_2 and Ge substrate. Therefore, reduction of GeO_X is need carefully controlled.

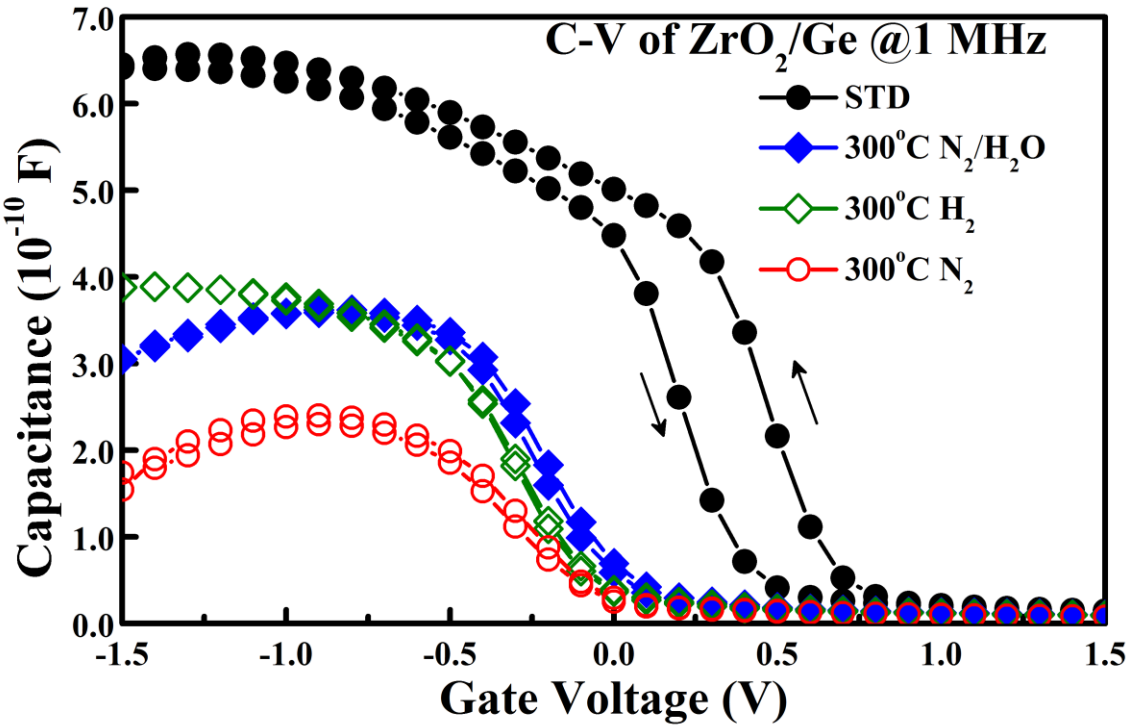

Figure 5-1 The C-V characteristics of ZrO_2 on Ge substrate with RTA in various ambiences.

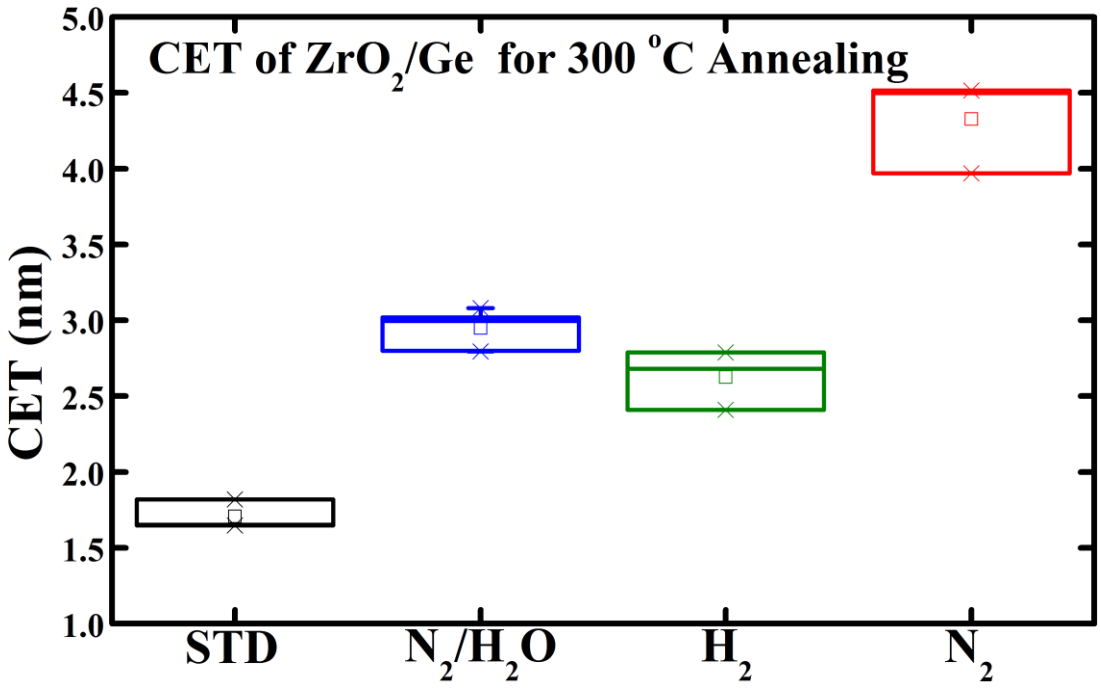

Figure 5-2 Summary of capacitance-equivalent thickness (CET) of ZrO_2/Ge capacitor with RTA in various ambiences.

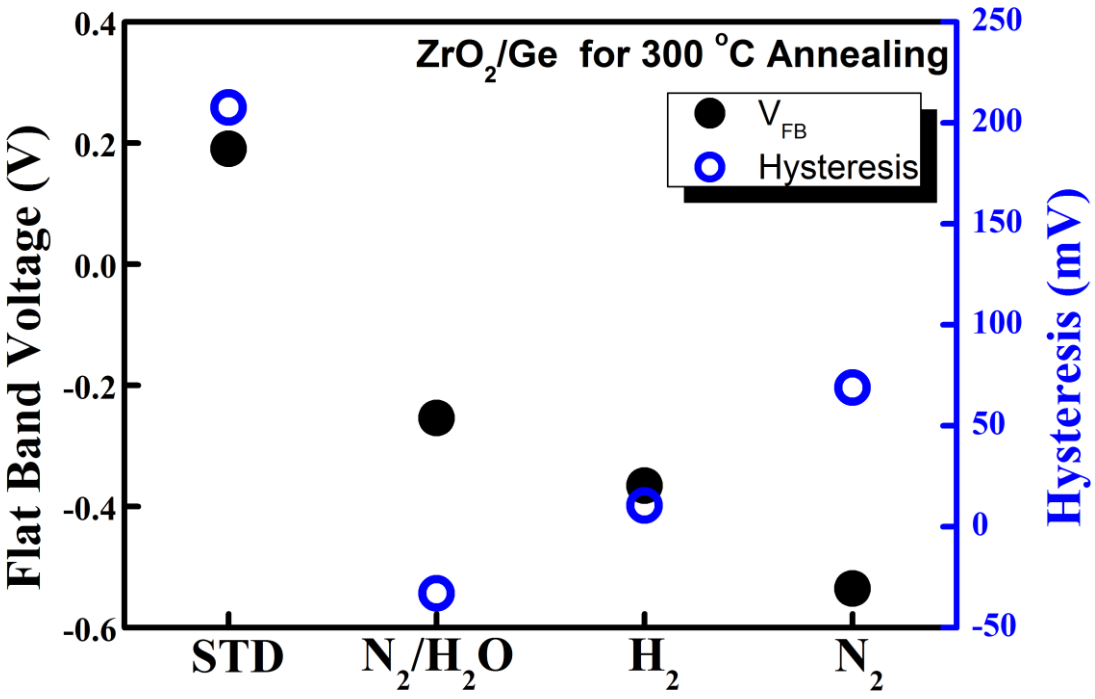

Figure 5-3 Summary of flat band voltage and hysteresis of ZrO_2/Ge capacitor with RTA in various ambiences.

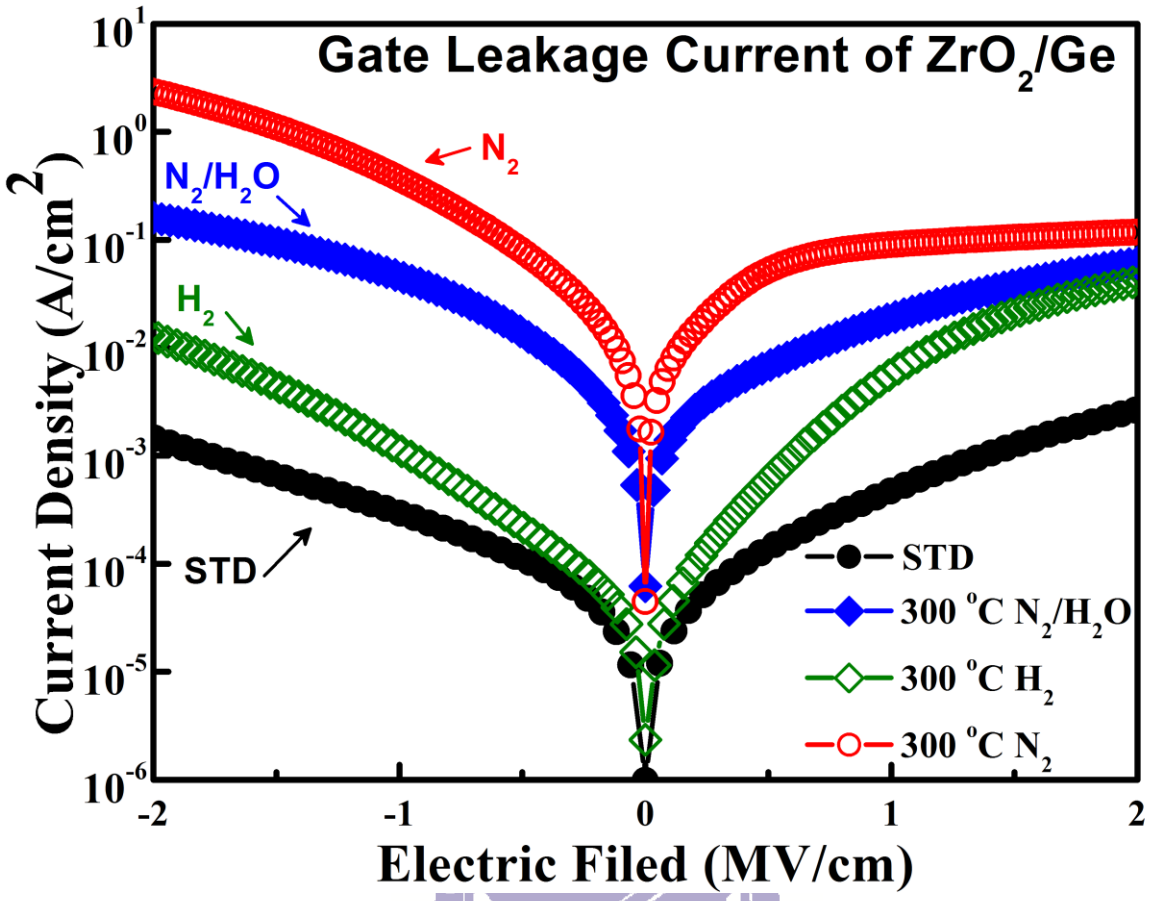

Figure 5-4 The gate leakage current of ZrO_2 on Ge substrate with RTA in various ambiences.

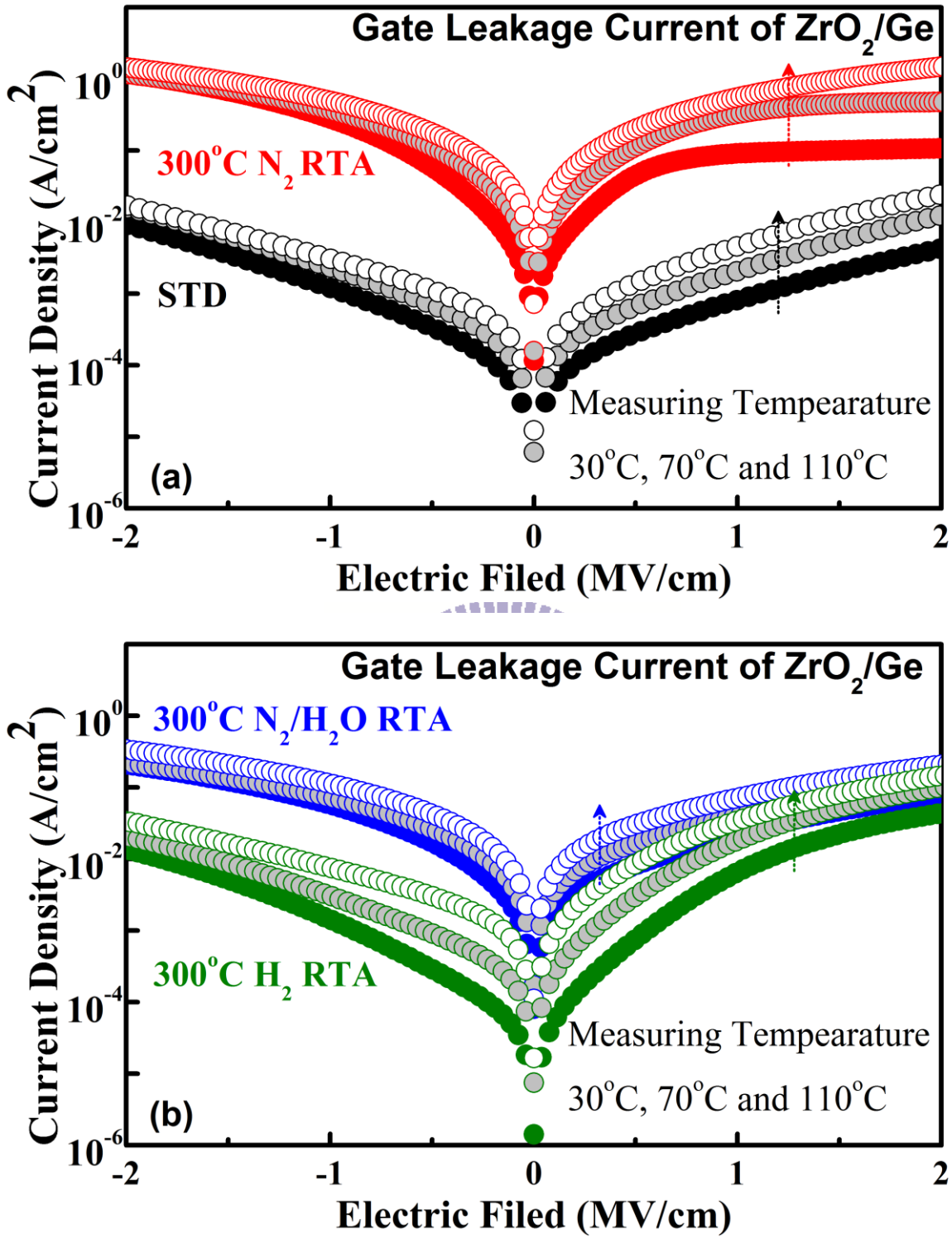

Figure 5-5 The gate leakage current of ZrO_2 on Ge substrate with various measuring temperature for (a) standard and N_2-RTA, and (b) N_2/H_2O and H_2 RTA.

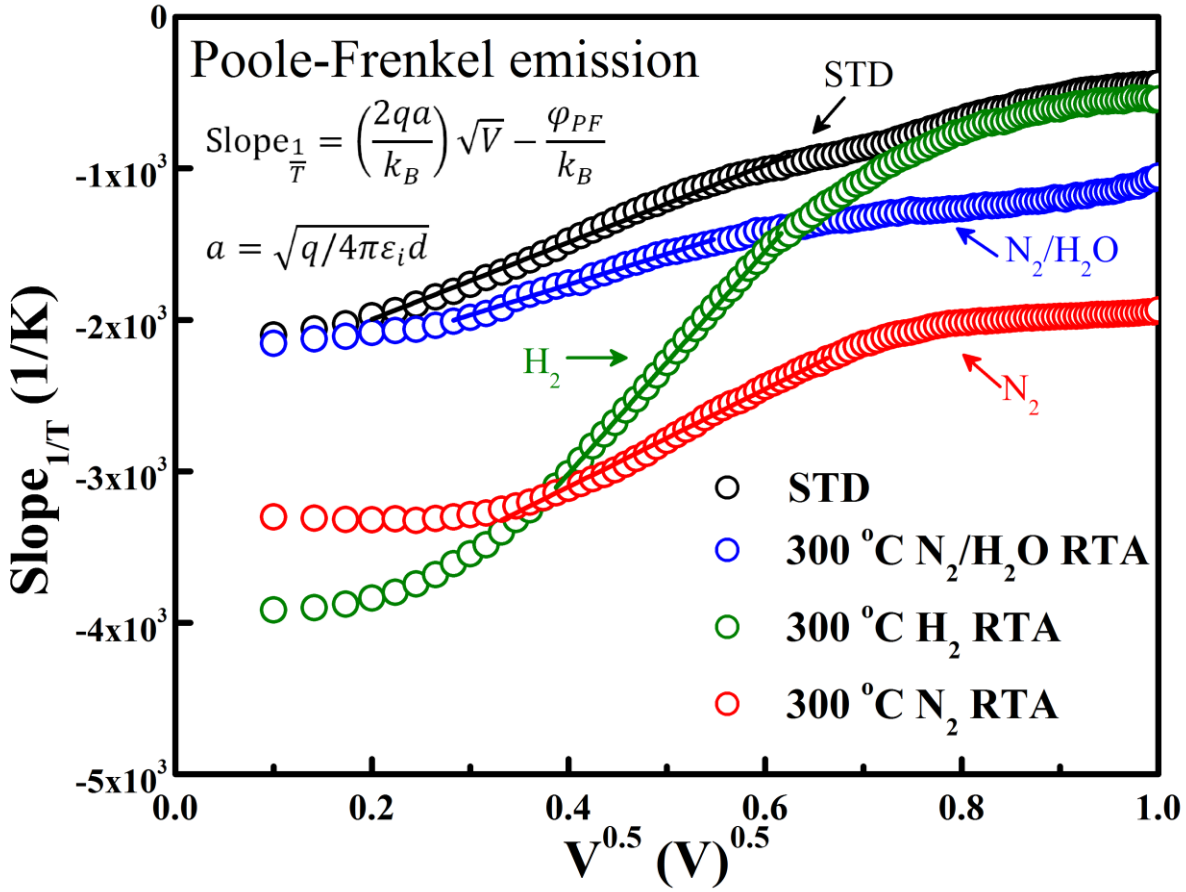

Figure 5-6 The plot of Poole-Frenkel emission fitting with RTA in various ambiences.

	Intercept	Slope	Tox (nm)	ε	ϕ_{PF}
STD	-2504.77	2543.75	7.90	15.17	0.22
N_2/H_2O	-2570.70	2011.05	7.90	24.28	X
H_2	-5943.91	7325.06	7.90	1.83	X
N_2	-4394.43	3228.29	7.90	9.42	X

Table 5-1 Summaries of Poole-Frenkel emission fitting.

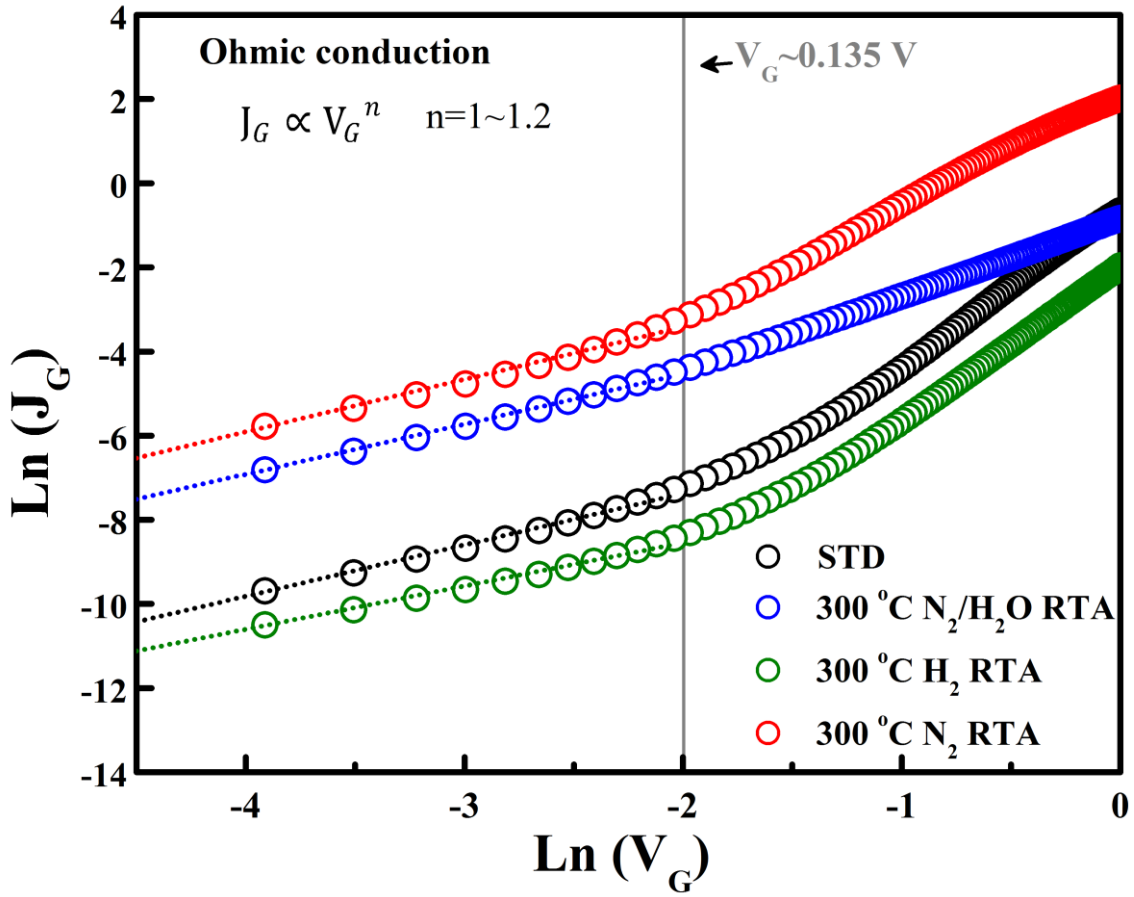

Figure 5-7 The plot of ohmic emission fitting with RTA in various ambiences.

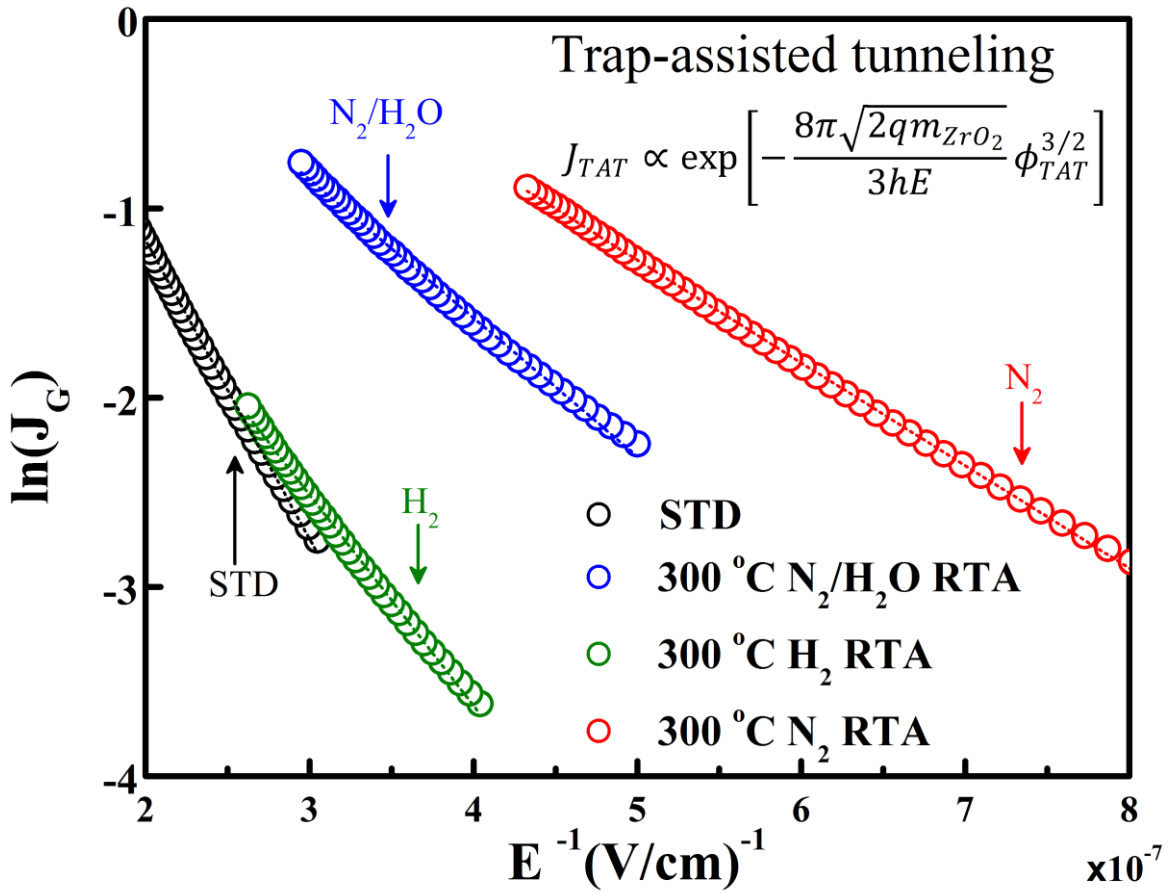

Figure 5-8 The plot of TAT fitting with RTA in various ambiences.

	Slope	m^*/m_0	ϕ_{TAT} (eV)
STD	-1.6E+07	0.25	0.60
N_2/H_2O	-7.3E+06	0.25	0.36
H_2	-1.1E+07	0.25	0.47
N_2	-5.4E+06	0.25	0.29

Table 5-2 Summaries of TAT fitting.

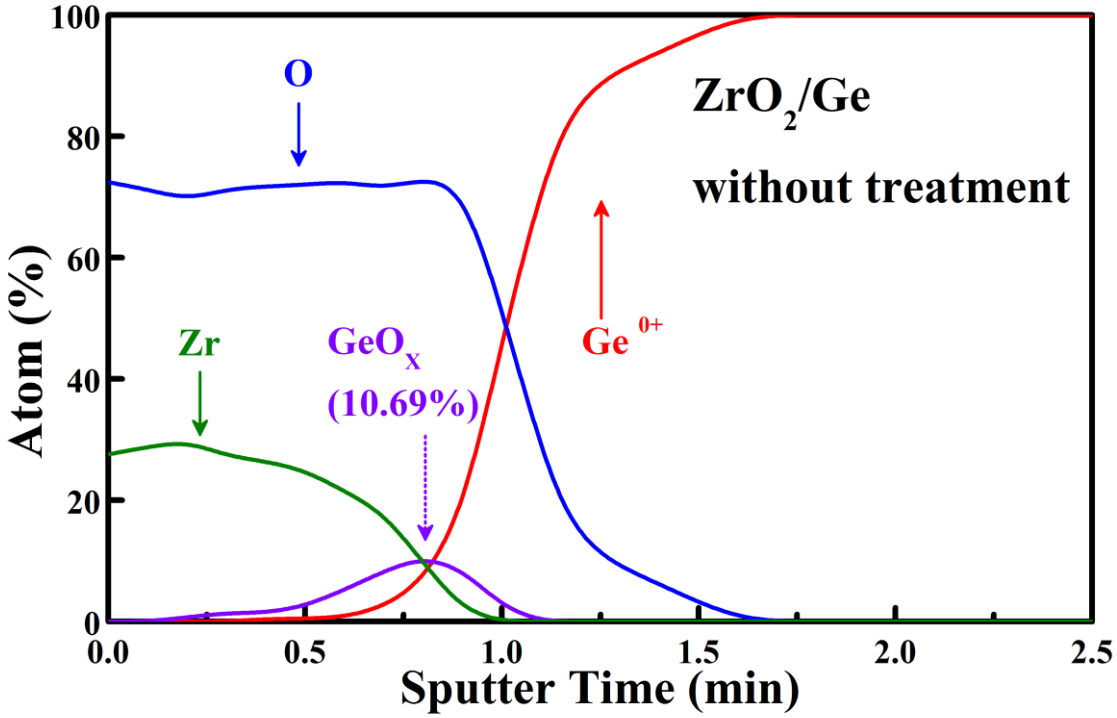

Figure 5-9 The composition-depth profiling analysis of XPS for ZrO_2 on Ge substrate.

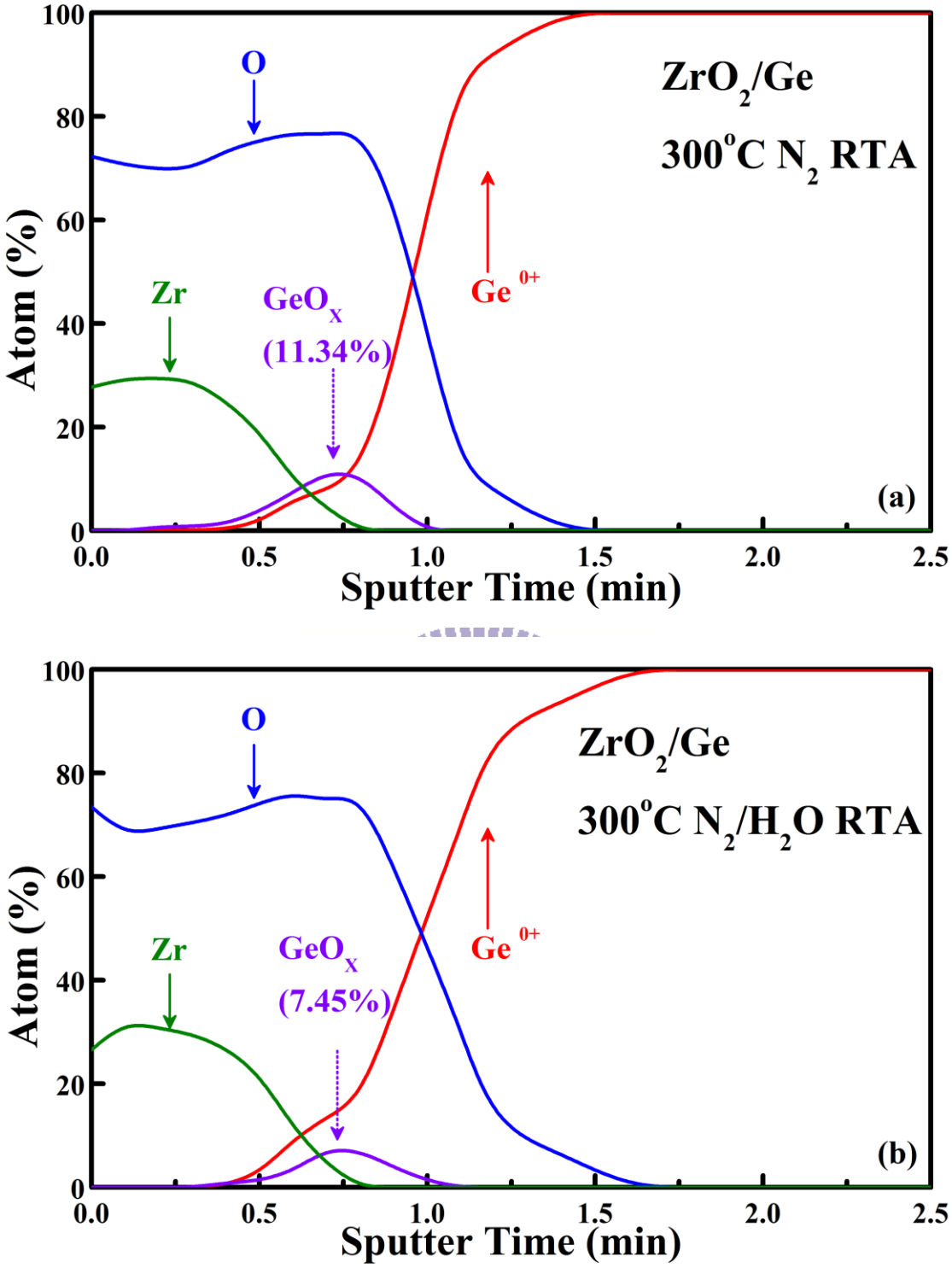

Figure 5-10 The composition-depth profiling analysis of XPS for ZrO_2 on Ge substrate with (a) N_2-RTA and (b) N_2/H_2O-RTA at 300 °C.

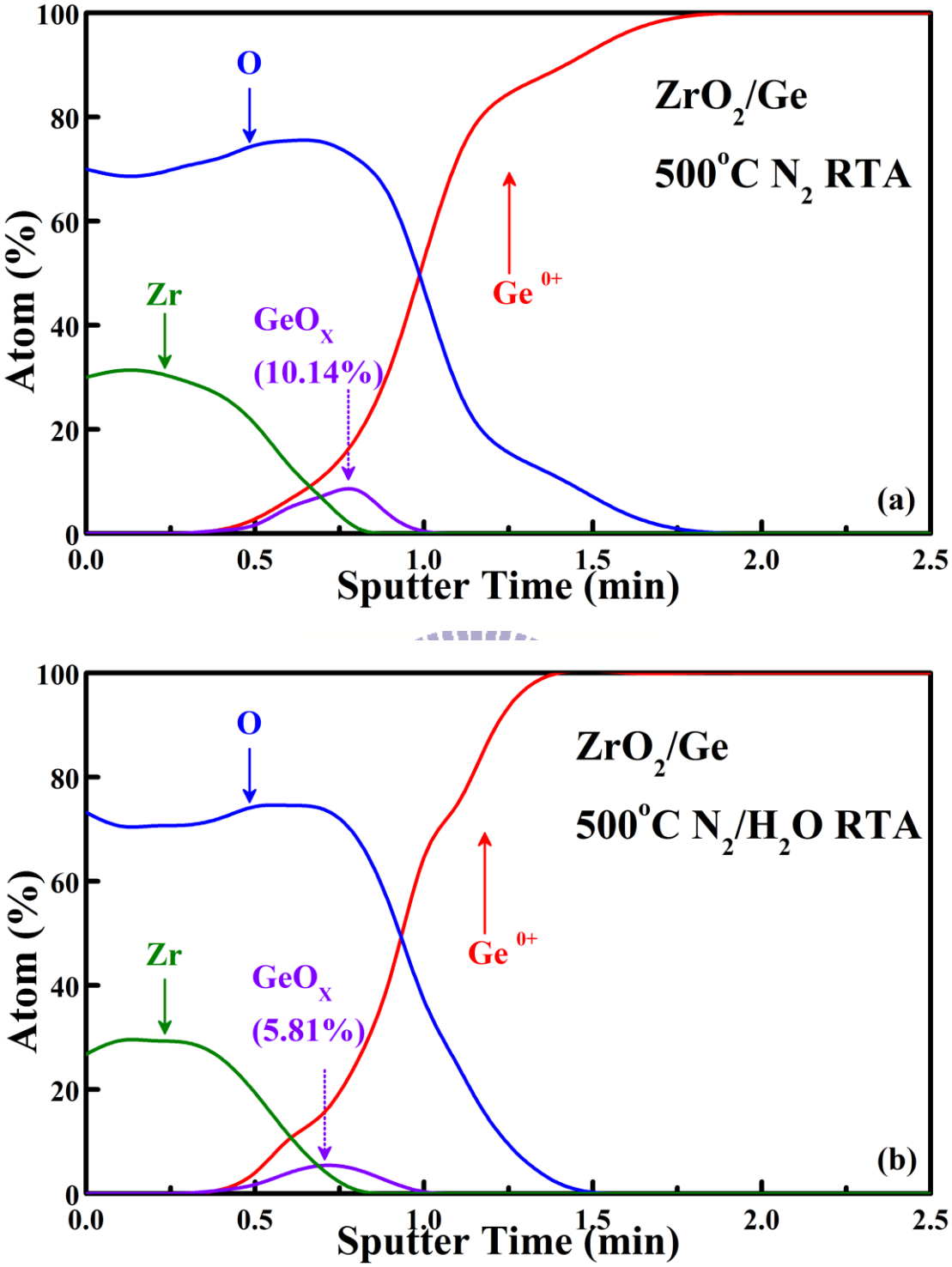

Figure 5-11 The composition-depth profiling analysis of XPS for ZrO_2 on Ge substrate with (a) N_2-RTA and (b) N_2/H_2O-RTA at 500 °C.

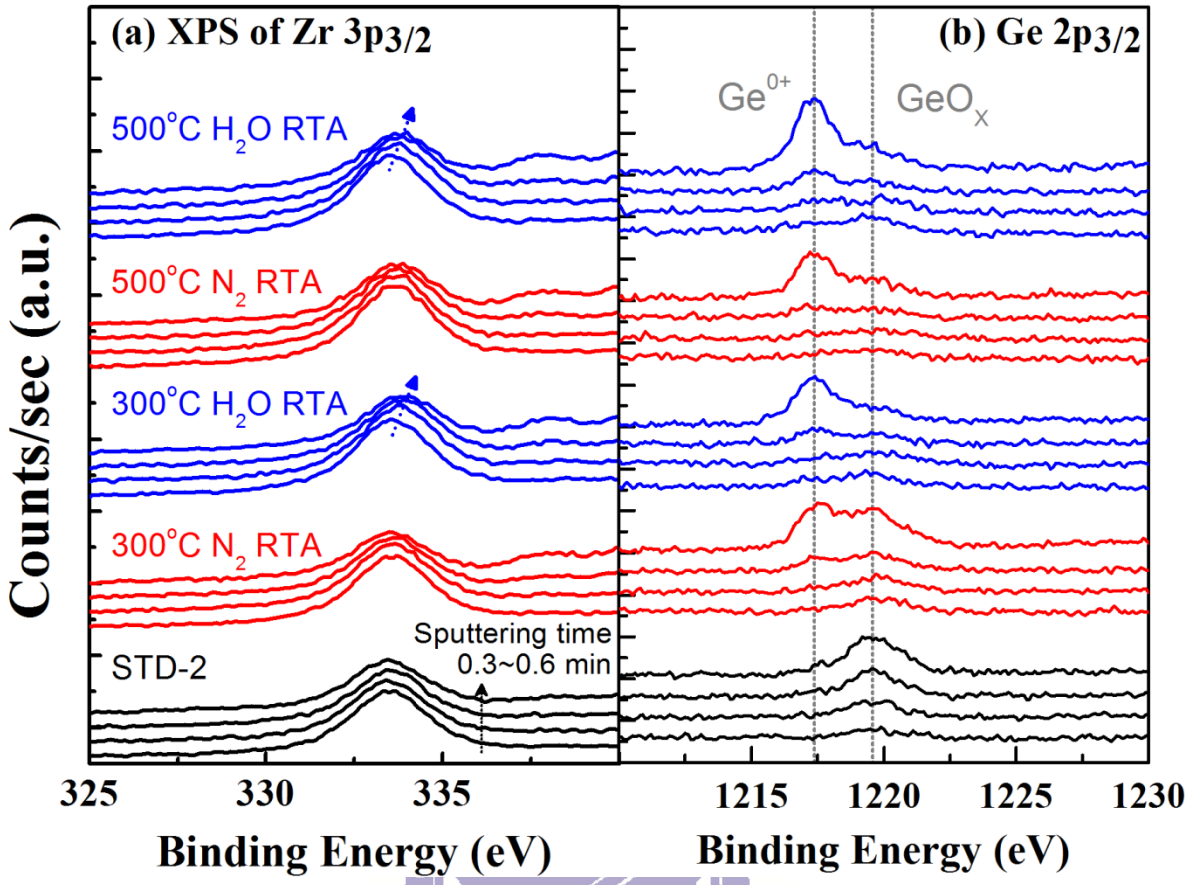

Figure 5-12 XPS spectra of (a) Zr $3p_{3/2}$ and (b) Ge $2p_{3/2}$ signals with various treatments.

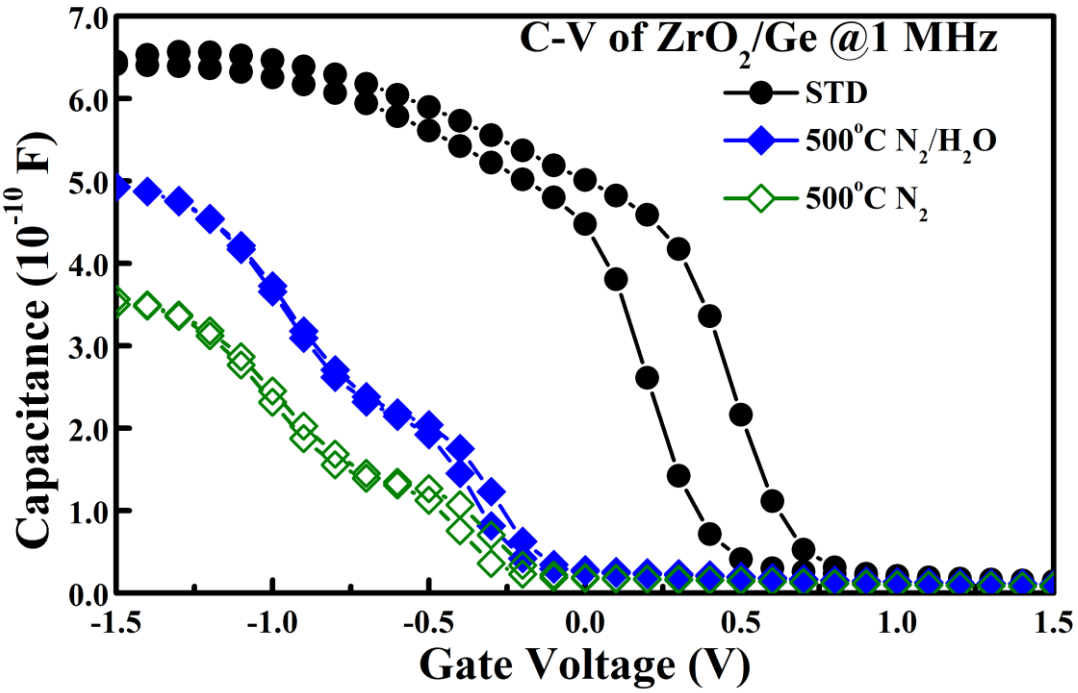

Figure 5-13 The C-V characteristic of ZrO_2/Ge capacitor with RTA treatment in N_2 and N_2/H_2O at 500 °C.

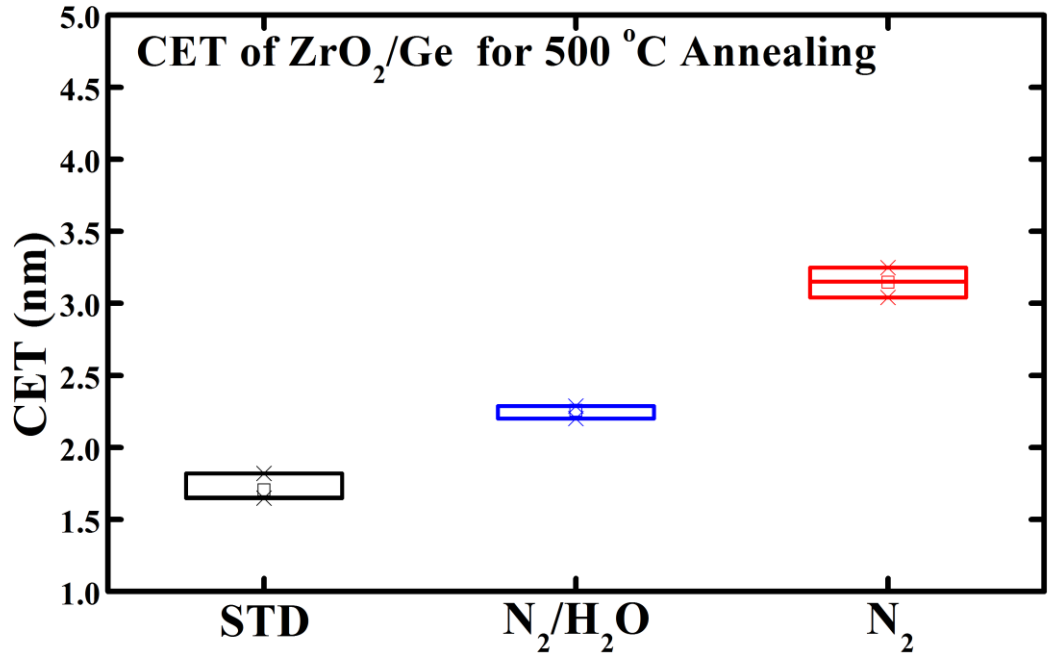

Figure 5-14 Summary of capacitance-equivalent thickness (CET) of ZrO_2/Ge capacitor with RTA at 500 °C.

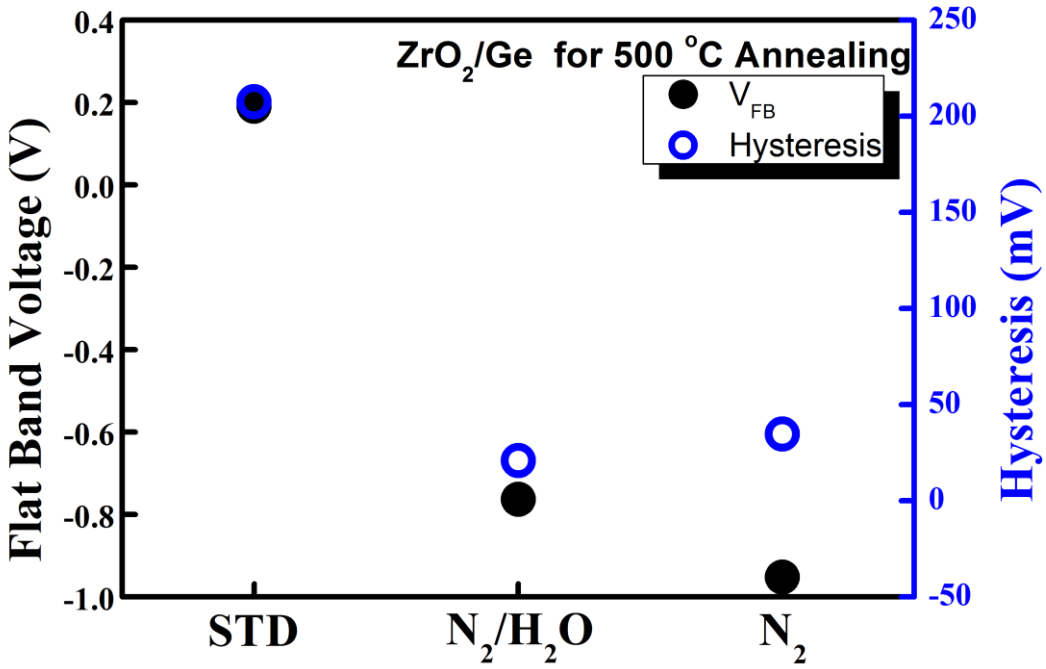

Figure 5-15 Summary of flat band voltage and hysteresis of ZrO_2/Ge capacitor with RTA in various ambiences in N_2 and N_2/H_2O at 500 ℃.

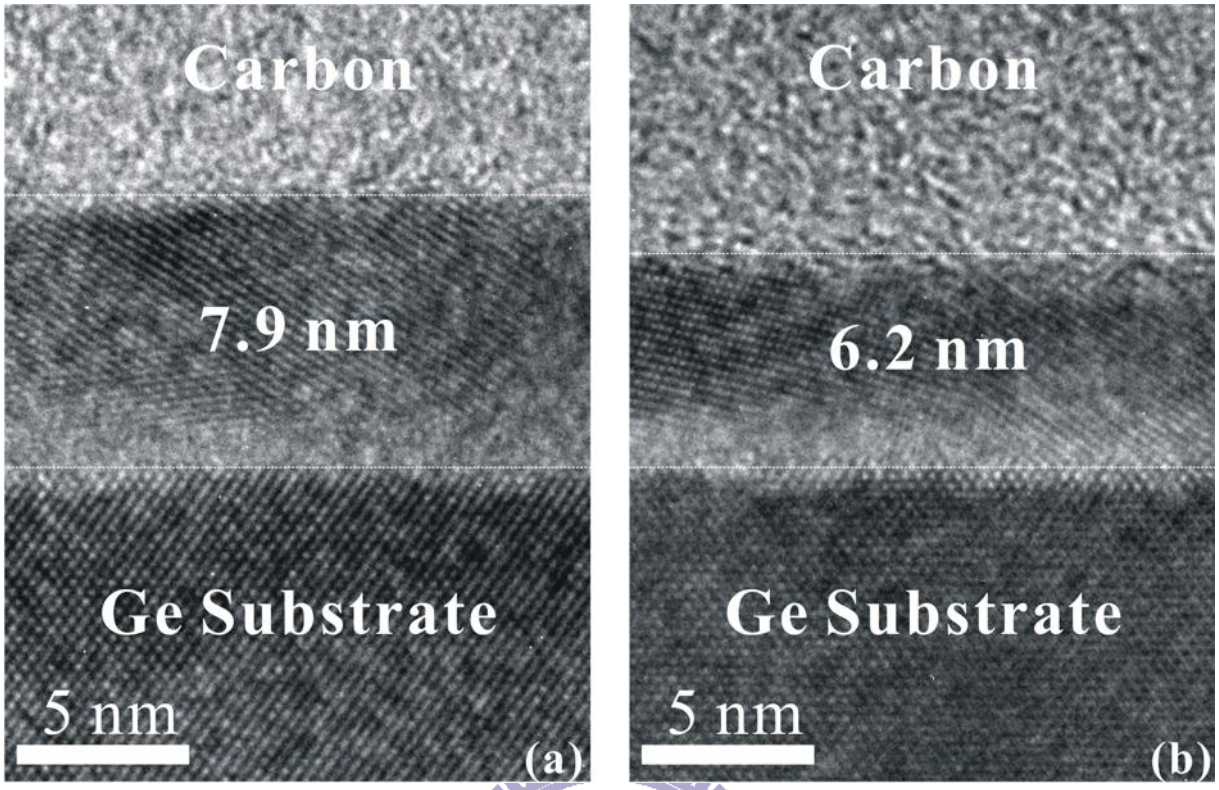

Figure 5-16 The cross-sectional of HRTEM images of ZrO_2 on Ge substrate (a) before and (a) after N_2/H_2O-RTA at 500 °C for 3 min.

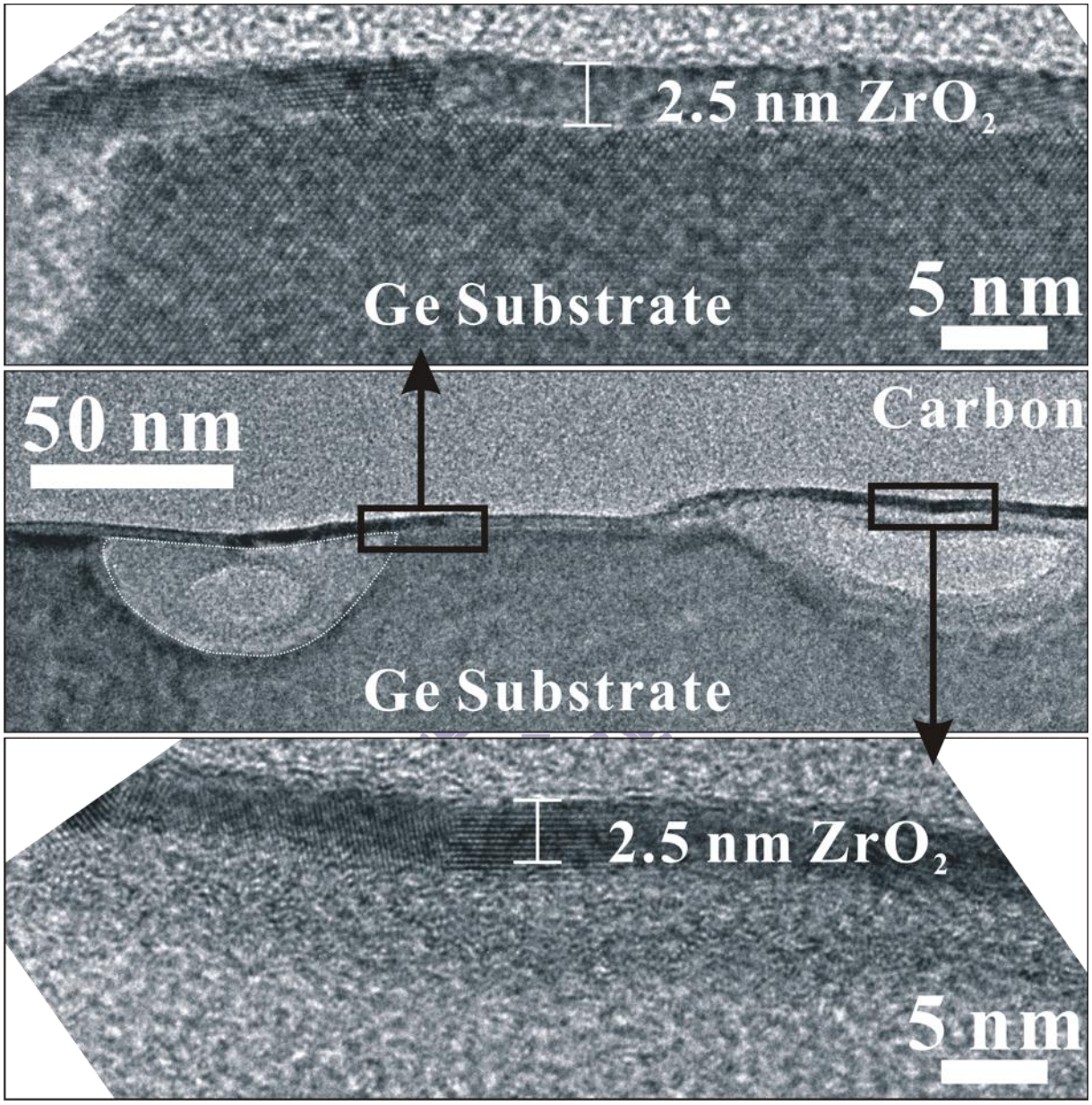

Figure 5-17 The cross-sectional HRTEM images of ZrO_2 on Ge substrate with RTA treatment in H_2 ambience at 500 °C.

Chapter 6

Summaries and Future Work

6.1 Summaries

First, the impacts of nitrogen profile and SMT on ultrathin SiON for 45-nm Si-based MOSFETs application are investigated in Chapter 3. For the investigation of nitrogen profile, we have proposed a model based on WKB that could well explain the gate tunneling-current through thin SiON with different nitrogen profile. The change in nitrogen profile influences the band shape of SiON, causing the change in tunneling probability. The SiON film with steeper nitrogen profile will exhibit a higher gate tunneling-current. Also, the phenomenon is more apparent in pMOSFET than in nMOSFET. The higher sensitivity of VB bending towards N-profile change explains why pMOSFET is showing a larger current increment than nMOSFET.

In the other way, experimental results also show that SMT boosts the electrical performance of nMOSFET, but the gain was achieved at the expense of a higher off-state gate tunneling current. Carrier separation measurement shows the increased gate tunneling current is originated from the higher gate-to-S/D tunneling current, which worsens when channel length gets shorter. Excessive strain degrades gate tunneling current via two approaches: (1) excessive LDD dopant diffusion and (2) gate edge damage. This was verified from the higher gate-to-S/D overlapping capacitance and the hot carrier stress study.

In the Chapter 4, a high-pressure H_2O treatment at low temperature (100~150 ℃) has been proposed to treat Ge MOS devices. The high-pressure H_2O treatment on Ge MOS devices is investigated step-by-step to discriminate the influence on individual layer in Ge MOS capacitor. The high-pressure H_2O treatment was respectively performed on SiO_2/Ge for exploration of Ge substrate, on ZrO_2/Si for exploration of ZrO_2 thin film and finally realized on ZrO_2/Ge capacitors.

For SiO_2/epi-Ge capacitors, it is observed that the uneven and poor interface was easily formed during thermal deposition processes on epi-Ge layer. After the high-pressure H_2O treatment, a smooth GeO_2 interface layer is formed and the frequency dispersion of inversion capacitance is alleviated. Furthermore, electrical degradation of Ge-MOS device after 450℃ PDA process leads to the reduction of accumulation capacitance and the increase of gate leakage current. The high-pressure H_2O treatment also can transport the oxidant into the gate dielectric layer and passivate the Ge-related defect states generated by PDA process. Electrical characteristics of Ge-MOS device are effectively recovered to an extent similar to the one before PDA process.

Then, high-pressure H_2O treatment for ZrO_2 dielectric layer was performed on Si substrate to prevent interruption of Ge. After thermal annealing, the J_G of ZrO_2 dielectric changes slightly until temperature at 400 ℃. However, the dramatic increment of J_G is observed in the 500 ℃ RTA-treated sample. The increase of J_G for ZrO_2 dielectrics is

attributed to defective grain boundaries induced by thermal crystallization. Moreover, increase of J_G also worsens the charge holding capability of ZrO_2 layer and results in increment of CET. After high-pressure H_2O treatment, the hysteresis behavior vanishes and CET reduces in ZrO_2/Si capacitor. It is inferred that the high-pressure H_2O treatment passivates the border traps in ZrO_2 nearby Si substrate and defective grain boundary regions in the bulk of ZrO_2.

The high-pressure H_2O treatment was finally realized on the sputter-deposition of ZrO_2 upon Ge substrate. The H_2O oxidant is carried into the ZrO_2 thin film by supercritical CO_2 fluid in which H_2O oxidant is dissolved. According to the composition-depth profiles from the analyses of XPS and HRTEM images, a GeO_X layer is formed at the interface between ZrO_2 and Ge during deposition and thermal cycles, and eliminated by high-pressure H_2O treatment. The analysis of XPS spectra reveals that the H_2O oxidant reacts with non-oxidized Zr film close to the GeO_X interlayer and produced H_2 further reduces GeO_X. Additionally, the elimination of GeO_X helps to reduce the gate leakage current.

According to the observations of high-pressure H_2O treatment on Ge MOS device, the effects of H_2O and H_2 were further explored in Chapter 5. The rapid thermal annealing of sputtered ZrO_2 on Ge substrate was investigated in N_2, N_2/H_2O and H_2 ambiences. The capacitor for sputtered ZrO_2 on Ge substrate without thermal treatment has larger hysteresis due to defective transition interlayer. While appropriate thermal annealing eliminates the

hysteresis, the ZrO_2/Ge capacitor has GeO_X interlayer resulting in thicker CET and gate leakage current degradation. Adding H_2O or H_2 in RTA process effectively suppress GeO_X formation and release degradation of gate leakage current. Experimental results show that suppression of GeO_X is owing to oxidation and reduction reactions occur at the interface between ZrO_2 and GeO_X by adding H_2O or H_2 ambience. Compare to N_2/H_2O additive, directly adding H_2 ambience at 300 ℃ have superior suppression of GeO_X formation resulting in smaller CET and lower gate leakage current. However, when the temperature of RTA treatment reaches at 500 ℃, the aggressive oxidation-reduction reaction in H_2 ambience cloud cause uneven surface and voids at the interface between ZrO_2 and Ge substrate. Therefore, reduction of GeO_X is need carefully controlled.

6.2 Future work

According to findings of Chapter 5, the H_2 additive in RTA process effectively suppression the GeO_X formation at 300 ℃, but worsen surface morphology of Ge substrate at 500 ℃. The degradation is attributed to aggressive oxidation-reduction reaction. Therefore, annealing temperature and concentration of H_2 ambience must be optimized to further application. In the other way, the poor GeO_X can be replaced by more stable Ge nitride (Ge_3N_4) as interfacial layer [67, 68]. The H_2 could be added in the nitridation process of Ge surface to prevent GeO_X formation from residue of ambient oxygen and increase nitrogen content in interlayer.

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Appendix

Author has also investigated negative-bias-temperature-instability (NBTI) of pMOSFET for polycrystalline silicon thin-film transistors and silicon-based MOSFETs. For integrity of this thesis, the scopes of NBTI are individually included in Appendix.

A.1 Impact of Negative-Bias-Temperature-Instability on channel bulk of polysilicon TFT by gated PIN diode analysis

Polycrystalline silicon thin-film transistors (poly-Si TFTs) are widely used as switch and driving devices in active matrix liquid crystal displays (AMLCDs) and active matrix organic light-emitting diodes (AMOLEDs). These poly-Si TFTs are suitable for multifunctional displays, because they enable the integration of driver electronics, sensors, memories, and peripheral circuits on glass substrates, to afford system-on-panel (SOP) displays. Complementary poly-Si TFTs operate with high duty cycles in peripheral driving circuit applications, and thus TFTs would suffer long-term negative and positive bias stress, at elevated ambient temperatures. Negative bias temperature instability (NBTI) is a critical reliability issue for metal-oxide-semiconductor field-effect transistors (MOSFETs), with single crystal silicon, also particularly for p-MOSFETs. It was reported that the electrochemical reaction between hydrogenated trivalent Si (Si-H) bonds and accumulated holes, triggers NBTI degradation, causing the formation of interface states and positive fixed charges [69]. Recently, the effects of NBTI on p-channel poly-Si TFTs have attracted much

research interest. One group reported that grain boundaries with many Si-H bonds experience greater NBTI degradation than usual degradation.[4, 70, 71] Both the Levinson and Proano method[70], and charge pumping method [72], provide the estimation of grain boundary traps. The presence of interface states complicates the calculation of grain boundary traps, additionally; the estimation applies only to a channel region just beneath the gate insulator. Thus, it is hard to investigate the grain boundary properties of poly-Si bulk under NBTI stress any further. Gated diodes are generally used to distinguish the interface trap states from bulk trap states in the single-crystal MOSFET technology.[73] However, the gated diodes were little used for the investigation of NBTI effects on the poly-Si. In this work, we used the gated P-intrinsic-N (PIN) diodes to investigate defect formation in the poly-Si bulk under NBTI stress, by analyzing the reverse defect-generation current.

The top gate p-channel poly-Si TFT were fabricated on a Corning 1737 glass substrate. First, the buffer nitride/oxide layer, and then a 50 nm-thick a-Si:H film were deposited by plasma enhanced chemical vapor deposition (PECVD) at 380 ℃. The a-Si:H film was dehydrogenated in a furnace at 450 ℃ for 60 minutes. The dehydrogenated a-Si was sequentially crystallized by XeCl excimer laser irradiation with a wavelength of 308 nm at 350 mJ/cm^2. Microlithography and plasma dry etching processes were used to pattern the active poly-Si region, and then a 100 nm-thick TEOS (Tetra-Ethyl-Ortho-Silicate) base oxide film was formed as a gate insulator layer. It was followed that a layer of Mo thin film was

sputter-deposited and patterned as the gate electrode. The formation of source/drain regions was self-aligned by born implantation process through the metal gate electrode as a mask with a dosage of 8×10^{14} cm^{-2}. Dopant activation was performed by rapid thermal annealing at 580 ℃ for 60 seconds. Hydrogen plasma passivation was carried out in a RF parallel-plate plasma reactor to passivate residual Si dangling bonds at the SiO_2/poly-Si interface, and in the poly-Si grain boundaries. SiO_2/SiN_x films acting as post-metal dielectrics were deposited and etched for contact holes. Mo/Al/Mo metal layers were deposited and patterned to form the source and drain electrodes, and finally complete the p-channel TFT fabrication. The gated PIN diode was also adopted to investigate the NBTI degradation in the poly-Si channel bulk simultaneously. The structure and manufacture processes of the gated PIN diode are similar to the one of the proposed p-channel TFT. However, there are two doping regions in the gated PIN diode, including p-side (p^+ doping with the boron dose of 8×10^{14} cm^{-2}) and n-side regions (n^- doping with the phosphorous dose of 1×1013 cm^{-2} and n^+ doping with a dose of 8×10^{14} cm^{-2}). When the gated PIN device was under NBTI stress, the negative gate bias sweep was applied to the gate electrode of the gated PIN diode, 0 V on the p-side region, and n-side floated. The gate bias stressing was relaxed periodically to explore device operation characteristics. The electrical operation conditions for device characterization are schematically shown in Fig. A-1. The reverse generation current of the gated PIN diode was determined at V_P = -2.5 V, with n-side grounded and gate bias sweeping.

Figure A-2 shows transfer characteristics of p-channel poly-Si TFT after periodic NBTI stress. The NBTI degradation of single crystal MOSFETs was reported to be related with the electrochemical reaction between Si-H bonds near the Si/SiO2 interface, and the accumulated hole-carriers at the surface. This led to the generation of Si dangling bonds at the interface and fixed oxide charges. The similar NBTI degradation results also occurred in the poly-Si TFT, namely a negative threshold voltage shift and the elevated sub-threshold swing. Especially, the effects of NBTI on the poly-Si TFT device are expected to be even significant, due to a great deal of Si-H bonds at the grain boundaries of poly-Si film.[70] Trap states at the surface and in the bulk of poly-Si channel are supposed to play critical roles in the increased drain leakage at off state since gate leakage current nearly kept almost intact after NBTI stress, as shown in Fig. A-2.

The gated poly-Si PIN diode was used to explore the properties of poly-Si bulk under NBTI stress, and schematically illustrated in Fig. A-3. The diode was kept in the reversed state with -2.5 V applied to the p-side, and gate bias was swept from the negative to the positive voltages. The reverse current arises from the generation of electron-hole pairs in defect trap centers, and relates to depleted interface states and bulk states. The diode reverse current is given by [28]

$$I_R = I_S + I_{ge} = I_S + (I_{Bulk} + I_{Int}) \quad \text{(A-1)}$$

$$I_{ge} \approx \frac{qn_i}{\tau_g} \times v = \frac{\sigma_n \sigma_p v_{th} N_{eff}}{\sigma_n + \sigma_p} \times qn_i v \propto N_{eff} \quad \text{(A-2)}$$

where I_R, I_S, I_{ge}, I_{Bulk} and I_{Int} are total reverse diode current, diode saturation current, total generation current, bulk generation current, and interface generation current, respectively. The τ_g, n_i, v, σ, v_{th}, and N_{eff} are the carrier generation lifetime, intrinsic carrier concentration, volume of depletion regime, cross-section area, thermal velocity, and effective defect concentration, respectively. The generation current is proportional to the effective defect concentration. When a conductive channel layer of electron or hole is formed, as shown in Figs. A-3(a) and A-3(c), thermal emission of charges generated from interface trap states is effectively suppressed, since large amount of electrons or holes occupy most interface traps [74]. In this case, the I_{Bulk} of poly-Si dominates the reverse current. On the contrary, charge emission from the interface traps occurs, and I_{Int} contributes to the reverse current, while the channel surface is at the depletion state under the operation condition of $V_P < V_G < 0$, as shown in Figs. A-3(b) and A-3(d). In addition, a dramatic increase of leakage current is observed at the high gate bias shown in Fig. A-3(d). It can be attributed to the carrier transportation at poly-Si grain boundaries near n-side or p-side depletion region by trap-assisted tunneling (TAT) mechanism. This is also expressed as followed, [75]

$$I_{TAT} \propto N_{eff} \times e^{-\alpha/\sqrt{|V_P \times (V_G - V_{TH})|}} \quad \text{(A-3)}$$

where V_{TH} is the threshold voltage for the formation of electron or hole channel, and α is a constant.

Figure A-4 shows electrical characteristics of the gated PIN diode under NBTI stress. It

is noted that the reverse current is elevated, due to defect creation at the interface and in the poly-Si bulk. The negative curve shift corresponds to the formation of positive fixed charges in the gate dielectric layer during the NBTI stress process. Additionally, the curve distortion at $V_G < V_P$ in Fig. A-4, can be attributed to the spatial distribution of bulk trap states. The asymmetric TAT current arises from the asymmetric structure of n/p-side regions. The n-side has a n- doping region and reduces the lateral electric field across the hole channel to the n-layer under negative bias. However, it does not influence our estimation of IInt and IBulk.

Figure A-4(b) shows the progression of NBTI over time durations. The power-law time (tn) dependence of VTH and IInt are consistent with a reaction-diffusion mode.[76] Additionally, the similar power-law time dependence of I_{Bulk} is observed in Fig. 4(b). Therefore, we consider that the creation of bulk defects shares the same cause as the interface defect creation by NBTI process. It has been reported that grain boundaries with enriched Si-H bonds also suffer from NBTI degradation.[4, 70] The evidence of increasing I_{Bulk} produced in this study also have shown that NBTI degradation has a spatial distribution and the Si-H bonds at grain boundaries of the poly-Si bulk interact with hole-carriers.

In summary, we proposed a gated poly-Si PIN diode device to investigate the effects of NBTI on the channel bulk of poly-Si TFTs. The gated diodes at a reversed state with gate bias sweeping can individually detect the evolution of interface states and bulk states in the poly-Si film, during the NBTI degradation process. Experimental results have shown that

interface states and bulk states of the PIN diode share power-law time dependences, and are consistent with a reaction-diffusion model. Additionally, NBTI degradation has a spatial distribution and Si-H bonds at the grain boundaries of the poly-Si bulk interact with hole-carriers.

A.2 Enhanced NBTI degradation by SMT in short-channel pMOSFET

This section reveals that SMT enhances nMOSFET's performance. Nevertheless, the gain will be achieved at the expense of poorer pMOSFET's performance and reliability, particularly when the device dimension is continued being scaled.

Mobility enhancement from the introduction of stressor has received a lot of attention. Stressors can be introduced in two main forms: substrate-strain based or process-induced strain based. The substrate-strain based makes use of material with different lattice spacing, such as SiGe/Si epitaxial stack to generate biaxial strain in the channel. This method introduces a global strain to the substrate. It boosts mobility effectively but at a higher cost [11]. On the other hand, process-induced strain based method provides a lower cost solution. They could appear in the forms of shallow trench isolation (STI), contact etching stop layer (CESL) and stress memorization technique (SMT), which introduce uniaxial strain to boost mobility [14, 77]. Both nMOSFET and pMOSFET have different requirements in strain. nMOSFET performed better under the presence of tensile strain, while pMOSFET performs better under the compressive strain. This article reveals that SMT enhances nMOSFET's

performance. Nevertheless, the gain will be achieved at the expense of poorer pMOSFET's performance and reliability, particularly when the device dimension is continued being scaled.

The MOSFETs used in this work were fabricated using conventional CMOS processes. SMT stack layer was introduced after source/drain implantation and followed by high temperature activation. Process details can be found elsewhere [15]. The impact of SMT process to device performance was examined from device's transfer characteristics. Since NBTI is of growing importance for modern ICs,[78] the impact of SMT on NBTI will be the key focus in this section. Charge pumping measurement will also be performed to substantiate the NBTI results.

Figure A-5(a) shows the linear mode Id-Vg for nMOSFET with and without SMT, at a drain voltage of 0.05V. Figure A-5(b) compares the corresponding mobility, as inferred from $Gm_{max} \times T_{ox}$ parameters. It is evident that the incorporation of SMT boosts the device performance for nMOSFET. The SMT layer introduces an uniaxial tensile strain along the channel direction and enhances electron mobility. Figure A-6(a) shows the linear mode Id-Vg for a pMOSFET with and without SMT, measured at Vd = -0.05V. Similarly, fig. A-6(b) compares the holes mobility from $Gm_{max} \times T_{ox}$ parameters for pMOSFET. Result shows the introduction of SMT degrades pMOSFET performance by lowering holes mobility. In summary, the introduction of SMT produces tensile strain in the direction of channel. This tensile strain boosts electrons mobility but "retards" holes mobility. Figures A-7 and A-8 show

the Id-Vd plots for both nMOSFET and pMOSFET, respectively. Both were plotted to compare the effect of SMT. Device with SMT was found to enhanced Id-Vd performance, valid for both nMOSFET and pMOSFET. This is consistent with the observations in Figs. A-5 and A-6. Again, the different observation could be attributed to the presence of tensile strain, introduced by SMT.

In addition to device performance, the impact of SMT to NBTI was also assessed. The NBTI stressing was performed under a constant negative gate biasing with the source, drain and substrate terminals grounded. Stressing was carried out at elevated temperature of 125^{O}C. Device is considered failed when its Idsat drifts by 10% from its initial value. Figure A-9 shows the NBTI lifetime for various channel lengths. In general, NBTI improves as the channel length shrinks progressively. This trend is valid, independent to whether SMT has been added onto the device. On the other hand, it is observed that for long channel device, SMT has negligible effect onto NBTI lifetime. However, as the channel length shrinks progressively, the impact of SMT onto NBTI lifetime becomes more evident. Device with SMT incorporated exhibits a much worsens NBTI lifetime. NBTI degradation has been correlated to the generation defects at the Si/SiO2 interface during electrical stress. Interface traps could exist in the form of silicon trivalent dangling bonds [78]. The presence of tensile strain, introduced by SMT, could enhance the interfacial hydrogen release to form more interface traps than that without SMT. For long channel device, the difference in strain could

be relatively smaller. As the channel length is being scaled down progressively, the difference in strain will be magnified and reflected as worsens NBTI. To substantiate this model, charge-pumping measurement was performed on these devices.

Figure A-10 shows the charge-pumping current density as a function of base voltage. Initial interface traps density (Dit_0) could be inferred from the maximum Icp, measured on fresh device. Figure A-11 compares the initial interface traps density for pMOSFETs, with and without SMT. Results are plotted for various channel lengths. Dit_0 level decreases with channel length, independent to whether SMT has been incorporated. This is consistent with Fig. 5 data, showing better NBTI performance at shorter channel length. On the other hand, comparing samples with and without SMT, the difference in Dit_0 is found to become larger as channel length shrinks. This verifies our model that the difference in tensile strain will be "felt more strongly" as the channel length shrinks. The key implication of this finding is that SMT incorporation boost nMOSFET's performance but it degrades pMOSFET's performance and NBTI at the same time. Degradation will be further enhanced as the device dimension continues to be down-scaled. So, removing the SMT over pMOSFET could be an option to bypass these issues.

Figure A-12 shows the lifetime of NBTI as a function of gate biasing for pMOSFET with short channel length of 0.06 μm. Devices with SMT device, has their NBTI lifetime deteriorates by 2-3 times. This result shows that if we pay much attention to nMOSFET

performance improvement and ignore the tensile stress impact in pMOSFET, it will not only degrade CMOS performance but also bring on reliability issues.

This article reveals that the SMT process increases the nMOSFET electrical performance (Id-Vg and Id-Vg) but at the expense of device performance and NBTI reliability for pMOSFET. In this study, we also clarified the dependence of NBTI on channel length. The incorporation of SMT causes more severe impact on pMOSFET, particularly when the device is continued becomes smaller.

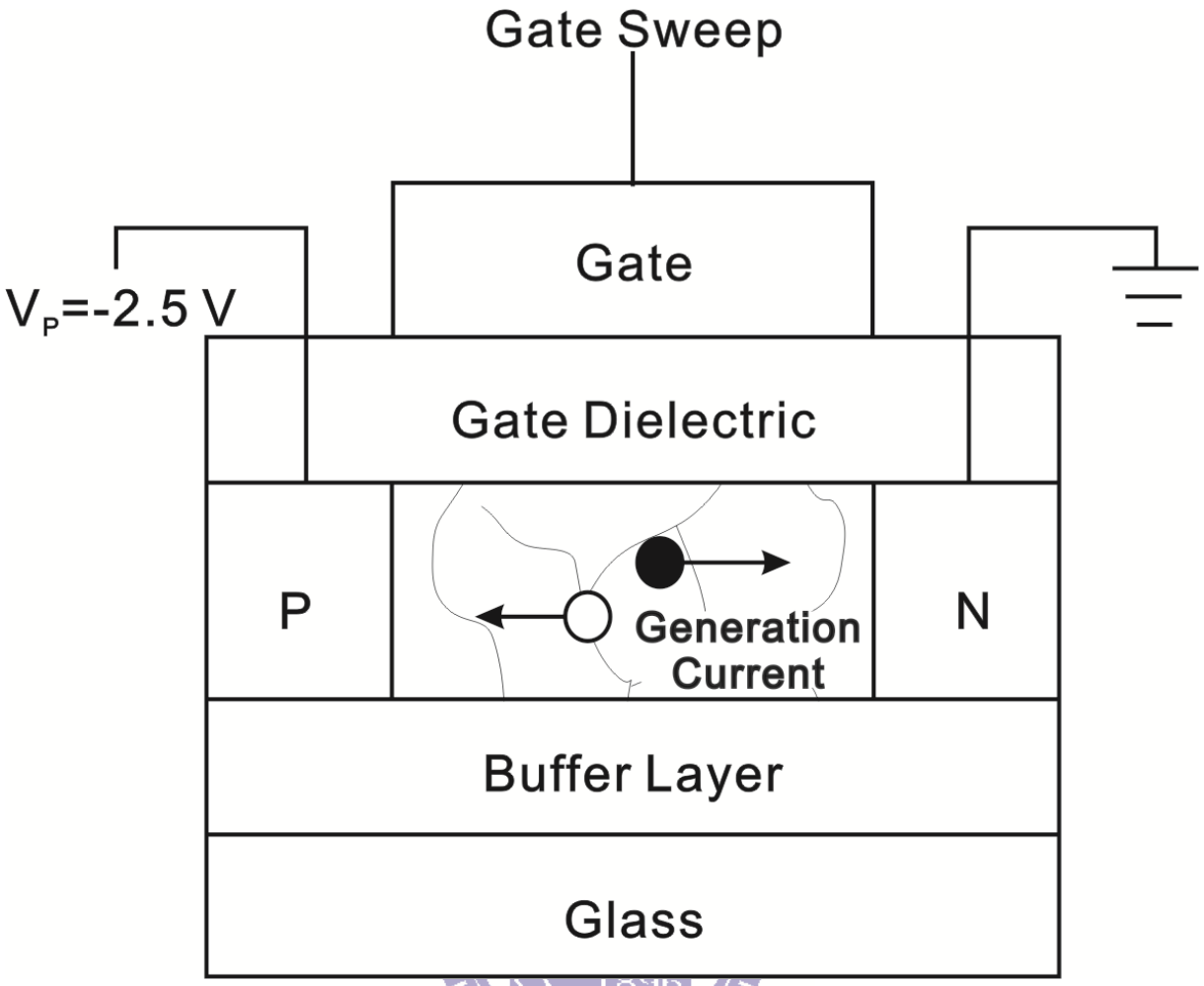

Figure A-1 Schematic cross-sectional views of the proposed gated PIN diode.

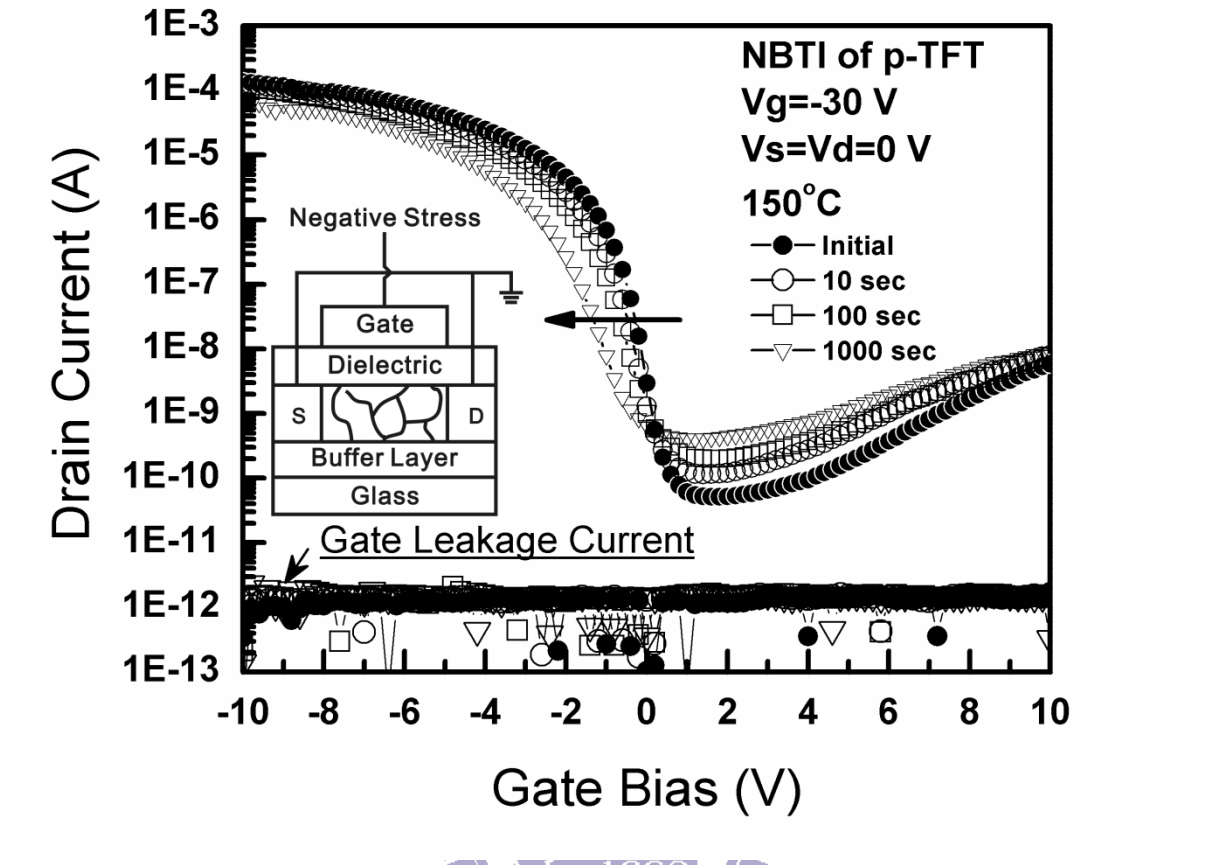

Figure A-2 Transfer characteristics and gate leakage current of p-channel poly-Si TFT after NBTI stress for different time durations.

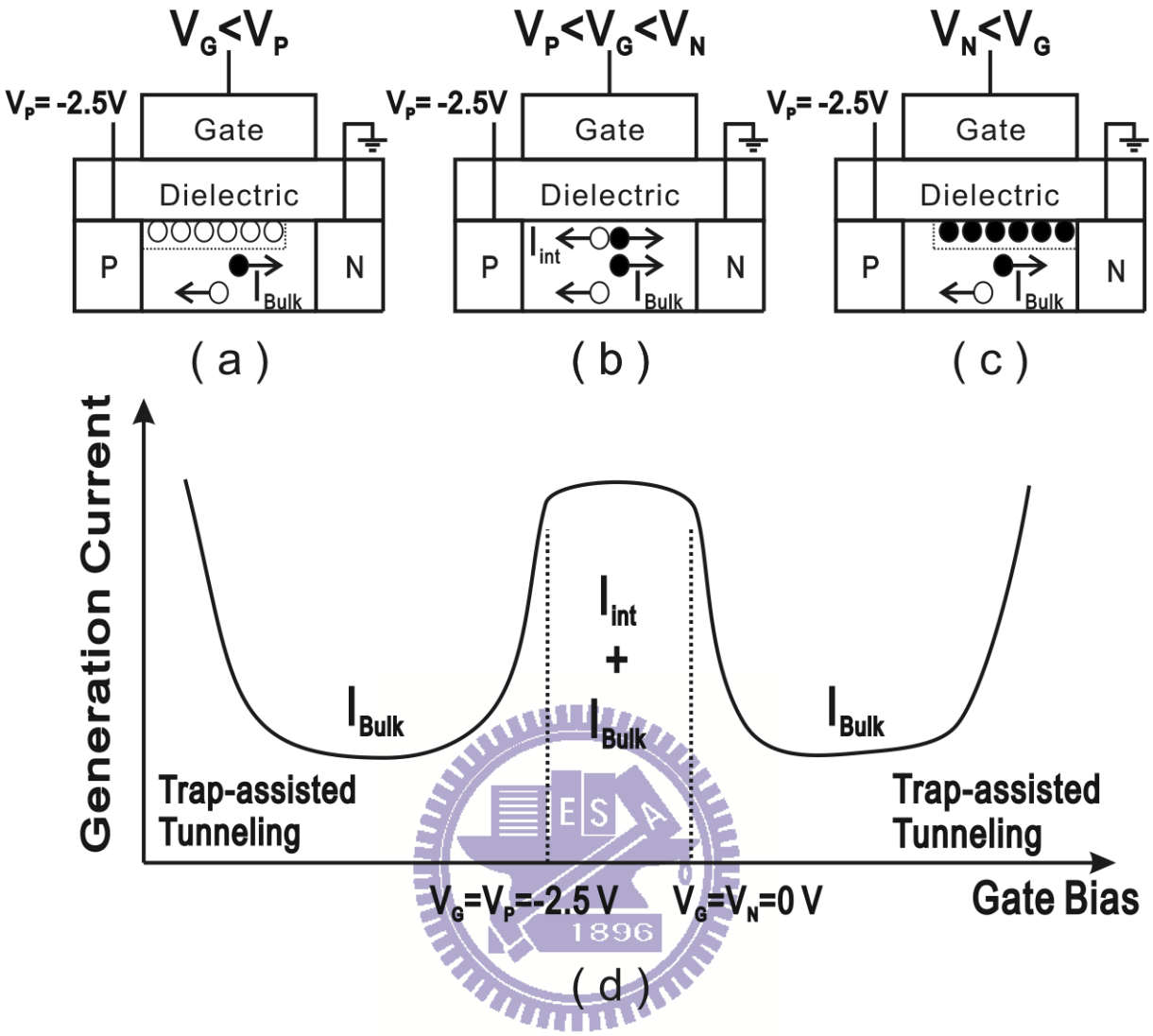

Figure A-3 Schematic operation regimes of the gated poly-Si PIN diode under the junction reverse bias condition with gate sweeping.

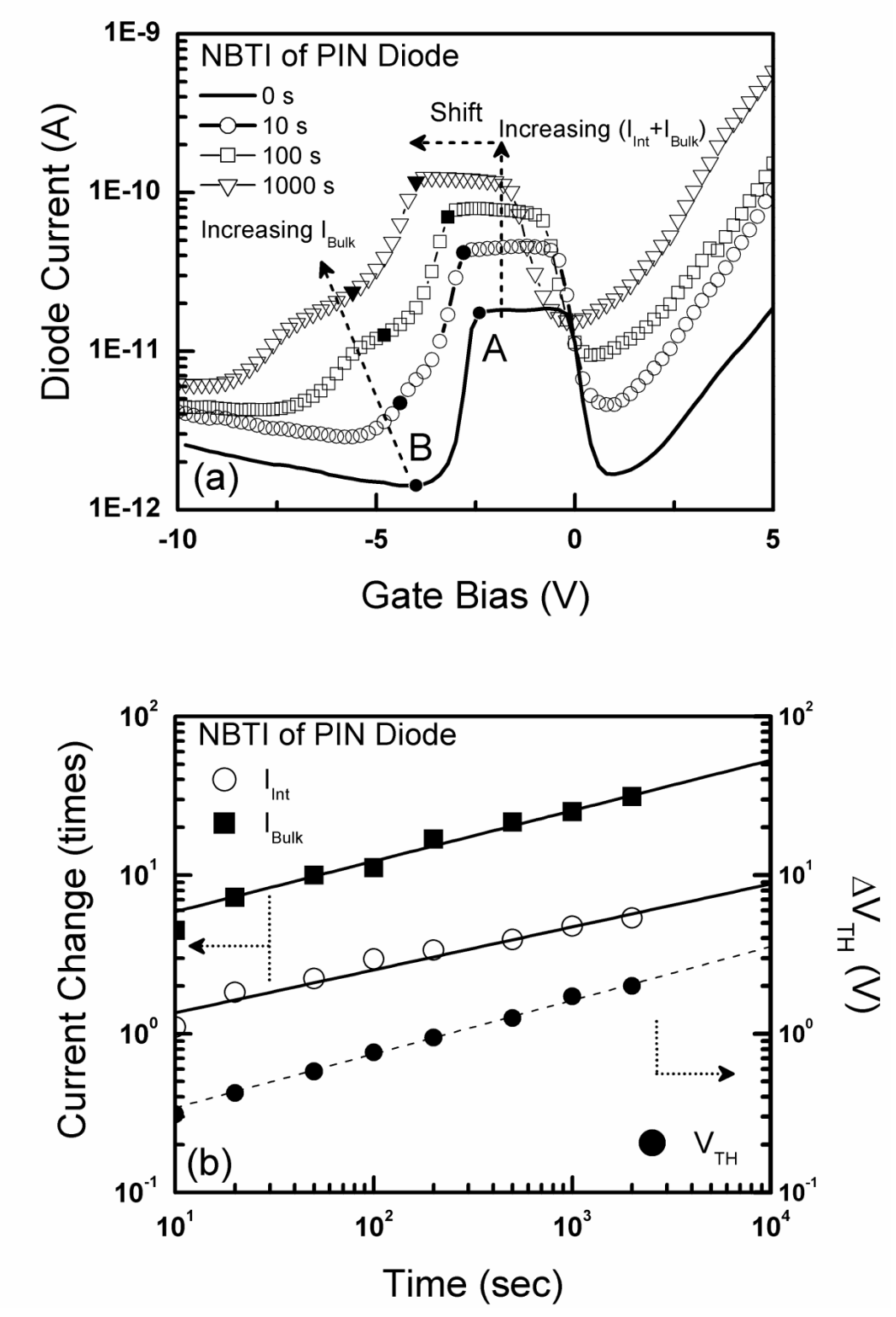

Figure A-4 (a) Electrical characteristics, and (b) current variation of the gated poly-Si PIN diodes under NBTI stress with time progressing.

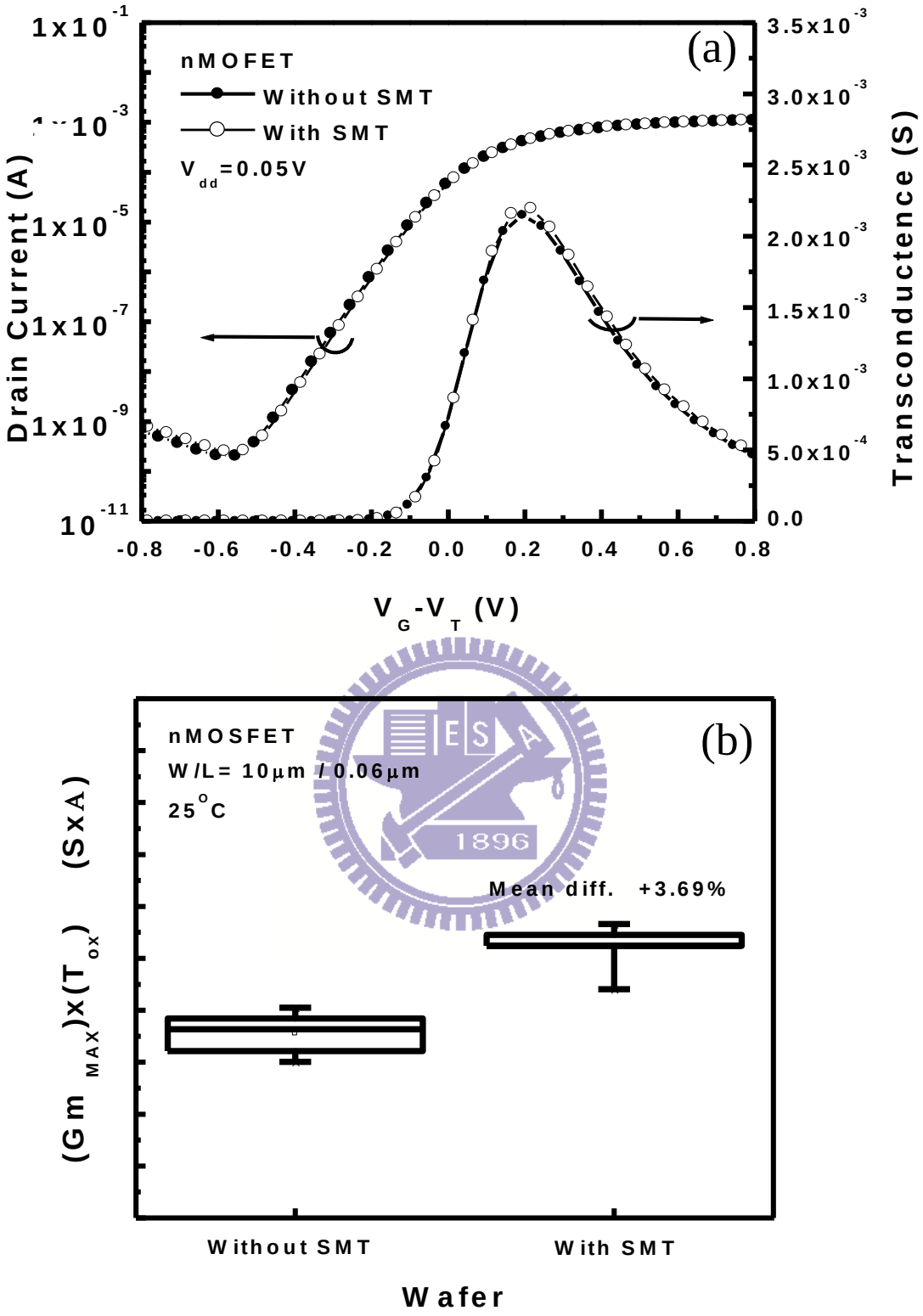

Figure A-5 Comparison of (a) linear mode transfer characteristic (Id-Vg) and (b) mobility for nMOSFET with and without SMT.

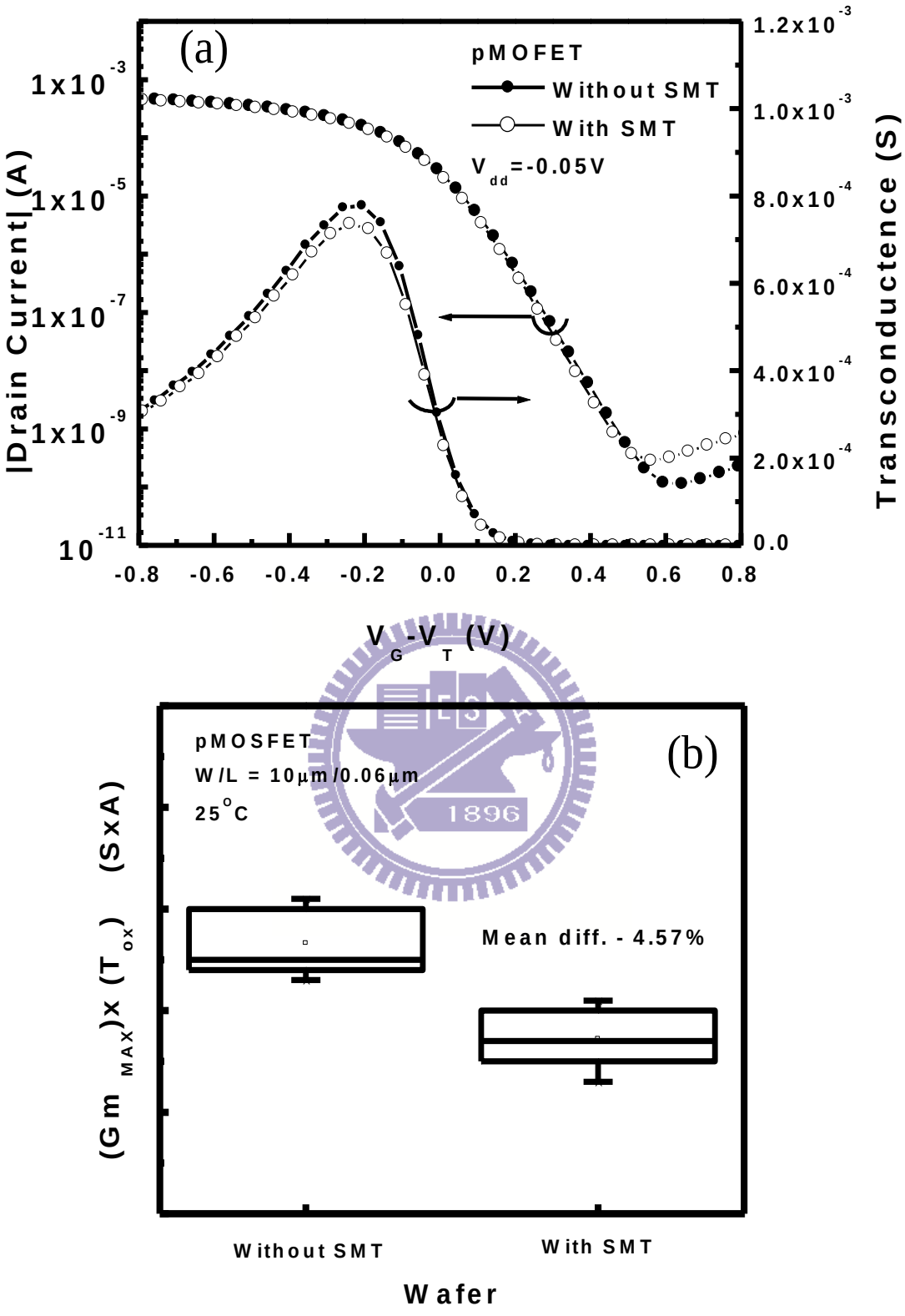

Figure A-6 Comparison of (a) linear mode transfer characteristic (Id-Vg) and (b) mobility for pMOSFET with and without SMT.

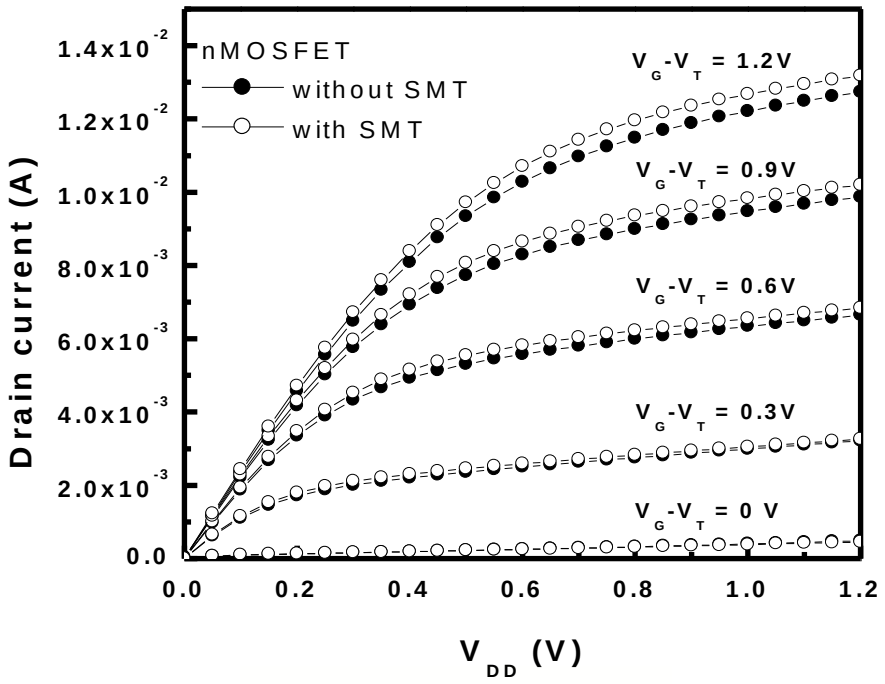

Figure A-7 Output characteristics of nMOSFET with and without SMT.

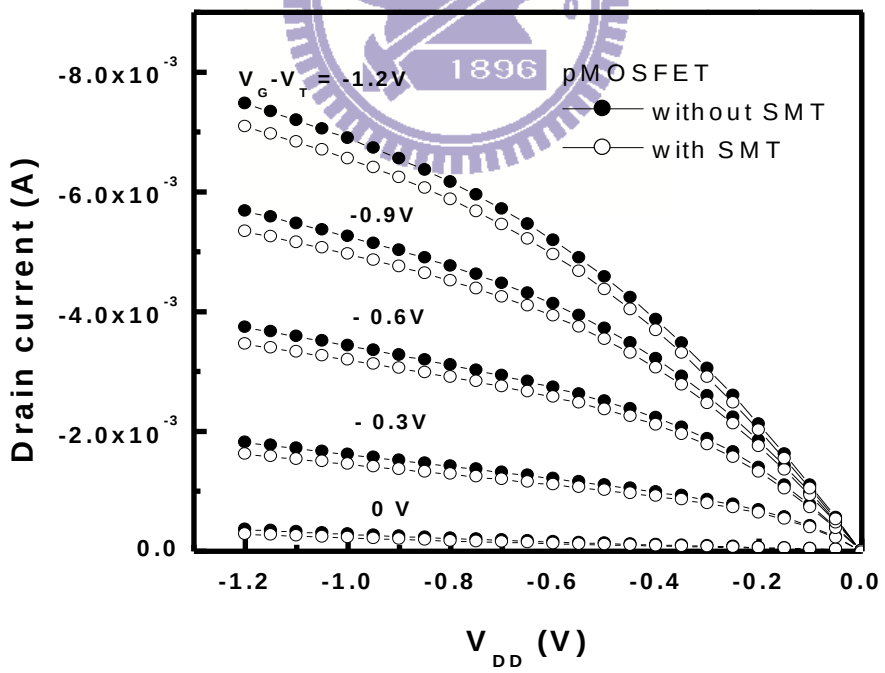

Figure A-8 Output characteristics of pMOSFET with and without SMT.

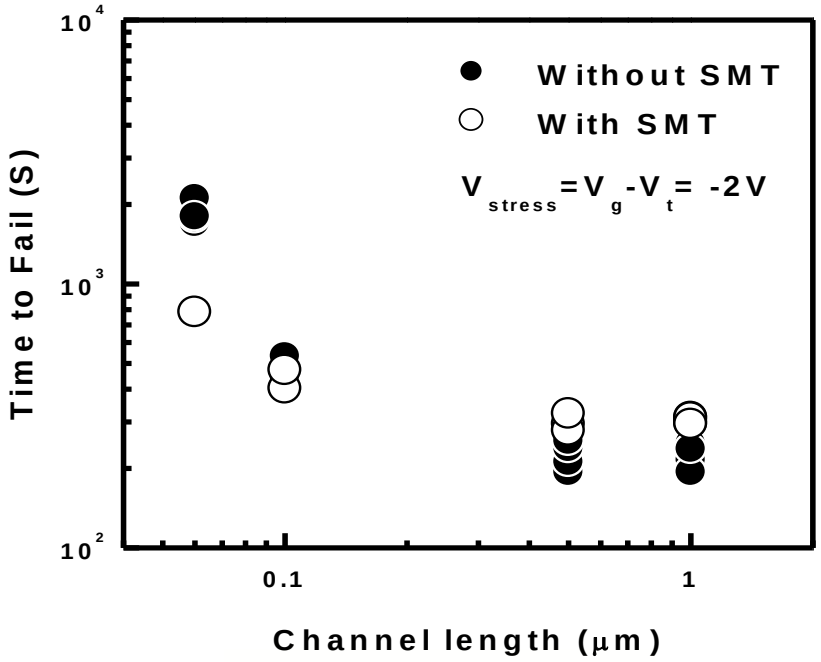

Figure A-9 NBTI lifetime for pMOSFET with and without SMT.

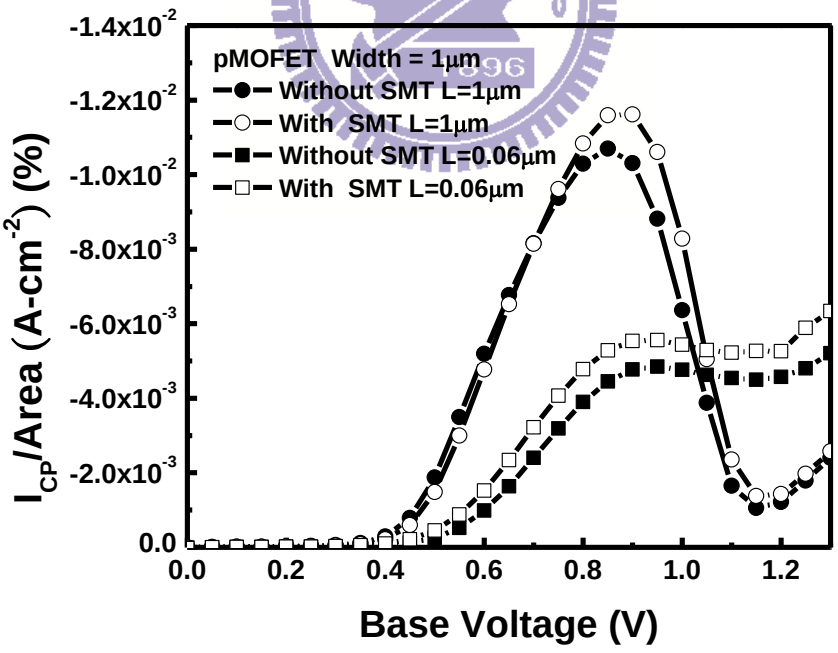

Figure A-10 Charge-pumping current versus base voltage for pMOSFET with and without SMT.

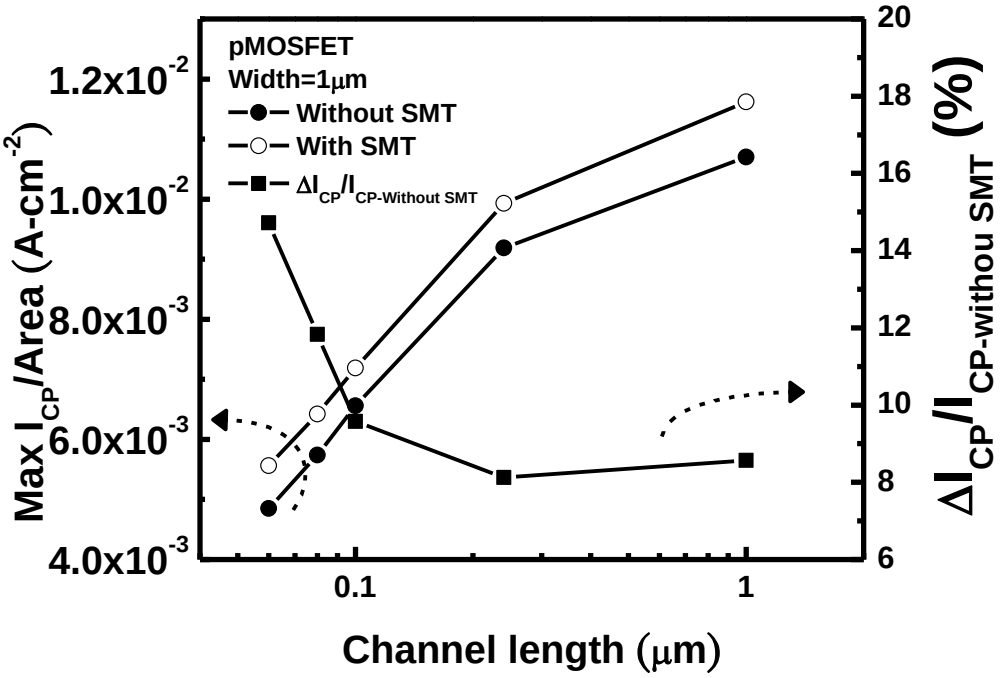

Figure A-11 Maximum charge pumping current as function of channel length.

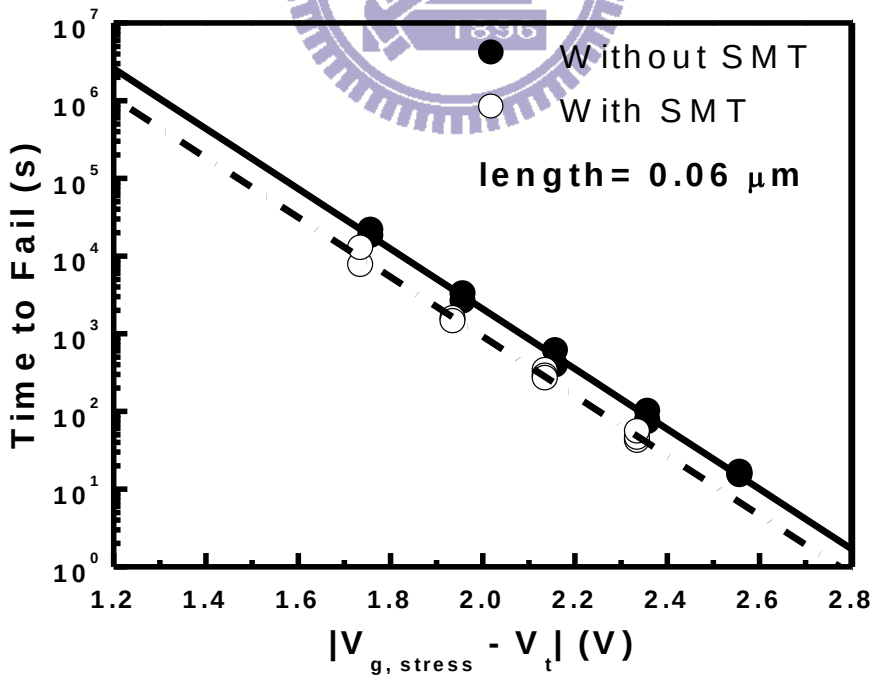

Figure A-12 Comparison of NBTI lifetime for short channel devices with and without SMT

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Study of Thin Gate Dielectrics on Silicon and Germanium MOSFETs

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2. Po-Tsun Liu, **C. S. Huang**, and C. W. Chen, "Enhanced Planar Poly-Si TFT EEPROM Cell for System on Panel Applications", *Electrochem. Solid-State Lett*. **10**, J89 (2007).
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7. **Chen-Shuo Huang** and Po-Tsun Liu, "Impact of Negative Bias Temperature Instability on Channel Bulk of Polysilicon TFT by Gated PIN Diode Analysis", *Electrochem. Solid-State Lett*. **14**, H194 (2011).

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3. Y. T. Chou, **C. S. Huang**, S. J. Shiau, P. T. Liu, L.W. Chu, "Investigation on Thin-Film-Transistors with a Transparent Material Zinc-Oxide Layer with DC sputter deposition system", International Display Manufacturing Conference, (IDMC, 2007)

4. **C.-S. Huang**, P.-T. Liu, "Repair of Thermal Damage in Gate Dielectric for Germanium-Based Metal-Oxide-Semiconductor Device by Supercritical Fluid

Technology", International Conference On Metallurgical Coatings And Thin Films (ICMCTF, 2011)

C. Patent:

1. 張鼎張，李泓緯，劉柏村，**黃震鑠**，"反堆積型薄膜電晶體"，中華民國專利申請案號：095132324
2. 張鼎張，李泓緯，劉柏村，**黃震鑠**，"具有埋藏層的薄膜電晶體及其製造方法"，中華民國專利申請案號：095132357
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