國立交通大學

電機與控制工程學系

碩 士 論 文

高頻寬切換電容式低通濾波器及內建自我測試電路

A High Bandwidth Switched-capacitor Low-pass Filter and Built-in-self-test Circuit

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中 華 民 國 九 十 三 年 七 月

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高頻寬切換電容式低通濾波器及內建自我測試電路

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摘　　要

隨著近幾年積體電路製程技術的進步，我們需要更快速及更複雜的測試設備來達到測試的規格及功能。有一種簡化測試設備的創新方法，就是將測試功能搬到晶片內部，而這種方法就叫作內建自我測試。如何在有限的面積及電源消耗增加之下來達到內建自我測試的功能，是現今混合信號測試設計者最重要的一項課題。

在本論文中，我們完成了一個全差動、取樣頻率 140 MHz、轉角頻率 10 MHz、切換電容式四階低通濾波器用來當作待測電路；此濾波器包括了兩個串接的 biquad 濾波器。除此之外，我們利用三角波各部份所佔的機率這樣一個觀念來實現我們切換電容式濾波器的內建自我測試電路。我們的內建自我測試電路包括了一個 29.2 KHz 三角波振盪器用來當作測試波形產生器、一個雙端轉單端電路及一個雙重比較器用來作為輸出響應分析器。利用這樣一個方法，我們可以由測試結果得知每一個 biquad 濾波器所擁有的增益誤差及偏移誤差。

A High Bandwidth Switched-capacitor Low-pass Filter and Built-in-self-test Circuit

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ABSTRACT

As IC fabrication technology advances in recent years, faster and more complex test equipments are required to achieve test specifications and test functions. An innovative method to simplify the test equipment is to move test functions onto the chip itself, which is called *Built-In-Self-Test* (BIST). How to achieve on-chip test function with limited area and power overhead is the main issue for mixed-signal testing designers.

In this thesis, we accomplish a fully-differential, 140 MHz sampling frequency, 10 MHz corner frequency, switched-capacitor 4^{th}-order low-pass filter to be the core circuit, which consists of two cascading biquad filters. Besides, we use the concept about probabilities of a triangular-wave to implement BIST circuits for the SC filter. In our BIST circuit, it consists of a 29.2 KHz triangular oscillator taken as test-waveform-generator, a differential-to-single-ended circuit and a dual-comparator taken as output-response-analyzer. According to this approach, we can obtain the information on gain error and offset error of each biquad filters from test results.

誌　　謝

碩士班兩年的時光一轉眼即將結束。回首過去這兩年交大生活的點點滴滴，我可以自豪的告訴自己：我有充份的把握每一個學習的機會，我也有盡到自己最大的努力，每一天都在進步。

我首先要感謝的人，兩年來指引著我方向、不斷督促我向前進步的人，就是我的指導教授：蘇朝琴 教授。老師教導我的，不只是專業領域的知識，還包括了待人處事應有的態度。他讓我了解到：遇到困難時，必須以勇敢、積極的態度去面對它並克服它；千萬不能有逃避的想法!

同時，我也要感謝我的父母，他們給我安定無憂的環境，並且一直支持著我，做我的後盾，讓我可以專心完成我的學業；還有我的女友，她在我低潮時不斷地鼓勵我，讓我有堅持下去的動力。

當然也要感謝學長們兩年來的照顧。謝謝鴻文、仁乾學長在我有疑問的時後都會熱心指導我；謝謝能哥學長在我有疑問的時後都會幫我找參考資料；也謝謝丸子學長在我沒有疑問之後都會陪我打電動。

感謝我的同學及學弟們：Pon 哥、Terry、HWWang、Angus、Levi、Marvel、Ada、Ku、Cgu、阿銘。在這兩年中，和你們一起熬夜寫作業、一起打籃球、一起 Men’s Talk 的時光，我永遠不會忘記！

最後，謝謝我高中或大學就認識的朋友：Madd、Nano、Herrylin、威哥、酷樟、Simon、Cepeda。還好交大的研究生活有你們在我身旁，謝謝你們陪我度過在新竹的無聊時光。看著你們一個一個畢業離去，也激勵了我要努力往前走。

袁成宇

07/06/2004

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Introduction

1.1 Motivation

CMOS technology has been growing very fast in recent years, Design of *integrated circuits* (ICs) becomes so complex and gate counts become so large. Undoubtedly, faster and more complex test equipments are required to achieve test specifications and test functions. An innovative method to simplify the test equipment is to move test functions onto the chip itself, which is called *Built-In-Self-Test* (BIST).

Built-in-self-test of digital circuits is a mature methodology now. For example, IEEE std. 1149.1, has defined completely test structure and test functions for on-chip and off-chip testing of digital circuits, and already be widely used in today's digital ICs. However, for analog or mixed-signal testing, it is still a big challenge since testability is not yet a precisely defined term in the analog world. Although IEEE std.1149.4 has defined mixed-signal testing, it's still not adopted widely because of the complexity and cost overhead. Design of

mixed-signal BIST circuits, in other words, how to observe and measure accuracy of internal signals on chip with limited cost increasing, is going to be the main issue for mixed-signal testing.

Switched-capacitor (SC) circuits are the most popular approach for realizing analog signal processing in MOS integrated circuits. As filtering technique, SC filters are quite popular in analog and mixed-signal designs. The replacement of resistors with capacitors and control clocks not only reduces layout area but also improves accuracy of the design. Accurate frequency response and good linearity are obtained since filter coefficients are determined by capacitor ratios which can be set quite precisely on the order of 0.1%.

In this thesis, we accomplish a 140 MHz sampling frequency, 10 MHz corner frequency, fully-differential, 4^{th}-order SC low-pass filter. It is implemented by two cascading biquad filters. Besides, we use the concept about probabilities of a triangular-wave to implement BIST circuits for the SC filter. According to this approach, we can obtain the information on gain error and offset error of each biquad filters.

1.2 Thesis Organization

This thesis comprises five chapters. Chapter 1 introduces the motivation of this thesis and thesis organization. Chapter 2 introduces mixed-signal testing standard, IEEE std.1149.4 and recent research about BIST of SC filters, and then describes test concepts and equations we adopted in this thesis. Chapter 3 describes the equation derivation of low-pass filters and circuit implementation of SC filters, which includes a fully-differential, high bandwidth

operational amplifier. Simulation results of each circuit will also be shown in this chapter. Chapter 4 describes the architecture of our approach and circuit implementation of BIST, which includes a *test-waveform-generator* (TWG) and an *output-response-analyzer* (ORA). Simulation results of the BIST and chip layout consideration, placement and implementation will also be shown in this chapter. Finally, conclusion and future work will be described in Chapter 5.

Chapter 2

Background

2.1 Introduction of IEEE std.1149.4

With increasing density and complexity for IC technology, *in-circuit test* (ICT) techniques become more costly and difficult to implement. Several electronic system manufacturers, such as Philips and IBM, have developed an innovative boundary scan method to improve design controllability and observability. In 1990, the IEEE adopted this approach as IEEE std.1149.1 and soon it has become a widely accepted DFT technique for digital circuits. Because IEEE std.1149.1 addressed only digital circuits, designers began developing equivalent test structures for mixed-signal circuits and corresponding measurement methodologies. In 1999, IEEE std.1149.4 was carried out for mixed-signal testing. We will introduce circuits and functions of main blocks for IEEE std.1149.4 below.

Figure 2.1 is the architecture of IEEE std.1149.4. There are 6 pins prepared for test I/Os. TCK is the test clock, TDI is the test data input, TDO is the test data output, TMS is the test

mode select, and AT1, AT2 are the analog test access ports. We can send test pattern into the scan chain and then obtain test results of each core blocks by connecting each boundary scan cell (DBM, ABM) together.

TAP controller, *Test Access Port controller*, is a very important block of the system. Its main objective is to facilitate board-level testing through boundary scan. TBIC, *Test Bus Interface Circuit*, is to connect internal test bus (AB1, AB2) and analog test access port (AT1, AT2). Figure 2.2 shows the architecture of TBIC. In this figure, TBIC controls ten switches (S1~S10) depending on the control signals sent from TAP controller. Figure 2.3 is the main architecture of ABM. ABM means *Analog Boundary Module*, it consists of 6 switches (Sh, Sl, Sg, SB1, SB2, SD), control registers and update registers. The objective of control registers and update registers is to generate the control signals for the 6 switches.

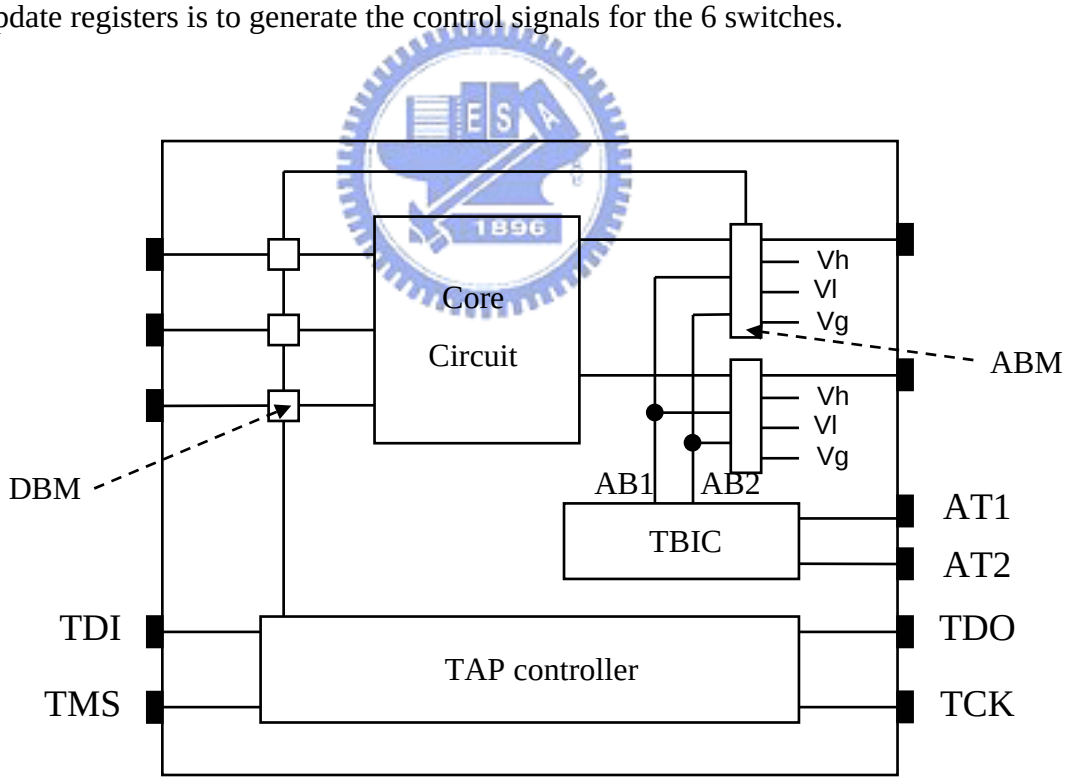


Figure 2.1 IEEE std.1149.4 architecture

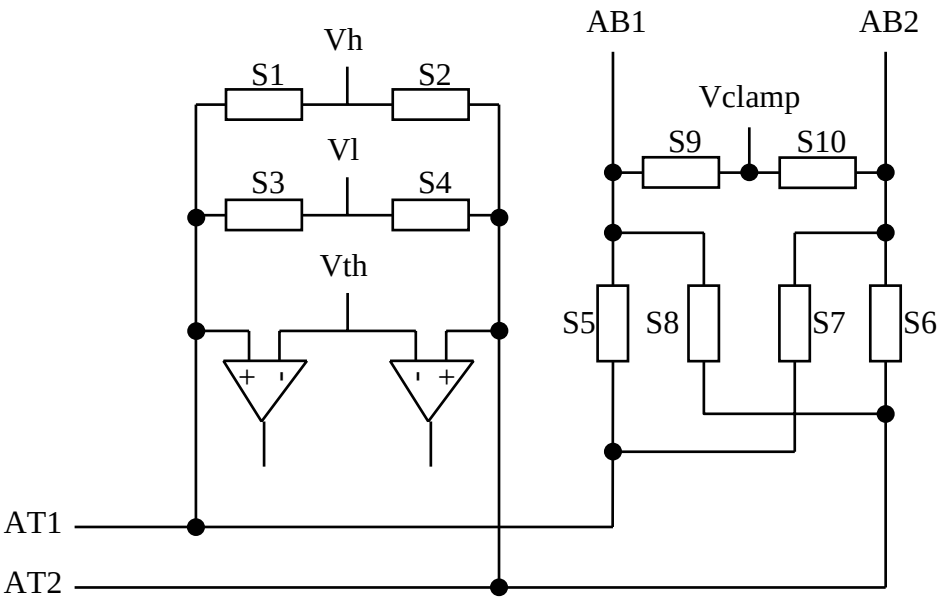


Figure 2.2 TBIC architecture

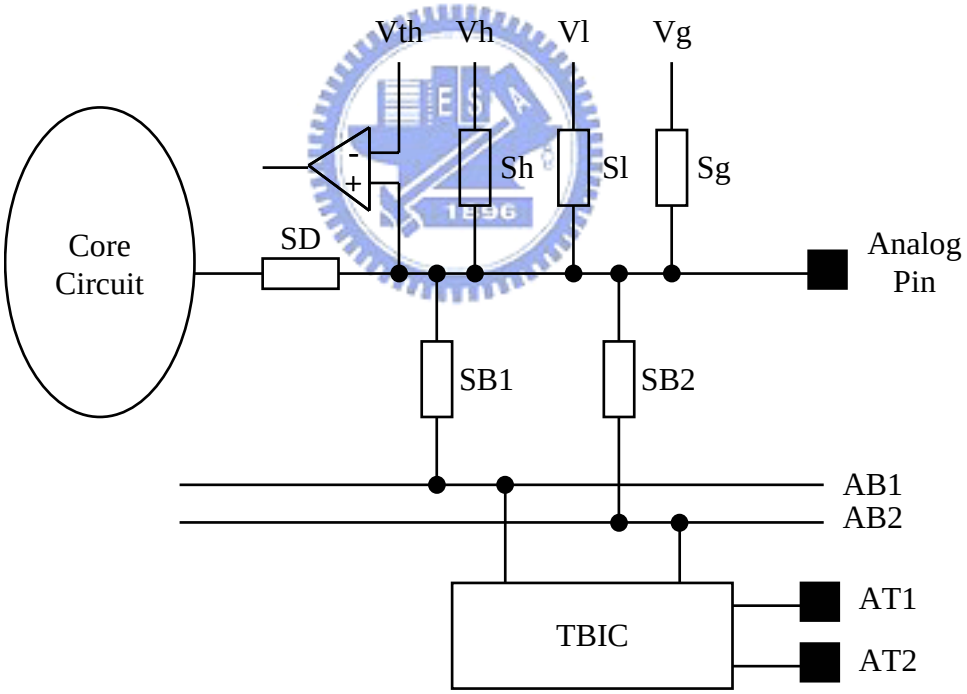


Figure 2.3 ABM architecture

The aim of the IEEE std.1149.4 research recently is to provide standardized approaches to interconnect test, parametric test and internal test [1], [2]. The first objective is to detect opens in the interconnections between integrated circuits. The second objective refers to the

problem of measuring the values of discrete components. And the third objective refers to the ability to perform internal test of a component. In [2], they take SC filter as core circuit for example and simulate the whole circuit under normal mode and test mode. Figure 2.4 shows its structure.

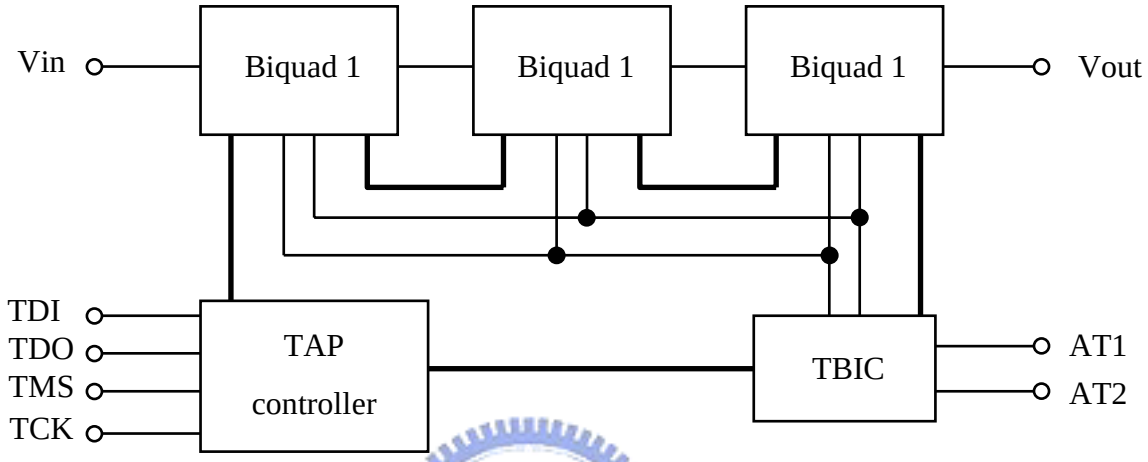


Figure 2.4 SC filter with IEEE std.1149.4 structure

2.2 Research of SC Filter BISTs

In recent years, design-for-test and built-in-self-test technique for SC filters are popular fields of research. Many papers have been presented to apply different approaches to achieve on-chip test functions with minimum area and power overhead [3]-[6]. Here, we take [6] for example because of its novel ideas and complete circuit structures.

The objective in [6] is to discuss the possibility of reusing the existing hardware originally present in SC filters to implement test functions for a completely autonomous self-testable solution. The implementation of completely autonomous self-test implies the use

of on-chip *Test Pattern Generators* (TPGs) and *Output Response Analyzers* (ORAs). Figure 2.5(a) gives an example of analog filter made of a cascade of basic biquad clocks, and the TPG and ORA are added to the original circuit. The concept of this paper is shown in Figure 2.5(b). Some of the existing biquad blocks are reused in test mode to implement the TPG and ORA.

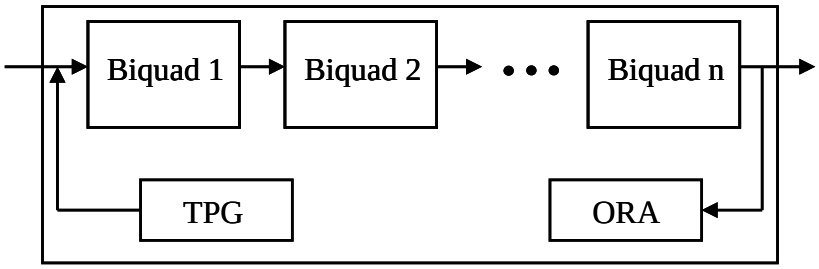


Figure 2.5(a) Classical BIST

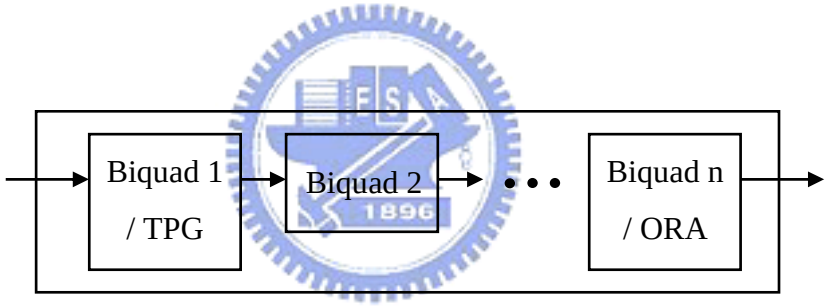


Figure 2.5(b) Reuse-based BIST

2.2.1 Multi-frequency TPG

The stimuli generator is a sine wave oscillator. As shown in Figure 2.6, this oscillator is based on two pure integrators connected in a ring configuration. A 360° phase shift is ensured because the first integrator is inverting and the second integrator is non-inverting. Non-inverting integrator uses negative resistor, which is implemented by swapping two clock phases of a positive switched-capacitor [7].

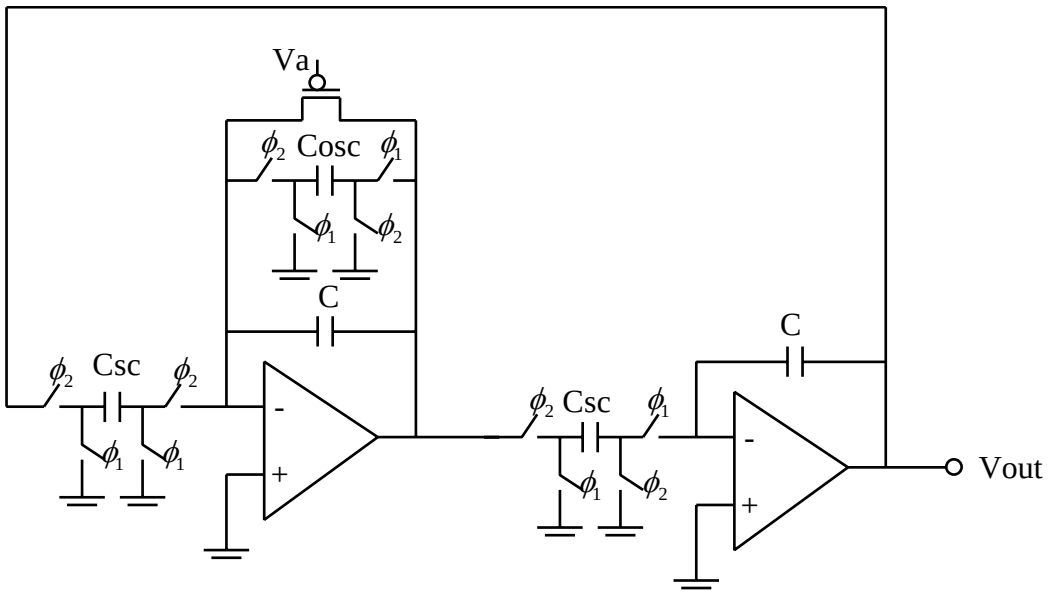


Figure 2.6 TPG

From Figure 2.6, oscillation frequency of TPG is given by

$$f_{osc} = \frac{f_{clk} \cdot C_{sc}}{2\pi C} \quad . \tag{2-1}$$

The negative SC resistor in the local feedback loop of the first integrator results in a positive feedback. It ensures circuit instability and a faster growth in the oscillation amplitude. The bias voltage Va is used to adjust the amplitude of the oscillation.

2.2.2 Multi-frequency ORA

As shown in Figure 2.7, the ORA is also based on cascade of two integrators and an additional comparator. A digital signature is obtained by computing the time for the output of the second integrator to reach Vref. There is a counter for computing digital signatures, and

this counter must be enabled from the integration start up to the time when the comparator output goes high [8], [9].

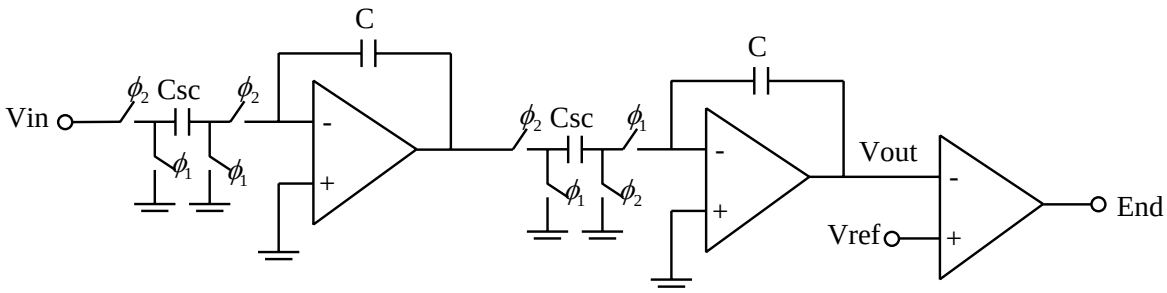


Figure 2.7 ORA

2.2.3 Reused-based BIST of 8th Order Filter

Figure 2.8 shows the new implementation of the 8th order low-pass filter with self-test facilities and Figure 2.9 is the new type low Q biquad filter circuit. Each biquad filter plays both roles of the TPG (mode2) or the ORA (mode3) in test mode. Besides, both integrators can be reset by shortening their integration capacitors (mode4). The operation mode of a given biquad filter is determined by two bits in two flips-flops. Only one comparator is added to the whole circuit and connected to each biquad filter output through a multiplexer.

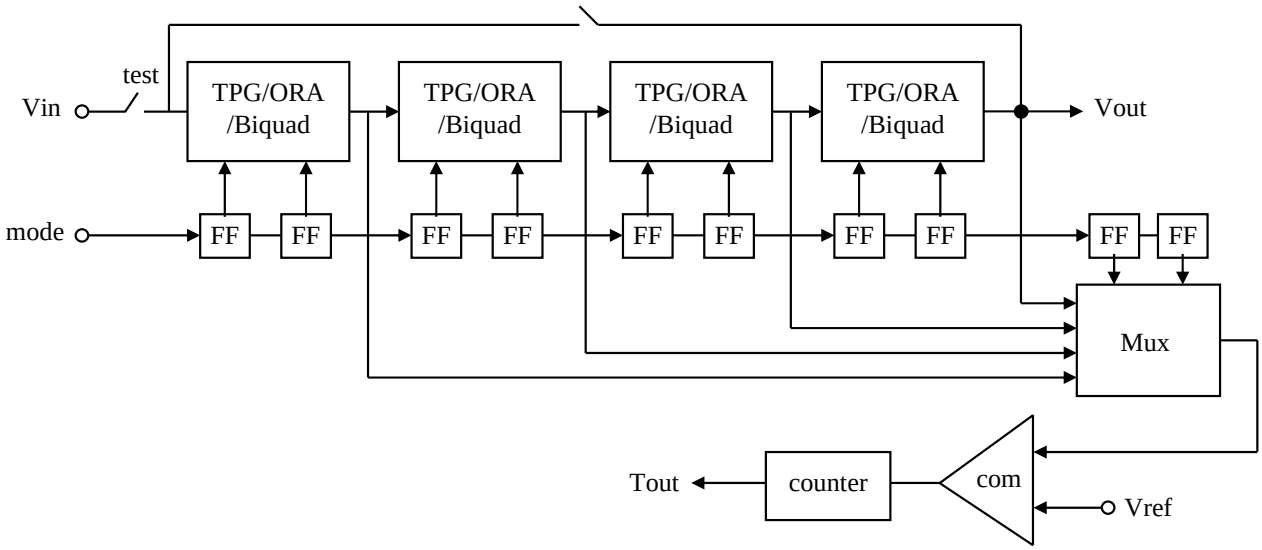


Figure 2.8 Self-testable 8th order low-pass filter topology

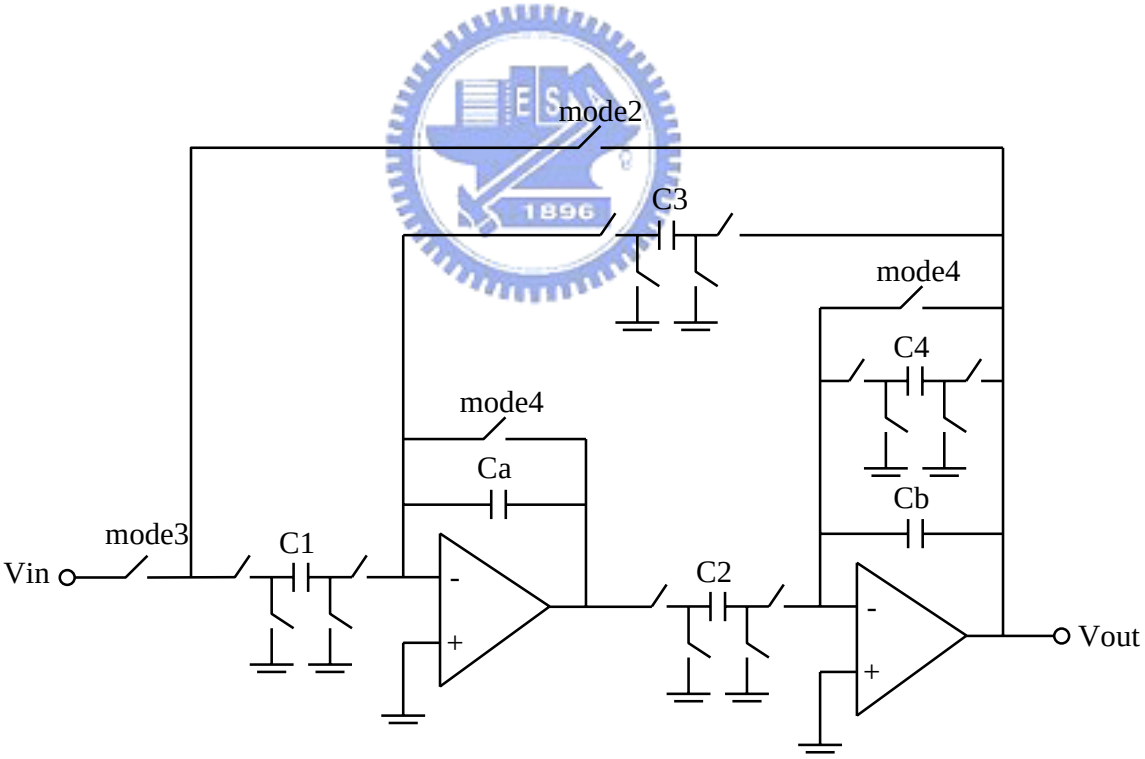


Figure 2.9 New low Q biquad

The test procedure includes 4 phases, each phase being dedicated to the test of one of the biquad filters. For example, if the second biquad filter is tested, then the first biquad filter acts as the TPG and the third one as the ORA. In the next phase, test functions are moved to the next blocks so the third biquad filter is tested in this phase.

The self-test method presented in [6] is innovative, but there are still some problems exist when we realize it for circuit implementation. First, each biquad filter is able to perform its normal function, work as sine wave oscillator, or as a signature analyzer. This characteristic can effectively decrease area overhead. But, performance of the core circuits is also affected because we change the structure of biquad filters. Second, design of a sine wave oscillator is complex and we can not generate the sine wave actually. This will affect the precision of test results.

2.3 Concept and Formula Derivation

In this thesis, we will use different concepts and methods from [6] to avoid its main drawbacks. First, we use triangular-wave as test waveform to replace sine wave. Therefore, we can implement a high resolution test waveform. Second, we use a pair of comparators called dual-comparator to replace single comparator. According to the dual-comparator analysis, we can divide a triangular-wave into 3 portions. Therefore, we can compute the probabilities of each portion. Moreover, we can also obtain the probabilities when the triangular-wave has different values of offset and amplitude. Finally, we can obtain the information about gain error and offset error of the core circuits by comparing the probability

of the self-test results to the derived ones.

Figure 2.10 shows the concepts of our method. In this figure, Va is the amplitude of the triangular-wave, Vx is offset of the triangular-waves, and Vr+, Vr- are the reference values of the dual-comparator.

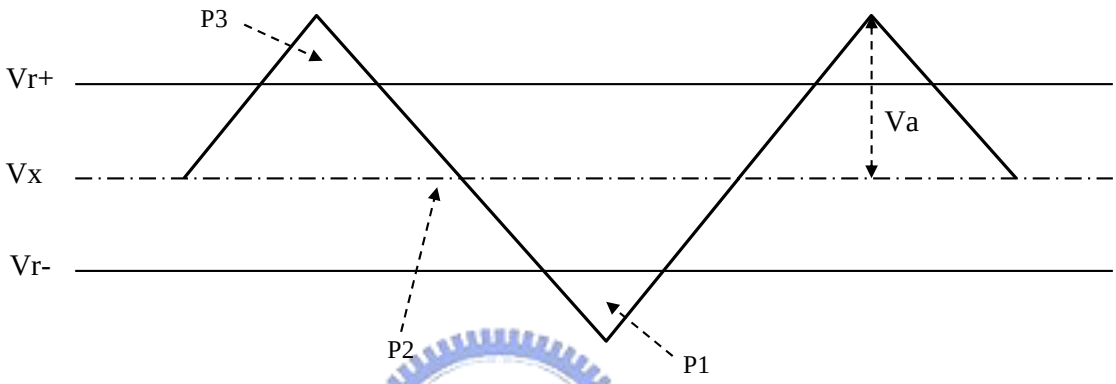


Figure 2.10 Concept of method

P1 is the probability of that the triangular-waves are lower than Vr-. P2 is the probability of that the triangular-waves are between Vr+ and Vr-. And P3 is the probability of that the triangular-waves are higher than Vr+. According to the formula derivation we can obtain the equations of P1, P2 and P3 as

$$\text{CASE 1: } V_X + V_A < V_{R+}$$
$$P_1 = \frac{1}{2} - \frac{(V_X - V_{R-})}{2V_A}. \quad (2\text{-}2)$$
$$P_2 = \frac{1}{2} + \frac{(V_X - V_{R-})}{2V_A}.$$
$$P_3 = 0.$$

CASE 2: $V_X + V_A < V_{R+}$, $V_X - V_A < V_{R-}$

$$P_1 = \frac{1}{2} - \frac{(V_X - V_{R-})}{2V_A}.$$

$$P_2 = \frac{(V_{R+} - V_{R-})}{2V_A}. \quad . \qquad \text{(2-3)}$$

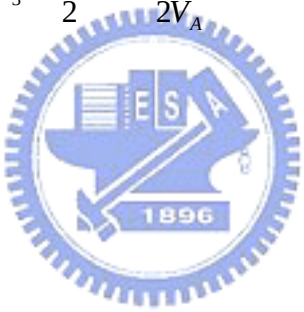
$$P_3 = \frac{1}{2} - \frac{(V_{R+} - V_X)}{2V_A}.$$

CASE 3: $V_X - V_A > V_{R-}$

$$P_1 = 0.$$

$$P_2 = \frac{1}{2} + \frac{(V_{R+} - V_X)}{2V_A}.. \qquad \text{(2-4)}$$

$$P_3 = \frac{1}{2} - \frac{(V_{R+} - V_X)}{2V_A}.$$



Chapter 3

Switched-capacitor Low-pass Filter

Switched-capacitor (SC) filters have become extremely popular due to their accurate frequency response, linearity, and dynamic range. Since coefficients of SC filters are determined by capacitance ratios which can be set precisely in ICs (on the order of 0.1%), accuracy of SC filters are much better than RC filters (as much as 20%).

A SC filter is realized with some basic building blocks such as opamps, capacitors, switches, and nonoverlapping clocks. We will detail the objectives, circuit structures and design considerations of these building blocks in this chapter.

3.1 Fully Differential, High Bandwidth Opamp

Most of SC circuits are implement with Opamps. However, some important opamp

nonidealities affect the accuracy of SC circuits such as DC gain, unity-gain frequency, phase margin and slew rate.

The *DC gain* of opamps in a CMOS technology is typically on the order of 60dB. Low DC gain affects the accuracy of the discrete-time transfer function.

The *unity-gain frequency* (Ft) and *phase margin* (PM) of an opamp gives an indication of the small signal settling behavior of an opamp. A general rule is that Ft should be at least 5 times larger in frequency than the clock frequency assuming little slew rate behavior occurs and PM is greater than 60° . Modern SC filters are realized using high-frequency single-stage opamps such as folded-cascode opamps or telescopic opamps. These opamps have very large output impedances (on the order of 100K Ohm) since the loads are purely capacitive, instead of resistive.

The finite *slew rate* (SR) of opamps can limit the clock frequency in SC filters as these circuits rely on charge being quickly transferred from one capacitor to another. Thus, at the instance of charge transfer, it is uncommon for opamps to exceed SR limit.

3.1.1 Fully-Differential Structure

In most analog applications, it is desirable to keep the signals in differential mode. Fully-differential signals imply that the difference between two lines represents the signal component. Thus, any noise appears as a common-mode signal on those two lines does not affect the signal. Fully differential circuits should also be balanced, implying that the differential signals operate symmetrically around a DC common-mode voltage which is called *analog ground*. Fully differential circuits have another advantage that if each single-ended signal is distorted symmetrically around the common-mode voltage, the differential signal

will have only odd-order distortion terms. These terms are often much smaller. Consider the block diagram shown in Figure 3.1, two nonlinear elements are identical and then each of the outputs can be found as a Taylor series expansion given by

$$V_o = k_1 \cdot V_i + k_2 \cdot V_i^2 + k_3 \cdot V_i^3 + \ldots \quad , \tag{3-1}$$

where k_i are constant terms. In this case, the differential output signal, V_{diff}, consists of only the odd-order terms,

$$V_{diff} = 2k_1 \cdot V_i + 2k_3 \cdot V_i^3 + 2k_5 \cdot V_i^5 + \ldots \quad . \tag{3-2}$$

With these two important advantages, most modern switched-capacitor circuits are realized using fully differential structures.

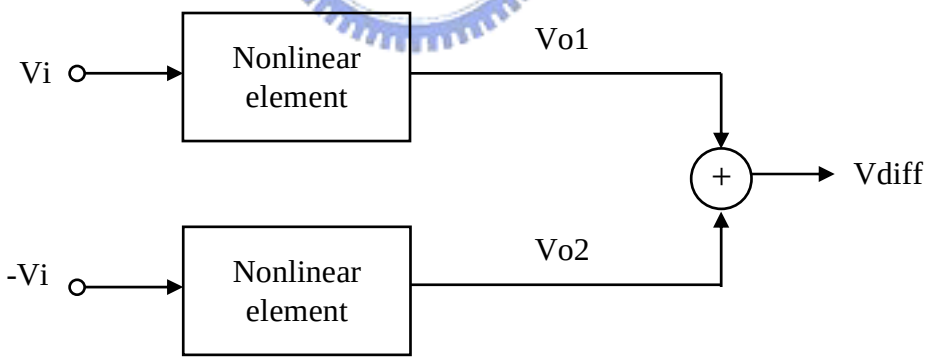


Figure 3.1

In this thesis, we introduce folded-cascode opamp as our opamp structure. We expect Ft of the opamp to be 5 times greater than clock frequency (140 MHz), and under this condition, we still have great DC gain about 60dB to reduce the gain error.

In the next parts, design considerations of the opamp and bias circuit for the opamp are described in detail. Finally, we compare pre-layout simulation and post-layout simulation results of the opamp.

3.1.2 Design considerations

Table 3.1 shows characteristics of three types of opamps. There are some critical points in choosing which one is suitable for our design. First, if we need high bandwidth, two-stage opamps is not a good choice. Second, we define V_{DD} as 1.8V for CMOS 0.18um technology, so output swing is a critical issue of our design. We can find that telescopic opamps are not applicable with its low output swing. So, in this thesis, we take folded-cascode opamp as the structure to implement opamp.

	Gain	**Output Swing**	**Speed**	**Power Dissipation**	**Noise**
Telescopic	medium	Low	high	Low	low
Folded-Cascode	medium	medium	high	High	medium
Two-Stage	High	High	low	medium	low

Table 3.1 Comparison of three types of opamps

Figure 3.2 is the structure of a typical fully-differential folded-cascode opamp. It has many advantages such as high bandwidth, high DC gain concurrently, and high dynamic range. However, its main drawback is the power dissipation. Compared to telescopic structure, folded-cascode has two current branches (differential input pair and cascode current mirror stage). For the circuit to work at normal region, we need larger current to drive it.

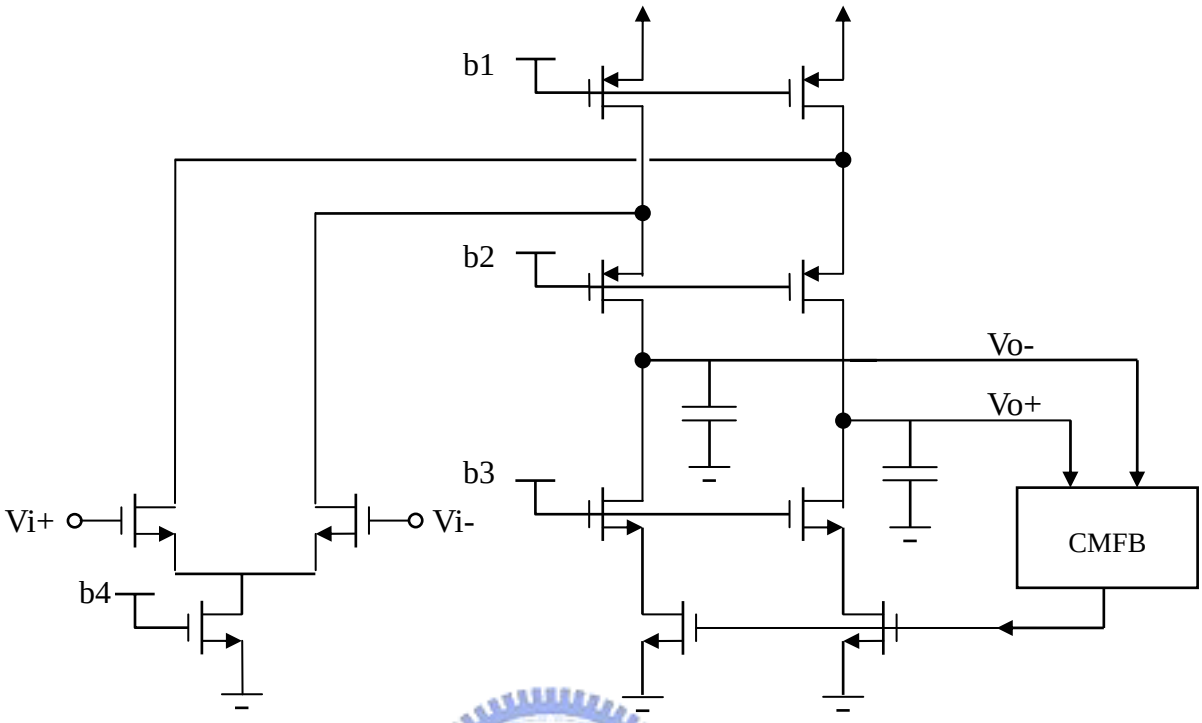


Figure 3.2 Typical fully-differential folded-cascode opamp

Typically, when using fully-differential opamps in a feedback application, the applied feedback determines the differential signal voltages, but does not affect the common-mode voltages. Therefore, it is necessary to add an additional circuit to determine the output common-mode voltage and to control it to be equal to the analog ground. This circuit is called *common-mode feedback* (CMFB) *circuitry*. CMFB has many drawbacks we can not overcome and these drawbacks will affect opamp performs. First, it is often the most difficult part of the opamp design. Second, there are two typical approaches to implement CMFB circuits, a continuous-time approach and a switched-capacitor approach. The former approach usually limits the signal range. And, if nonlinear, it may introduce common-mode signals. The latter one will increase additional capacitance loadings to the main circuit and then reduce bandwidth of the opamp. Switched-capacitor CMFB may also introduce clock-feedthrough

glitches.

To avoid the disadvantages of CMFB but achieve fully-differential structure, we use the approach in [10]. Figure 3.3 is a typical single-ended folded-cascode opamp. We use cascode current mirror to obtain wide-swing output range. Because a single-ended folded-cascode opamp has excellent *Common-mode Rejection Ratio* (CMRR), it has robust common-mode output voltage and tiny effects from noises and distortions. Due to these characteristics, we can implement a fully differential folded-cascode opamp without CMRR by two single-ended ones with inverse differential inputs. Figure 3.4 shows this concept. This structure can improve the bandwidth. Unfortunately, it has larger power dissipation than the typical one.

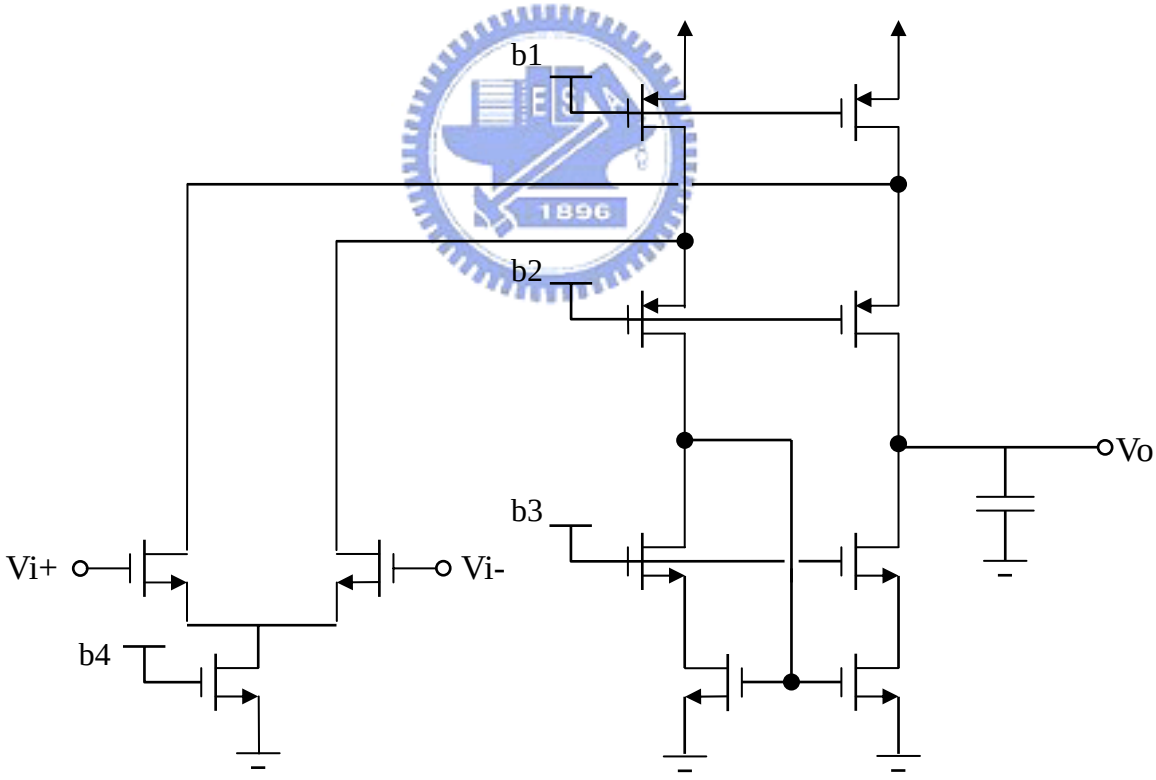


Figure 3.3 Typical single-ended folded-cascode opamp

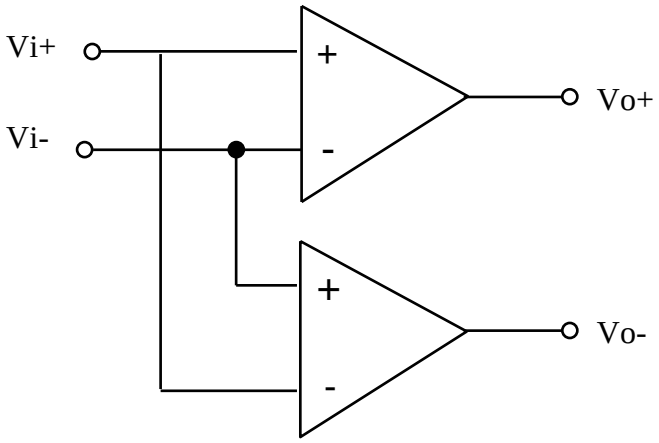


Figure 3.4 Concept of fully differential opamp presented in [10]

3.1.3 Fully differential, High Bandwidth Opamp

With recent technologies, High gains become more difficult to achieve because of short-channel effect. We let channel length as 0.36um here for the consideration of DC gain and to reduce the process variation concurrently. Figure 3.5 is the circuit structure of fully differential, high bandwidth opamp we use in this thesis. We set output loadings 2pF, current goes through Ms is 4.2mA and goes through M3,4, Ma3,4 is 1.9mA. Under these conditions, we obtain transconductance of differential input pair (M1,2 , Ma1,2) to be 15.8m (1/Ohm) and output impedance to be 51K (Ohm). Then, according to (3-3~5) we can compute specifications of the opamp as: DC gain=58.2 dB, Ft=790 MHz and Maximum SR=950 us/sec.

$$\text{DC gain} = g_m \cdot r_{out} \quad . \tag{3-3}$$

$$F_t = \frac{g_m}{C_{load}} \quad . \tag{3-4}$$

$$SR = \frac{I}{C_{load}} \quad . \tag{3-5}$$

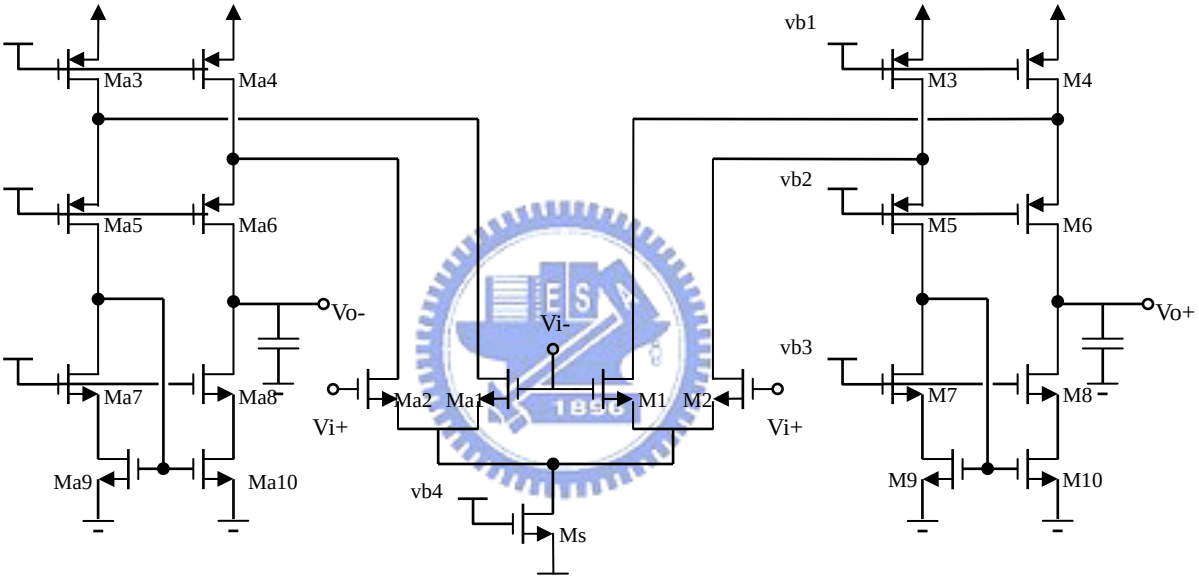


Figure 3.5 fully differential, high bandwidth opamp

Figure 3.6 is the frequency response simulation results of the opamp. It shows that the dominate pole falls into 1 MHz and the first nondominate pole falls into 990 MHz. At low frequency, DC gain is 57.1 dB (DC gain). The unity-gain frequency is 783 MHz and the phase margin is 57° .

Figure 3.7 is the CMRR simulation results. The CMRR is 74.3 dB at low frequency.

Figure3.8 is the simulation results of SR. We connect the opamp positive output and negative input together to become a unity-gain buffer. Use ideal square waves as input signal to obtain the SR simulation results. It shows that at rising edge SR is 552 us/sec (SR+) and at falling edge SR is 435 us/sec (SR-).

According to these data, we find that the simulation results are very close to the computing values according to the formulas.

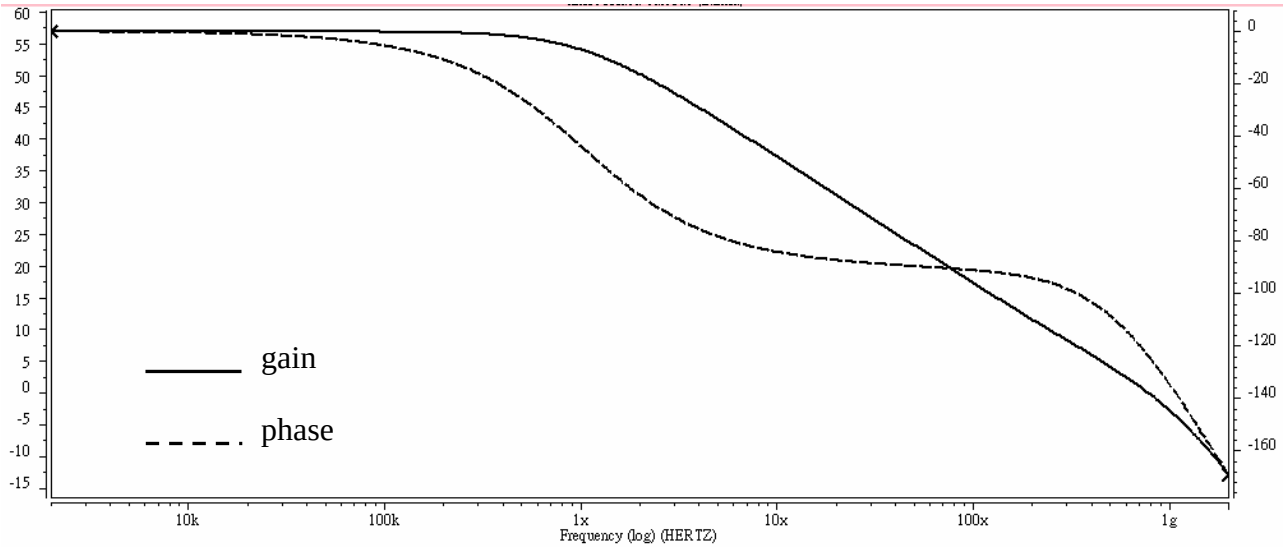


Figure 3.6 Frequency response simulation

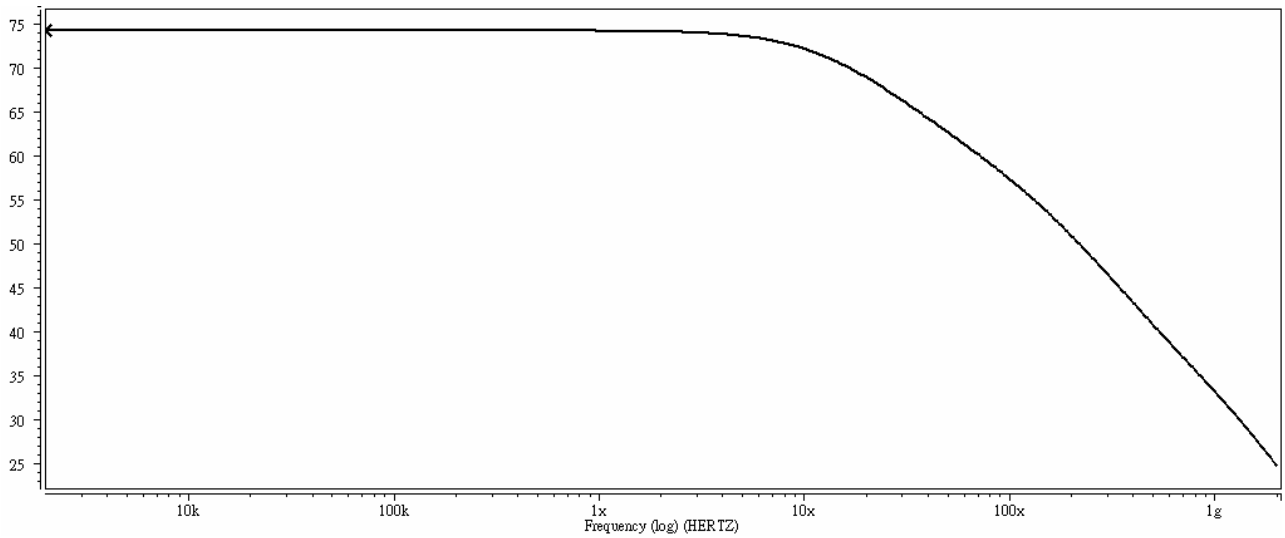


Figure 3.7 CMRR simulation

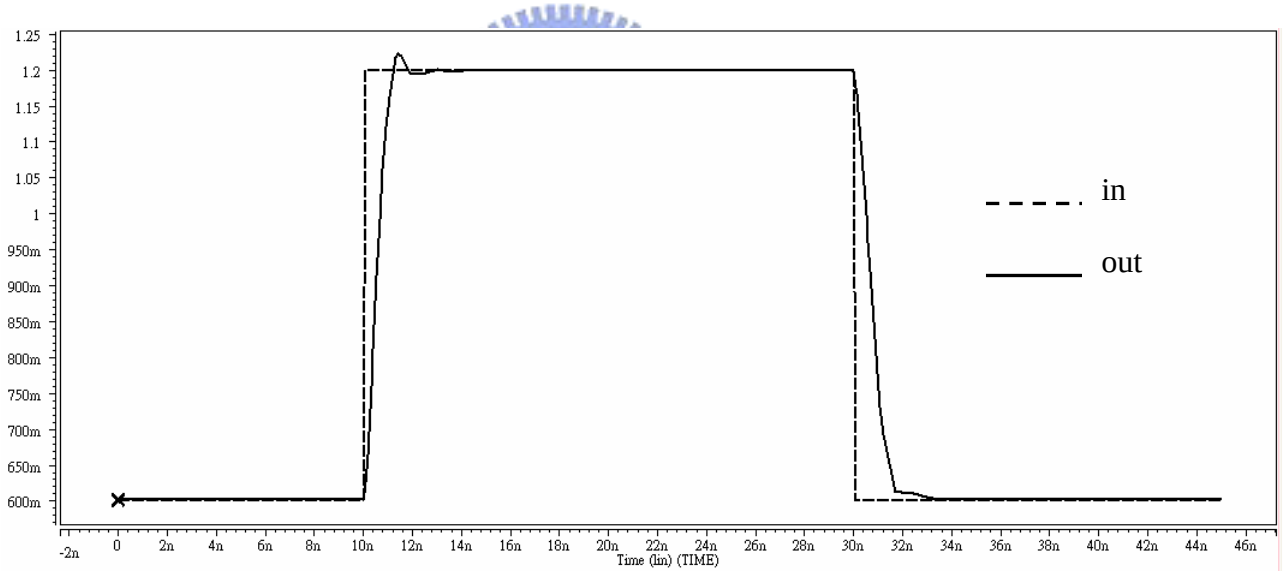


Figure 3.8 SR simulation

Table 3.2 shows the specifications summary of the opamp. It also shows the post-layout simulation results to compare with the pre-layout simulation results. For layout consideration, we use *Source-Drain Merge* method to reduce parasitic capacitor at the output of the opamp. Although using *common-centroid* method can reduce the input offset, it also increase parasitic

capacitor at input pair and decrease the Ft. So in this thesis we adopt traditional method for the opamp layout in order to hold the high bandwidth. Figure 3.9 is the layout of the fully differential, high bandwidth opamp, the area is 275 * 75 um^2.

	Pre-sim	**Post-sim**
loading (pF)	2	2
DC gain (dB)	57.1	57.4
Ft (MHz)	783	771
PM (degree)	57	57
SR+ (us/sec)	552	540
SR- (us/sec)	435	427
CM (V)	0.9	0.9
CMRR (dB)	74.3	74.6
power (mW)	14.8	15

Table 3.2 Specifications summary of the fully differential, high bandwidth opamp

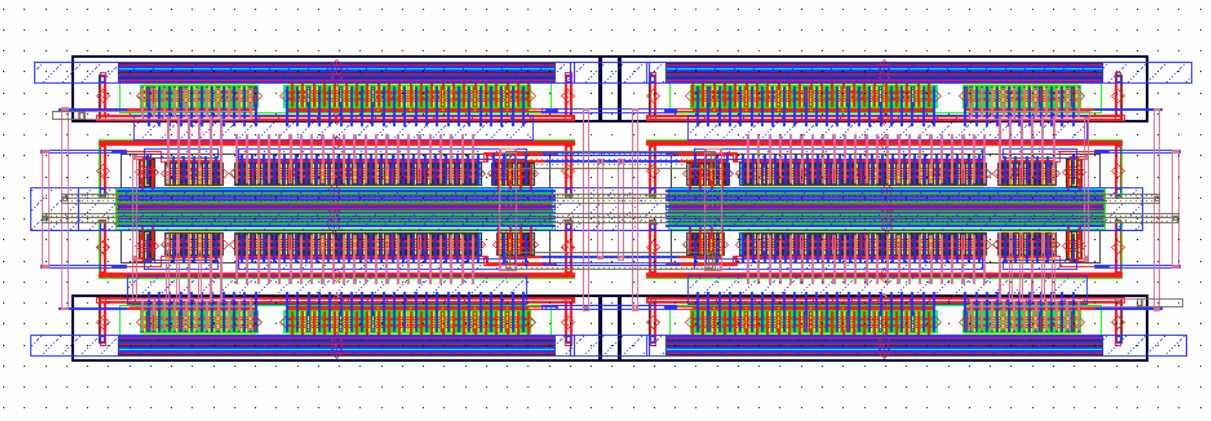


Figure 3.9 Layout of the fully differential, high bandwidth opamp

3.1.4 Wide-swing Constant-transconductance Bias Circuit

Besides the main circuit of the opamp described in the above section, bias circuit is also an important part. Its main function is to apply steady, noise-insensitive voltage for biasing points of the opamp. In this thesis, we introduce a wide-swing, constant-transconductance bias circuit to implement the biasing circuit. It consists of the start-up circuit to prevent the circuit working at unexpected steady state.

Perhaps the most important parameters in opamps are the transconductance of transistors. Figure 3.10 is a bias circuit that gives very stable transconductances. With this method, to a first-order effect, the transconductances are independent of power-supply as well as process and temperature variations.

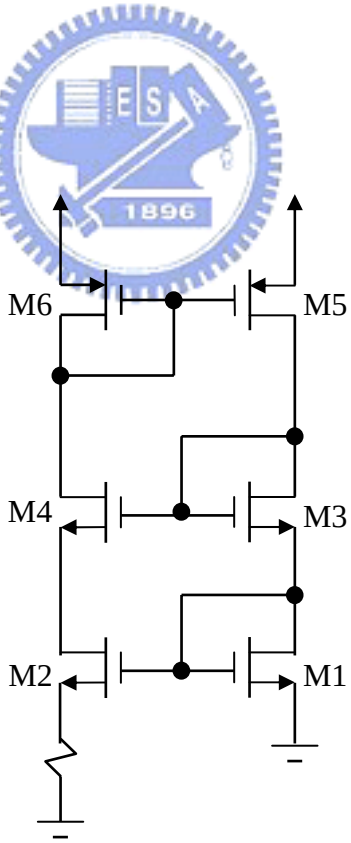


Figure 3.10 Bias circuit with stable transistor transconductances

Assuming the sizes of M5 and M6 are equal and the circuit has the same current (I_D) due to the current-mirror pair. As a result,

$$V_{gs1} = V_{gs2} + I_D \cdot R \quad . \tag{3-6}$$

Recalling that

$$V_{eff} = V_{gs} - V_t \quad . \tag{3-7}$$

We can subtract the threshold voltage from both sides in (3-6) and rewrite (3-6) as

$$\sqrt{\frac{2I_D}{\mu_n C_{ox}(\frac{W}{L})_1}} = \sqrt{\frac{2I_D}{\mu_n C_{ox}(\frac{W}{L})_2}} + I_D \cdot R \quad . \tag{3-8}$$

And recalling that

$$g_{m1} = \sqrt{2\mu_n C_{ox}(\frac{W}{L})_1 \cdot I_{D1}} \quad . \tag{3-9}$$

We obtain the important relationship

$$g_{m1} = \frac{2[1 - \sqrt{\frac{(W/L)_1}{(W/L)_2}}]}{R} \quad . \tag{3-10}$$

Thus, the transconductance of M1 is determined by geometric ratios only, independent of power-supply, process parameters, temperature or other parameters with large variability. For the special case of $(W/L)_2=(W/L)_1$, we can find

$$g_{m1} = \frac{1}{R} \quad . \tag{3-11}$$

As new technologies with shorter channel lengths are used, designers are often forced to use cascode current mirrors to achieve high gain. Unfortunately, the use of conventional cascode current mirror limits the signal swings, this drawback reduces the circuit practicality. One novel structure of cascode current mirrors that do not limit the signal swings is shown in Figure 3.11, which is called the *wide-swing cascode current mirror*.

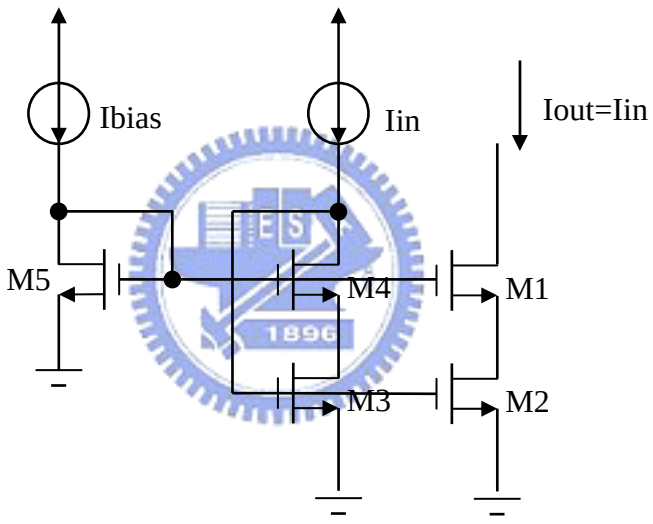


Figure 3.11 Wide-swing cascode current mirror

The basic idea of this current mirror is to bias the drain-source voltages of transistors M2 and M3 to be close to the minimum possible without going into the triode region. Note that the transistor pair M3, M4 acts like a single diode-connected transistor in creating the gate-source voltage for M3. The reason for including M4 is to lower the drain-source voltage of M3 so that it is matched to the drain-source voltage of M2. This matching makes Iout more accurately match Iin.

To determine the bias voltages for this circuit, we have

$$V_{eff} = V_{eff\ 2} = V_{eff\ 3} = \sqrt{\frac{2I_{D\ 2}}{\mu_n C_{ox}\frac{W}{L}}} \quad . \tag{3-12}$$

Furthermore, we let size of M1~M4 be the same and 4 times greater than that of M5, then we have

$$\begin{aligned} V_{eff\ 1} &= V_{eff\ 4} = V_{eff} \\ V_{eff\ 5} &= 2 \cdot V_{eff} \end{aligned} \quad . \tag{3-13}$$

Thus,

$$V_{ds\ 2} = V_{ds\ 3} = V_{gs\ 5} - V_{gs\ 1} = V_{eff} \quad . \tag{3-14}$$

So, M2 and M3 are at the edge of the triode region. Thus, the minimum allowable output voltage is

$$V_{out} > V_{eff\ 1} + V_{eff\ 2} = 2 \cdot V_{eff} \quad . \tag{3-15}$$

According to the two concepts we have introduced, we incorporate wide-swing current mirrors into the constant-transconductance bias circuit. This circuit minimizes most of the second-order imperfections caused by the finite-output impedance of the transistors. Without greatly restricting signal swings. The complete circuit is shown in Figure 3.12.

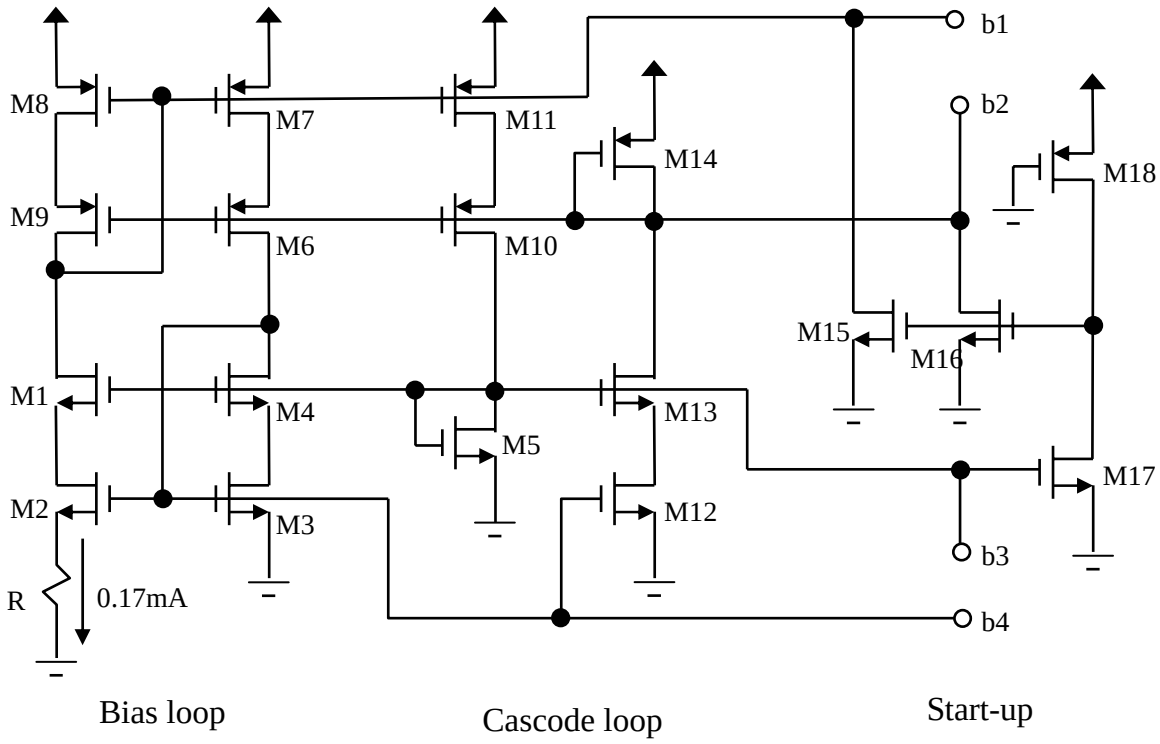


Figure 3.12 Wide-swing constant-transconductance bias circuit

This bias circuit does have the problem that it is possible for the current to be zero in all transistors, and the circuit will remain in the stable state. It is necessary to include *start-up circuitry*. An example of a start-up circuit consisting M15 ~ M18 is shown in Figure 3.12. If all currents in the bias loop are zero, M17 will be off. Since M18 operates as a high-impedance load that is always on, the gate voltages of M15, M16 will be pulled high and these transistors will inject currents into the bias loop. Once the Bias loop starts up, M17 will turn on and then pull the gate voltages of M15, M16 low. Finally, start-up circuitry will be turned off and no longer affects the bias loop.

The simulation result of the whole bias circuit is shown in Figure 3.13. In this figure, we set the initial currents of all transistors are zero. Thus, the initial values of b1, b2 are 1.8 V

and b3, b4 are 0 V. Due to the start-up circuitry, the four bias points will work at normal stable state after 5 nsec.

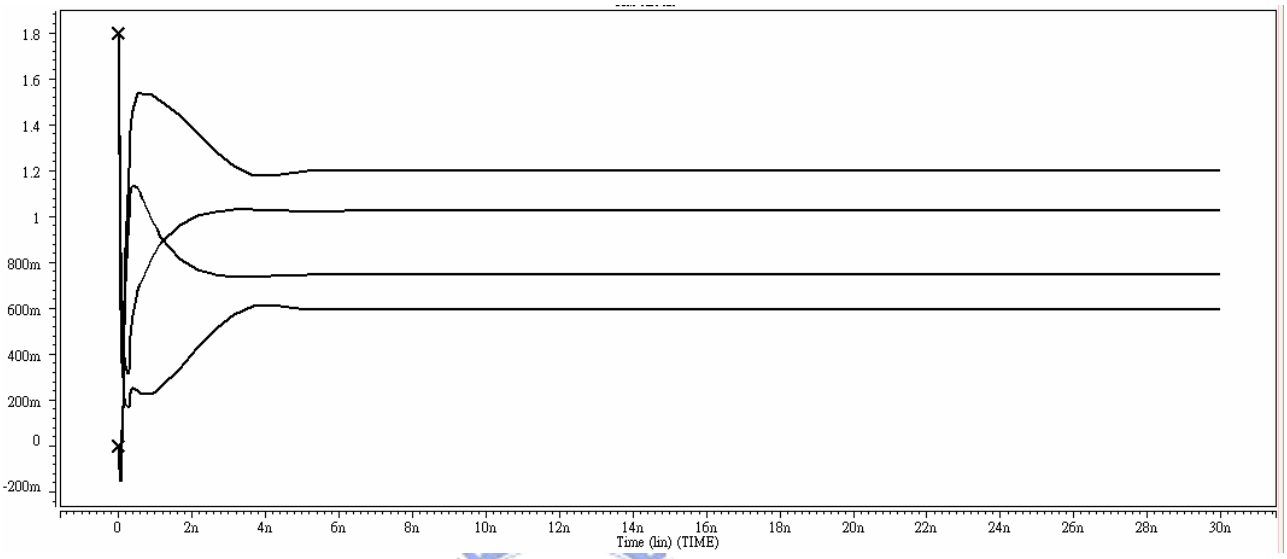


Figure 3.13 Simulation results of the Wide-swing constant-transconductance bias circuit

3.2 SC Low-pass Filter

3.2.1 Resistor Equivalence of a Switched capacitor

Consider the switched-capacitor circuit shown in Figure 3.14. Assuming ϕ_1 and ϕ_2 are two nonoverlapping clocks. C is charged to V1 and then V2 during each clock period. Therefore, the change in charge over one clock period is given by

$$\Delta Q = C(V_1 - V_2) \quad . \tag{3-16}$$

Then, we can also find the equivalent average current over one clock period is given by

$$I_{avg} = \frac{C(V_1 - V_2)}{T} \quad , \tag{3-17}$$

where T is the clock period. Finally, we see the equivalent resistor of the switched capacitor in Figure 3.14 over one clock period is given by

$$R_{eq} = \frac{V_1 - V_2}{I_{eq}} = \frac{T}{C} = \frac{1}{C \cdot f_s} \quad , \tag{3-18}$$

where fs is the sampling frequency.

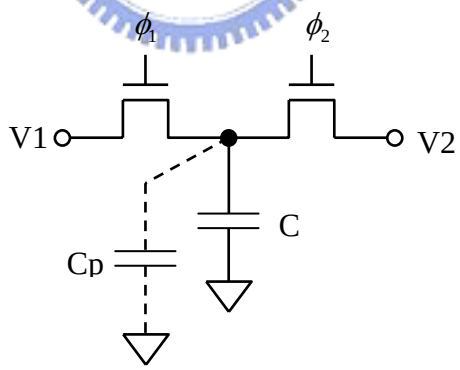


Figure 3.14 SC resistor

In Figure 3.14, we ignore the effect of the parasitic capacitors. Here, Cp represents the parasitic capacitor of the top plate of C as well as the nonlinear capacitors associated with the two switches. It is in parallel with C and therefore cause gain error of the circuit transfer function. To overcome this drawback, parasitic-insensitive structures have been developed to

realize high accuracy. Figure 3.15(a) is a parasitic-insensitive resistor equivalence of switched capacitor in positive type and Figure 3.15(b) is the negative one.

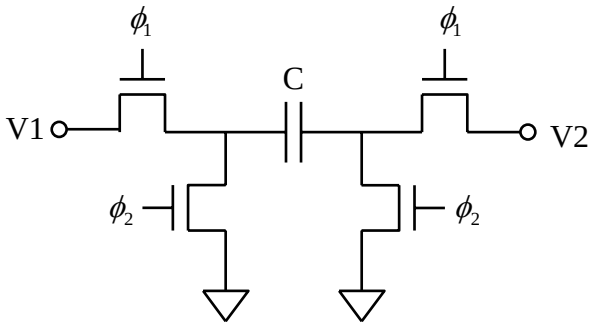


Figure 3.15 (a) Positive parasitic-insensitive SC resistor

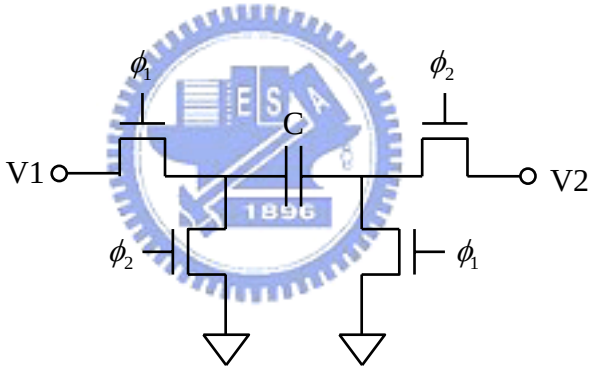


Figure 3.15 (b) Negative parasitic-insensitive SC resistor

3.2.2 Signal-flow-graph Analysis of Low-pass Biquad Filter

The transfer function of typical continuous-time biquad filters are given by

$$H(s) \equiv \frac{V_o(s)}{V_i(s)} = -\frac{k_0}{s^2 + (\frac{\omega_0}{Q}) \cdot s + \omega_0^2} \quad , \tag{3-19}$$

where ω_0 represents the corner frequency and Q is called *Q factor*. Signal-flow-graph is shown in Figure 3.16.

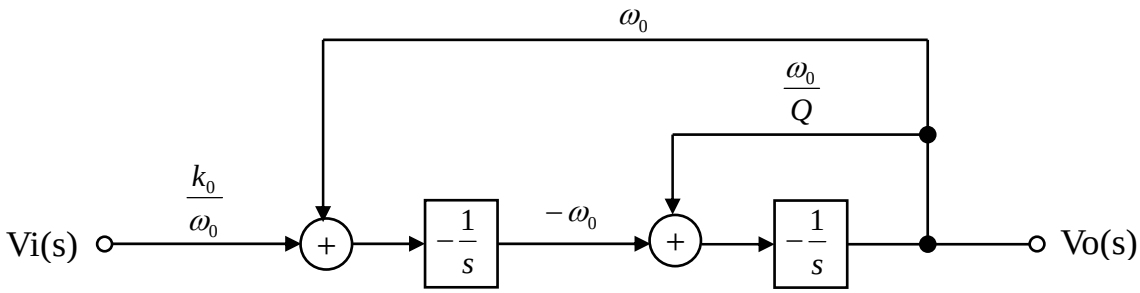


Figure 3.16 Signal-flow-graph of continuous-time biquad filter

We can transfer the signal-flow-graph from S-domain (Figure 3.16) into Z-domain (Figure 3.17) for discrete-time biquad filters, and according to Figure 3.17, the transfer function of the discrete-time biquad filters, H(z), are found to be

$$H(z) \equiv \frac{V_o(z)}{V_i(z)} = -\frac{K_1 K_3 \cdot z}{(1+K_4)\cdot z^2 + (K_2 K_3 - K_4 - 2)\cdot z + 1} \qquad (3\text{-}20)$$

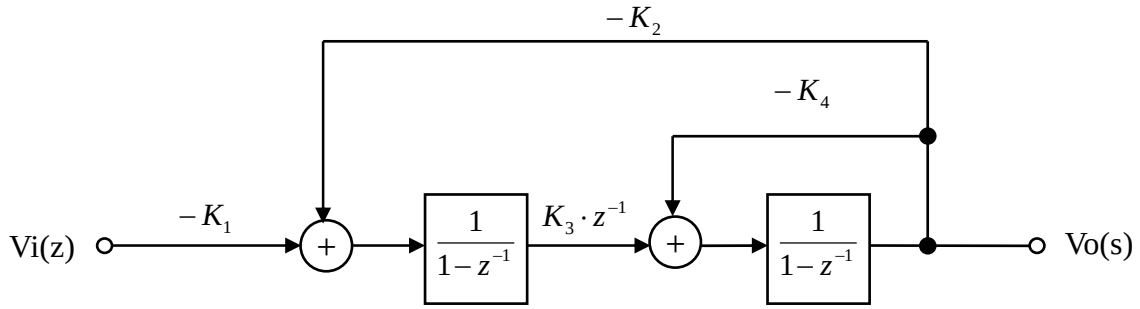


Figure 3.17 Signal-flow-graph of discrete-time biquad filter

Finally, comparing Figure 3.16 and Figure 3.17 we can find the approximations for feedback capacitor ratios are given by

$$K_2 \approx K_3 \approx \omega_0 T \quad . \tag{3-21}$$

$$K_4 \approx \frac{\omega_0 T}{Q} \quad . \tag{3-22}$$

$$K_1 \approx (\text{DC gain}) \cdot K_2 \quad . \tag{3-23}$$

A switched-capacitor low-pass biquad filter based on Z-domain signal-flow-graph is shown in Figure 3.18. Note that this SC biquad filter has redundant switches, as switch sharing has not yet been applied.

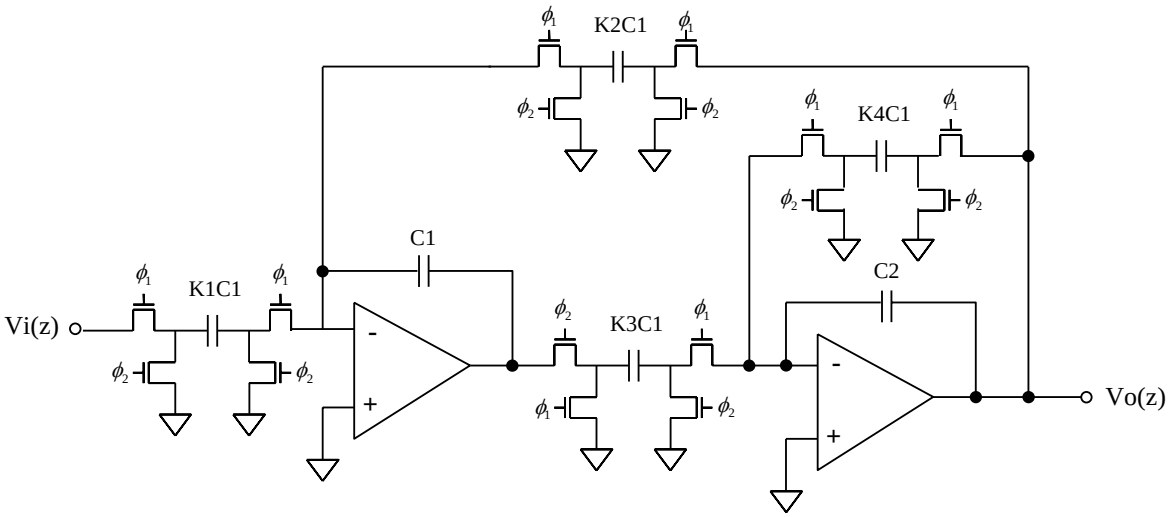


Figure 3.18 Switched-capacitor Low-pass biquad filter

In this thesis, we set $\omega_0 T = 0.45$ and sampling frequency to be 140 MHz due to limitation of the opamp bandwidth, so corner frequency of the biquad filter will be 10 MHz. We also set Q factor and DC gain of the biquad filter to be unity. Then, we can see all capacitor values of the biquad filters shown in Table 3.5.

C1	C2	K1C1	K2C2	K3C2	K4C2
1.5 pF	1.5 pF	0.675 pF	0.675 pF	0.675 pF	0.675 pF

Table 3.3 Capacitor values of the biquad filter

3.2.3 Switches

The requirements for switches used in SC filters must have a very high off resistance, a relatively low in resistance, and no offset voltage when it turns on. In today's CMOS technology, using of MOSFET transistors as switches satisfies these requirements.

MOS switches consist of NMOS, PMOS and CMOS switches, like Figure 3.19 shows. NMOS switches are applicable for low voltage range and PMOS switches are applicable for high. However, CMOS switches combine the advantages of both ones. It can work for full range. Figure 3.20 shows method to simulate the turn-on resistance of MOS switches [11]. We use AC current as input signal and then obtain drain-source voltage of the switch as output signal. Inductors in this figure are used to make sure that AC signals only pass through MOS switches. Therefore, turn-on resistance of the switch is given by

$$R_{on} = R_{onN} \;//\; R_{onP} = \frac{V_{out}}{I_{in}} \quad . \tag{3-24}$$

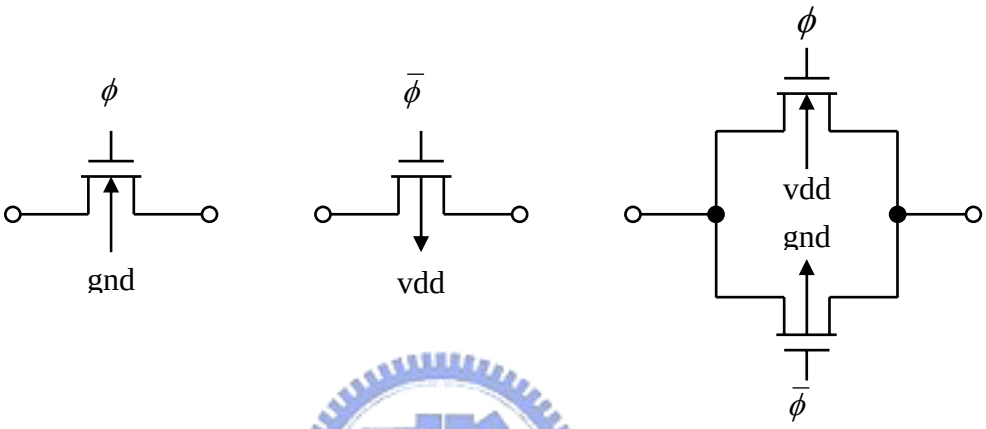


Figure 3.19 3 types of MOS switches

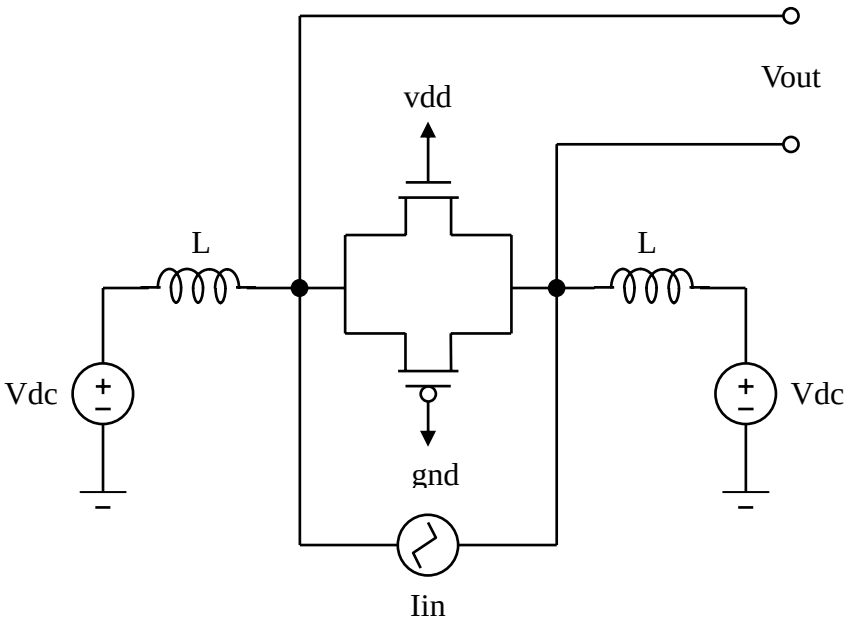


Figure 3.20 Turn-on resistance simulation method

Figure 3.21 is the CMOS switches turn-on resistance simulation results. Different figures represent different ratios between NMOS sizes and PMOS sizes. We simulate overall four kinds of ratios that NMOS sizes over PMOS sizes are 1/2, 1/3, 1/4 and 1/5. In these simulation results we find that when NMOS size over PMOS size is 1/4, the turn-on resistance of CMOS switches is mostly like constant. Besides, we also see that larger sizes bring lower turn-on resistances. However, we have to consider non-ideal effects of MOS switches such as charge-injection and clock-feedthrough, which introduce errors proportional to the switch sizes when we design MOS switches. Therefore, determination of MOS switch sizes is a trade-off between turn-on resistance and non-ideal error.

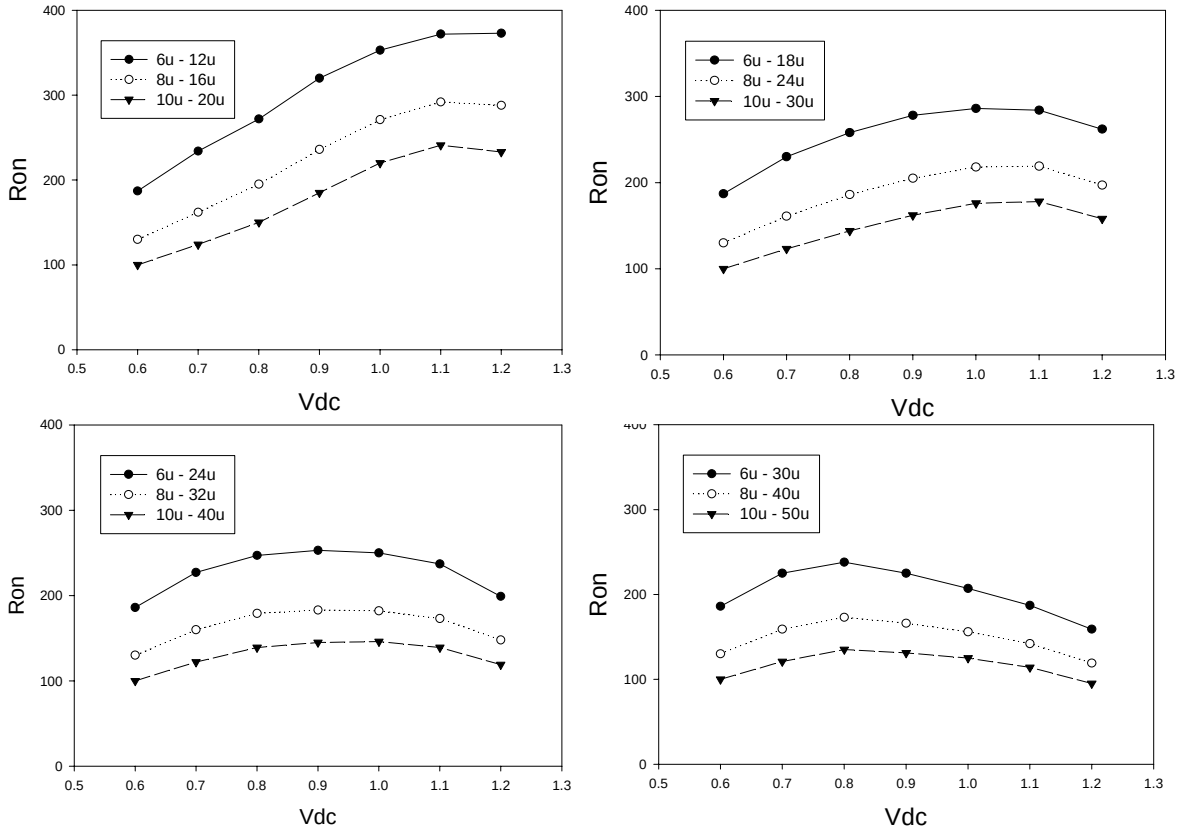


Figure 3.21 CMOS switch turn-on resistance simulation results

Non-ideal effects of MOS switches are the major limitation on resolution of SC circuits. They cause error due to unwanted charges being injected into the circuit when switches turn off. Non-ideal effects include two types called *charge injection* and *clock feedthrough*. We have more detail analysis of these two effects in Figure 3.22 and next description.

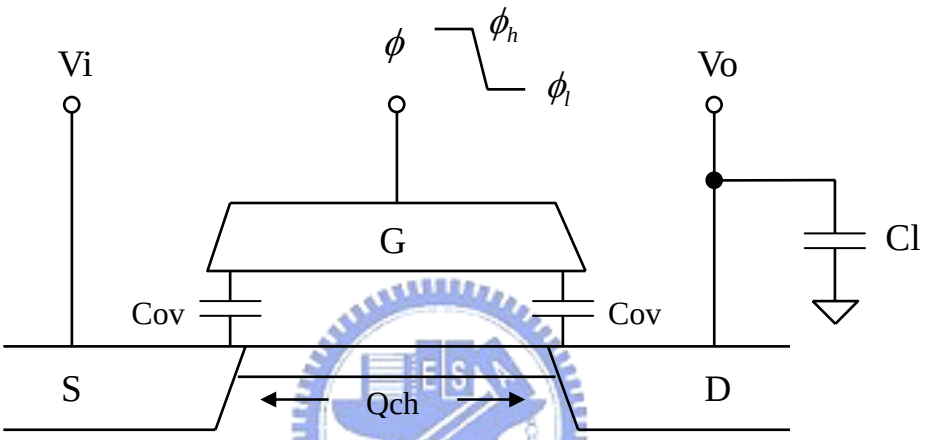


Figure 3.22 Non-ideal effects of MOS switches

(1) Charge Injection: Charge injection occurs by channel charge when MOS switches turn off. From Figure 3.22 we can see the channel charge flow out from the channel region of the transistor to the drain and source junctions. The channel charge of a transistor had zero drain-source voltage is given by

$$Q_{ch} = WLC_{ox}V_{eff} = WLC_{ox}(V_{gs} - V_t) \quad . \tag{3-25}$$

And we derive voltage error due to charge injection is given by

$$\Delta V = -\frac{1}{2}Q_{ch} \cdot \frac{1}{C_l + C_{ov}} \approx -\frac{WLC_{ox}(V_{gs} - V_t)}{2C_l} \quad . \tag{3-26}$$

(2) Clock Feedthrough: From Figure 3.22, overlap capacitors between gate and junctions will inject additional charge into circuit when switches turn off, and this effect is called clock feedthrough. Voltage error due to clock feedthrough is given by

$$\Delta V = -(\phi_h - \phi_l) \cdot \frac{C_{ov}}{C_l + C_{ov}} \quad , \tag{3-27}$$

where ϕ_h is V_{DD} and ϕ_l is Gnd.

Due to (3-26) and (3-27) we find that error caused by clock feedthrough is small and signal-independent, which can be eliminated by fully-differential structure. On the other hand, error caused by charge injection is much larger. We also can divide charge injection into two parts, signal-dependent and signal-independent. Switches connected to analog ground and virtual ground will cause signal-independent error because its turn-on voltage is constant. Just like clock feedthrough, we can eliminate this kind of errors duo to fully-differential structure. Besides these, switches connected to the signal will cause signal-dependent error which is changed with signal. Signal-dependent error is important because it truly affects resolution of the circuit. Therefore, How to reduce this kind of errors is the critical issue when we design switches of SC filter. In this thesis, we use three kinds of approaches to reduce charge injection and have description about these approaches as below.

(1) The first approach to lower charge injection effect is incorporating both NMOS and PMOS devices that have same charge amount but opposite direction as a CMOS switch. This approach can make channel charges of two different transistors cancel each other at DC level (no AC signal input).

(2) Using *dummy switches*. As Figure 3.23 shown, a dummy switch (M2) driven by inverse clock is added to the circuit. Therefore, the charge injected by the main switch (M1) can be removed to M2 after M1 turns off and M2 turns on. Note that both source and drain of M2 are connected to the output node and M2 has half size of M1 in order to make $\Delta q_1 = \Delta q_2$.

(3) The third approach is called *bottom-plate sampling*. Here, we take an SC integrator as example. As Figure 3.24 shows, we add a pair of clocks (ϕ_{1a}, ϕ_{2a}) that slightly advance than original clocks (ϕ_1, ϕ_2). When M1 turns off, the injected charge Δq_1 will not cause any change in the charge stored in Cl since M2 has already turned off and the right side of C1 is connected to an effective open circuit. Therefore, by this approach, the circuit is affected only by M2 and M4 which are connected to virtual ground or analog ground. Charges injected by these transistors are signal-independent and be cancelled by fully-differential structure.

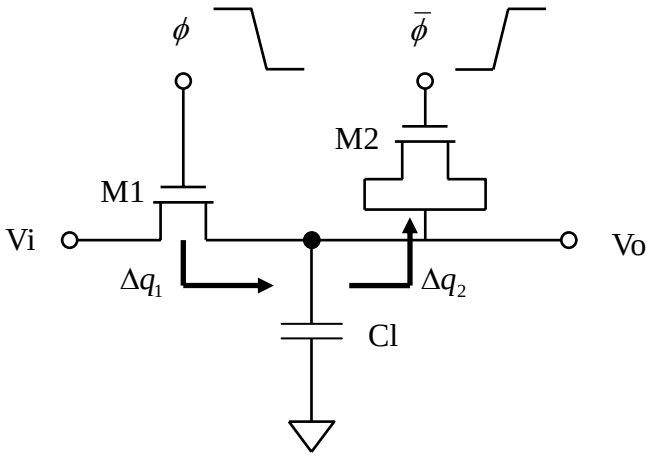


Figure 3.23 Addition the dummy switch to reduce charge injection

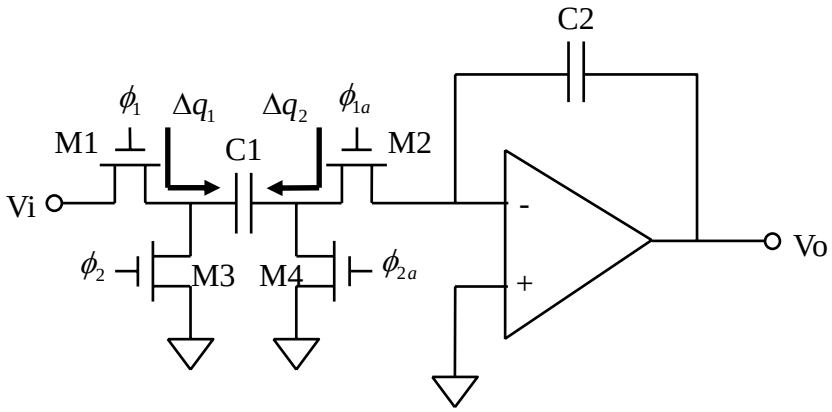


Figure 3.24 SC integrator with bottom-plate sampling

Due to concepts of turn-on resistance and charge injection cancellation we have described, now we can determine the sizes of MOS switches.

At beginning, we take a biquad filter as two first-order system with a single delay around the loop due to the negative SC resistor. And the output error of an ideal first-order system is given by

$$V_e(t) = e^{-\frac{t_s}{\tau}}, \tag{3-28}$$

where τ is RC time constant of the first-order system and t_s is settling time of the first-order system. Assuming the circuit has N bits resolution, then (3-28) can be rewritten as

$$e^{-\frac{t_s}{\tau}} \le \frac{1}{2^{N+1}} \quad . \tag{3-29}$$

We set capacitance loading as 2 pF, settling time as half of clock period and resolution as 8 bits, then we can obtain the term of turn-on resistance limitation given by

$$R_{on} \le \frac{t_s}{(N+1)\cdot \ln 2 \cdot C_l} = \frac{3.57n}{9\cdot \ln 2 \cdot 2p} \approx 0.28K \quad . \tag{3-30}$$

Due to (3-30) we can determine the size of NMOS switches. As for CMOS switches, we still have to consider the size ratio between NMOS and PMOS.

How to determine the ratio? First of all, we recall that the equation of transistor current versus voltage at triode region is given by

$$I_d = \mu C_{ox}(\frac{W}{L})[(V_{gs} - V_t)\cdot V_{ds} - \frac{1}{2}V_{ds}^2] \quad . \tag{3-31}$$

And then turn-on resistance of MOS switches is given by

$$R_{on} = (\frac{\partial I_d}{\partial V_{ds}})^{-1} = \frac{1}{\mu C_{ox}(\frac{W}{L})\cdot V_{eff}} . \tag{3-32}$$

Due to (3-25), (3-32) and MOS parameters such as mobility and threshold voltage, the optimize size ratio between NMOS and PMOS of a CMOS switch can be derived as below.

First, we set R_{on} of NMOS to be equal to that of PMOS, then we obtain

$$\frac{R_{on(n)}}{R_{on(p)}} = 1 = \frac{\mu_p C_{ox}(W_p / L_p)V_{ov(p)}}{\mu_n C_{ox}(W_n / L_n)V_{ov(n)}} \quad . \tag{3-33}$$

(3-33) can be rewritten as

$$\frac{(W_p / L_p)}{(W_n / L_n)} \cong 4.23 \quad . \tag{3-34}$$

(3-34) shows the computing result is fit in with the simulation result in Figure (3-21).

Second, to reduce charge injection effect, we set channel charge of NMOS and PMOS are the same. Then we get

$$\frac{V_{\text{ch(n)}}}{V_{\text{ch(p)}}} = 1 = \frac{W_n L_n \cdot C_{ox} \cdot V_{ov(n)}}{W_p L_p \cdot C_{ox} \cdot V_{ov(p)}} \quad . \tag{3-35}$$

(3-35) can be rewritten as

$$\frac{W_n \cdot L_n}{W_p \cdot L_p} \cong 0.73 \quad . \tag{3-36}$$

Due to (3-34) and (3-36), ratios of channel width and length between NMOS and PMOS are given by

$$\frac{L_n}{L_p} = 1.77 \quad , \quad \frac{W_n}{W_p} = 0.42 \quad . \tag{3-37}$$

Finally, according to (3-30) and (3-37), we can determine the sizes of CMOS switches**.**

3.2.4 Nonoverlapping Clocks

Clocks determine when charge transfers occur and they must be nonoverlapping in order to guarantee charge is not lost. One simple approach for generating nonoverlapping clocks is shown in Figure 3.25. Here, delay blocks are used to ensure clocks are nonoverlapping with each other.

Figure 3.26 is the output buffer of nonoverlapping clocks to generate the final clock and its inverse clock applied for the SC filter. The transmission gates are used to match the clock and its inverse clock. Figure 3.27 shows the complete circuit of the clock driver. Because of bottom-plate sampling, we need two pairs of nonoverlapping clocks.

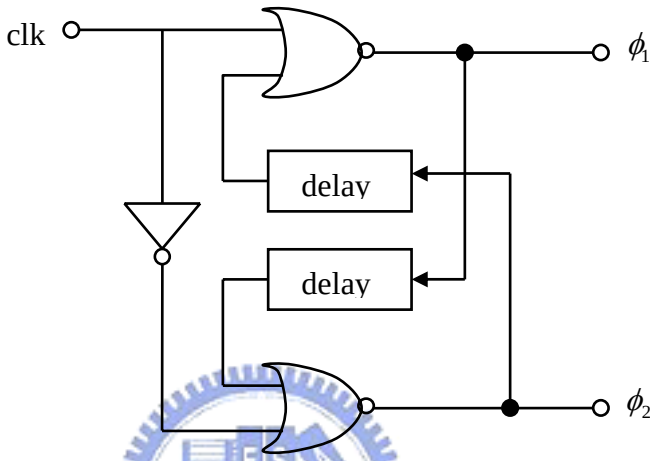


Figure 3.25 Circuit implementation of nonoverlapping clocks

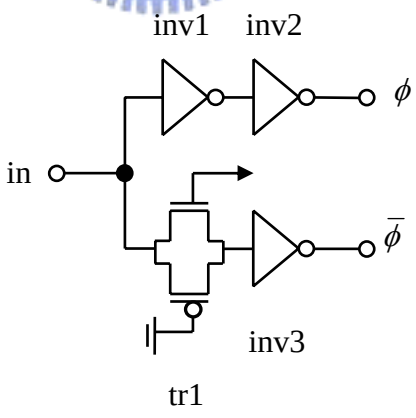


Figure 3.26 Output buffer of nonoverlapping clocks

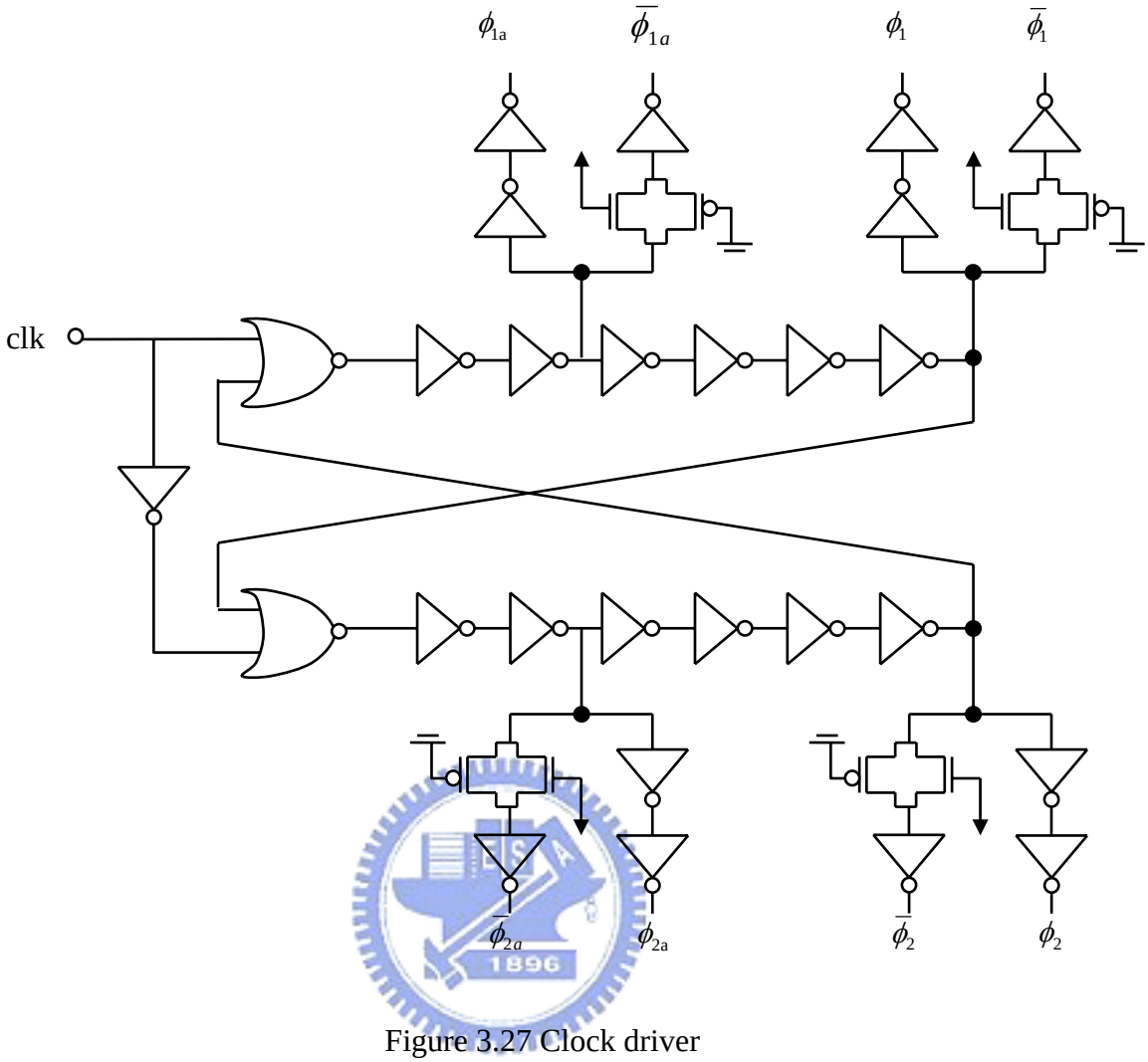


Figure 3.27 Clock driver

3.2.5 Simulation Results of the SC Low-pass Filter

Figure 3.28 shows the low-pass biquad filter circuit structure. Some redundant switches are removed due to the concept of switch sharing. Switches that connected to analog ground or virtual ground will be implemented with NMOS switches because they are always working at 0.9V when turn on. Other switches connected to the signal will be implemented with CMOS switches for working at wide range. Capacitor values have been already introduced in Table 3.5.

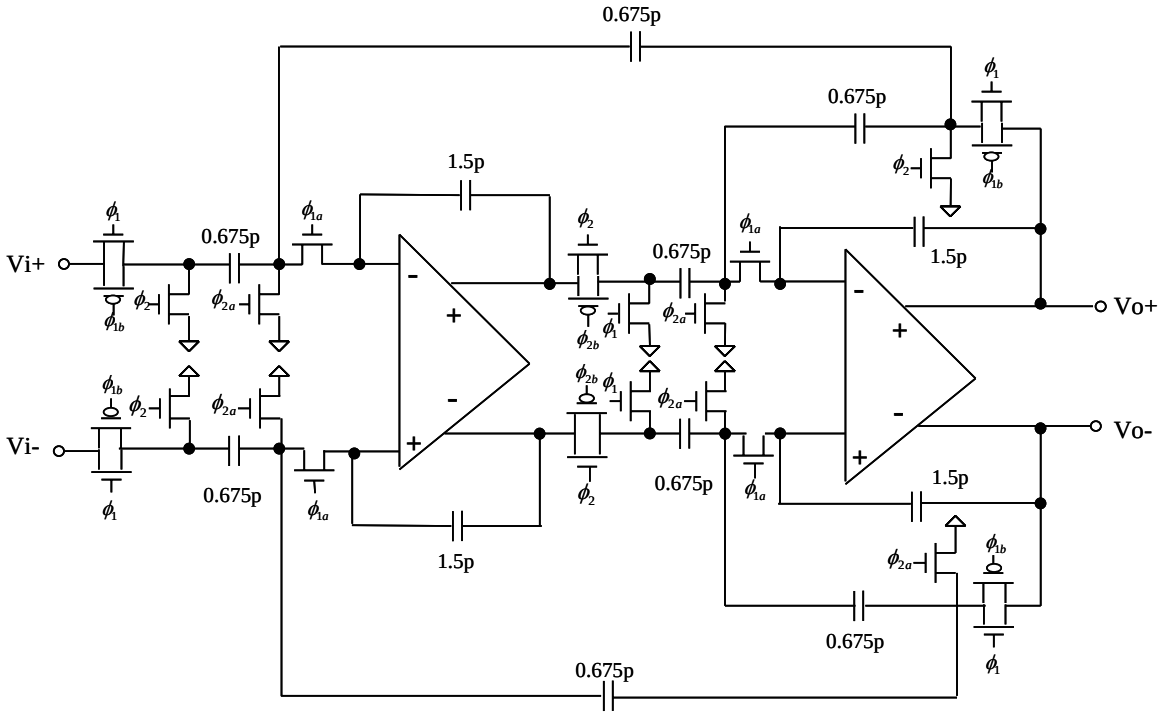


Figure 3.28 Fully-differential low-pass biquad

Finally, we implement a fully differential, high bandwidth, 4th-order SC low-pass filter due to two cascading biquad. Figure 3.29 is the frequency response simulation results. In this figure, we see that pre-layout simulation results are very close to post-layout simulation results, and maximum error between ideal filter and the SC filter is 0.8dB at 8 MHz.

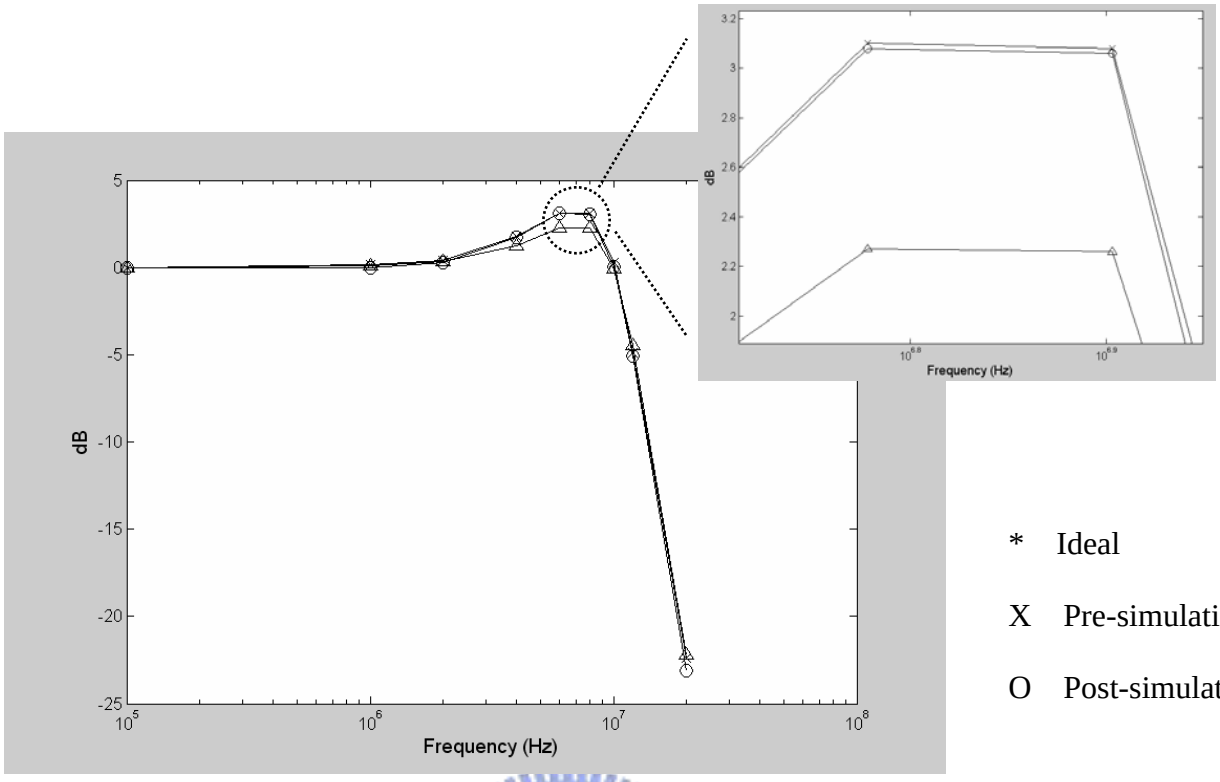


Figure 3.29 Frequency response simulation results

Figure 3.30 shows the harmonic distortion simulation results of the SC filter. The input single tone is at about 1/3 of the corner frequency in order to capture the worst case for the dominant third harmonic [12]. In this figure, we see the maximum harmonic distortion is -43 dB at corner frequency. Finally, we list specifications of the fully-differential, high bandwidth, 4^{th}-order SC low-pass filter in Table 3.4.

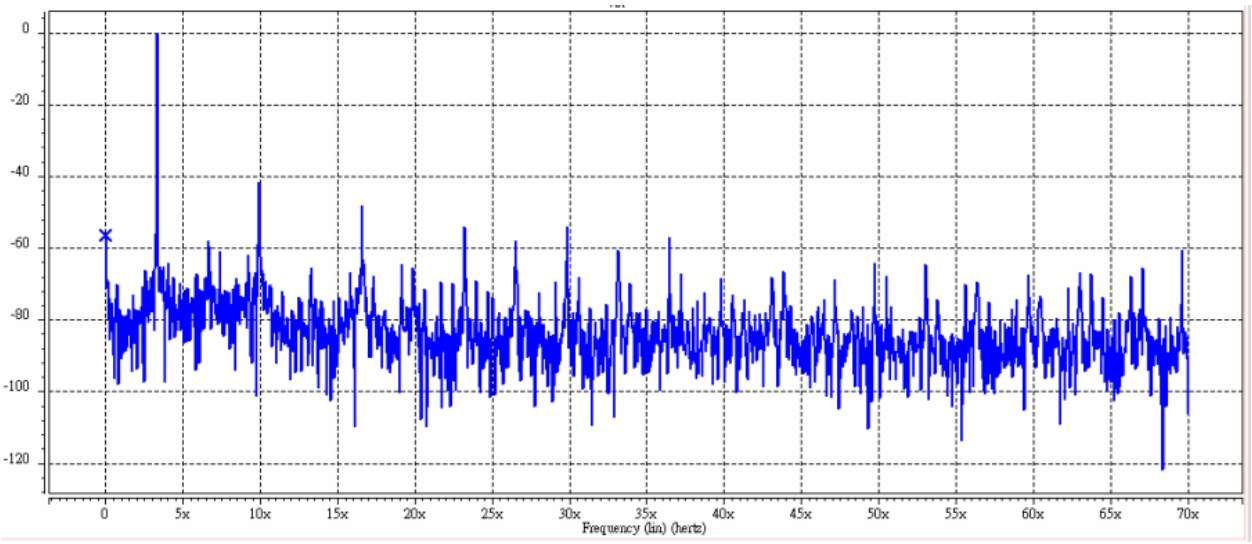


Figure 3.30 Harmonic distortion simulation result

Sampling Frequency	140 MHz
Corner Frequency	10 MHz
DC Gain	1
$\omega_0 T$	0.45
Q Factor	1
CM Voltage	0.9 V
Signal Range	0.65 V ~ 1.15 V
Max. Harmonic Distortion	-43 dB

Table 3.4 Specifications summary of the fully differential, high bandwidth, 4th-order SC low-pass filter

Chapter 4

Built-in-self-test Circuit

How to achieve on-chip test function of SC filters with limited area and power overhead is the critical issue for mixed-signal testing designers. It is also the top target of this thesis. Test concept and method we adopted have already been introduced in Chapter 2, section 3. In this chapter, we will describe how to transfer the ideas into the hardware circuits. The circuit implementation will include a triangular-wave oscillator to take as *test-waveform-generator* (TWG), a differential-to-single-ended circuit with a dual-comparator to take as *output response analyzer* (ORA). The triangular-wave oscillates at 29.2 KHz. We determine a very low frequency here in order to increase accuracy of the triangular-wave itself and linearity of the core circuit (SC filter) output response.

In the last section of this chapter, we will introduce layout considerations of the SC filter and the BIST circuit. Total area of the chip is 1.65(mm)*1.3(mm) and total power is 72 mW.

4.1 Test-waveform-generator

Figure 4.1 shows a pair of differential triangular-waves. In this figure, we see some critical specifications to adjust the performance of differential triangular-waves are:

(1) Amplitude (Va): voltage amplitude error of the triangular-wave will cause error of signal swing. Here, we use a pair of dual-comparator to take as the amplitude judgment device. Oscillation frequency of the triangular-wave is very low to reduce the comparator offset voltage.

(2) Phase shift ($\Delta\phi$): Phase shift between each of the triangular-waves will also affect precision of the test result. To minimize the phase shift error, we use only one corner-judgment circuit for the differential triangular-waves.

(3) Common-mode (CM): common-mode voltage of the differential signals is also a key-point. In this thesis, we add *common-mode feedback* (CMFB) circuit into the triangular-wave oscillator in order to control the common-mode voltage and protect it from the noise affection.

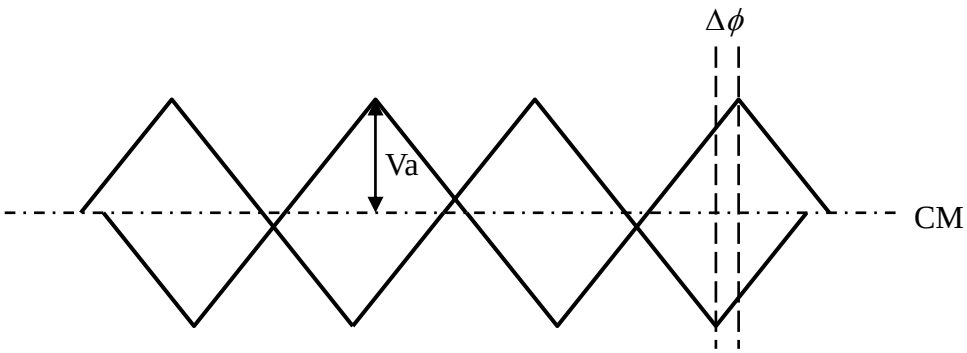


Figure 4.1 Differential triangular-wave

4.1.1 Triangular-wave Oscillator

The traditional circuit of the triangular-wave oscillator is based on an integrator with a bistable circuit to be the triangular-wave corner-judgment circuit. Like Figure 4.2 shows, a RC integrator with square-wave input signal will generate triangular-wave at output node. The amplitude of the triangular-wave is determined by the bistable circuit. If the output voltage of the bistable circuit is high, the triangular-wave will change linearly from high voltage to low voltage .When triangular-wave goes down to the low threshold voltage of the bistable circuit, the bistable circuit will be triggered and output voltage will become low. Therefore, the triangular-wave will generate a corner and begin to go to high voltage.

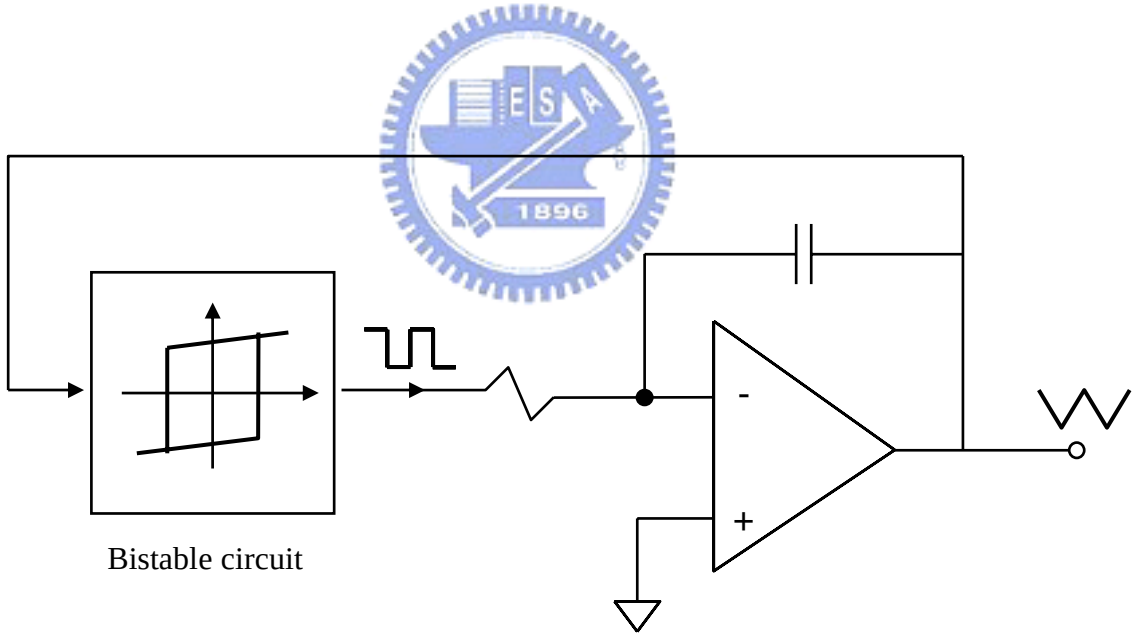


Figure 4.2 Traditional triangular-wave oscillator

However, there are some drawbacks in this approach. First, RC time-constant has bad precision with unpredictable process error. Second, the bistable circuit is complex to design, and precision of the high and low threshold voltages is also a big problem. Third, high and

low level of the square-wave to be the input signal of the integrator are V_{DD} and gnd. It is not a good approach to take power lines as the reference voltages because there are ±10 mV variations due to the bounding-wire inductance effect.

Figure 4.3 is the structure of the fully-differential triangular-wave oscillator in this thesis. It is also called test-waveform-generator (TWG). Comparing the innovative structure we used to the traditional one, we replace the resistor in Figure 4.2 with switched-capacitor in order to obtain high accuracy coefficient. Besides, we use a pair of dual-comparator and a SR latch to replace the bistable circuit. With the approach we adopted, precision of the triangular-wave amplitude increases greatly. We use only one corner-judgment circuit to control the differential triangular-waves. This approach guarantees the minimum phase error between the differential pair. Finally, we add a common-mode feedback (CMFB) circuit to obtain the robust common-mode voltage.

Because the capacitors Cc1 and Cc2 are very large, unity-gain frequency of the opamp reduces and the sampling frequency should also be lower. We determine the clock frequency for the BIST circuit to be 1/4 of that for the core circuit, which is equal to 35 MHz. Vr+ and Vr- are 1.15 V and 0.65 V. Thus, the amplitude of the triangular-wave is 250 mV and the oscillation frequency is 29.2 KHz.

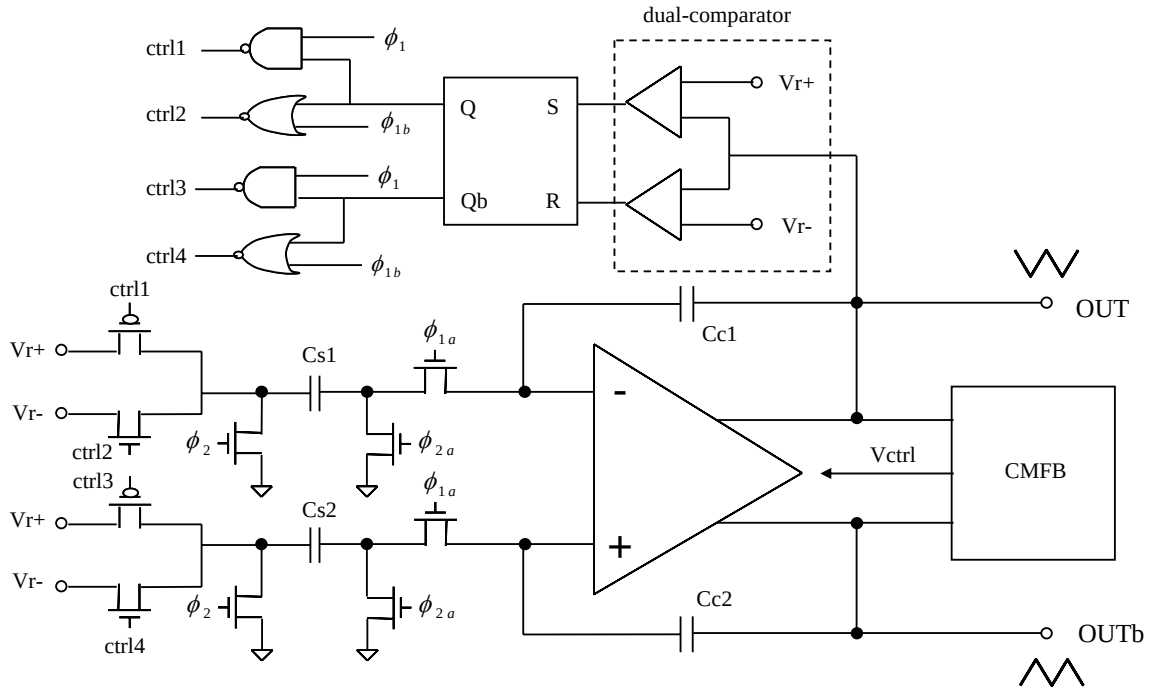


Figure 4.3 Fully-differential triangular-wave oscillator in this thesis (TWG)

4.1.2 CMFB

The CMFB we used here is implemented in SC circuits. Like Figure 4.4 shows, capacitors labeled Cc generate the average output voltages, which are used to create control voltage (Vctrl) for current source of the opamp. The DC voltage across Cc is determined by capacitors Cs, which are switched between bias voltages and in parallel with Cc. The SC CMFB acts like a SC low-pass filter with DC input signal. Cs must be between 1/4 and 1/10 the sizes of Cc. Capacitor values are not critical to circuit perform, but with too small sizes will cause common-mode offset due to charge injection of the MOS switches. All switches are implemented by NMOS except those connected to the outputs (OUT and OUTb), which are realized by CMOS.

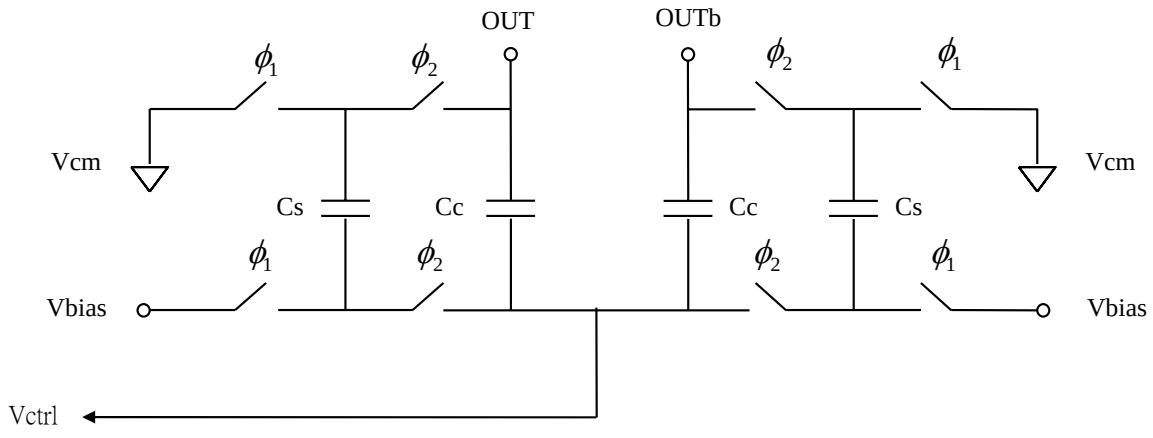


Figure 4.4 CMFB circuit

4.1.3 Simulation Results of TWG

Figure 4.5 is the simulation results of TWG. There are three signal lines in this figure: two of the signal lines are differential triangular-waves and the other one is Vctrl. The differential triangular-waves oscillate between 1.15 V and 0.65 V, and the common-mode voltage is 0.9 V. Vctrl is the ctrl signal of CMFB circuit feedback to the opamp current source. We find that Vctrl changes during a triangular-wave period and it affects the common-mode voltage of the opamp.

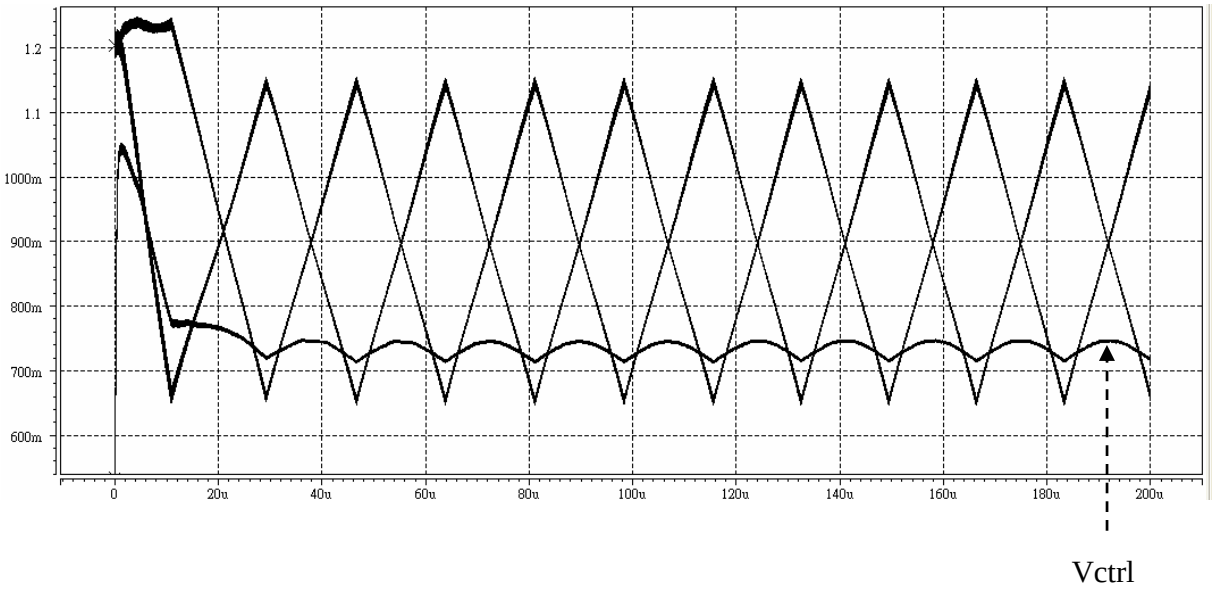
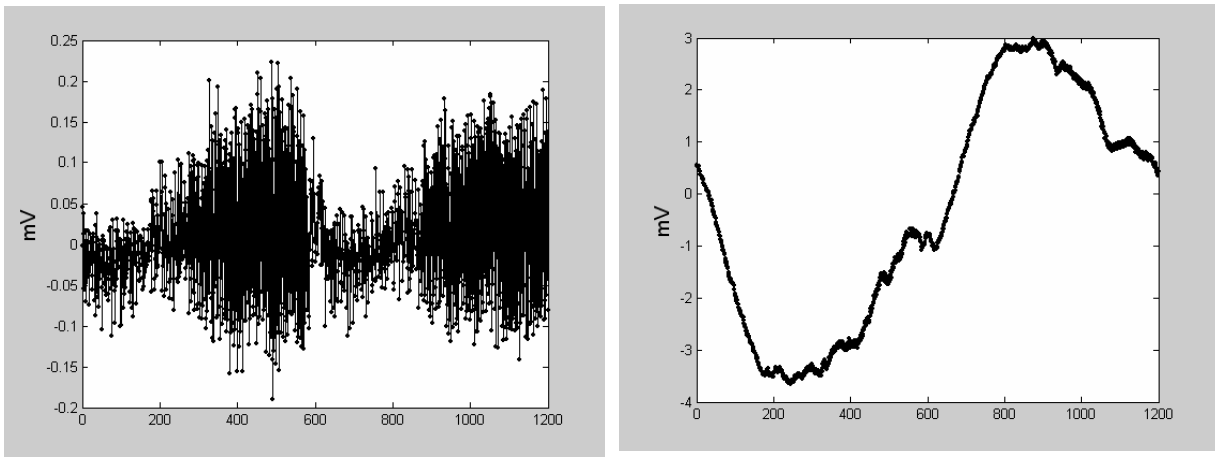


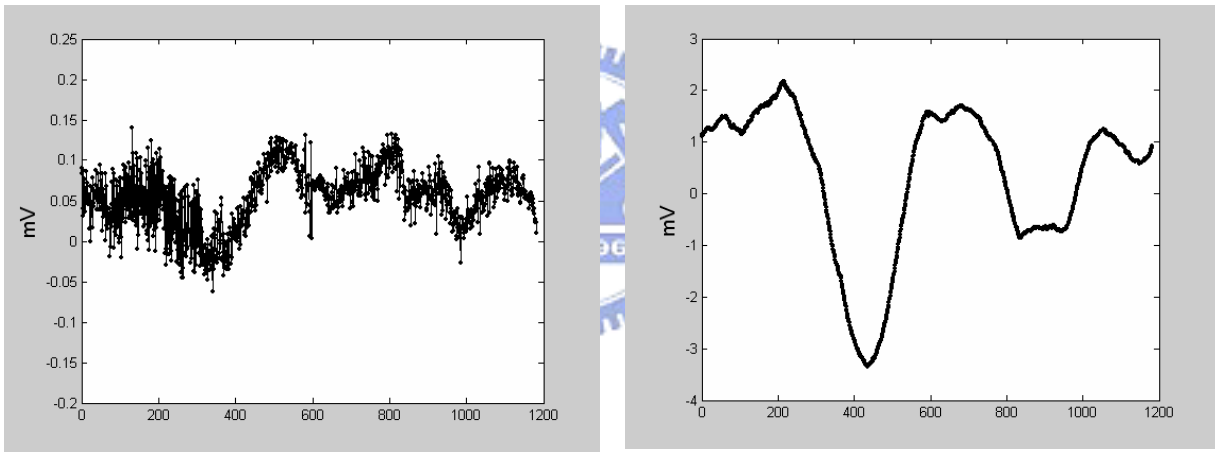
Figure 4.5 TWG simulation result

Figure 4.6 shows INL and DNL of the triangular-wave. We first subtract the differential triangular-waves to each other to obtain the single-ended signal wave. Then, sample voltage values of each test clock period. There are 1200 periods during a triangular-wave period in total. Then, compare the sampling data to the ideal values. Finally, we obtain DNL and INL of the pre-layout simulation result. Figure 4.7 shows DNL and INL of post-layout simulation result with the same method.



DNL INL

Figure 4.6 DNL and INL of TWG (pre-layout simulation)



DNL INL

Figure 4.7 DNL and INL of TWG (post-layout simulation)

From above two figures we see that DNLs of both the triangular-waves are close to perfect. The maximum DNL is only 0.25 mV. On the other hand, INL of the triangular-wave is the critical accuracy limitation. We can see the maximum INL of pre-layout simulation and post-layout simulation is 3.7 mV, which is equal to 7 bits resolution. The main factor of the INL errors is the Vctrl variation during a triangular-wave period. This term introduces common-mode voltage error to the opamp.

4.2 Output-response-analyzer

4.2.1 Dual-comparator

In this thesis, ORA includes a dual-comparator and a differential-to-single-ended circuit. Dual-comparator is implemented due to one N-type and one P-type one-stage amplifier, shown in Figure 4.8. N-type amplifier takes high reference voltage (Vr+) as input and the P-type one takes low reference voltage (Vr-) as input. The output response frequency of SC filter would be very low, so the offset error of the dual-comparator is ignorable.

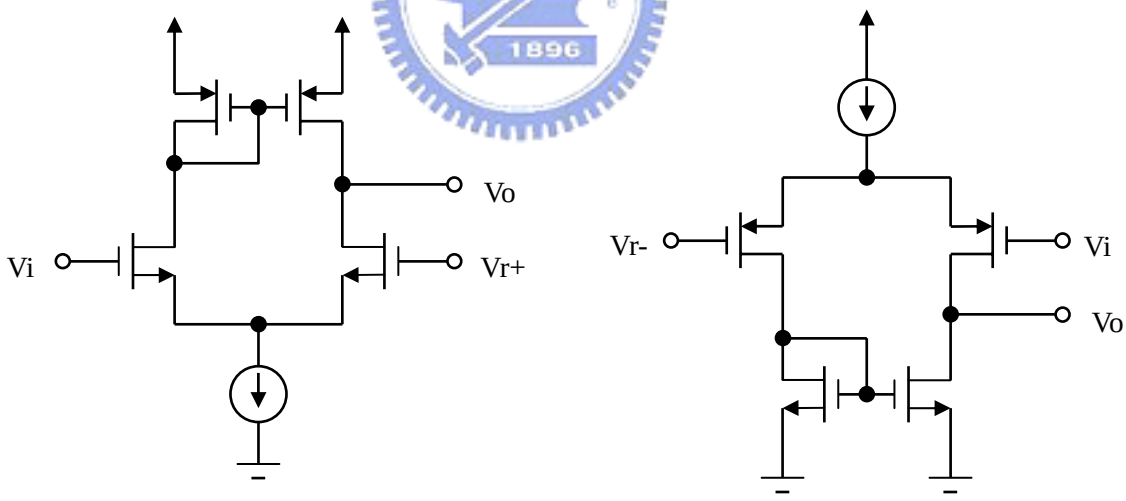


Figure 4.8 Dual-Comparator

Next, we describe the differential-to-single-ended circuit [13]. It is realized by SC circuit, too. It has offset voltage cancellation without requiring the output to slew to ground each time

the amplifier is reset. Except that, it is also insensitive to low opamp gain.

4.2.2 Differential-to-single-ended Circuit

First, Figure 4.9 is a capacitive-reset gain circuit. Capacitor Cd is an optional deglitching capacitor. It is used to provide continuous-time feedback during the nonoverlapping clock times when all switches are turned off. The gain circuit can be either inverting or non-inverting depending on the clock phases of the input stage. To see how this circuit operates, consider during the reset phase of ϕ_2, as shown in Figure 4.10(a). C3 is charged to the output voltage during the previous ϕ_1 phase, so output voltage does not reset to zero during reset phase, which is different from the traditional resettable gain circuit [14]. At this phase C1 and C2 are charged to the input offset voltage of the opamp. The next valid output phase of ϕ_1 is shown in Figure 4.10(b). In this figure we see the output voltage is independent of the offset voltage.

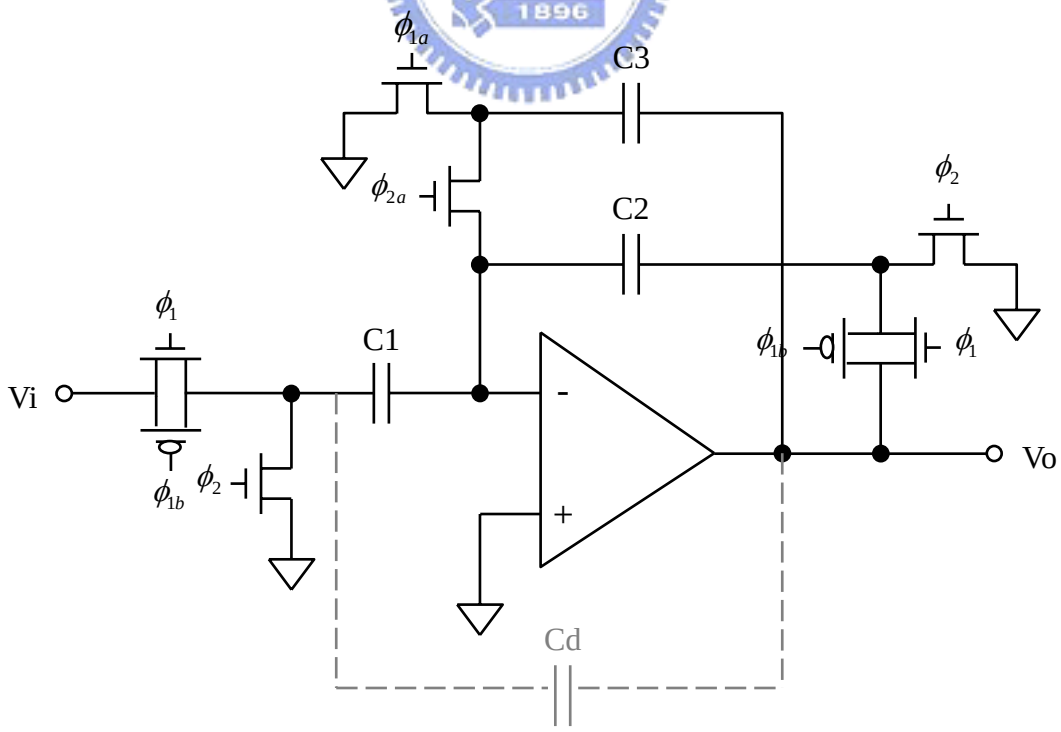


Figure 4.9 Capacitive-reset gain circuit

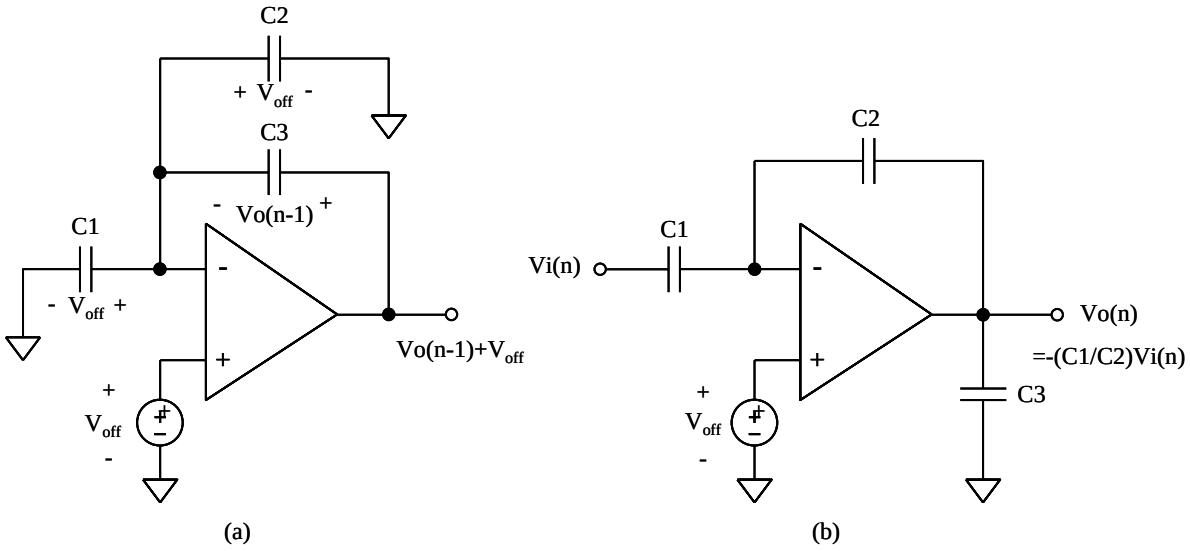


Figure 4.10 Capacitive-reset gain circuit (a) reset phase (b) valid output phase

Figure 4.11 shows complete structure of the differential-to-single-ended circuit. In this circuit, C1 is equal to C2 in order to make the closed-loop gain unity. Besides, switches connected to analog ground and virtual ground are realized by NMOS, others are realized by CMOS for large operating swing. Assuming the opamp has finite open-loop gain A, its transfer function in the z-domain is found to be

$$\frac{V_o(z)}{V_i(z)} = \frac{z^{-1/2} \cdot \frac{C_1}{C_2} a}{1 - bz^{-1}} \quad . \tag{4-1}$$

Where

$$a = \left(\frac{1}{1+\frac{C_1+C_2}{C_2 A}}\right)\left(1-\frac{C_1+C_2}{A\left(C_3+\frac{C_1+C_2+C_3}{A}\right)}\right) \quad . \tag{4-2}$$

and

$$b = \frac{\frac{C_1+C_2}{A}\left(C_2+C_3+\frac{C_1 C_2}{A}\right)}{C_2\left(1+\frac{C_1+C_2}{C_2 A}\right)\left(C_3+\frac{C_1+C_2+C_3}{A}\right)} \quad . \tag{4-3}$$

For low frequency z is approximately equal to unity and (4-1) can be rewritten as

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2}\left(1-\frac{C_1+C_2}{C_2 A^2}\right) \quad . \tag{4-4}$$

From (4-4) we can find the gain error is proportional to A^{-2}, which is much more insensitive to open-loop gain error than the traditional gain circuit.

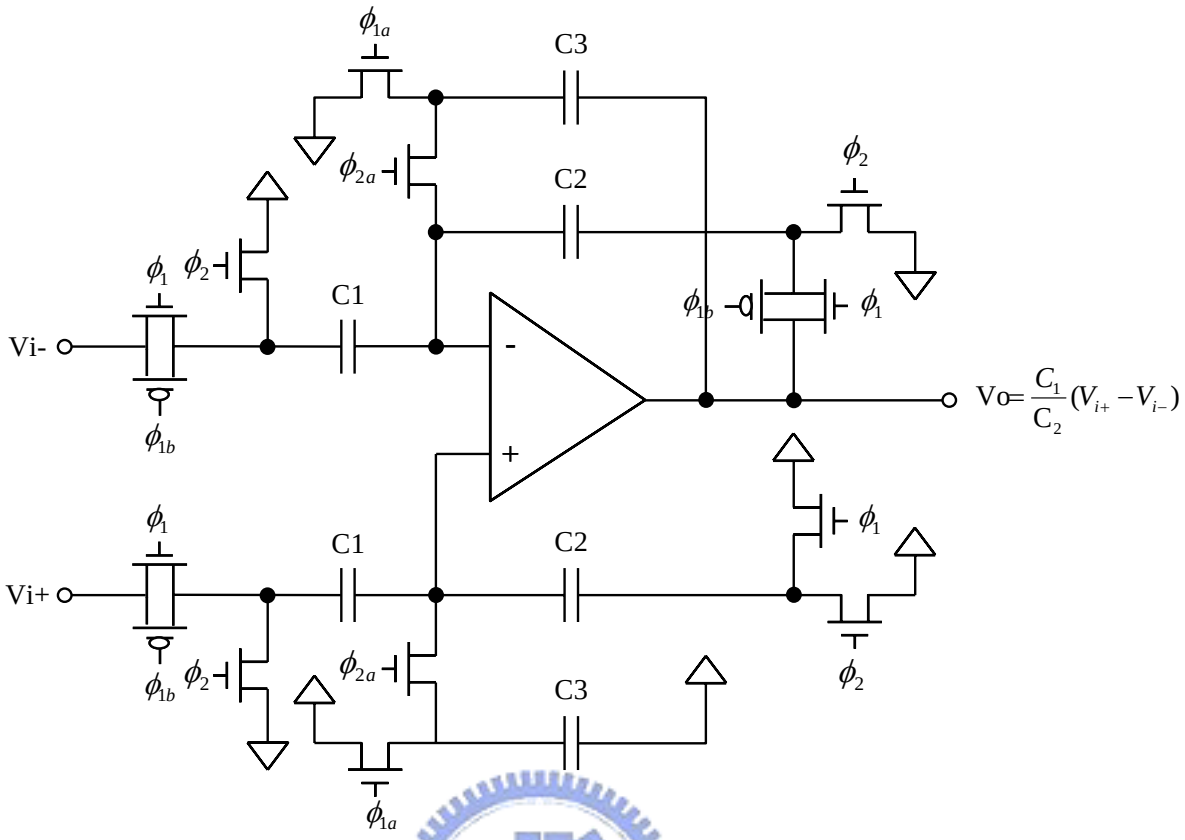


Figure 4.11 Differential-to-single-ended circuit

4.2.3 Simulation Results of the Differential-to-single-ended Circuit

Figure 4.12 is the simulation results when input signal is a pair of differential sine-waves at 1 MHz. The maximum glitch of the output is 100 mV. Figure 4.13(a) and (b) are the DNL and INL analysis results with input signals are differential triangular-waves at 40 KHz. Upper figures of 4.13(a) and (b) are the sampled data of output voltages and lower figures of 4.13(a) and (b) are the DNL and INL results. From these figures we find that the errors increase rapidly when output voltage is close to analog ground because output voltage moves up and down.

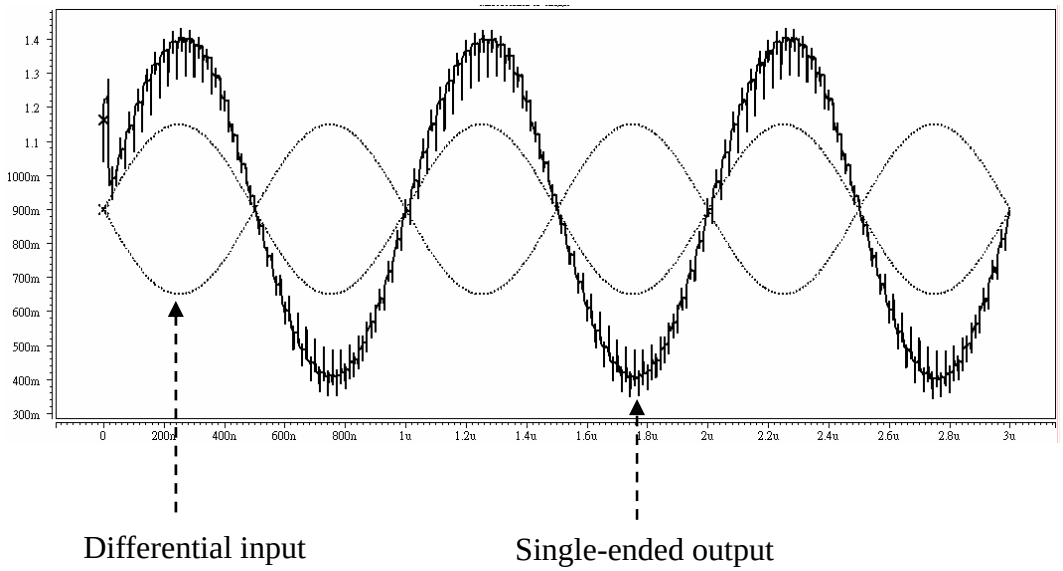
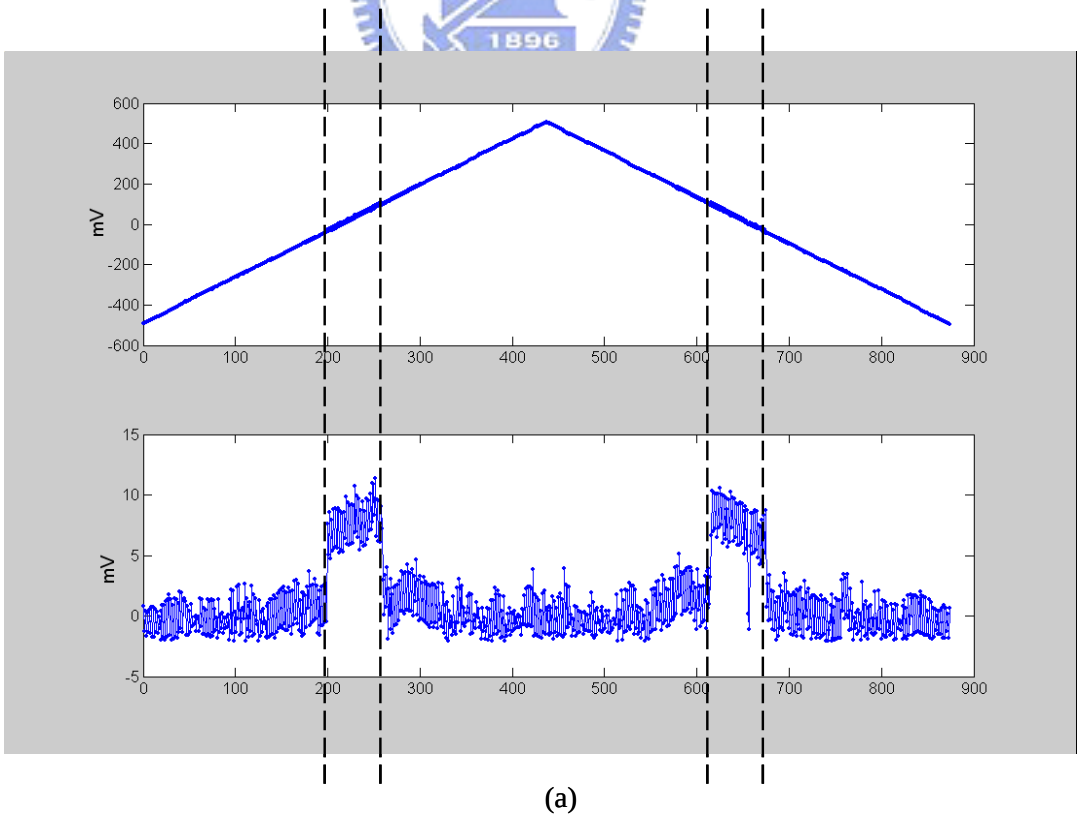
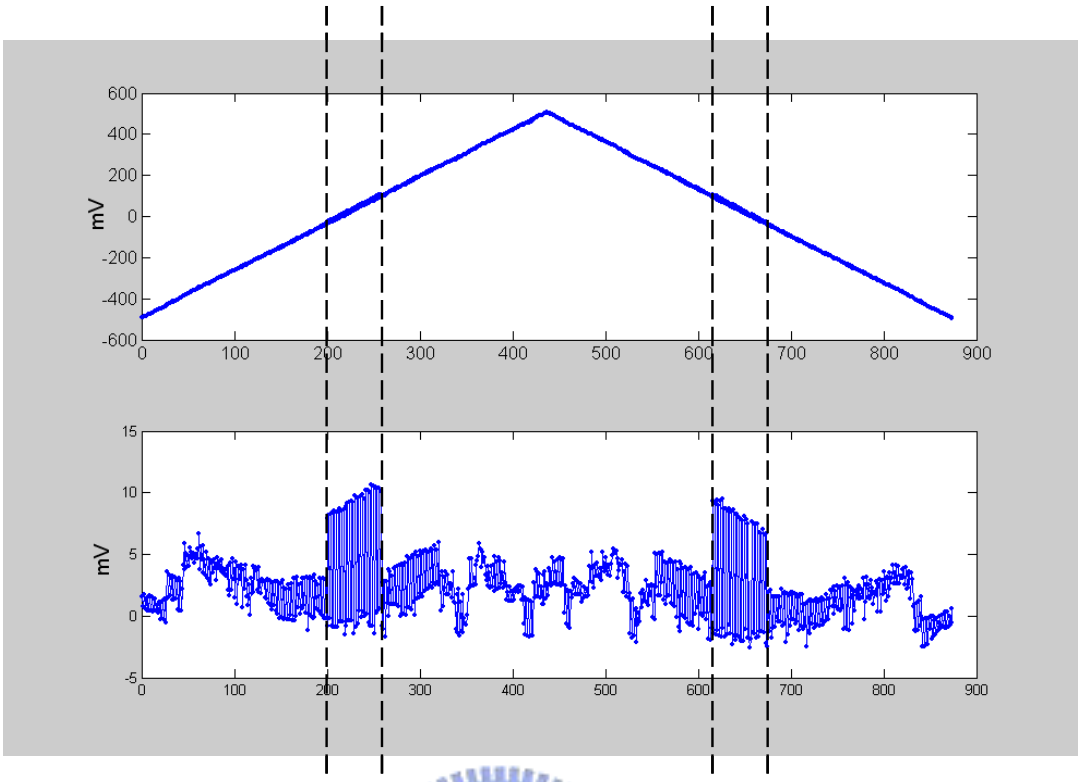


Figure 4.12 Simulation results of the differential-to-single-ended circuit



(a)



(b)

Figure 4.13 (a) DNL and (b) INL results of the differential-to-single-ended circuit

4.3 Top Architecture and Simulation Result

Figure 4.14 is top architecture of the total design. We see that two cascading biquad filters introduced in Chapter 3 are taken as the core circuits. Except that, TWG applies differential test input waveforms for the core circuit, which are connected to aBUS1 and aBUS1b. Differential-to-single-ended circuit and dual-comparator receive the test output responses from one of the biquad filters, which are connected to aBUS2 and aBUS2b. Switches (S0 ~ S3) determine the circuit operating in the normal mode or the test mode, and

these switches are controlled by the test1 and the test2 signals. For example, if {test1, test2} is {0, 0}, the circuit operates in the normal mode. In this case, S0 will turn on and others turn off, differential input signals will from IN and INb transmit to OUT and OUTb through the 4^{th}-order low-pass filter. If {test1, test2} is equal to {1, 0} or {0, 1}, the circuit operates in the test mode. Biquad1 will be taken as core circuit and switches S1 turn on for the case of {1, 0}. Similarly, Biquad2 will be taken as core circuit and switches S2 turn on for the case of {0, 1}. The differential test output responses (aBUS2, aBUS2b) will be transferred into single-ended type (aBUS2s) and be analyzed by the dual-comparator.

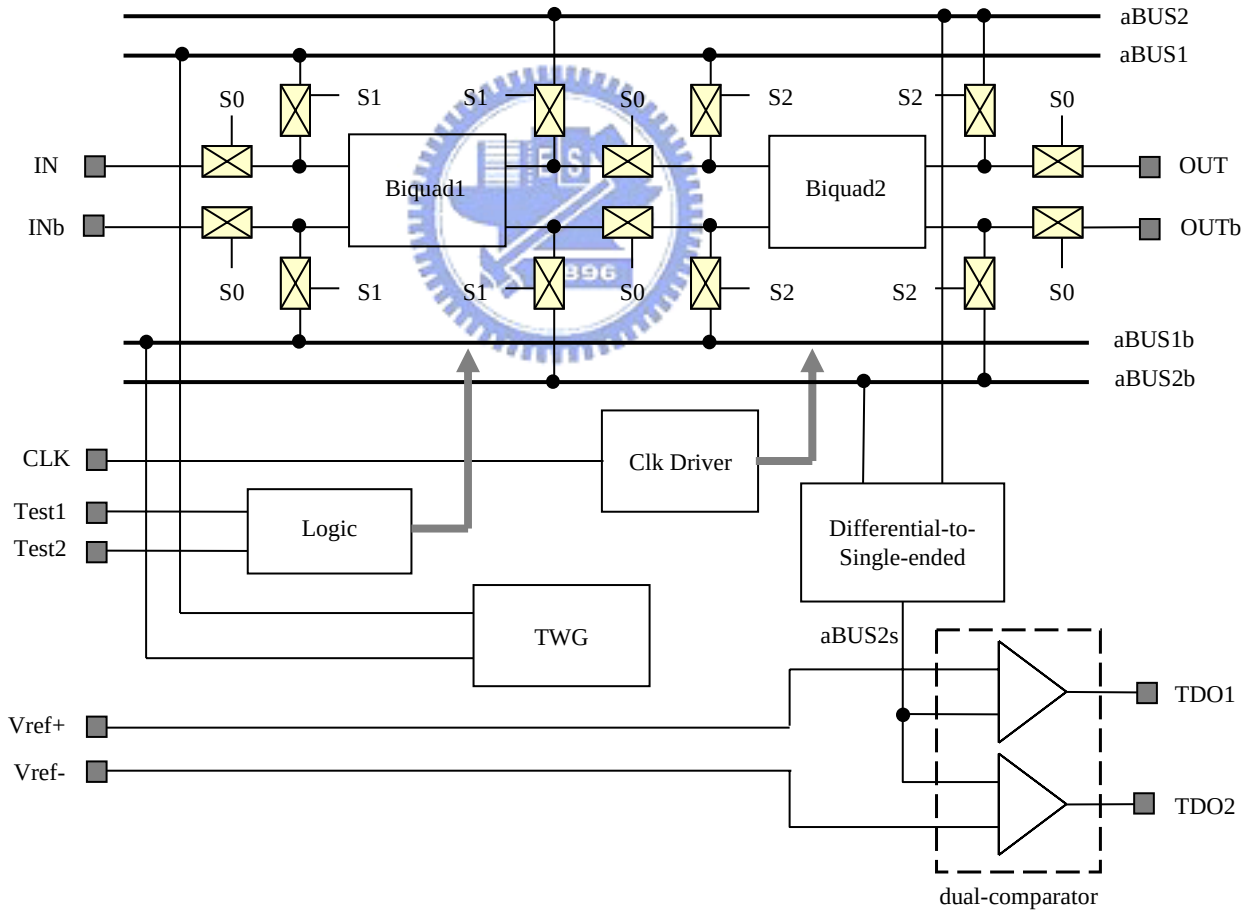
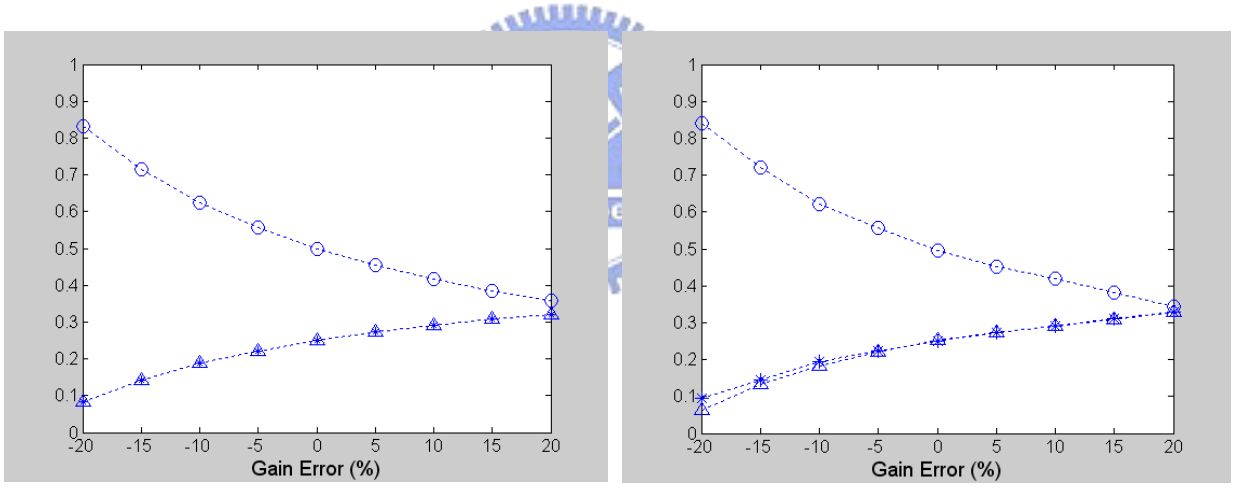


Figure 4.14 Top architecture

We have already described the concept of the test approach and the equation for computing probabilities in Chapter 2. Now, we compare the derived probabilities to the simulation results and discuss the reason of the difference between these two terms.

First, we discuss the case of gain error. We totally compare 9 cases here. Figure 4.15(a) shows the derived probabilities of each case and Figure 4.15(b) shows the BIST circuit simulation results. The unit of X-axis is percentage. Theoretically, S1 should always be equal to S3. However, from Figure 4.15(b), we see the case of -10%, -15% and -20%, the difference between S1 and S3 becomes larger gradually. This is because the triangular-waves itself have offset voltages.



(a)

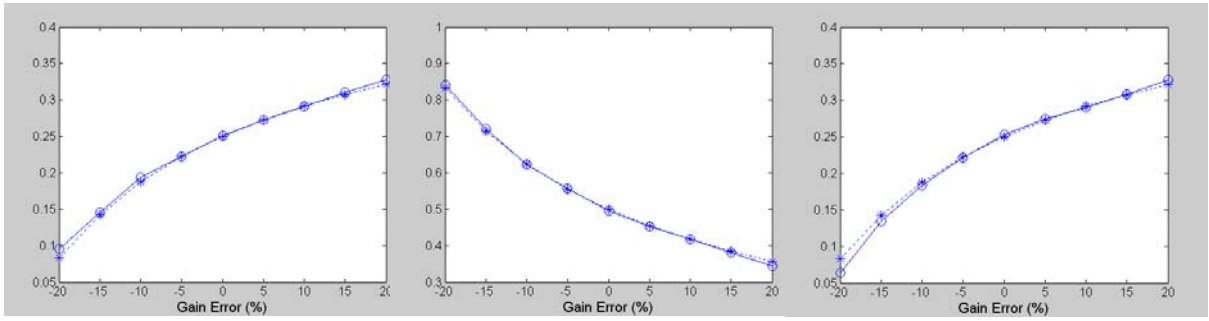
* P1 o P2 ^ P3

(b)

* S1 o S2 ^ S3

Figure 4.15

Figure 4.16 (a), (b), (c) show the comparison between P1-S1, P2-S2 and P3-S3 of gain errors. We find the simulation results are very close to the probabilities except the cases of -10%, -15% and -20%. This is because the input test waveform is not accurate enough in these cases.

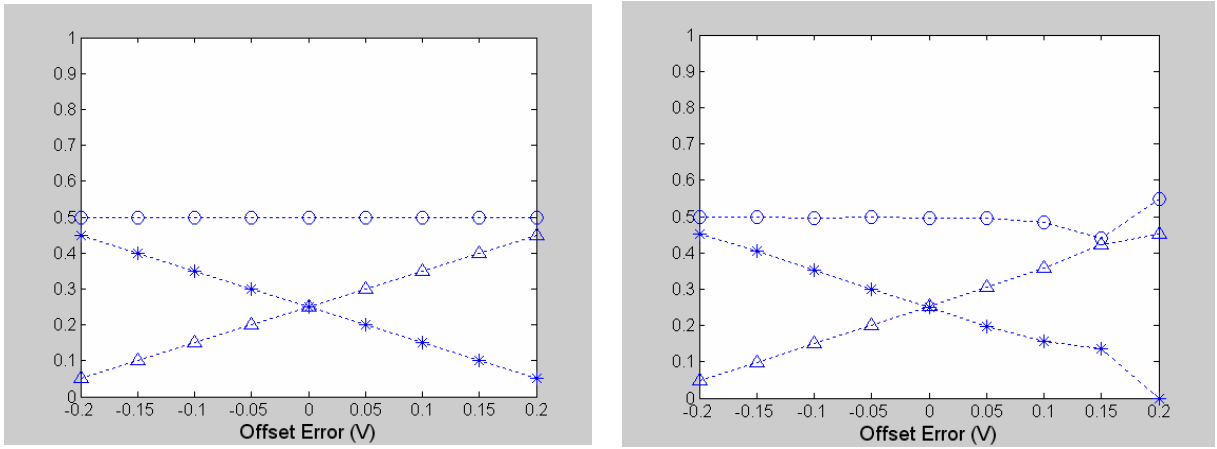


(a) (b) (c)

* Probability o Simulation

Figure 4.16

Next, we will discuss the case of offset error. Figure 4.17(a) and (b) show derived probabilities (P1, P2, P3) and simulation results (S1, S2, S3) of offset errors. The unit of X-axis is voltage. Due to Figure 4.17(b) we find that simulation results have errors in the cases of 0.1, 0.15 and 0.2. This is because the core circuit output responses generate amplitude errors in these cases and this reason affects the test results.

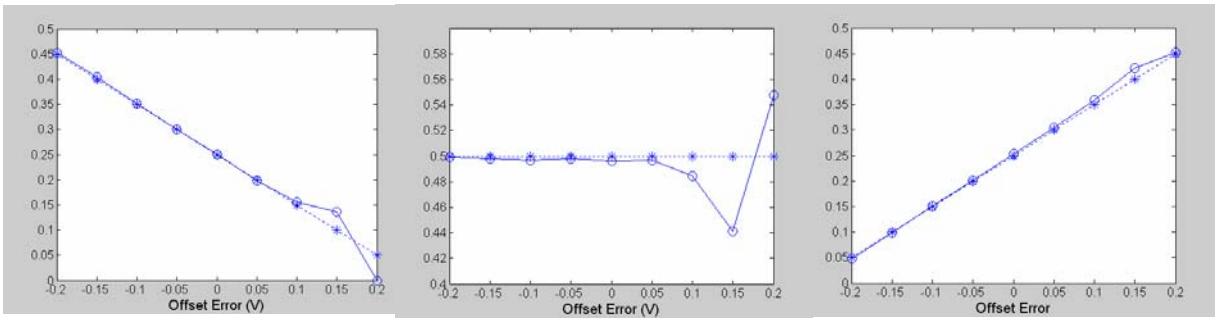


(a) (b)

* P1 o P2 ^ P3 * S1 o S2 ^ S3

Figure 4.17

Figure 4.18 (a), (b), (c) show the comparison between P1-S1, P2-S2 and P3-S3 of offset errors. We see the simulation results are very close to the probabilities except the cases of 0.1, 0.15 and 0.2. This is because the output responses generate the amplitude errors.



(a) (b) (c)

* Probability o Simulation

Figure 4.18

4.4 Layout Consideration and Implementation

In this section, we will describe layout considerations of some key-points, such as power-lines, capacitors and layout placement of the top circuit. The total area of the layout is 1.65(mm) * 1.3(mm) and total power is 72 mW.

4.4.1 Power Lines

Assume we use the approach shown in Figure 4.19(a) for the power lines connecting. It will cause a voltage drop exists inside the chip, which is called *power-supply coupling effect*. To avoid this problem, we apply two independent pair of pins for the connection of analog power lines and digital power lines. Like Figure 4.19(b) shows.

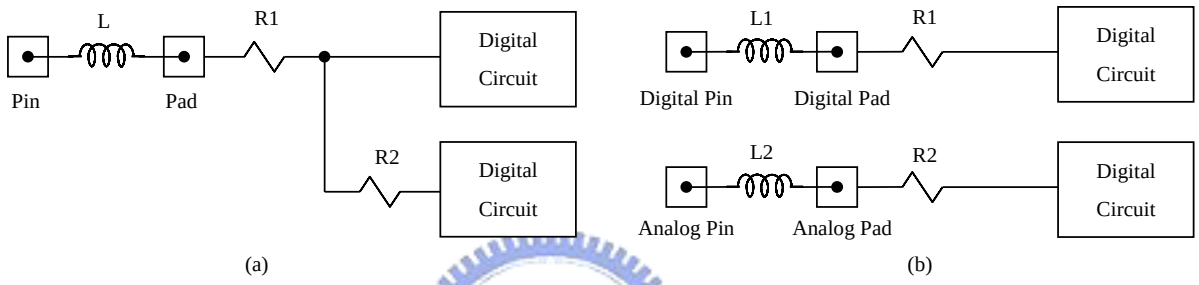


Figure 4.19 Layout consideration of power lines

4.4.2 Capacitors

For high accuracy of the capacitances, we use *MIM structure* to realize the capacitors of SC circuits because another approach, MOS capacitors are sensitive to the bias voltage and temperature. Figure 4.20 shows the structure of the MIM capacitor.

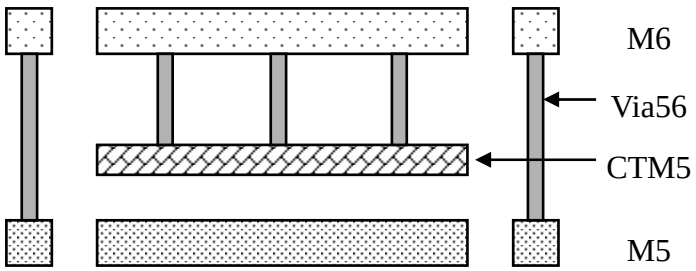


Figure 4.20 MIM capacitor structure

4.4.3 Top Layout Placement Considerations

Placement of the top layout is shown in Figure 4.21. This approach is suit for all SC circuits. Switches and digital circuits cause large impulse current during operating, which will introduce large *substrate coupling noise*. Substrate coupling noise affects analog circuits seriously because all circuits are placed on the same substrate. We have to use some layout skills to reduce this effect.

First, we place switches and digital circuits far away from analog circuits. As shown in Figure 4.21, we place the capacitor array in the center of the whole chip to divide analog circuits apart from digital circuits and switches. Except that, we use the approach of *N-well shielding*. We place the capacitor array in N-well and apply an additional power-supply VDD for the N-well to isolate the noise from *substrate coupling*. Second, we place analog power lines surrounding all of the analog blocks, which is called *guard ring*. This approach can protect circuits in the guard ring from the outside noise affecting. The third approach is dividing source of all digital transistors from the substrate in order to reduce substrate coupling. As shown in this figure, we apply an independent power line GNDd, which connects sources of all digital transistor together but not connect to VSSd (substrate) inside the chip.

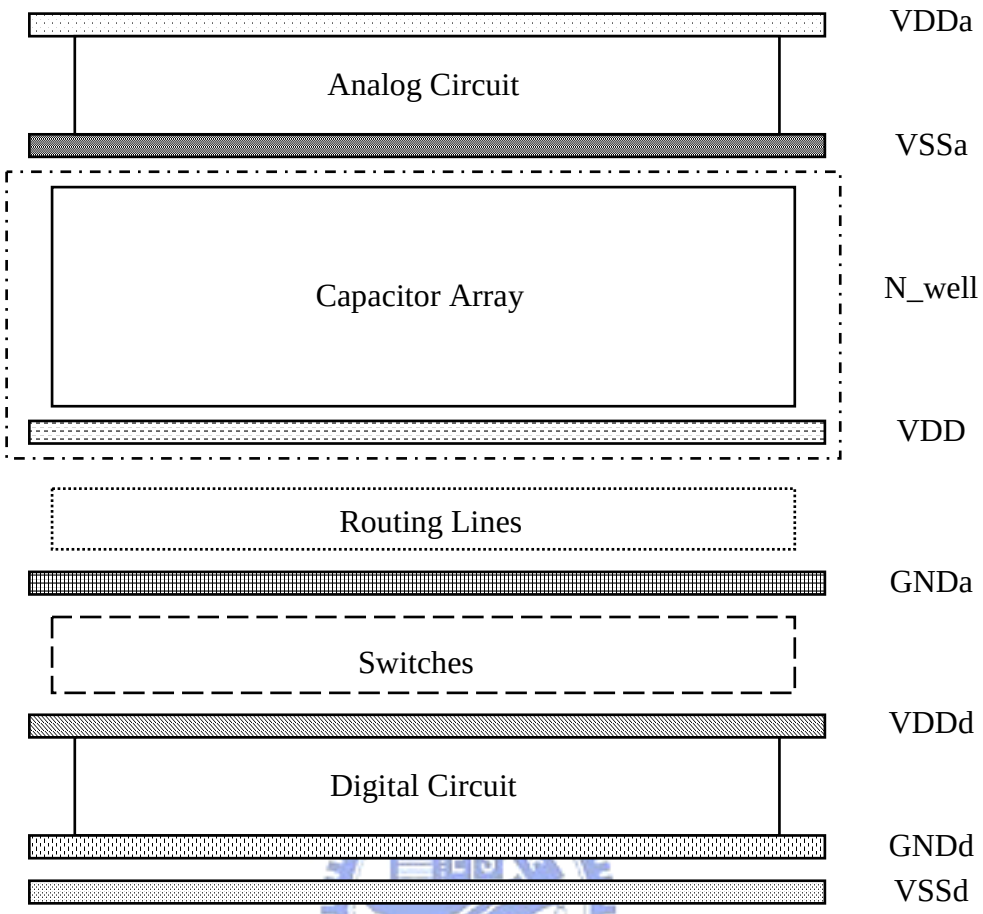


Figure 4.21 Placement of the top layout

Total layout is shown in Figure 4.22. The technology we use here is TSMC CMOS 0.18um 1P6M. The area is 1.65(mm)*1.3(mm) and power consumption is 72 mW. We also show the area and power proportion of BIST which occupies in the total circuit in Figure 4.23.

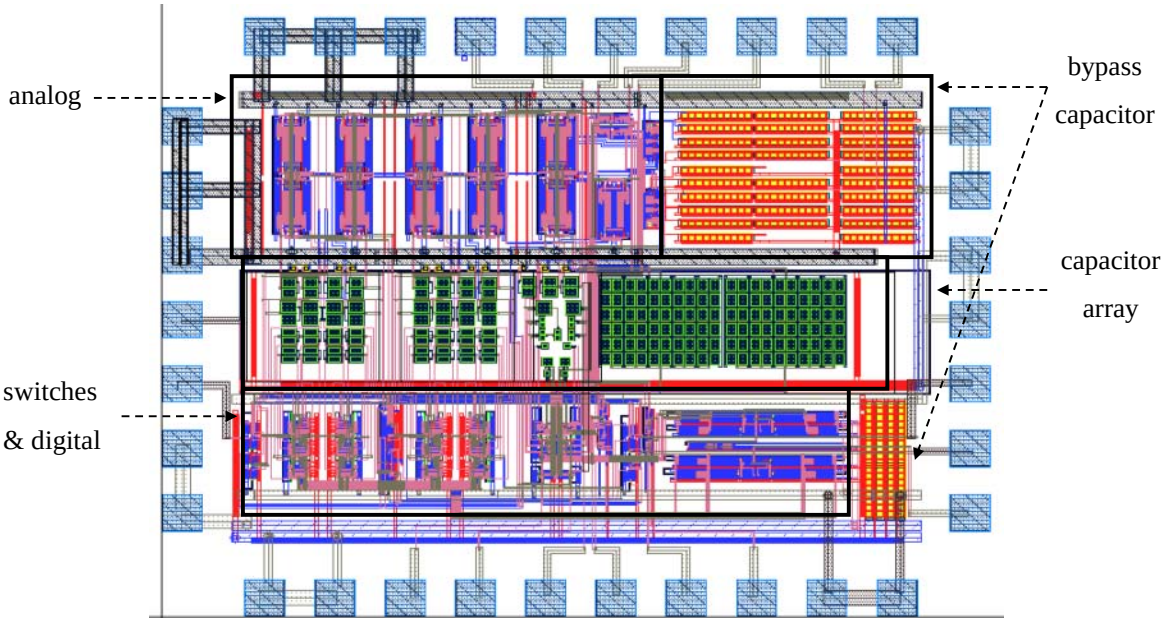


Figure 4.22 Layout of the high bandwidth, 4th-order, SC low-pass filter and the BIST circuit

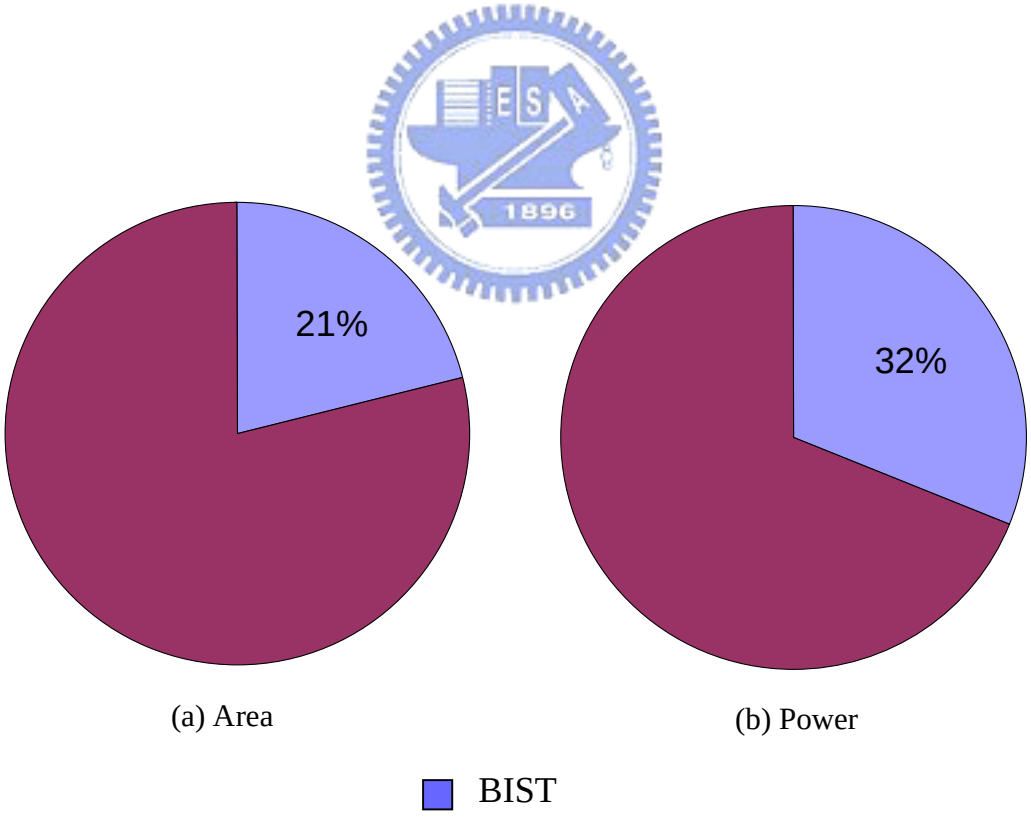


Figure 4.23 Area and power proportion of BIST

Chapter 5

Conclusion and Future Work

5.1 Conclusion

How to achieve on-chip testing of analog circuits with lower cost is the critical issue for today's mixed-signal testing. In this thesis, we design a fully-differential, 140 MHz sampling frequency, 10 MHz corner frequency, 4^{th}-order low-pass SC filter. Except that, we take the SC filter as the core circuit and design the BIST circuit for the SC filter. The test approach we adopted is taking triangular-wave as input waveform and comparing the probability of the self-test results to the derived results to estimate the gain error and the offset error. In our design, there is a test-waveform-generator, which generates a 29.2 KHz, 7 bits resolution, differential triangular-waves, and an output-response-analyzer, which includes a differential-to-single-ended circuit and a dual-comparator.

5.2 Future Work

There are some key-points should be improved in this thesis:

(1) Bandwidth of opamp: we implement a fully-differential opamp with unity-gain frequency at 770 MHz, if we achieve higher bandwidth, we can make the system operating in higher sampling frequency.

(2) Resolution of the triangular-wave: we achieve 7 bits resolution in this thesis, and we find the main accuracy limitation is because of the CMFB. It introduces common-mode voltage error during a period.

(3) DNL and INL error of differential-to-single-ended circuit: The DNL and INL error increase rapidly when output voltage close to analog ground. How to solve this problem is an important point of future works.

(4) Controllable-frequency TWG: We realize a TWG with a fixed-frequency test waveform. However, we can add some digital circuits to achieve controllable-frequency capability.

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