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Study on Low Oversampling Ratio Cascaded ΣΔ ADC with 1- or 1.5-bit Feedback DAC for Broadband Telecommunication Applications

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To my parents

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Supervisor: Lan-Rong Dung

Abstract

The speed and resolution of analog-to-digital converter (ADC) must advance before the signal bandwidth and the modulation depth of digital telecommunications receivers can improve. Hence, the data rate achievable by a communications standard is inevitably linked to the performance of the ADC. Sigma-Delta (ΣΔ) ADCs have demonstrated the possibility of achieving very high resolutions (>13 bit) without the need for expensive post-processing techniques, such as laser trimming or calibration. Nevertheless, ΣΔ ADCs have generally a limited signal bandwidth due to their oversampling nature. The basic requirement for a broadband ΣΔ ADC is, therefore, low oversampling ratio and high sampling frequency. Among many existing architectures, continuous-time single-loop architecture, discrete-time single-loop architecture, and discrete-time cascaded architecture are three possible and popular candidates. Considering the advantages and disadvantages of each architecture, this thesis is dedicated to addresses the design of two discrete-time cascaded ΣΔ ADCs with low oversampling ratio (OSR) for broadband telecommunication applications.

The first one is a low-power ΣΔ ADC for the extended bandwidth asymmetric digital subscriber line (ADSL2+); it performs 14 bit of resolution at a conversion rate of 4.4 MS/s. The core modulator employs a cascaded 2-1-1 fourth-order loopfilter with three 1.5-bit quan-

tizer. A three-stage digital decimation filter following the modulator output is designed to accomplish the complete analog-to-digital conversion. The sampling frequency is 70.4 MHz and the signal bandwidth is 2.2 MHz, which results in an OSR of 16. The circuit is implemented in TSMC 1P5M 0.25-μm CMOS technology and occupies an area of 2.8 mm^2. The measured dynamic range, peak signal-to-noise ratio and peak signal-to-noise-and-distortion ratio are 86 dB, 84 dB, and 77 dB, respectively. The total power consumption is 180 mW from a 2.5-V power supply including decimation filter and reference voltage buffers.

The second one is a resonator-based cascaded $\Sigma\Delta$ modulator (RAMSH) for low OSR applications. Based on two resonator topologies, the architecture can be immune to leakage quantization noise caused by circuit nonidealities over a large portion of the input range when OSR is low, and hence the dynamic range can be improved. The key of improving dynamic range is to use a cascade-of-resonator-with-feedforward (HQCRFF) 1-bit modulator in the first stage and makes the modulator from normal modulation mode into a novel oscillation mode. The theoretic analysis of operational condition for oscillation mode is presented and the transient behavior between two modes is also discussed. Finally, the design methodology and simulation results of RMASH are addressed. Without using additional calibration techniques, the dynamic range of the two RMASH architectures, RMASH 2-0 and RMASH 2-2 with the op-amp dc gain of 60 dB, the capacitor mismatch of 0.2%, and the OSR of 8 can be as high as 87 dB and 84 dB respectively.

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Chapter 1

Introduction

The high performance signal processing in applications such as digital audio, digital subscriber line system, and wireless communication systems has efforts toward improving the performance of data acquisition interfaces. Although the performance increases in the speed and density of integrated circuits due to the advances in VLSI technology, the interfaces between analog and digital systems still limit the speed and resolution. Therefore, it is very important to design a powerful analog-digital converter (ADC) in above applications.

As we know, ADCs can be classified into two categories: Nyquist-rate converters and oversampling converters. The principle of Nyquist-rate converters is that they sample analog signals at a rate approximately twice of the maximum frequency of the input signal and they are usually used to digitize wide-bandwidth signals with low to medium resolution such as pipelined ADCs. The other is oversampling converters which sample the analog signal at a rate much higher than the maximum frequency of the input and employ the increase of oversampling ratio (OSR) to produce a high-resolution digital output. Although the Nyquist-rate converters can get the maximum signal bandwidth, the main disadvantage of them is the high sensitivity to component matching and thus they usually can not obtain high resolution.

Sigma-Delta ($\Sigma\Delta$) ADCs, which provide a robust and economical solution for high-resolution analog-to-digital conversion, have being developed since the 60s of last century [1]. A $\Sigma\Delta$ ADC realizes that the input signals and the corresponding quantization errors pass through the low-pass loop filter and the high-pass filter, respectively. Therefore, the output signals comprise of the delayed input signals and the quantization errors are shaped by the high-order high-pass filter. Theoretically, quantization error can be infinitely shifted out the interesting bandwidth and the conversion resolution can be arbitrarily increased until

the device thermal noise floor physically limits the resolution. Furthermore, ΣΔ ADCs do not require accurate analog component matching to achieve the superior resolution, which makes it suitable for standard CMOS processes. In comparison with the Nyquist-rate ADCs, however, ΣΔ ADCs have to operate at an oversampling frequency, which results in the main drawback: the narrow conversion bandwidth. Recently, more and more research has been focus on development and implementation of ΣΔ ADCs with broad conversion bandwidth [8-10,28-39].

Considering the circuit realization, ΣΔ ADCs can be categorized into discrete-time (DT) structure and continuous-time (CT) structure [2]. Using switched-capacitor (SC) circuits, the DT ΣΔ ADC offers a good degree of accuracy. But the circuit speed is limited by the defective settling of SC integrator. CT ΣΔ ADCs are more adaptive to low supply voltage. The low power dissipation makes the realization of CT ADCs more attractive in future advanced CMOS processes. Input-signal sampling errors, like settling error, charge injection and some other DT problems do not exist in CT circuits. The circuits can operate at a higher speed for a given technology than their DT counterpart. Furthermore, CT ΣΔ ADCs provide implicit anti-alias filtering, thus reducing the need for explicit anti-alias filtering prior to the modulator [3]. But the drawbacks of CT ΣΔ ADCs are serious. A CT ΣΔ ADC requires a highly linear resistor or transconductor, which is not well-suited for implementation in modern sub-micro CMOS processes. Additionally, the pole locations of these integrations are set by the RC (or C/Gm) time constants of these devices. The variation of pole locations determined by products of two different device parameters can be as large as about ±30%. The large mismatch greatly limits the efficacy of CT ΣΔ ADCs without adding elaborate tuning mechanisms. It is also more sensitive to clock jitter [4] and quantizer metastability [5], which cause random pulse width modulation in the feedback DAC. Therefore, they, in turn, cause high-frequency quantization noise to fold into the signal bandwidth, which lowers the conversion resolution [6]. Since the requirement on ADC resolution in high-integration low-cost broadband telecommunication application is normally higher than other applications, this drawback prevents CT ΣΔ ADCs from being a good choice for broadband telecommunication application.

Before going into detail in describing the contributions of this work, a short introduction to the analog-to-digital conversion, and to the ΣΔ modulation is given.

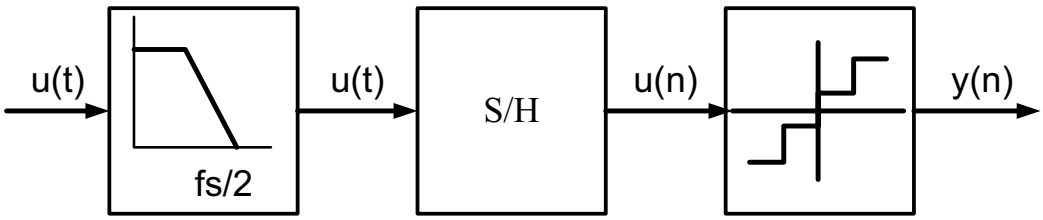

Figure 1.1: Block diagram of a generic ADC.

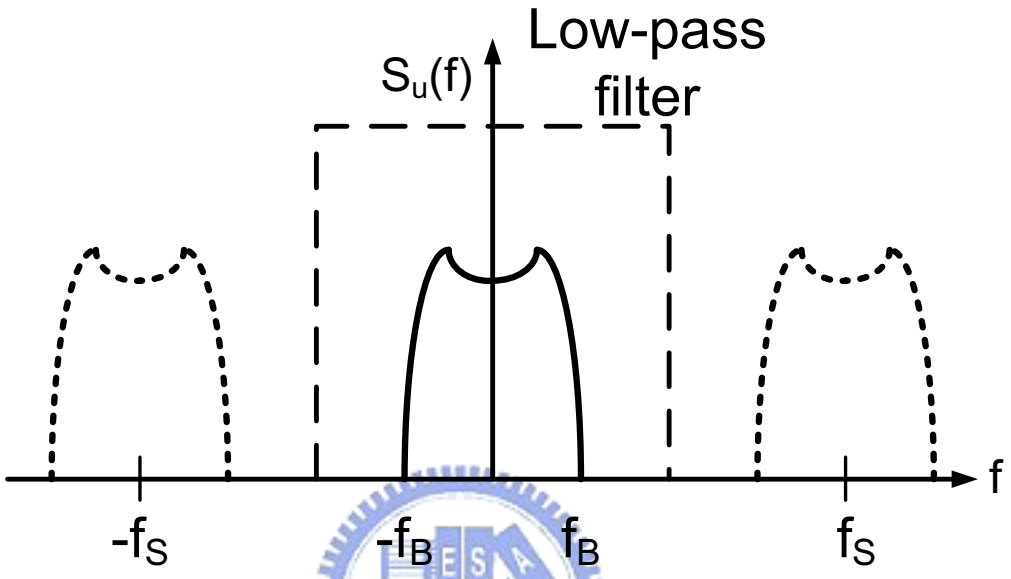

Figure 1.2: Spectral sampling operation.

1.1 Analog to Digital Conversion

The conversion of a continuous-time analog signal into a digital one is done in two operations as shown in Figure 1.1. First there is a sampling of the analog signal (usually with a constant sample period T_s), then a quantization of the signal amplitude is done. If the signal band of a sampled signal is less than half the sampling frequency, the sampling in time is a completely invertible process. Looking at the frequency spectrum of a sampled signal in Figure 1.1 this could be understood. When a signal is sampled at uniform time intervals, this results in a periodicity of the signal spectrum at multiples of the sampling frequency, f_S, in the frequency domain as seen in the Figure 1.2. With simple low-pass filtering it is clear that the original baseband spectrum can be reconstructed as long as the spectrums does not overlap. This is achieved when

$$f_s \geq 2f_b = f_N \tag{1.1}$$

where f_b is the bandwidth of the input signal. This equation is known as the Nyquist theorem, and f_N is called the Nyquist frequency. An analog filter preceding the sampling operation is required to assure that the input signal bandwidth is limited to f_b. This filter is known as the anti-aliasing filter (AAF). A basic ADC structure is shown in Figure 1.1. An ADC working at a sampling frequency that equals to f_N is called a Nyquist-Rate converter. These converters are hard to design in practice because of the zero transition band required for the AAF. To overcome this problem, this type of converters often use a slight amount of oversampling. The oversampling ratio (OSR) is defined as

$$OSR = \frac{f_s}{f_N} = \frac{f_s}{2f_b}. \tag{1.2}$$

Nyquist rate converters operates in most cases with an OSR = 1.5∼10 [7]. Increasing the OSR greatly relaxes the demands to the AAF, thus simplifies the design and reduces the power and chip area of the filter.

1.1.1 Quantization

The quantizer encodes a continuous range of analog values into a set of predefined discrete levels. Quantization is usually uniform and the space between two adjacent output levels of the quantizer is defined as the quantizer step size:

$$\Delta = \frac{FS}{2^N - 1} \tag{1.3}$$

where FS is the full-scale input range and 2^N is the number of different output levels. Since an infinite number of input values of the sampled input signal is mapped to an finite number of values in the quantizer, the quantization is an noninvertible process. A very useful and important assumption for quantization noise is white. If the input signal $x(n)$ has a rapidly and random variying behavior, the quantization noise $e(n)$ can be approximated as a random number uniformly distributed between $\pm\frac{\Delta}{2}$ and uncorrelated with its previous values. It is also assumed that $e(n)$ has statistical properties independent of $x(n)$. By these properties, $e(n)$ is classified as white noise with a mean square value of $e_{rms}^2 = \frac{\Delta^2}{12}$ [2].

1.1.2 Oversampling

When using a one-sided representation of the frequency domain, the power spectral density (PSD) of the quanization noise is:

$$S_e(f) = e_{rms}^2 \left(\frac{2}{f_s}\right). \tag{1.4}$$

Equation (1.4) implies that the quantization noise is uniformly distributed in the frequency range $0 < f < f_s/2$. The signal band, however, might have a range from $0 < f < f_0$. The total in-band noise power is then calculated by using Equations (1.2) and (1.4):

$$q_{rms}^2 = \int_0^{f_0} S_e(f)df = \frac{2f_0 e_{rms}^2}{f_s} = \frac{e_{rms}^2}{OSR} \tag{1.5}$$

Equation (1.5) shows for each doubling of OSR, the in-band noise power decreases by 3dB or 0.5 bits. Data converters employing oversampling to benefit from this property are called oversampled converters. By increasing the OSR they can achieve higher accuracy than Nyquist converters which use the same quantizer.

1.1.3 Performance Metrics

This subsection reviews the key metrics, such as signal-to-noise ratio, dynamic range, and Nyquist rate, which are needed by the evaluation of the $\Sigma\Delta$ modulator quality.

Total harmonic distortion (THD):

THD is the ratio between the sum of the power of the higher harmonics, and the power of the fundamental harmonic.

Signal-to-noise ratio (SNR):

SNR is the ratio in power between the input sine wave f_{in} and the noise of the converter from DC to Nyquist rate. SNR includes all noise sources in the modulator, both thermal and quantization. It is typically expressed in decibels.

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise}}\right). \tag{1.6}$$

Signal-to-noise-distortion ratio (SNDR):

SNDR is similar to SNR, except that it includes the harmonic content.

$$SNR = 10\log\left(\frac{P_{signal}}{P_{noise} + P_{distortion}}\right). \tag{1.7}$$

For small signal levels, distortion is not important. As the signal level increases, distortion degrades the modulator performance, and the SNDR will be less than the SNR.

Dynamic range (DR):

DR is the ratio in power between the maximum input signal level that the modulator can handle and the minimum detectable input signal. Practically, the maximum input signal level is the input level where the SNDR drops 3 dB beyond the peak. For an ADC, if the signal is too large, it will over-range the ADC input. If it is too small, the signal will get lost in the quantization noise of the converter.

Spurious-free dynamic range (SFDR):

SFDR is the ratio of the power value of the input sine wave with a frequency f_{in} for an ADC, to the power value of the peak spur observed in the frequency domain. A large spur in the frequency domain may not significantly affect the SNR, but will significantly affect the SFDR. SFDR is a useful metric in communication applications, where the distortion component can be much larger than the signal of interest due to the intermodulation of unwanted interferential signals. Consequently, the small input signals are masked into the spurs; the dynamic range of the ADC is attenuated.

Nyquist rate:

Nyquist rate f_N is the lowest sampling frequency that can be used for analog-to-digital conversion of a signal without resulting in significant aliasing. This frequency is twice the rate of the highest input frequency f_b. Therefore, Nyquist rate specifies the minimum sampling frequency required to avoid aliasing.

1.2 Sigma-Delta ADC

The basic idea of Sigma-Delta ($\Sigma\Delta$) ADC is that it exchanges resolution in amplitude to resolution in time. In such ADC, the analog signal is modulated into a low resolution code at a frequency much higher than the Nyquist rates, and then the excess quantization noise is removed by the following digital filters [2]. Thus, if OSR is high, the oversampling ADCs are very suitable for CMOS VLSI digital technology because it does not require high performance analog buildings.

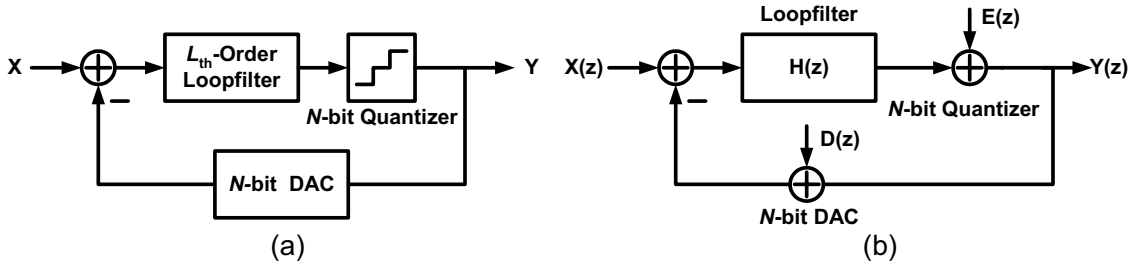

Figure 1.3: Sigma-Delta modulator architecture:(a) Basic block diagram, (b) Corresponding linear model.

Figure 1.3 shows the basic block diagram of a $\Sigma\Delta$ modulator and its corresponding linear model. The $\Sigma\Delta$ modulator consists of a feedforward path formed by a *Lth*-order loopfilter and a N-bit quantizer, and a negative feedback path around them, using a N-bit digital-to-analog converter (DAC). In the linear model as illustrated in Figure 1.3(b), the DAC is assumed to be ideal, D(z)=0, and the injected quantization error, E(z), of the quantizer is assumed as an additive white noise approximation. In this way, the modulator can be considered as a two-input, one-output linear system. Therefore, a signal transfer function (STF) and a noise transfer function (NTF) can be derived:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)}. \tag{1.8}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}. \tag{1.9}$$

In the frequency domain, the output signal is obtained as the combination of the input signal and the noise signal, with each being filtered by the corresponding transfer function:

$$Y(z) = STF(z)X(z) + NTF(z)E(z). \tag{1.10}$$

By properly selecting the loop filter, the STF and the NTF of a theoretical *Lth*-order modulator yield in the z-domain:

$$STF(z) = \frac{Y(z)}{X(z)} = \frac{H(z)}{1+H(z)} = z^{-L} \tag{1.11}$$

$$NTF(z) = \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} = (1-z^{-1})^{L} \tag{1.12}$$

where $H(z) = 1/(1-z^{-1})$. Figure 1.4 plots the frequency responses of NTFs with different orders of L. When the loop order is higher than one, the frequency response of NTF

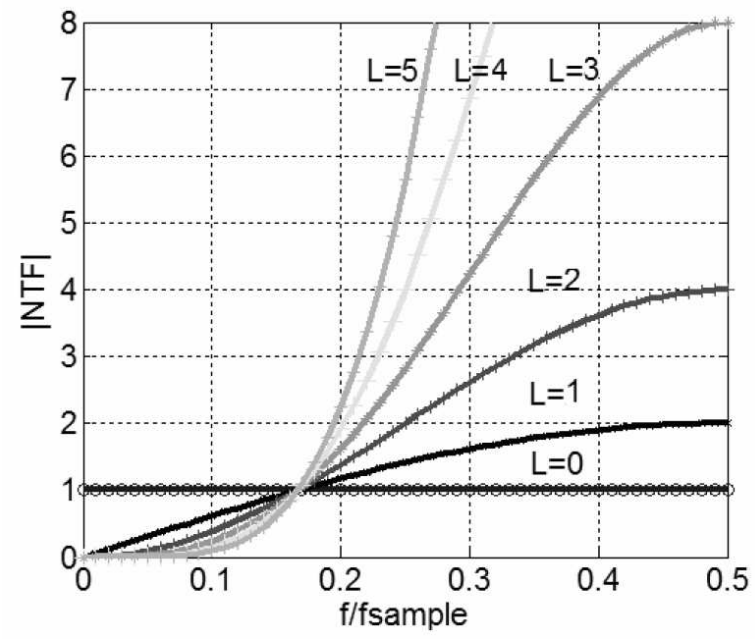

Figure 1.4: Frequency responses of NTFs with different orders of L

presents the characteristic of highpass filters. The higher the order L is, the more quantization error energy is suppressed at low frequencies. For Lth-order loopfilters, a function for approximation of the theoretical in-band noise power is [2]:

$$q_{rms}^2 = \frac{\pi^{2L} e_{rms}^2}{(2L+1)(OSR)^{2L+1}} \tag{1.13}$$

This function is plotted in Figure 1.5. Stability considerations will reduce the practical achievable resolution of higher-order modulators. For higher-order single-bit modulators the difference is substantial (say, more than 60 dB for a 5th-order modulator) [2]. These stability issues arise when the modulator order is higher than second order.

1.3 Motivation and Contribution

In general, the oversampling converter is used in lower signal bandwidth and high-resolution applications such as digital audio. However, due to the requirements of high resolution for modern telecommunication systems (ADSL, VDSL), the increasing resolution and bandwidth of $\Sigma\Delta$ modulators are necessary. Two ways can be used to increase the resolution of $\Sigma\Delta$ modulators. The first one is the increase of the loopfilter order to get better noise shaping. When the high-order $\Sigma\Delta$ modulators are designed, the most important topic is to choose the NTF. In $\Sigma\Delta$ modulator, the more noise is shaping into the out-band

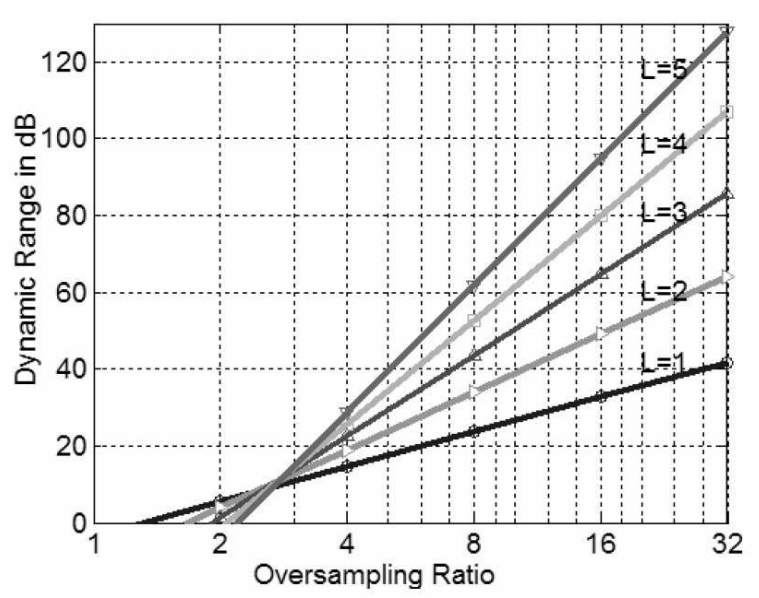

Figure 1.5: DR versus OSR of a theoretical Sigma-Delta modulator for for different Lth-order (with all zeros at DC).

frequency, and the better resolution is obtained. For single-stage ΣΔmodulators, additional integrators are placed in the forward path to increase the order of the noise shaping. However, the single-stage ΣΔ modulators are prone to instability if the order is greater than two [2]. Therefore, to design a high-order ΣΔ modulator with stable loopfilter is a very important issue for broadband applications. The second method is the increase of the bit number of internal quantizer to get lower noise floor. The ΣΔ modulators employing multi-bit quantizer can have several advantages over those using the single-bit quantizer [2]. However, the major problem in designing the multi-bit sigma-delta modulators is that much better component matching for the internal DAC linearity is required. Therefore, the performance of the multi-bit ΣΔ modulators is directly related to the linearity of the internal multi-bit DAC in the feedback path. Although, there are various innovative multi-bit DAC architectures employing dynamic element matching (DEM) to improve the linearity of the internal DAC, most of them will increase the analog circuit complexity.

To be compatible with the telecommunication applications, this thesis describes two cascaded high-order ΣΔ modulators to achieve high DR at low OSR. The first one is a cascaded 2-1-1 modulator with an OSR of 16 and a signal bandwidth of 2.2 MHz suited for ADSL2+. The key features of this cascaded modulator are the use of 1.5-bit quantizer/DAC in each stage and the use of two pairs of reference voltages. The second one is a resonator-based cascaded modulator with an intrinsic oscillation mode which can be used to improve DR.

1.4 Thesis Organization

This thesis consists of five chapters, of which that is the first.

Chapter 2 provides a architecture survey of ΣΔ modulators that are suited for broadband applications. The broad bandwidth (>1 MHz) usually implies some trends and limitations of architecture design. Firstly, the OSR must be reduced to avoid the high sampling frequency. Secondly, the orders of loopfilter should be increased to maintain desired DR by using aggressive noise shaping. Finally, the multi-bit internal quantizers and multi-bit feedback DACs may be used to increase DR and to provide good stability of the loopfilters. Among existed architectures, three architectures are most possible candidates for broadband applications. They are continuous-time ΣΔ modulator, single-loop ΣΔ modulator, and cascaded ΣΔ modulator. The basic characteristic of each architecture are addressed as well as some major design limitations and challenges are discussed.

Chapter 3 describes the proposed fourth-order cascaded modulator for ADSL2+ application. Three architectural features are involved in the proposed modulator. They are the use of 1.5-bit quantization, the use of bandpass noise shaping, and the use of two different pairs of reference voltages. The detailed architectural analysis and circuit implementation are addressed. The modulator is fabricated in a 0.25-μm CMOS technology, in a 2.8-mm^2 active area including decimation filter and reference voltage buffers, and dissipates 180 mW from a 2.5-V power supply. As shown in the experimental result, for a 2.2 MHz signal bandwidth, the ADC achieves a dynamic range of 86 dB and a peak signal-to-noise and distortion ratio (SNDR) of 77 dB with an oversampling ratio of 16.

Chapter 4 presents a new resonator-based cascaded architecture, called RMASH, for low-OSR ΣΔ modulators. Based on two resonator topologies, the architecture can be immune to leakage quantization noise caused by circuit nonidealities over a large portion of the input range when OSR is low, and hence the DR can be improved. The key of improving DR is to use a cascade-of-resonator-with-feedforward modulator in the first stage and a low-Q cascade-of-integrator-with-feedforward in the following stage. The first stage can operates in the modulation mode or the oscillation mode depending on the input amplitude. When the first stage oscillates, the leakage quantization noise problem can be alleviated. The theoretic analysis of operating condition for oscillation mode is presented and the transient behavior between two modes is also discussed. Finally, the design methodology and simulation result of RMASH are addressed. As can be seen from the simulation results, without using additional calibration techniques, the DR of the proposed RMASH 2-2 architecture with the op-amp

dc gain of 60 dB, the capacitor mismatch of 0.2%, and the OSR of 8 can be as high as 84 dB.

Chapter 5 begins with a summary which concludes the results achieved in this thesis. Also some issues are brief discussed for future work.

Chapter 2

Architecture Survey

ΣΔ modulators have been notably employed to implement high-resolution analog-to-digital conversions (ADCs) or digital-to-analog conversions (DACs) for narrow bandwidth applications such as voice-band telecommunications and audio signal acquisitions in the last decade. One of the most important reasons is that they make the realization of high-resolution data converters possible while requiring only moderate-quality analog components. The performance of a ΣΔ modulator is mainly determined by the performance of the analog building blocks whose specifications are dictated by the selected architecture. Therefore it is important to select the best suitable architecture that relaxes the circuit specifications while keeps the desired performance. With the increasing demand of ΣΔ modulator with broader bandwidth and higher dynamic range (DR), the architectures with low oversampling ratio (OSR) becomes more and more attractive. For this reason this chapter surveys possible architectures which are suited for low OSR applications.

There are many architectures to implement a ΣΔ modulator and three architectures are most popular choices for high-DR and low-OSR applications among them. They are continuous-time, discrete-time single-loop, and discrete-time cascaded modulators. In the following subsections, the architectural characteristic and design challenge of these architectures are addressed.

2.1 Continuous-Time ΣΔ Modulator

The exist and implementation of continuous-time (CT) ΣΔ modulator have been a long time. Due to the coming of switched-capacitor (SC) circuits in the 1980s, the majority of ΣΔ modulator have been implemented by SC loopfilters referred as discrete-time (DT) modula-

tors. This development comes from the fact that SC filters exhibit both good accuracy and good linearity. Furthermore the transfer function of a SC filter is independent of clock rate. In contrast, CT filters usually have poor linearity and accuracy. The time-constants of the CT filter suffer from large variation and typically require calibration. Recently, $\Sigma\Delta$ modulators utilizing CT loopfilters become more and more attractive because of three important reasons [2]:

1). CT modulators have inherent anti-aliasing property. The use of CT loopfilter postpones the unavoidable sampling of the signal to the output of the loopfilter. Thus, imperfections of the sampling process and the folding of the wideband noise have the same degree of suppression to that of quantization noise suppression. This inherent anti-aliasing relaxes the requirement of anti-aliasing filters, which typically must precede the SC modulators.

2). CT modulators potentially can operate in high sampling frequency. The theoretical limit on the sampling frequency of a CT modulator is determined by the regeneration time of the quantizer and the update rate of the feedback DAC, whereas in an SC modulator the sampling frequency is limited by the opamp settling performance dominated by the unity-gain frequency of the amplifiers within it. As a result, the CT modulator can operate with a clock frequency which is 2-4 times faster than that which can be achieved with SC loopfilters. This increases the achievable signal bandwidth of CT modulators in spite of lower linearity and accuracy.

3). CT modulators have the advantage of low power dissipation. In contrast to an SC design, in a CT loopfilter there is no need for fast settling integrators. Hence, in a CT loopfilter, the bandwidth requirements of the sub-blocks (opamps, or Gm-C cells) are more than three times lower compared to an SC loopfilter.

The above three advantages make the development of CT modulators benefit from the broadband applications [8, 9, 10]. However, the feedback loop delay and timing jitter usually limits the achievable performance.

2.1.1 Excess Loop Delay

Ideally DAC currents respond immediately to the quantizers clock edge, but the non-zero transistor switching time of the latched comparator and the DAC result in a finite delay between the comparator and the DAC [11]. This delay is called "*Excess Loop Delay*". Excess loop delay can be modeled as $t_d = \rho_d \cdot T$ as depicted in Figure 2.1 for an non return to zero (NRZ) DAC pulse. ρ_d is dependent on the switching speed of the transistors f_t, the quantizer

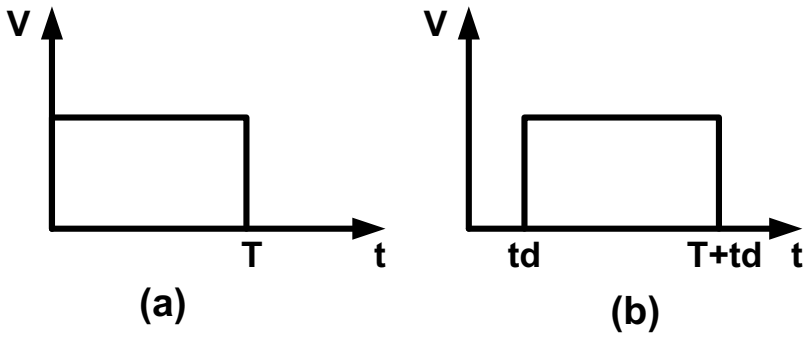

Figure 2.1: Excess loop delay: (a) ideal DAC pulse, (b) delayed DAC pulse.

clock f_s, the number of transistors in the feedback path n_t, as well as the loading on each transistor, and a rough approximation is $\rho_d \approx \frac{n_t f_s}{f_t}$ [11]. This excess loop delay increases the noise floor for a given $\Sigma\Delta$ modulator [11] since this noise adds to the quantization noise of the $\Sigma\Delta$ modulator and is shaped by the noise transfer function. The excess loop delay also potentially increases the instability of the $\Sigma\Delta$ modulator by adding another order to the loop filter [12]. The detailed analysis of excess loop delay for a CT modulator can be found in [11, 12]. Here a fifth-order 1-bit CT modulator with OSR of 32 is used to evaluate the effect of excess loop delay as shown in Figure 2.2. Assuming that the excess loop delay is 0.1% of the sampling period 10ns, the output spectrum of the modulator is shown in Figure 2.3. According to Figure 2.3, the excess loop delay increases not only the noise floor but also the instability of the modulator loopfilter.

2.1.2 Clock Jitter

Clock jitter is statistical variations of clock edges [13]. Two clocks are present in a CT $\Sigma\Delta$ modulator and both can be affected by clock jitter. One of the clocks controls the decision instant of the quantizer while the other clock controls the DAC output. Since the output of the quantizer is shaped by the NTF, the impact of this error will be relatively small. Conversely, the output of the DAC is shaped by the STF since this signal adds to the input signal, and thus the impact of this error will affect the baseband noise in the $\Sigma\Delta$ modulator [14]. There are two varieties of clock jitter, delay clock jitter and pulse-width clock jitter. Paper [15] demonstrates that in a second-order $\Sigma\Delta$ modulator, the delay clock jitter is shaped by the NTF while the pulse-width clock jitter manifests itself as white noise. This jitter noise degrades the SNR of the $\Sigma\Delta$ modulator more severely since the white noise spreads evenly across the frequency spectrum. Therefore the clock jitter discussed will be

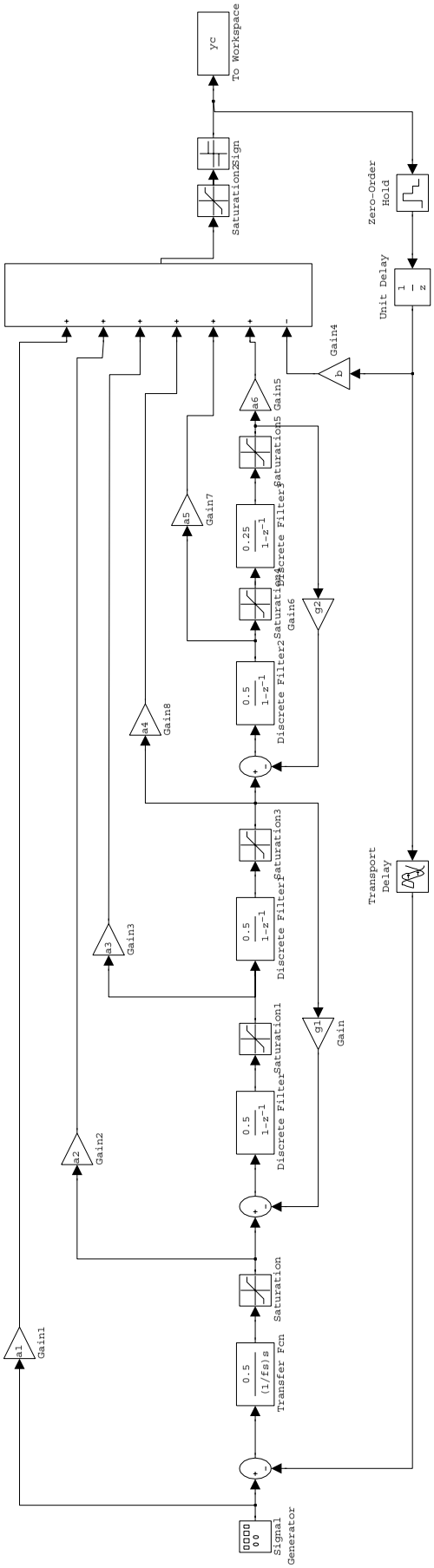

Figure 2.2: The simulink model of a fifth-order 1-bit CT modulator with excess loop delay

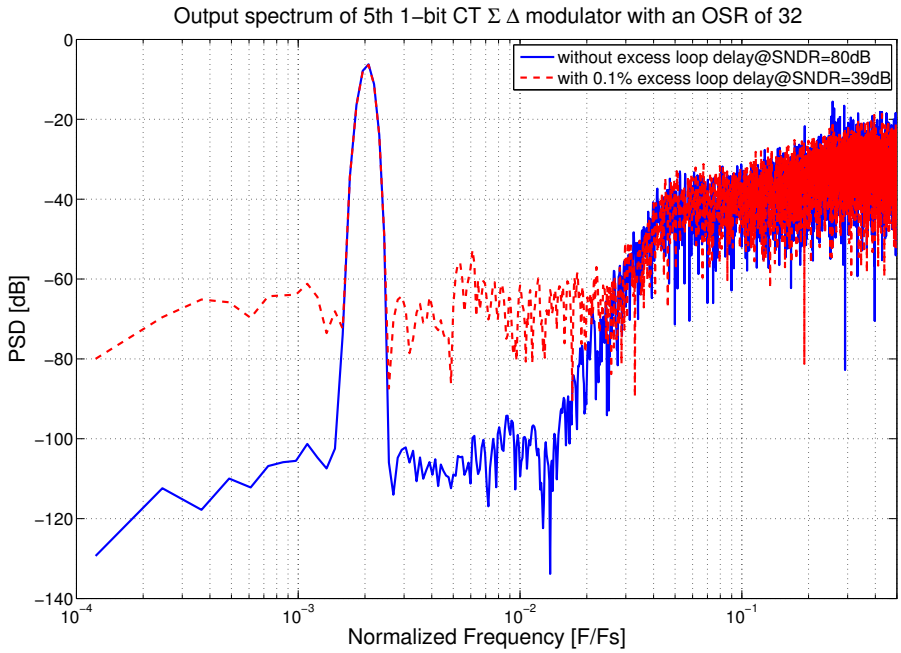

Figure 2.3: The output spectra of the fifth-order 1-bit CT modulator with and without excess loop delay

the pulse-width clock jitter incurred in the DAC.

DT ΣΔ modulators are relatively insensitive to pulse-width clock jitter because they are utilized by SC circuits. The insensitivity is due to the sloping pulse form of the feedback [13]. Since most of the charge transfer in a SC circuit occurs at the beginning of the clock period, clock jitter introduces a minimal amount of error in the charge lost ΔQ_D as shown in Figure 2.4(a). The capacitor is discharged over a switch with very low on-resistance, thus reducing the value of $\tau = RC$ and causing a fairly steep slope as the DAC discharges [5]. In contrast, CT ΣΔ modulators transfer charge at a constant rate over the clock period, and thus the charge loss ΔQ_C due to a timing error is proportionally much greater than that of the DT ΣΔ modulator as shown in Figure 2.4(b). Assuming white clock jitter, the sampling times of the output bits (for a sampling period T) are given by $t_n = nT + \Delta t$ where Δt is an independent and identically distributed random variable with variance $\sigma^2_{\Delta t}$. The resulting noise power of the clock jitter for a 1-bit quantizer with a step size of Δ and a typical return-to-zero (RZ) DAC pulse is given by [13]

$$P_j = \frac{\Delta^2 \sigma^2_{\Delta t}}{OSR \cdot T^2} \tag{2.1}$$

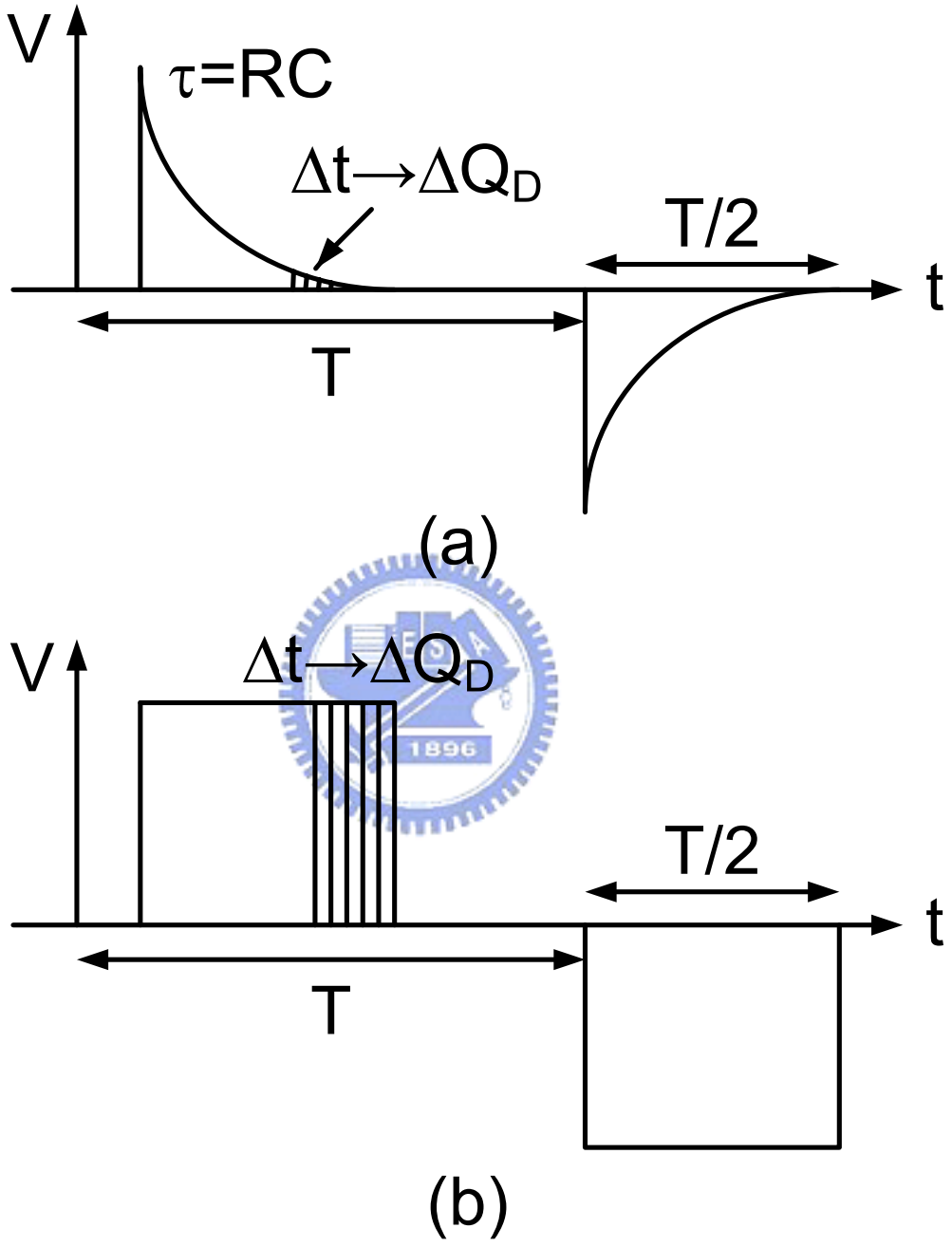

Figure 2.4: (a) Clock jitter in DT modulator. (b) Clock jitter in CT modulator.

The quantization noise power of a general Lth order $\Sigma\Delta$ modulator is given by [2]

$$P_q = \frac{\Delta^2 \pi^{2L}}{(24L+12) \cdot OSR^{(2L+1)}} \tag{2.2}$$

An figure of merit for the noise can be defined as the point at which the noise power of the clock jitter is equal to the noise power of the quantization noise, thus reducing the SNR by 3dB [13]. Equating (2.1) and (2.2), this critical value is found to be

$$\frac{\sigma_{\Delta t}}{T} = \frac{\pi^L}{\sqrt{(24L+12)} \cdot OSR^L} \tag{2.3}$$

This value decreases with increasing OSR, meaning that as the OSR increases the clock jitter becomes more detrimental. Also, as the order of the modulator is increased, $\frac{\sigma_{\Delta t}}{T}$ decreases, indicating that proportionally the clock jitter becomes more significant in higher order CT $\Sigma\Delta$ modulators.

2.2 Single-Loop $\Sigma\Delta$ Modulator

The single-loop architecture means the modulator has only one conversion stage and one quantizer. In [2], it has been shown that OSR, loopfilter order, quantizer bit are related to the DR of the $\Sigma\Delta$ modulator by

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N - 1)^2 OSR^{2L+1}. \tag{2.4}$$

where L is the order of loopfilter and n is the bit number of quantizer. This equation is valid only for the case of pure-differentiation NTF, e.g. $NTF = (1 - z^{-1})^L$. For the case of $L \leq 2$, its prediction is exact. However, the stability considerations usually present the such NTF being implemented when $L \geq 2$. As a result, the achievable DR in the case of $L \geq 2$ is usually lower than that predicted by Equation (2.4). The higher the order, the worse the degradation becomes especially when 1-bit quantizer is used. As a result, the high-order multi-bit structures are usually the best choice for single-loop low-OSR modulators. There are two general structures to implement the high-order single-loop modulators called feedforward (FF) and feedback (FB). The main difference between FF and FB structures is that in the FB structure, the quantizer output is fed back to the input of each integrator. In the contrast to FB, the quantizer output of FF structure is fed back only to the input

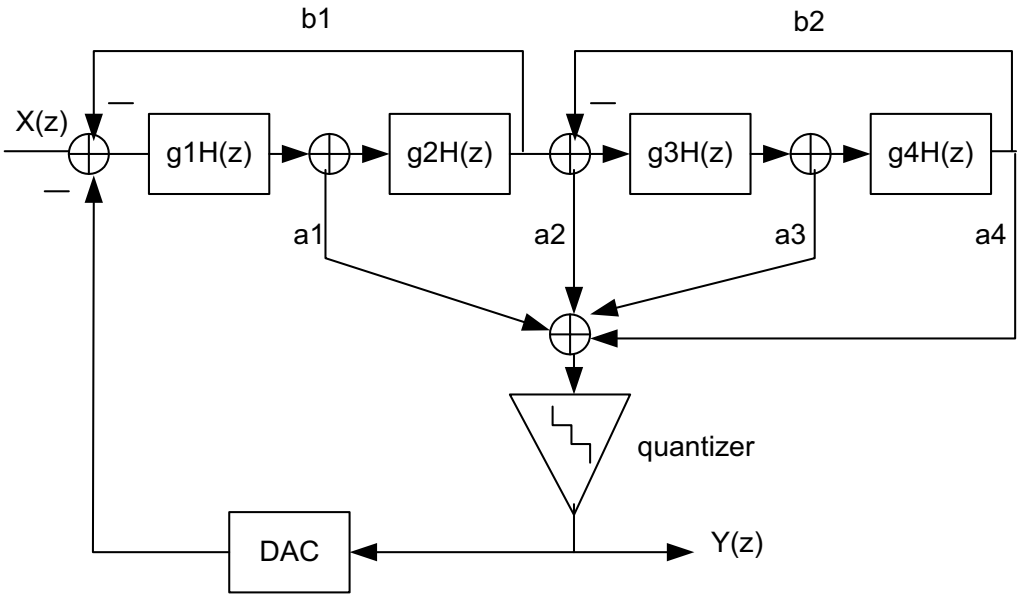

Figure 2.5: The block diagram of FF fourth-order single-loop modulator.

stage. According to analysis of [16], the single-loop modulator with FF structure is preferred for broadband applications. Thus, the FF structure is selected to be the design example of high-order single-loop modulators. The readers who interest in FB structure can refer the articles [2].

2.2.1 Feedforward Structure

When a high-order sigma-delta modulator is designed, the NTF is the main considered condition because it decides the performances of the modulator. Generally, the NTF of an even-order FF sigma-delta modulator can be expressed as

$$NTF(z) = \frac{\prod_{i=1}^{m}[(1-z^{-1})^2 + b_i]}{\prod_{i=1}^{m}[(1-z^{-1})^2 + b_i] + \sum_{i=1}^{m}([a_{2i-1}(1-z^{-1}) + a_{2i}]\prod_{j=i+1}^{m}[(1-z^{-1})^2 + b_j])} \quad (2.5)$$

The NTF determines what extent the quantization noise is reduced in a given bandwidth and hence determines the overall signal-to-noise ratio (SNR) of the converter. The feedback coefficients may decide the zeros and the feedforward coefficients decide the poles. There are several design tools for automatic coefficients synthesis of high-order loopfilter [16, 2]. One of them is called "DELTA-SIGMA TOOLBOX", which is made by Richard Schreier [2]. This toolbox is programmed by MATLAB and the reader can obtain your free copy of it from the MathWorks web site [17]. In order to get more sight, two sample design

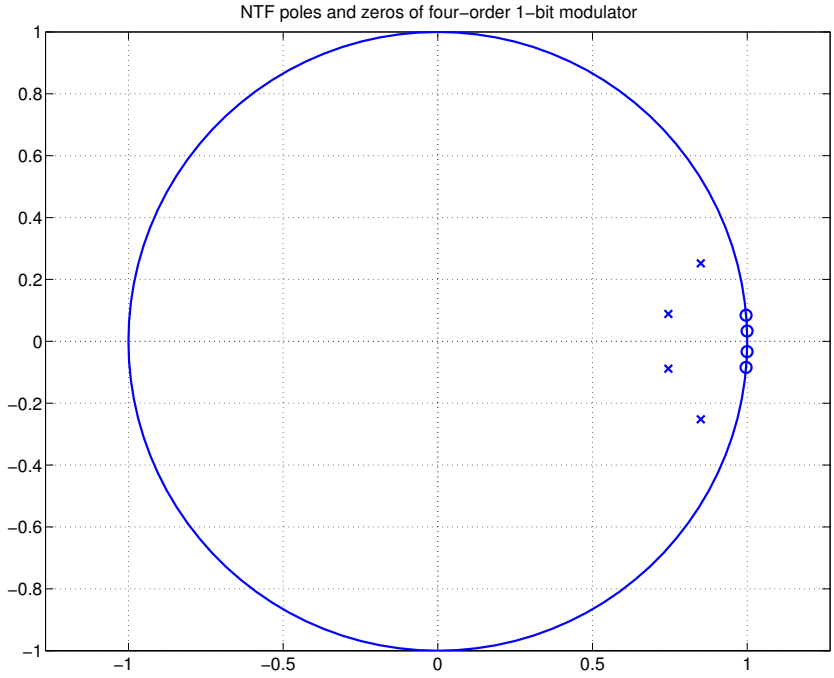

Figure 2.6: The locations of NTF poles and zeros for FF fourth-order 1-bit modulator.

examples of fourth-order 1-bit and 4-bit modulators synthesized by this tools are provided. The block diagram of FF fourth-order single-loop modulator is shown in Figure 2.5. Given the OSR of 32 for the fourth-order 1-bit modulator, the NTF can be synthesized by using the "*synthesizeNTF*" function and the results is given as

$$NTF_{1-bit} = \frac{(1 - 1.999z^{-1} + z^{-2}) \cdot (1 - 1.993z^{-1} + z^{-2})}{(1 - 1.49z^{-1} + 0.563z^{-2}) \cdot (1 - 1.7z^{-1} + 0.7861z^{-2})} \tag{2.6}$$

Note that the maximum out-of-band gain of the NTF of 1-bit modulator is set to be 1.5 according to the Lee's rule (say, $L < 2$). Figure 2.6 shows the locations of NTF poles and zeros. By adding the small negative-feedback terms, b_1 and b_2, around pairs of integrators in the loopfilter as shown in Figure 2.5, the zeros are distributed through the signal band in order to lower the in-band noise [18]. The poles are chosen to flat the frequency response at high frequency in order to reduce the high-frequency noise. It is possible to move the open-loop zeros away from dc along the unit circle by using a feedback loop around pairs of integrators in the loopfilter. This approach is especially useful for broadband or low-OSR applications because the in-band quantization noise can be suppressed. The frequency response of NTF is shown in Figure 2.7. Obviously, the in-band NTF zeros result in the notch filtering, thus causing a flat shape in the signal band. The rms gain of NTF in the signal

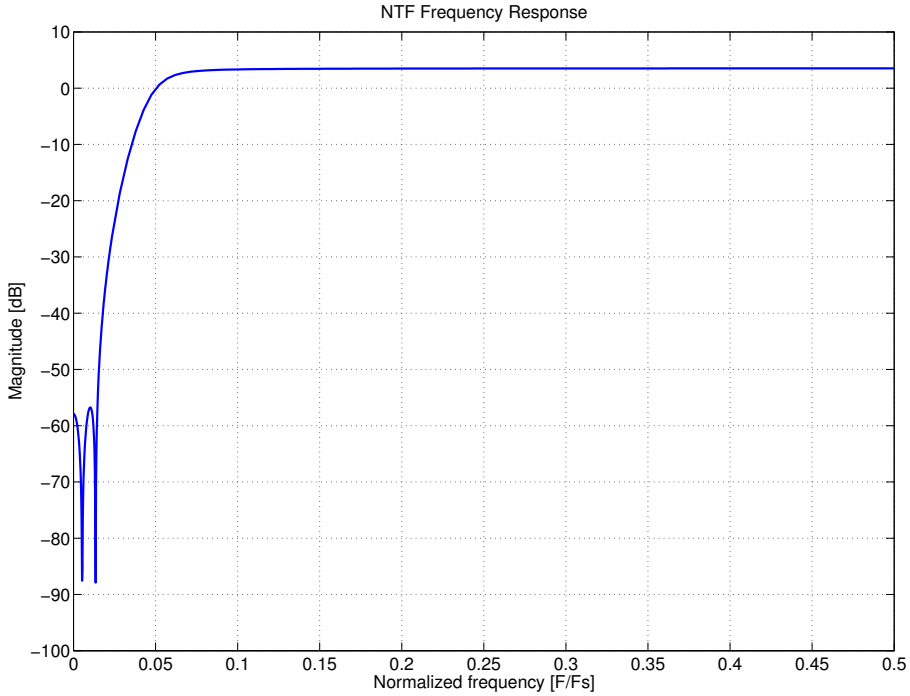

Figure 2.7: The frequency response of NTF for FF fourth-order 1-bit modulator.

band is approximatly -59dB. The simulated and expected power spectrum density (PSD) of fourth-order 1-bit modulator by using the "*simulateDSM*" function is shown in Figure 2.8. The predicted and simulated SNDR versus input level is shown Figure 2.9. According to Figure 2.9, the peak SNDR of fourth-order 1-bit modulator with OSR of 32 is 79.2dB which is less than 14-bit resolution. To further increase the peak SNR, the higher order or OSR is required at the expense of increasing the silicon cost and power dissipation.

The fourth-order 4-bit modulator with OSR of 16 has the similar design flow to 1-bit one, but benefits from the more stable gain of the quantizer, because the better the gain of the quantizer is known, the more stable is the loop and more aggressive can be the noise shaping. As a result the maximum out-of-band gain of the NTF is increased to be 5, which greatly enhances the resolution of the modulator. The synthesized NTF of fourth-order 4-bit modulator is given as

$$NTF_{4-bit} = \frac{(1 - 1.996z^{-1} + z^{-2}) \cdot (1 - 1.971z^{-1} + z^{-2})}{(1 - 0.6214z^{-1} + 0.1142z^{-2}) \cdot (1 - 0.49z^{-1} + 0.3385z^{-2})} \tag{2.7}$$

The simulated and expected PSD of fourth-order 4-bit modulator is shown in Figure 2.10. while the simulated SNDR versus input level is shown Figure 2.11. According to Figures 2.10 and 2.11, the modulator achieves peak SNR of 107.7dB which is larger than 17-bit

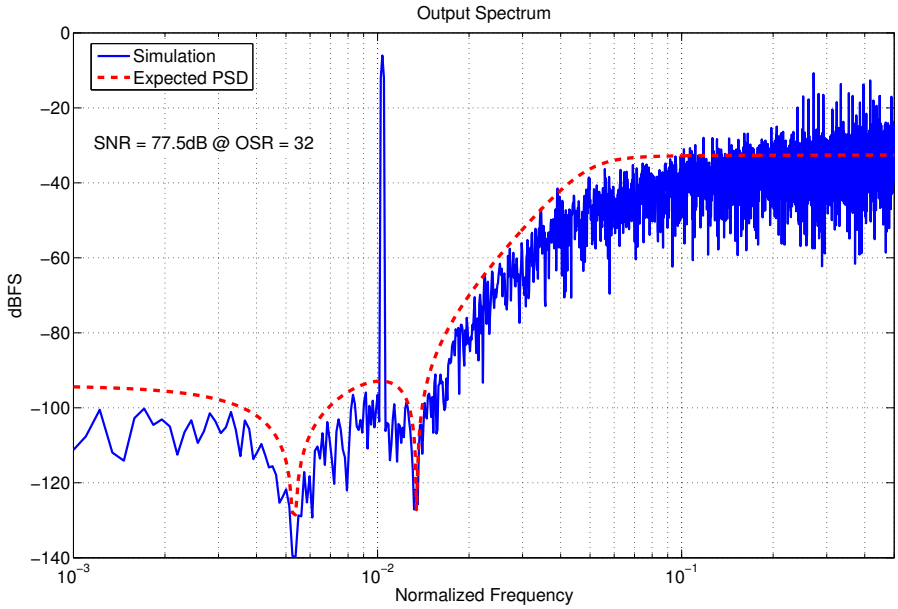

Figure 2.8: The simulated and expected power spectrum density (PSD) of fourth-order 1-bit modulator.

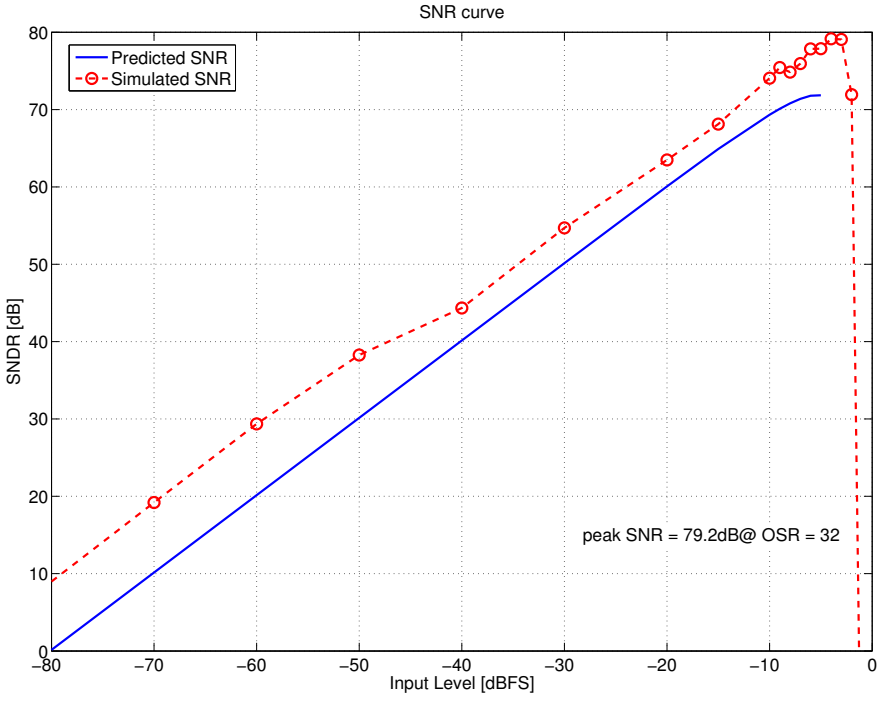

Figure 2.9: The predicted and simulated SNDR versus input level of FF fourth-order 1-bit modulator.

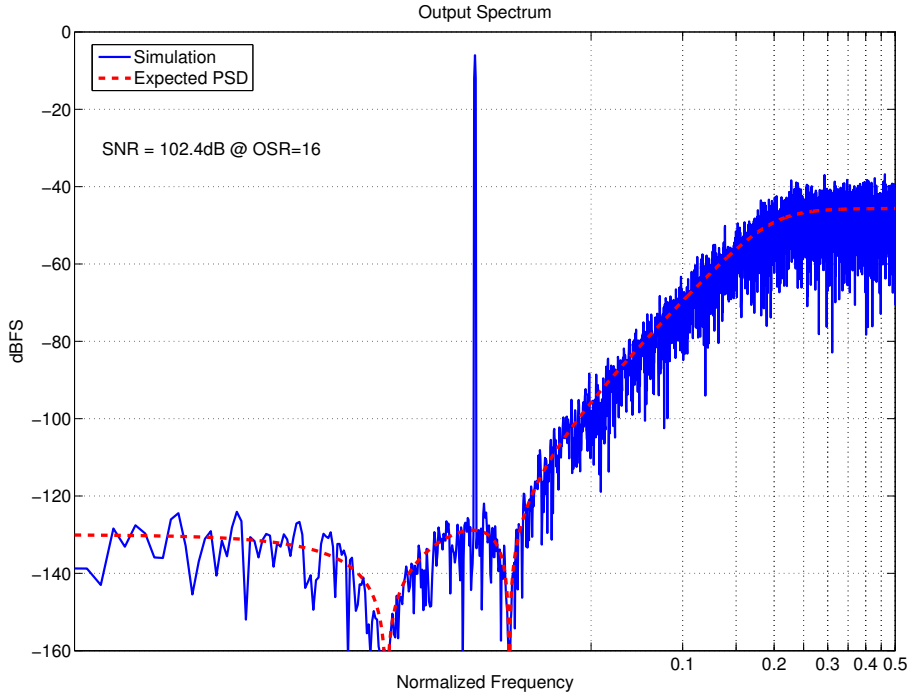

Figure 2.10: The simulated and expected power spectrum density (PSD) of fourth-order 4-bit modulator.

Table 2.1: Coefficients of fourth-order 4-bit CIFF modulator with an OSR of 16.

Coefficient	Value	Coefficient	Value
a1	2.8886	a4	0.3220
a2	3.3902	b1	0.0044
a3	1.8321	b2	0.0283

resolution. In order to convert the NTF into a set of coefficients for a particular topology, the "*realizeNTF*" function is used. Considering the cascade-of-integrators, feedforward form (CIFF) as shown in Figure 2.5, the resulting set of coefficients is listed in Table 2.1. Although the fourth-order 4-bit modulator has higher peak SNR and lower OSR compared with 1-bit one, a notable limitation of this modulator is that the linearity of the feedback DAC is not perfect. We can model the nonlinearities in an ADC system as additive noise sources as shown in Figure 2.1. The quantizer is replaced by two additive noise sources. The one labeled $E(z)$ represents the quantization errors of an ideal converter and $D(z)$ represents the errors due to the deviation of the internal DAC outputs from their ideal values. For noise shaping, the gain of must be large at low frequencies. Therefore, both quantization errors $E(z)$ is reduced by this large gain when they are referred back to the input $X(n)$. However, the nonlinearity of the internal DAC, $D(n)$, resides in the feedback path where its nonlinearities due to mismatches in levels are not reduced by the negative feedback. The

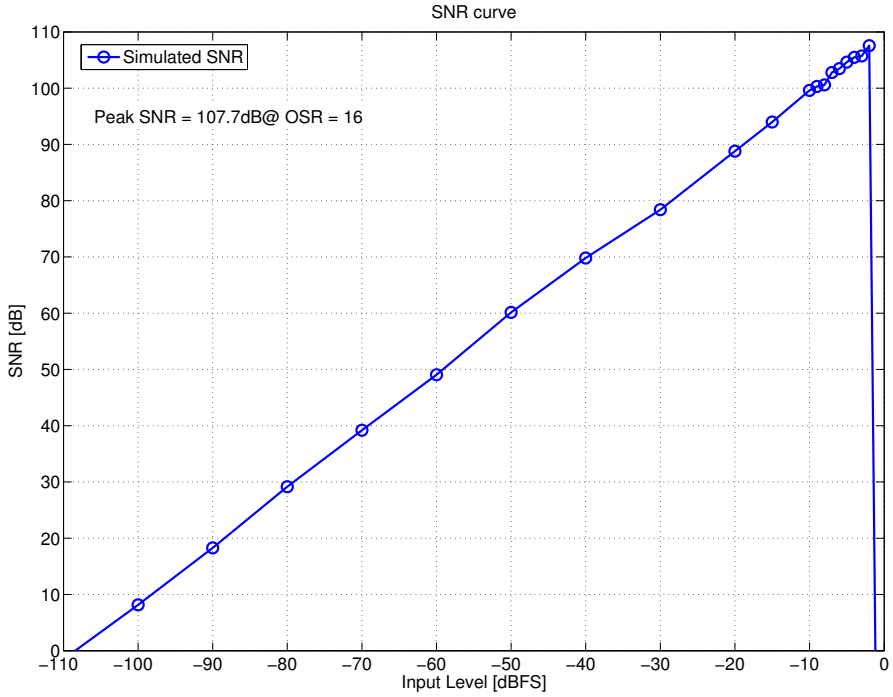

Figure 2.11: The simulated SNDR versus input level of FF fourth-order 4-bit modulator.

mismatch of the N-bit internal DAC will thus become an important factor of nonlinearity to whose ADC system.

2.2.2 Dynamic Element Matching

Element mismatches in the multi-bit feedback DAC introduce an output error, which consists of the harmonics of the input signal as well as an increased noise floor due to the folding of high-frequency quantization noise into the signal band. In some cases, the increased noise floor is acceptable, but the harmonic distortion is not. Thus, the dynamic Element matching (DEM) is a circuit technique for the randomization of the static nonlinearity of the DAC by converting the energy of the harmonic spurs into pseudo-random noise [19]. The concept of DEM for a parallel-unit-element DAC is shown in Figure 2.12 where the N^{th} output level is generated by connecting N unit elements to the output summing node. Since the error term ΔE_i of unit element E_i is only approximate but not exactly equal, two different output levels can be obtained by closing switches S_1, S_2 and S_1, S_3 namely, $2E + \Delta E_1 + \Delta E_2$ and $2E + \Delta E_1 + \Delta E_3$. In a multi-bit DAC without DEM, always the same set of switches are closed to implement the same output level while the DAC with DEM the sets of switches are changed dynamically controlling a given DEM algorithm. Then the DAC error will not be correlated with the value of is input, and hence the signal distortion

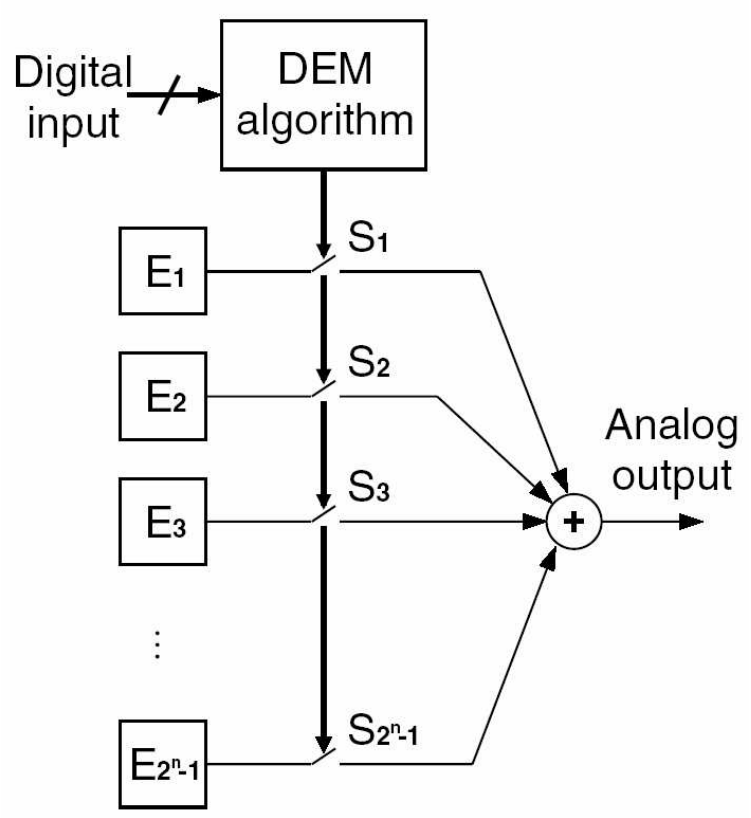

Figure 2.12: DAC with dynamic element matching linearization.

is replaced by random noise in the DAC output. To illustrate the effect of DEM, Figure 2.13 compares the output spectrum of a third-order CIFF modulator with a 3-bit quantizer and a fixed OSR of 32, without and with DEM. A ±1% linear-gradient mismatch is applied to the unit elements of the 3-bit feedback DAC. Accordingly, the DEM eliminates the large harmonic spurs caused by the DAC mismatch. However, as shown in Figure 2.12, DEM techniques requires some digital signal processing between the output of the quantizer and the input of the DAC. This causes an additional delay in the feedback path, thus limiting the maximum sampling frequency.

Since DEM techniques improve DAC linearity by the use of noise shaping, this improvement strongly depends on the capability of noise shaping namely OSR and loopfilter order. Broadband ΣΔ modulators require low OSR therefore the shaping capability have to maintain by increasing the loopfilter orders. The higher the order of the loopfilter, the higher complexity and delay of the DEM algorithms is. As a result, it turns out that in the case of low OSR and broadband applications, the modulator performance and DEM complexity becomes a trade-off. There are serval improved versions of DEM techniques were proposed for broadband ΣΔ modulators, such as data-weighted average (DWA) [20, 21, 22], Bi-DWA [34], individual level averaging (ILA) [23], digital correction or calibration [24, 25]. All of

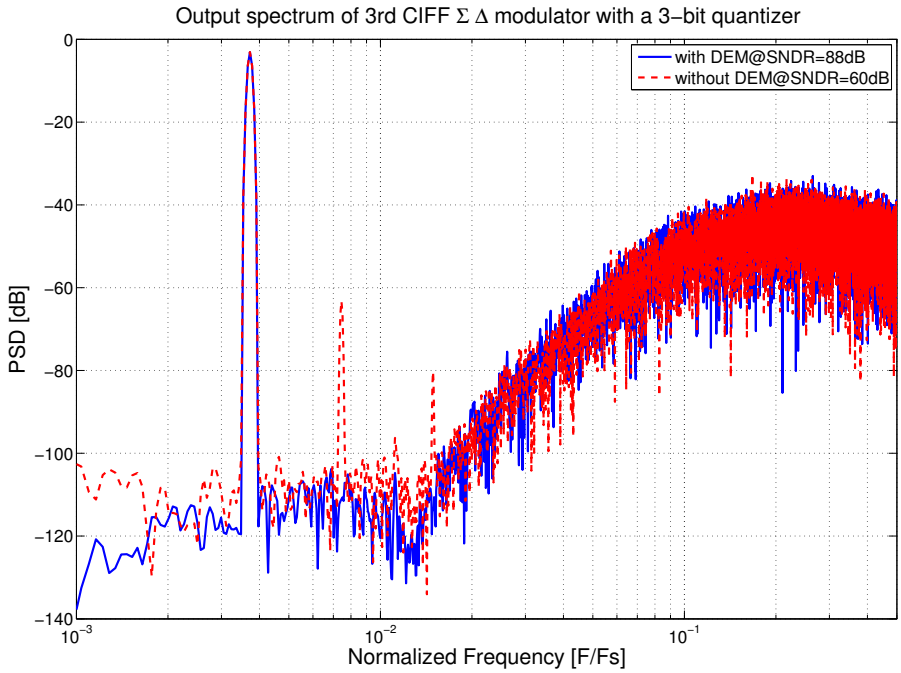

Figure 2.13: The output spectrum of a third-order 3-bit CIFF modulator with and without DEM.

these techniques require additional circuities and power dissipation.

2.3 Cascaded ΣΔ Modulator

The main difference between the cascaded and the single-loop ΣΔ modulator is the number of conversion stages. The single-loop modulator has only one conversion stage, while the cascaded modulator has more conversion stages. Figure 2.14 shows a block diagram of a possible implementation; several single-loop modulators can be seen, where each stage takes the error of the previous quantizer and digitizes it. The output streams are then combined in the error correction logic (ECL) in such a way that each quantization error e_{Qi}[k], but the one generated in the last stage, is cancelled. The result of this exercise is that, if every operation is exact, the remaining noise is shaped with an order equal to the sum of the orders of the employed loopfilters. Compared with single-loop high-order modulator, cascaded one, instead, do not need loops with $L > 2$ to achieve higher-order noise shaping. Hence, they have better stability and they usually reach higher DR at similar OSR, n, and L conditions. In addition, the architectures with cascaded loops also take advantage of the fact that the quantization noise is reduced when the residual error of an internal quantizer is amplified, before being converted by the following stage. The final DR is actually increased by the gain

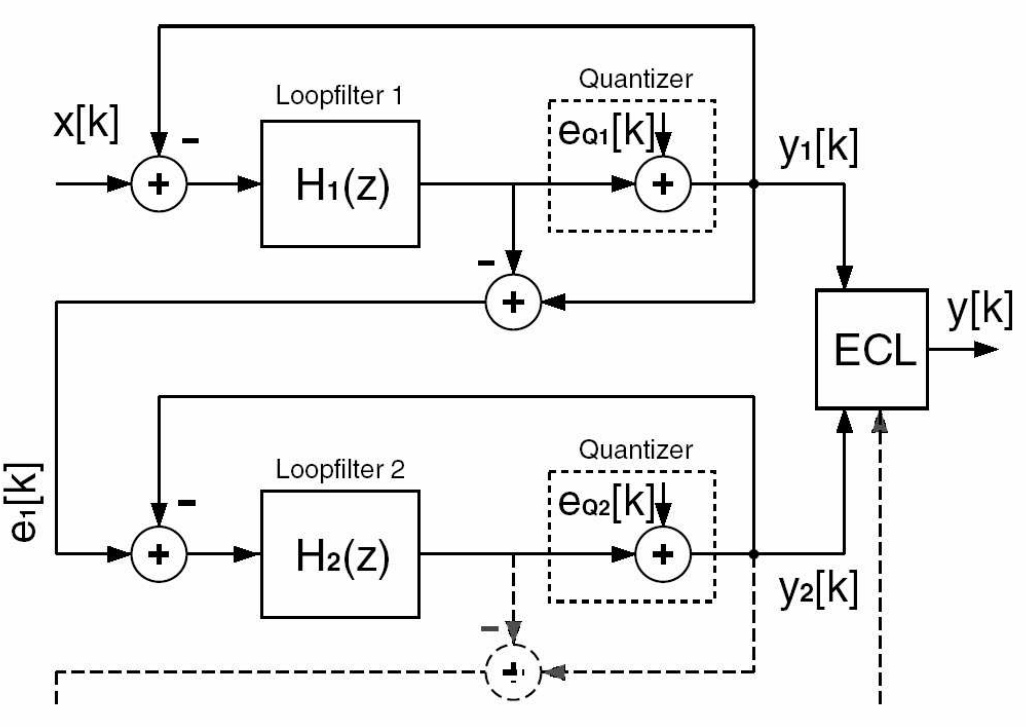

Figure 2.14: Cascaded ΣΔ modulator.

itself and may even exceed the value given by Equation (2.4).

2.3.1 Leakage Quantization Noise

Unfortunately the cascaded modulator requires a very accurate NTF of the first stage putting high specifications on the analog building blocks. The biggest problem of cascaded modulators is their sensitivity to mismatch between analog and digital circuities. In single-loop modulator a mismatch between the realized transfer function and the ideal designed filter degrades the stability of the loop. Nevertheless, it has been observed that coefficients variations of up to 20% and large integrator leakage, caused by amplifier finite gain can still be tolerated without a noticeable loss in performance. In contrast,the finite opamp dc gain and capacitor mismatch reshape the STF and NTF of a cascaded modulator and hence degrade the modulator performance. In order to explain the sensitivity of the cascaded modulator to the NTF accuracy, the operation of a cascaded 2-2 modulator (MASH2-2) is described. The block digram of MASH 2-2 can be referred as Figure 2.14 where $H_1(z)$ and $H_2(z)$ are second-order loopfilters. Assuming that the perfect match between the $NTF_1(z)$ (the first-stage NTF) and error correction logic $ECL(z)$ the output of the MASH 2-2 can be

given by:

$$Y_{MASH2-2}(z) = z^{-2}X(z) + d_1 ECL(z) NTF_2(z) E_{mb}(z) \tag{2.8}$$

where $X(z)$, $E_{sb}(z)$, and $E_{mb}(z)$ represent the input signal, 1-bit quantization noise, and multi-bit quantization noise, respectively.

In the ideal analysis, the dc gain of the op-amp is assumed to be infinite. However, this assumption is impossible to be achieved due to circuit limitations. In the presence of a finite-gain op-amp, the transfer function of a leaky integrator can be expressed as follows: [2]

$$I(z) = \frac{az^{-1}}{1-(1-\mu)z^{-1}} \tag{2.9}$$

where where μ denotes the inverse open-loop gain A_0 of the op-amp, and a is the integrator scaling factor. Based on Equation (2.9), the numerator of the NTFs can be approximately given by

$$NTF_{2nd}(z) \approx (1+2\mu)(1-z^{-1})^2 + \mu(\tilde{a}_1 + \tilde{a}_2)(1-z^{-1}) \tag{2.10}$$

where the coefficients $\tilde{a}_1$ and $\tilde{a}_2$ are two cumulative scaling factors of integrators. Thus, the resulting output noise powers of a second-order 1-bit modulator can be written as:

$$P_{2nd} \approx \frac{\Delta_{sb}^2}{12}\frac{1}{(a_1 a_2)^2}\left[\frac{\pi^4}{5}OSR^{-5} + \mu^2(\tilde{a}_1+\tilde{a}_2)^2\frac{\pi^2}{3}OSR^{-3}\right]. \tag{2.11}$$

Assuming a typical MASH 2-2 uses the multi-bit quantizer in the second stage, the output quantization noise power can be approximately given by:

$$\begin{aligned} P_{MASH2-2} \approx{}& \tfrac{\Delta_{sb}^2}{12}\tfrac{1}{(a_1a_2)^2}\left[\tfrac{\pi^4}{5}OSR^{-5} + \mu^2(\tilde{a}_1+\tilde{a}_2)^2\tfrac{\pi^2}{3}OSR^{-3}\right] \\ &+\tfrac{\Delta_{mb}^2}{12}\tfrac{1}{(a_3a_4)^2}\left[\tfrac{\pi^8}{9}OSR^{-9} + \mu^2(\tilde{a}_3+\tilde{a}_4)^2\tfrac{\pi^6}{7}OSR^{-7}\right]. \end{aligned} \tag{2.12}$$

where Δ_{sb} and Δ_{mb} represent the separation of the 1-bit and multi-bit quantizers for the first and second stages, respectively. According to Equation (2.12), the finite opamp gain arises the quantization noise power and thus degrades the achievable peak SNR.

Generally, the integrator gain can be achieved by the capacitor ratio in an SC modulator and thus capacitor mismatch affects the modulator performance due to the change of the

NTF. In the cascaded multi-bit modulator, however, the capacitor mismatch not only changes the NTF, but also leaks the single-bit quantization noise to the final modulator output. We first define the gain error of the integrator gain as:

$$a_1' = a_1(1 - \varepsilon_{a1}) \tag{2.13}$$

The *epsilon* represents the relative error of the analog coefficients, and can be calculated as:

$$\varepsilon_{a1} = \frac{\Delta a_1'}{a_1} \tag{2.14}$$

Substituting Equation (2.14) in Equation (2.8) yields the following modulator output:

$$\begin{aligned} Y_{MASH2-2}(z) \approx\ & z^{-2}X(z) + d_1 H_2(z) NTF_2(z) E_{mb}(z) \\ & +(1 - z^{-1})^2(1 - \varepsilon_g) E_{sb}(z) \end{aligned} \tag{2.15}$$

where $1 - \varepsilon_g = (1 - \varepsilon_{a1})(1 - \varepsilon_{a2})$. It is observed that the 1-bit quantization noise appears at the modulator output and dominates the total in-band noise power due to the lower order noise shaping. Taking the finite op-amp dc gain, capacitor mismatch and DAC error into account, combining Equations (2.12) and (2.15), the in-band power for the MASH2-2 can be approximated as:

$$\begin{aligned} P_{MASH2-2} \approx\ & \frac{\Delta_{sb}^2}{12}\frac{1}{(a_1 a_2)^2}\left[\frac{\pi^4}{5}OSR^{-5} + (1-\varepsilon_g)^2\frac{\pi^4}{5}OSR^{-5} + \mu^2(\tilde{a}_1 + \tilde{a}_2)^2\frac{\pi^2}{3}OSR^{-3}\right] + \\ & + \frac{\Delta_{mb}^2}{12}\frac{1}{(a_3 a_4)^2}\left[\frac{\pi^8}{9}OSR^{-9} + \mu^2(\tilde{a}_3 + \tilde{a}_4)^2\frac{\pi^6}{7}OSR^{-7} + \sigma_D^2\frac{\pi^4}{5}OSR^{-5}\right] \end{aligned} \tag{2.16}$$

where σ_D represents the power of the DAC error in the feedback path. The presence of leakage quantization noise from the 1-bit quantizer, the last term in Equation (2.16), limits the achievable resolution of the MASH 2-2 modulator. Figure 2.15 shows the output spectra of a MASH 2-2 modulator with 1-bit and 4-bit quantizers in the first and second stages respectively where the 60dB OTA dc gain and 0.1% capacitor mismatch are assumed. Obviously, the leakage noise seriously degrades the performance of cascaded modulator for low-OSR application.

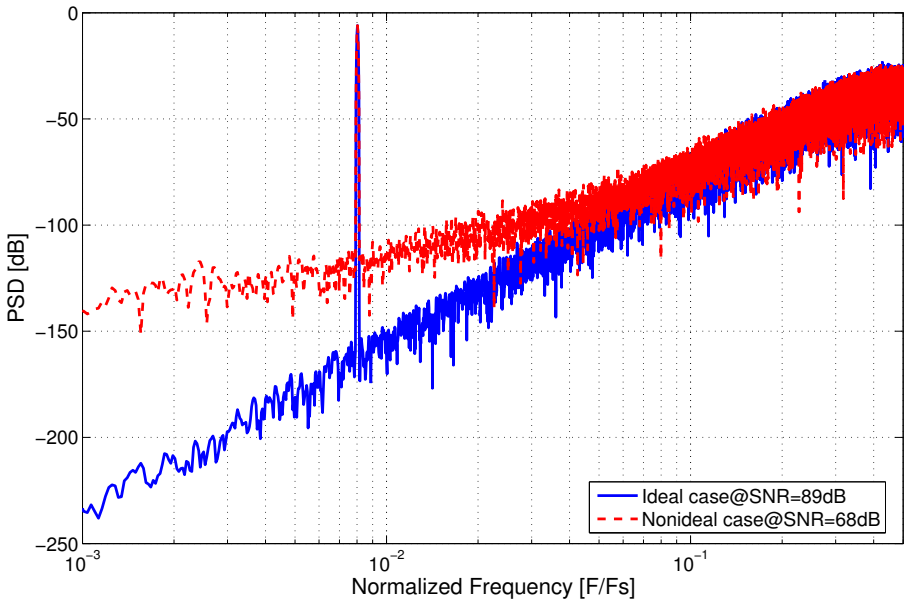

Figure 2.15: The output spectrum of MASH 2-2 with finite OTA dc gain and capacitor mismatch.

2.4 Summary

In Section 2.1 the CT modulator have been introduced and its architectural characteristics are also reviewed. The CT modulator has good potentiality for broadband applications since their sampling clock rate are usually three times faster compared to a DT solution. However, the variation of RC time constant, clock jitter, and excess loop delay of the CT modulator seriouly degrades the performance, thus limiting the achievable DR.

The DT modulator can be divided into two parts based on their loopfilter types, single-loop architecture and cascaded architecture. The single-loop high-order modulators with have been widely applied to broadband applications because of having lower sensitivity to the finite dc gain of opamps and capacitor mismatch. However, the instability of single-loop high-order modulators with 1-bit quantizer limits their capability of noise shaping, thus resulting in a poor SNR for broadband applications. The single-loop high-order modulators with multi-bit quantizer not only relax the instability of loopfilter but also increase the achievable DR. However, the distortion caused by multi-bit feedback DAC degrades the SNDR. It is unacceptable for broadband telecommunication applications. Several circuit techniques have been proposed to reduce the distortion caused by multi-bit feedback DAC at the expense of increasing circuit complexity and power dissipation.

The cascaded modulators combine serval low-order stages in the ECL to generate the desired high-order NTF. Since no high-order loopfilter is used, they have better stability

and they usually reach higher DRs compared with single-loop ones. However, cascaded modulators are sensitive to the finite dc gain of opamps and capacitor mismatch due to the leakage quantization noise in the ECL output. Thus, the performance degradation strongly depends on the specifications of analog building blocks, which increases the circuit design challenges. This degradation becomes worse when the OSR is low and the multi-bit quantizer is used in last stage. Although some digital calibration techniques can reduce leakage quantization noise, they usually require complex digital processing.

The next two chapters will describe two new cascaded modulators for broadband telecommunication applications. The first one is a cascaded 2-1-1 modulator with 1.5-bit quantizer to achieve high DR and low OSR for the newly asymmetric digital subscriber line (ADSL2+) standard. The architectural analysis, circuit implementation, and experiment result will be given. The second one is a resonator-based cascaded modulator in which a new operating principle is present to improve the DR loss caused by leakage quantization noise. The theory analysis, architecture design, and simulation results will be addressed.

Chapter 3

A Fourth-Order Cascaded ΣΔ ADC for ADSL2+ Application

Asymmetric digital subscriber line (ADSL) technology can use the plain old telephone service (POTS) consisting of the existing telephone lines, on-site transceivers and shared exchange multiplexers to deliver high-rate digital data [26]. Since the POTS has different degree's of quality and different lengths, a new modulation technology called Discrete Multi-tone (DMT) is used to allow the transmission of high speed data. Such transmission is paid with an increased accuracy in the detection of the modulated signals, which requires analog-to-digital converters (ADCs) with a resolution in the range of 13-15 bits. Today, the newly released ADSL standard called ADSL2+ is a double frequency band version of ADSL2 [27]. The ADSL2+ system increases the frequency ranges on the transmission line from 1.1 MHz to 2.2 MHz as shown in Figure 3.1. This has the potential to increase the short-loop data transmission rate up to 26 Mbps (downstream) as shown in Figure 3.2 [27]. Although ADSL2+ provides higher data rates, it increases the design challenge of the ADCs in the analog front-ends (AFEs). High resolution and broad bandwidth are not only requirements for an ADSL2+ ADC. The power dissipation is also an issue since the limited available energy in mobile device or in the powered modems. Thus, how to choose the ADC architecture for optimizing the trade-off among power, resolution and bandwidth becomes a key issue.

Pipelined and ΣΔ converters, among the existing ADC architectures, are most suitable candidates to meet the requirements of ADSL2+ standard. Generally speaking, pipelined ADCs can achieve broad bandwidth, but have limited dynamic range (DR), high power dissipation, and large silicon area. On the other hand, the state-of-the-art ΣΔ ADCs can achieve high DR and wide bandwidth with noise shaping and oversampling techniques. Pa-

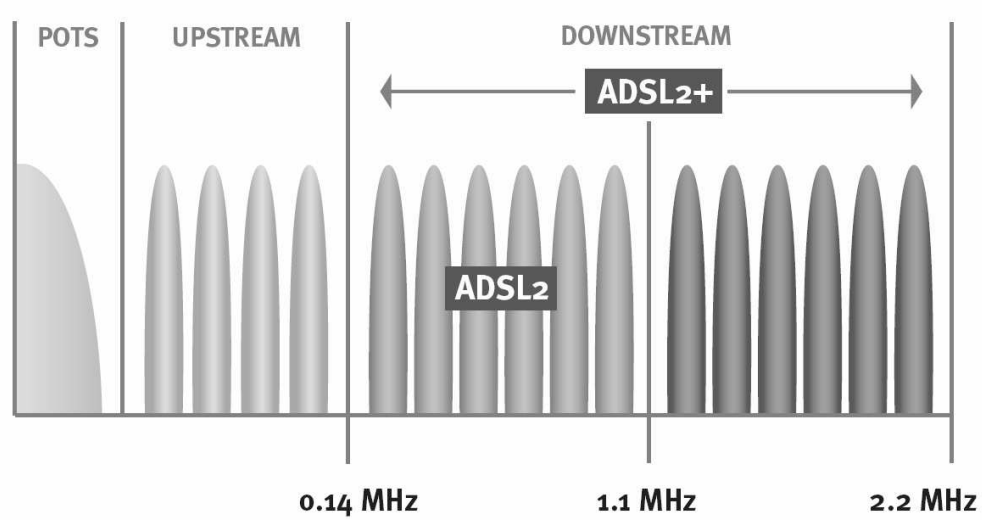

Figure 3.1: Signal bandwidth of ADSL2 and ADSL2+.

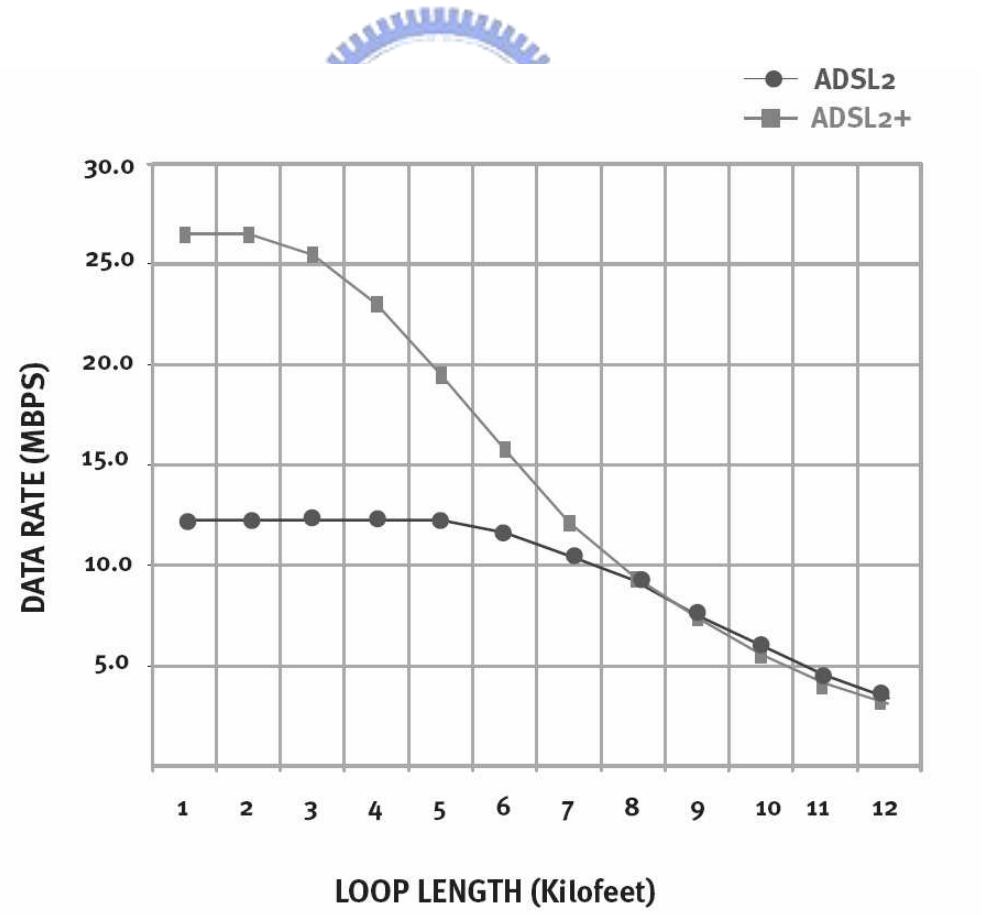

Figure 3.2: Maximum date rate of ADSL2 and ADSL2+.

pers [28, 29] have presented single-bit cascaded ΣΔ modulators for ADSL application, which achieved 15-bit resolution and 1.1 MHz signal bandwidth with an OSR of 24. To further extend the signal bandwidth and reduce the OSR, several papers [30, 31, 32, 33, 34] have presented modulators with high-order multi-bit topologies. As shown in their results, they can achieve 13-bit (or above) and up to 2 MHz of signal bandwidth when the OSRs range from 8 to 24. However, the use of the multi-bit quantizer requires data weighted averaging (DWA) algorithms to solve the nonlinear problem of multi-bit digital-to-analog converters (DACs). The DWA circuits usually consume extra power (say 30 40mW with 2.5-V supply) [33], [34] and cost additional silicon area. Papers [35], [36] instead of using DWA, use the cascaded architecture with the single-bit quantizer in the first stage and multi-bit quantizer in the last stage to relieve the linearity requirement of feedback DACs. Ideally, they can achieve high dynamic range for low-OSR design. Yet, in practical, the leakage quantization noise of such architectures may limit achievable dynamic range, and the multi-bit quantizer of the last stage may increase circuit complexity and power dissipation. Recently, paper [37] presents a single-loop fifth-order modulator with a 1.5-bit quantizer popular in pipelined ADCs, to achieve high dynamic range and consume low power for ADSL applications. Accordingly, this chapter describes the design methodology, circuit implementation, and experimental result for a cascaded ΣΔ modulators taking the advantage of the 1.5-bit quantization to perform good trade-offs among power consumption, dynamic range and signal bandwidth.

3.1 Architecture

The discussion for the architectural consideration of a broadband ΣΔ modulator has been given in Chapter 2. Accordingly, an intuitive and most important guideline is the design of the modulator with a low OSR. Since the OSR is bounded, the order L of the loopfilter and the number of bits n of the quantizer are the remaining free parameters to determine the achievable DR. The high-order (L>4) loopfilter is essential for low-OSR design (say, <32). High-order single-loop structure is a good choice for implementing the broadband ΣΔ modulator. However, the achievable DR of such modulator with 1-bit quantizer is greatly limited due to the loopfilter instability. By using multi-bit quantizer, the single-loop modulator can achieve high DR and low OSR at the expense of increasing circuit complexity of the feedback DAC.

Alternative choice for the implementation of high-order loopfilter is the use of cascaded

structure. It cascades several low-order ($L \leq 2$) stages to realize the high-order loopfilter, thus relaxing the loopfilter instability. The number of bits of the quantizer in each stage can be the 1-bit or multi-bit . Ideally, the quantization noise is only determined by the number of bits of the quantizer in the last stage. However, the nonidealities of analog circuity such as finite opamp gain, capacitor mismatch, usually limit the achievable DR. This section addresses the architectural design of a low-OSR 1.5-bit cascaded $\Sigma\Delta$ modulator with small silicon area and low power dissipation. Three architectural approaches are applied for the proposed cascaded $\Sigma\Delta$ modulator [38, 39]. First of all, the structure of the proposed cascaded modulator is 2-1-1 where uses the 1.5-bit quantizer and DAC in each stage. Comparing with single-bit quantizer, the 1.5-bit quantizer can reduce the quantization noise and result in larger inter-stage gain and, hence, larger DR. Since the 1.5-bit DAC suppresses the nonlinearity of the DAC to the required performance, the proposed modulator does not need DWA algorithm. Secondly, to improve the signal-to-noise ratio (SNR) of the modulator for low-OSR design, we employ a resonator-based topology in the first stage. The resonator-based topology adds in-band zeros in the noise transfer function (NTF) and hence suppresses the quantization noise over the signal band [2]. Furthermore, by adding an input feed-forward path into the first stage, the swing ranges and distortions of integrator outputs are reduced [22], [40]. Although this arrangement raises objections due to the increased difficulty of analog-digital mismatch (i.e. leakage quantization noise), with properly scaling the coefficients of the resonator, the proposed modulator can still achieve more than 80-dB SNR in case the capacitor mismatch is 0.5% and the opamp dc gain is 70-dB. Finally, we employed two different pairs of reference voltages for comparators and DACs to enhance the achievable DR; a pair of 0.9-V is used in the first stage and another pair of 0.45-V in the succeeded stages. A functioned ADC for ADSL2+ has been realized in the 0.25-μm CMOS technology using the proposed $\Sigma\Delta$ modulator. To produce the Nyquist-rate signal, following the $\Sigma\Delta$ modulator, a three-stage digital decimation filter is designed and implemented. The decimation filter consists of a fifth-order comb filter, a 31-tap FIR filter, and a fourth-order IIR filter. As shown in the experimental results, the ADC, for a 2.2MHz signal bandwidth, can achieve a DR of 86 dB and a peak SNDR of 78 dB. It costs an active area of 2.8-mm^2 and consumes 180 mW from a 2.5-V supply voltage.

The details for the analog modulator design, nonlinearity effect analysis, and decimation filter design will be discussed in the next sections.

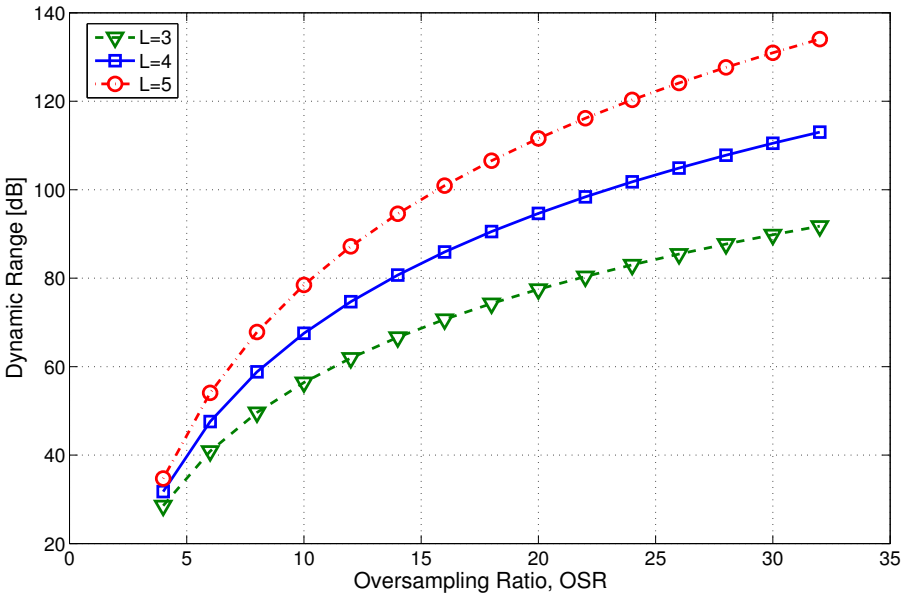

Figure 3.3: Dynamic range of a conventional 1.5-bit ΣΔ modulator with L=3, 4, and 5, as a function of OSR.

3.1.1 Design of Analog Modulator

The most important issue for the design of a ΣΔ ADC is to determine the order, topology, and the coefficients of the modulator loopfilter. The optimal loopfilter design can achieve the required DR with the minimum cost of resource, i.e., with the small silicon area and power dissipation. The silicon area and power dissipation for a switched-capacitor (SC) circuit implementation are mainly determined by the orders of loopfilters and values of the capacitances. The first consideration of loopfilter design should be the orders and the segments. The theoretical DR of a ΣΔ modulator with typical pure differentiation noise transfer function (NTF) depends on the oversampling ratio, OSR, the order of loopfilter L, the quantizer resolution N, and can be given as follow [2]:

$$DR = \frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N-1)^2 OSR^{2L+1}. \tag{3.1}$$

Figure 3.3 plots the DR as a function of OSR for third-, fourth-, fifth-order loopfilter with 1.5-bit quantization. According to Figure 3.3, the DR improvement for high-order loopfilter becomes saturation when OSR is below 8, which determines the minimum required OSR. Since the targeted DR for ADSL2+ is over 86dB (say, 14-bit), the minimum required OSRs for the loopfilter order of L=3, 4, and 5 are 26, 16, and 12, respectively. Although fifth-order modulator has lowest OSR, it actually will not provide significant improvement than

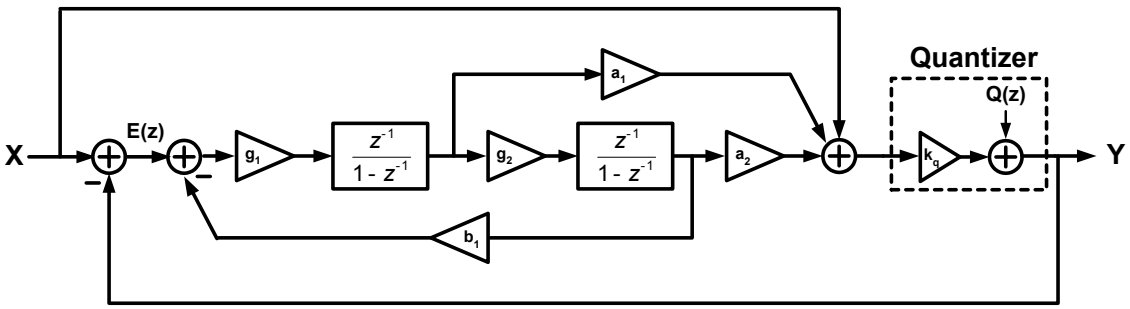

Figure 3.4: Resonator-based second-order 1.5-bit modulator.

the fourth-order one due to the larger leakage quantization noise [2]. In this work, the fourth-order 1.5-bit cascaded modulator with an OSR of 16 was chosen to be the decision.

While the order of loopfilter is fixed, the segmentation of cascaded loopfilter should be determined especially for the order and topology of the first stage. Since the first stage processes the input signal and generates the quantization noise to the succeeded stages, the performance of entire modulator is bounded by behaviors of the first-stage topology, such as noise-shaping capability, linearity, and tone behavior. To design a high dynamic range, low-power $\Sigma\Delta$ modulator for ADSL2+ application, a resonator-based, second-order modulator is used in the first stage as shown in Figure 3.4. It uses a low-Q resonator-based loop filter that introduces a pair of zeros into the NTF. The NTF of this resonator-based modulator can be expressed as:

$$NTF(z) = \frac{1 - 2z^{-1} + (1+r)z^{-2}}{1 - (2 - k_q c)z^{-1} + (1 + r + k_q d - k_q c)z^{-2}} \tag{3.2}$$

where $c = g_1 a_1$, $d = g_1 g_2 a_2$, and $r = g_1 g_2 b_1$. Note that r is the loop gain of the resonator and k_q is the gain of the quantizer. The zeros of NTF create a notch around the edge of signal band and hence suppress the in-band quantization noise. The suppression can significantly improve the signal-to-noise ratio (SNR) of modulators, especially for low OSR modulator [2]. The feedforward path from input to the adder followed by the quantizer is used to reduce the distortion caused by integrator nonidealities [22]. Equation 3.3 shows the signal transfer function (STF) induced by the feedforward path.

$$STF(z) = \frac{k_q[1 - (2 - d)z^{-1} + (1 + r + c - d)z^{-2}]}{1 - (2 - k_q d)z^{-1} + (1 + r + k_q c - k_q d)z^{-2}}. \tag{3.3}$$

Based on Equation (3.3), the error signal E(z) (=X(z)-Y(z)) becomes:

$$\begin{aligned} E(z) &= [1 - STF(z)]X(z) - NTF(z)Q(z) \\ &= (1 - k_q)NTF(z)X(z) - NTF(z)Q(z). \end{aligned} \tag{3.4}$$

In Equation (3.4), the term of $(1-k_q)$ can be treated as the impact factor of $X(z)$ to $E(z)$. Obviously, the smaller the impact factor is, the less sensitive the loop filter is to input signal. When k_q is a unity, the $E(z)$ does not have the component $X(z)$ and the integrators of the loop filter will only process the quantization noise $Q(z)$. In this case, the distortion caused by integrator nonidealities can be significantly reduced [22]. Unfortunately, k_q cannot be a unity in practical design because there always exists quantization error between input and output of a quantizer. In case of using the 1-bit quantizer, k_q is varying with the input signal of quantizer and its value can be much greater than a unity. The variation of k_q causes the sensitivity of loop filter to input signal to be high. To take the advantage of making k_q a unity, one can use the multi-bit quantizer to lower the sensitivity as much as possible [22]. Nevertheless, when using the multi-bit quantizer, the modulator requires the data weighted averaging (DWA) algorithm to compensate the nonlinearity of the multi-bit DAC. Here we replace multi-bit quantizer with a 1.5-bit one in that the k_q variation of 1.5-bit quantizer can be reduced and the perfomacne is improved as compared with 1-bit quantizer. Although the 1.5-bit DAC introduces distortion, the 14-bit linearity can be achieved by careful sizing of transistors composing the OTA and symmetrical layout [41].

The mostly popular fourth-order cascaded architectures are MASH 2-2 and MASH 2-1-1. An in-depth study on comparison of 2-2 and 2-1-1 cascaded architectures has been presented in [42]. Figure 3.5 illustrates the block diagram of two fourth-order resonator-based cascaded $\Sigma\Delta$ modulators, which are referred to as RMASH 2-1-$1_{1.5b}$ and RMASH 2-$2_{1.5b}$. The first stage of the RMASH 2-1-$1_{1.5b}$, as mentioned above, uses the resonator-based modulator and the following two stages are the conventional first-order modulators. The $H_1(z)$ and $H_2(z)$ in Figure 3.5(a) denote the digital error cancellation logic, which are used to cancel the first- and second-stage quantization noise of RMASH 2-1-$1_{1.5b}$. The transfer functions of $H_1(z)$ and $H_2(z)$ are deduced

$$\begin{aligned} H_1(z) &= 1 - 2z^{-1} + (1 + r)z^{-2}, \\ H_2(z) &= (1 - z^{-1}) \cdot [1 - 2z^{-1} + (1 + r)z^{-2}]. \end{aligned} \tag{3.5}$$

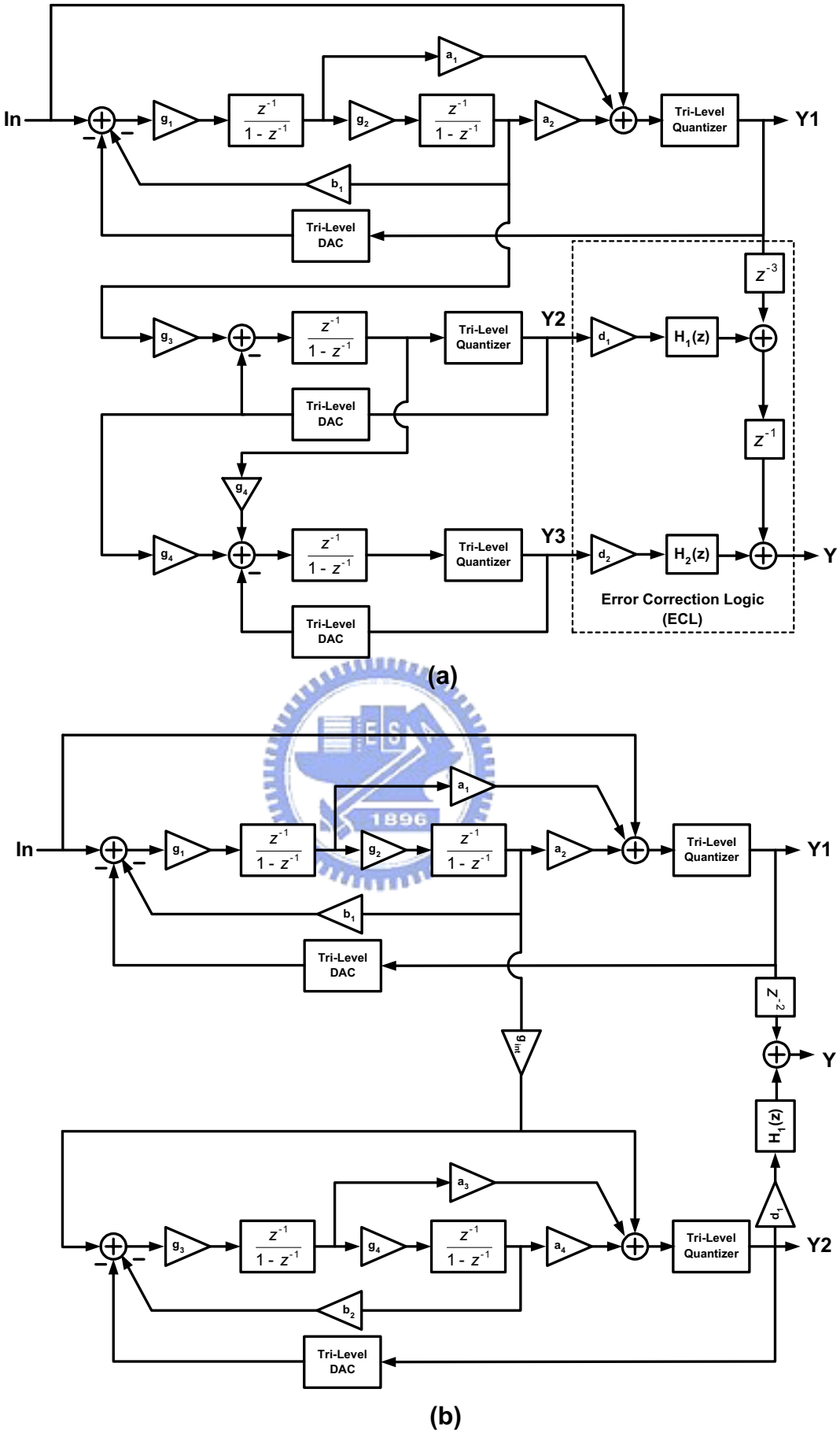

Figure 3.5: The block diagrams of (a) RMASH 2-1-$1_{1.5b}$ (b) RMASH 2-$2_{1.5b}$.

With ECL, the NTF of RMASH 2-1-$1_{1.5b}$ is given by:

$$Y(z)/Q_3(z) = d_2[1 - 2z^{-1} + (1 + r)z^{-2}] \cdot (1 - z^{-1})^2, \tag{3.6}$$

where $Q_3(z)$ is the quantization noise of tri-level quantizer in the third stage and d_2 is the inverse of $g_1g_2g_3g_4$. Obviously, the SNR can be improved by tuning parameters, d_2, r, and $Q_3(z)$. With the careful selection of the resonator loop gain r, the NTF zeros can produce a notch near the edge of the signal band to suppress the quantization noise over the desired signal band. According to [18], the NTF zeros are placed at the corner frequency of the signal band, and the value of r can be chosen by the following expression.

$$r = g_1g_2b_1 \approx \left[2\pi \cdot (f_{notch}/f_s)\right]^2. \tag{3.7}$$

At the OSR of 16, with in-band zeros, the fourth-order NTF can improve the SNDR by 14-dB.

3.1.2 Analysis of 1.5-bit quantization

The 1.5-bit quantization technique has been proved to be able to achieve high dynamic range without using DWA circuitry [41]. In our work, the use of 1.5-bit quantization is twofold: (1) to keep the impact factor of X(z) to E(z) lower than that of the single-bit quantizer so the performance can meet the requirement of ADSL applications, and (2) to have the nonlinearity of feedback DAC lower than multi-bit quantizers so that the DWA is not a necessity for high dynamic range. Based on Equation (3.3), the input signal X(z) and quantization error Q(z) are the two input sources of the first integrator. Since the Q(z) is assumed to be a white noise, the term $(1\text{-}k_q)NTF(z)X(z)$ becomes the major distortion source of the first integrator. Thus, to reduce the harmonic distortion, the term $(1\text{-}k_q)$ has to be as small as possible. From [37], the "*equivalent gain*" of a quantizer is defined as:

$$k_q = \frac{rms(V_o)}{rms(V_i)} = \lim_{n\to\infty} \sqrt{\frac{\sum_{n=1}^{N} V_o^2[n]}{\sum_{n=1}^{N} V_i^2[n]}}, \tag{3.8}$$

where V_o and V_i are the output voltage and input voltage of the quantizer, respectively. The equivalent gain can only be used to evaluate the static performance of modulator. In order to observe the dynamic performance of distortion, we defined the $k_q(n)$ as $V_o(n)/V_i(n)$ and

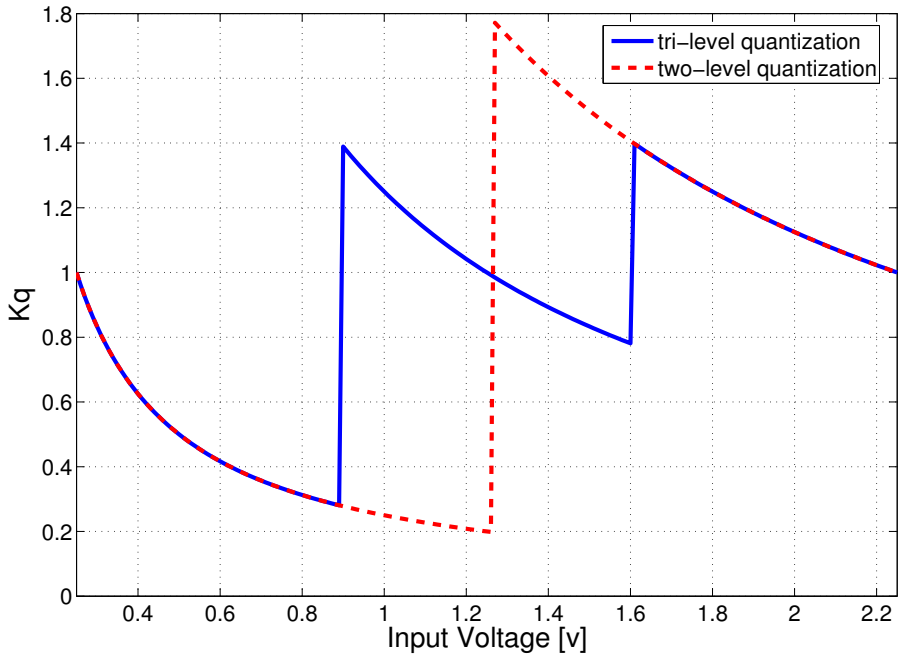

Figure 3.6: The nonlinear gain of 1.5-bit and 1-bit quantizer.

the output voltage of the tri-level quantizer as:

$$V_o(n) = \left\{ \begin{array}{ll} V_{cm} + V_R & if\ V_i \geq V_{cm} + V_{th} \\ V_{cm} & if\ V_{cm} + V_{th} > V_i > V_{cm} - V_{th} \\ V_{cm} - V_R & if\ V_i \leq V_{cm} - V_{th} \end{array} \right\} \tag{3.9}$$

where V_{cm} and V_{th} are the common-mode voltage and threshold voltage of the quantizer, respectively. Here we calculate the k_q for both tri-level and two-level quantizers by considering practical design condition. If the voltage set [V_{cm}, V_{R+}, V_{R-}] is equal to [1.25V, 1V, 0.35V], Figure 3.6 plots the k_q versus input voltage for both tri-level quantizer and two-level quantizer. As shown in the plot, the variation of (1-k_q) of the tri-level quantizer is narrower than that of the single-bit quantizer. Hence, the use of tri-level quantizer can lower the sensitivity of the loop filter to input signal.

The characteristic and nonlinearity of a tri-level DAC can be briefly described in Figure 3.7(a). The horizontal axis represents the digital input codes while the vertical axis represents the analog output levels, which can vary due to circuit nonidealities. The nonlinearity is then defined by the displacement, ε, of medium level. With an approximation by using quadratic polynomial as shown in Figure 3.7(b), the nonlinear error function of tri-level DAC can be

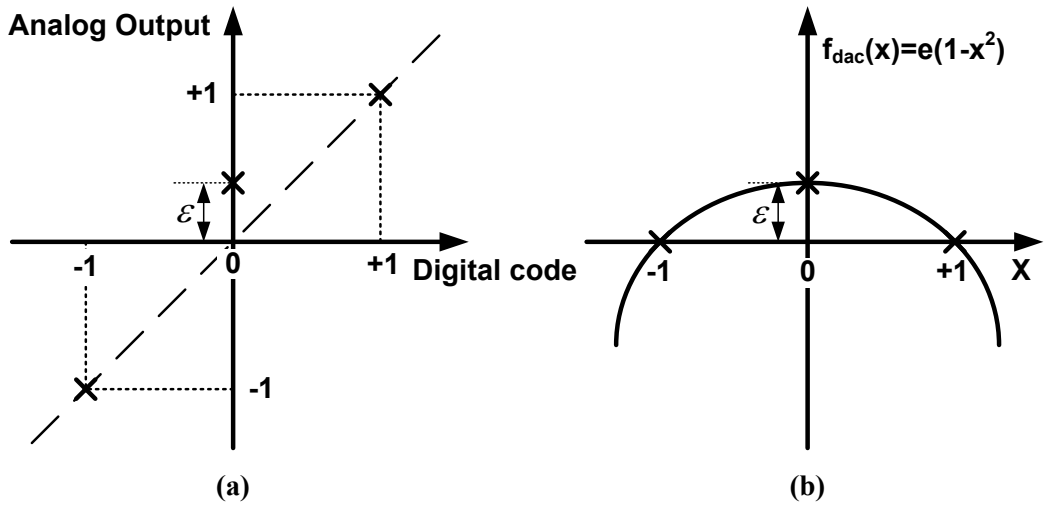

Figure 3.7: (a) transfer characteristic and (b) error function of tri-level DAC.

expressed as:

$$e_{DAC}(x) = \varepsilon(1 - x^2). \tag{3.10}$$

According to the analysis of paper [41], the well-sizing of the transistor of OTA and symmetrical layout will result in an ε of 0.01%, which enables 14-bit linearity.

To see if the tri-level quantizer is good enough for the ADSL2+, we applied single-bit quantizer and tri-level quantizer for the resonator-based modulator respectively and observed the third harmonic distortion. Considering a nonideal integrator with finite unity gain frequency (GBW), the output voltage of the integrator is given by

$$v_o(t) = v_o(nT_s - T_s) + V_s\left(1 - e^{-\frac{t}{\tau}}\right),\ 0 < t < \frac{T_s}{2} \tag{3.11}$$

where $V_s = V_{in}(nT_s - T_s)$ and τ=1/(2πGBW). With a finite GBW, the incomplete settling causes the harmonic distortion in the integrator outputs. Given V_{th}=0.45 V, OSR=16, f_s=70.4 MHz, and GBW=240MHz, we employed sinusoids with -6 dB and 500 kHz as the input signals to simulate the output harmonic distortion of the first integrator. Figure 3.8 shows a sketch of the third harmonic distortion results for the first integrator with tri-level quantizer and single-bit quantizer. As shown in Figure 3.8, the third harmonic distortion of resonator-based modulator with tri-level quantizer is lower than -90 dB and hence its linearity can be greater than 90 dB. Comparing with the single-bit version, the use of tri-level quantizer lowers the sensitivity of the loop filter to input signal and consequently reduces the distortion caused by integrator setting error. Furthermore, the linearity of 90 dB is higher

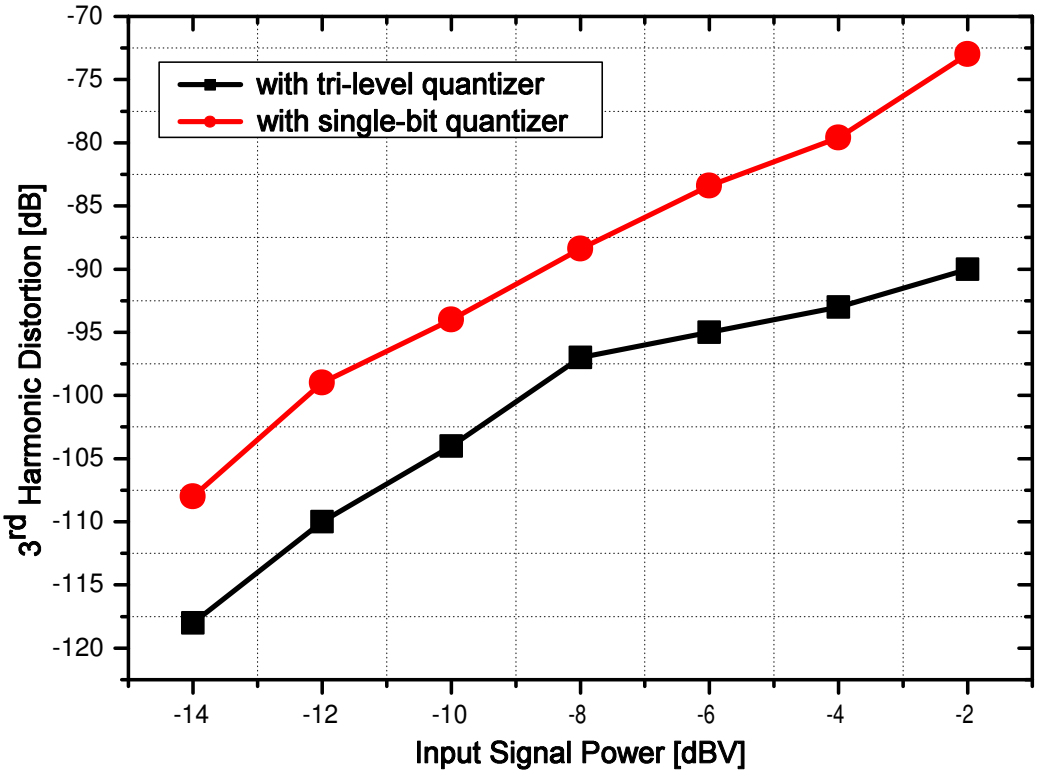

Figure 3.8: The simulated 3rd harmonic distortion of resonator-based modulator with tri-level and single-bit quantizers. (V_{th}=0.45V, fin=500KHz, OSR=16, fs=70.4MHz)

than the requirement of 14-bit ADC (say 86 dB) so it is possible for us to makes the overall ADC achieve 14-bit resolution without using DWA.

3.1.3 Two Pairs of Reference Voltages

Furthermore, we applied two pairs of reference voltages (TPRVs) for the proposed modulator; a pair of ±0.9V for the tri-level quantizer of first stage and another pair of ±0.45V for the quantizers in the second and third stages. The high voltage pair can have the first stage operated at high dynamic range while the low voltage pairs can reduce the output swing of the second stage and the power of $Q_3(z)$. Based on Equation (3.6), the theoretical quantization noise (TQN) can be expressed as:

$$TQN_{rms} \approx 20\log_{10}\left(\frac{\Delta d_2 \pi^4}{108}\right) + 20\log_{10}\left(\frac{1}{OSR}\right) \tag{3.12}$$

where Δ is the step size of tri-level quantizer in the third stage. Accordingly, two paraments d_2 and Δ can be used to reduce the TQN of the modulator. Firstly, the reduction of the output swing of the second stage implies the integrator gain of g_4 can be increased. Since the $d_2 = 1/g_1g_2g_3g_4$, the TQN can be reduced by reduction of d_2. In gerneal, the d_2 with

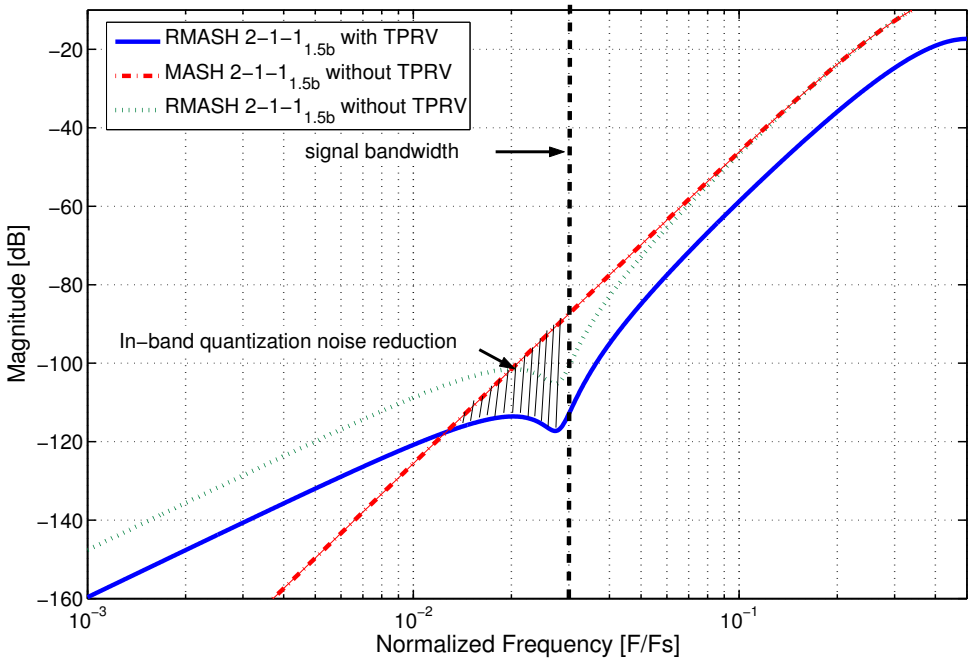

Figure 3.9: The TQN plots of RMASH 2-1-1$_{1.5b}$ with TPRVs, MASH 2-1-1$_{1.5b}$ without TPRVs, and RMASH 2-1-1$_{1.5b}$ without TPRVs.

TPRVs can be half of that without TPRVs, which increases the TQN of RMASH 2-1-1$_{1.5b}$ by 6dB. Furthermore, the additioanl 6dB of SNR is gained by halving the reference voltage of third stage since the step size Δ of tri-level quantizer is one-half of that without TPRVs, which totally increases the TQN of RMASM 2-1-1$_{1.5b}$ by 12dB. The use of TPRVs only affects the scaling gain d_2 and does not change the frequency responses of NTF and ECL equations. Although the SNR of the modulator is enhanced, this arrangement increases the effect of the leakage quantization noise caused by capacitor mismatch and finite OTA DC gain. Fortunately, the desired SNR still can achieve 90 dB with 0.1% of capacitor mismatch and 70 dB of OTA DC gain. Using the same design methodology, the RMASH 2-2$_{1.5b}$ can achieve similar performance to RMASH 2-1-1$_{1.5b}$. One can apply the second-order resonator-based modulator to either stage or both stages of the RMASH 2-2$_{1.5b}$.

Given the OSR of 16 and the d_2 of 2, Figure 3.9 shows the NTFs of the proposed RMASH 2-1-1$_{1.5b}$ with TPRVs, conventional MASH 2-1-1$_{1.5b}$ without TPRVs, and RMASH 2-1-1$_{1.5b}$ without TPRVs. We can see the performance gain of 20 dB in the shadow region. Figure 3.10 illustrates the SNR versus OSR in comparison of the fourth-order modulators using 1.5-bit quantizer. To achieve the SNR of 90-dB (or higher), the single-loop architecture needs to operate at the OSR of 32 while the others need the OSR of 16. The lower OSR implies the lower power dissipation. To optimize the load of the second integrator of first-stage

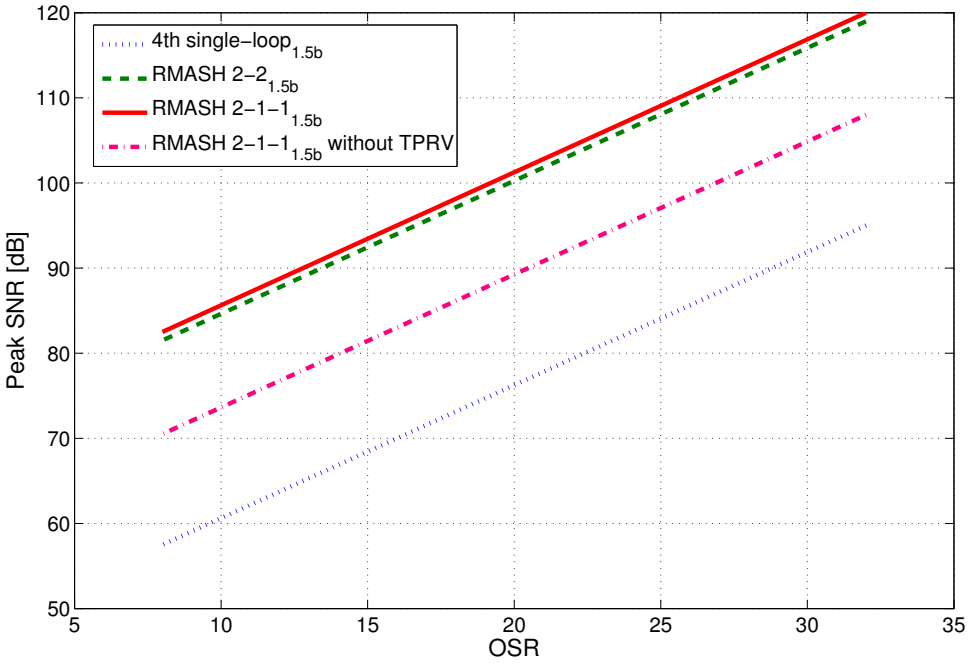

Figure 3.10: The peak SNDR versus OSR plots for four different modulators.

modulator and trade off the dynamic range of the opamp in the following stages, here we adopt the RMASH 2-1-$1_{1.5b}$ as our design target.

The high reference voltages, ±0.9V, are used in the first stage and their settling error directly limits the performance of overall modulator. Thus, the reference buffers for ±0.9V thus require fast settling, which increases the static current and the value of decoupling capacitor. However, the settling error of the low reference voltages,±0.45V, for second and third stages can be relaxed by the second-order and third-order high-pass noise shaping of H1(z) and H2(z), respectively. Figure 3.11 shows the simulated peak SNDR of RMASH 2-1-$1_{1.5b}$ with settling error of the low reference voltages, ±0.45V. With 14-bit DR, the low reference voltages for second and third stages can tolerate the settling error of 0.5%, which greatly reduces the power and accuracy of their reference buffers.

3.1.4 Scaling of Loopfilter Coefficients

In general, the leakage quantization noise is the major concern on the design of a cascaded ΣΔ modulator. The leakage quantization noise is mainly caused by the finite OTA gain and capacitor mismatch of the first-stage integrators. In the RMASH 2-1-$1_{1.5b}$, the capacitor mismatch is especially critical because the SNR improvement mainly relies on the in-band zeros induced by the first-stage resonator. Therefore, we have to select coefficients of the

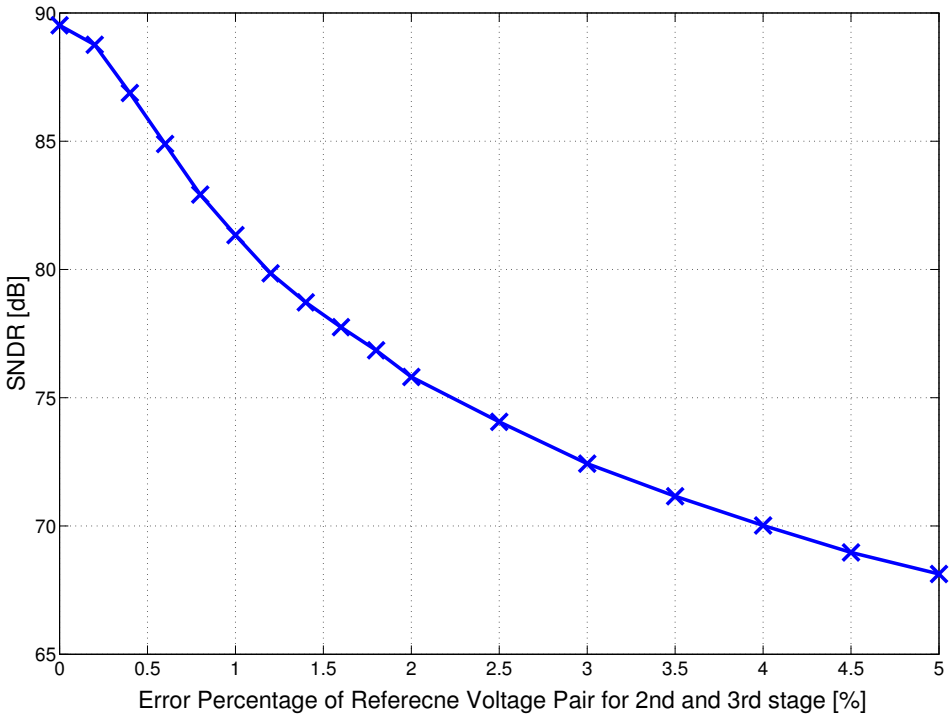

Figure 3.11: The simulated peak SNDR of RMASH 2-1-$1_{1.5b}$ with settling error of the low reference voltages, ±0.45V.

Table 3.1: Coefficients of RMASH 2-1-$1_{1.5b}$ for OSR=16

Coefficients	Values	Coefficients	Values
g1	0.5	b1	0.25
g2	0.25	a1	2
g3	2	a2	4
g4	2	d2	2

loop filter in the first stage carefully to achieve the desired SNR. Figure 3.12 shows a circuit implementation of the first integrator where the $g_1 = C_{S1}/C_{I1}$ and $b_1 = C_{FB}/C_{S1}$. Given the notch and sampling frequencies of 2.25MHz and 70.4MHz, the resonator loop gain r, based on Equation (3.7), approximates to 0.04. In order to simplify the design of the digital cancellation filters H_1(z) and H_2(z), we scaled the value of r to be the power of 2 (say 0.03125), which shifts the notch frequency to 2MHz. This arrangement only degrades the theoretical SNR by 1.5dB. In general, the g_1 and g_2 should be as large as possible to keep the thermal noise low, and thus b_1 has to be relatively small for the given r. Consequently, the difference between C_{S1} and C_{FB} may become large and cause a large ratio mismatch [18]. For instance, if g_1=1, g_2=0.5, and C_{S1}=1.5 pF, b_1 and C_{FB} will be 0.0625 and 93.75fF, respectively. The value of C_{S1} is way larger than that of C_{FB}. To reduce the mismatch

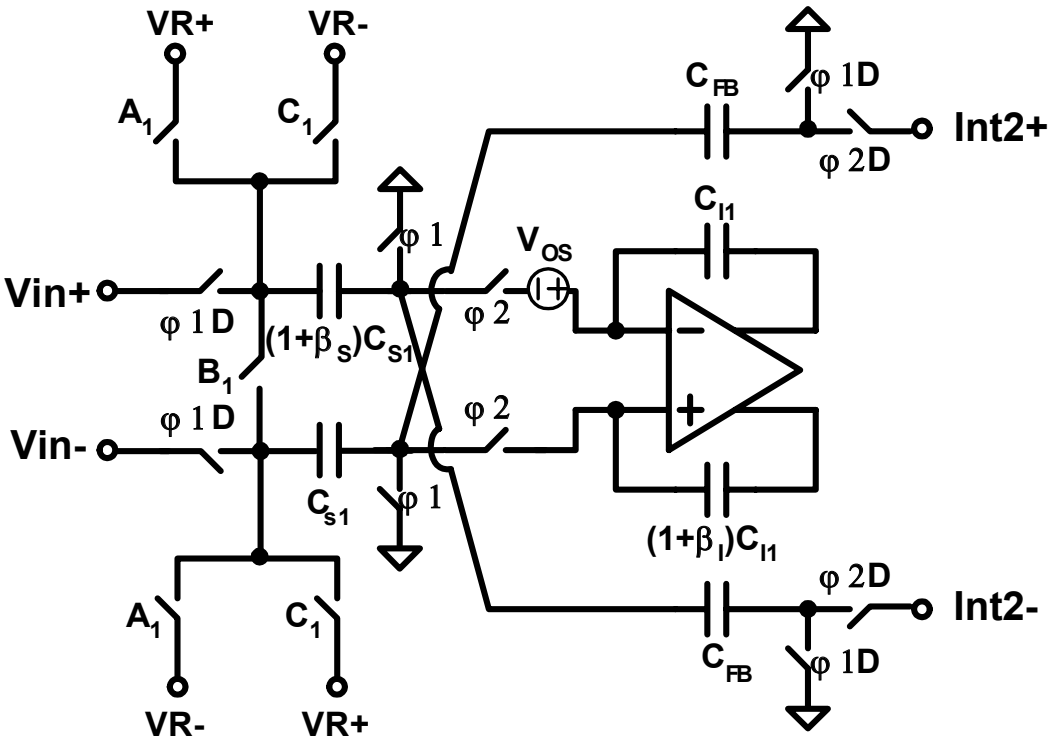

Figure 3.12: The circuit implementation of the first integrator in the first stage of RMASH 2-1-$1_{1.5b}$.

of C_{S1} and C_{FB}, we scaled the g_1 and g_2 down to 0.5 and 0.25 respectively. In this case, the $b1$ and C_{FB} become 0.25 and 375 fF, respectively, and the mismatch can be reduced. Table 3.1 shows the coefficient sets of the RMASH 2-1-$1_{1.5b}$ we used in this work, and the proposed RMASH 2-1-$1_{1.5b}$ can achieve a peak SNDR of 92 dB and a dynamic range of 95 dB, respectively.

3.1.5 Design of Decimation Filter

Since the digital output of the ΣΔ modulator is an over-sampled, noise-shaped signal, the complete ADC chip requires a digital decimation filter to perform down-sampling and out-band noise filtering. In this work, we designed a three-stage decimation filter to meet the linearity requirement of ADSL2+. The design of the decimation filter determines the filter types and coefficients by considering the finite word-length effect and the SNDR requirement, which results in a three-stage digital filter. Figure 3.13 shows the block diagram of the three-stage decimation filter. The first-stage is a fifth-order Cascaded Integrator-Comb (CIC) filter with the down-sampling ratio of 4 and its transfer function is shown as follow:

$$\mathrm{CIC(z)} = \left(\frac{z^{-1}}{1-z^{-1}}\right)^5 z^{-4}\left(1-z^{-4}\right)^5 \tag{3.13}$$

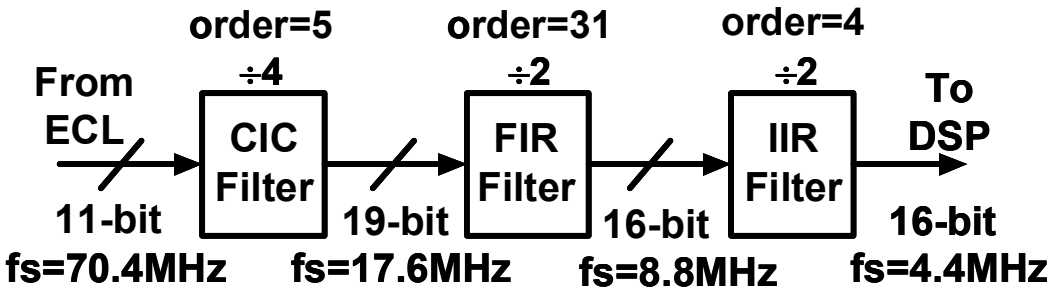

Figure 3.13: The block diagram of the three-stage decimation filter.

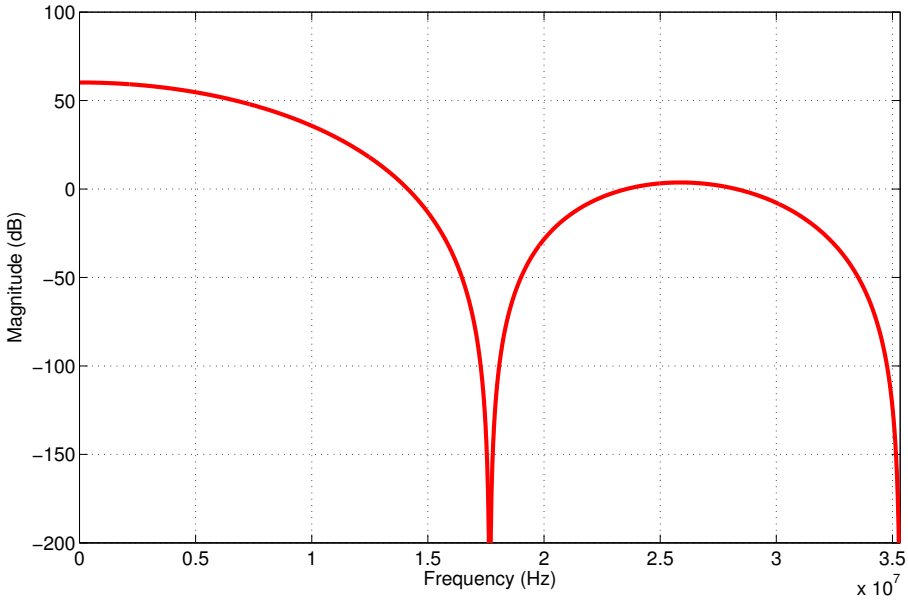

Figure 3.14: The frequency response of the five-order CIC filter.

Figure 3.14 illustrates the frequency response and circuit implementation of CIC filter. Following the CIC filter, the second stage is a 31-tap finite impulse response (FIR) filter with the down-sampling ratio of 2. Figure 3.15 shows its frequency response with finite word-length effect. Finally, the third stage is an infinite impulse response (IIR) filter with the down-sampling ratio of 2. The IIR filter is synthesized by the fourth-order Chebyshev Type II topology. The frequency response of the IIR filter is shown in Figure 3.16.

3.2 Circuit Specifications

In the case of a high-resolution, high-speed ΣΔ modulator, circuit nonidealities can significantly influence the performance. Since ΣΔ modulator is a over-sampled and close loop system, transistor-level simulations such as HSPICE are time-consuming. Therefore

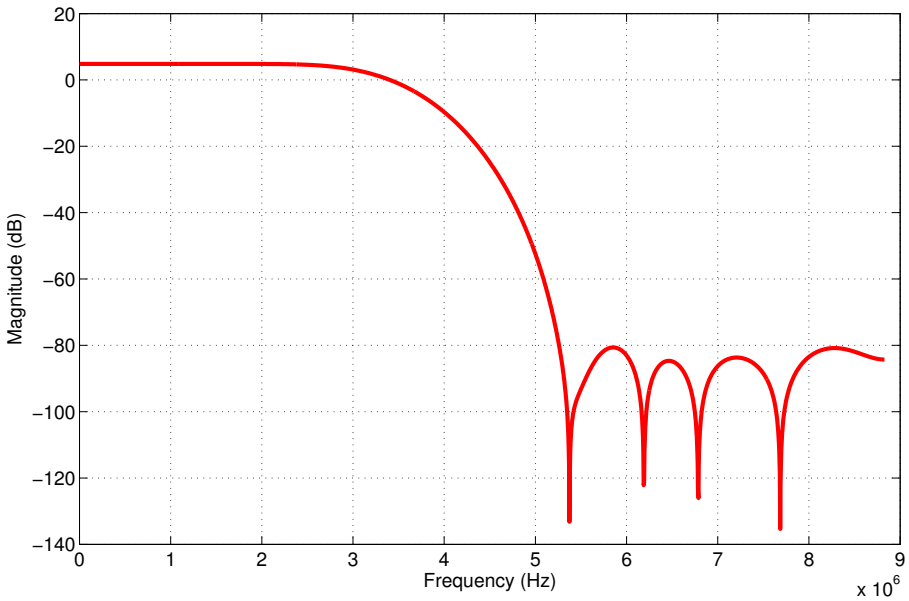

Figure 3.15: The frequency response of the 31-tap FIR filter.

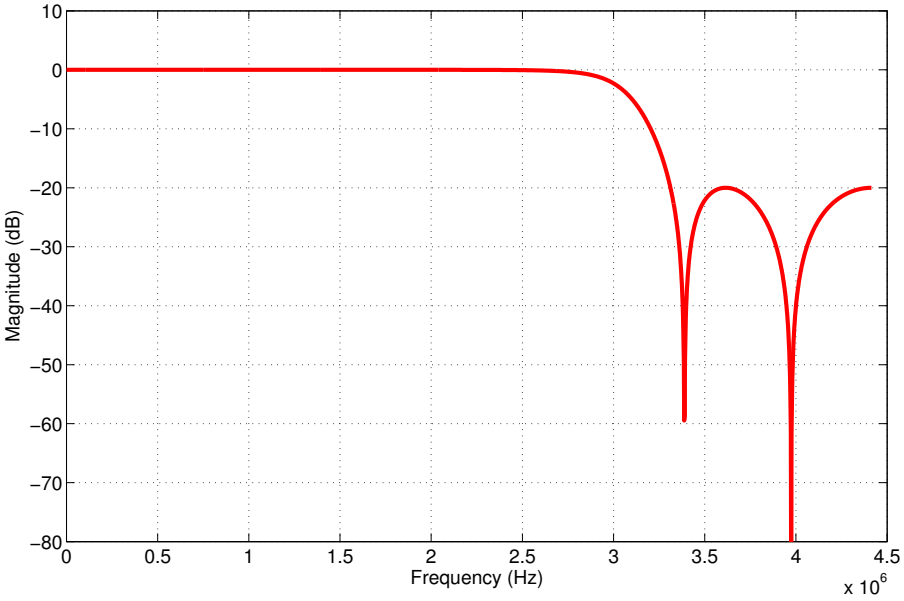

Figure 3.16: The frequency response of the fourth-order IIR filter.

the system-level behavioral simulation is necessary in order to efficiently evaluate the performance of the modulator with circuit nonidealities. Most importantly, it can avoid the over-design of the circuit implementation and can optimize the trade-off between performance and power dissipation, which achieves a low-power and cost-effective circuit design. Papers [43] addressed the effects and impacts of the circuit nonidealities on the $\Sigma\Delta$ modulator and presented several sets of Matlab and Simulink models, which allow one to perform exhaustive behavioral simulations of any $\Sigma\Delta$ modulator taking into account most of the nonidealities, such as sampling jitter, KT/C noise and operational amplifier parameters (noise, finite gain, finite bandwidth, slew-rate, settling time and saturation voltages).

3.2.1 Switch Thermal Noise

Among the noise sources present in an SC circuit, the most important are the thermal noise contributed by the input switches. Thermal noise has a white spectrum and is power can be considered as an equivalent resistor with resistance aliased into a band from 0 to $f_s/2$ [44].

$$R_{eq} = \frac{1}{f_s C} \tag{3.14}$$

The total noise power models the resistor as having a noise source in serious with a power source equal to the Johnson noise $4kTR_{eq}f$ and can be approximately evaluated as:

$$P_T = 4kTR_{eq}\frac{f_s}{2} = \frac{2kT}{C} \tag{3.15}$$

where k is Boltzmann's constant and T is the absolute temperature.

For a switching scheme of dual-reference voltages as shown in Figure 3.12, the thermal noise power is reduced by 3dB and the feedback factor is increased by a factor of two. To consider this fully differential SC integrator used in our design, the thermal noise is given by

$$P_{thn} = \frac{4kT}{C_{S1} \cdot OSR} \tag{3.16}$$

By assuming that other noise sources in the first integrator can be negligible, the DR due to the thermal noise can be expressed as

$$DR_{thn} = 10 \cdot \log\left(\frac{V_R^2}{2} \cdot \frac{C_{S1} \cdot OSR}{4kT}\right) \tag{3.17}$$

To achieve at least 14 bit of resolution and to leave the 3dB margin for the noise contributed by other nonidealities a $DR > 90$dB is determined. Since the modulator is stable for input signals with swing up approximately 0.7 times of the DAC reference voltage, here chosen to be $V_R = 0.7(V_{R+} - V_{R-}) = 1.26V$. Thus, by substituting DR=90dB in Equation (4.17) and by solving for C_{S1}, one can find that $C_{S1} \approx 1.5$pF.

3.2.2 Integrator Nonidealities

In switched-capacitor (SC) cascaded modulators, the capacitor mismatch and finite OTA gain are two main static nonidealities. These nonidealities is particularly important in cascaded $\Sigma\Delta$ modulator since they can lead to imperfect cancellation of the first- and second-stage quantization noises at modulator output and thus degrade the performance.

For a non-inverting SC as shown in Figure 3.12 its transfer function of the can be expressed as [29]

$$H_{\text{int}}(z) = \frac{C_{S1}}{C_{I1}} \times \frac{\gamma_2 z^{-1}}{1 - \frac{\gamma_2}{\gamma_1} z^{-1}} \tag{3.18}$$

where γ_1 and γ_2 are the closed-loop static errors, andβ_1 and β_2 are the feedback factor during the sampling and integration phase, respectively. They are expressed as follows:

$$\gamma_1 = \frac{\beta_1 A}{1 + \beta_1 A} \tag{3.19}$$

$$\gamma_2 = \frac{\beta_2 A}{1 + \beta_2 A} \tag{3.20}$$

$$\beta_1 = \frac{C_I}{C_P + C_I} \tag{3.21}$$

$$\beta_2 = \frac{C_I}{C_P + C_I + C_S} \tag{3.22}$$

where C_P is a parasitic capacitance at the input and A is the amplifier's open loop gain. By applying Equations.(3.19) (3.22) for the behavioral simulation, Figure 3.17 shows that increasing the finite OTA gain above 70 dB will not significantly improve the performance. So, in our work, we set the finite OTA gain to 70 dB. Given 70-dB OTA gain and 0.5% capacitor mismatch, Figure 3.18 illustrates that the RMASH 2-1-$1_{1.5b}$ can achieve a peak SNR of 86 dB.

Furthermore another nonideality that introduces gain and pole errors in the transfer

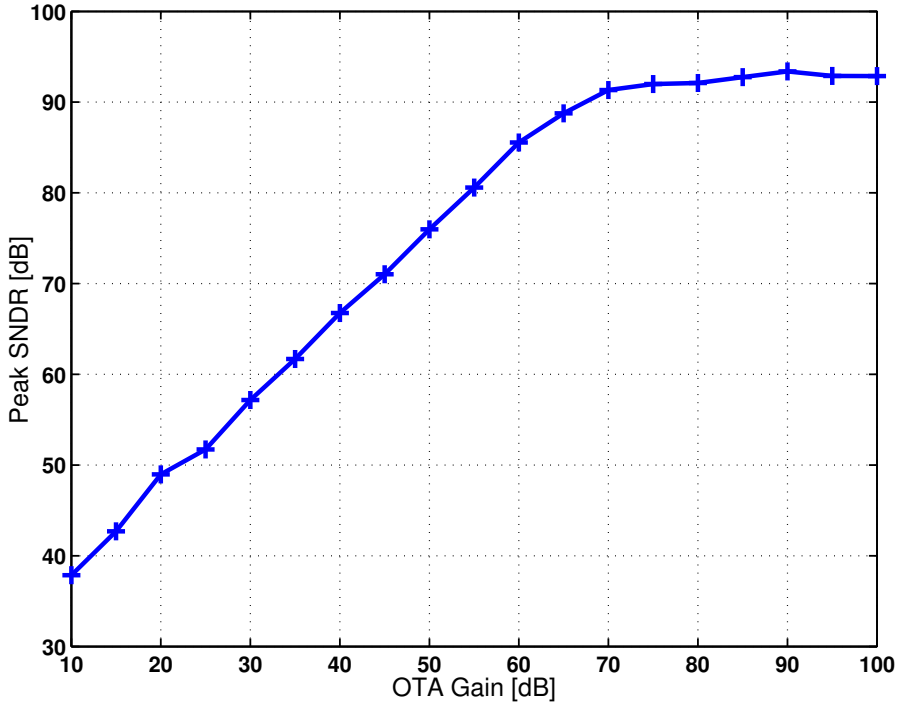

Figure 3.17: Plots of simulated SNDR versus OTA dc gain. (OSR=16)

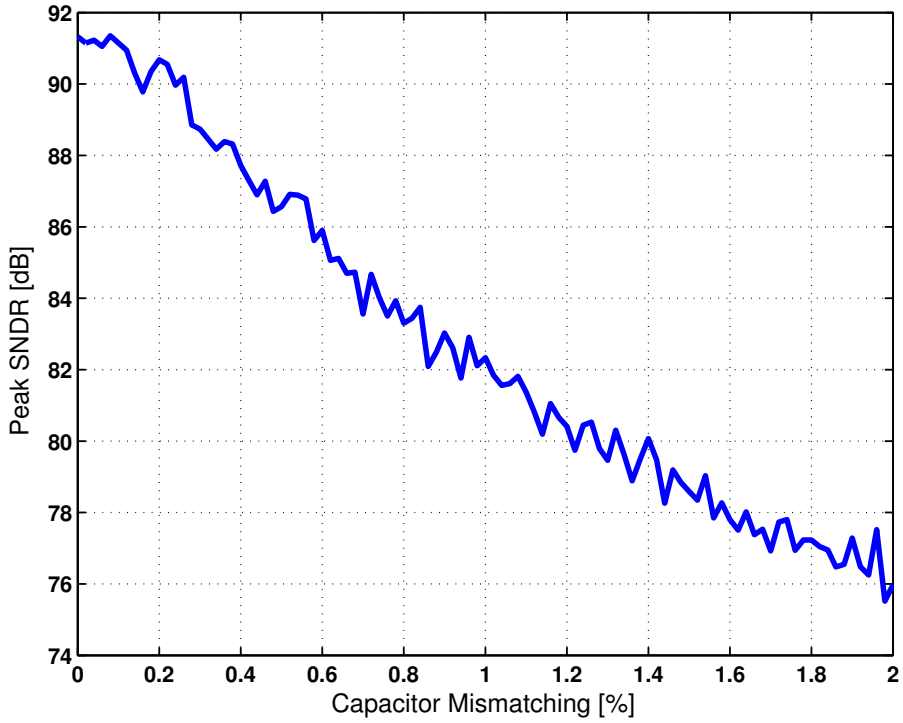

Figure 3.18: Plots of simulated SNDR versus 70-dB OTA dc gain and 0.5% capacitor mismatch. (OSR=16)

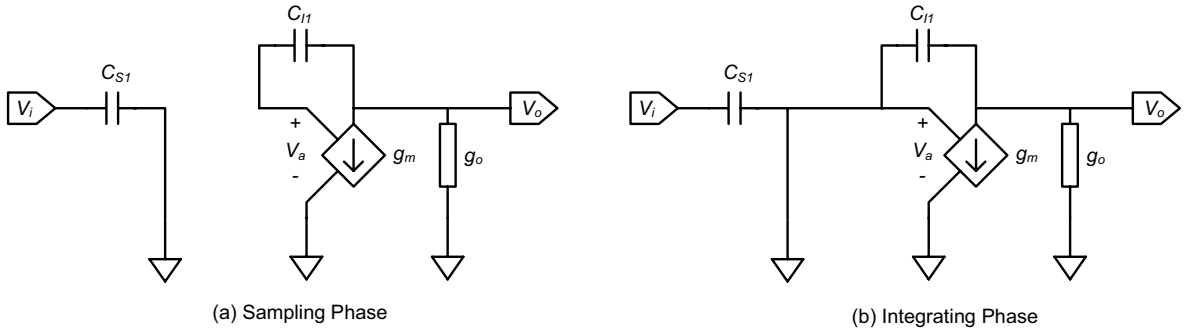

Figure 3.19: OTA-based SC integrator.

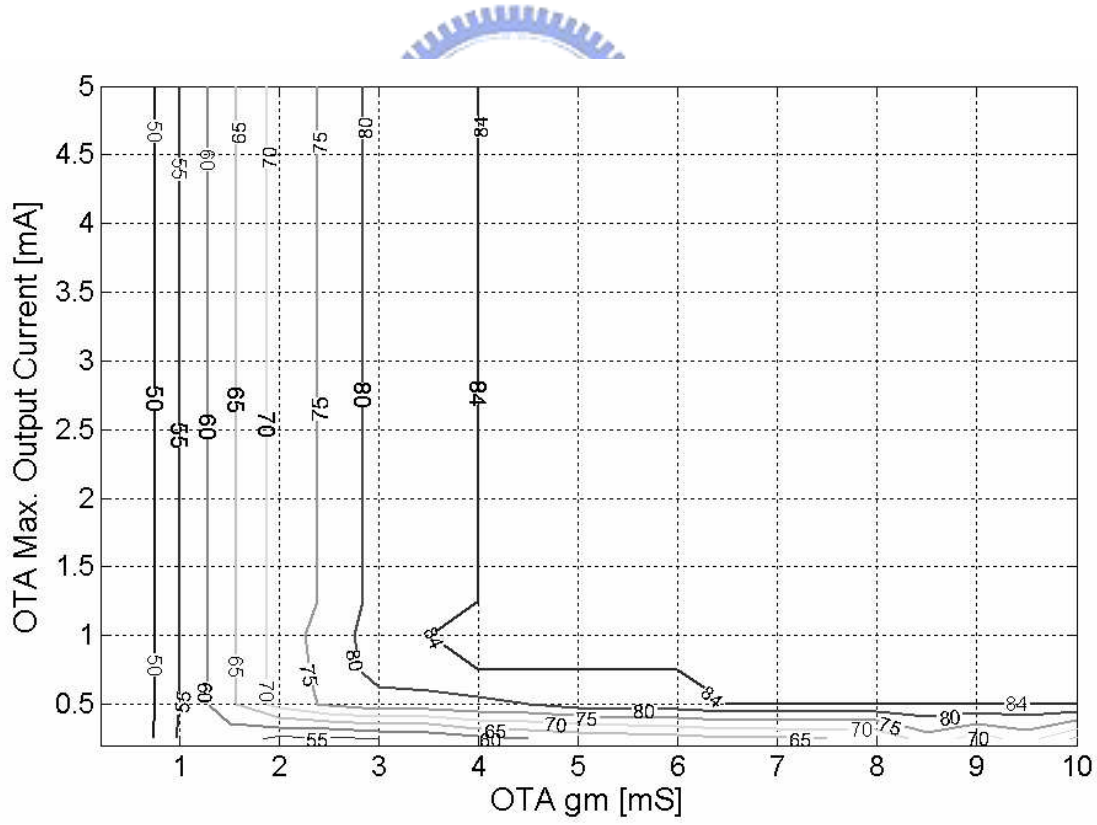

Figure 3.20: Plots of simulated SNDR versus OTA transconductance and output current for RMASH 2-1-$1_{1.5b}$

function is the finite closed-loop pole of the OTA. The OTA is modeled with a finite output conductance g_o and an input transconductance g_m, as shown in Figure 3.19. Based on the analysis similar to [29], the transfer function of the integrator can be calculated and given by

$$H_{\text{int}}(z) = \frac{C_{S1}}{C_{I1}} \cdot \frac{\gamma_2(1-k)z^{-1}}{1-\frac{\gamma_2}{\gamma_1}\left(1-k\left(1-\frac{\gamma_1}{\gamma_2}\right)\right)z^{-1}} \tag{3.23}$$

where the parameter k represents the settling error in the integration phase, which is expressed by

$$k = \exp\left(-\frac{g_m}{C_S + C_P + \frac{(C_S+C_P+C_I)C_L}{C_I}} \cdot \frac{\tau}{\gamma_2}\right) \tag{3.24}$$

where τ represents the available time for settling during the integration phase. It is usually half of the clock pried T_s. Assuming an OTA gain of 70 dB, behavioral simulations show that the minimum g_m and slew current for 14-bit RMASH 2-1-$1_{1.5b}$ must be larger than 8mS and 0.8mA respectively as shown in Figure 3.20.

3.2.3 Tri-Level DAC Nonidealities

In the RMASH 2-1-$1_{1.5b}$, the nonlinearity of tri-level DACs can also introduce distortion to the modulator output, especially for the first-stage DAC. To consider the nonidealities of tri-level DACs, [41] has provided a good study and insight for the issue. The first integrator involved with the tri-level DAC has been shown in Figure 3.12. Three major sources of nonidealities contributed to the tri-level DAC are the mismatch of sampling capacitor β_S, the mismatch of integrating capacitor β_I, and the input-referred OTA offset V_{OS}. Of course, other sources, such as charge injection and parasitic capacitors...etc. also contribute the distortion. However, these effects are hard to quantify and actually can be negligible with careful design and layout schemes. To analyze the distortion of the tri-level DAC, we first calculate the output voltages for three feedback signals, A1=1, B1=1, and C1=1.

$$\begin{aligned} V_O^{A1} \cong \quad & V_{R+} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)C_S+(1+\beta_{SI})C_I}{(1+\beta_{SI})C_S+(1+\beta_I)C_I}\right] \\ & +V_{OS} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)(C_S+C_I)}{(1+\beta_{SI})C_S+(1+\beta_I)C_I}\right] \end{aligned} \tag{3.25}$$

$$V_O^{B1} = 0 \tag{3.26}$$

$$V_O^{C1} \cong V_{R-} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)C_S+(1+\beta'_{SI})C_I}{(1+\beta_{SI})C_S+(1+\beta_I)C_I}\right] + V_{OS} \cdot \left[\frac{C_S}{C_I}\frac{(1+\beta_S)(C_S+C_I)}{(1+\beta'_{SI})C_S+(1+\beta_I)C_I}\right] \tag{3.27}$$

where $\beta_{SI} = (\beta_S + \beta_I)/2$ and $\beta'_{SI} = (\beta_S + \beta_I + \beta_S\beta_I)/2$. Accordingly, the nonlinearity factor defined in Equation (3.5) can be calculated

$$\varepsilon = \frac{V_O^{A1} + V_O^{C1} - 2V_O^{B1}}{2V_O^{A1}} \tag{3.28}$$

By assuming $\beta_S, \beta_I \ll 1$ and $V_{OS} \ll V_{R+}$ and by substituting Equation (3.25), Equation (3.26), and Equation (3.27) in Equation (3.28), we can find that

$$\varepsilon = \frac{\beta_S\beta_I}{4}\frac{(1+\beta_I)C_I^2 - (1+\beta_S)C_S^2}{(C_S+C_I)^2} - \frac{V_{OS}}{2V_{R+}} \tag{3.29}$$

Since the β_S and β_I are small, the $\beta_S\beta_I/2$, first term of Equation (3.29), can be considered negligible. By substituting Equation (3.29) in Equation (3.5), the discrete-time error function of tri-level DAC approximates

$$e_{DAC}[k] \approx \frac{V_{OS}}{2V_{R+}}(1 + y_1[k]^2) \tag{3.30}$$

where V_{OS}, V_{R+}, and y_1[k] denote the offset voltage of OTA, reference voltage and output of tri-level quantizer, respectively. As shown in Equation (3.30), the nonideality of tri-level DAC mainly depends on the offset voltage of OTA for a given reference voltage. Figure 3.21 shows the simulated dynamic range of RMASH 2-1-$1_{1.5b}$ as a function of offset voltage of OTA. To target the peak SNDR of 84dB, the offset voltage of 0.2 mV is required. The offset voltage of 0.2 mV is achievable with carefully sizing and paying attention to layout of the input differential pairs of OTA.

3.2.4 Clock Jitter

Since the operation of a SC circuit depends on complete charge transfers during each of the clock phases, the effect of clock jitter on a SC ΣΔ modulator can be calculated in a fairly simple manner. In fact, once the analog signal has been sampled the SC circuit is a sampled-data system where variations of the clock period have no direct effect on the circuit performance. Therefore, the effect of clock jitter on the SC circuit is completely described by computing its effect on the sampling of the input signal. This means that the

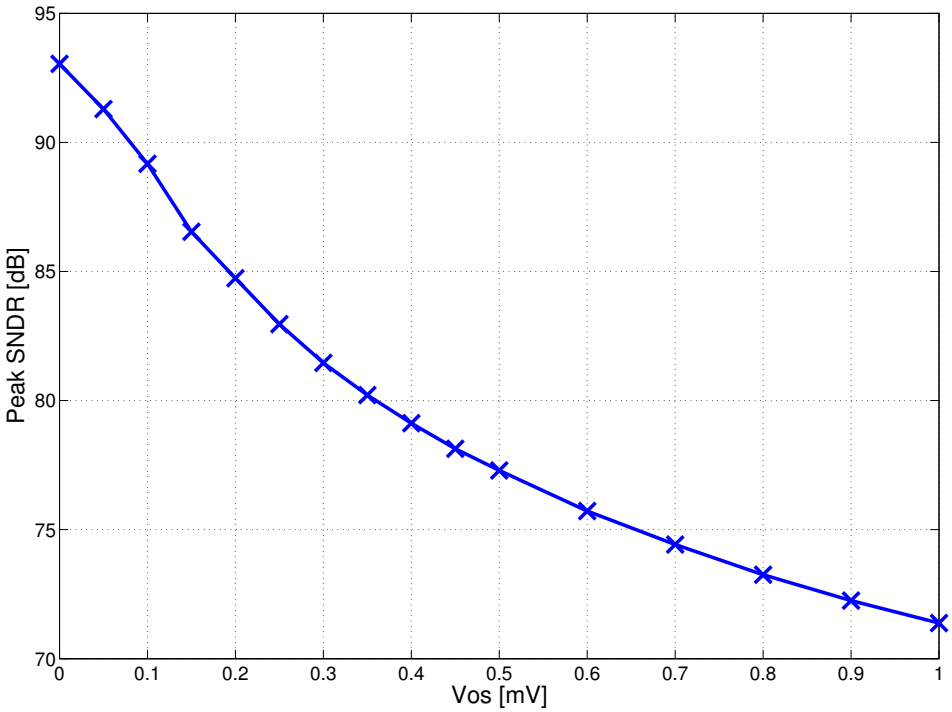

Figure 3.21: Plots of simulated dynamic range versus OTA offset voltage. (OSR=16)

effect of clock jitter on a $\Sigma\Delta$ modulator is independent of the architecture or order of the modulator. Sampling clock jitter results in non-uniform sampling and the total noise power is thus increased in the modulator output. The magnitude of this noise increase is a function of both the statistical properties of the sampling jitter and input to the ADC. The error resulting from sampling a sinusoidal signal with amplitude A and frequency f_{in} at an instant that is shifted in time by an amount of is given by [45],

$$x(t+\delta) - x(t) \approx 2\pi f_{in}\delta A\cos(2\pi f_X t) = \delta\frac{d}{dt}x(t) \tag{3.31}$$

By applying this equation for behavioral simulation, the plot of the SNDR versus clock jitter for three different structures of the modulator is shown in Figure 3.22. A sinusoidal signal with maximum amplitude of 2Vpp and frequency of 2.14MHz is used to perform worst-case simulations. Expectably, the jitter noise only depends on OSR not structure of modulator. The plot of the SNDR versus input sinusoidal frequency for the proposed RMASH 2-1-$1_{1.5b}$ with OSR of 16 is shown in Figure 3.23. According to this figure, the minimum root mean square jitter for the RMASH 2-1-$1_{1.5b}$ ADC with 14-bit resolution and 2.2MHz signal bandwidth must less 20ps.

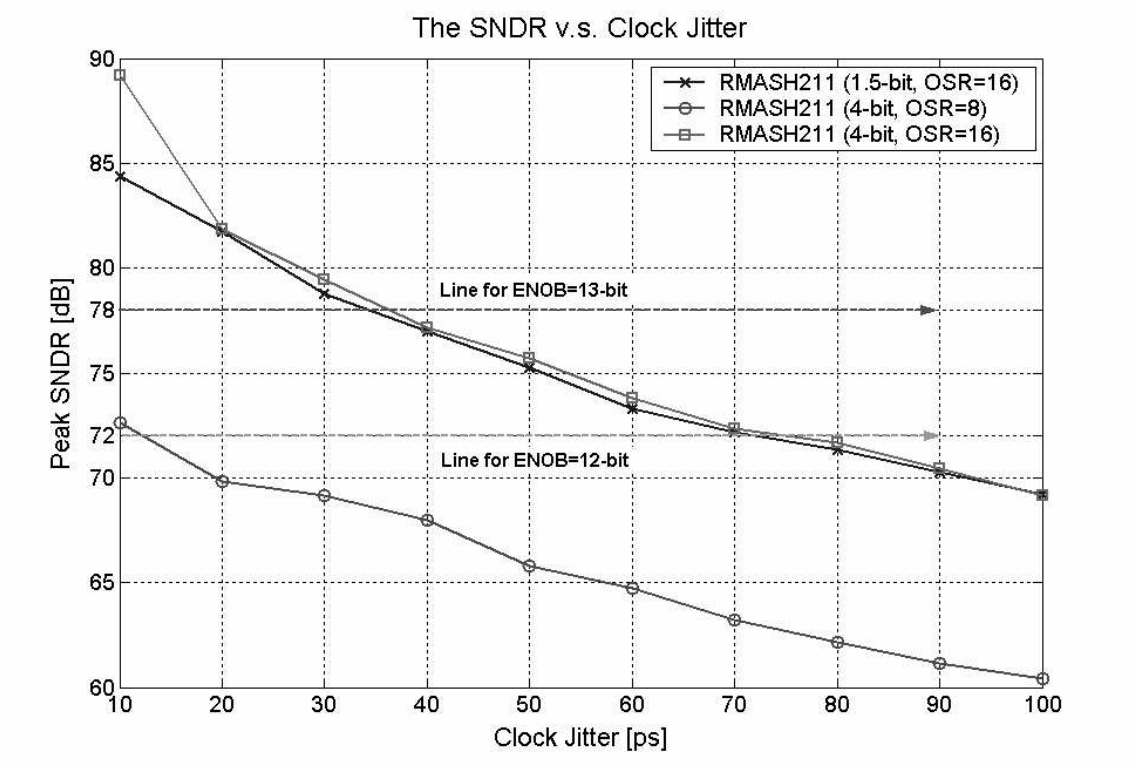

Figure 3.22: The plot of the SNDR versus clock jitter for three different structures of the modulator

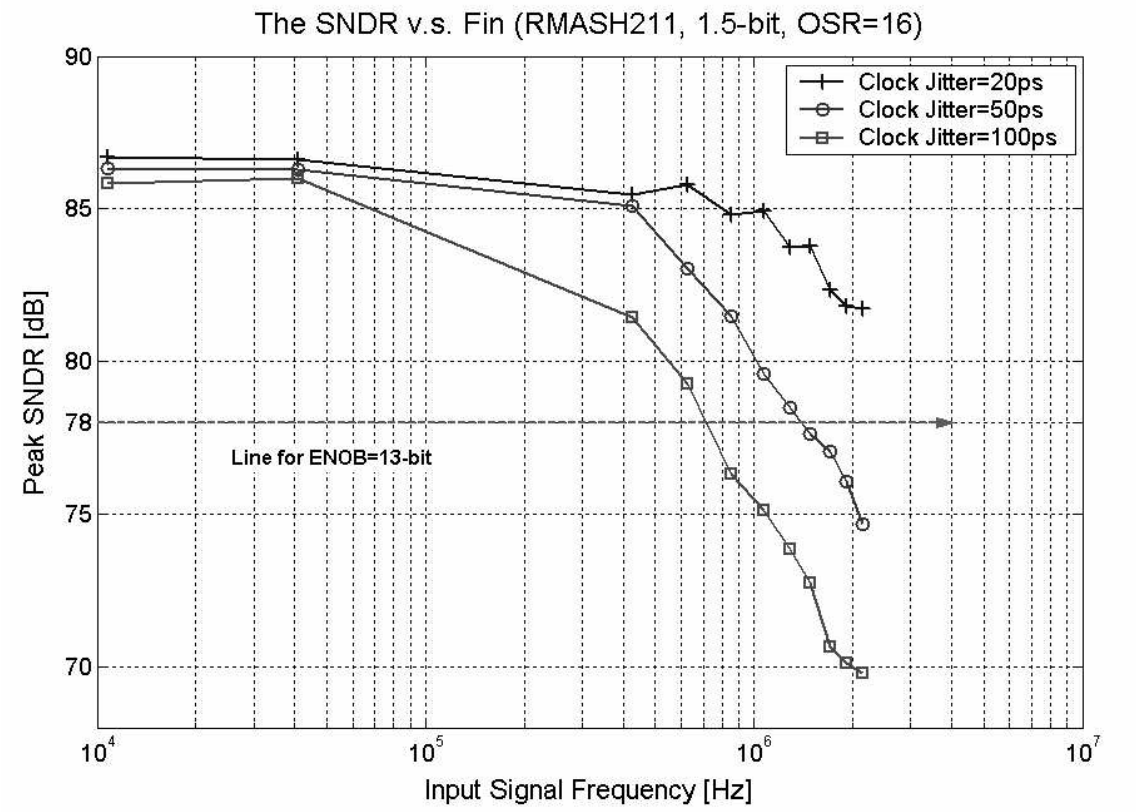

Figure 3.23: The plot of the SNDR versus input sinusoidal frequency for the proposed RMASH 2-1-$1_{1.5b}$ (OSR=16)

Table 3.2: Circuit specifications for 14-bit 4.4Ms/s RMASH 2-1-$1_{1.5b}$.

Optimized Spec. For	14-bit@4.4MS/s	
Modulator	Topology	RMASH 2-1-$1_{1.5b}$
	Oversampling ratio	16
	Sampling frequency	70.4MHz
	Clock jitter	15ps
	Reference voltages	±0.9V for 1st stage
		±0.45V for other stages
OTAs	Gm	10mS for 1st stage
		5mS for other stages
	DC-gain	75 dB for 1st stage
		60 dB for other stages
	Output swing range	1.2V
	Max. output current	1mA for 1st stage
		0.5mA for other stages
	Unity gain bandwidth	300MHz for 1st stage
		200 MHz for other stages
	Input noise	$8nV/\sqrt{Hz}$
	Input offset	0.25mV
Integrators	Input sampling capacitor	2pF
	Unit capacitor	0.5pF
	Capacitor deviation	0.5%
	Switch on-resistance	150Ω
Comparators	Offset	±15mV

3.2.5 Summary

Upon simulating the behavior of the proposed RMASH 2-1-$1_{1.5b}$ with MATLAB, we determined the specifications of analog building blocks with consideration of power-performance trade-offs. Table 3.2 summarizes the circuit specifications for the 14-bit 4.4MS/s RMASH 2-1-$1_{1.5b}$. To evaluate the robustness, we modeled the critical circuit parameters as Gaussian distribution with the standard deviation of 20% and executed the Monte Carlo analysis by using MATLAB. The critical parameters are dc gain, transconductance, unity-gain bandwidth (GBW), output current, and input offset of OTAs, on-resistance of switches, and clock jitter. In addition, the standard deviations of integrator and feedforward gains are 0.5% and 2%, respectively. As shown in Figure 3.24, the mean, minimum, and standard deviation of peak SNDR are 84.6dB, 81.5dB, and 0.72%, respectively.

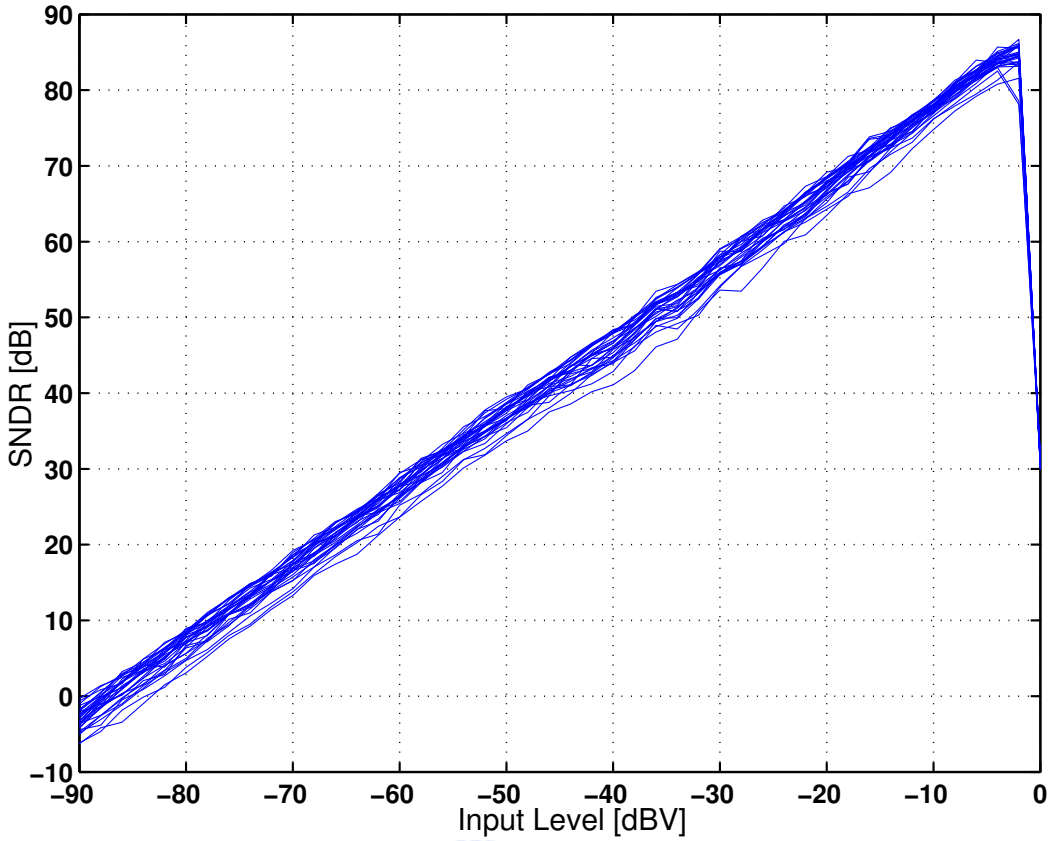

Figure 3.24: Plots of simulated SNDR versus input level with 30 Monte Carlo analysis runs.

3.3 Circuit Implementation

This section describes the transistor-level design of the critical building blocks for the proposed RMASH 2-1-$1_{1.5b}$ ADC. The ADC was implemented in TSMC 2.5V, 0.25-μm, 1P5M, CMOS technology with metal-insulator-metal (MIM) capacitors.

3.3.1 SC Circuit Design

The SC diagram of the implemented circuit is shown in Figure 3.25. The fully differential SC technique is preferred because of increased signal DR, higher immunity to clock and charge feed-through, and better rejection to the common-mode noise. The non-inverting integrators are operated with two non-overlapping clock phases: in the phase φ_1 the sampling capacitors C_{Si} are charged, while in the phase φ_2 this charge is transferred to the integrating capacitor C_{Fi}. The coefficients are realized as the capacitor ratios based on charge conservation [29]. To reduce the effect of the signal-dependent charge injection, the delayed clock phases φ_{1D} and φ_{2D} have been used [29]. Figure 3.26 shows the on-chip clock generator with two non-overlapping phases. The feedback loop is used to ensure the non-overlapping

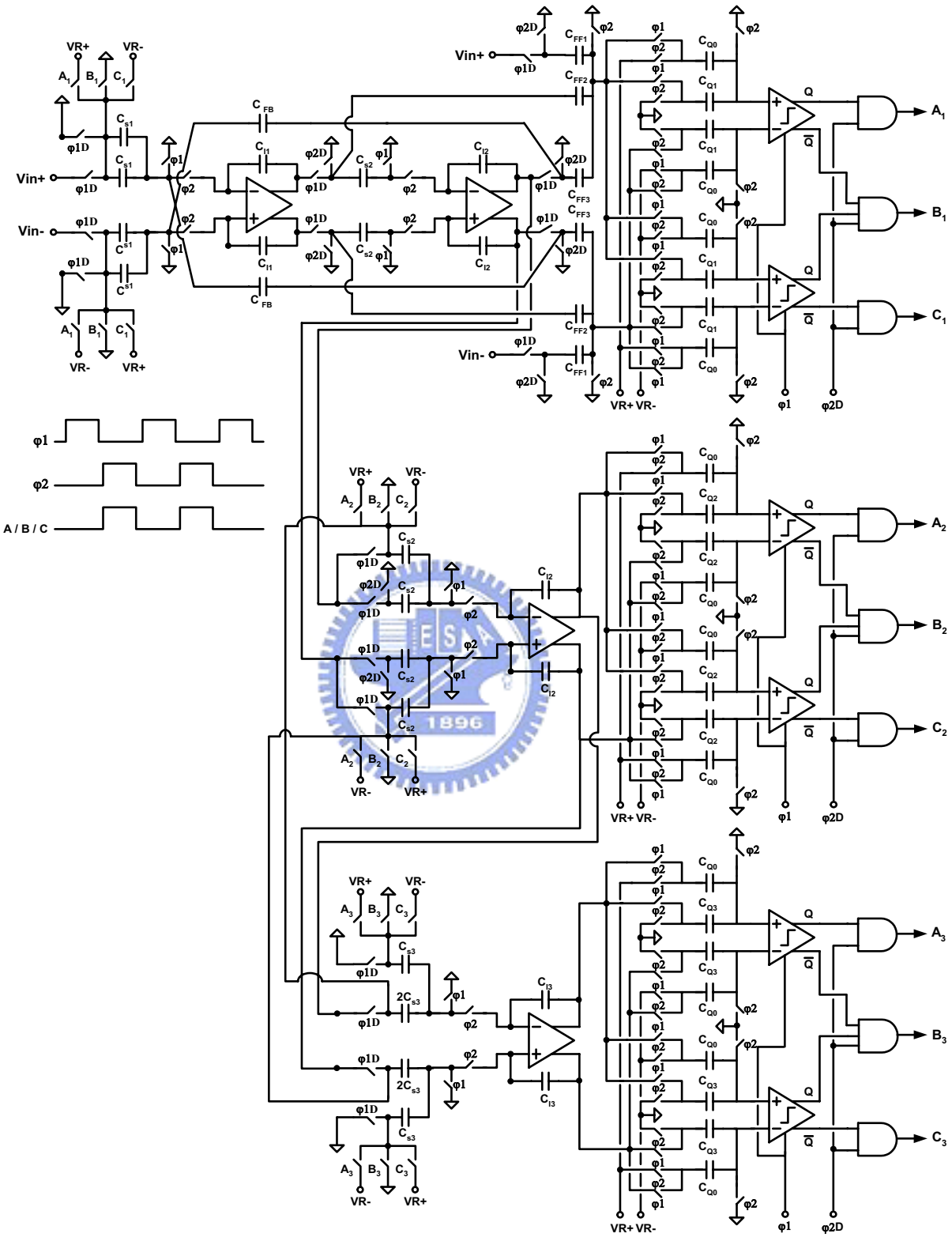

Figure 3.25: The SC diagram of RMASH 2-1-1$_{1.5b}$.

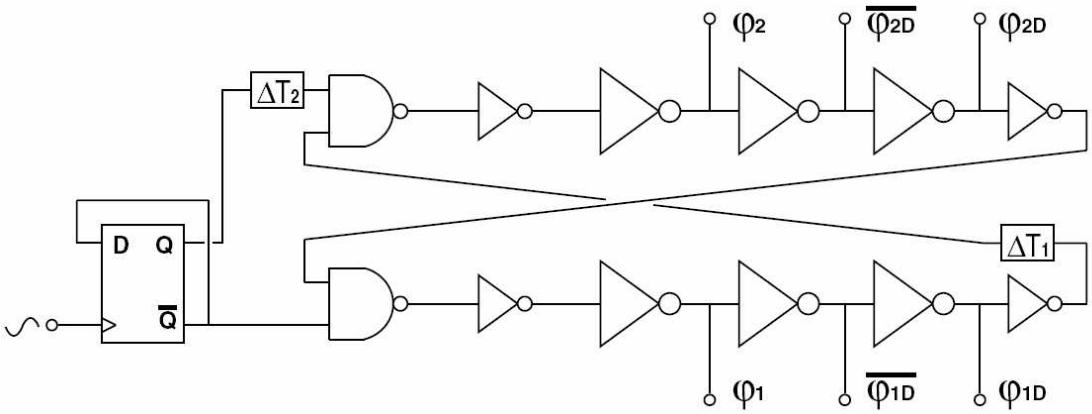

Figure 3.26: Non overlapping two-phase clock generator.

function between φ_1 and φ_2. All of the circuits are operated from a 2.5V supply voltage. The values of first-stage reference voltages used in the 1.5-bit quantizer and DAC are 2.15V and 0.35V while the values of second- and third-stage reference voltages are 1.7V and 0.8V. All the reference voltages are driven by on-chip reference buffers and are decoupled by off-chip capacitors.

3.3.2 OTA Circuit

According to Table 3.2, the proposed modulator requires the dc gain of 75-dB and the GBW of 300 MHz for the OTA with a supply voltage of 2.5 V. To meet the requirements, we chose a folded-cascode OTA with additional gain-boosting amplifier. By carefully design and sizing of the gain-boosting amplifiers, the induced nondominant pole can be located at 1GHz. As mentioned in Section II, the output swing of the first-stage integrators can be reduced by using the tri-level quantizer and the input feedforward path. Hence, for a supply voltage of 2.5 V, the required single-ended output swing of OTA is approximately 1 V.

Figure 3.27 shows the schematic of the folded-cascode OTA being used for the first-stage integrators. The single-ended output swing of OTA is 1.4 V, which can sufficiently accommodate the required output swing at the integrator outputs, and a dc gain of 75 dB is accomplished over the entire output range. The OTA, including gain-boosting and biasing circuits, dissipates 15 mW from a 2.5-V supply and achieves a GBW of 300MHz with a capacitive loading of 5 pF, while the phase margin is 75 degree. The total thermal noise contribution over 2.5-MHz signal bandwidth is about 12.6 μV. The SC common-mode feedback is used for designed OTA because it does not dissipate the static power. The capacitors used in the common mode feedback (CMFB) circuitry are properly chosen to

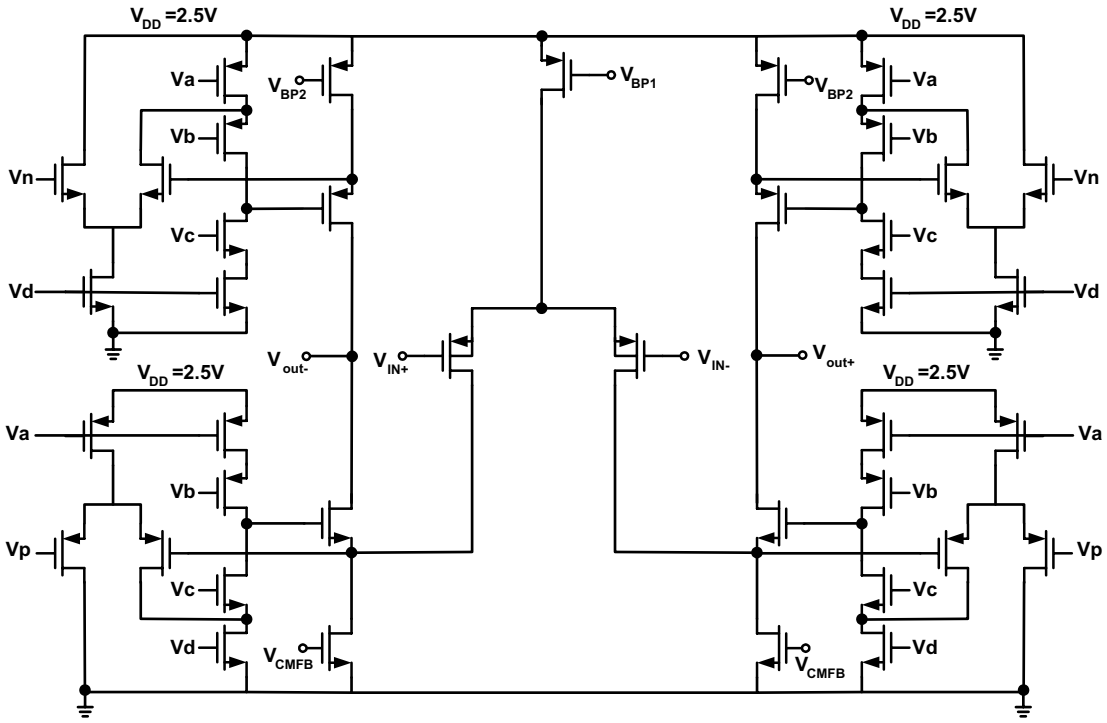

Figure 3.27: Circuit schematic of the OTA.

maximize the gain bandwidth, and thus avoid the settling error. We also used the similar OTA for other stages, and it dissipates 0.7 times of the power consumption the first-stage OTA consumes.

3.3.3 First Stage Design

As mentioned in Chapter 2, the noise and distortion performance of a cascaded $\Sigma\Delta$ modulator is determined primarily by the noise and distortion performance of first stage. The implementation of the first stage is therefore the most important task of the design. Figure 3.28 illustrates the SC circuit diagram of the first stage of the RMASH 2-1-$1_{1.5b}$. Since the dynamic range of the modulator is targeted at 90-dB at the sampling rate of 70.4MHz, the sampling capacitor is chosen to be 1.5 pF and, accordingly, the integrating and resonator feedback capacitors are 3 pF and 0.375 pF, respectively. The closed-loop bandwidth of front-end integrator is about 255MHz, which is larger than three times the sampling frequency. Because the feedback gain of the tri-level DAC is equal to one, we can use the share-capacitor switching technique to eliminate coefficient mismatch. The share-capacitor switching technique is to have the input sampling and feedback DAC share a common sampling capacitor C_{S1} [46]. However, the dependent load on the reference voltage may cause harmonic distortion. In our work, we used a dummy SC network to reduce the

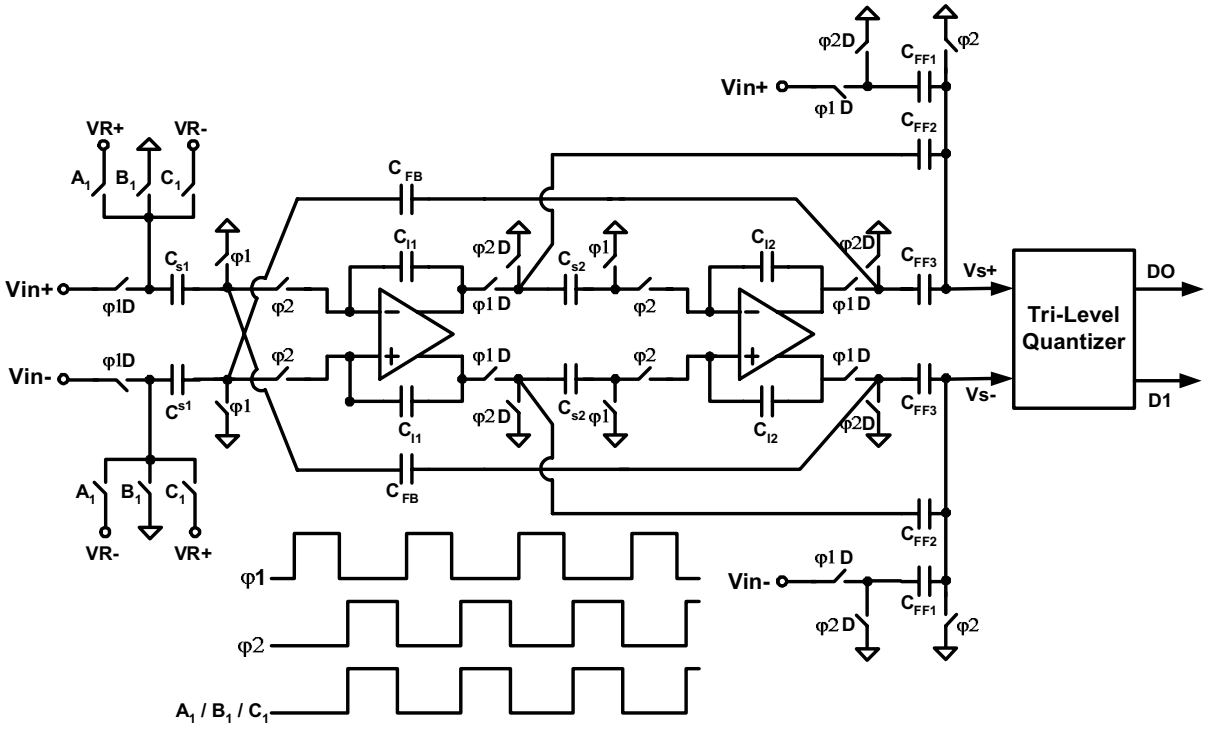

Figure 3.28: Circuit implementation of the first-stage modulator.

distortion [47]. The output two-bit code of tri-level quantizer is used to switch A_1, B_1, and C_1 at the integrating phase.

The summing circuit in front of the quantizer is implemented by using a passive SC network to avoid the use of additional OTA and save the power dissipation. The summed signal can be expressed as

$$V_S(z) = \frac{C_{FF1}V_{in}(z) + C_{FF2}Int1(z) + C_{FF3}Int2(z)}{C_{FF1} + C_{FF2} + C_{FF3}}, \tag{3.32}$$

where C_{FF1}, C_{FF2}, and C_{FF3} are the capacitors for feedforward gains. According to behavioral simulation, the feedforward gains are not critical and can tolerate the variation up to 2%. This allows the use of small capacitance to implement the feedforward gains. We set the values of C_{FF1}, C_{FF2}, and C_{FF3} to 0.125 pF, 0.25 pF, and 0.5 pF, respectively. Note that the summed signal is scaled down by 1/7 when comparing with the parameters of Table 3.1 and Figure 3.4. In order not to affect the desired performance of the modulator, the reference voltages of the quantizers must be scaled down by a factor of 1/7 from the nominal value. This also scales down the quantizer step size, and hence increases the requirement of the comparator resolution. In our case, the required step size of the tri-level quantizer is about 150 mV. This requirement is feasible because, in practice, the CMOS comparator with preamplifier can provide a resolution better than 50mV.

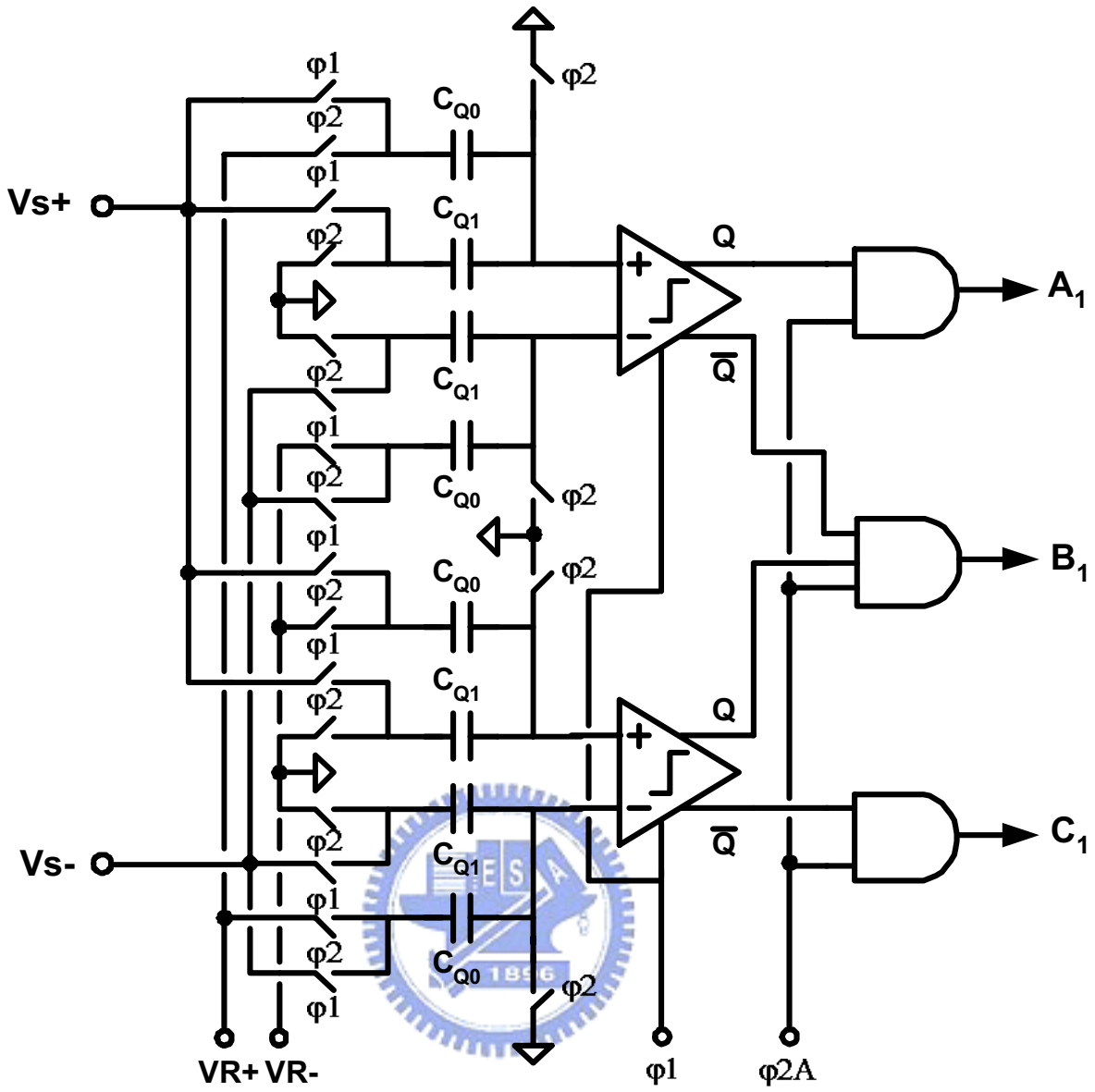

Figure 3.29: Circuit implementation of tri-level quantizer.

3.3.4 Tri-Level Quantizer Circuit

The circuit diagram of tri-level quantizer is shown in Figure 3.29. As mentioned above, the SC network must scale down the reference voltages, VR+ and VR-, by a factor of 1/7. So, we set the values of the capacitors C_{Q0} and C_{Q1} to 0.125 pF and 0.75 pF, respectively. In our design, we used a high-speed, high-accuracy CMOS comparator with preamplifier which is presented by [48]. The clock φ2A is used to control the generation of A_1, B_1, and C_1. Because of the time-delay of AND gates, the non-overlapping interval of φ2A is limited to 1$\sim$ 2ns when a sampling rate of 70.4 MHz.

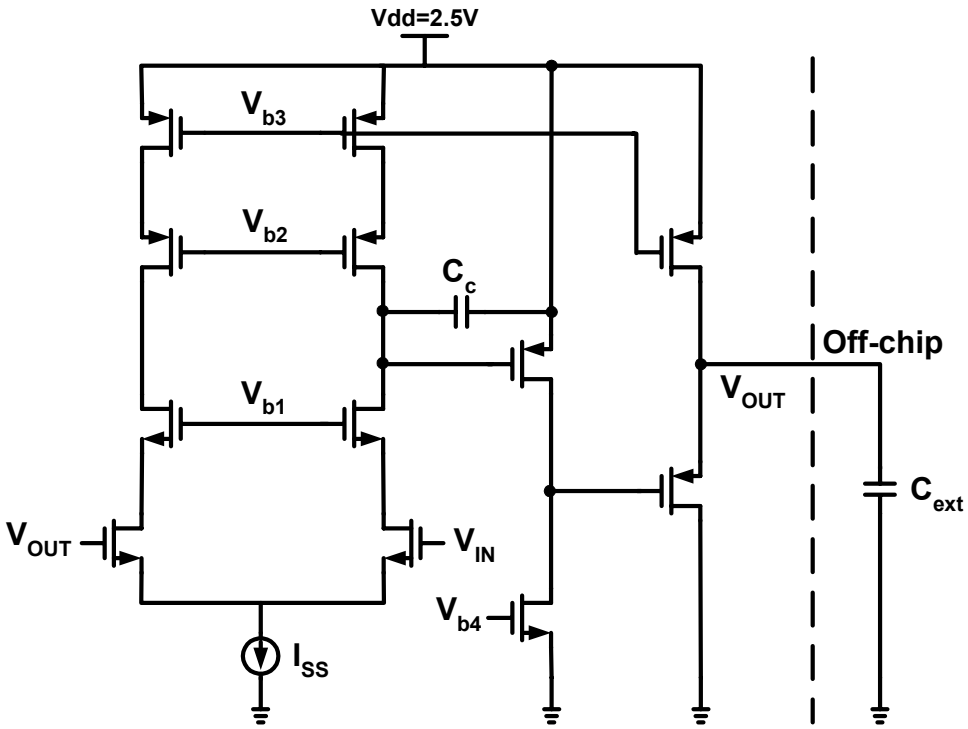

Figure 3.30: The schematic of reference voltage buffer amplifier.

3.3.5 Reference Buffer

Since the first integrator samples the input signal, it draws a signal-dependent current from the voltage reference and introduces harmonic distortion due to the finite output impedance of reference buffers. A high-bandwidth reference voltage buffer with fast settling behavior during the integrating phase $\varphi 2$ is required to deal with this problem. However, such kind of reference buffer is power-consuming especially for high signal-bandwidth design. In this work, we use a class-A amplifier with an external capacitor to make output impedance low enough to meet desired linearity requirement [49]. The schematic of the class-A amplifier is shown in Figure 3.30. The output impedance of this amplifier increases with frequency due to its finite gain-bandwidth product. Thank to the large external capacitor, the output impedance remains low at high frequencies. In other words, the transient charge is delivered from the external capacitor and the reference voltage is controlled by the class-A amplifier. By using this topology, the power consumption of reference buffers can be reduced at the cost of using large external decoupling capacitors. The buffers for the reference voltages of the second and third stages are similar to Figure 3.29, but dissipate approximately half of that of the first stage. This arrangement is practical because the settling errors of reference voltages in the second and third stages will be suppressed by the high-pass noise shaping of $H_1(z)$ and $H_2(z)$, respectively.

3.3.6 Cancellation Filter and Decimation Filter Circuit

The implementation of digital cancellation filter and decimation filter is based on the cell-based synthesis flow. According to the coefficients listed in Table 3.1, the transfer functions of the digital cancellation filters, H_1(z) and H_2(z), are show as follows:

$$H_1(z) = 1 - 2z^{-1} + 1.03125z^{-2}, \tag{3.33}$$

$$H_2(z) = 1 - 3z^{-1} + 3.03125z^{-2} - 1.03125z^{-3}. \tag{3.34}$$

Figure 3.31 illustrates the implementation structure of H_1(z) and H_2(z). By precision and error analysis, the output bit-width of digital cancellation filter is chosen to be eleven bits. The following equations are the transfer functions of CIC filter and 31-tap FIR respectively:

$$\begin{aligned} &\text{CIC(z)} = z^{-9}\left(\tfrac{1-z^{-4}}{1-z^{-1}}\right)^5 = z^{-4}[(1+z^{-1})(1+z^{-2})z^{-1}]^4 \\ &\cdot[(1+z^{-1}+z^{-2}+z^{-3})z^{-1}], \end{aligned} \tag{3.35}$$

$$\begin{aligned} &\text{FIR(z)} = a_0z^{-1} + a_1z^{-2} + a_2z^{-3} + ... + a_{30}z^{-31}, \text{where} \\ &\text{a0} = \text{a30} = -0.000061035; \text{a1} = \text{a29} = -0.0003662; \\ &\text{a2} = \text{a28} = -0.000366211; \text{a3} = \text{a27} = 0.001464844; \\ &\text{a4} = \text{a26} = 0.0036315918; \text{a5} = \text{a25} = -0.000823975; \\ &\text{a6} = \text{a24} = -0.012054443; \text{a7} = \text{a23} = -0.010437012; \\ &\text{a8} = \text{a22} = 0.019775390; \text{a9} = \text{a21} = 0.043701172; \\ &\text{a10} = \text{a20} = -0.002899160; \text{a11} = \text{a19} = -0.09893799; \\ &\text{a12} = \text{a18} = -0.088989258; \text{a13} = \text{a17} = 0.154602051; \\ &\text{a14} = \text{a16} = 0.516235351; \text{a15} = 0.692199707; \end{aligned} \tag{3.36}$$

By precision and error analysis, the output bit-width of the CIC filter, FIR, and IIR are 19 bits, 16 bits and 16 bits, respectively. The fourth-order IIR is a Chebyshev Type-II filter. The stability of the fourth-order Chebyshev filter is guaranteed by considering the signal swing and filter coefficients. The overall SNDR of the decimation filter is designed to be higher than 80 dB to satisfy the requirement of ADSL2+ performance.

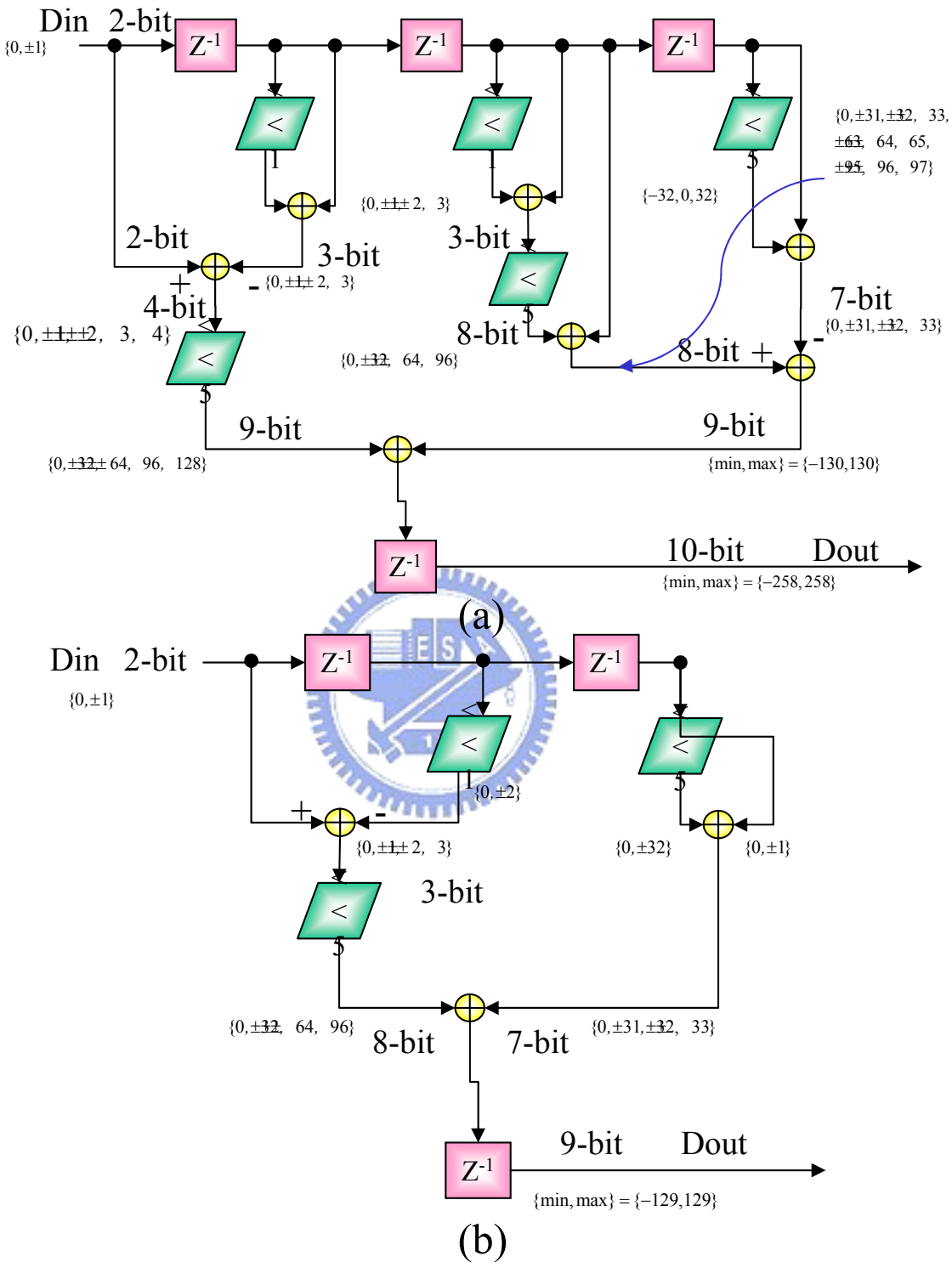

Figure 3.31: (a) $H_1(z)$ and (b) $H_2(z)$ of Circuit implementation of the cancellation filters

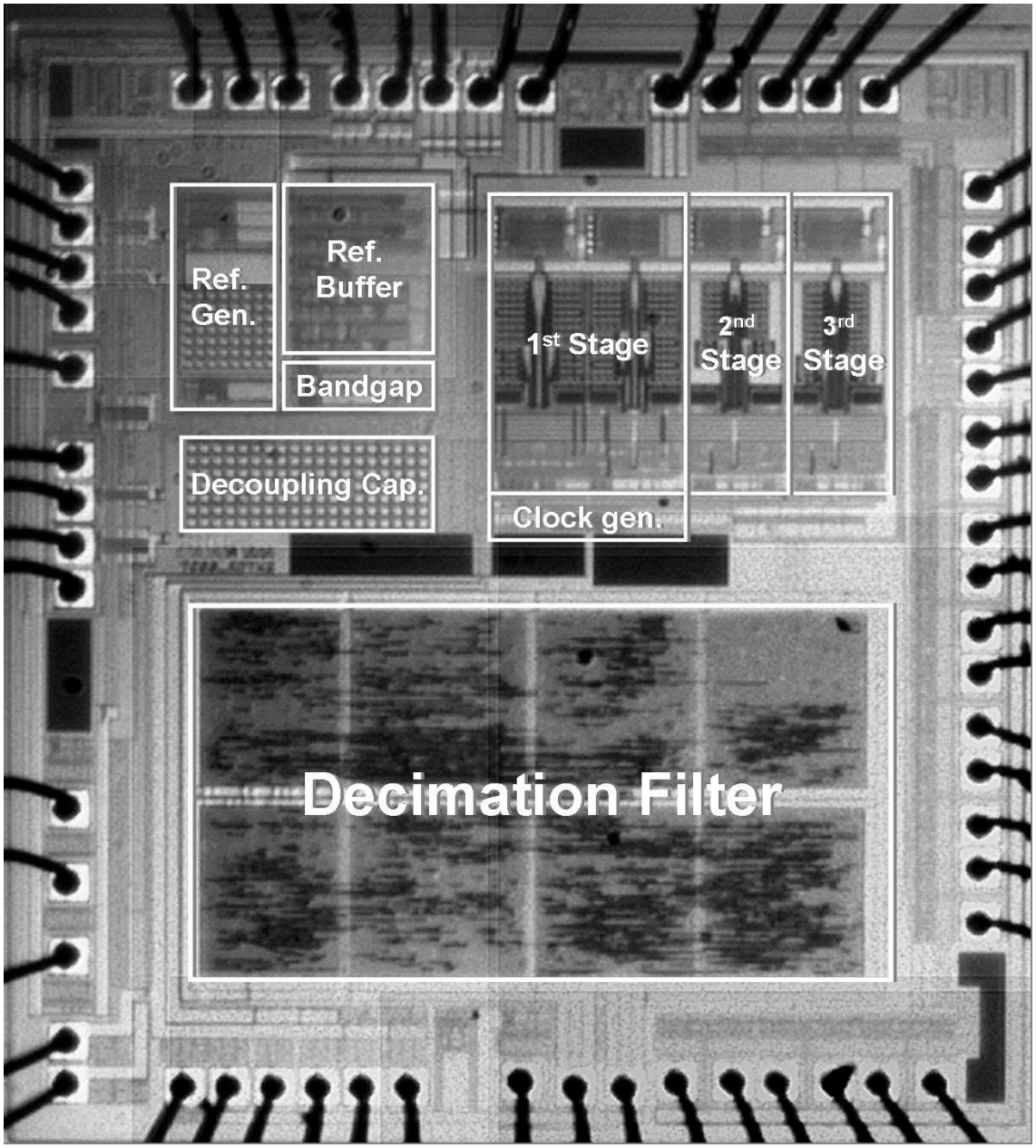

Figure 3.32: Chip micro-photograph.

3.4 Experimental Results

The modulator was fabricated in TSMC 0.25-μm 1P5M CMOS technology with metal-insulator-metal (MIM) capacitors. The power dissipation of the modulator and digital decimation filter with I/O pads is 62.5 mW and 120 mW with a 2.5-V supply, respectively. Figure 3.32 shows the chip micro-photograph in which the experimental ADC includes the clock generator, reference buffer, bandgap circuitry, and decimation filter. To measure the performance data, the chip was mounted onto a four-layer printed circuit board (PCB)to separate the analog signal from digital signal and hence reduce the crosstalk as shown in Figure 3.33. The input clock is generated from an external low-jitter crystal with independent

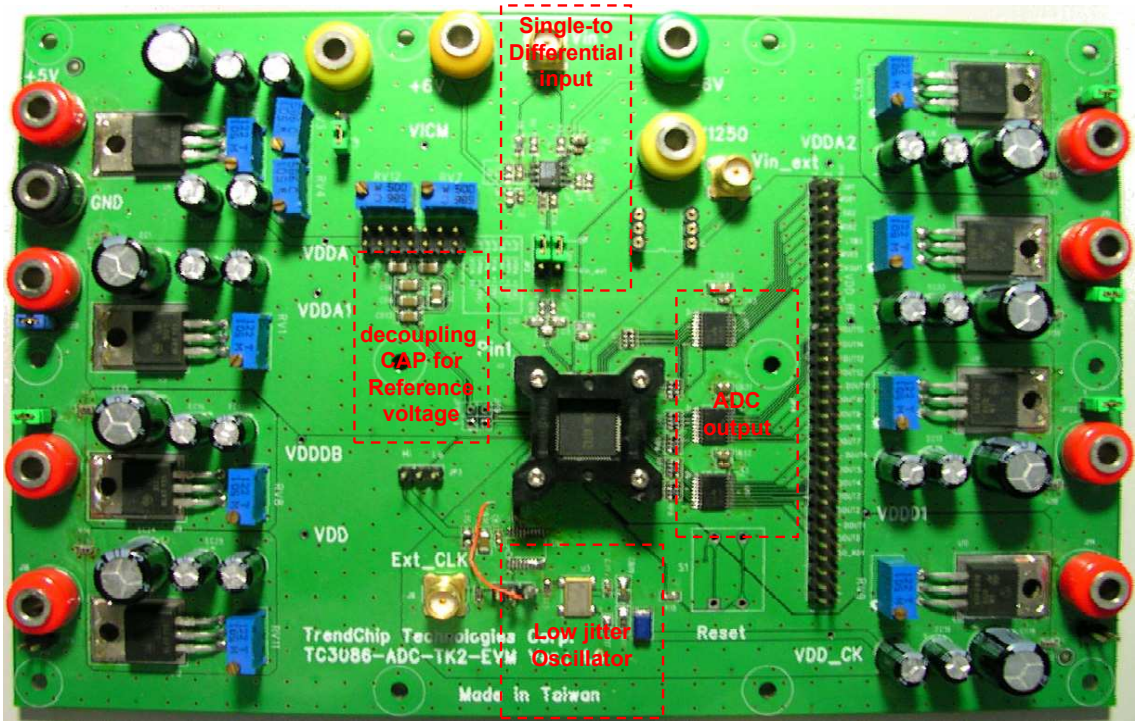

Figure 3.33: The EVM board of test chip measurement.

power supply voltages to avoid the switching-noise coupling. In order to get more insight of the proposed RMASH 2-1-$1_{1.5b}$, the performance of core modulator on the integrated ADC chip can be measured individually by turning off the digital decimation filter.

3.4.1 Modulator Performance

The modulator is designed for a sampling rate of 80 MHz and a fixed OSR of 16; so, the signal bandwidth is 2.5 MHz. Figure 3.34 shows that the modulator can achieve a dynamic range of 86 dB, a peak SNR of 83 dB, and a peak SNDR of 78.5 dB for a 2.5 MHz signal band. To observe the nonlinearity of the 1.5-bit feedback DAC, a simple DC input level was applied to the modulator. The unfiltered power spectral density (PSD) of the measured output data was shown in Figure 3.35. Accordingly, no obvious tone was observed and the measured noise floor is as low as the thermal noise calculated by sizing the sampling capacitor. Figure 3.36 illustrates the PSD of the measured output signal with a sampling rate of 80 MHz and a signal bandwidth of 2.5 MHz; the input sinusoid is -5 dB and 268-KHz. The result implies that the spurious-free dynamic range (SFDR) is 93 dB. When the modulator operates at a sampling rate of 100 MHz, as shown in Figure 3.37, it still stay functional without significant harmonic distortion and can achieve a SFDR of 90 dB. However, because of the switching activity of the digital output buffers, the in-band noise floor rapidly increases at the pad-pin

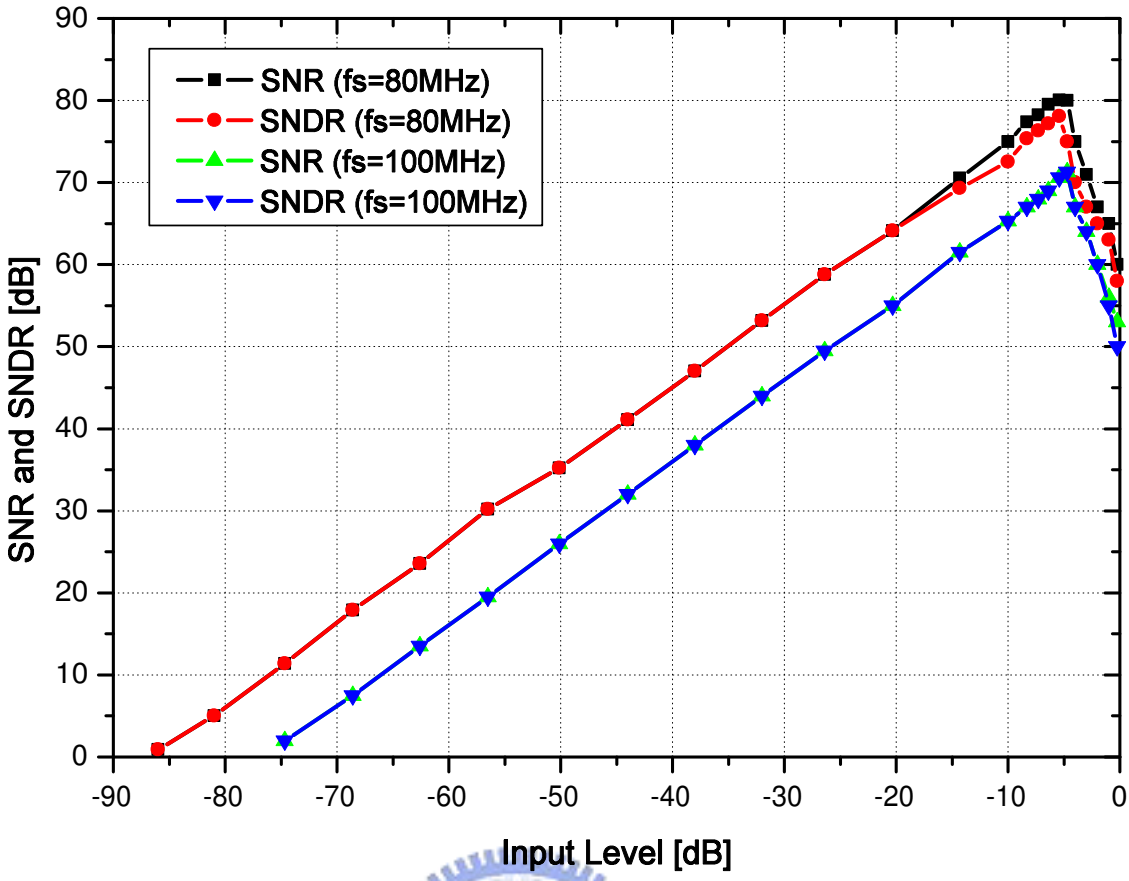

Figure 3.34: Plots of measured SNDR and SNR versus input signal level.

level, and the dynamic range and peak SNDR become 77.5 dB and 72 dB, respectively, for a 3.125 MHz bandwidth.

3.4.2 ADC Performance

Since our design target is ADSL2+ application, the ADC is operated with a sampling rate of 70.4 MHz and a fixed OSR of 16; so, the signal bandwidth is 2.2 MHz. The ADC achieves a dynamic range of 86 dB and a peak SNDR of 78 dB. Note that the overall power dissipation of the ADC can be further reduced by synthesizing the digital decimation filter with lower supply voltage. Figure 3.38 illustrates the measured SNR and SNDR against input level for the ADC. The measured output spectrum for a 500-kHz sinusoidal input is shown in Figure 3.39, and accordingly the SFDR is 89 dB. Comparing with the performance of core modulator, the SFDR drops by 4dB and more in-band tones are observed. This is attributed to the noise coupling from the switching of digital decimation filter.

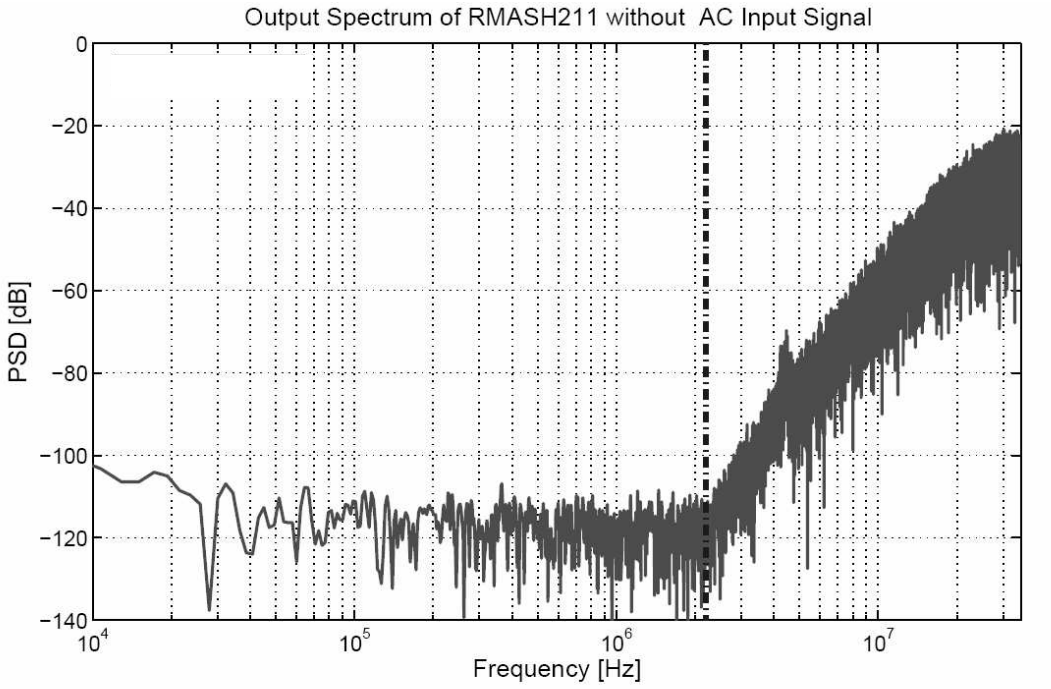

Figure 3.35: Measured output PSD of RMASH 2-1-$1_{1.5b}$ with DC input.

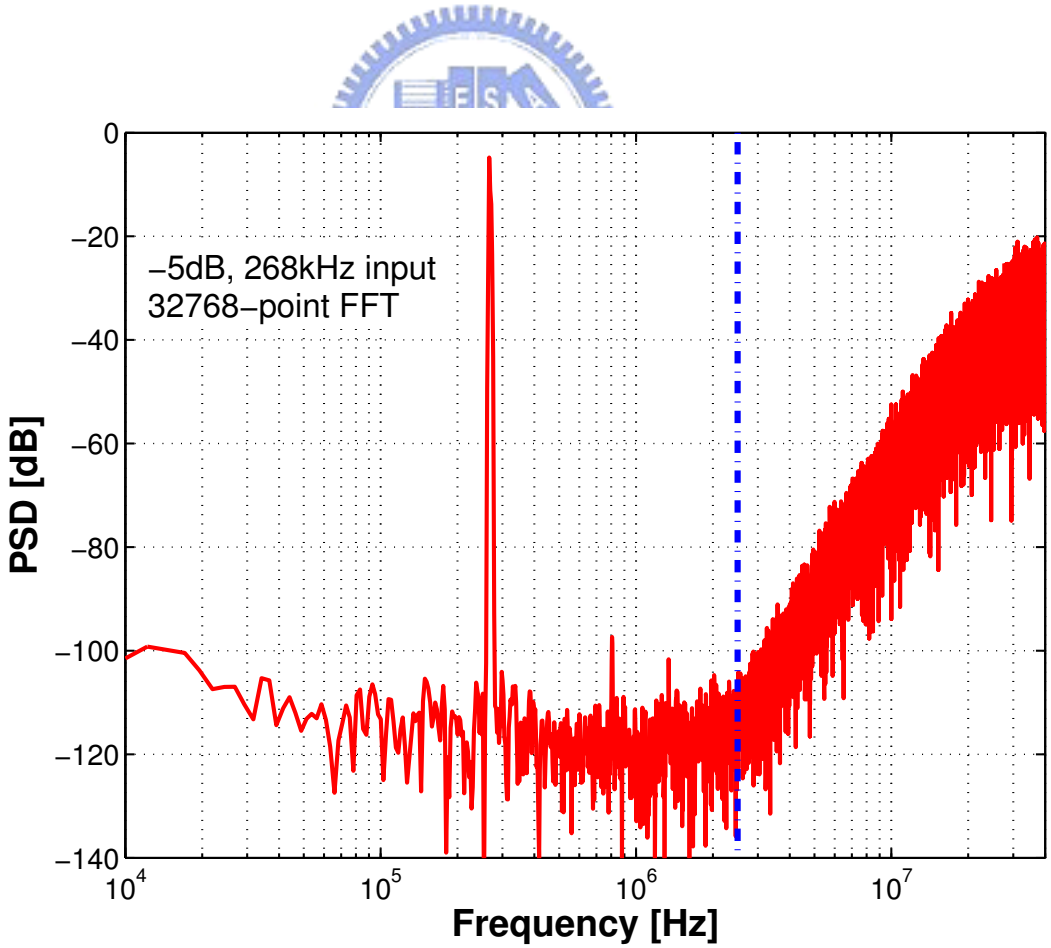

Figure 3.36: Measured output PSD of RMASH 2-1-$1_{1.5b}$ operating at 80 MHz sampling rate.

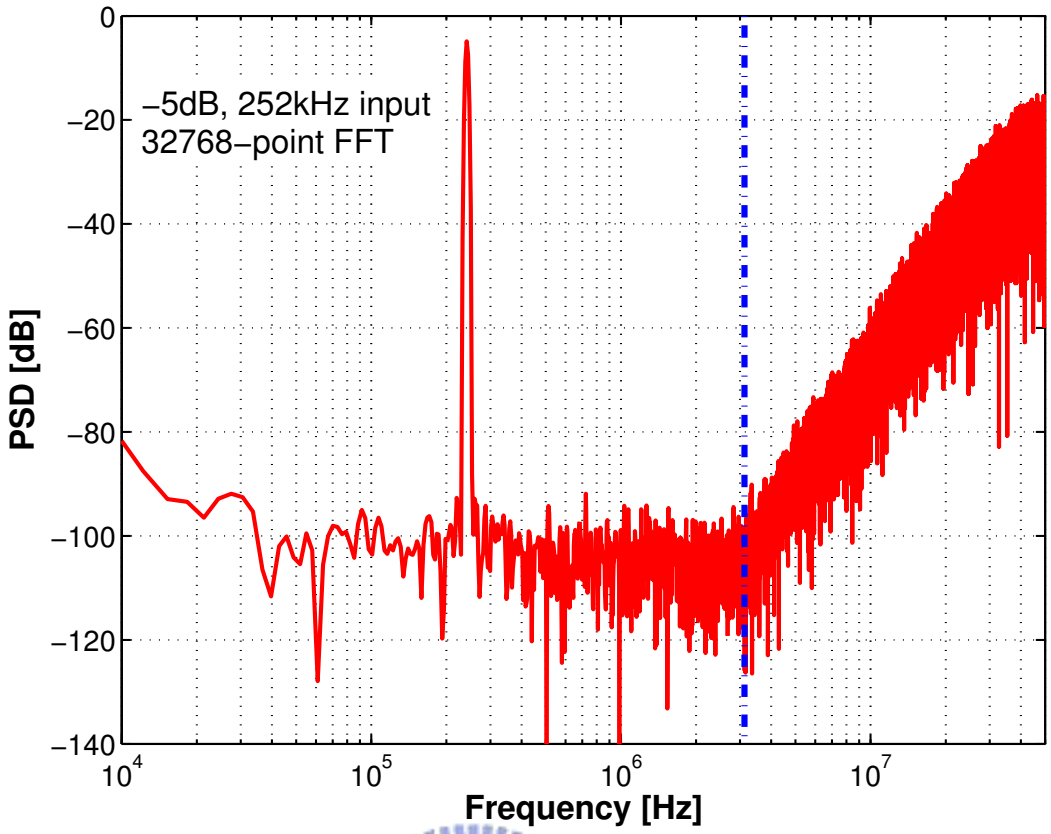

Figure 3.37: Measured output PSD of RMASH 2-1-$1_{1.5b}$ operating at 100 MHz sampling rate.

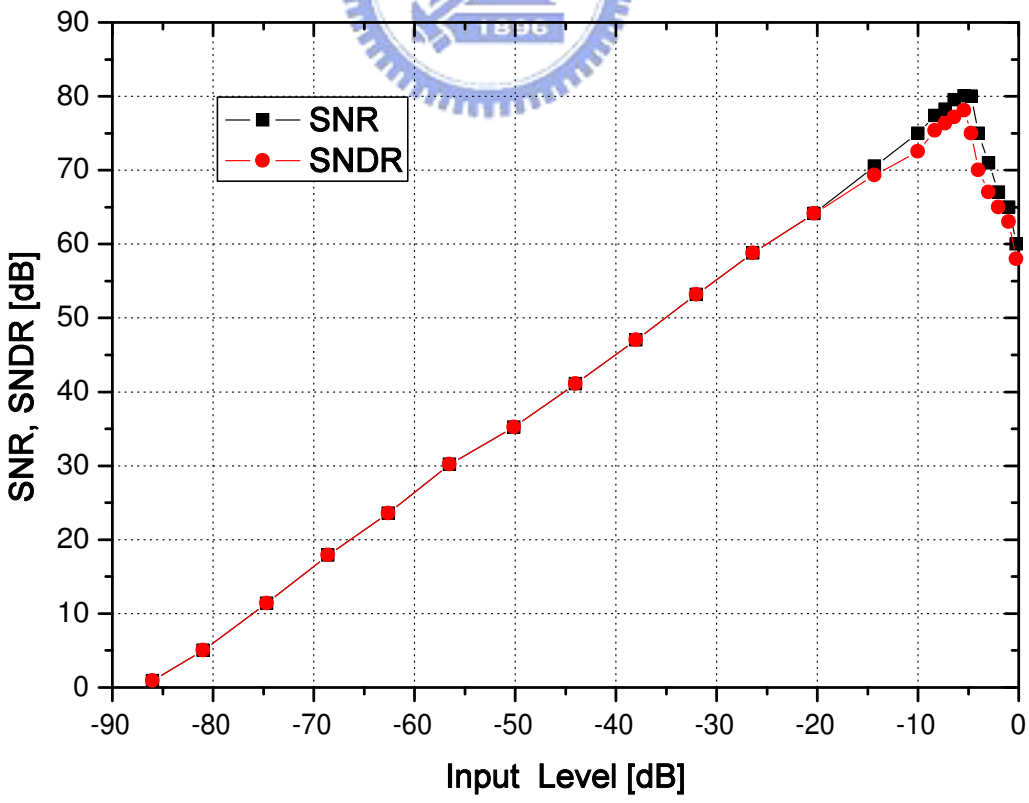

Figure 3.38: Plots of measured SNDR and SNR versus input signal level.

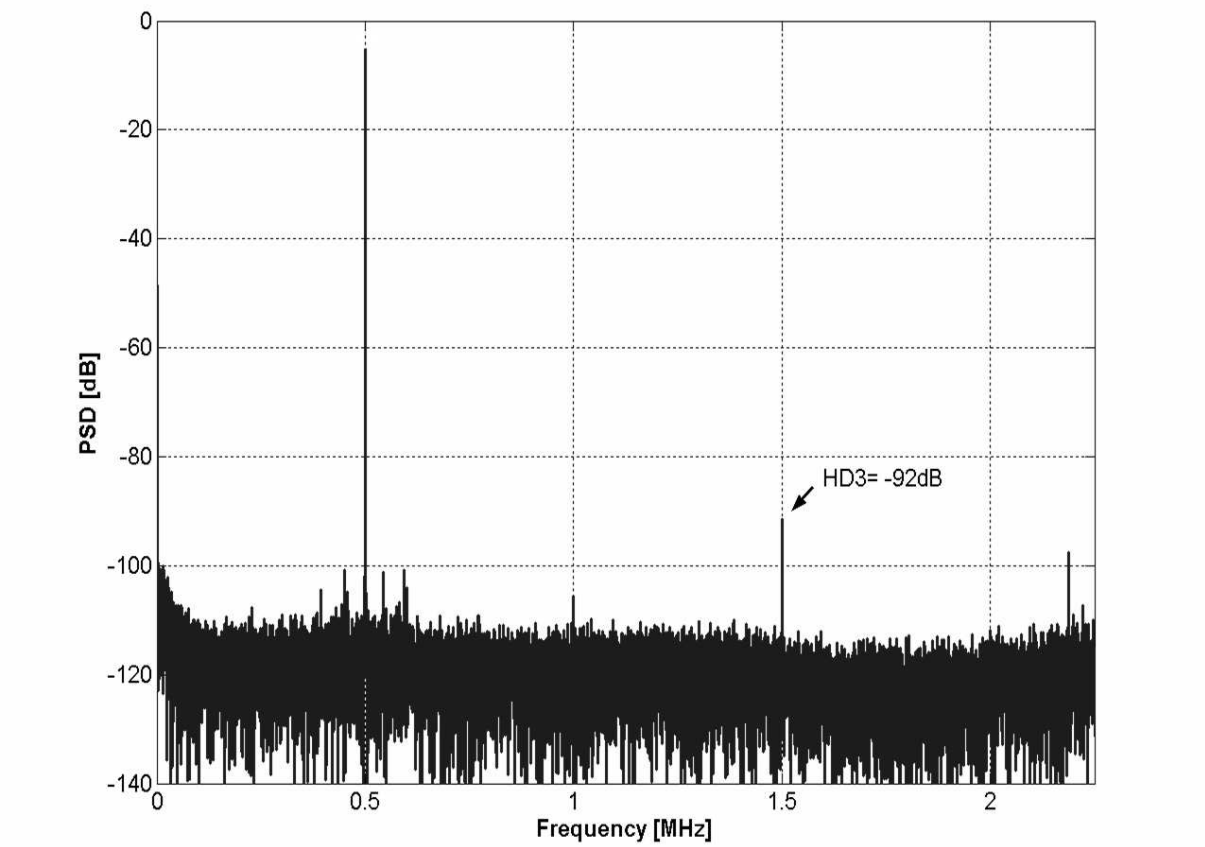

Figure 3.39: Measured output PSD of proposed RMASH 2-1-$1_{1.5b}$ ADC.

3.5 Summary

in this chapter, the design of a 14-bit, 180mW, 4.4MS/s, cascaded ΣΔ ADC with 16x OSR is addressed. The ADC includes a cascaded 2-1-1 modulator with 1.5-bit quantization and a three-stage digital decimation filter. The detailed architectural analysis and design methodology are provided. The circuit nonidealities are analyzed carefully while the circuit specifications are determined by considering optimizing the trade-off between performance and power dissipation. The principle and implementation of critical circuit blocks are described.

The measured performance is very similar to the simulated one and a 14-bit DR has been achieved. To quantitatively evaluate the efficiency among power dissipation, dynamic range, and conversion rate, we use the formulas for the effective number of bits (ENOB) of ADC and the figure-of-merit (FOM) as shown below [36], [50]:

$$\begin{aligned} ENOB &= \frac{dynamic\ range - 1.76}{6.02} \\ FOM &= \frac{Power}{2^{ENOB} \times Conversion\ Rate} 10^{12} \end{aligned} \tag{3.37}$$

Table 3.3: Performance summary of the the RMASH 2-1-$1_{1.5b}$ and the other published broadband SC modulators.

Refs	Topology	Bandwidth (MHz)	OSR	SNDR/DR (dB)	Technology (CMOS)	Die Size (mm2)	Power (mW)	FOM (pJ/conv)
[31]	5th	2	8	82 / 83	0.18-μm 1.8V	2.9	150	3.25
[32]	2nd	1.92	12	70 / 76	0.18-μm 2.7V	1.4	50	2.53
[33]	4th	2	12	74 / 80	0.25-μm 2.5V	2.6	105	3.21
[34]	2-2-1	2	16	87 / 95	0.5-μm 2.5V	10	150	0.82
[36]	2-1-1	2.2	16	72.7 / 78	0.25-μm 2.5V	2.78	65.8	2.3
this work	2-1-1	2.2	16	78.5 / 86	0.25-μm 2.5V	1.4	62.5	0.87
						2.8*	182.5*	2.5*

*Include digital decimation filter

Figure 3.40 shows the FOM distribution of our work and existing wideband (>1MHz) SC $\Sigma\Delta$ modulators. Table 3.3 summarizes the measured performance and specifications of the proposed modulator, and compares with the other wideband SC $\Sigma\Delta$ modulators as well.

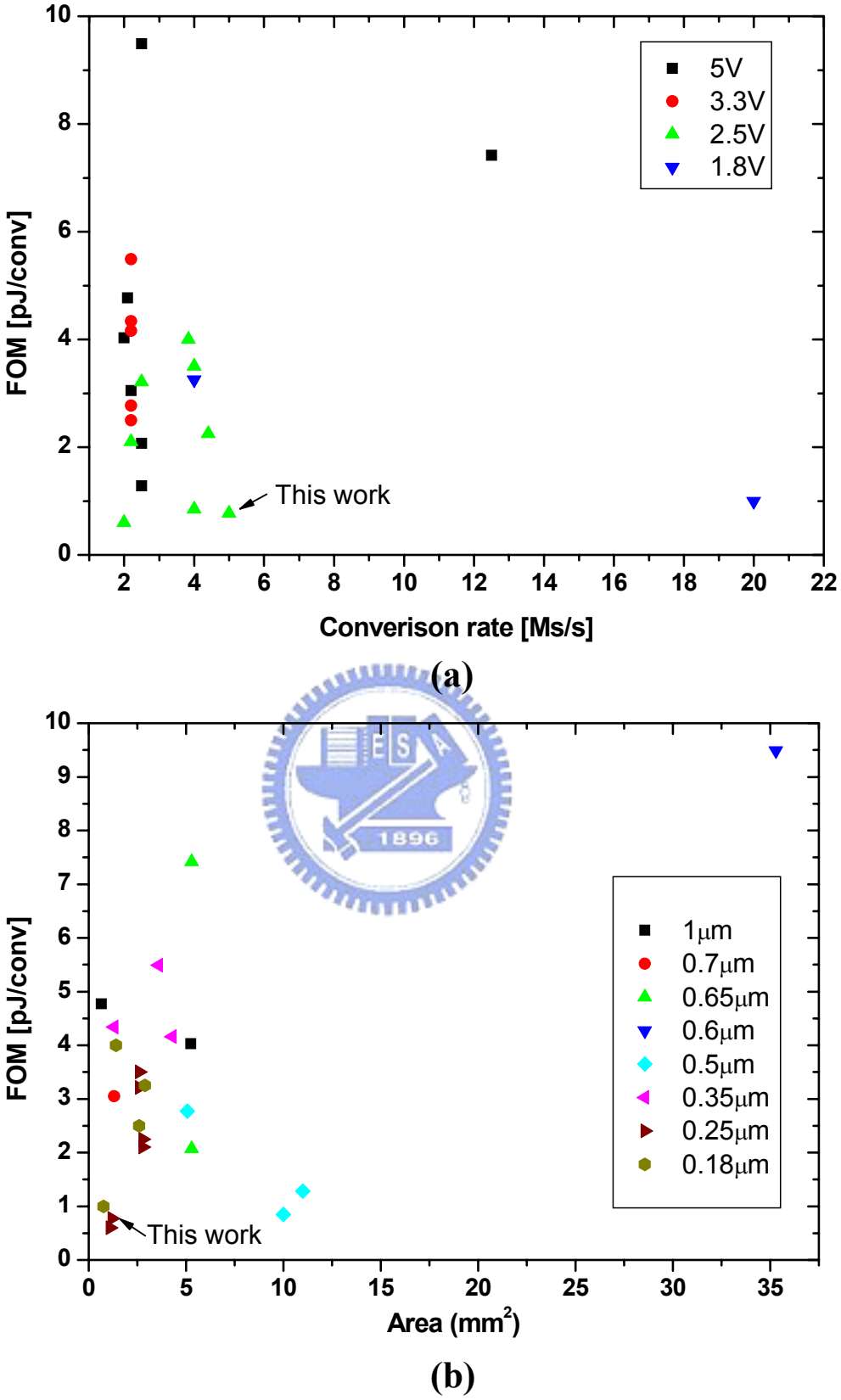

Figure 3.40: (a) FOM distribution of broadband SC ΣΔ modulators with respect to conversion rate, and (b) FOM distribution of wideband SC ΣΔ modulators with respect to area.

Chapter 4

Resonator-Based Cascaded ΣΔ Modulator for Low-OSR Applications

With the increasing demand of ΣΔ modulator with broader bandwidth and higher dynamic range (DR), new architectures or structures with low oversampling ratio (OSR) must be exploited. However, for low OSR, the ΣΔ modulator becomes very sensitive to circuit imperfection and requires high-quality components [22, 51]. Recently, cascaded (MASH), multi-bit architectures become attractive to the designers in that they can effectively reduce the OSR while maintaining the desired resolution for broadband applications. Nevertheless, the achievable resolution of a MASH multi-bit modulator is usually limited by circuit nonidealities, such as finite op-amp gain and capacitor mismatch [2, 52, 53]. Although the leakage noise is substantially attenuated when the OSR is high enough (say, greater than 32), it is not negligible in the case of low OSR. Some papers thereby propose digital calibration techniques to solve the leakage noise problem at the expense of extra costly circuits [52, 53].

This chapter propose a new architecture that not only takes advantages of using the MASH structure and introducing additional zeros into the NTF but also relieves the DR degradation caused from the circuit nonidealities [54, 55]. The key to improving DR is to have the first stage of the MASH architecture oscillated. When the first stage oscillates, the 1-bit quantization noise vanishes and hence circuit nonidealities do not cause leakage quantization noise. According to this concept, two resonator topologies, high-Q cascade-of-resonator-with-feedforward (HQCRFF) and low-Q cascade-of-integrator-with-feedforward (LQCIFF), are selected to realize the internal loop filters in the proposed modulator. In proposed architecture, we use HQCRFF-based single-bit modulator at the first stage and LQCIFF-based multi-bit modulator at the second stage. Depending on the input amplitude,

the first stage can operate in either modulation mode or oscillation mode. When the input amplitude is less than a threshold voltage, the first stage oscillates because its internal loop is high-Q lossless resonator. According to simulation results, the threshold voltage of this oscillation varies with the OSR of the modulator; that is, the lower the OSR the higher the threshold voltage. Furthermore, the simulation results show that the transient behavior between oscillation and modulation modes of the HQCRFF single-bit structure has "*inertia*". For instance, when the HQCRFF operates in oscillation mode, the larger threshold level is required to force it back into modulation mode. It implies that the architecture can be immune to circuit nonidealities over a large portion of input range when OSR is low. Yet, when the first stage operates in modulation mode, the leakage coarse quantization noise still occurs and limits the achievable peak signal-to-noise-plus-distortion (SNDR) of modulator. Thanks to the NTF with additional zeros, the peak SNDR of the proposed architecture is still efficient.

The theoretic analysis of operating condition for oscillation mode is presented and the transient behavior between two modes is also discussed. The design methodology and simulation result of RMASH are given. As can be seen from the simulation results, without using additional calibration techniques, the DR of the proposed RMASH 2-0 and RMASH 2-2 architectures with the op-amp dc gain of 60 dB, the capacitor mismatch of 0.2% and the OSR of 8 can be as high as 87 dB and 84 dB, respectively. Finally, the circuit implementation of RMASH 2-2 for Wideband Code-Division Multiple-Access (WCDMA) standard is addressed. The SPICE simulation results shows the RMASH 2-2 can achieve the DR of 82 dB and dissipates only 55 mW from a 2.5V supply voltage.

4.1 Leakage Quantization Noise

Figure 4.1 shows the block diagram of the traditional MASH 2-2 in which there are two quantization noises, E_{Q1} and E_{Q2}. Ideally, E_{Q1} can be further cancelled by the error correction logic (ECL) and the output signal $Y(z)$ is free of the quantization noise E_{Q1}. To observe E_{Q1}, let us assume that $X(z)$ and E_{Q2} are zeros. Equation (4.1) shows the outputs $Y_1(z)$ and $Y_2(z)$ in terms of $H_1(z)$, $H_2(z)$, and $E_{Q1}(z)$, where NTF_1 is the noise transfer function of the first stage and STF_2 is the signal transfer function of the second stage.

$$\begin{cases} Y_1(z) = \frac{1}{1+H_1(z)} \cdot E_{Q1}(z) = NTF_1(z) \cdot E_{Q1}(z) \\ Y_2(z) = \frac{H_2(z)}{1+H_2(z)} \cdot E_{Q1}(z) = STF_2(z) \cdot E_{Q1}(z) \end{cases} \tag{4.1}$$

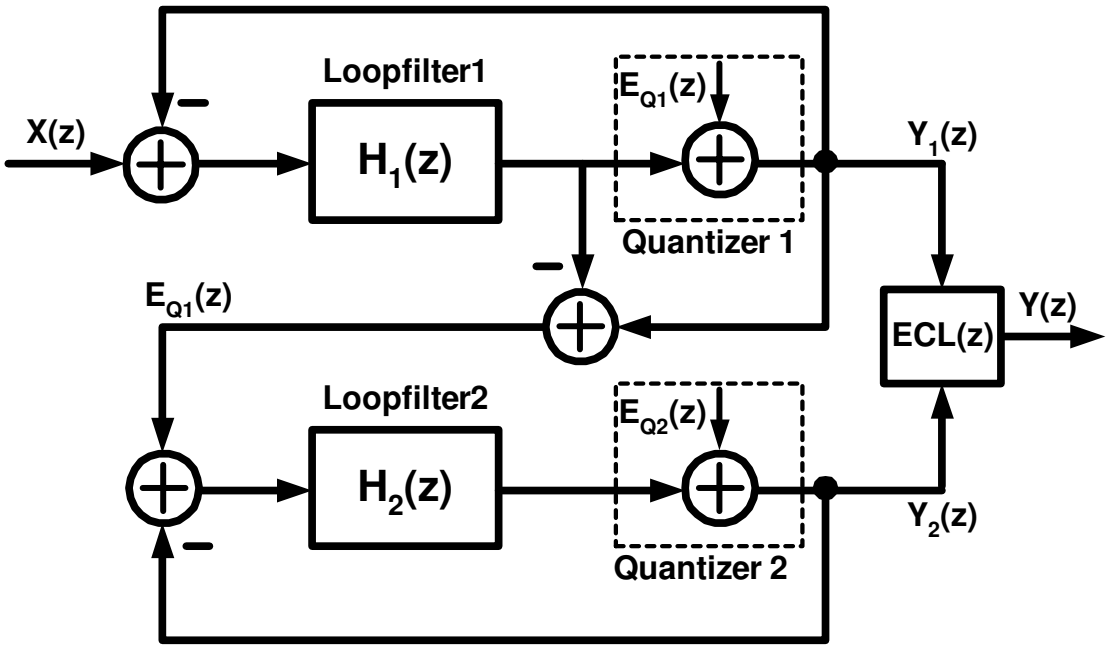

Figure 4.1: The traditional MASH ΣΔ modulators.

Given $STF_2(z) = 1$, when $ECL(z) = Y_1(z)$, the output $Y(z) = Y_1(z) - Y_2(z) \cdot ECL(z)$ becomes zero and thus the noise E_{Q1} is cancelled. Unfortunately, in practical, E_{Q1} cannot be cancelled completely because of the circuit nonidealities who cause the mismatches between $ECL(z)$ and $NTF_1(z)$. In this brief, we mainly deal with two nonidealities: the finite op-amp gain and capacitor mismatch. These two nonidealities make the integrator of $NTF_1(z)$ nonideal with pole error and gain error, as shown in Equation (4.2).

$$I(z) = \frac{(1-\alpha)\, z^{-1}}{1-(1-\mu)\, z^{-1}} \tag{4.2}$$

where μ is the inverse of the op-amp dc gain and α is the capacitor mismatch. The nonideal integrator thereby causes the inequality of $NTF_1(z)$ and $ECL(z)$ and hence the leakage noise. Equation (4.3) expresses the leakage noise due to the circuit nonidealities.

$$Y_{leakage}(z) = E_{Q1}(z) \cdot (NTF_1(z) - ECL(z)) \tag{4.3}$$

Article [56] has shown that the contribution of the leakage noise caused by the finite op-amp dc gain and capacitor mismatch to the MASH 2-2 as:

$$P_{leakage} \approx \frac{\Delta^2}{12}\left(\frac{\mu^2\pi^2}{3OSR^3} + \frac{\alpha^2\pi^4}{5OSR^5}\right) \tag{4.4}$$

where $\triangle$ is the level step of the first quantizer and OSR is the oversampling ratio of the modulator. Based on Equation (4.4), for high OSR, the leakage noise is substantially attenuated and can be neglected when comparing with the other noise sources. Nevertheless, for low OSR and a single-bit quantizer, it is not negligible and the SDM requires high-performance circuitry with little μ and α. For instance, the MASH 2-2 with the OSR of 8, a single-bit quantizer and the DR of 84dB requires the op-amp dc gain of 90 dB and the capacitor matching of 0.025%. Note that the specifications are hard to be achieved in the modern CMOS technology, especially for low voltage circuit. The digital calibration techniques are proposed to solve the leakage noise problem, but they usually require costly additional circuit [52, 53].

4.2 The Proposed Resonator-Based Modulator

In this section, we will first give a conceptual architecture to avoid the leakage quantization noise of a MASH modulator. In the following, a new single-bit resonator-based modulator with an *oscillation mode* is proposed to achieve leakage noise removal like the conceptual architecture. Finally, the theoretic analysis and transition behavior of the proposed resonator-based modulator are addressed in detail.

4.2.1 The Conceptual Architecture

The key idea of the proposed architecture that avoids the leakage quantization noise is motivated from blocking the quantization noise E_{Q1} to the second stage. To start with, we simply remove the feedback path of the first stage as illustrated in Figure 4.2. Doing so, the first stage becomes an open-loop structure and losses the capability of error tracking and noise shaping. Then, the output $I(z)$ of $H_1(z)$ does not deliver the quantization noise E_{Q1} and hence there is no leakage noise. To have this conceptual architecture the same performance as MASH, the overall STF of $\Sigma\Delta$ modulator has to be unity and the result of $ECL(z) \cdot H_1(z)$ must be equal to unity. Thereafter, the output $Y(z)$ can be expressed as Equation (4.5), in which the contribution of E_{mb} to the output is exactly the same as that of MASH.

$$Y(z) = X(z) + NTF_2(z) \cdot ECL(z) \cdot E_{mb}(z) \tag{4.5}$$

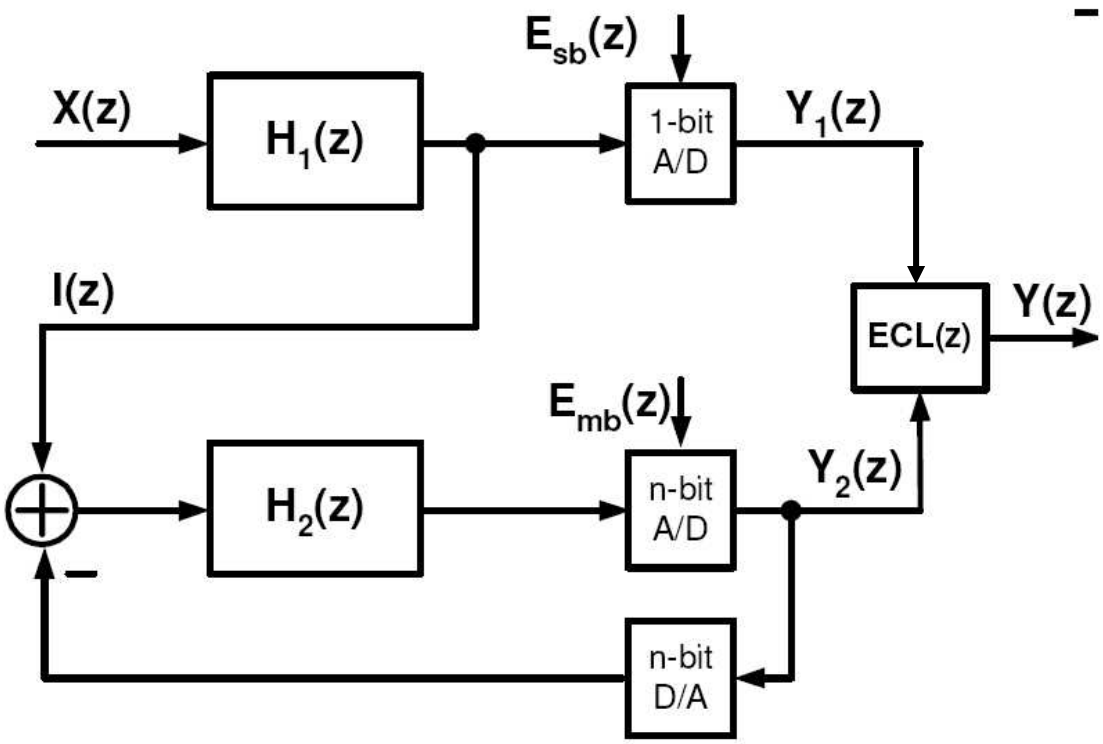

Figure 4.2: The conceptual block diagram of the leakage noise removal.

where the $NTF_2(z)$ is the noise transfer function of the second stage and $E_{mb}(z)$ is the quantization noise of the multi-bit quantizer in the second stage.

Since $ECL(z)$ is equal to $NTF_1(z)$ in Equation (4.1), the $ECL(z)$ is a high-pass filter and its in-band gain can be less than unity. As mentioned above, the loop filter $H_1(z)$ of Figure 4.2 is the inverse of $ECL(z)$ and thus the in-band gain of $H_1(z)$ can be greater than unity. For a large input amplitude, the output $I(z)$ of the loop filter $H_1(z)$ may make the second stage saturated. The saturation will then cause severe harmonic distortion and consequently degrade the DR. Therefore, the architecture may suffer from the DR degradation, in spite of its leakage noise removal. In the following, we will propose a single-bit resonator-based modulator which can be used in the first stage of a MASH to avoid the leakage noise and DR degradation.

4.2.2 The Single-Bit HQCRFF Modulator

To avoid the DR degradation while the leakage noise is warded off, we hence propose a single-bit high-Q cascade-of-resonator-with-feedforward (HQCRFF) modulator as the first stage of the MASH, which is shown in Figure 4.3. It is interesting that depending on the input signal amplitude, this kind of modulator has two different functional properties [57].

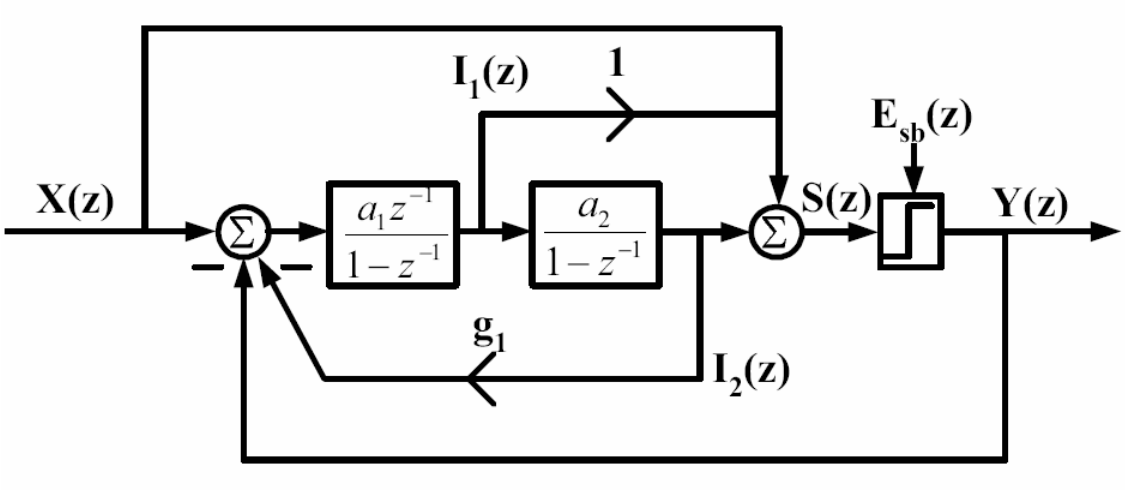

Figure 4.3: The architecture of proposed single-bit HQCRFF modulator.

This is because the loop filter induces a strong resonance power that may make the input signal underflow, and consequently the quantizer output is free of the input signal. Under this situation, the HQCRFF loses the capability of error tracking and the feedback path from quantizer output to input summing stage is equivalently disable. In other words, the HQCRFF has similar behavior to the first stage of the conceptual architecture and we call that it operates in oscillation mode. The oscillation means the resonance power dominates the behavior of the modulator. On the contrary, we call the HQCRFF operates in modulation mode when the feedback path recovers the capability of error tracking. Therefore, the HQCRFF can operate in either oscillation mode and modulation mode depending on the amplitude of the input signal.

4.2.3 Condition of Oscillation Mode

In this subsection, we will discuss the behavior and the condition of oscillation mode with theoretic analysis. First, the signal transfer function (STF) and noise transfer function (NTF) of Figure 4.3 are shown in Equations (4.6) and (4.7), respectively.

$$STF(z) = \frac{k_q[1 + (r + a_1 + a_1a_2 - 2)z^{-1} + (1 - a_1)z^{-2}]}{1 + (r + a_1k_q + a_1a_2k_q - 2)z^{-1} + (1 - a_1k_q)z^{-2}} \tag{4.6}$$

$$NTF(z) = \frac{1 - (2 - r)z^{-1} + z^{-2}}{1 + (r + a_1k_q + a_1a_2k_q - 2)z^{-1} + (1 - a_1k_q)z^{-2}} \tag{4.7}$$

where $r = a_1 a_2 g_1$ presents the resonance frequency and k_q is the gain of single-bit quantizer. Let the characteristic equation to be zero,

$$1 + (r + a_1 k_q + a_1 a_2 k_q - 2)z^{-1} + (1 - a_1 k_q)z^{-2} = 0 \tag{4.8}$$

and the poles of the HQCRFF are shown in the follow.

$$z_p = \frac{-b \pm \sqrt{b^2 - 4c}}{2} \tag{4.9}$$

where $b = r + a_1 k_q + a_1 a_2 k_q - 2$ and $c = 1 - a_1 k_q$

Note that when the HQCRFF operates in oscillation mode, it can be considered as a linear system. This is because the constant resonance signal dominates the behavior of the HQCRFF and thus the gain of single-bit quantizer is approximated to constant. According to Z-domain analysis [58], for a linear system, the condition of periodic oscillation is that the poles is located on the unity circle. Given r and set $z_p = 1$, we can find out the specific value of K_q for oscillation mode as follow

$$K_q = -\frac{r - 4}{2a_1 + a_1 a_2}. \tag{4.10}$$

For instance, the theoretic value of the K_q for oscillation mode is equal to 3.11 when we set $a_1 = a_2 = 0.5$ and $g_1 = 0.45$. For the sake of comparison, the simulated values of the K_q for oscillation mode are shown in Figure 4.4. According to Figure 4.4, the simulated result agrees with theoretic value well and the K_q is approximately independent of input signal power in oscillation mode. Now consider a two-tone input signal and simulation result is shown Figure 4.5. Accordingly, the K_q is also independent of input signal frequency in oscillation mode.

Since the presence of the oscillation mode depends on the input signal amplitude, we have to derive a threshold voltage which can define what modes the HQCRFF will operate in. Recall that the presence of the oscillation mode is because in the loop filter the strong resonance power masks the input signal power. Thus the constrain of oscillation mode is shown as the follows,

$$P_{in} < -|G_{RES} + G_{STF}| = |G_{NTF}|, \tag{4.11}$$

where P_{in} denote the input signal power; G_{RES}, G_{RES}, and G_{NTF} present the in-band

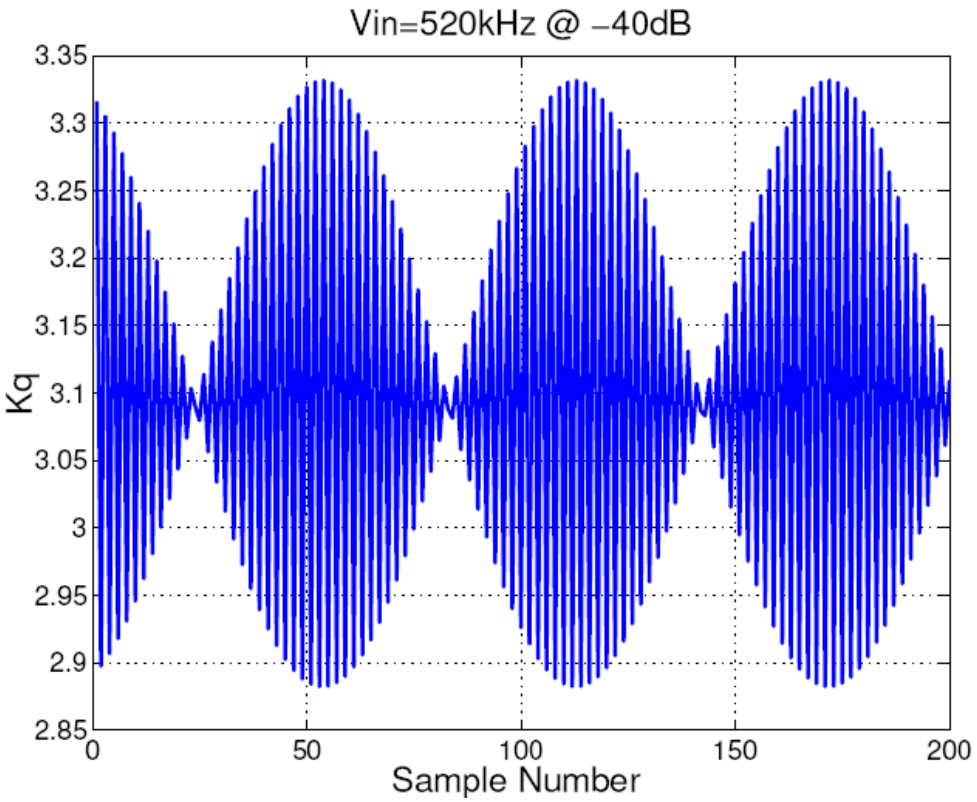

Figure 4.4: The simulated K_q of HQCRFF with single-tone input in oscillation mode.

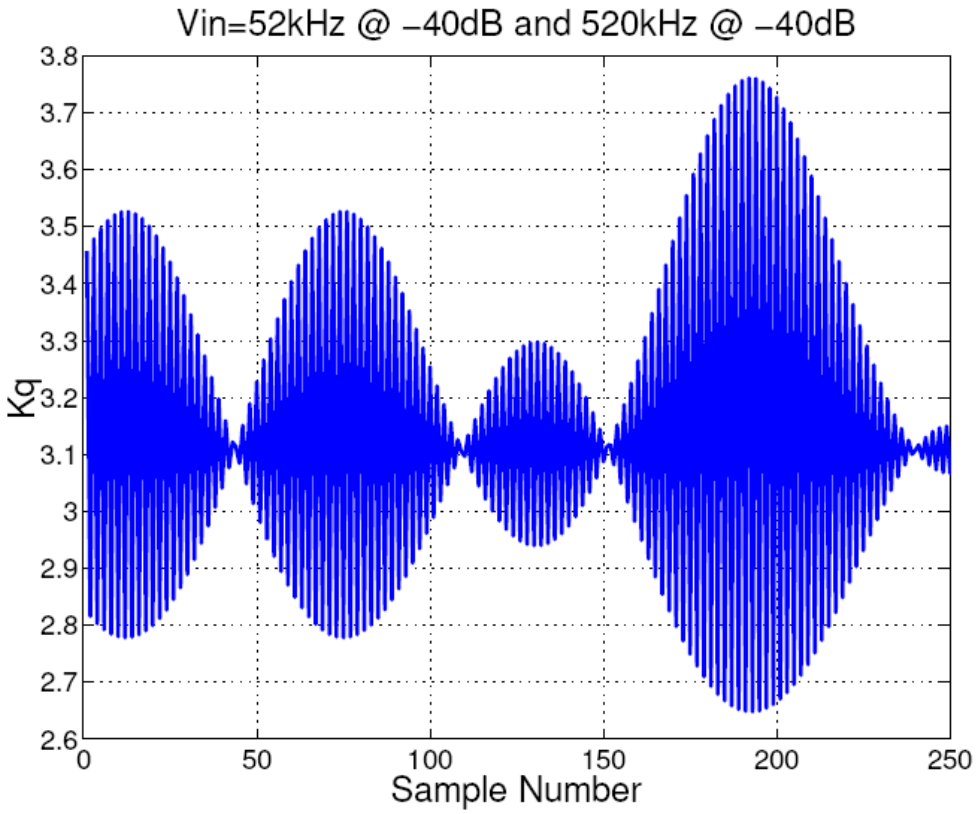

Figure 4.5: The simulated K_q of HQCRFF with single-tone input in oscillation mode.

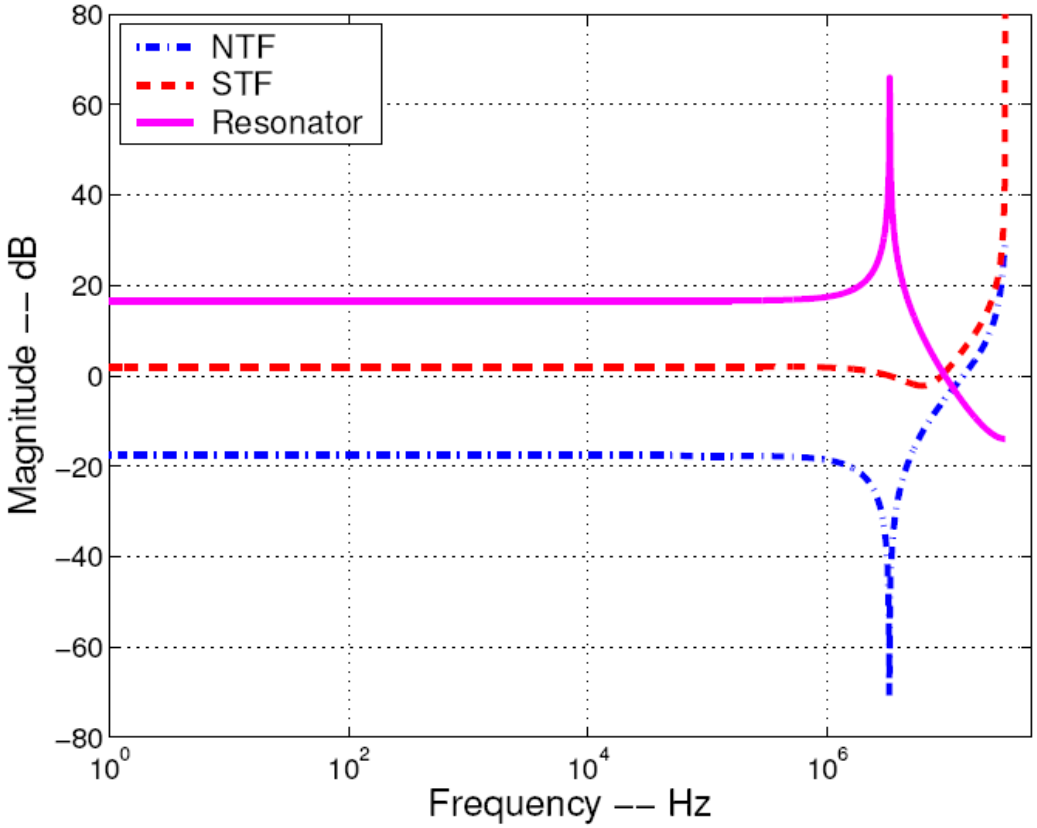

Figure 4.6: The frequency responses of NTF, STF, and resonator of HQCRFF.

resonator gain, in-band STF gain, and in-band NTF gain, respectively. Based on Equation (4.11), the input threshold voltage, V_{th}, can be approximately derived as the in-band NTF gain of HQCRFF.

$$V_{th} \cong |NTF(z)|_{z=e^{j\omega_{in}}} , \tag{4.12}$$

where ω_{in} denotes the input signal frequency. Notice that Equation (4.12) is valid when we assume that $\omega_{in} < \omega_{resonator}$ and the PSD of quantization noise is equal to unity. If the ω_{in} is close to $\omega_{resonator}$, the amplitude gain of loop filter becomes much large and HQCRFF will, more probably, operate in modulation mode. This fact is important since we hope that HQCRFF can operate in oscillation mode for a large range of input amplitude. One simple way to overcome this problem is that let the resonant frequency outside the signal bandwidth at the expense of peak SNR loss. For instance, given $a_1 = a_2 = 0.5$, $g_1 = 0.45$, and k_q=3.11, the frequency responses of NTF, STF, and resonator of the HQCRFF are shown in Figure 4.6. The theoretic value of V_{th} is -18 dB and the simulated value of V_{th} is about -20 dB. Figure 4.7 shows the theoretic values and simulated results of input threshold voltage using Equation (4.12) and SIMULINK, respectively. According to Figure 4.7, we can find that

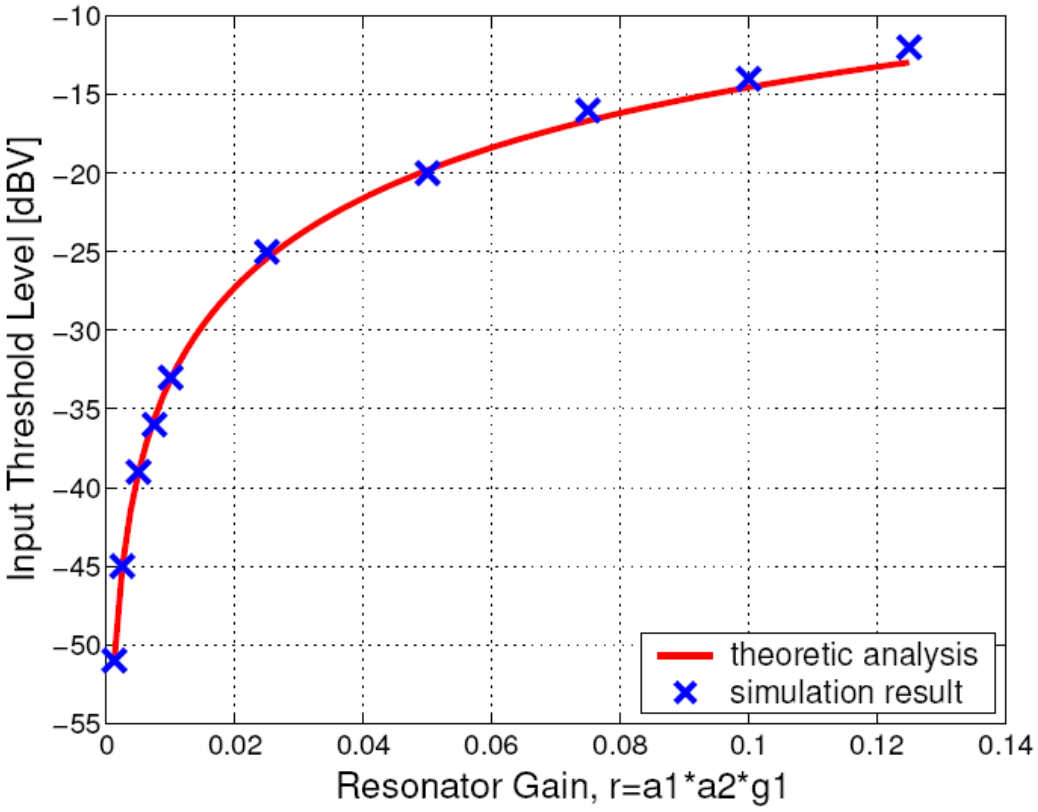

Figure 4.7: The theoretic values and simulated results of input threshold voltage using Equation (4.12) and SIMULINK.

the theoretic analysis agree the simulation results well and the higher the resonator loop gain the higher the input threshold voltage. Since the resonator loop gain, r, determines the notch frequency of NTF as well as the input singal bandwidth, the OSR of HQCRFF is also function of resonator loop gain. This means that the performance of a low-OSR HQCRFF is dominated by the oscillation mode, which can be used to eliminate the leakage quantization noise of a MASH modulator. In all simulations, however, we use the sinusoids with constant amplitude to analyze the behavior of the oscillation mode. This means we do not consider the transient and transition analysis here. Therefore, the transient and transition analysis between oscillation mode and modulation mode will be addressed in the next subsection.

4.2.4 Transient and Transition Behavior of Oscillation Mode

In the above subsection, the input signals with constant amplitude have been used to determine occurrence of the oscillation mode. Practically, the signal amplitudes in real world are dynamic. Here we use two approaches to evaluate the transient and transition behaviors of the proposed HQCRFF structure. In the first approach, a fixed-frequency sinusoid with dynamic input amplitude is applied to analyze the transient behavior of HQCRFF. The

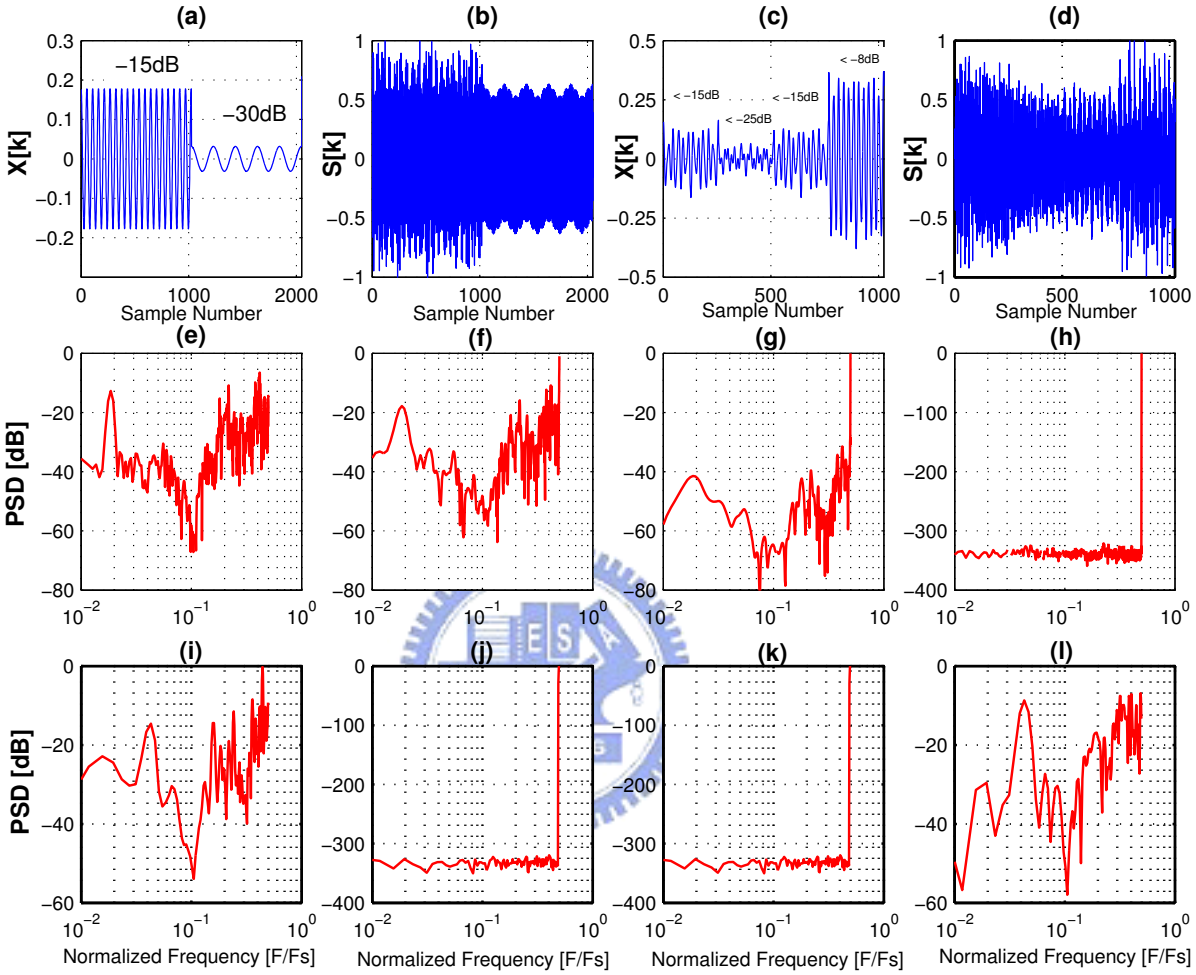

Figure 4.8: (a), (b) X[k] and S[k] of HQCRFF with two dynamic amplitudes, -15dB and -30dB of the input sinusoid; (c), (d) X[k] and S[k] with dynamic amplitudes, -15dB, -25dB, -15dB, and -8dB of the input band-limited signal; (e)-(h) The transient behavior of HQCRFF with input sinusoid: The short-time FFTs of HQCRFF outputs for four data intervals, 1∼1024, 513∼1536, 769∼1792, and 1025∼2048 points, respectively; (i)-(l) The transition behaviors of HQCRFF with input band-limited signal: The short-time FFTs of HQCRFF outputs for four data intervals, 1∼256, 257∼512, 513∼768, and 769∼1024 points, respectively.

four output spectrum of HQCRFF with overlap intervals are performed to understand what happen during transient between oscillation and modulation modes. According to simulation results of Figure 4.8(e)∼(h), we can find that the switching between oscillation and modulation modes does not occur suddenly, but smoothly. Thus it does not cause the discontinuity and hence harmonic distortion. In the second approach, the a band-limited signal with dynamic input amplitude is applied to analyze the transition behavior of HQCRFF. Similarly, the four output spectrum of HQCRFF, but with non-overlap intervals are performed to evaluate what the threshold voltage is required to change the operation mode of HQCRFF. Figure 4.8(i)∼(l) show the output spectrum of the four different intervals. As the simulation results, we can find that the transition behavior between oscillation and modulation modes has the "*inertia*", that is, when the HQCRFF operates in oscillation mode, the larger threshold voltage is required to force the HQCRFF back into modulation mode. This fact implies that one can make the HQCRFF operates in oscillation for wider input range. In the following sections, we will show that the oscillation of HQCRFF can be further used to improve the performance of the MASH ΣΔ modulator.

4.3 Proposed HQCRFF-based MASH Modulator

The presence of oscillation mode in the HQCRFF-based modulator is not a good phenomenon for single-loop ΣΔ modulator since it results in the fail of the normal analog-to-digital conversion. However, the oscillation in the first stage can improve DR of a MASH ΣΔ modulator. When the first stage oscillates, the coarse quantization noise vanishes and hence nonideal circuit effects, such as finite op-amp gain and capacitor mismatch, do not cause leakage quantization noise problem. The detailed analysis and discussion of the resonator-based MASH will be made in following subsections.

4.3.1 RMASH 2-0 ΣΔ Modulator

In the article [59], Leslie and Singh proposed an attractive multistage architecture. It improves the peak SNDR of a ΣΔ modulator with multi-bit quantizer, but only uses single-bit feedback to avoid the extremely linearity requirement of the traditional multi-bit DAC approach. Such architecture can be terms as MASH M-0 structure. However, the performance of this architecture would be seriously degraded due to imperfect matching between the analog and digital NTFs. By replacing the internal loop filter with the HQCRFF structure, a

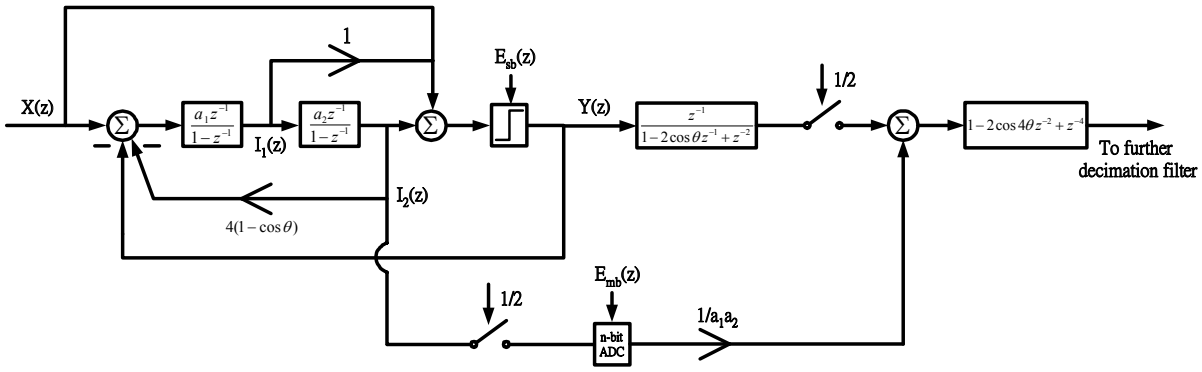

Figure 4.9: The proposed HQCRFF-based MASH 2-0 with RSR technique

new architecture of the MASH 2-0 is proposed to avoid from this performance degradation. Furthermore, paper [60] also addresses the MASH M-0 with an improved reduced-sample-rate (RSR) technique. Their approach not only reduces the sampling rate of the multi-bit quantizer in second stage but also improves the SNR loss existed in [61]. Nevertheless, it uses two multi-bit quantizers and may need DEM technique to enhance the DAC linearity. Because of the similarity of internal loop filter between our approach and paper [60], we also use this improved RSR technique in our approach. The proposed HQCRFF-based MASH 2-0 with RSR technique is shown in Figure 4.9.

Recall that when the input signal amplitude is less than the threshold level, the HQCRFF-based modulator is in oscillation mode. Thereafter, the modulator output is free of the single-bit quantization noise. Although the first stage is out of function when it is oscillating, fortunately, the second stage can still provides the signal path for the analog-to-digital conversion. This not only keeps the same functionality as the standard MASH 2-0 architecture, but also eliminates the performance degradation caused by the leakage noise of the single-bit quantizer. When wide bandwidth and high DR are required, the proposed HQCRFF-based MASH 2-0 with RSR technique becomes attractive because it does not need the additional calibration technique [52, 53].

4.3.2 RMASH 2-2 $\Sigma\Delta$ Modulator

Figure 4.10 shows the proposed resonator-based MASH 2-2 (RMASH 2-2) architecture in which the first stage is HQCRFF single-bit structure and the second stage is LQCIFF multi-bit structure. Having the HQCRFF in first stage, the RMASH 2-2 naturally has two different operation modes depending on the amplitude of input signal. When the amplitude of input signal is larger than the threshold voltage, the RMASH 2-2 operates in the modulation mode.

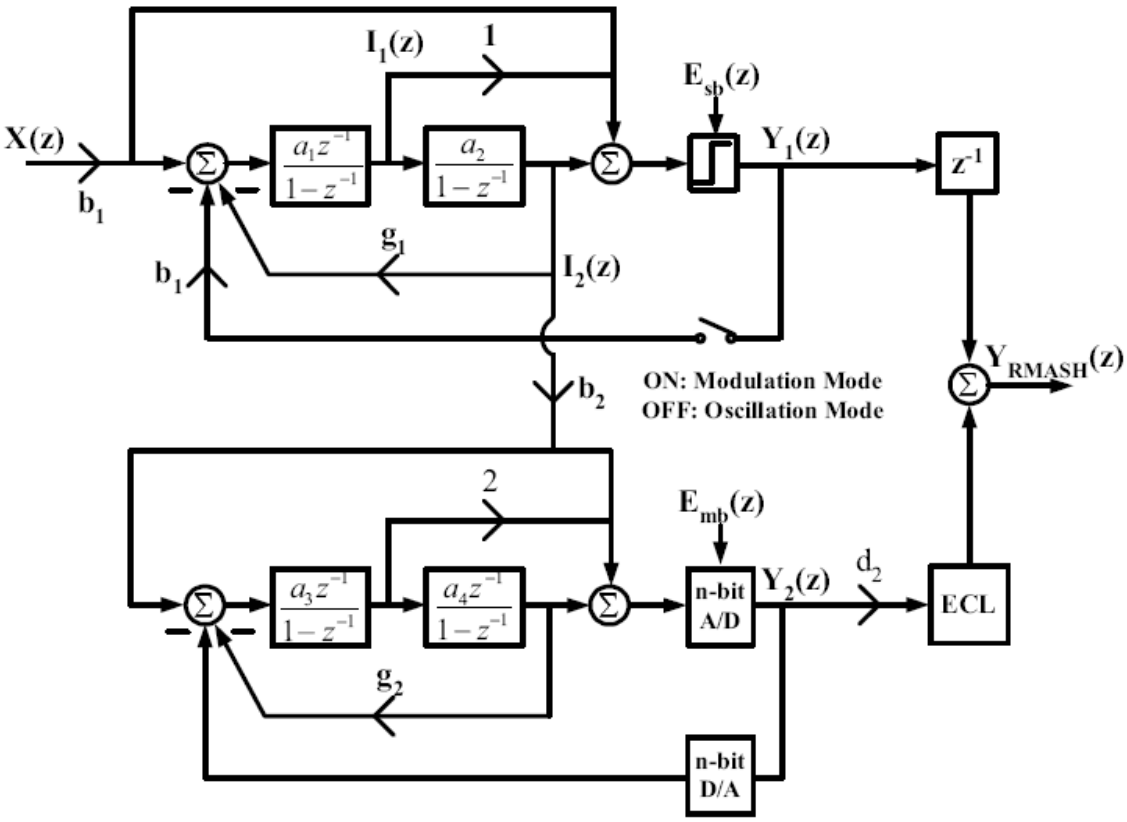

Figure 4.10: The Block diagram of the proposed RMASH 2-2 architecture

In the modulation mode, the RMASH 2-2 has the same behavior as the traditional MASH 2-2 and its output can be expressed as follow

$$Y_{RMASH,mod}(z) = z^{-1}X(z) + d_1 ECL(z) \cdot NTF_{CIFF}(z)E_{mb}(z), \tag{4.13}$$

where $ECL(z) = 1 - (2 - r_{CRFF})z^{-1} + z^{-2}$ and $d_1 = 1/a_1a_2a_3a_4b_1b_2$. In the expression of $ECL(z)$, r_{CRFF} is the resonator gain; it is equal to $a_1a_2g_1$. According to paper [18], the pairs of complex-conjugate zeros of NTF can be used to suppress the in-band quantization noise and hence improves SNR. However, the improvement relies on perfect matching between the numerator of NTF_{CRFF} and $ECL(z)$. When mismatch occurs, the single-bit quantization noise leaks to modulator output and consequently degrades the modulator performance. To avoid the leakage quantization noise, we utilize the oscillation of the HQCRFF structure.

When the first stage operates in the oscillation mode, the first stage lose the capability of error tracking and noise shaping; that is, the virtual switch on the feedback path shown in Figure 4.10 is equivalently open, i.e. out of function. Hereby, the single-bit quantization noise $E_{sb}(z)$ is blocked and thus the matching between $NTF_1(z)$ and $ECL(z)$ is not required. Therefore, when the first stage oscillates, the mismatch between NTF_1 and ECL does not

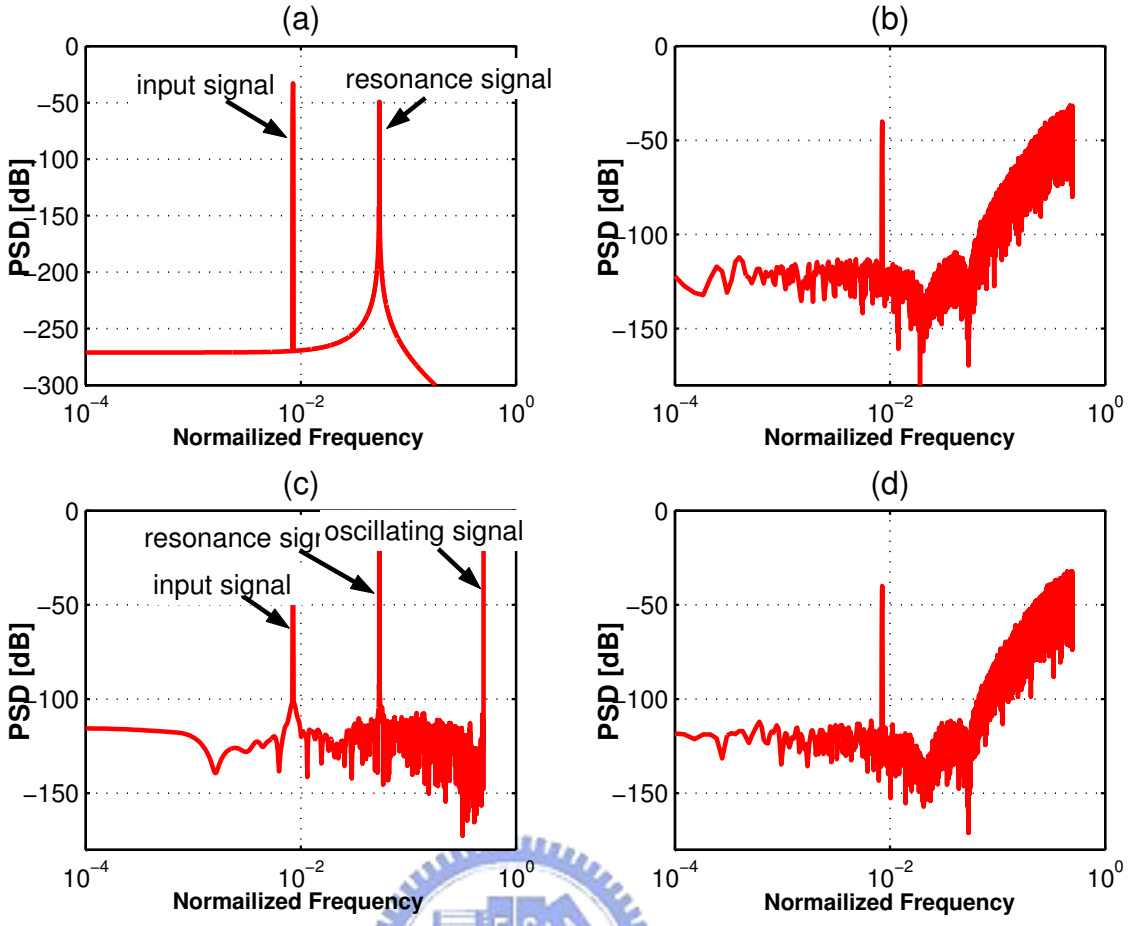

Figure 4.11: (a)and (b) are spectra of $I(z)$ and $Y(z)$ of Figure 4.2, respectively. (c) and (d) are spectra of $I_2(z)$ and $Y_{RMASH}(z)$ of Figure 4.10, respectively. The input amplitude is equal to -40dBV.

become a problem to the output and the pole error and gain error of the integrator do not result in the leakage noise. Figure 4.11 demonstrates the signal spectra of architectures in Figure 4.10 when the input amplitude is -40dBV.

As seen in Figure 4.11, in oscillation mode, the $I_2(z)$ of RMASH 2-2 has the similar spectrum to $I(z)$ of Figure 4.2. Note that there exists an additional tone at $f_s/2$. The additional tone is a period-2 (+1 -1 +1 -1...) PWM signal and it is caused from the nonlinear oscillation of HQCRFF [62]. Thereby, in the oscillation mode, the signal $I_2(z)$ can be approximately expressed as Equation (4.14).

$$I_{2,osc}(z) \approx \frac{a_1 a_2 b_1 z^{-1}}{1-(2-r_{CRFF})z^{-1}+z^{-2}} X(z) + O(z), \tag{4.14}$$

where $O(z)$ represents a period-2 (+1 -1 +1 -1...) oscillating signal at $f_s/2$. Finally, the

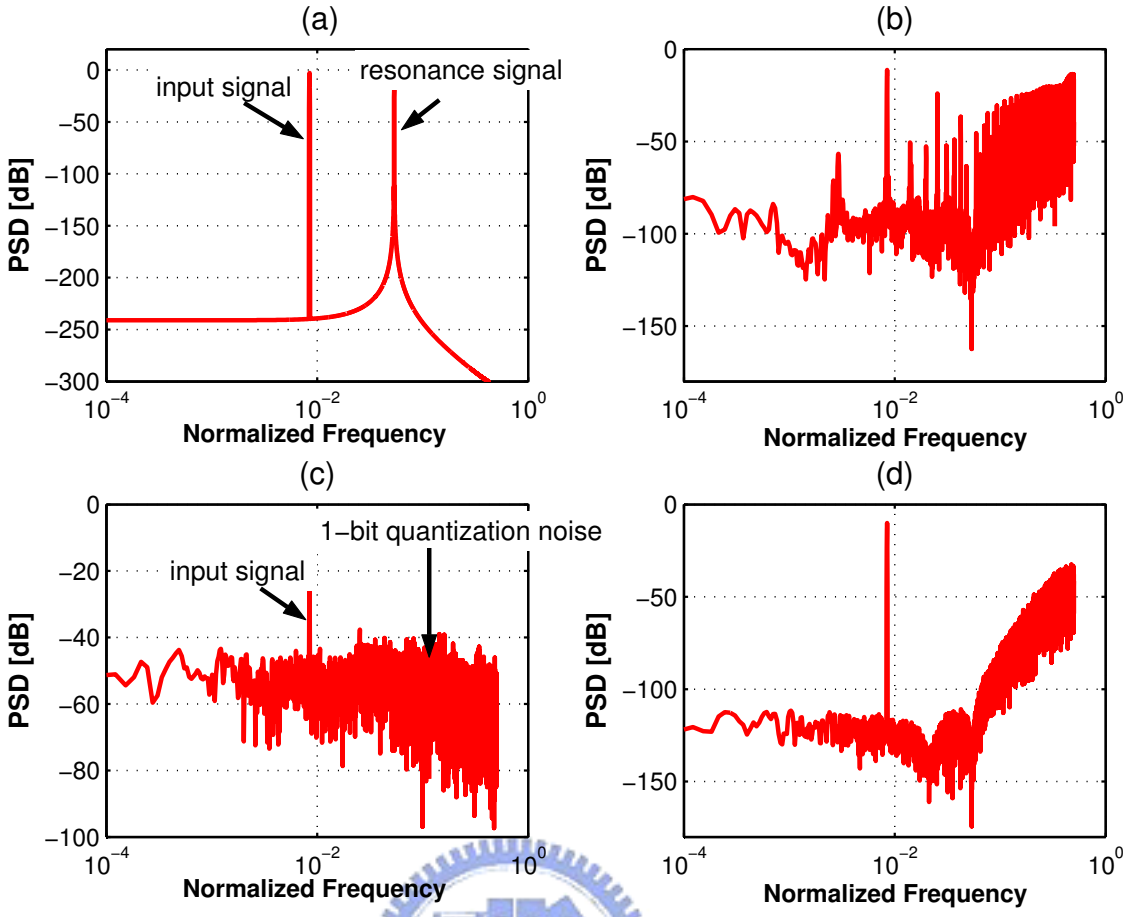

Figure 4.12: (a)and (b) are spectra of $I(z)$ and $Y(z)$ of Figure 4.2(a), respectively. (c) and (d) are spectra of $I_2(z)$ and $Y_{RMASH}(z)$ of Figure 4.2(b), respectively. The input amplitude is equal to -10dBV.

output in the oscillation mode becomes the expression shown in Equation (4.15).

$$Y_{RMASH,osc}(z) = z^{-1}X(z) + d_1 ECL(z)\cdot [O(z) + NTF_{CIFF}(z)E_{mb}(z)] \tag{4.15}$$

Comparing with Equation (4.13), the output in the oscillation mode has an additional term $d_1 ECL(z)O(z)$. This term can be ignored since the O(z) will be filtered out by digital decimation filter. Therefore, Equation (4.15) can be further modified as:

$$Y_{RMASH,osc}(z) = z^{-1}X(z) + d_1 ECL(z) \cdot NTF_{CIFF}(z)E_{mb}(z). \tag{4.16}$$

Note that the Equation (4.16) is exactly the same as Equation (4.13). Hence, the nonlinear oscillation does not make the RMASH 2-2 out of order, but free of the leakage noise. Now, let us analysis the performance when the input amplitude is large (say, -10 dBV). As mentioned in Section 4.2, with large input amplitude, the conceptual architecture of Figure 4.2 may

suffer from the saturation of the second stage. The saturation will cause harmonic distortion. Figure 4.12(b) illustrates the severe harmonic distortions for the input amplitude of -10 dBV. In RMASH 2-2, as seen in Figure 4.12(d), the harmonic distortions are disappeared because the RMASH 2-2 operates in the modulation mode for large input amplitude.

Here we provide a design methodology of the proposed RMASH 2-2.

1.) Given the system specifications; they are DR, OSR, modulator order, and number of level of multi-bit quantizer.

2.) Set the loop resonator gains according to the following equation

$$r_{CRFF} = \left(\frac{\pi}{OSR}\right)^2, \quad r_{CIFF} = \frac{1}{3}\left(\frac{\pi}{OSR}\right)^2. \tag{4.17}$$

3.) Adjust the integrator gains to avoid the saturation of signal swing.

4.) Find out the threshold voltage based on Equation (4.17).

5.) Simulate and check the oscillation mode of the resulting RMASH 2-2 by using MATLAB and SIMULINK.

4.4 System-Level Simulations

The proposed HQCRFF-based MASH 2-2 and MASH 2-0 architectures have been simulated in SIMULINK and MATLAB. The modulators were designed with a sampling rate of 61.44 MHz, a fixed OSR of 8, yielding a signal bandwidth of 3.84 MHz for broadband application such as Wideband Code-Division Multiple-Access (WCDMA).

4.4.1 RMASH 2-0

The single-bit quantizer is used in first stage of the proposed MASH 2-0 modulator because of the excellent linearity of feedback DAC. The second stage is a 10-bit quantizer (pipeline ADC architecture) with reduce-speed-factor (RSF) of 2, say, 30.72 MHz. To avoid the overload of the integrators, the scaling gains are set to a1=a2=0.5 and g1=0.4112. The same circuit specifications are applied to the traditional MASH 2-0 with RSR technique [60] for comparison. The output spectra of the both MASH 2-0 structures were computed by 32768-point FFTs, and shown in Figure 4.13.

Thanks to the in-band zeros of the proposed structure, the peak SNDR is slightly im-

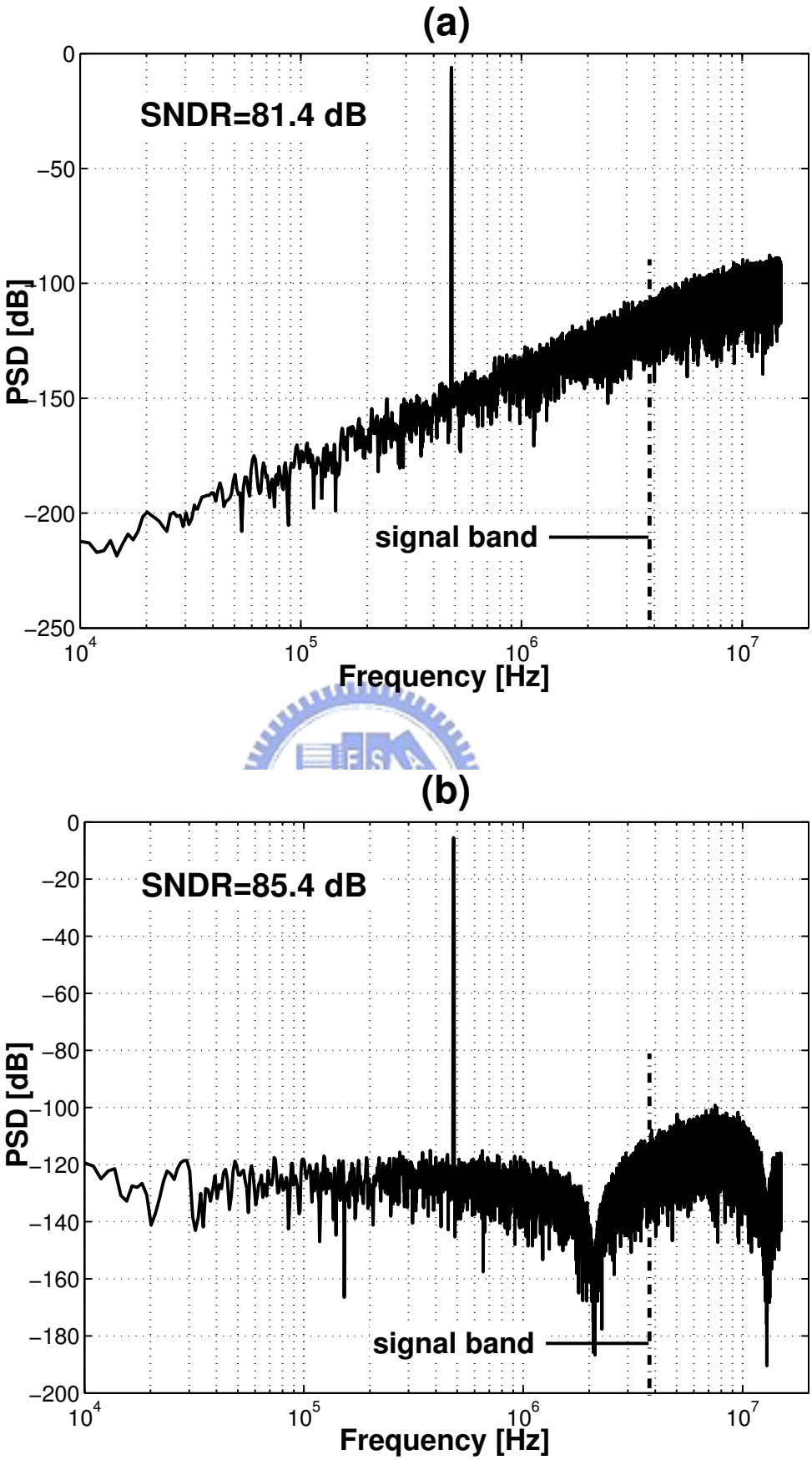

Figure 4.13: The output spectra of the MASH 2-0 architectures using: (a) traditional RSR technique [60] and (b) improved RSR technique [61].

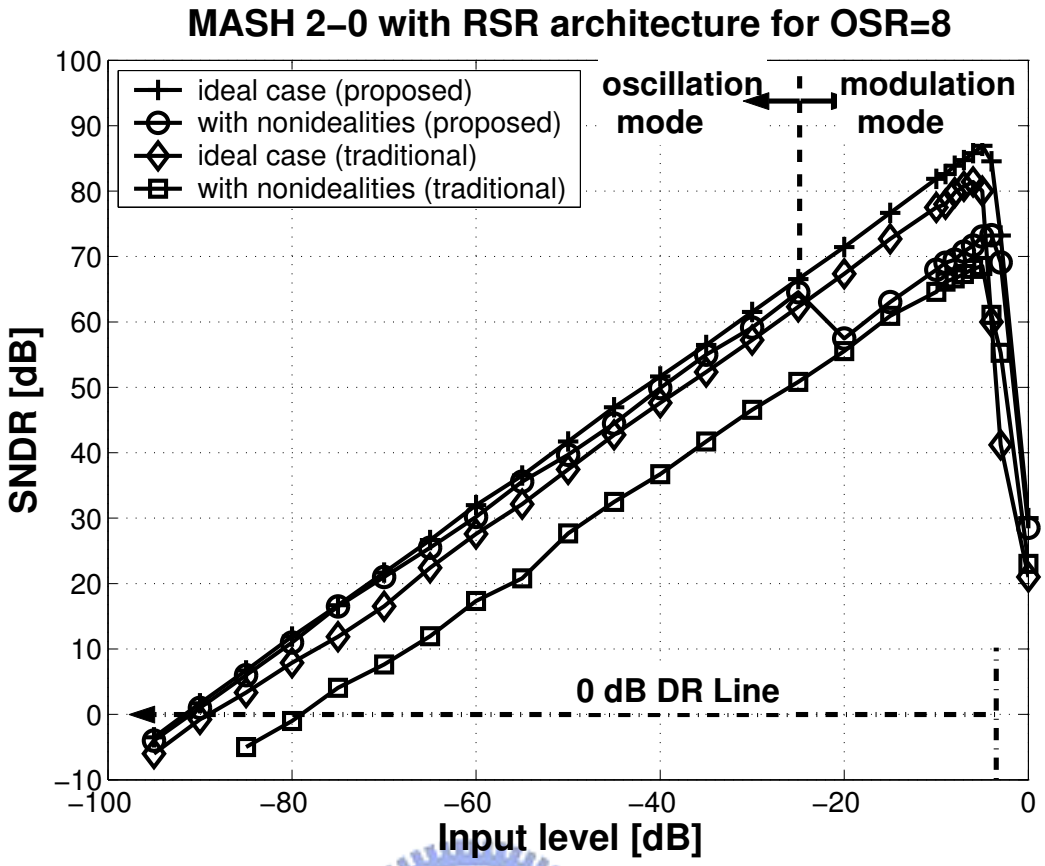

Figure 4.14: The SNDR as a function of input level for both traditional and proposed MASH 2-0 with RSR technique.

proved compared to traditional one. To consider the circuit nonidealities, we use a simple but effective model [43] for the integrators. The integrator model models a nonlinear op-amp function with the maximum gain of 60 dB, the slew-rate of 150 V/μs, the gain-bandwidth of 300 MHz, and the output swing of $\pm$1V. The capacitor mismatch is set to 0.2%. The SNDRs as functions of input level for both traditional and proposed MASH 2-0 with RSR technique are shown in Figure 4.14. As shown in Figure 4.14, compared to traditional approach, the proposed one in oscillation mode is insensitive to circuit nonidealities.

4.4.2 RMASH 2-2

The single-bit and four-bit quantizers are used for the first- and second-stage of RMASH 2-2, respectively. The scaling loop gains are listed in Table 4.1. The finite opamp dc gain, capacitor mismatch and four-bit DAC mismatch are set to 60 dB, 0.2% and 0.5%FS, respectively. In order to evaluate the performance, such as the SNDR or DR, we have to use the single sinusoid to simulate the proposed multi-bit RMASH 2-2. According to previous analysis, however, the utility of nonlinear oscillation in the proposed architecture

Table 4.1: Coefficients of RMASH 2-2 for OSR=8

Coefficients	Values	Coefficients	Values
a1	0.5	b1	1
a2	0.5	b2	2
a3	1	g1	0.5
a4	1	g2	0.025

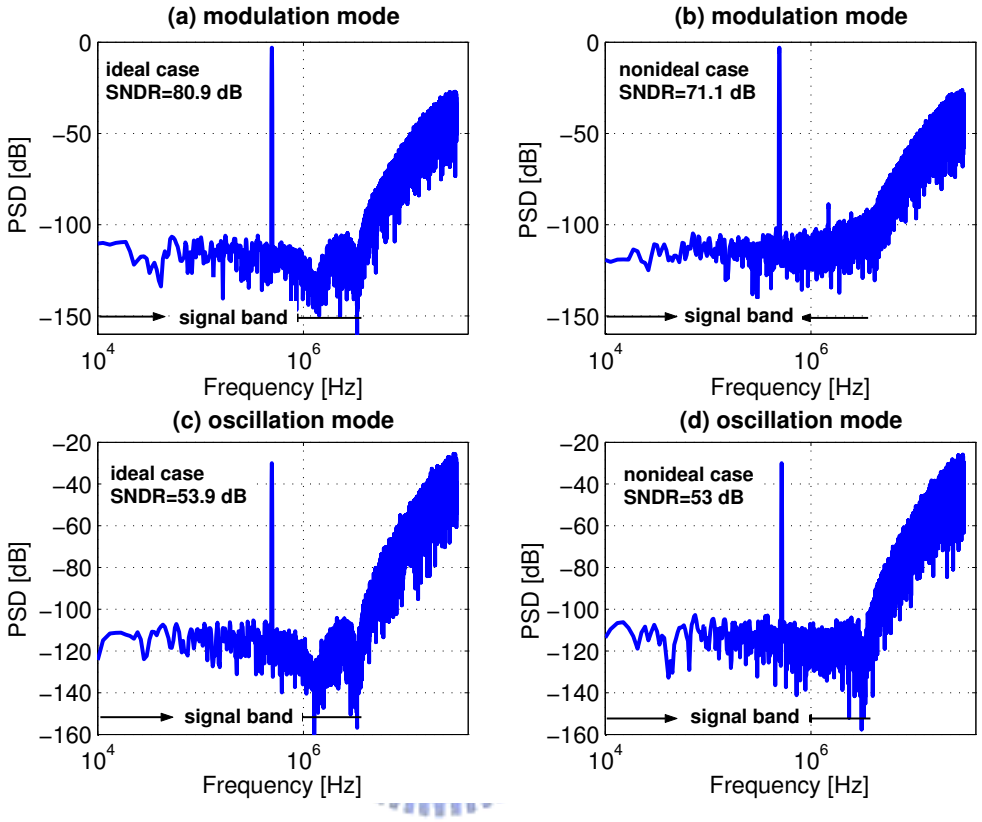

Figure 4.15: The output spectra of the proposed MASH 2-2 (a) with ideal case, (b) with circuit nonidealities in modulation mode, (c) with ideal case, and (d) with circuit nonidealities in oscillation mode.

is not limited to a sinusoidal signal. The output spectra in modulation (input level= -3dB) and oscillation modes (input level= -30dB) are shown in Figure 4.15. As seen in Figure 4.15, the leakage noise is disappeared when RMASH 2-2 is in the oscillation mode and the 0.5% FS mismatch of four-bit DAC only results in 1 dB SNDR degradation. To verify the function of AD conversion, a two-tone signal is applied to the proposed RMASH 2-2 and the output of RMASH 2-2 following a decimation filter is observed. Figure 4.16 shows the simulation results. Accordingly, the two-tone input signal makes RMASH 2-2 switch between oscillation and modulation and decimated output signal has a constant delay compared with input signal. This results mean that the switch between oscillation and modulation does not make the analog-to-digital conversion of RMASH 2-2 out of function.

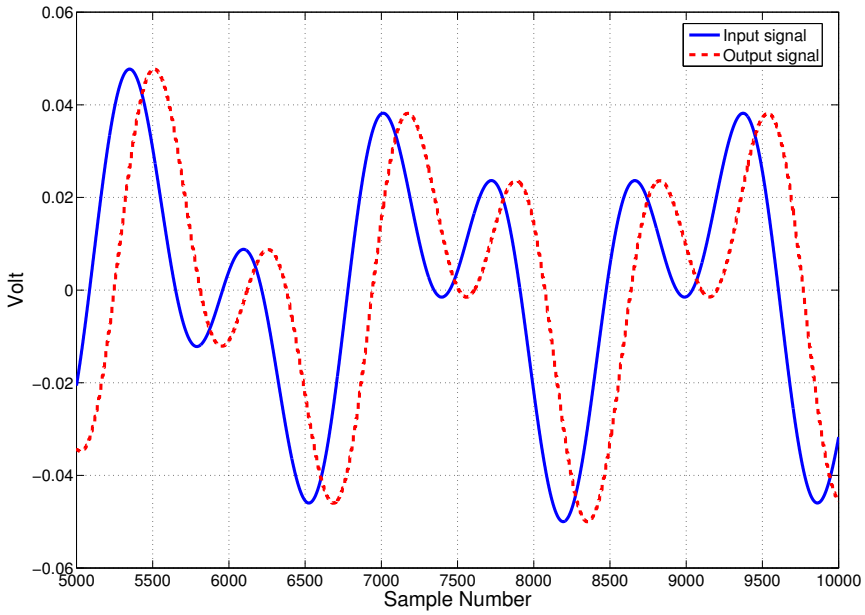

Figure 4.16: The two-tone input signal and output of the RMASH 2-2 following a decimation filter.

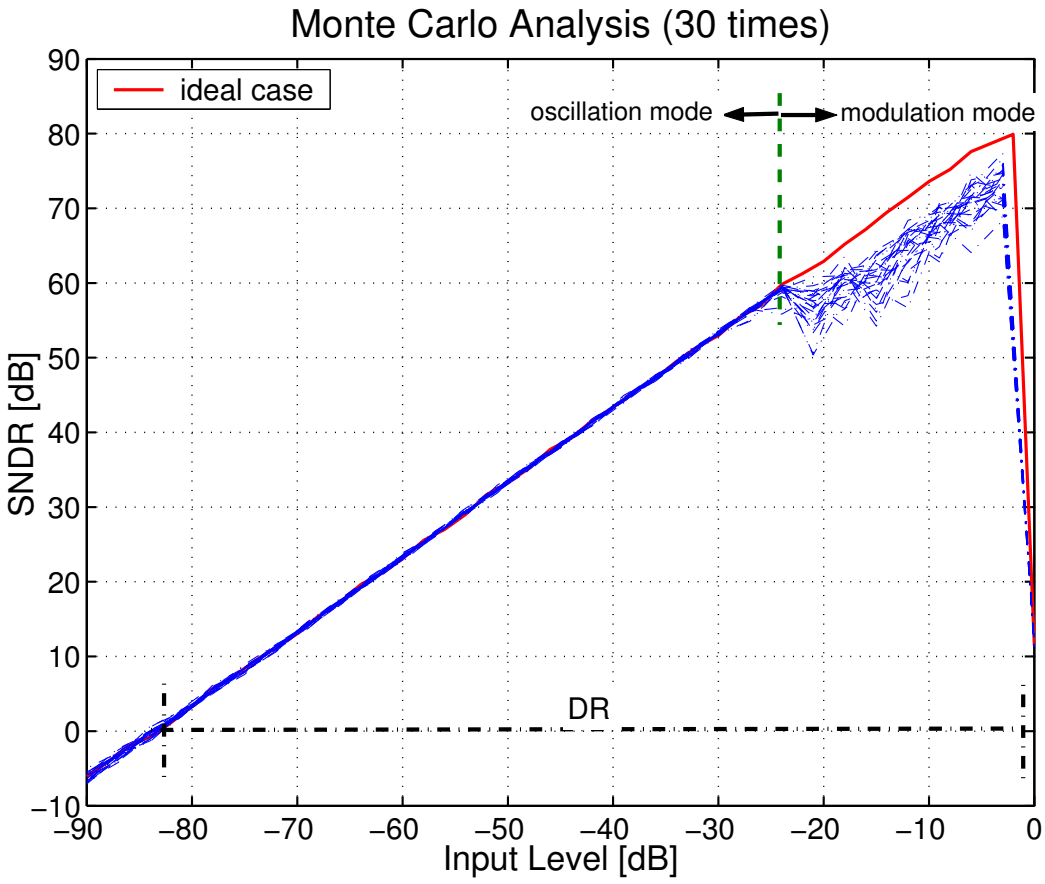

Figure 4.17: The SNDR against input level in the proposed MASH 2-2 with Monte Carlo analysis.

Figure 4.17 illustrates the SNDR against input level for the proposed RMASH 2-2 with Monte Carlo analysis of 30 repetitions. Based on Figure 4.17, because of the oscillation operation, the DR of RMASH 2-2 is about 84dB and the peak SNDR of RMASH 2-2 is about 71dB. Accordingly, although the RMASH 2-2 has high DR inherently its achievable peak SNDR is still degraded by leakage noise in that the first stage is operating in the modulation mode. Thanks to the introduced in-band zeros, the in-band quantization noise is effectively suppressed; hence, the peaks SNDR is still efficient for moderate resolution (say 72dB). The result is comparable to the traditional MASH 2-2 or MASH 2-1-1. Note that the traditional MASH 2-2 and MASH 2-1-1 with the same circuit specifications and OSR have the peak SNDR approximates 61dB and 68dB, respectively [63].

4.5 Circuit Implementation of RMASH 2-2

This section presents the transistor-level design of the critical building blocks for a 13-bit RMASH 2-2 with the sampling frequency of 60 MHz and the signal bandwidth of 3.84 MHz, which results in an OSR of 8. The first stage is a HQCRFF 1-bit modulator while the second stage is a LQCIFF 4-bit modulator. The RMASH 2-2 was implemented in TSMC 0.25-μm, 1P5M, CMOS technology and dissipated 55mW form a 2.5V supply voltage.

4.5.1 HQCRFF 1-bit Modulator

As shown in Figure 4.10, the first stage of proposed RMASH 2-2 is HQCRFF 1-bit modulator and its coefficients are listed in Table 4.1. According to above analysis, the leakage quantization noise and oscillation mode operation both depend on HQCRFF 1-bit modulator. Therefore much effort should be paid for it. First, the same OTA shown in Figure 3.25 is used to implement the integrators of HQCRFF 1-bit modulator. The OTA accomplishes a dc gain of 75 dB and achieves a GBW of 300MHz with a capacitive loading of 5 pF. The OTA including gain-boosting and biasing circuits, dissipates 15 mW from a 2.5-V supply voltage. Figure 4.18 illustrates the SC circuit diagram of the HQCRFF 1-bit Modulator. Since the dynamic range of the modulator is targeted at 84-dB at the sampling rate of 60 MHz, the sampling capacitor is chosen to be 1 pF and, accordingly, the integrating and resonator feedback capacitors are 2 pF and 0.5 pF, respectively. The closed-loop bandwidth of front-end integrator is about 255MHz, which is larger than three times the sampling frequency. Because the feedback gain of the 1-bit DAC is equal to one,

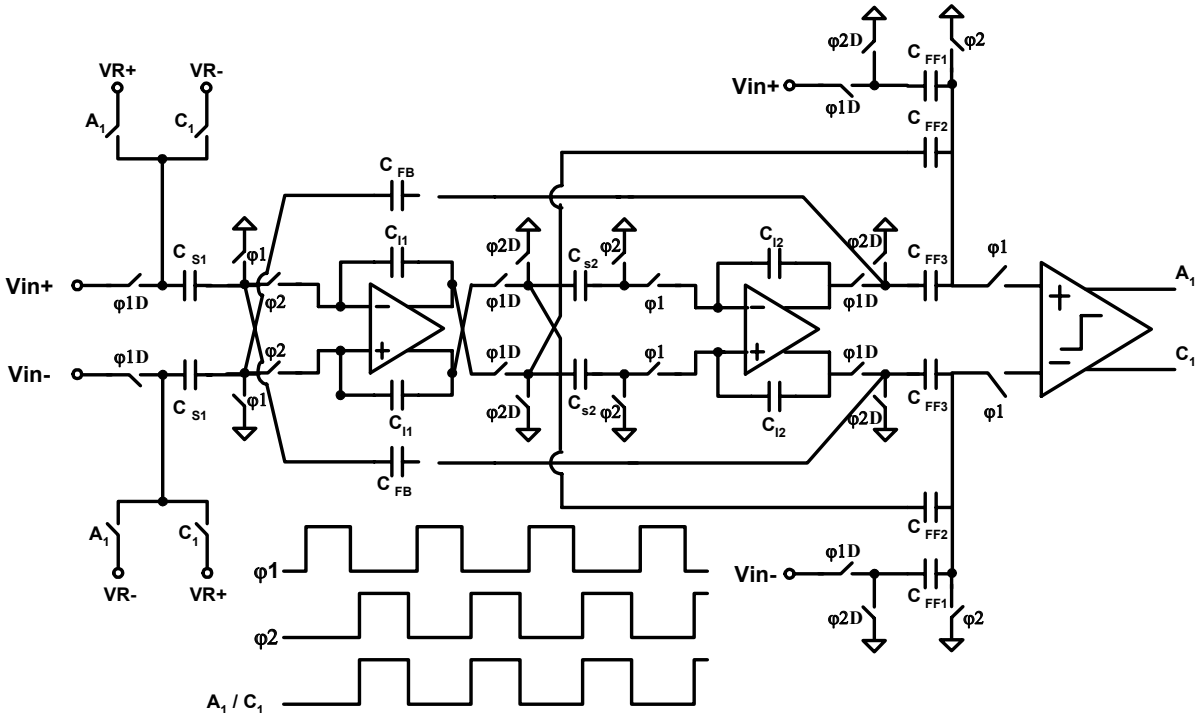

Figure 4.18: Circuit implementation of HQCRFF 1-bit modulator.

we can use the share-capacitor switching technique to eliminate coefficient mismatch. The share-capacitor switching technique is to have the input sampling and feedback DAC share a common sampling capacitor C_{S1} [46]. The summing circuit in front of the quantizer is implemented by using a passive SC network to avoid the use of additional OTA and save the power dissipation. The summed signal can be expressed as

$$V_S(z) = \frac{C_{FF1}V_{in}(z) + C_{FF2}Int1(z) + C_{FF3}Int2(z)}{C_{FF1} + C_{FF2} + C_{FF3}}, \tag{4.18}$$

where C_{FF1}, C_{FF2}, and C_{FF3} are the capacitors for feedforward gains. Here we set the values of C_{FF1}, C_{FF2}, and C_{FF3} to be 0.1 pF because these feedforward gains are equal and not critical. Since the key to improving the DR of RMASH 2-2 is the operation of oscillation mode, it is important to observe the behavior of HQCRFF 1-bit modulator in transistor-level simulations. With a 290 kHz sinusoid, Figures 4.19 and 4.20 show the integrator output voltages and the 1-bit quantizer outputs of HQCRFF 1-bit modulator, respectively. Obviously, the small input signal level make the HQCRFF 1-bit oscillate compared with large one. Also, the output spectra of HQCRFF for Figures 4.19 and 4.20 are show in Figure 4.21. Accordingly, this transistor-level simulation results agree the pervious system-level simulation results well.

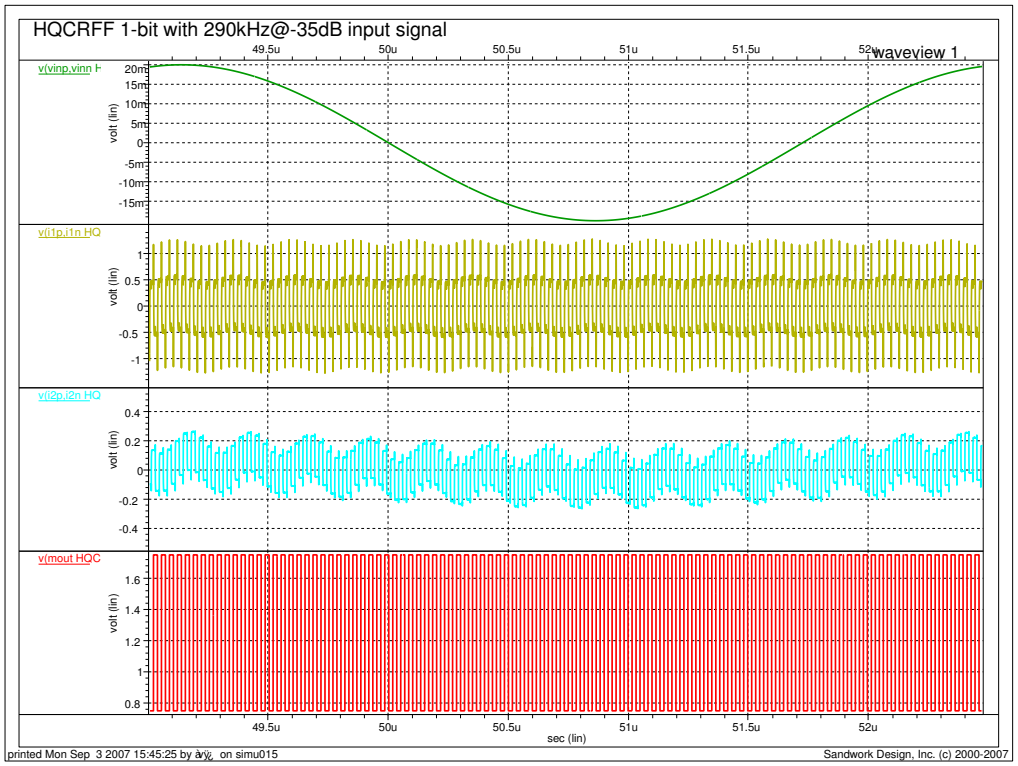

Figure 4.19: The -35 dBV input signal, integrator output voltages, and 1-bit quantizer output of HQCRFF 1-bit modulator in oscillation mode.

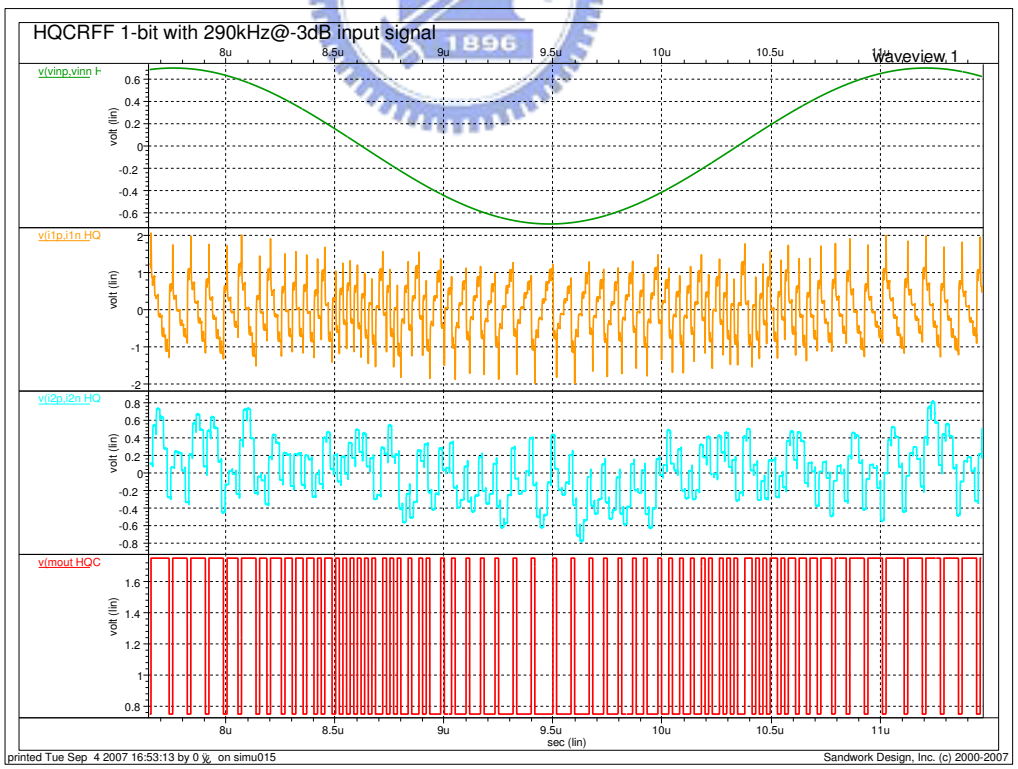

Figure 4.20: The -3 dBV input signal, integrator output voltages, and 1-bit quantizer output of HQCRFF 1-bit modulator in modulation mode.

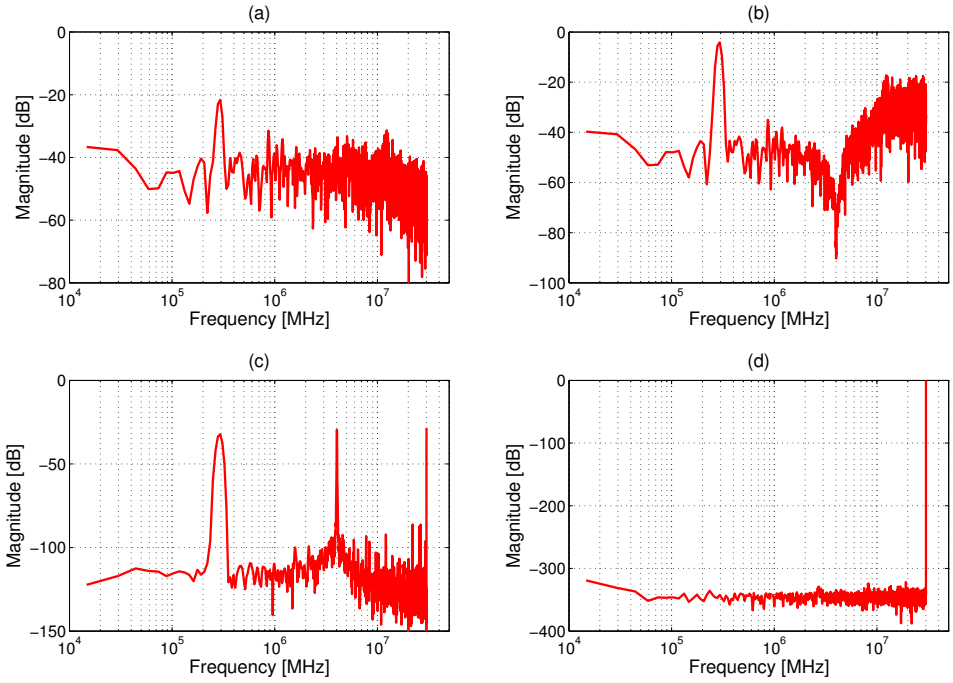

Figure 4.21: (a) and (b) The SPICE output spectrum of second integrator and 1-bit quantizer of HQCRFF 1-bit modulator with -3dBV input level; (c) and (d) The SPICE output spectrum of second integrator and 1-bit quantizer of HQCRFF 1-bit modulator with -35dBV input level.

4.5.2 LQCIFF 4-bit Modulator

As shown in Figure 4.10, the second stage of proposed RMASH 2-2 is LQCRFF 4-bit modulator and its coefficients are listed in Table 4.1. According to papers [22, 40, 51] and the analysis of subsection 3.1.1, the feedforward path of LQCIFF multi-bit modulator not only reduces signal-dependent harmonic distortion but also suppresses the output swing of integrator. This largely relaxes the circuit specifications of OTA, thus reducing the power dissipation. The similar OTA as shown in Figure 3.25 without gain-boosting is used for the integrators of the LQCIFF and dissipates only 7 mW for a 2.5-V supply voltage. The detail schematic of the LQCIFF 4-bit modulator is shown in Figure 4.22 where the first integrator stage incorporates the 4-bit feedback DAC circuits at the input sampling networks. The sampling capacitances are composed of seventeen small unit capacitances, one extra unit capacitance for level shift. The unit capacitance is 0.1pF. The mismatch of the feedback 4-bit DAC can be suppressed due to the noise shaping of the second-order high-pass digital cancellation filter, ECL(z), which avoids the use of additional DEM or DWA circuits. The 4-bit quantizer is implemented with a flash architecture as shown in Figure 4.23. This 4-bit quantizer includes a resistor string for generating reference voltage for switched-capacitor

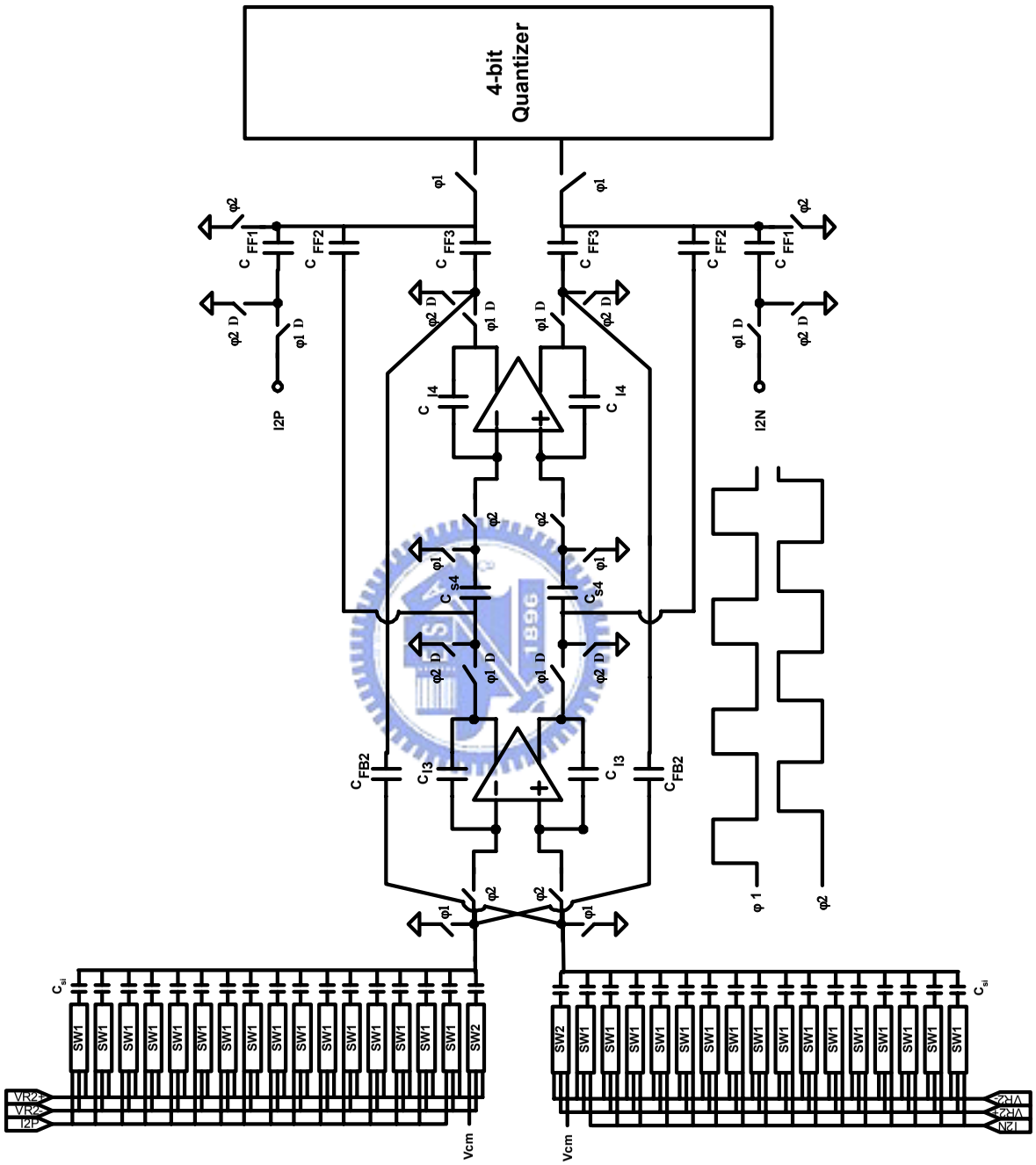

Figure 4.22: Circuit implementation of 4-bit LQCIFF modulator.

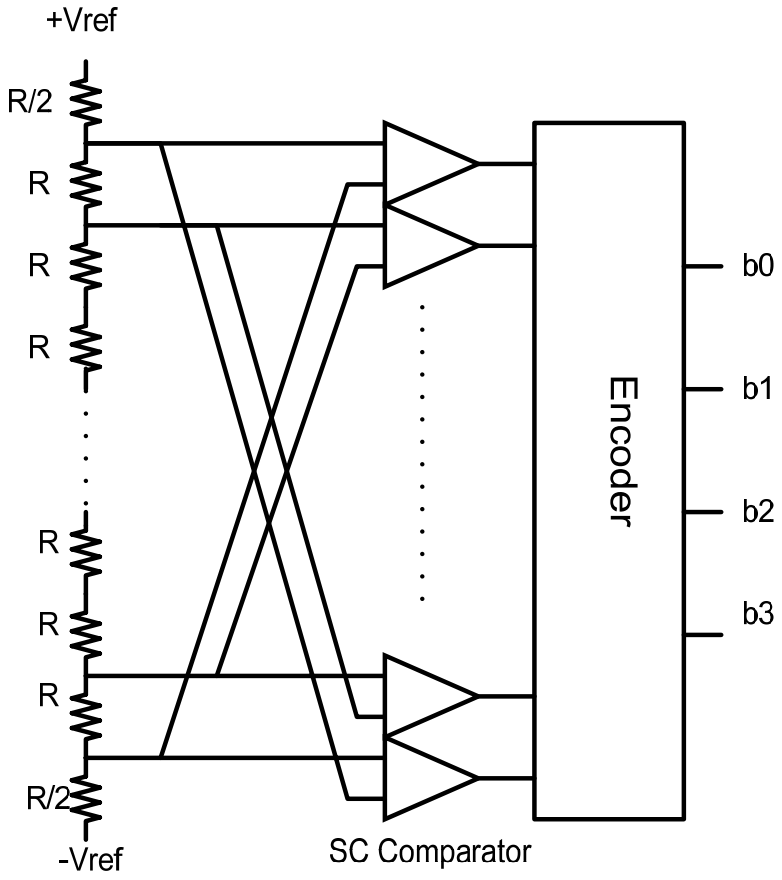

Figure 4.23: The circuit schematic of 4-bit quantizer.

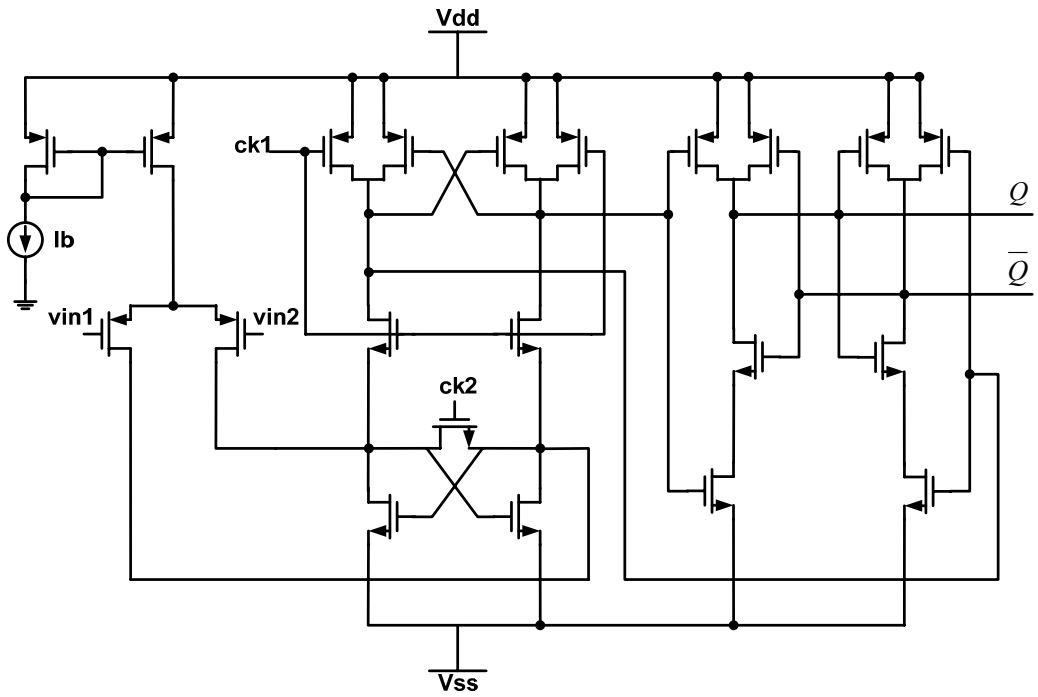

Figure 4.24: The circuit schematic of comparator.

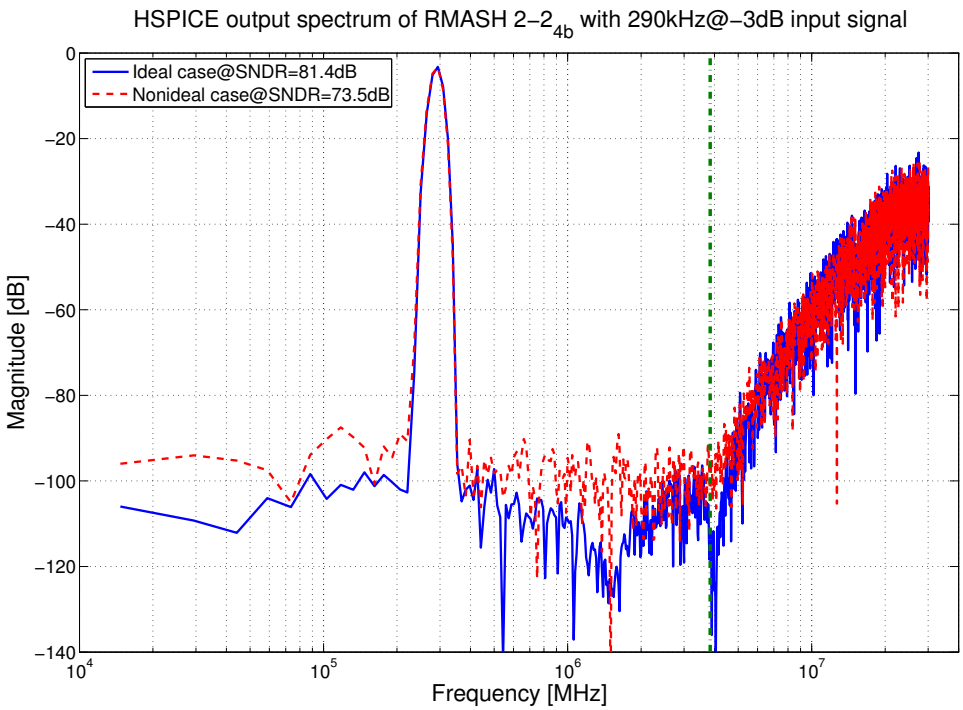

Figure 4.25: The output spectrum of RMASH 2-2 with 290kHz@-3dBV input signal.

(SC) comparators, sixteen SC comparators for quantizing the input signal and a thermal-meter to binary encoder. The positive and negative reference voltages (+Vref and -Vref) are 1.5V and 1V, respectively. A unit resistance of 500Ω is used. Due to the noise-shaping characteristics of the SDM, the 4-bit quantizer design can be quite relaxed. The core circuit of the SC comparator is shown in Figure 4.24. This comparator includes a pre-amplifier stage and a latch stage. The bias current for the comparator is 30μA. When ck2 is high, the differential input are compared and the comparator is in a reset mode. Then when ck2 is low and ck1 is high, the comparator enter a regeneration (latch) mode. The comparator output is stored in the output of the NAND-gate latch.

4.5.3 Simulation Results

The RMASH 2-2 is designed for a sampling rate of 61.5 MHz and a fixed OSR of 8; so, the signal bandwidth is 3.84 MHz. It is implemented in TSMC 0.25-μm 1P5M CMOS technology and dissipates 55 mW with a 2.5-V supply voltage. In order to evaluate the performance of RMASH 2-2 in both modulation mode and oscillation mode, the 0.2% capacitor mismatch is applied to each SC integrator. Figures 4.25 and 4.26 show the output spectrum of RMASH 2-2 with -3dBV and -35dBV input levels, respectively.

According to Figure 4.25, the large input level makes the first stage of RMASH 2-2,

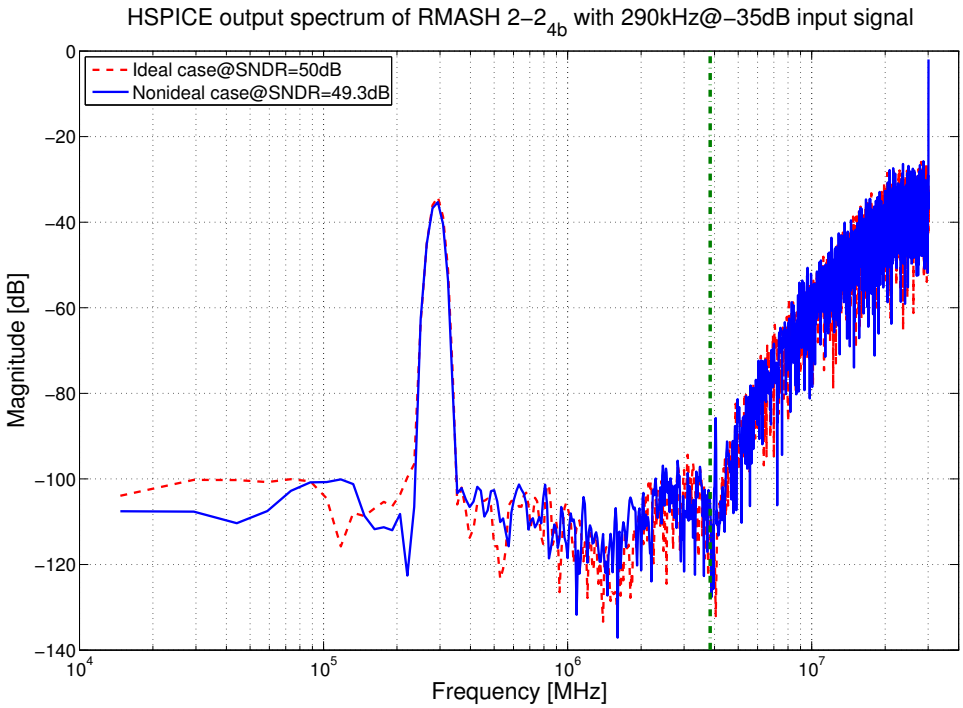

Figure 4.26: The output spectrum of RMASH 2-2 with 290kHz@-35dBV input signal.

Table 4.2: Performance summary of RMASH 2-2.

Architecture	RMASH 2-2
Sampling Frequency	61.5 MHz
Signal Bandwidth	3.84 MHz
Peak SNDR	73.5 dB
DR	82 dB
Power Dissipation	55 mW
FOM	0.7 pJ/conv
Technology	0.25μm

HQCRFF 1-bit modulator, into the normal modulation mode and hence the 1-bit leakage quantization noise degrades the performance of RMASH 2-2. In the contrary, the samll input level as shown in Figure 4.26 makes the HQCRFF 1-bit modulator into the oscillation mode and hence the performance can improve due to the absence of 1-bit leakage quantization noise. Figure 4.27 shows that the RMASH 2-2 can achieve a dynamic range of 82 dB adnd a peak SNDR of 78.5 dB for a 3.84 MHz signal band. Table 4.2 lists the performance summary of RMASH 2-2. Based on Equation (3.37), the RMASH 2-2 achieves a FOM of 0.7 pJ/conv, which is lower than the existed wideband SC $\Sigma\Delta$ modulator.

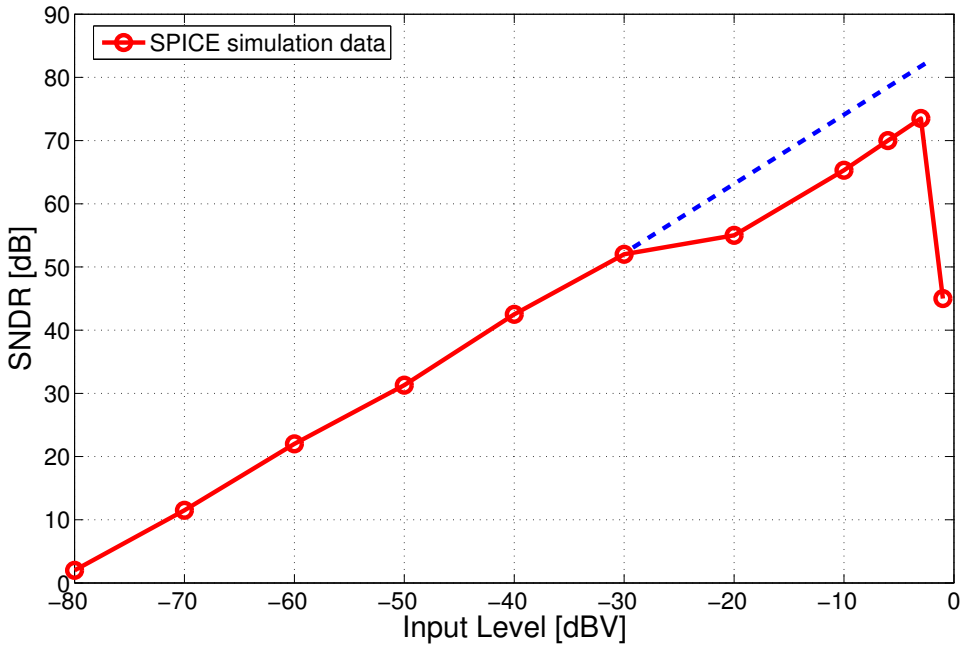

Figure 4.27: Plots of SPICE simulated SNDR versus input signal level of RMSAH 2-2.

4.6 Summary

This paper presents two resonator-based MASH architectures which are suitable for wide-band applications. The main contributions of the proposed HQCRFF-based MASH architectures are: 1) The proposed MASH architectures introduce the complex-conjugate zeros to suppress the in-band quantization noise and hence enhance the peak SNDR of the A/D converters. 2) The use of HQCRFF-based single-bit structure in the first stage can effectively make the modulator insensitive to the circuit nonidealities and hence improve DR. Note that this improvement is intrinsic in the proposed architectures. Unlike the other published MASH architectures, the proposed modulator does not need calibration techniques to compensate the circuit mismatch. This makes the implementation robust and reduces the circuit complexity. 3) The other MASH architectures can take advantage of the intrinsic DR improvement when using the HQCRFF-based single-bit structure in the first stage. 4) Although the peak SNDR of the proposed MASH architectures is still sensitive to circuit imperfections, considering reasonable circuit nonidealities, the moderate SNDR (say, 72 dB) can be still achieved.

Chapter 5

Conclusion

The increasing demand for broadband Internet access and the growing use of digital processing, motivates the implementation of communications standards employing sophisticated decoding methods, capable of achieving high data rates using existing communications media. However, the trend toward increased data rates and digital signal processing increases the dynamic range (DR) and the bandwidth needed at the ADC interface. Furthermore, the power dissipation and circuit complexity are the important issues for consumer electronic products.

5.1 Thesis Contributions

In this thesis, the characteristic and the limitation of the existing three popular architectures of $\Sigma\Delta$ ADCs have been discussed. The continuous-time $\Sigma\Delta$ ADC has the features of high sampling frequency and low power dissipation for broadband applications. However, the large variation of RC time constant, the high sensitivity to jitter noise, and the poor immunity of loop excess delay usually limits the achievable resolution (say, $\leq$12 bits). The discrete-time single-loop multi-bit $\Sigma\Delta$ ADC has the features of high resolution and good immunity of circuit nonidealities for broadband applications. However, the nonlinearity of multi-bit feedback DAC and the instability of high-order loopfilter limits the achievable resolution. Several kinds of digital algorithms have been proposed to improve the linearity of multi-bit feedback DAC. Although they work well, the additional power dissipation and digital circuit hardware are required, thus may lower the conversion efficiency (say, figure of merit). In order to avoid the instability of high-order loopfilter, additional algorithm is required to initialize some critical node, e.g. integrator outputs. The discrete-time cascaded

$\Sigma\Delta$ ADC has the features of high resolution and good stability of high-order loopfilter for broadband applications. However, the high sensitivity to leakage quantization noise caused by finite OTA gain and capacitor mismatch usually limits the achievable resolution. Several kinds of digital processing algorithms have been proposed to calibrate the error correction logic (ECL), which the leakage quantization noise can be eliminated. Although they work well, the additional power dissipation and digital circuit hardware are required, thus may lower the conversion efficiency. This work is dedicated to the design of high-order cascaded $\Sigma\Delta$ ADC and two architecture were, then, proposed to achieve high DR, low power, and low cost for broadband applications.

The first cascaded architecture is a 2-1-1 fourth-order modulator, which is referred as RMASH 2-1-$1_{1.5b}$. This modulator targets on the newly asymmetric digital subscriber line (ADSL2+) standard and can achieve 14-bit DR and 2.2 MHz signal bandwidth. To reduce the power dissipation and save silicon area , the desired DR is achieved using three architectural approaches. The first one is the use of 1.5-bit quantization in each stage, which can enhance the DR without additional linearized techniques of feedback DAC. The leakage quantization noise is also reduced compared with multi-bit approach, which relaxes the specifications of OTA dc gain and capacitor mismatch. The second one adds the in-band zeros to the NTF to enhance the DR by suppressing the in-band quantization noise. This can be achieved by adding the local feedback path around two integrators (say, a resonator) in the first stage. Since the feedback coefficient is very small, the leakage noise may increase due to the capacitor mismatch. By proper scaling coefficients, the capacitor ratio can be modified to provide better capacitor match. The third one is the use of two pairs of reference voltages; the high one for the first stage to enhances signal dynamic range and the low one for the other stages to reduce quantization noise. The optimal circuit specifications are extracted by system-level simulation. A digital decimation filter is designed to downsample the conversion rate of modulator digital outputs into the Nyquist-rate. This ADC is implemented in a 0.25 technology. The measured DR, peak SNR and peak SNDR are 86 dB, 84 dB, and 78 dB respectively and consumes 65mW and 120mW for core modulator and deciamtion filter from 2.5V supply voltage. The figure of merit (FOM) of the core modulator and overall ADC are 0.77pJ and 1.5pJ respectively which was lower than the published switched-capacitor (SC) modulator with this order of resolution and bandwidth.

The second cascaded architecture is a resonator-based modulator, which is referred as RMASH. This kind of modulator is based on two resonator topologies, high-Q cascade-

of-resonator-with-feedforward (HQCRFF) and low-Q cascade-of-integrator-with-feedforward (LQCIFF). With HOCRFF loopfilter and 1-bit quantizer, the modulator can operate in an interesting mode, called as oscillation mode. This oscillation mode is caused by the high-Q resonant gain of loopfilter and the 1-bit modulator outputs the periodic +1,-1 bit streams. Actually, the presence of oscillation mode mainly depend on the amplitude of the input signal. In other words, there may exist a threshold voltage to make HOCRFF-based 1-bit modulator oscillate. According to the theoretical analysis and simulation result, the lower the OSR the higher the threshold voltage. Once the modulator has this kind of situation, the modulator output is only the function of resonant signal. This makes the 1-bit quantization error free of the input signal. Since the leakage quantization noise of cascaded modulator is mainly caused by the imperfect cancellation of first-stage quantization error, this characteristic thus can be used to eliminate the leakage quantization noise. Two cascaded modulators, RMASH 2-0 and RMASH 2-2 are proposed by employing the HQCRFF 1-bit structure as the first stage. The second stage of RMASH 2-0 is a 10-bit pipelined ADC with an improved reduced-sample-rate (RSR) technique and the second stage of RMASH 2-2 is a second-order LQCIFF-based modulator with 4-bit quantizer. The RMASH 2-2 and RMASH 2-0 architectures have been simulated in SIMULINK and MATLAB. The modulators were designed with a sampling rate of 61.44 MHz, a fixed OSR of 8, yielding a signal bandwidth of 3.84 MHz for broadband applications. With an OTA dc gain of 60 dB and a capacitor mismatch of 0.1%, both modulators can achieve the DR over 84 dB. Comparing to traditional architecture with the same conditions, the DR approximately increases 24 dB. Although the peak SNDR of the both modulators are still sensitive to circuit imperfections, considering reasonable circuit nonidealities, the moderate SNDR (say, 72 dB) can be still achieved. The SPICE simulated DR and peak SNDR of RMASH 2-2 are 82 dB and 73.5 dB, respectively and consumes 55mW from 2.5V supply voltage. The FOM of the RMSAH 2-2 is 0.7pJ which was lower than the published switched-capacitor (SC) modulator with this order of resolution and bandwidth.

5.2 Future Work

Two cascaded $\Sigma\Delta$ modulators have been described for broadband applications. Based on the analysis, simulation, and experiment results, several interesting issues can be further explored.

The first one would be to further extend the signal bandwidth of RMASH 2-1-$1_{1.5b}$, which

can be achieved by further lowering the OSR. In order to compensate the DR loss due to lower OSR, the order of RMASH 2-1-$1_{1.5b}$ should be increase. Therefore, RMASH 2-2-$1_{1.5b}$ or RMASH 2-2-$2_{1.5b}$ with OSR of 8 will be a good study case for this issue.

The second one would be to implement the proposed RMASH 2-0 and RMASH 2-2 with prototype chips. Since the key of proposed RMASH is to make the modulator oscillate, the experiment results should be studied to prove the capability of DR improvement of proposed RMASH.

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List of Publication

[1] T.-H. Chang, L.-R. Dung, J.-Y. Guo, and K.-J. Yang, "A 2.5V, 14-bit, 180mW Cascaded ΣΔ ADC for ADSL2+ Application," accepted by *IEEE Journal of Solid-State Circuits*.

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