國立交通大學

電機與控制工程學系

博士論文

高輕載轉換效率及最小互穩壓特性之

單電感多輸出直流-直流轉換器

Single-Inductor Multi-Output (SIMO) DC-DC Converters

with High Light-Load Efficiency and Minimized Cross-Regulation

研 究 生：黃銘信

指導教授：陳科宏 副教授

中 華 民 國 九 十 八 年 三 月

高輕載轉換效率及最小互穩壓特性之

單電感多輸出直流-直流轉換器

Single-Inductor Multi-Output (SIMO) DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation

研 究 生：黃銘信　　Student：Ming-Hsin Huang

指導教授：陳科宏　　Advisor：Dr. Ke-Horng Chen

國 立 交 通 大 學

電 機 與 控 制 工 程 學 系

博 士 論 文

A Thesis

Submitted to Department of Electrical and Control Engineering

College of Electrical Engineering National Chiao Tung University

in partial Fulfillment of the Requirements

for the Degree of Doctor

in

Electrical and Control Engineering

March 2009

Hsinchu, Taiwan, Republic of China

中　華　民　國　九　十　八　年　三　月

國　立　交　通　大　學

博碩士紙本論文著作權授權書

（提供授權人裝訂於全文電子檔授權書之次頁用）

本授權書所授權之學位論文，為本人於國立交通大學電機與控制工程系所 B 組，97 學年度第 2 學期取得博士學位之論文。

論文題目：高輕載轉換效率及最小互穩壓特性之單電感多輸出直流-直流轉換器

指導教授：陳科宏 副教授

■ 同意

本人茲將本著作，以非專屬、無償授權國立交通大學，基於推動讀者間「資源共享、互惠合作」之理念，與回饋社會與學術研究之目的，國立交通大學圖書館得以紙本收錄、重製與利用；於著作權法合理使用範圍內，讀者得進行閱覽或列印。

本論文為本人向經濟部智慧局申請專利(未申請者本條款請不予理會)的附件之一，申請文號為：＿＿＿＿＿＿＿＿＿＿＿＿，請將論文延至＿＿＿＿年＿＿＿＿月＿＿＿＿日再公開。

授 權 人：黃銘信

親筆簽名： 黃銘信

中華民國 九十八 年 三 月 十一 日

國家圖書館博碩士論文電子檔案上網授權書

ID:GT009112825

本授權書所授權之論文為授權人在國立交通大學電機學院電機與控制工程系所 B 組 97 學年度第 2 學期取得博士學位之論文。

論文題目：高輕載轉換效率及最小互穩壓特性之單電感多輸出直流-直流轉換器

指導教授：陳科宏 副教授

茲同意將授權人擁有著作權之上列論文全文（含摘要），非專屬、無償授權國家圖書館，不限地域、時間與次數，以微縮、光碟或其他各種數位化方式將上列論文重製，並得將數位化之上列論文及論文電子檔以上載網路方式，提供讀者基於個人非營利性質之線上檢索、閱覽、下載或列印。

※ 讀者基於非營利性質之線上檢索、閱覽、下載或列印上列論文，應依著作權法相關規定辦理。

授權人：黃銘信

親筆簽名： 黃銘信

中華民國 九十八 年 三 月 十一 日

1. 本授權書請以黑筆撰寫，並列印二份，其中一份影印裝訂於附錄三之二(博碩士紙本論文著作權授權書)之次頁；另一份於辦理離校時繳交給系所助理，由圖書館彙總寄交國家圖書館。

國　立　交　通　大　學

博碩士論文全文電子檔著作權授權書

（提供授權人裝訂於紙本論文書名頁之次頁用）

本授權書所授權之學位論文，為本人於國立交通大學電機與控制工程系所B組，97學年度第2學期取得博士學位之論文。

論文題目：高輕載轉換效率及最小互穩壓特性之單電感多輸出直流-直流轉換器

指導教授：陳科宏 副教授

■ 同意 □不同意

本人茲將本著作，以非專屬、無償授權國立交通大學與台灣聯合大學系統圖書館：基於推動讀者間「資源共享、互惠合作」之理念，與回饋社會與學術研究之目的，國立交通大學及台灣聯合大學系統圖書館得不限地域、時間與次數，以紙本、光碟或數位化等各種方法收錄、重製與利用；於著作權法合理使用範圍內，讀者得進行線上檢索、閱覽、下載或列印。

論文全文上載網路公開之範圍及時間：	
本校及台灣聯合大學系統區域網路	■ 中華民國 99 年 6 月 6 日公開
校外網際網路	■ 中華民國 99 年 6 月 6 日公開

授 權 人：黃銘信

親筆簽名： 黃銘信

中華民國 九十八 年 三 月 十一 日

推薦函

一、事由：推薦電機與控制工程系博士班研究生黃銘信提出論文以參加國立交通大學博士論文口試。

二、說明：本校電機與控制工程系博士班研究生黃銘信已完成博士班規定之學科及論文研究訓練。

有關學科部分，黃君以修必應修學分（請查學籍資料），通過資格考試；有關論文方面，黃君已完成“具高輕載轉換效率及最小互穩壓特性之單電感多輸出直流-直流轉換器”博士論文初稿。其論文“Single-Inductor Dual-Output DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices,” 已被 IEEE Journal of Solid-State Circuits 接受將於 April 2009 刊載。另有論文”Low-Ripple and Dual-Phase Charge Pump Circuit Regulated by Switched-Capacitor Based Bandgap Reference,” 已被 IEEE Transaction on Power Electronics 接受將於 2009 刊載。另有論文”Single-Inductor Dual-Output (SIDO) DC-DC Converters for Minimized Cross Regulation and High Efficiency in Soc Supplying Systems” 已被 Analog Integrated Circuits and Signal Processing 接受將於 2009 刊載

三、總言之，黃君已具備國立交通大學電機與控制工程系博士班研究生應有之教育及訓練水準，因此推薦黃君參加國立交通大學電機與控制工程系博士論文口試。

此致

國立交通大學電機與控制工程學系

電機與控制工程學系副教授

陳 科 宏

陳科宏

中 華 民 國 九 十 八 年 一 月 十 九 日

國立交通大學

論文口試委員會審定書

本校電機與控制工程學系博士班黃銘信君

所提論文：高輕載轉換效率及最小互穩壓特性之單電感多輸出直流-直流轉換器

合於博士資格水準，業經本委員會評審認可。

口試委員：

指導教授：

系 主 任：

中 華 民 國　九十八　年　三　月　十一　日

Department of Electrical and Control Engineering

National Chiao Tung University

Hsinchu, Taiwan R.O.C.

Date: March 11, 2009

We have carefully read the dissertation entitled ***Single-Inductor Multi-Output (SIMO) DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation*** submitted by **Ming-Hsin Huang** in partial fulfillment of the requirements of the degree of **DOCTOR OF PHILOSOPHY** and recommend its acceptance.

Ke-Horng Chen

Ching-Tsai Pan

Wang Ching-Sung

Thesis Advisor: Ke-Horng Chen

Chairman: J. C. Chiou

高輕載轉換效率及最小互穩壓特性之
單電感多輸出直流-直流轉換器

研究生：黃銘信　　指導教授 陳科宏 副教授

國立交通大學電機與控制工程學系（研究所）博士班

摘　要

本論文提出可同時提供降壓(buck)及升壓(boost)輸出電源準位並具磁滯模式(hysteresis mode)與負載電流相依式峰值電流控制(load-dependant peak-current control, LDPCC)機制之單電感多輸出直流-直流電源轉換器(single-inductor multi-output converter, SIMO converter)。在 LDPCC 機制及磁滯(hysteresis)模式的自動調節功能控制之下，各個輸出端的互穩壓(cross regulation)效應可被有效的降低。此外，新發表的壓差產生電路(delta-voltage generator)與功率比較器(power comparator)的控制下，SIMO 電源轉換器能平順地在脈寬調變(pulse width modulation, PWM)操作模式與磁滯模式之間切換，故能有效消除當降壓端的輸出功率大於升壓端的輸出功率情形下所產生的電感電流累積效應。本論文所發表的 SIMO 直流電源轉換器使用了 TSMC 0.25μm 2P5M 製程來實現驗証晶片的設計。驗証晶片的實驗結果呈現出在磁滯模式下有 80%的輕載轉換效率及脈寬調變模式下 93%的重載轉換效率，並可得到最小互穩壓效應可減少至 0.35%的輸出電壓準位之內。

關鍵字：單電感多輸出直流電源轉換器(SIMO converter)，互穩壓效應(cross regulation)，磁滯模式(hysteresis mode)

Single-Inductor Multi-Output (SIMO) DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation

Student: Ming-Hsin Huang Advisor: Dr. Ke-Horng Chen

Department of Electrical and Control Engineering

National Chiao-Tung University

Abstract

A load-dependant peak-current control single-inductor multiple-output (SIMO) converter with hysteresis mode is proposed. It includes multiple buck and boost output voltages. Owing to the adaptive adjustment of the load-dependant peak-current control technique and the hysteresis mode, the cross-regulation can be minimized. Furthermore, a new delta-voltage generator can automatically switch the operating mode from pulse width modulation (PWM) mode to hysteresis mode, thereby avoiding inductor current accumulation when the total power of the buck output terminals is larger than that of the boost output terminals. The proposed SIMO converter was fabricated by TSMC 0.25μm 2P5M technology. The experimental results show high conversion efficiency at light loads and small cross-regulation within 0.35%. The power conversion efficiency varies from 80% at light loads to 93% at heavy loads.

Keywords—Single-inductor multi-output (SIMO) converter, cross-regulation, and hysteresis mode.

誌　　謝

行文至此，意味著博士生涯的落幕。在這漫長的博班研讀期間，在校的課程學習、產學合作的研究經歷以及在業界的工作經驗，讓我切切實實地成長為一名獨立自主的研究人員。終於，今年的鳳凰花開對我有著不同意義，不再是督促自我的警剔，而是滿載著離別的愁緒與燦紅的祝福。

如今能順利取得博士學位，感謝 陳科宏教授。那年，在我為研究方向困頓不已之時修了您的課，成了我博士生涯的轉捩點。您那股對實務研究的堅持與熱情一直是我感佩與企求的境地，您總是能在談笑間開拓我的思維，給予我在研究上最大的包容與信賴，引領我前往更寬闊精深的研究領域。每次與您的對話所得的不僅是學術上的洗禮，更是實務技術上的沈積。論文及 PAPER 的產出過程，有您一路指引，感激難以言表。

感謝口試委員 郭斯彥教授、 潘晴財教授、 王清松教授、 黃立仁副總、 鄒應嶼教授及 陳福川教授在口試期間對論文的指導與斧正，使得論文能更臻完善，讓我在幾度峰迴路轉後又見曙光，有了您們寶貴的意見，自己才能對整份研究有了更深切的感知。

感謝與我共事研究、為我擔待的實驗室伙伴們：裕農、 小柯、 國林、 逢哥、 漢翔、 均元、 福龍、 東樺、 君晏，這幾年你們的下線時程總是因我的研究變得不盡合理，謝謝你們毫無怨言、全心全力的配合。還有 謝小乖、 昱輝，謝謝你們願意與我相互分享、討論研究的想法，減少探索研究議題的時間。感謝 小契，每每與我在實驗室挑燈到午夜。

感謝一路相守的 彥君，有妳的耳提面命，我才能不忘作為一個學生的本分，不致迷失在茫茫的學海之中，有妳的支持鼓勵，我才能筆直向前，努力不懈，相信這一切的過程值得我們一輩子咀嚼回味。感謝 爸媽、 岳父母以及我的家人，是你們默默的支持及守護，讓我可以毫無迭躂地走完博士研究的道路。感謝伴隨在我週遭的朋友，你們的鼓勵與陪伴，給了我不少的動力。

誠如 陳之藩先生於謝天一文所述的：「真正做了一些小貢獻以後，才有了一種新的覺悟：即無論什麼事，得之於人者太多，出之於己者太少。因為需要感謝的人太多了，

就感謝天罷。無論什麼事，不是需要先人的遺愛與遺產，即是需要眾人的支持與合作，還要等候機會的到來。越是真正做過一點事，越是感覺自己的貢獻之渺小。」

感謝天，讓我立足於此，佔有一席，沒有因為挫折壓力而放棄求學的道路。感謝天，付予我堅強的勇氣和毅力，讓我能在研究學習的長河中喘息。最後，感謝這一直伴隨我的校園長廊，一如往昔地聆聽著我低聲的獨語。

黃銘信 謹誌

國立交通大學 電機與控制學系

二〇〇九 初春

Contents

Figure Captions

Table Captions

Chapter 1

Introduction

1.1 Background

Today's field of power management requires high power conversion efficiency, fast line/load transient response, and small volume of the power module. In particular, cell phones, digital cameras, MP3 players, PDAs and portable products require varied voltage levels of power supplies for delivery to different sub-modules in portable products. Thus, there are different designs that provide different voltage levels as shown in Fig. 1~3. Low dropout (LDO) regulator arrays are one of the designs for different voltage levels as depicted in Fig. 1, where the index i is from 1 to n which is used to index the n^{th} output. However, LDO regulator arrays sacrifice power conversion efficiency and greatly reduce battery life. The other solution is illustrated in Fig. 2, which combines with different inductive switching converters. The high power conversion efficiency is ensured by the inductive switching converter. However, the large number of inductors occupies the large footprint area and increase fabrication cost.

The single inductor multiple output (SIMO) converter has been developed as a suitable solution to achieve microminiaturization and high power conversion efficiency for a power management unit. The conceptual SIMO converter shown in Fig. 3 uses only one external inductor component to generate multiple voltage levels for different sub-modules in the portable products. The SIMO converter not only reduces the footprint area and fabrication cost but also achieves high power conversion efficiency [1]. However, all load current

conditions of the multiple output terminals arise in the current level of the inductor. When the load current condition of each output accumulates in the same inductor, the design challenges of the SIMO converter such as cross-regulation, power conversion efficiency, system stability, and lack of flexibility of both the buck and boost must be seriously addressed.

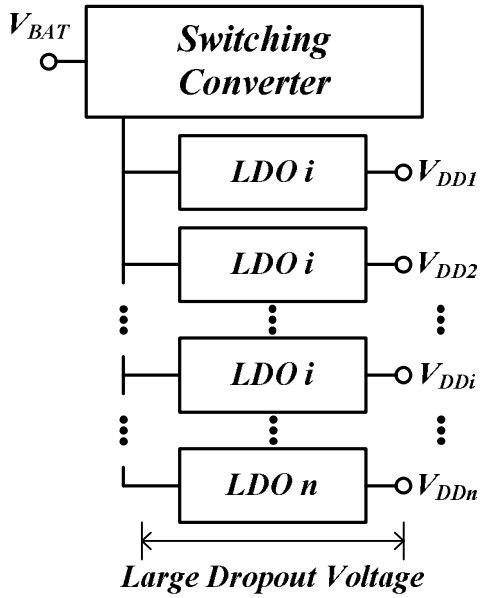


Fig. 1. The power management designs which uses LDO array.

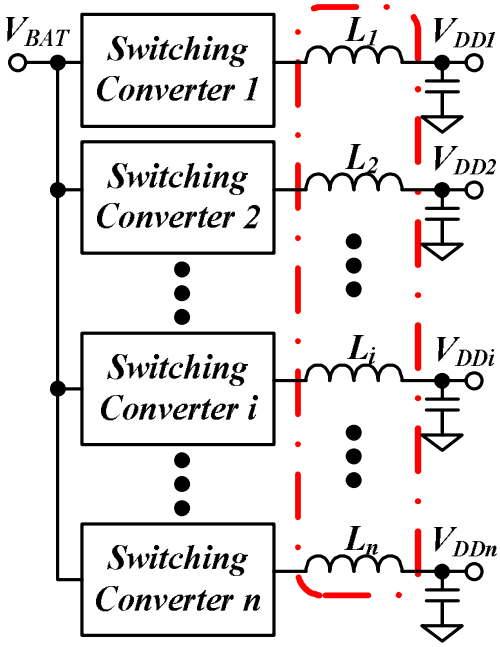


Fig. 2. The power management designs which combines with different inductive switching converters.

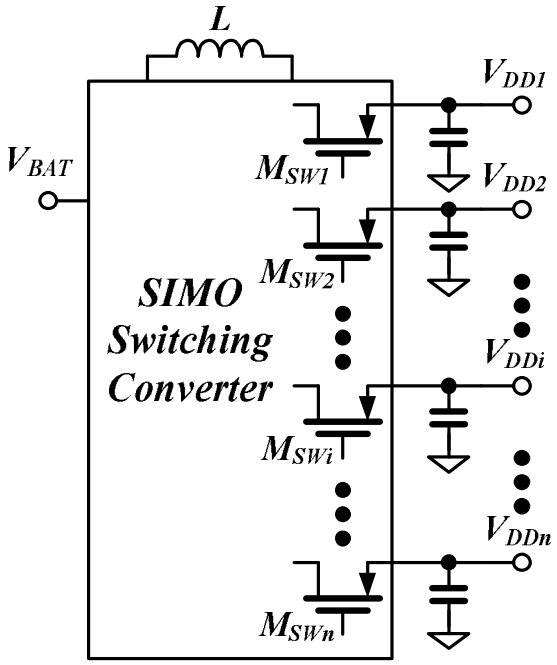


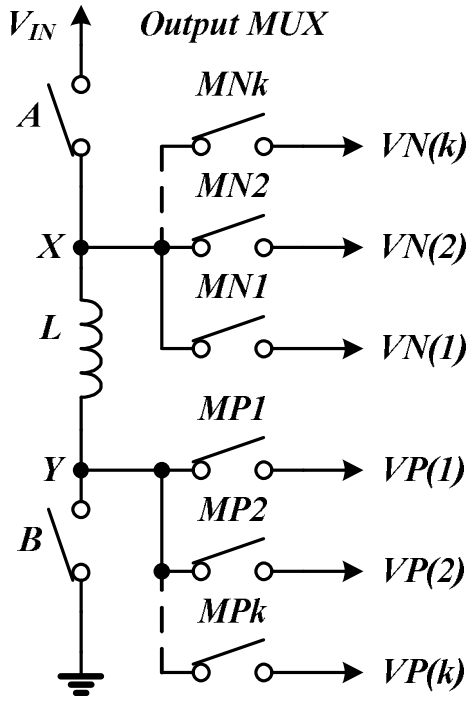
Fig. 3. The conceptual SIMO converter uses only one external inductor component to generate multiple voltage levels.

1.2 Prior Arts

Several topologies and control techniques have been proposed to implement SIMO converters [2]-[13]**.** The SIMO converter in [1] uses the hysteretic continuous current mode (CCM) control method and state machine to regulate output voltage. The proposed single-inductor multiple positive/negative output dual-loop DC-DC converter illustrated in Fig. 4 can deliver all positive and negative output voltage levels independently cycle by cycle. The output power stage of SIMO converter depicted in Fig. 4 takes physical behavior of an inductor which is loaded with a certain current (I_{PEAK}) when switches *A* and *B* closed. Since the current in the inductor is continuous, the inductor always generates a voltage with reverse polarity across its two terminals when disconnected from the supply. For the positive inductor node *X* getting open, when switch *A* opened and switch *B* closed, node *X* goes negative (below ground), since the inductor tries to keep current running the same direction and magnitude than before. Oppositely, a positive voltage (above V_{IN}) is generated on negative node *Y* if switch *A* closed and switch *B* opened. In these two situations the multiplexing

switches *MN1~MNk* and *MP1~MPk* determine which outputs *VN(1)~VN(k)* and *VP(1)~VP(k)* can get energy stored in the inductor. When inductor is periodically loaded with current (I_{PEAK}) when switches *A* and *B* closed, each output *VN* and *VP* can be supported with energy cycle by cycle. The implementation of output power stage as shown in Fig. 5 generates two positive voltages (V_{GH} and V_{BOOT}) and one negative voltage (V_{GL}). A synchronous rectifier *P2* runs in parallel to the Schottky diode *D1* to enhance efficiency. A back-to-back isolated rectifiers ($N2 + D1 // P2$ and $N3 + D2$) in output multiplexers are required; otherwise to lower positive output voltage would always clamp the higher one. An off-chip Schottky Diode *D3* is used for negative rectification. Transistors *N1* and *P1* connect inductor *L* to supply terminals.

The state machine as shown in Fig. 6 determines the operating pattern of output power stage. Comparators *Vgl*, *Vgh*, and *Vbt* of each channel detect output voltage level to regulate output voltages. Logic part of state machine takes previous states and calculates next state of output power stage. A hysteretic control scheme which simply runs with a fixed off-time and adaptive peak current control is applied. Since inductor always is loaded with an independent peak current level at the beginning of off-state, output cross-regulation is negligible in adaptive peak current control shown in Fig. 7. The frequency of adaptive peak current control is directly coupled to output loads and adjusted accordingly to state machine. Therefore, there are two different types of regulation loops running in the converter. A hysteretic loop is utilized to take care of the output voltages. Hence, the control of individual channel is managed by a state-machine controlling loop which allows hysteretic converter to run in a pseudo-continuous current mode (PCCM) to guarantee a high power capability. The second loop works as adaptive peak current control to minimize inductor current. It yields a small output voltage ripple and minimized cross-regulation. Since the work proposed the back-to-back rectifier and state-machine controller, the power dissipation and the size of controller become hardly to decrease.



Outputing Pattern

Operation	Switch A	Switch B	Output MUX
Load Ind	ON	ON	
VN(1)		ON	MN1
VN(2)			MN2
VN(k)		ON	MNk
VP(1)			MP1
VP(2)	ON		MP2
VP(k)			MPk

Fig. 4. The physical behavior of single-inductor multiple positive/negative output dual-loop DC-DC converter.

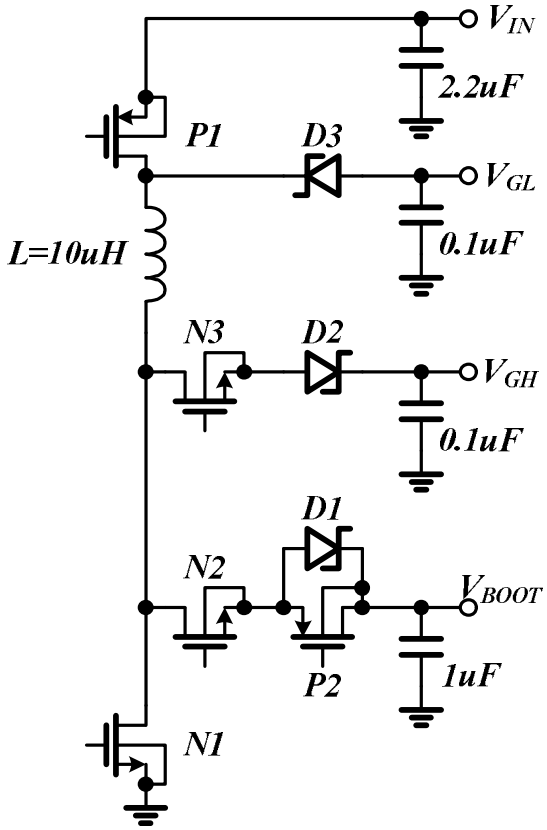


Fig. 5. The implementation of output power stage.

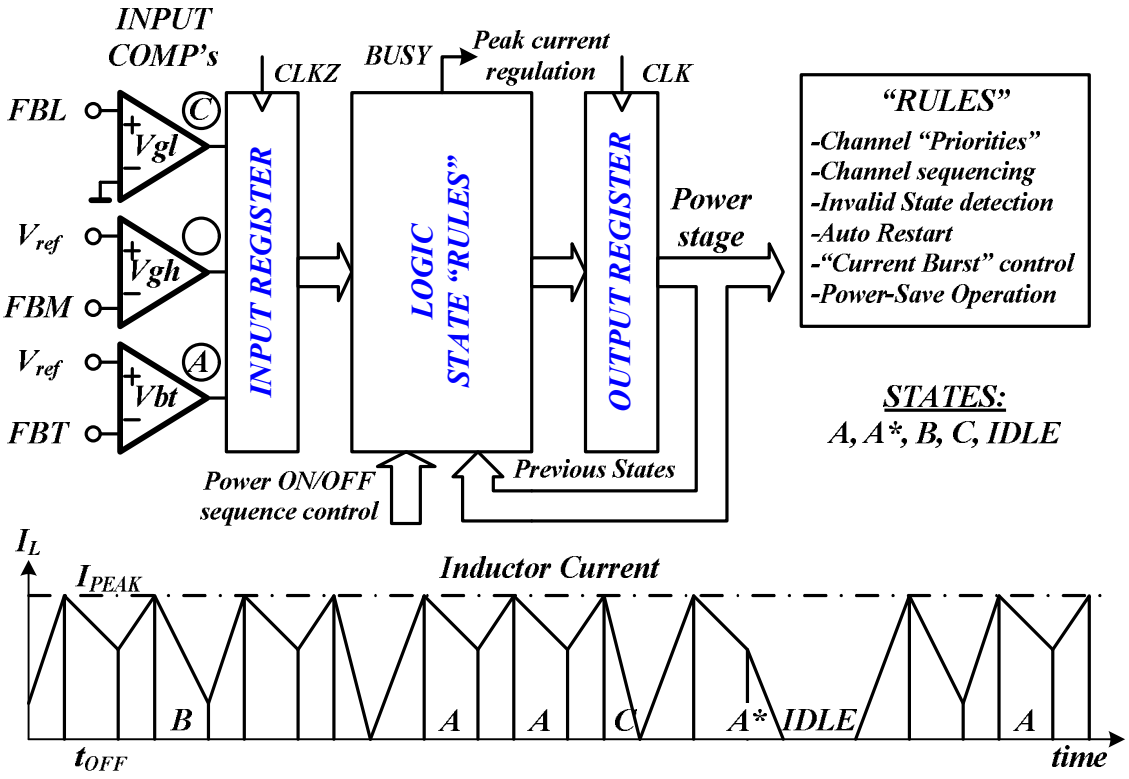


Fig. 6. The state machine determines the operating pattern of output power stage.

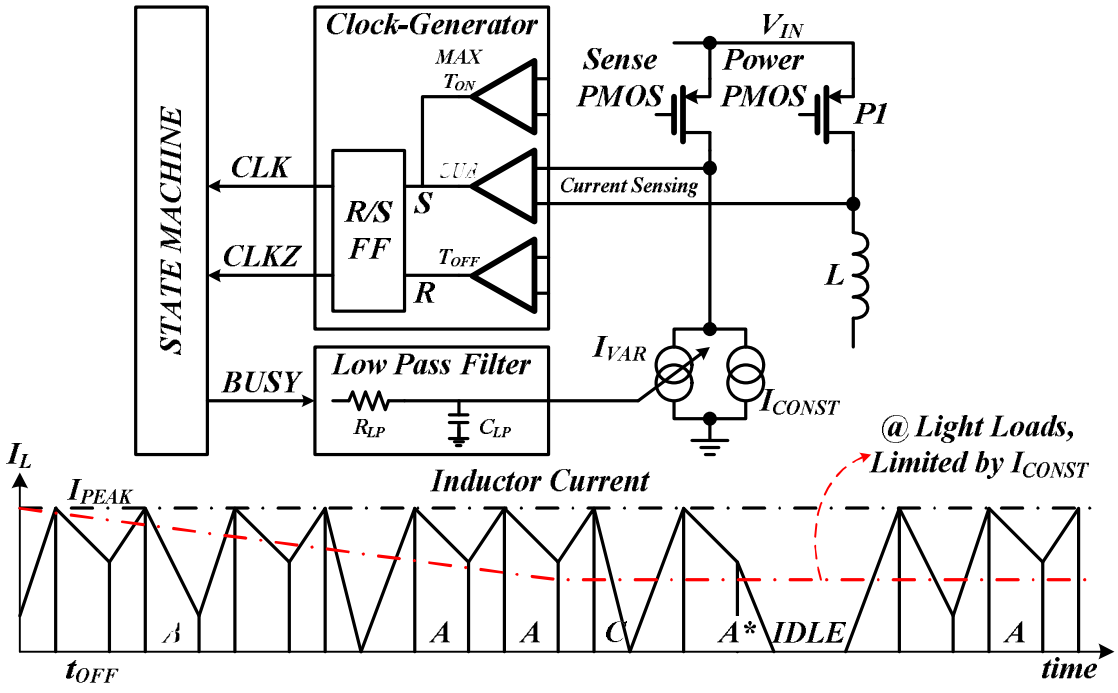


Fig. 7. The adaptive peak current control is applied to directly couple to output loads and adjust accordingly to state machine.

The work in Fig. 8 proposed a charge-control (QC) method that works in PCCM to regulate output voltage (V_{oa}) is lower than source voltage (V_g) and output voltage (V_{ob}) is higher than source voltage (V_g) [2]. Fig. 9 shows the corresponding timing diagram of QC method. A minimum number of switches are used for the single-inductor dual-output (SIDO) converter with QC method. At the instant of clock (φ_1), switch S_2 is closed and inductor current ramps up from a freewheeling level (I_1) with slope (V_g/L) until it reaches the predefined level (I_{DC}). Inductor is then connected to output V_{oa} after closing switch S_{3a} and then clock (φ_a) is set to high. The inductor current (I_L) continues to ramp up with a positive slope ((V_g–V_{oa})/L) and is integrated by capacitor C_{ia} of current sensor which is shown in Fig. 8. As a result, the charge (Q_{oa}) on capacitor C_{ia} can be used to decide duty cycle of output V_{oa}. Switch S_{3a} is opened and switch S_{3b} is closed, the inductor is connected to output V_{ob} and clock (φ_b) is set to high. The inductor current (I_L) ramps down with a negative slope ((V_{ob}–V_g)/L) and is integrated on the capacitor C_{ib} of current sensor which is shown in Fig. 8. The charge (Q_{ob}) on the capacitor C_{ib} decides the duty cycle of output V_{ob}. Switch S_{3b} is then opened and switch S_1 is closed, shorting out the inductor to allow freewheeling current (I_1). The inductor current waveform of QC method is shown in Fig. 10. The characteristic of inductor current can be expressed as follows. Let the slopes (m_1, m_2 and m_3) of inductor current in the time intervals (t_1, t_2 and t_3) be:

$$m_1 = \frac{V_g}{L}; m_2 = \frac{V_g - V_{oa}}{L}; m_3 = \frac{V_{ob} - V_g}{L} \tag{1}$$

$$t_1 = \frac{I_{DC} - I_1}{m_1} \tag{2}$$

The charge (Q_{oa}) under time interval (t_2) which depends on the load current (I_{oa}) of output V_{oa} is the charge delivered to output V_{oa}:

$$Q_{oa} = \frac{1}{2}\left(I_{DC} + I_{DC} + m_2 t_2\right)t_2 = I_{oa}T \tag{3}$$

$$t_2 = \frac{1}{m_2}\left(\sqrt{I_{DC}^2 + m_2 I_{oa}} - I_{DC}\right) \tag{4}$$

Similarly, the charge (Q_{ob}) under the time interval (t_3) which depends on the load current (I_{ob}) of output V_{ob} is the charge delivered to output V_{ob}:

$$Q_{ob} = \frac{1}{2}\left(I_1 + I_1 + m_3 t_3\right)t_3 = I_{ob}T \tag{5}$$

$$t_3 = \frac{1}{m_3}\left(\sqrt{I_1^2 + m_3 I_{ob}} - I_1\right) \tag{6}$$

With reference to Fig. 10, the volt–second balance of inductor current can derive (7) and (8).

$$m_1 t_1 + m_2 t_2 = m_3 t_3 \tag{7}$$

$$I_{DC}^2 - I_1^2 = m_2 I_{oa} T - m_3 I_{ob} T \tag{8}$$

This converter in Fig. 8 requires fewer switches than the conventional design. Comparing the simulation results of the non-inverting fly-back converter with that of the buck/boost converter, 5% improvement in efficiency is achieved under the same load condition. Also, good line and load regulations are also guaranteed and cross-regulation is minimized by a pre-defined and fixed freewheeling current level (I_{DC}). Owing to the fixed freewheeling current level (I_{DC}) and an undesired inductor current level which is generated by the charge (Q_{oa}) under time interval (t_2), the power efficiency is greatly decreased at light load condition.

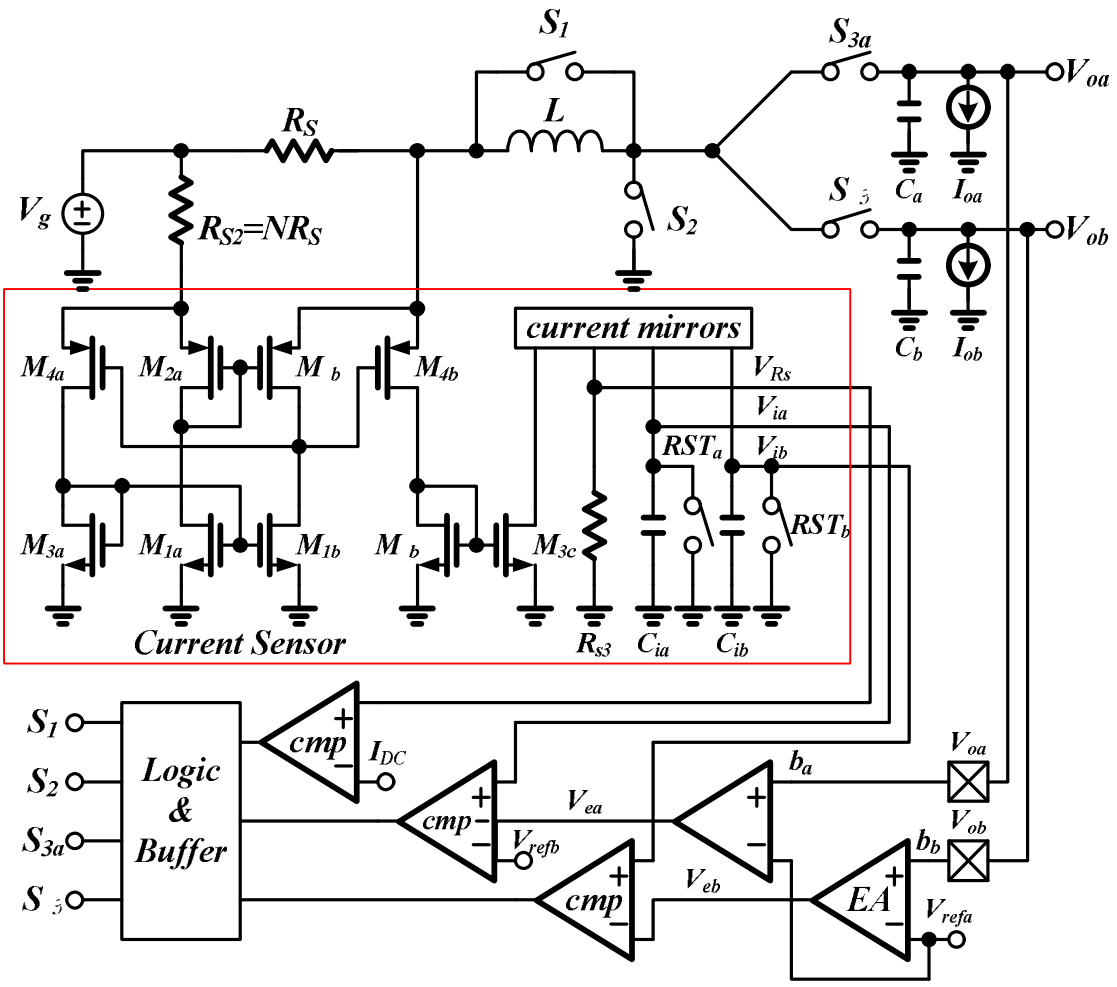


Fig. 8. The QC method which works in PCCM to regulate one buck and one boost output.

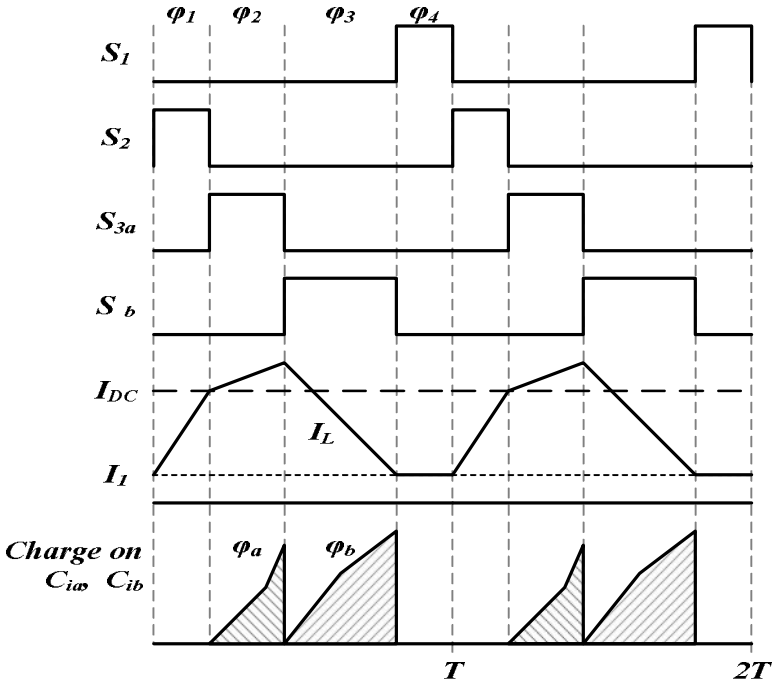


Fig. 9. The corresponding timing diagram of QC method.

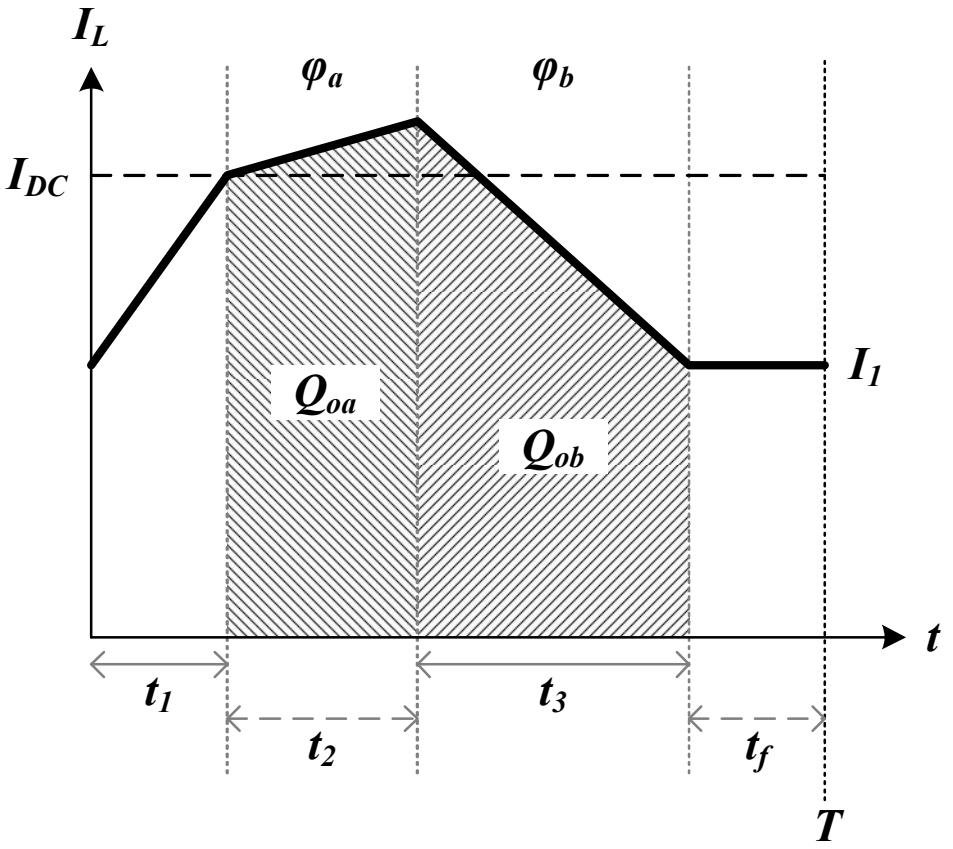


Fig. 10. The inductor current waveform of QC control method.

The works in [3 and 10] calculate and minimize cross-regulation problem when one period is divided to regulate dual boost output voltages. The sub-converters *A* and *B* of SIDO converter as shown in Fig. 11 share inductor *L* and switch S_1 [3]. The operating principle is described with reference to the timing diagram shown in Fig. 12. Let clock (φ_a) and clock (φ_b) be complementary phases of the same duration. During clock (φ_a) is set to high, switch S_b is opened and no current flows into output V_{ob}. Then, switch S_1 is closed first. The inductor current (I_L) increases until time interval ($D_{1a}T$) expires, which is determined by the output of an error amplifier. During time interval ($D_{2a}T$), switch S_1 is opened and switch S_a is closed to divert inductor current (I_L) into output V_{oa}. A zero current detector senses inductor current (I_L), and when it goes to zero, the converter enters time interval ($D_{3a}T$), and switch S_a is opened again. The inductor current stays zero until clock (φ_b) is set to high. Time intervals (D_{1a} and D_{2a}) satisfy the requirements that

$$D_{1a} + D_{2a} \le \frac{1}{2} \tag{9}$$

During clock (φ_b) is set to high, the inductor current (I_L) is multiplexed into output V_{ob}. Similar switching action repeats for sub-converter B and the two outputs are regulated alternately. When converter which works at CCM or discontinuous current mode (DCM) suffers serious cross-regulation, therefore the SIDO converter in [3] employs time-multiplex (TM) control and works in the DCM. Let the conversion ratio (M_a) of sub-converter A be $M_a = V_{oa}/V_g$. Volt-second balance of sub-converter A gives

$$V_g D_{1a} = \left(V_{oa} - V_g\right) D_{2a} \tag{10}$$

For boost converter, load current (I_{oa}) is equal to averaged diode current. Hence, from Fig. 12

$$I_{oa} = \frac{V_g}{2L} \frac{D_{1a}^2}{\left(M_a - 1\right) f_s} \tag{11}$$

where is the f_s switching frequency. Maximum power occurs when $D_{1a} + D_{2a} = 0.5$, and sub-converter A works at the boundary of CCM and DCM. The maximum duty ratio, maximum load current ($I_{oa(\max)}$), and maximum power ($P_{o(\max)}$) are then given by

$$D_{1a(\max)} = \frac{M_a - 1}{2M_a} \tag{12}$$

$$I_{oa(\max)} = \frac{V_g}{2L} \frac{\left(M_a - 1\right)}{4M_a^2 f_s} \tag{13}$$

$$P_{o(\max)} = P_{oa(\max)} + P_{ob(\max)} = \frac{V_g^2}{8Lf_s} \left[\frac{1}{M_a\left(M_a - 1\right)} + \frac{1}{M_b\left(M_b - 1\right)} \right] \tag{14}$$

Moreover, the definition of duty cycle $\left(D_{1a} + D_{2a}\right)T = 0.5T$ and switching period $T = \varphi_a + \varphi_b$ are used to analyze the cross-regulation of output current at sub-converters A and B. The analysis in [10] gives

$$I_{oa} = \frac{V_g}{2L} \frac{\left(M_a - 1\right)}{M_a^2} \frac{\varphi_a^2}{\varphi_a + \varphi_b} \tag{15}$$

$$I_{ob} = \frac{V_g}{2L} \frac{(M_b - 1)}{M_b^2} \frac{\varphi_b^2}{\varphi_a + \varphi_b} \tag{16}$$

$$\frac{I_{oa}}{I_{ob}} = \left(\frac{M_b}{M_a}\right)^2 \frac{M_a - 1}{M_b - 1}\left(\frac{\varphi_a}{\varphi_b}\right)^2 \tag{17}$$

From the previous discussion, a PCCM mode for SIDO converter as shown in Fig. 13, which not only inherits the merits of cross-regulation suppression, but is also capable of handling large current stress at heavy loads. Moreover, the implementation should be simple to achieve high efficiency. The converter switches at a fixed frequency (f_s) and the inductor current (I_L) goes to zero or fixed offset current level (I_{DC}) after discharging into each output. A load change at output V_{oa} will change both time intervals (D_{1a} and D_{2a}), but as long as (9), the energy transfer for output V_{ob} will remain unaffected. In fact, the duty cycle (D_{1a}) of output V_{oa} is given by

$$D_{1a} = \sqrt{\frac{2M_a(M_a - 1)L}{R_{oa}} f_s} \tag{18}$$

which depends only on the equivalent load resistances (R_{oa}) at output V_{oa} and fixed offset current (I_{DC}). Hence, the converter does not exhibit cross-regulation. However, owing to the fixed current level (I_{DC}), the power efficiency is greatly decreased at light load condition.

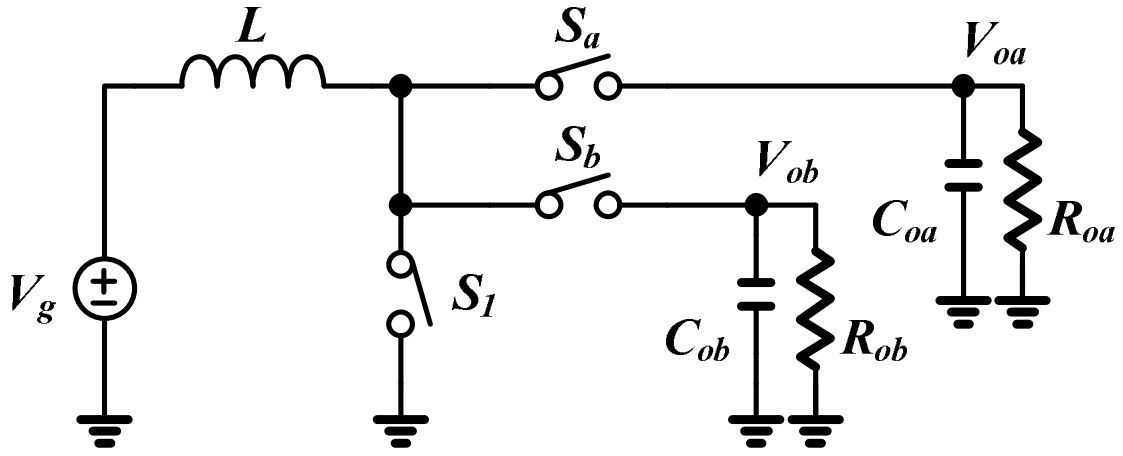


Fig. 11. The architecture of dual output DCM converter with TM control method [3].

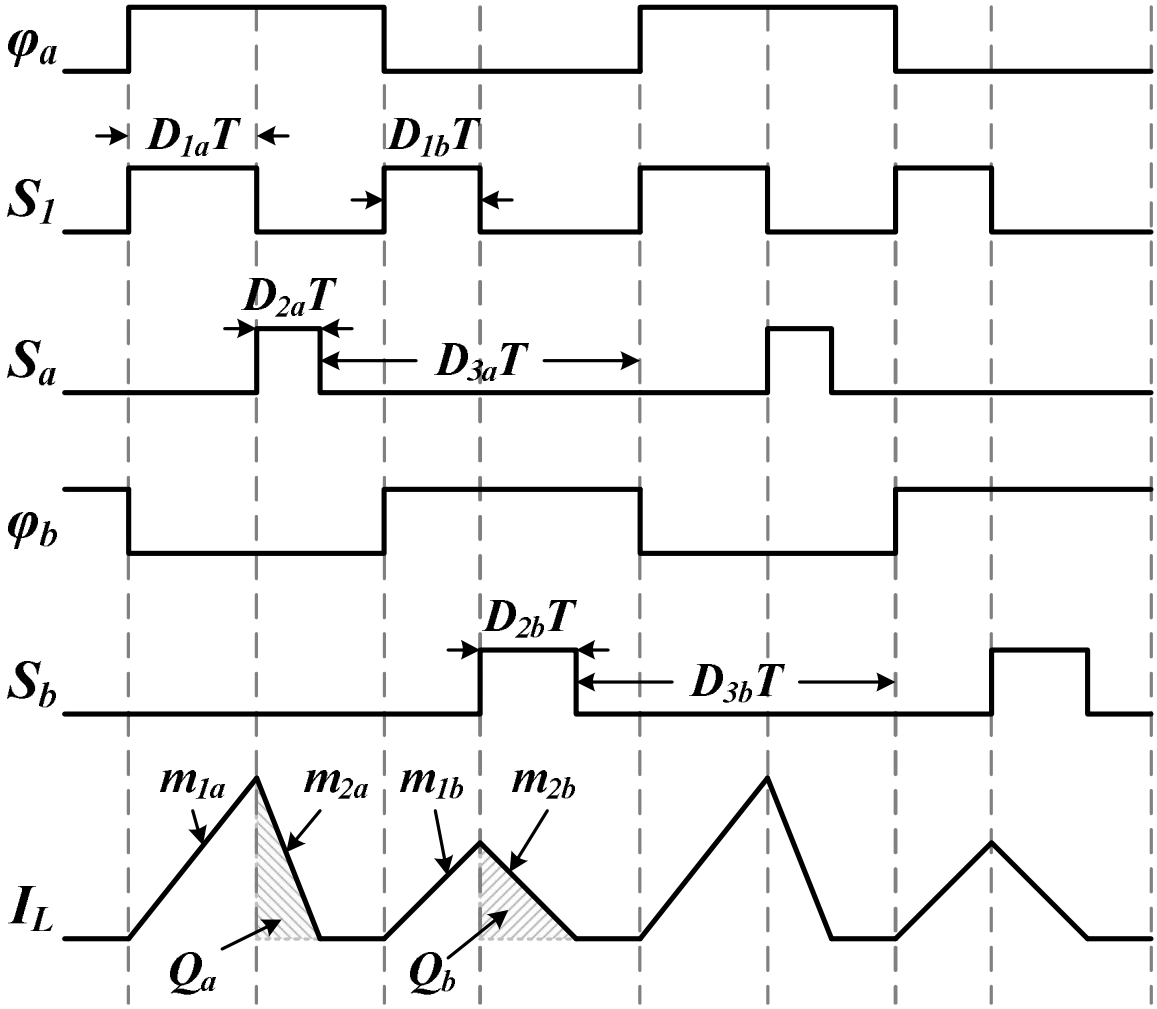


Fig. 12. The timing diagram of TM control method [10].

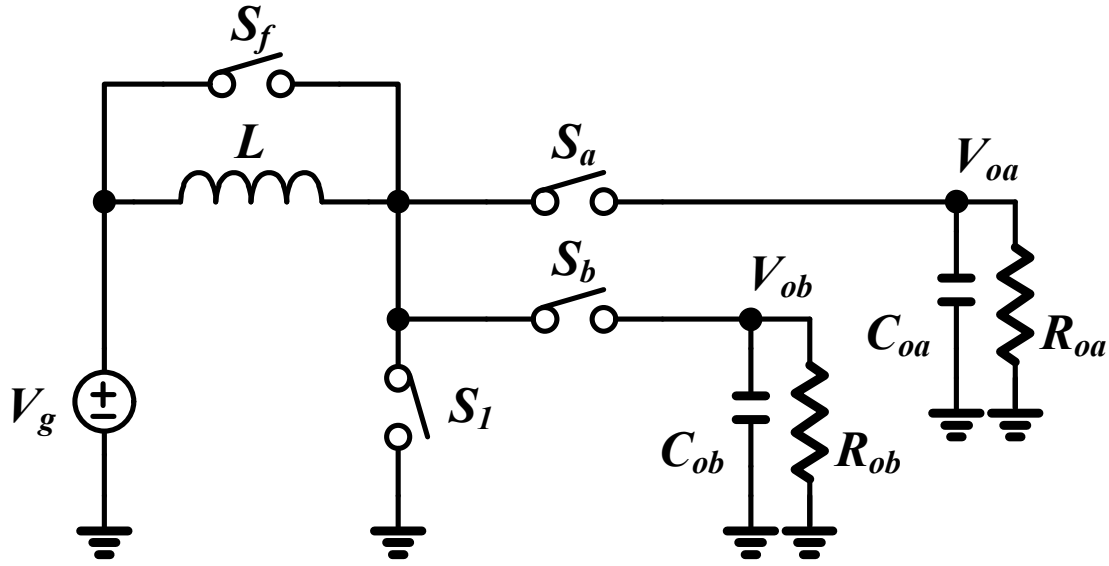


Fig. 13. The architecture of PCCM control mode for SIDO converter which [10].

The works in [11 and 24] propose a freewheeling current feedback as current control method to regulate multiple-boost output voltages. Figure 14 illustrates the architecture of multiple-boost output converter with freewheeling current feedback, and Fig. 15 shows the operational timing diagram for a single output operation. The storage energy which should be stored and transferred to output terminal is stored and monitored in form of inductor current (I_L) during freewheeling period (D_fT) of every switching cycle (T). In operations, if output needs more energy, the average current (I_{avg}) of freewheeling current (I_{fw}) will be decreased to a lower level or zero to supply output; else if output suddenly needs less energy, the average current (I_{avg}) of freewheeling current (I_{fw}) will be increased to a high level. Since that freewheeling current (I_{fw}) is monitored and compared to a reference, the main control loop of converter will indirectly know an instantaneous condition of output to charge either more or less energy in the inductor L, without sensing output nodes.

An error signal at output of transcondcutance amplifier $G_C(s)$ determines peak current level (I_{pk}) of inductor, similar to a conventional current mode control. A reference current (I_{offset}) gives an offset of freewheeling current (I_{fw}) from ideally zero. The output switch S_{o1} is controlled by a comparator CMP_{o1} with a reference voltage, forming a feedback loop to regulate output V_{o1}. The voltage feedback loop only cares for rated output voltage level, but not total current charged in the inductor L. In this way, neither inductor L and output capacitor C_{o1}, nor equivalent load resistance R_{L1} affects total current loop response. While main switch S_n is closed, inductor current (I_L) increases with a positive slope (V_g/L). When inductor current (I_L) reaches a current level (I_{pk}) which is determined by the compensator CMP_d and output of transcondcutance amplifier $G_C(s)$, main switch S_n is opened and S_{o1} is closed. During time interval (D_oT), inductor current (I_L) decreases with a negative slope ((V_{o1}-V_g)/L), transferring the storage energy to output capacitor C_{o1}. As soon as comparator CMP_{o1} detects that output voltage (V_{o1}) reaches its target voltage (V_{ref1}), switch S_{o1} is opened and the freewheeling switch S_f is closed. Then, the residual current or extra energy of inductor L freewheels through

freewheeling switch S_f during time interval D_fT. In steady state, there always exists some residual energy in the inductor L at the end of every switching cycle.

In Fig. 15, the left diagram shows an operation of single output converter in a light load condition, where the freewheeling current level (I_{fw}) is low but the duty cycle D_f is large. The right diagram shows an operation of single output converter in a heavy load condition, where the freewheeling current level (I_{fw}) is high but duty cycly D_f is small. The extra energy in form of average current ($I_{avg} = (D_f \times I_{fw})$) of freewheeling current (I_{fw}) but not its instantaneous current level is controlled to the average current (I_{avg}), thus area A_2 equals to area A_1. The freewheeling current (I_{fw}) will introduce a power loss due to non-zero on-resistance of freewheeling switch S_f. To minimize this power loss, the average current (I_{avg}) is expected as low as possible which ideally close to zero. Although the main switch current (I_n) is used for duty cycle control like conventional current mode converters, slope compensation is not necessary for the main current feedback loop in the proposed control since a freewheeling period exists in every switching cycle making the operation similar to that of DCM converter. Similar inductor current waveforms are found in PCCM converters. Since that main control loop of converter indirectly knows an instantaneous condition of output to charge either more or less energy in the inductor L, a low transient response is appeared at output terminals. Moreover, since the regulation of each output terminal has to be detected that output voltage reaches its target voltage by comparator, a poor cross-regulation is going to exhibit at different output load condition.

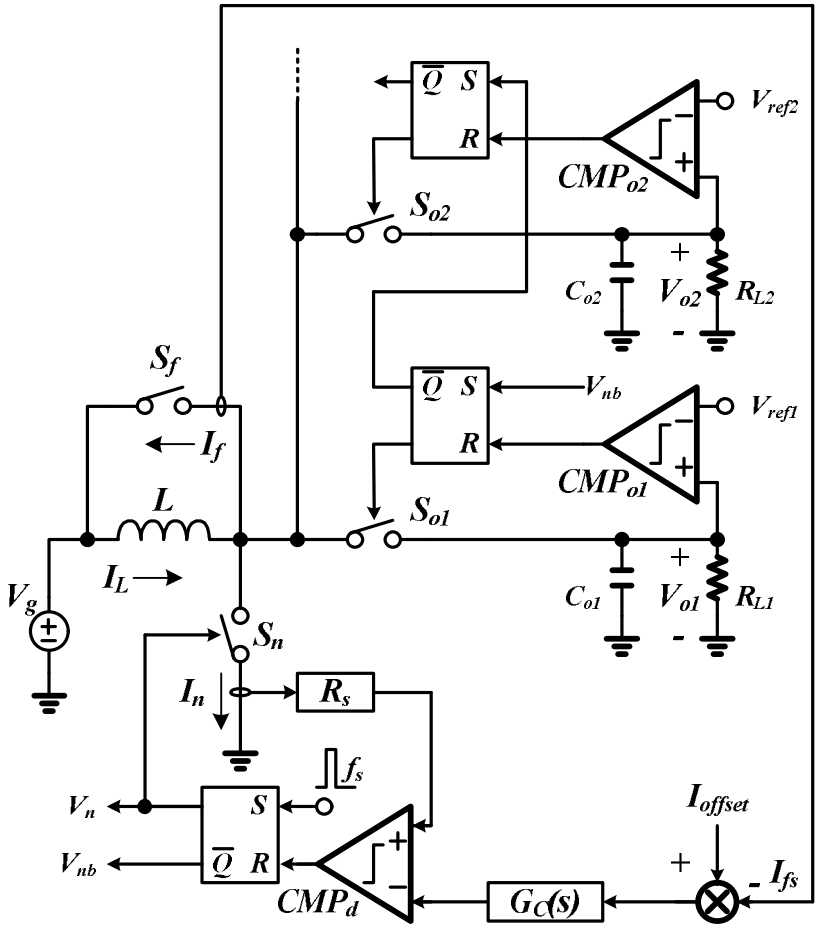


Fig. 14. The synchronous boost converter with freewheeling current feedback [24].

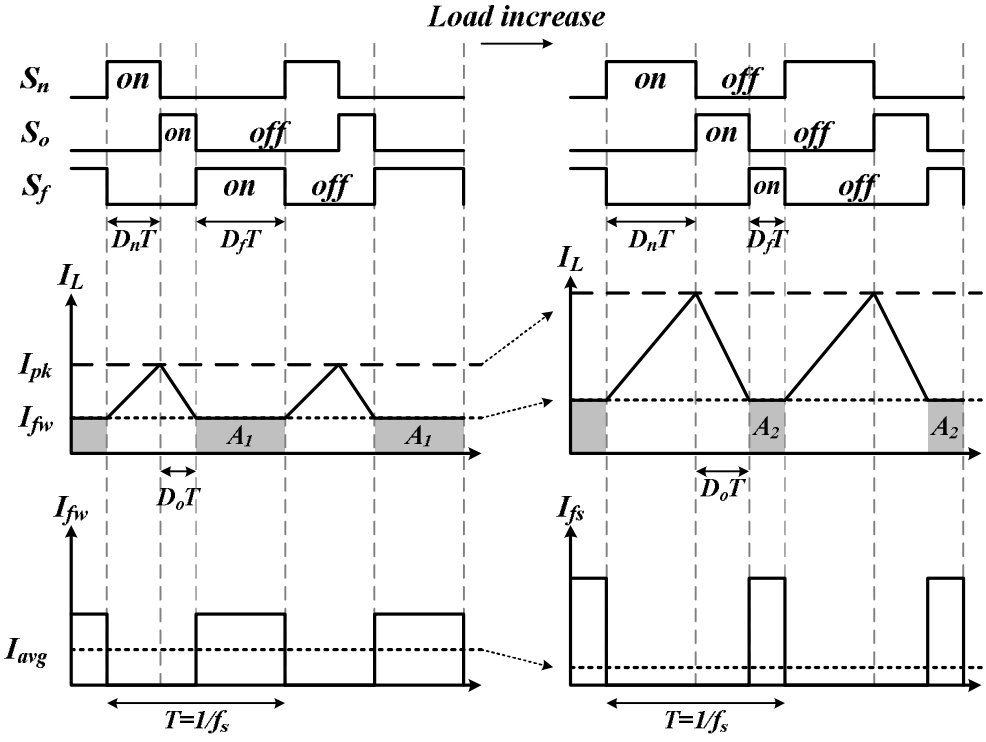


Fig. 15. The timing diagram at different load condition.

The architecture of five-output SIMO converter in [13] is shown in Fig. 16. The ordered power-distributive control (OPDC) converter arranges one negative output V_{oN} and four boost output terminals V_{o1}, V_{o2}, V_{o3}, and V_{o4} in descending order of priority to, one by one, share the charge from inductor in every switching cycle or, more correctly, every power distribution cycle. The first three boost output terminals V_{o1}, V_{o2}, and V_{o3} are controlled using comparators and are thus called comparator-controlled output voltages, while the last-ordered output V_{o4} is P-I controlled with an error amplifier that is responsible for the total storage charge of OPDC converter Therefore, in OPDC converter, all of the errors of preceding comparator-controlled output voltages are transferred and accumulated to the last, which is only one requiring a compensation network in the feedback loop.

The operating principle of OPDC converter can be explained using timing diagram in Fig. 17, where the high part of the signal S_i represents on-state of switch S_i. During the time interval (DT), main switch S_N is closed and inductor current (I_L) ramps up with a positive slope (V_g/L) until it reaches the peak current level (I_{peak}). The freewheeling switch S_f and four output switches S_1, S_2, S_3, and S_4 turn on during the time interval ($D'T$), where $D'+D=1$. During time interval ($D'T$), inductor current (I_L) ramps down with different slopes depending on the output voltages and switching sequence. Output switch S_1 is closed at the beginning of time interval ($D'T$), making inductor current (I_L) ramps down with a negative slope ((V_{o1}-V_g)/L) and flow into output V_{o1}. As soon as comparator CP_1 detects that voltage of output V_{o1} is larger than its target voltage (V_{ref1}), time interval (D_1T) expires, output switch S_1 is opened, and switch S_2 is closed. The same sequence then repeats as inductor current (I_L) ramps down with a slope, while V_{o2}, V_{o3} and then V_{o4}, in turn, get the portions of charge, respectively. When the inductor current (I_L) is zero, time interval (D_4T) expires, output switch S_4 is opened, and freewheeling switch S_f is closed during time interval (D_fT) to short the two ends of inductor L and suppress possible ringing at node V_X until the end of the switching cycle. In this mode of operation, the converter works in DCM.

The inductor current (I_L) of different load conditions is illustrated in Fig. 18. Since doesn't decrease to zero in CCM operation, there is no freewheeling period as illustrated by inductor current waveform $I_L(1)$. Dependent on the last portion of charge, the loop containing output V_{o4} and the total current loop are compensated and controlled by peak current control method. These control loops guarantee that the last portion of charge is enough to keep the last output at its target voltage, while good voltage regulation is already maintained in the preceding output terminals V_{o1}, V_{o2}, and V_{o3}. A charge-pump circuit included in Fig. 16 with two Schottky diodes and two capacitors (C_{N1} and C_{N2}) is connected to node V_X and makes a negative output V_{oN} from voltage changes at node V_X. The flying capacitor C_{N1} gets charge when positive outputs get energy and node V_X goes high and then transfers negative charge to output capacitor C_{N2} when switch S_N is closed and node V_X goes low. The negative voltage of output V_{oN} depends on voltage drop over Schottky diodes and the highest positive output voltage. The flexibility of the OPDC converter proves that the converter can have different switching patterns in regulating the outputs, as shown in Fig. 18. Inductor current waveform $I_L(2)$ shows the case of CCM operation where three or two output switches are orderly and alternately on in one switching cycle. Operation at the boundary of CCM and DCM and one in DCM are illustrated with Inductor current waveforms $I_L(3)$ and $I_L(4)$, respectively. Furthermore, OPDC converter allows that the turn-on frequency and the duty cycle (D_i) of an output switch do not always have to be constant.

Inductor current waveforms $I_L(5)$ and $I_L(6)$ in Fig. 19 are used as examples to maintain low cross-regulation for load changes in output V_{o3}, which are seen similar to those in output terminals V_{o1} and V_{o2}. In inductor current waveform $I_L(5)$, the load changes to heavy loads, making output V_{o3} drop below the predetermined voltage. Detecting that by the relative comparator, OPDC converter will allow switch S_3 to occupy the rest of discharge period after switches S_1 and S_2 in next switching cycles until output V_{o3} returns to its required voltage. As output V_{o4} receives no charge in those cycles, the P-I loop increases the duty cycle D of

switch S_N which is current charge in the inductor L. At the same time, the duties and are spontaneously reduced by the comparators cp_1 and cp_2 in Fig. 16 to make sure output terminals V_{o1} and V_{o2} stay at their level. The opposite situation is shown with inductor current waveform $I_L(6)$. As output loading is decreased in output V_{o3}, the duty cycle D_3 is reduced abruptly by comparator cp_3 in Fig. 16 to keep output V_{o3}, leaving the residual charge to output V_{o4}. The output V_{o4} will soon be stabilized back to its regulating level because of P-I loop and total current loops. Owing to the OPDC converter allows the turn-on frequency and duty cycle of output switch don't have to be constant, a poor cross-regulation and low transient response is going to exhibit at output terminals.

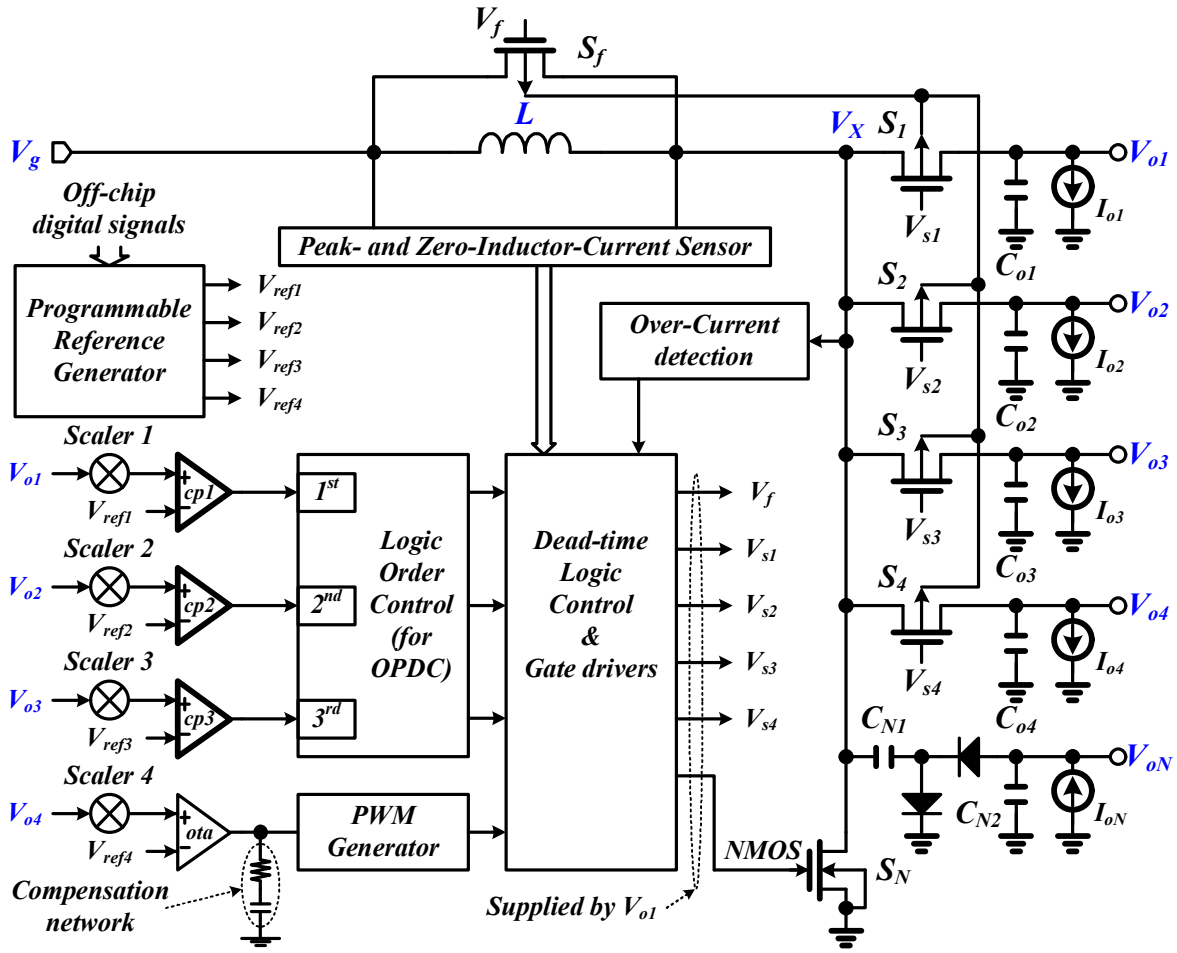


Fig. 16. The five-output SIMO converter with OPDC in [13].

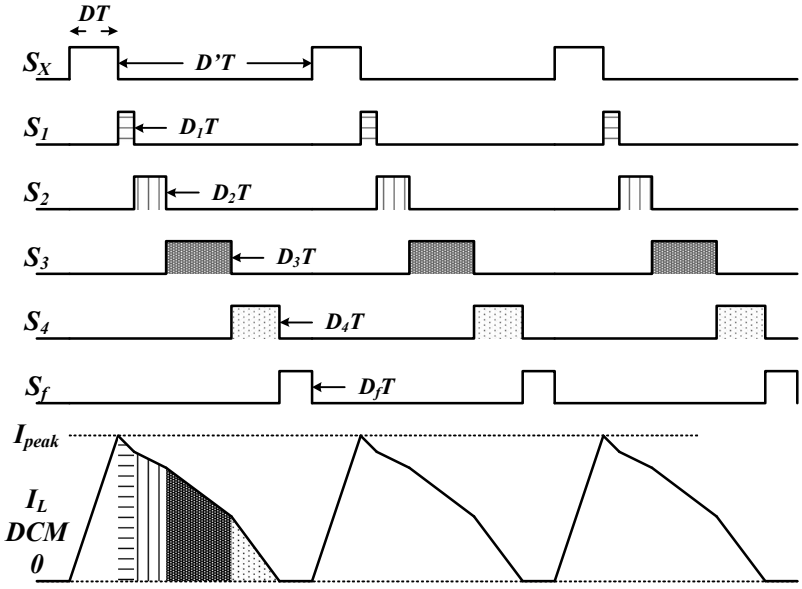


Fig. 17. The timing diagram of OPDC operation.

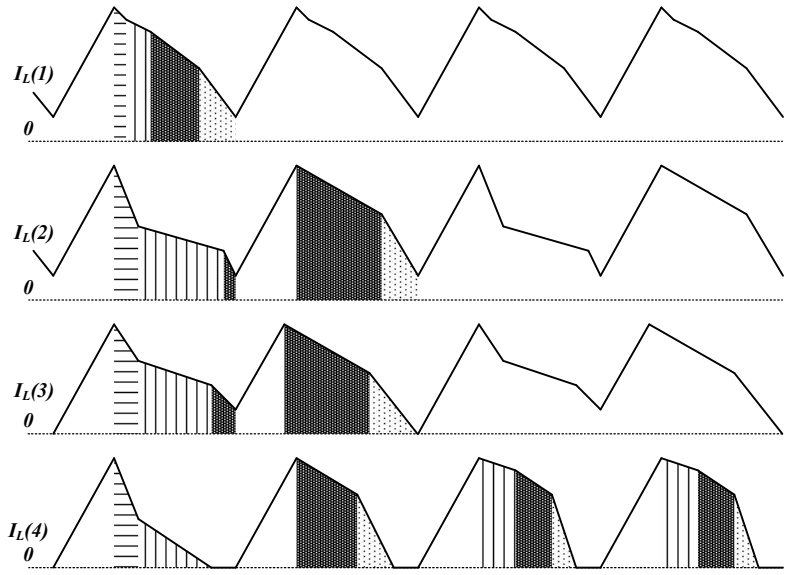


Fig. 18. The inductor current of different load conditions.

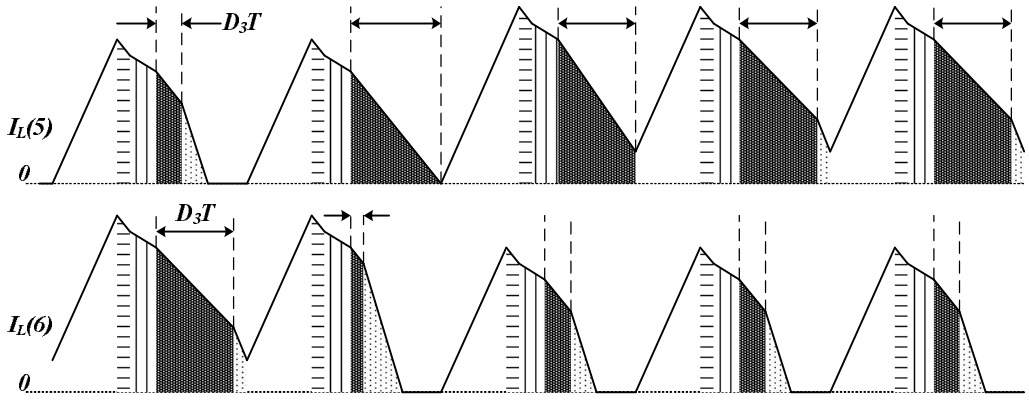


Fig. 19. An example of the load condition changes in V_{o3}.

1.3 Motivation

For previous multiple-output converter which works in PCCM or DCM with a freewheeling period, trying to handle large load currents and eliminate cross-regulation. However, PCCM operation unnecessarily dissipates energy in the resistance of inductor and freewheeling switch because of the nonzero inductor current during freewheeling time, which reduces the overall efficiency. More disadvantageously, the flexibility of the buck and boost output voltages is limited by the structure of the converter and control methodology. Thus, to simultaneously generate buck and boost output voltages, the previous work in [2] proposed the charge control method and used minimum switches to provide one buck and one boost output voltage. The SIMO converter which uses minimum the number of switches may cause charge accumulation in the inductor during unbalanced output loads. Thus, this thesis studies previous design problems and applies extended solutions to a study case. A load-dependant peak-current control SIMO converter with hysteresis mode is proposed to provide multiple buck and boost output voltages and solve the challenges of cross-regulation, power conversion efficiency, and system stability [9].

1.4 Thesis Organization

The organization of this thesis is as follows. Chapter 2 describes the minimum switch methodology of the SIMO converter with the load-dependent peak-current control technique in order to improve cross-regulation and light load efficiency. Chapter 3 describes the implementation of the proposed SIMO converter. Chapter 4 presents the power comparator and delta-voltage generators to smoothly switch the operating mode between the PWM and hysteresis modes. In Chapter 5, the experimental results show the minimized cross-regulation and performance of the proposed SIMO converter. Finally, the conclusion and future works are made in Chapter 6.

Chapter 2

Minimum Switch Number Structure with the Load-Dependant Peak-Current Control Technique

2.1 Controlling Sequence Used to Minimize the Number of Switches

The controlling sequence decides how many energy stores in inductor or delivers to different output terminals. Figure 20 shows the fundamental behavior of a conventional SIDO converter with buck and boost output voltages [2 and 12] as an example for introducing the operation of SIMO converter. Five kinds of inductor current paths, operating in six switching steps, are used to regulate the output voltages during one switching cycle. As shown in Fig. 20, paths 1 and 2 provide charge to the buck output V_{OA}. Paths 3 and 4 deliver the charge to the boost output V_{OB}. Path 6 is used to hold the charge in the inductor and to function as a freewheeling current loop. The inductor current waveform of conventional control sequence [10] is shown in Fig. 21. As description in [3 and 10], the prerequisite offset level (I_{FW}) of inductor current (I_L) trying to handle large load current and eliminate cross-regulation. However, it is obvious to clearly classify these paths into different regulation of output voltage levels. For boost output terminal V_{OB}, charge store in inductor L during path 3 while charge are delivered to boost output terminal V_{OB} with a negative inductor current slope ((V_{OB}-V_{IN})/L) during path 4 which shows in Table I. That is, switches SW_1 and SW_3 efficiently

store charge in inductor L for regulation of boost output terminal V_{OB}. Switch SW_5 are used to isolate output terminal V_{OB} from output terminal V_{OA}. For buck output terminal V_{OA}, charge not only delivers to buck output terminal V_{OA} but also store in inductor L during path 1. Moreover, the storage charge in path 1 is delivered to buck output terminal with a negative inductor current slope ((V_{IN}-V_{OA})/L) during path 2. Therefore, switches SW_1 and SW_4 are used to deliver charge to buck output terminal V_{OA} and switch SW_4 isolates buck output V_{OA} from output terminal V_{OB}. In the meanwhile, charge store in inductor L with a small positive inductor current slope ((V_{IN}-V_{OA})/L) which shows in Table I. Switches SW_2 and SW_4 deliver the storage charge in inductor L to buck output terminal V_{OA} with a large negative inductor slope (V_{OA}/L) during path 2. According to storage-charge and charge-delivering paths, all of paths can be classified into categories according to the inductor slope, which shows in Table I.

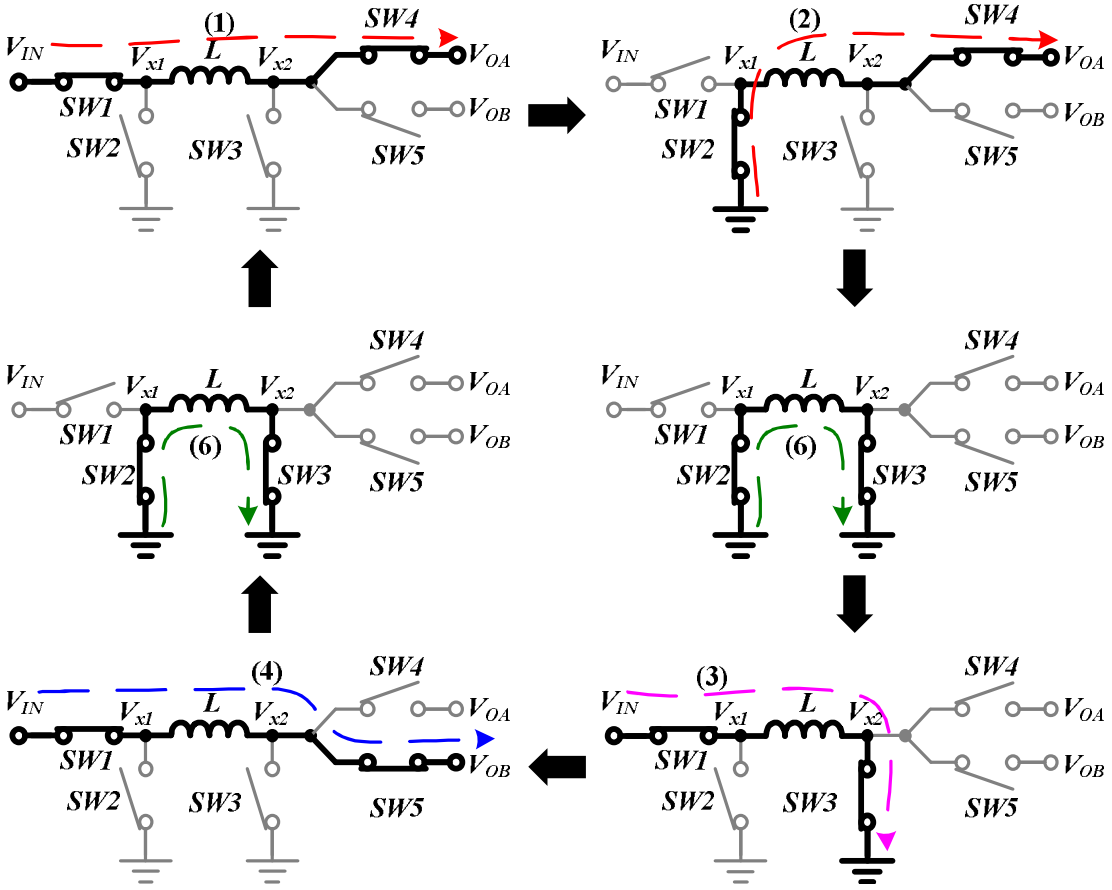


Fig. 20. The behavior of conventional SIDO converter with one buck and one boost output in [2, and 12].

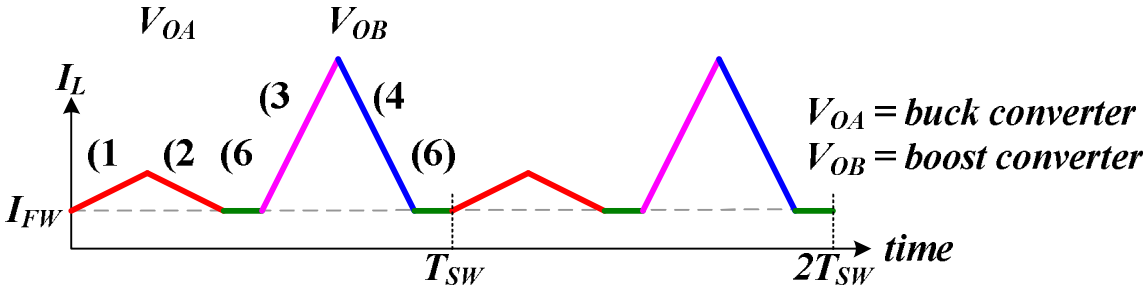


Fig. 21. The inductor current waveform of conventional control sequence [3 and 10].

Table. I. The specific of inductor current path in conventional SIDO converter.

Path	1	2	4	3	6
Function	buck	buck	boost	boost	freewheel
Sign	+	−	−	+	−
I_L Slope	$\frac{V_{IN}-V_{OA}}{L}$	$\frac{V_{OA}}{L}$	$\frac{V_{IN}-V_{OB}}{L}$	$\frac{V_{IN}}{L}$	
Switches	SW1 & SW4	SW2 SW4	SW1 & SW5	SW1 SW3	SW2 SW3
Relation	V_{OA}		V_{OB}	$V_{OA, B}$	Inside

As in previous works, the minimum number of power switches is shown in [10, 11, and 13]. These works generated the boost output voltages and controlled the storage charge of the inductor L in order to regulate the output voltages during one switching cycle. Thus, to minimize the number of power switches in the SIMO converter, the dual boost output terminals converter as shown in Fig. 22 is going to generate one buck and one boost output voltage [2]. The work in [2] provides a QC method that works in PCCM to regulate output voltage V_{OA} is lower than source voltage V_{IN} and output V_{OB} is higher than V_{IN}. According to the behavior analysis of conventional SIDO converter which is shown in Fig. 20 and Table I, paths 1, 3, and 4 must be kept in the structure of SIDO converter. Path 1 is the only one path to deliver charge to the buck output V_{OA}. Path 3 is the only choice to store charge in the inductor with a large current slope (V_{IN}/L), and path 4 is the only path to deliver charge to the boost output V_{OB}. Furthermore, the buck output voltage can only be regulated by path 1. Thus, path 2 can be removed. This means the switches SW_1 and SW_2 which are shown in Fig. 20 are

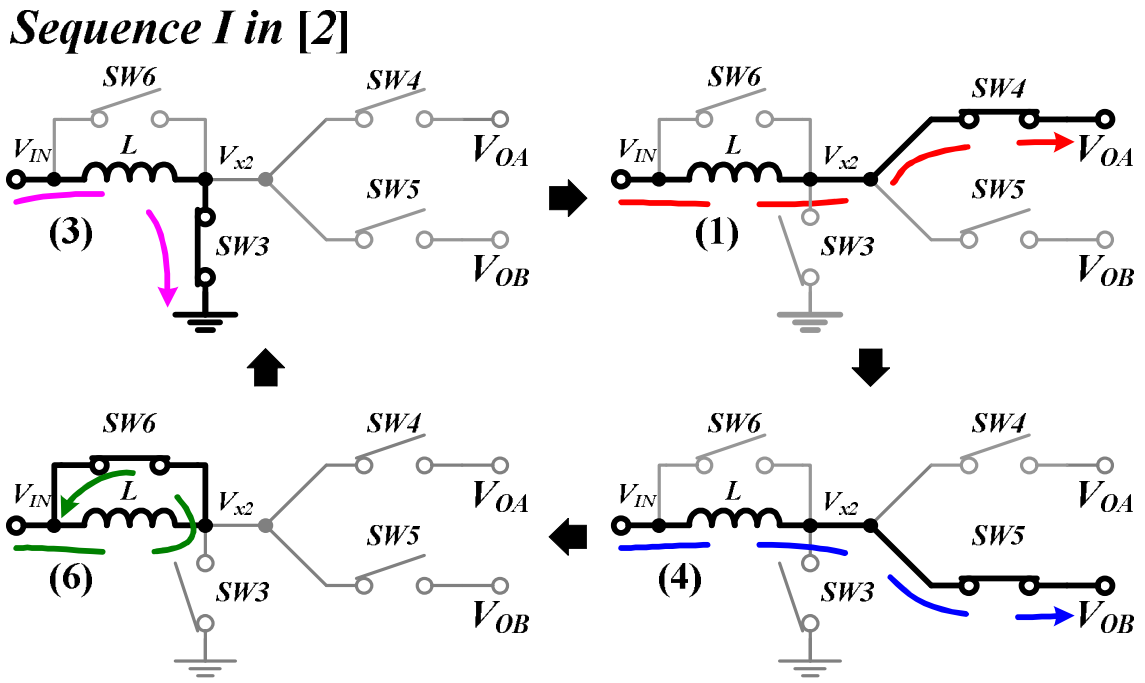


Fig. 22. The topology of minimum number of switches in [2] with one buck and one boost output voltage.

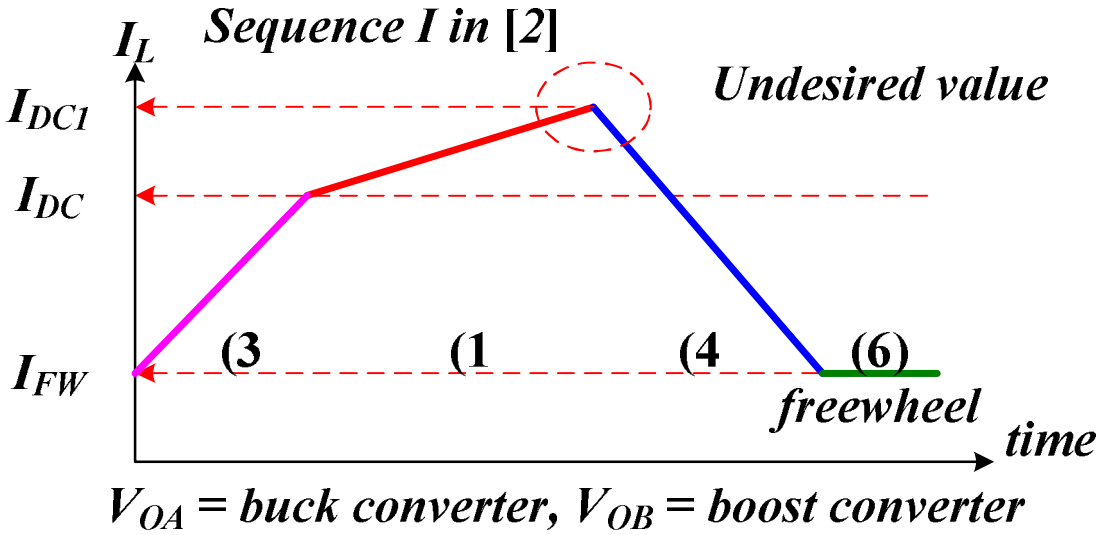


Fig. 23. The previous proposed controlling sequence-I in [2].

removed for a minimum number of switches.

After the removal of path 2, a switch SW_6 is added to generate a freewheeling current loop. A previous controlling sequence-I in [2] is depicted for one buck output V_{OA} and one boost output V_{OB} in Fig. 23. At the beginning of every switching cycle, path 3 which is

illustrated in Fig. 22 stores charge of inductor with a positive current slope (V_{IN}/L) from the freewheeling current level (I_{FW}) to the pre-defined and fixed current level (I_{DC}). Then path 1 is selected to deliver charge with a positive current slope ((V_{IN}-V_{OA})/L) to the buck output V_{OA}, and the inductor current level (I_L) is increased to a value (I_{DC1}), which is dependent on the load condition (I_{OA}) of the buck output V_{OA} at the same time. After buck output V_{OA} operation, the boost output V_{OB} draws the charge with a negative current slope ((V_{OB}-V_{IN})/L) from path 4 and the inductor current drops back to the freewheeling current level (I_{FW}). Finally, the freewheeling current level (I_{FW}) of inductor L is kept by path 6.

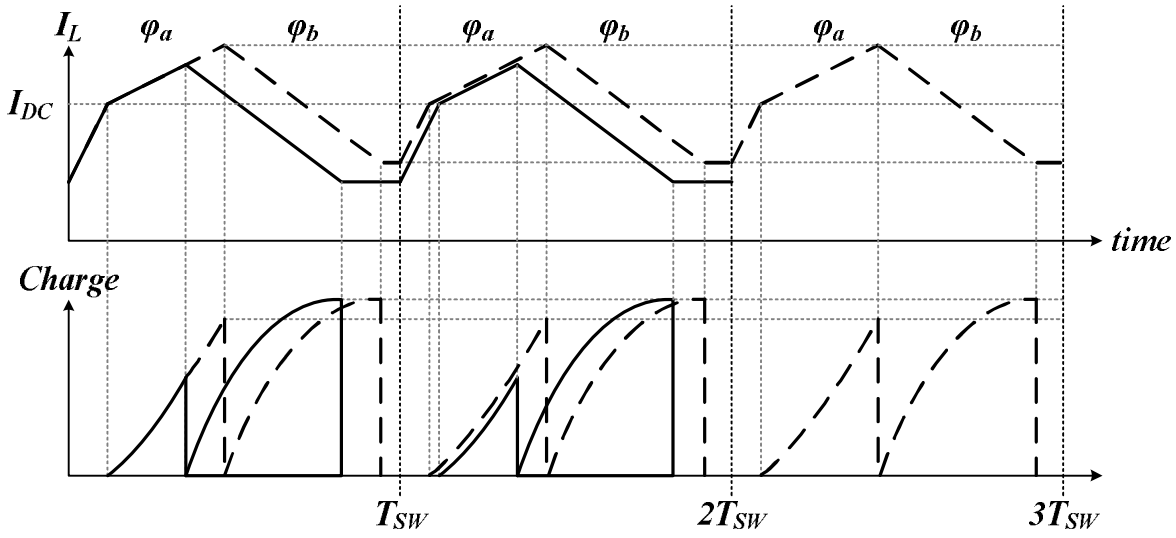


Fig. 24. The cross-regulation and inductor current waveform of SIDO converter when the load changes from light to heavy at output terminal V_{OA} in [2].

Furthermore, the QC method can minimizes the cross-regulation as is demonstrated in Fig. 24. Suppose that the inductor current (I_L) required by load current (I_{OA}) of buck output terminal V_{OA} suddenly increases, the duration of time interval (φ_a) will then increase so that more inductor current (I_L) can be delivered to buck output V_{OA}. As the load condition for output terminal V_{OB} remains unchanged, the output of the corresponding error amplifier remains the same. Although the whole duration of time interval (φ_b) is shifted to the right, the same amount of charge is still delivered to boost output V_{OB}. The freewheeling level (I_{FW}) is

then higher at the start of the next period, and the inductor current (I_L) reaches the pre-defined and fixed current level (I_{DC}) sooner. Hence, the duration of time interval (φ_a) is shifted left, so as the subsequent time interval (φ_b). In the third period, the inductor current (I_L) assumes the new profile as in the second period and a new steady state is reached. All along, the inductor current (I_L) delivered to boost output terminal V_{OB} is not affected, and cross regulation is minimized.

However, the inefficient performance is the major disadvantage since the inductor current (I_L) is increased to a highly undesired value if the buck output V_{OA} is derived during heavy load condition and the boost output V_{OB} is derived during light load condition. The other drawback is the predefined and fixed current level (I_{DC}) that contributes to the highly freewheeling current (I_{FW}) and the serious decrease in power conversion efficiency in the light load condition. Furthermore, the highly undesired current value (I_{DC1}) of the inductor L also causes the serious cross-regulation in the output terminals since the energy accumulates in the inductor L. As a result, there is difficulty in ensuring the conversion efficiency and minimum cross-regulation of the controlling sequence-I [2]. Furthermore, when the load condition which is shown in Fig. 22 of the buck output V_{OA} is larger than that of the boost output V_{OB}, the storage charge of the inductor L accumulates without a releasing path. The highly current level (I_L) appears in the inductor L and results in un-regulation problem.

To address these issues, a new proposed controlling sequence-II with the load-dependent peak-current control (LDPCC) technique is presented as illustrated in Fig. 25. In the beginning of controlling sequence-II, path 1 is used to simultaneously regulate the buck output terminal V_{OA} and store the charge with a positive current slope ((V_{IN}-V_{OA})/L) in the inductor L, since the voltage level of output terminal V_{OA} is smaller than that of supply terminal V_{IN}. Path 1 expires; the inductor current (I_L) then rapidly increases with a positive current slope (V_{IN}/L) to the LDPCC level (I_{peak}) by path 3. Then controlling sequence-II switches to path 4 to draw the charge of the inductor L with a negative current slope

($(V_{OB}$-$V_{IN})/L$) to boost the output terminal V_{OB}; after which, it drops back to the inductor current to a freewheeling current level (I_{FW}). Finally, the inductor current level (I_L) is kept by path 6. Since the current level (I_{peak}) increases during heavy load condition and decreases during light load condition, the power dissipation during the freewheeling loop can be minimized. Due to the storage charge of the inductor L in path 1 having been fully taken into account in the proposed controlling sequence-II, the highly undesired current value (I_{DC1}) in previous work [2] is eliminated. Thus, power conversion efficiency and cross-regulation can be improved in the proposed controlling sequence-II. However, when the load condition of output terminals V_{OA} and V_{OB} operate in unbalance output load condition which is the buck output V_{OA} is derived during heavy load condition and the boost output V_{OB} is derived during light load condition, the energy still accumulates in the inductor L without releasing path. Other words, when storage charge during path 1 is higher than releasing charge during path 4, the value of inductor current level (I_L) will not able to decrease inductor current level (I_L) below the LDPCC current level (I_{peak}) in every switching cycle. Thus, the inductor current accumulation appears during unbalance output load condition**.**

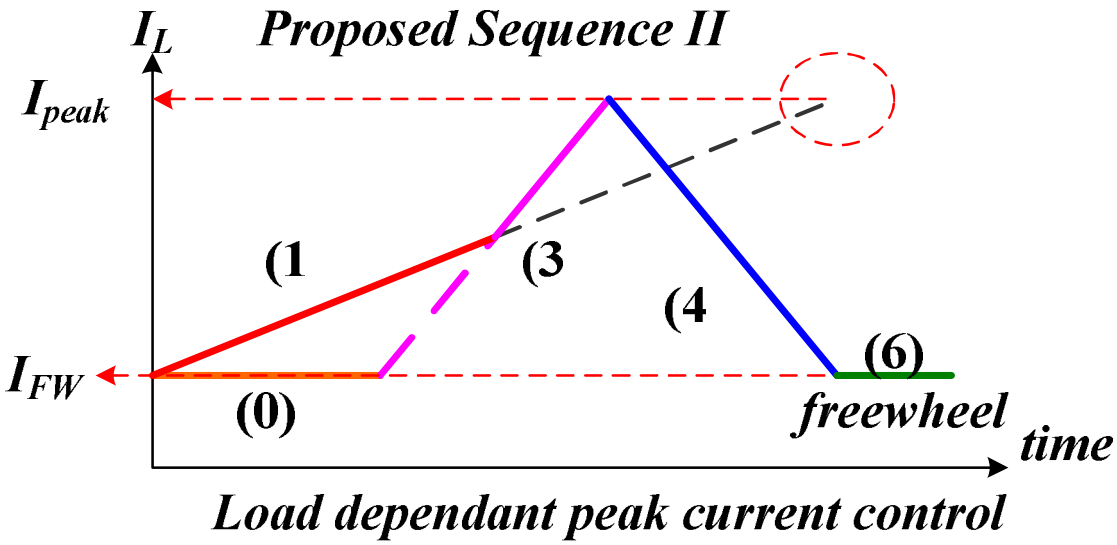


Fig. 25. The proposed sequence-II with LDPCC technique which eliminates the undesired value of inductor current level.

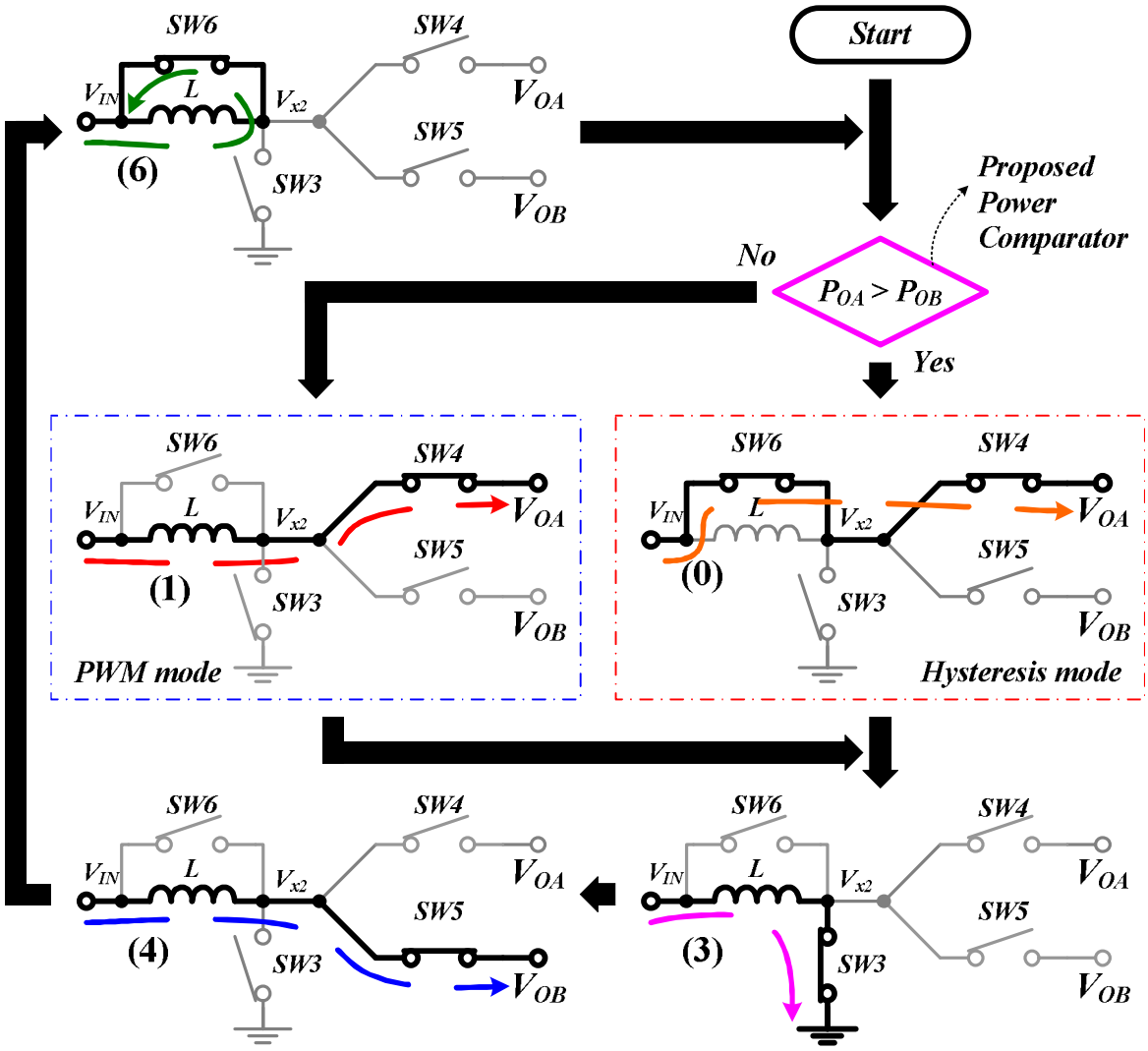


Fig. 26. The proposed controlling sequence and path 0 of the hysteresis mode control.

In order to address the inductor current (I_L) accumulation in the structure of minimum power switches, a new energy delivering path, which names as path 0 and illustrates in Fig. 26, is proposed to eliminate the energy accumulation issue while the condition that storage charge during path 1 is higher than consumption charge during path 4. Therefore, a power comparator is proposed to detect the output load condition. If the output power of output terminal V_{OA} is smaller than that of output terminal V_{OB}, the proposed controlling sequence-II is use to regulate voltage level of output terminals. Oppositely, when the output power of output terminal V_{OA} is larger than that of output terminal V_{OB}, the proposed path 0 is enabled to eliminate current accumulation issue. When path 0 is enabled, switches SW_4 and SW_6 are

closed. A current path is created through switches SW_4 and SW_6 and used to regulate output terminal V_{OA}. Since the path 0 passes inductor L, the voltage of output V_{OA} is regulated by a hysteresis voltage window. Therefore, the proposed path 0 also calls as hysteresis mode control. Since the proposed hysteresis mode control is used to regulate voltage level of output V_{OA} and to limit regulating ripple of output V_{OA}, the inductor current waveform (I_L) which operates in hysteresis mode is shown in Fig. 25. At the beginning of every switching cycle, hysteresis mode is enabled. Since inductor current (I_L) flows through switches SW_4 and SW_6 to output terminal V_{OA}, the energy does not accumulate in the inductor L. Thus, inductor current level (I_L) does not increase until path 0 expires. The duration of path 0 is determined by hysteresis voltage window and the on-resistance of switches SW_4 and SW_6. Then, path 3 turns on, switches SW_4 and SW_6 is opened, and switch SW_3 is closed. The inductor current (I_L) is increased with a positive current slope (V_{IN}/L). When inductor current (I_L) raises to LDPCC level (I_{peak}), path 3 expires and then switch SW_3 turns off. Then, path 4 and switch SW_5 turns on, the storage charge, in form of inductor current (I_L), ramp down with a negative current slope ((V_{OB}-V_{IN})/L), the duration of path 4 is determined by the amount of delivering charge. Finally, the residue current level (I_{FW}) is held by path 6. Owing to the output voltage of output terminal V_{OA} is regulated by a hysteresis voltage window during path 0, the special operation which is named as hysteresis control mode caused a larger output ripple and sacrificed power conversion efficiency in the proposed path 0. However, as the analysis of the hysteresis control mode, the energy accumulation and cross-regulation during the unbalanced load condition can be eliminate through path 0.

2.2 LDPCC Method for Improving Light-Load Efficiency, Stability, and Cross-Regulation

The inductor waveform (I_L) represents status of energy storage and the order of system.

Four inductor waveforms are depicted in Fig. 27~30. At first, the inductor current waveform (I_L) of DCM is shown in Fig. 27. The characteristic of inductor current (I_L) is that current level decreases to zero before the end of each switching cycle. The order of the system is equal to one. That is, only one low-frequency pole exists in the close loop. When load current changes from light to heavy load condition, the peak value of inductor current (I_L) is increased for storage more energy. There is a maximum peak current level existed, because of the disappearance of zero-current condition and thus a maximum power limitation exists in the operation of DCM. As a result, the characteristic of inductor current waveform (I_L) changes from DCM to CCM operation as shown in Fig. 28 when the sudden power is larger than maximum power limitation of DCM operation. The order of system becomes two and the

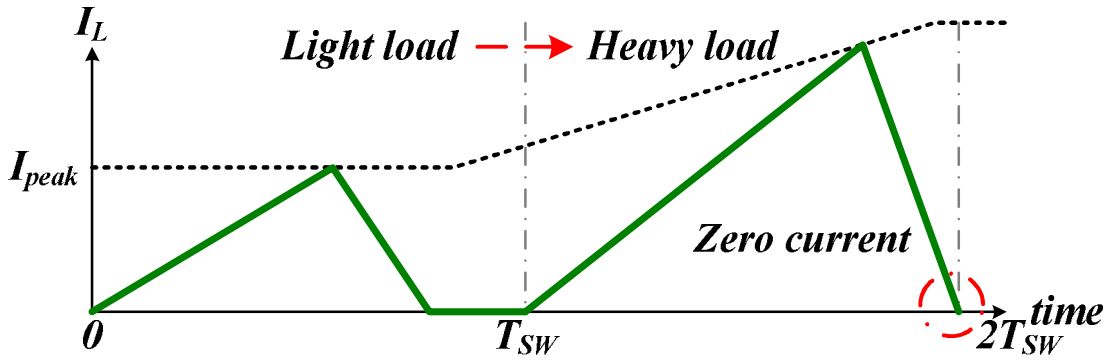


Fig. 27. The inductor current waveform in DCM operation when the load current changes from light to heavy load conduction.

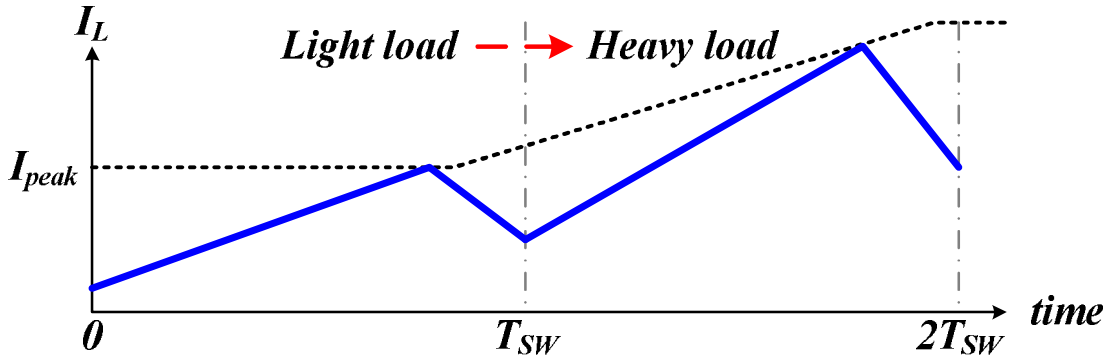


Fig. 28. The inductor current waveform in CCM operation when the load current changes from light to heavy load conduction.

compensation of system needs a complicated compensation like proportional integral differential (PID) compensator to make sure large low-frequency gain and suitable phase margin. Another serious problem is disappearance of isolation period which is zero-current stage works as freewheeling stage. Since disappearance of isolation period may cause worse cross regulation. The cross regulation and instability of system comes from the charge accumulation of inductor. A summary of the two operation modes is that disadvantage of the DCM operation is maximum power limitation while the disadvantage of CCM operation is charge accumulation of inductor *L*.

The PCCM operation was proposed to improve the disadvantages in DCM and CCM operation [10]. The PCCM technique sets a constant inductor current DC level to store enough energy in inductor as depicted in Fig. 29. Thus, the order of system is similar to that of DCM operation while the maximum power delivered by PCCM operation is larger than that of DCM operation. That is, the order of system is one, and thereby simplifying compensation skill. After the usage of P-I compensator, bandwidth can be extended to have better performance for transient response. Nevertheless, the advantages of the PCCM operation only exist when freewheeling stage exists at end of each switching cycle. Once disappearance of freewheeling stage happens when load current exceeds maximum power limitation or when sudden load current changes from light to heavy load level, the stability and minimized cross regulation isn't guaranteed since the order of system becomes two. The solution of scenario is that pre-defined and fixed inductor current level (I_{DC}) is required large enough to provide maximum power to all output terminals. That is, the value of the pre-defined and fixed inductor current level (I_{DC}) causes the power conversion lower than that by CCM or DCM operation at light load condition since the freewheeling stage with high inductor current occupies the most period of switching cycle. Thus, the light-load efficiency is decreased. As well, the power conversion efficiency at light-load determines usage time of battery for portable devices.

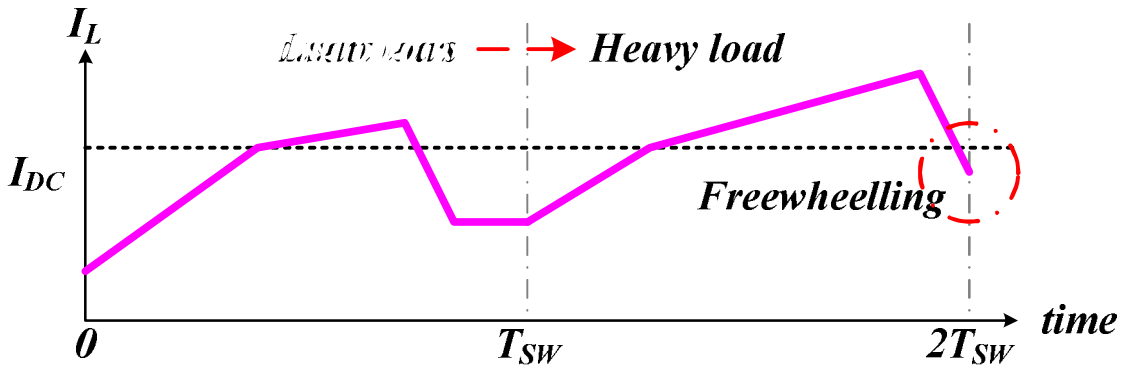


Fig. 29. The inductor current waveform in PCCM operation of work [2] when the load current changes from light to heavy load conduction.

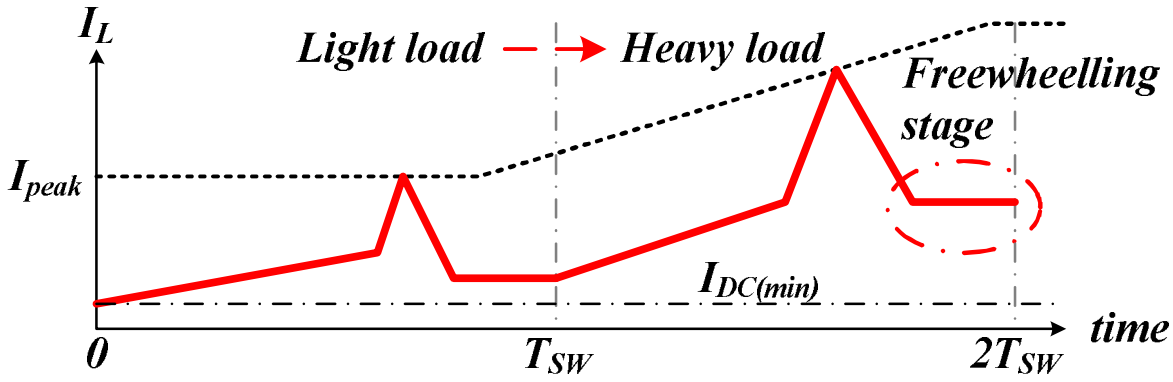


Fig. 30. The inductor current waveform in proposed LDPCC technique operation when the load current changes from light to heavy load conduction.

To enhance the power conversion efficiency at light-load becomes most important issue in today's portable devices. The LDPCC technique is needed to effectively improve the power conversion efficiency at light-load condition. As illustrated in Fig. 30, the LDPCC technique is proposed to adaptively store suitable energy in inductor *L*. When load current changes from light to heavy load condition, the LDPCC current level (I_{peak}) is raised to a higher current level to store enough charge in inductor *L*. On other hand, when the load current becomes small, the LDPCC current level (I_{peak}) will be decreased to a small current level for ensuring high power conversion efficiency at light load condition. Besides, a minimum inductor current level ($I_{DC(min)}$) is defined to prevent output terminal from large transient drop voltage. Thus, the LDPCC technique can have advantages of simple compensation, large driving

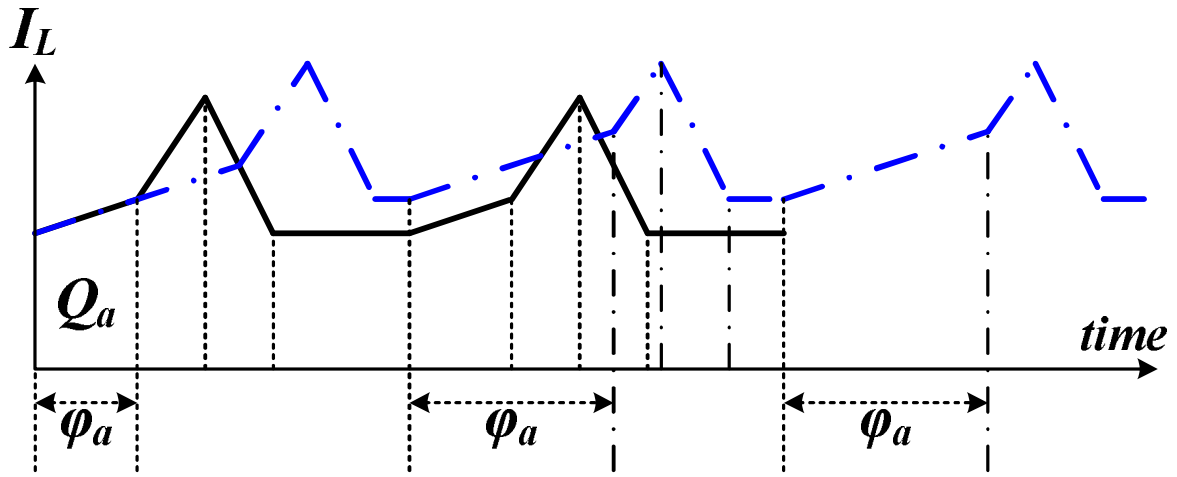


Fig. 31. The inductor current variation when the load condition changes from light to heavy in output terminal V_{OA}.

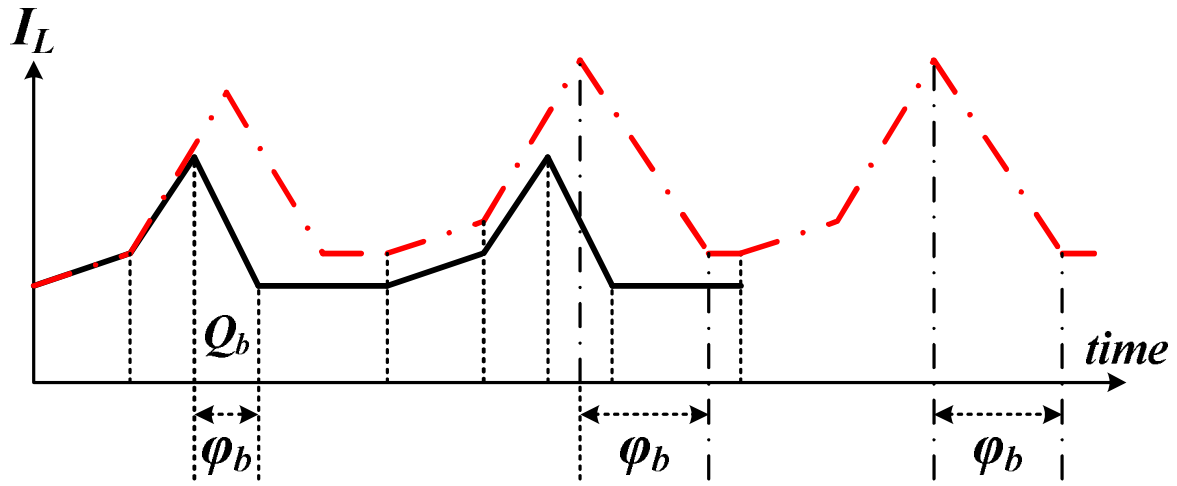


Fig. 32. The inductor current variation when the load condition changes from light to heavy in output terminal VOB.

capability, and high power conversion efficiency at light-load condition. The LDPCC technique can minimizes the cross-regulation, which looks alike the QC method in [2], as is demonstrated in Fig. 31. Suppose that the current required by output terminal V_{OA} suddenly increases, the duration of time interval (φ_a) will then increase so that more current can be delivered to output terminal V_{OA}. The inductor current (I_L) then reaches the LDPCC level (I_{peak}) sooner. As the load for output terminal V_{OB} remains unchanged, the output of the corresponding error amplifier remains the same. Although the whole duration of time interval

(φ_b) is shifted to the right, the same amount of charge is still delivered to output terminal V_{OB}. The LDPCC level (I_{peak}) is then higher at the start of the next period. Hence, time interval (φ_a) is extended left, so as the subsequent time interval (φ_b). In the third period, the inductor current (I_L) assumes the new profile as in the second period and a new steady state is reached. All along, the current delivered to output terminal V_{OB} is not affected, and cross-regulation is minimized. Similarly, Fig. 32 demonstrates the minimized cross-regulation in that output load current required by output terminal V_{OB} suddenly increases.

2.3 System Architecture of SIMO DC-DC Converter

According to the proposed controlling sequence-II and the LDPCC technique, the architecture of the proposed SIMO converter is illustrated in Fig. 33. As previous analysis of switch number, the minimum number of switch is shown in the top of Fig. 33. The main switch SW_N and freewheeling switch SW_F construct paths 3 and 6 of controlling sequence-II. Switches SW_{K1}~SW_{Kn} and SW_{T1}~SW_{Tm} are used to extend and isolate output terminals V_{OK1}~V_{OKn} and V_{OT1}~V_{OTm}. Therefore, the total number of power switch is equal to the number of output terminals pluses two. Output voltages are detected by error amplifier array via output divider array. The output signals V_{EK1}~V_{EKn} and V_{ET1}~V_{ETm} of error amplifier array connect to the input terminals of LDPCC circuit for generating load dependant peak current signal V_{Ipeak}. Moreover, the LDPCC circuit also generates current signals I_{EK1}~I_{EKn} and I_{ET1}~I_{ETm} which are used to be discharging current sources in charge reservation circuit. Since the charge reservation circuit uses the output current I_{SEN} of current sensor and the LDPCC current signals I_{EK1}~I_{EKn} and I_{ET1}~I_{ETm} as charging and discharging current sources respectively, the storage charge on indicative capacitors C_{IK1}~C_{IKn} and C_{IT1}~C_{ITm} of charge reservation circuit can fully depend on inductor current (I_L) and load variations. Therefore, the voltages V_{IK1}~V_{IKn} and V_{IT1}~V_{ITm} on indicative capacitors C_{IK1}~C_{IKn} and C_{IT1}~C_{ITm} are used to

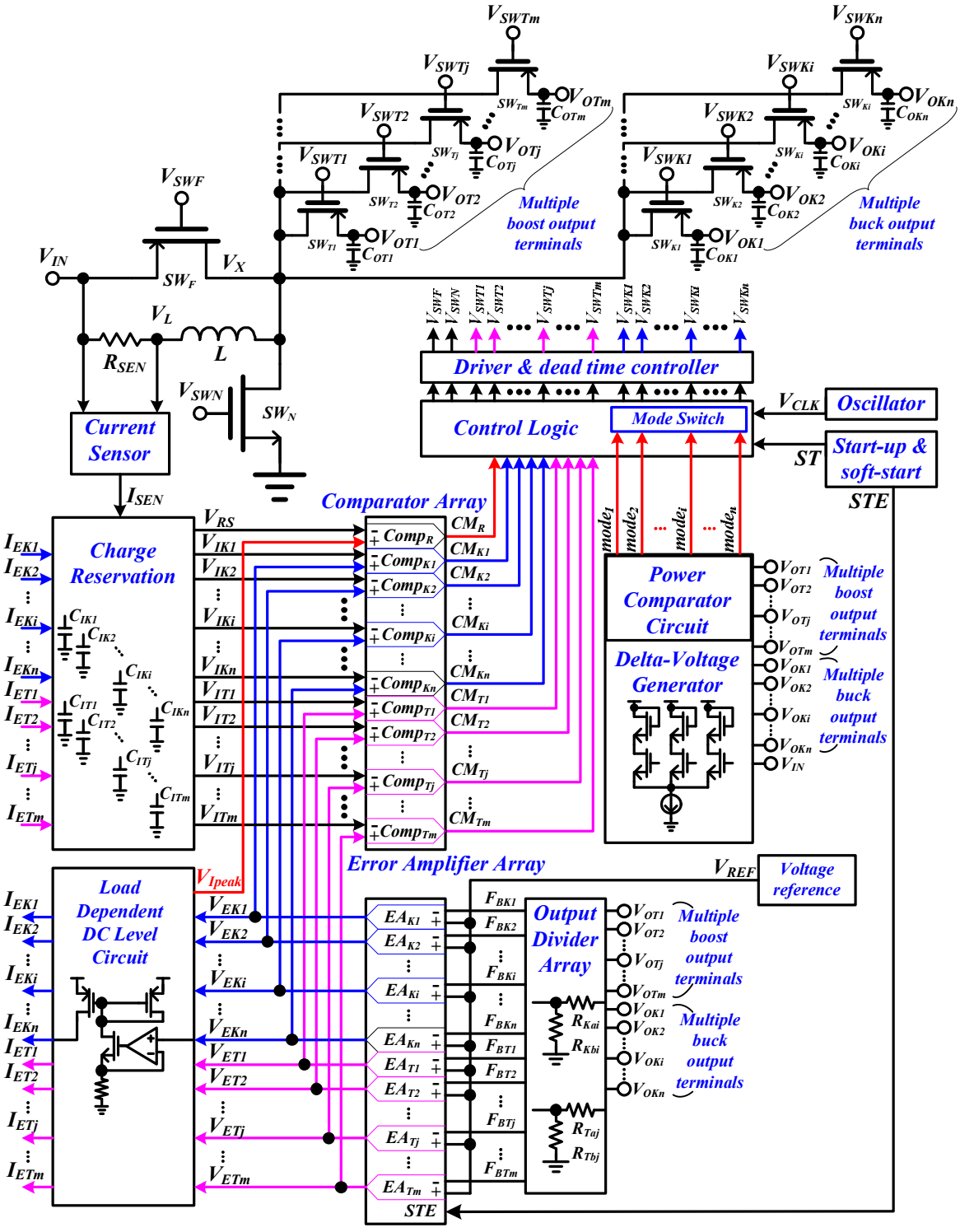


Fig. 33. The proposed load-dependent peak current control SIMO DC-DC converter with hysteresis mode for high power conversion efficiency and minimum cross regulation.

compare with output signals V_{EK1}~V_{EKn} and V_{ET1}~V_{ETm} of error amplifier array for deciding the energy delivering duration of each output terminal. The time interval of path 3 is decided

by the comparison of current signal V_{RS} and LDPCC signal V_{Ipeak}. The output signals CM_R, CM_{K1}~CM_{Kn}, and CM_{T1}~CM_{Tm} of comparator array are used to enable control sequence-II in control logic circuit and generate the MOSFET's driving signals V_{SWF}, V_{SWN}, V_{SWK1}~V_{SWKn}, and V_{SWT1}~V_{SWTm} via dead-time controller and driver. For current accumulation issue, power comparator and delta-voltage generator continuously monitor the voltage deviation of output terminals and generate output signals $mode_1$~$mode_n$ to control mode switch of control logic.

Chapter 3

Design and Analysis of Proposed SIMO DC-DC Converter

3.1 LDPCC Decision Circuit

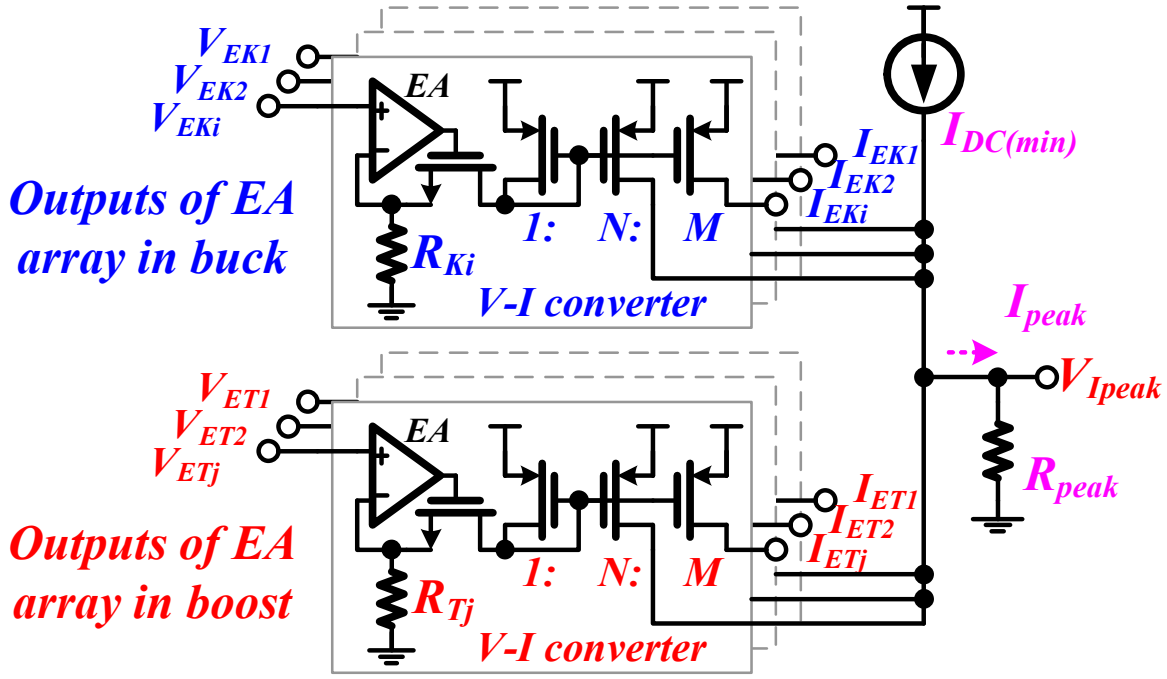


Fig. 34. The implementation of the proposed LDPCC circuit which dynamically adjusts the peak current level according to the value of load current.

As previous discussion in [2], the peak inductor current level (I_{DC}) is used to provide pre-charged energy in inductor L for large load variations. A high value of peak current has sufficient capability for driving large load condition. However, the disadvantage of high peak current level (I_{DC}) is inefficient power conversion efficiency at light load condition. Oppositely, a lower value of peak current has good power conversion efficiency at light load

condition while converter needn't high capability to handle large load current step. Therefore, the peak current level must adjust with variation of load current. Besides, peak current level also affects cross-regulation in SIMO converter owing to the over-storage charge in inductor *L*. To improve the power conversion efficiency at light loads and to reduce the effect of cross-regulation, a peak current decision circuit is depicted in Fig. 34. Where the suffix *i* is from *1* to *n* for buck output terminals and the suffix *j* is from *1* to *m* for boost output terminals. The peak current decision circuit dynamically adjusts peak current level V_{Ipeak} according to variation of output load conditions. All output voltages of feedback error amplifiers are converted current signals by the voltage to current (V-I) converters. Each V-I converter generates two current signals with a conversion ratio (*1: N: M*). The current signals I_{EK1}~I_{EKn} and I_{ET1}~I_{ETm} (where the suffix index *i* is 1 to *n* for buck output terminals and the suffix index *j* is 1 to *m* for boost output terminals) are used to work as discharging currents of the charge reservation circuit. The other current signals are summed to generate the LDPCC current (I_{peak}), which varies with load currents. Furthermore, to avoid the zero inductor peak current, a minimum peak inductor current is set by a current source $I_{DC(min)}$. The non-inverting input of the comparator is decided by the voltage signal V_{Ipeak}, which is generated by flowing two current signals (I_{peak}) and $I_{DC(min)}$ through the resistor R_{peak}. The value of LDPCC level V_{Ipeak} is determined by (19).

$$V_{Ipeak} = R_{peak}\left(I_{Peak} + I_{DC(\min)}\right) \tag{19}$$

The input voltages of the V-I converters are V_{EK1}~V_{EKn} and V_{ET1}~V_{ETm} from the error amplifier array that indicates the load conditions of all multiple buck and boost output terminals. The value of peak current decision circuit varies with the variation of load current. At very light load, the value is kept at value of $I_{DC(min)}$ and thus current level (I_{peak}) of freewheeling stage can be reduced compared to that with the fixed inductor current level (I_{DC}) in conventional design [2]. That is, the light-load efficiency can be improved without over-storage charge in

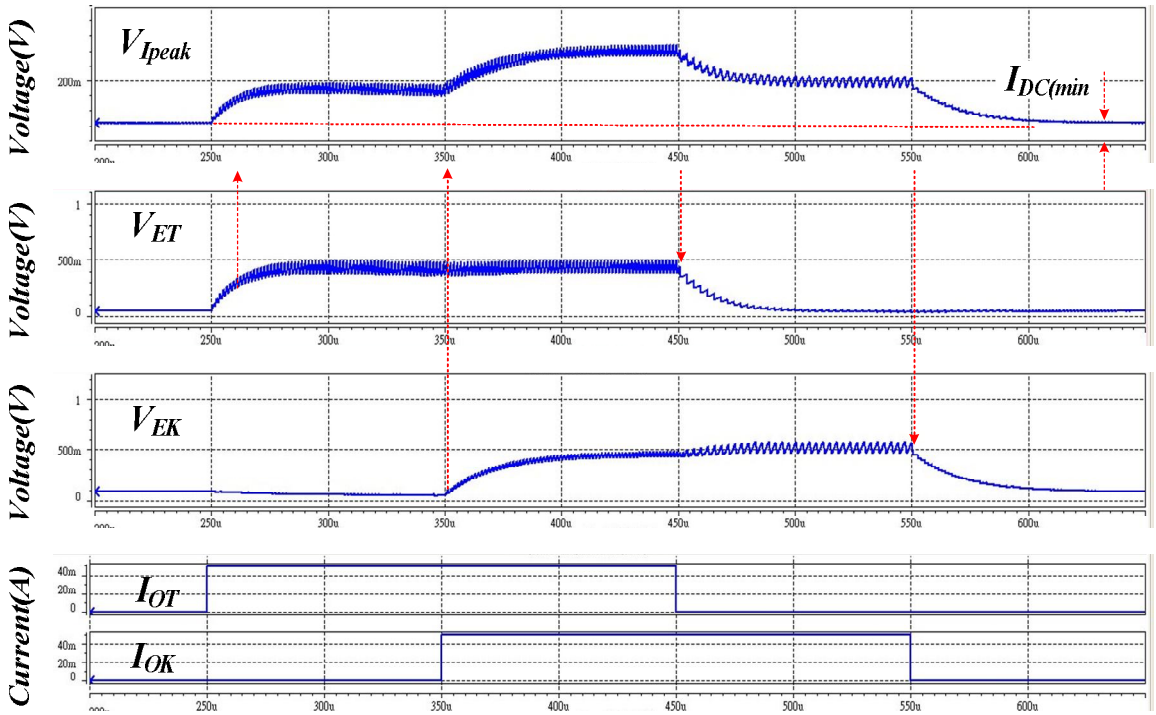


Fig. 35. The transient simulation result of proposed LDPCC circuit which uses dual-error output signals as an example.

the inductor L. For a dip in one of the output terminals due to an increase in load current, for example, the control system increases the duty ratio, which in turn indirectly causes an increased peak inductor current level V_{Ipeak}. The energy stored in the inductor L is gradually increased to minimize cross-regulation due to the LDPCC level at heavy load conditions. Similarly, the period of freewheeling stage occupies little duration of every switching cycle. The order of the system is still kept as one, and the power dissipation is always kept small. Therefore, the P-I compensator can ensure the stability of the system, and the heavy-load power conversion efficiency can be kept high. The transient simulation result of LDPCC circuit, which uses dual-error output signals as an example, is shown in Fig. 35. While the output load condition (I_{OT}) suddenly changes to heavy load condition, the output signal (V_{ET}) of error amplifier increases to a rated value for generating LDPCC level V_{Ipeak}. When the output load condition (I_{OK}) is increase at the same time, the output signal (V_{EK}) of error amplifier also increases the LDPCC level V_{Ipeak}. Therefore, the LDPCC level V_{peak} depends on

output load conditions and the energy stored in the inductor L is gradually increased to minimize cross-regulation and handle higher power capability due to the LDPCC level at heavy load conditions.

3.2 Current Sensor and Charge Reservation Circuits

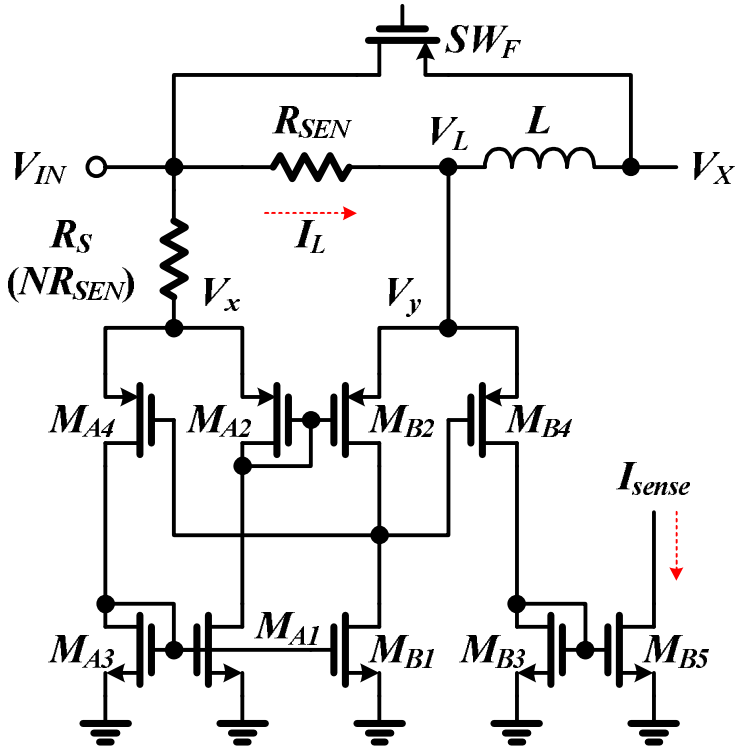


Fig. 36. The current sensor of [2 and 3] is composed by a fully symmetrical matching structure.

The current sensor shown in Fig. 36 [2 and 3] has a proportional register R_S which is N times of the sensing resistor R_{SEN}. The current sensor is composed by a fully symmetrical matching structure. Sufficient accuracy and high bandwidth is used to follow output current variations. To achieve the LDPCC technique, the current sensor cannot be turned off during the whole switching cycle. Thus, the freewheeling power MOSFET as illustrated in Fig. 36 is connected between the input power source V_{IN} and the node V_X at the expense of power

conversion efficiency during the freewheeling stage. The current sensor is realized by the matched PMOS transistors M_{A2} and M_{B2} which are used to enforce the same voltage at node V_x and node V_y. The PMOS transistors M_{A2} and M_{B2} are biased in the saturation region. Two small and equal biasing current force the PMOS transistors M_{A2} and M_{B2} to have the same threshold voltage. Self-bias loop is composed by transistors M_{A4}, M_{A3}, M_{A1}, and M_{B1}. Sensing current is generated via transistor M_{B4}. The simulation result of current sensor is shown in Fig. 37 and a test pattern of inductor current (I_L) is given by piecewise-linear (PWL) waveform in HSPICE simulation tool. The sensing signal converts the current scale (I_{sense}) into voltage scale (V_{RS}) for detecting LDPCC level V_{Ipeak}. The mirrored current signal (I_{sense}) is used to charge the indicative capacitors C_{IK1}~C_{IKn} and C_{IT1}~C_{ITm} of charge reservation circuit which is shown in Fig. 38.

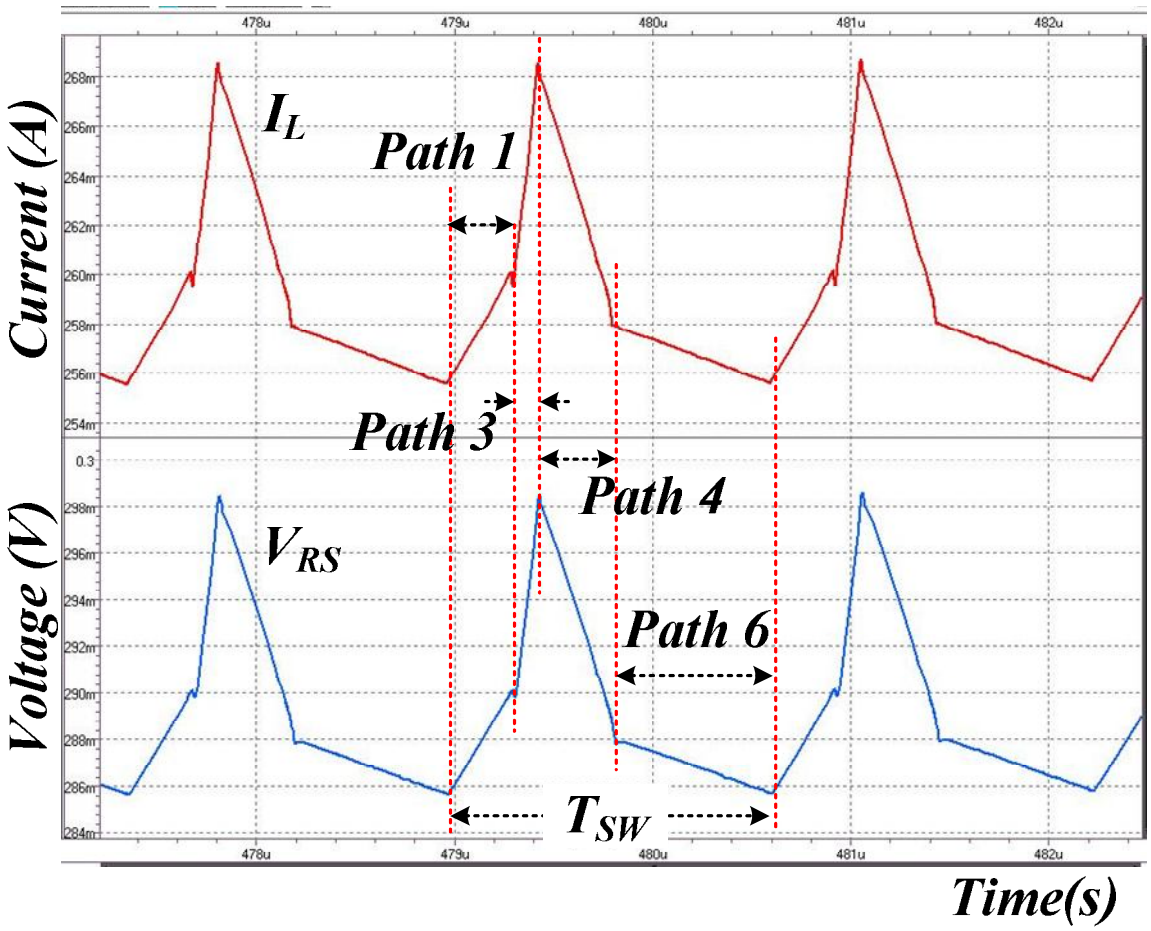


Fig. 37. The simulation result of current sensor.

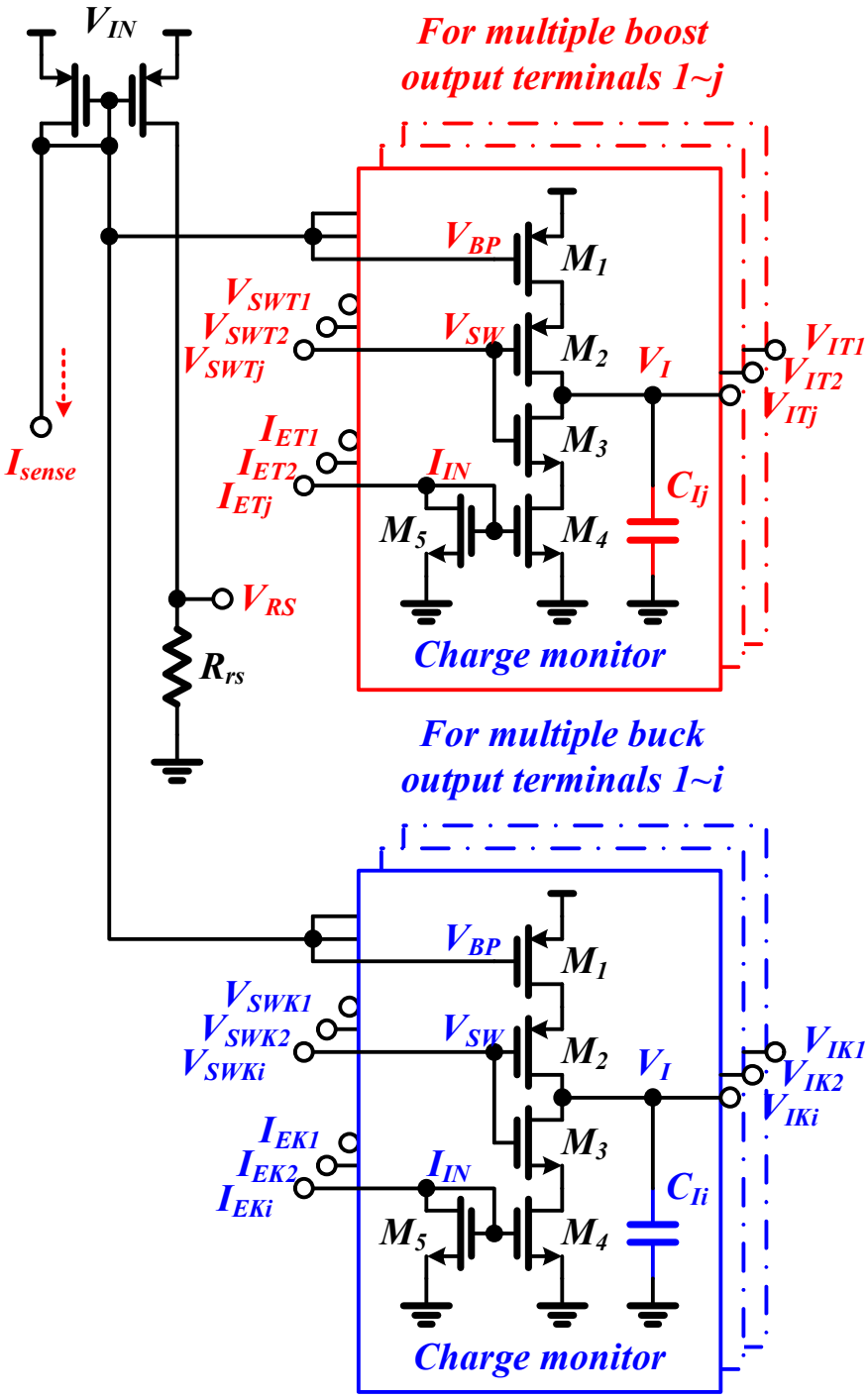


Fig. 38. The proposed charge reservation circuits and charge monitor circuit for reducing output ripple.

The architecture of the charge reservation circuit is shown in Fig. 38. The sensing current (I_{sense}) is converted to the voltage V_{RS}, which is used to compare with the LDPCC level V_{Ipeak} as illustrated in Fig. 33. The sensing current (I_{sense}) is also used to determine the individual

duty cycle of each buck or boost output terminal. Thus, there are n and m charge monitoring circuits in the charge reservation circuit. The indicative capacitors C_{IK1}~C_{IKn} and C_{IT1}~C_{ITm} are used to monitor the buck and boost output voltages, respectively. The charge monitor circuit in the sub-block is also shown in Fig. 38. When the voltage of driving signal V_{SW} is set to low, sensing current (I_{sense}) flows into indicative capacitor C_I to indicate the energy delivering condition of one of buck or boost output voltage. Once the voltage of driving signal V_{SW} is changed from low to high state, the discharging current (I_{in}), which comes from the LDPCC circuit, starts to discharge indicative capacitor C_I. Thus, the voltage ripples ΔV_{IK1}~ΔV_{IKn} and ΔV_{IT1}~ΔV_{ITm} on indicative capacitors C_{IK1}~C_{IKn} and C_{IT1}~C_{ITm} can monitor the status of the buck and boost output voltages. As a result, the duty cycle can be determined by the voltage V_I on indicative capacitor C_I and the output voltage V_{EKi} (or V_{ETj}) of error amplifier array after the operation of comparator array in Fig. 33.

Assume that the value of voltage ripples ΔV_{IKi} and ΔV_{ITj} is k_{Ki} and k_{Tj} times that of output ripples ΔV_{OKi} and ΔV_{OTj} for the buck output terminal i and boost output terminal j, where the suffix i is *1* to n for buck output terminals and the suffix j is *1* to m for boost output terminals. The buck and boost output ripples ΔV_{OKi} and ΔV_{OTj} express as (20) by voltage ripples ΔV_{IKi} and ΔV_{ITj} on the indicative capacitors C_{IKi} and C_{ITj} in charge reservation circuit.

$$\Delta V_{OKi} = \frac{1}{k_{Ki}} \Delta V_{IKi} \quad \text{and} \quad \Delta V_{OTj} = \frac{1}{k_{Tj}} \Delta V_{ITj} \tag{20}$$

The value of voltage ripples ΔV_{IKi} and ΔV_{ITj} are set within the input common-mode range of the comparator array in Fig. 33. Besides, the value of inductor current (I_L) is N times that of sensing current (I_{sense}), which is the sensing current for buck and boost output terminals. Thus, the values of indicative capacitors C_{IKi} and C_{ITj} in the charge reservation circuit are given by (21) and (22), respectively.

$$C_{IKi} = \frac{I_{sense}}{I_L} \frac{1}{k_{Ki}} C_{OKi} = \frac{1}{N k_{Ki}} C_{OKi}, \text{ for buck output } i \tag{21}$$

$$C_{ITj} = \frac{I_{sense}}{I_L}\frac{1}{k_{Tj}}C_{OTji} = \frac{1}{Nk_{Tj}}C_{OTj}\text{, for boost output } j \tag{22}$$

In order to generate the discharging current sources I_{EKi} and I_{ETj} of LDPCC circuit proportional to load current condition in Fig. 34, the values of the resistors R_{K1}~R_{Kn} and R_{T1}~R_{Tm} in the V-I converters must depend on output load condition. As a result, the charge reservation circuit in the SIMO DC-DC converter can accurately discharge storage charge in indicative capacitors C_{IK1}~C_{IKn} and C_{IT1}~C_{ITm}. The discharging current sources I_{EKi} and I_{ETj} are proportional to V_{EKi}/R_{Ki} and V_{ETj}/R_{Tj} for buck and boost output terminals, respectively. Considering parameters in buck output terminals, the value of voltage ripple ΔV_{IKi} can be described as (23).

$$\Delta V_{IKi} = \Delta I_{EKi}\frac{t_{Ki}}{C_{IKi}} = \frac{\Delta V_{EKi}}{R_{Ki}}\frac{t_{Ki}}{C_{IKi}} \tag{23}$$

Besides, the output voltage V_{EKi} of error amplifier array which is composed by operational trans-conductance amplifier (OTA) can be express as (24) by adopting equation (21).

$$V_{EKi} = G\left(V_{REF} - \beta_{Ki}V_{OKi}\right) = G\left(V_{REF} - \beta_{Ki}\frac{I_L t_{Ki}}{C_{OKi}}\right) = G\left(V_{REF} - \beta_{Ki}\frac{I_L t_{Ki}}{Nk_{Ki}C_{IKi}}\right) \tag{24}$$

where G and β_{Ki} are the trans-conductance of error amplifier and the ratio of voltage divider, respectively. Then, as shown in (25), the discharging current source I_{EKi} is equal to that the error signal V_{EKi} is divided by internal resistor R_{Ki}.

$$I_{EKi} = \frac{V_{EKi}}{R_{Ki}} = \frac{G\left(V_{REF} - \beta_{Ki}V_{OKi}\right)}{R_{Ki}} = \frac{G}{R_{Ki}}\left(V_{REF} - \beta_{Ki}\frac{I_L t_{Ki}}{Nk_{Ki}C_{IKi}}\right) \tag{25}$$

Differentiating both sides of (25) by the inductor current (I_L) and setting the value equal to one, (26) is derived to get a discharging current source I_{EKi} that is proportional to output load current. Consequently, (27) defines the value of resistor R_{Ki} in charge reservation circuit

for buck output terminals.

$$\frac{\partial I_{EKi}}{\partial I_{LKi}} = \frac{G\beta_{Ki}t_{Ki}}{R_{Ki}Nk_{Ki}C_{IKi}} = 1 \tag{26}$$

$$R_{Ki} = \frac{G\beta_{Ki}t_{Ki}}{Nk_{Ki}C_{IKi}}, \text{ for buck output terminal } i \tag{27}$$

Similarly, the value of resistor R_{Tj} for boost output terminals can be expressed as (28).

$$R_{Tj} = \frac{G\beta_{Tj}t_{Tj}}{Nk_{Tj}C_{ITj}}, \text{ for boost output terminal } j \tag{28}$$

Therefore, for controlling charge reservation circuit, the value of resistors R_{Ki} and R_{Tj} ensure that discharging current sources I_{EKi} and I_{ETj} in LDPCC circuit are proportional to load current condition of buck and boost output terminals. The discharging current sources I_{EKi} and I_{ETj} are expressed as equation (29) and (30) for buck and boost output terminals, respectively.

$$I_{EKi} = V_{EKi}\frac{Nk_{Ki}C_{IKi}}{G\beta_{Ki}t_{Ki}}, \text{ for buck output terminal } i \tag{29}$$

$$I_{ETj} = V_{ETj}\frac{Nk_{Tj}C_{ITj}}{G\beta_{Tj}t_{Tj}}, \text{ for boost output terminal } j \tag{30}$$

The charge stored on indicative capacitor C_{IKi} or C_{ITi} can effectively represent the regulated output voltage at the buck or boost output terminals. Thus, the proposed charge reservation circuit can accurately decide the duty cycle of the buck or boost output terminals. The simulation result of charge reservation circuit is shown in Fig. 39. The output signals V_{EKi} and V_{ETj} of error amplifier array indicate the output voltage deviation. Since the indicative capacitors C_{IKi} and C_{ITi} are charged and discharged by sensing current I_{sense} and LDPCC circuit sources I_{EKi} and I_{ETj}, the voltages V_{IKi} and V_{ITj} on indicative capacitors act sensing ripple of output terminals and compare with the output signals V_{EKi} and V_{EKj} of error amplifier array for detecting operation duty cycle of each output terminal.

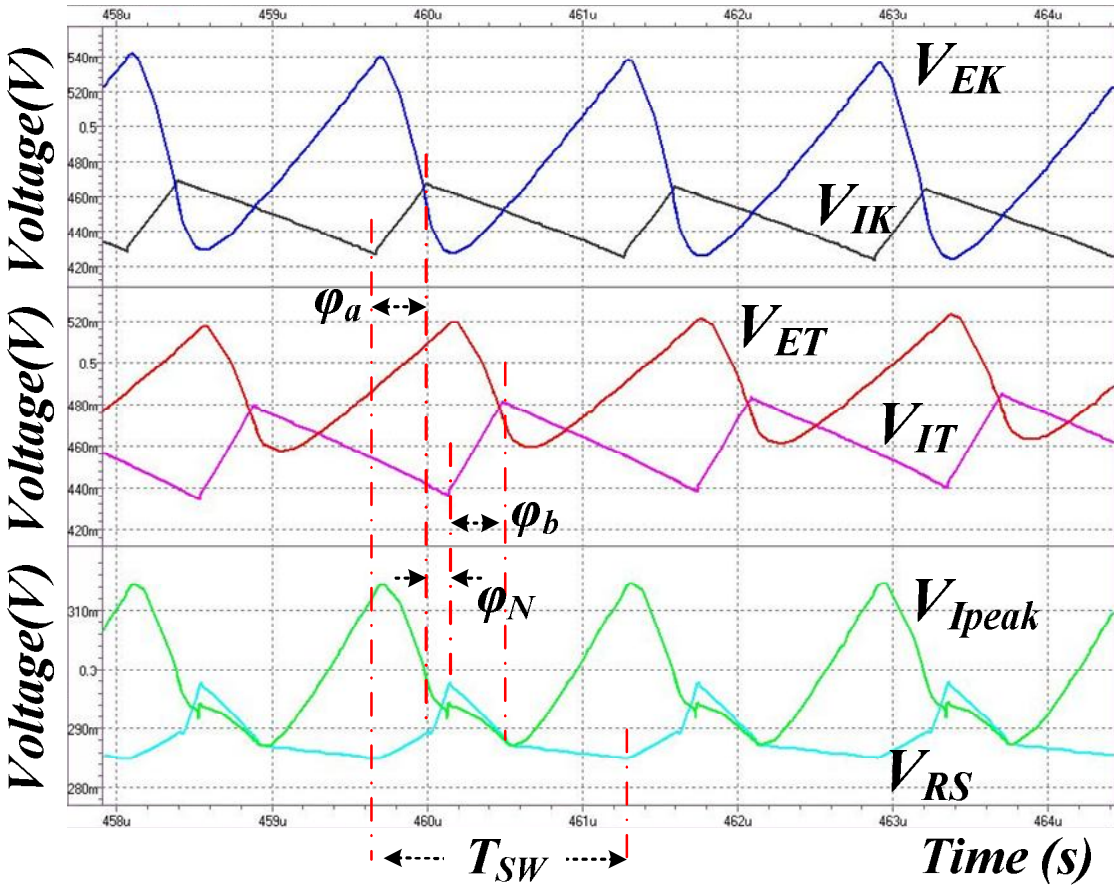


Fig. 39. The simulation result of the proposed charge reservation circuit.

3.3 Logic Control Circuit with Automatic Mode Switch for Avoiding Instability Problem

The control logic generator with automatic mode-switch controller is depicted in Fig. 40. It generates logic control signals D_{SWN}, D_{SWF}, D_{SWK1}~D_{SWKn}, and D_{SWT1}~D_{SWTm} for driving power switches according to system clock V_{CLK} and output signals CM_{Ki}, CM_R, and CM_{Tj} of comparator array. The operation of the control logic is divided into four durations of current paths 1, 3, 4, and 6, which sustain for the four charge-delivering paths in Fig. 25. At the beginning of path 1, the system clock V_{CLK} of control logic generator is triggered by a positive edge and 90% duty cycle of system clock V_{CLK}. The state of logic control signal D_{SWKi} is set to low state and converted to driving signal V_{SWKi} for delivering charge from supply source V_{IN}

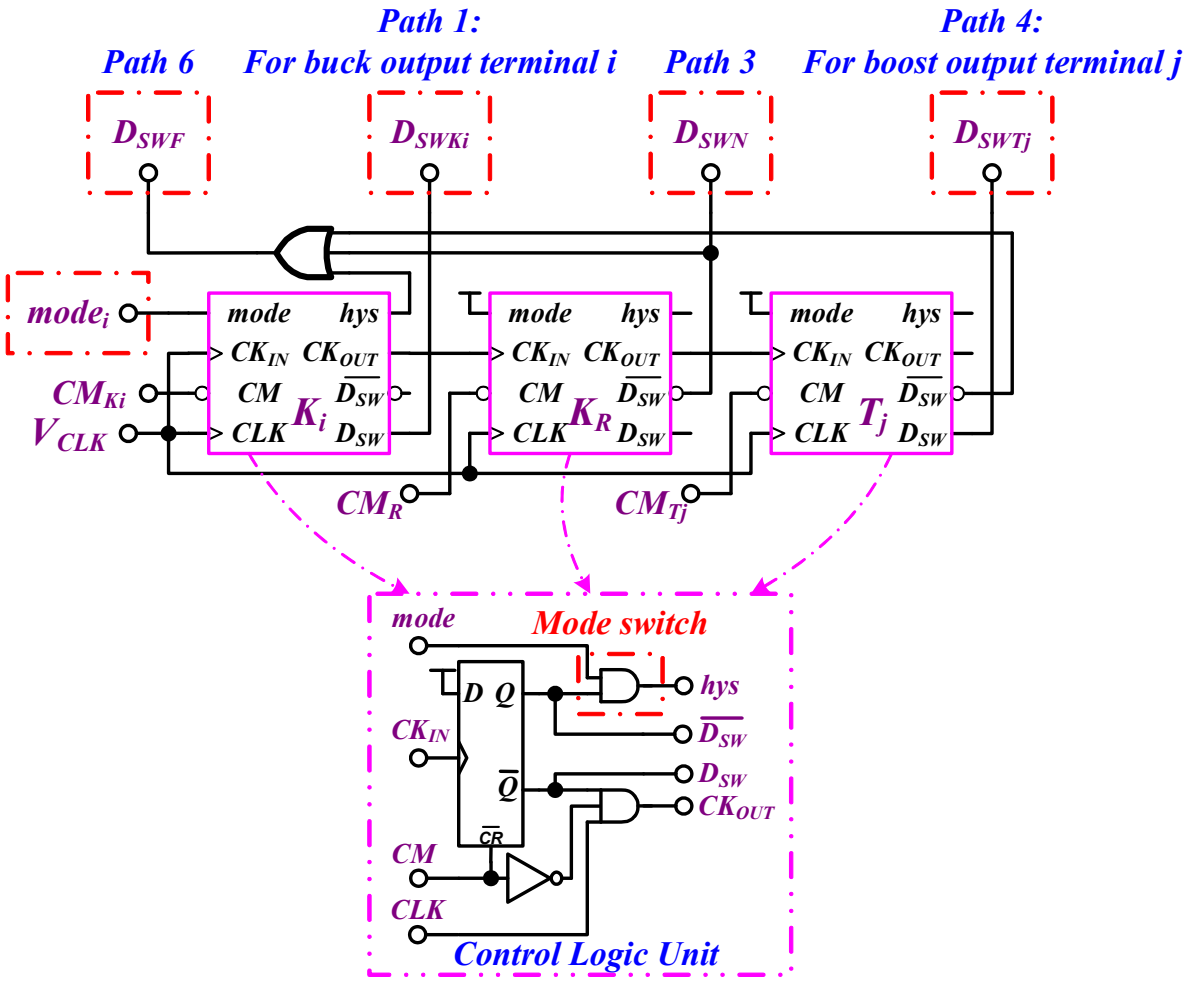


Fig. 40. The control logic generator with the mode switch controller.

to buck output terminal V_{OKi}. The input signal CM_{Ki} of control logic circuit, where the suffix i is from *1* to n for buck output terminals, is from output signals of related comparator i in Fig. 33, which decides the duty cycle of buck output terminal i. At the same time, the inductor current (I_L) is increased with a positive current slope ((V_{IN}-V_{OKi})/L). According to charge reservation circuit operation, current sensor senses inductor current (I_L) for charging indicative capacitors C_{IKi} and C_{ITj} of charge-reservation circuit. Therefore, the indicative capacitor C_{IKi} is charged by sensing current I_{sense} of current sensor. When the charging voltage V_{IKi} on indicative capacitor C_{IKi} is larger than output signal V_{EKi} of error amplifier array in Fig. 33, the output signal CM_{Ki} of comparator array changes to a low state and path 1 then turns off. Since the control logic unit combines the system clock V_{CLK} and comparator output CM_{Ki}

as trigger signal CK_{OUT}, Path 3 starts to ensure sufficient energy to be stored in the inductor L at the negative edge of comparator output CM_{Ki}. That is, the inductor current (I_L) is increased to the LDPCC level (I_{peak}).

In path 3, the LDPCC signal V_{Ipeak} in (19) which defines charge requirement according to the LDPCC circuit in Fig. 34 and the value of current signal V_{RS} in Fig. 36 are used to determine the time interval of output signal D_{SWN} for increasing the inductor current (I_L) to the LDPCC level (I_{peak}) until the value of current signal V_{RS} is large than that of LDPCC signal V_{Ipeak}. That is, the output signal D_{SWN} is set to high state for increasing the value of inductor current (I_L) to LDPCC level (I_{peak}) until the value of current signal V_{RS} is large than that of LDPCC signal V_{Ipeak}. However, the time interval of output signal D_{SWN} may be zero if the inductor current (I_L) is increased to exceed the LDPCC level (I_{peak}) during path 1. This condition is caused by the heavy load condition at buck output terminals and light load condition at boost output terminals. This means that the inductor current level (I_L) is high enough to provide sufficient energy to the multiple boost output terminals after path 1. There is no need to store more charge in the inductor L since it may cause current accumulation issue in Fig. 41. Therefore, a hysteresis mode which is shown in Fig. 26 is proposed to address the current accumulation issue and provide a new charge-delivering path rather than path 1.

Once the value of current signal V_{RS} is large than that of LDPCC signal V_{Ipeak}, comparator output CM_R changes to low state and path 3 turns off. Path 4 then is enabled by negative edge of comparator output CM_R and starts to deliver charge to boost output terminals. At the same time, the inductor current (I_L) is decreased with a negative current slope ((V_{OB}-V_{IN})/L) which according to the load condition of the boost output terminals. Similarly, according to charge reservation circuit operation, indicative capacitor C_{ITj} is charged by sensing current (I_{sense}) of current sensor. When the charging voltage V_{ITj} on indicative capacitor C_{ITj} is larger than output signal V_{ETj} of error amplifier array in Fig. 33, the output

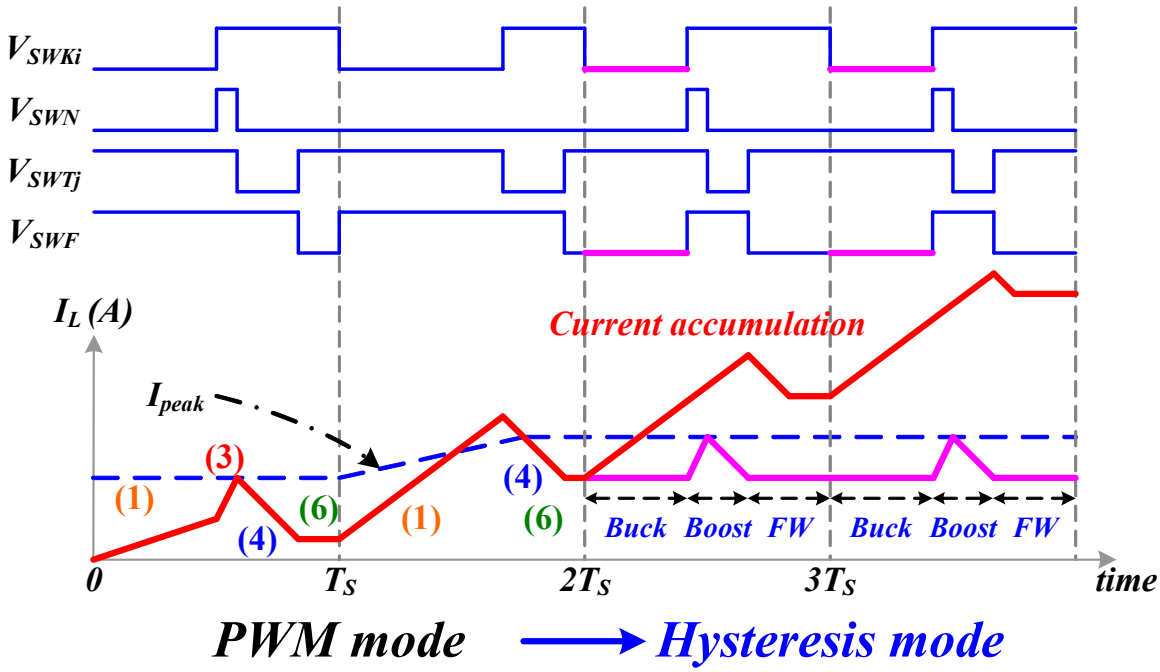


Fig. 41. The timing diagram of the transition from the PWM mode to the hysteresis mode.

signal CM_{Tj} of comparator array changes to low state. Once comparator output CM_{Tj} is changed to a low state when the value of charging voltage V_{ITi} is larger than output signal V_{ETj} of error amplifier array, the charge-delivery to the boost output terminals is completed. Then the controlling sequence-II enters path 6 named as freewheeling stage. That is, the surplus energy is reserved in the inductor L. The longer the period of the freewheeling stage is, the lower the power conversion efficiency. Owing to the adjustment of the LDPCC circuit, the inductor current level (I_L) at the freewheeling stage is kept at a low level which is limited by a minimum current level $I_{DC(min)}$ and thus the conduction loss can be reduced at light load conditions. All the output signals D_{SWK1}~D_{SWKn}, D_{SWN}, D_{SWT1}~D_{SWTm}, and D_{SWF} of the control logic circuit are converted by the dead-time controller and driver circuit which is shown in Fig. 33 to the gate driving signals V_{SWN}, V_{SWF}, V_{SWK1}~V_{SWKn}, and V_{SWT1}~V_{SWTm} which are used to control the power MOSFET switches SW_N, SW_F, SW_{K1}~SW_{Kn}, and SW_{T1}~SW_{Tm}.

However, the mentioned current accumulation issue which is illustrated in Fig. 41 still exists in the structure of SIMO converter. When the output power of buck output terminals is

larger than that of boost output terminals, the current accumulation occurs. The charge from supply source not only delivers to the buck terminals but also store charge in the inductor L during path 1 operation. The only way to release storage charge in inductor L is to transfer storage charge to boost terminals during path 4 operation. Thus, when charge deliver to boost terminals are smaller than that of buck terminals, the inductor current level (I_L) is going to increase higher than the LDPCC level (I_{peak}). Owing to the current accumulation in inductor L, the sensing current (I_{sense}) also increase to high value. Therefore, the charging voltage V_{ITj} on the indicative capacitor C_{ITj} of charge reservation circuit rapidly increases during short period. The operating duration of boost terminals becomes much smaller than the original due to the highly inductor current level (I_L). This situation causes that the comparator array is not able to react to such a small operating duration. Thus, the accumulated current causes serious cross-regulation and poor conversion efficiency at light load conditions.

To address this problem, it is important to provide other releasing path to alleviate the instability. Hence, a new current path which is path 0 and named as hysteresis mode is proposed in Fig. 26. During operation of hysteresis mode, original path 1 in PWM mode is changed to path 0 to force the delivering current to flow through freewheeling switch SW_6 to the buck terminals. Therefore, the delivering energy of the buck terminals does not cause current accumulation in the inductor L. Thus, the buck terminals works as a hysteresis buck converter, and the output voltage V_{OKi} is directly regulated and limited by a hysteresis window. The power MOSFET's driving signals and inductor current waveform (I_L) as depicted in Fig. 41 which shows the transition from the PWM mode to the hysteresis mode. To achieve the hysteresis control mode, a mode switch, a power comparator, and a novel delta-voltage generator are proposed. The mode switch as shown in the sub-block of control logic unit in Fig. 40 is composed of only one AND logic gate, and the output signal "*hys*" of mode switch is kept at a high state during the PWM operation until the input signal "$mode_i$" of mode witch which comes from the power comparator circuit is changed to a low state. Then the operation

of the buck terminals is switched to hysteresis mode. Since path 6 directly connects the buck terminals to supply source V_{IN}, the output ripple of buck terminals is increased for ensuring system stability during hysteresis mode. The simulation results are shown in Fig. 42 and 43 which are shown the PWM mode and hysteresis mode, respectively. Next chapter discusses the power comparator and delta-voltage generators to smoothly switch the operating mode between the PWM and hysteresis modes in detail.

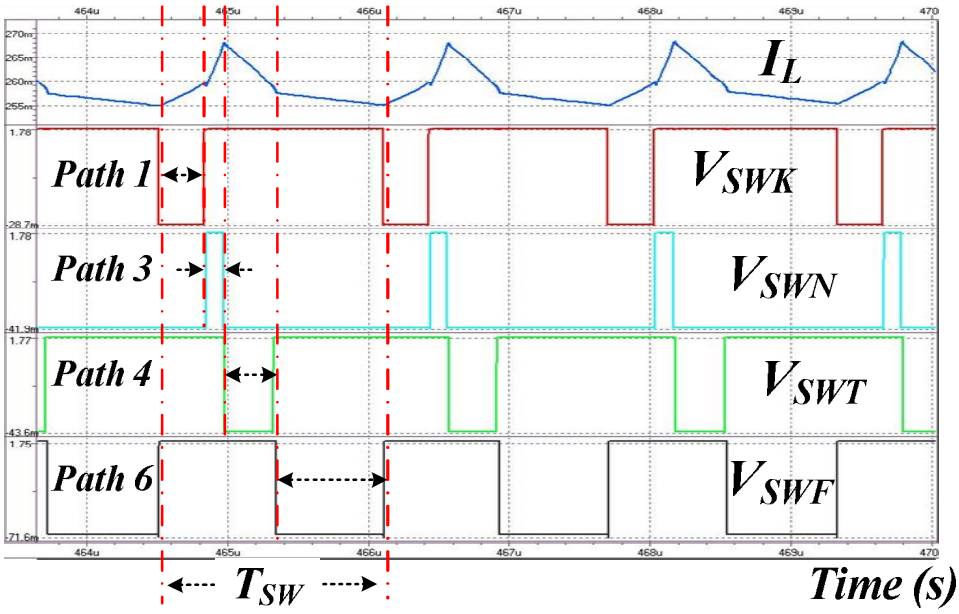


Fig. 42. The simulated waveforms of control logic circuit in PWM mode operation.

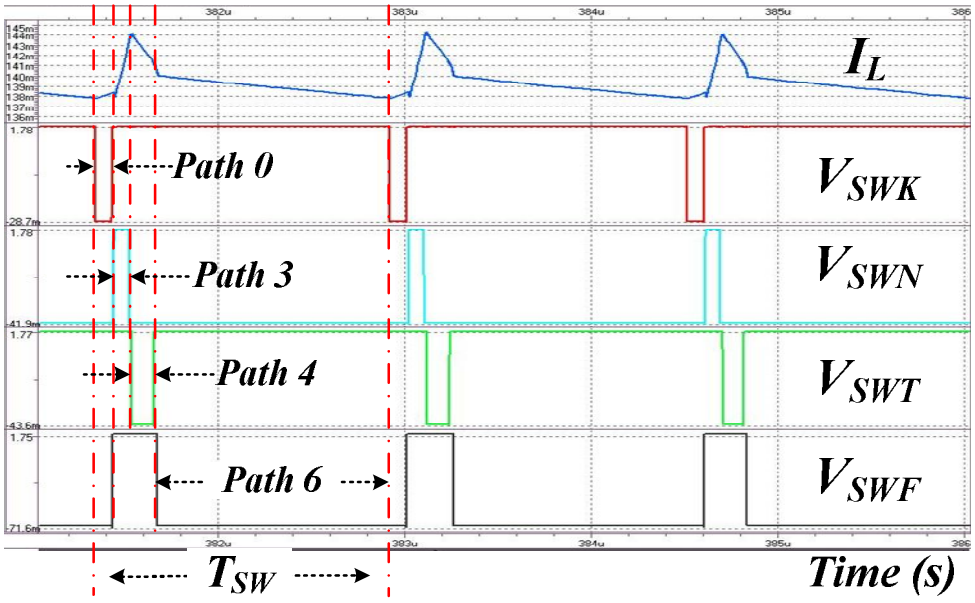


Fig. 43. The simulated waveforms of control logic circuit in hysteresis mode operation.

3.4 Clock Generator with Power-On Reset Mechanism and Startup Circuit

A system clock circuit with power-on reset (POR) control circuit is shown in Fig. 44 which generates the system clock V_{CLK} and sawtooth signal V_{ramp} for controlling logic circuit of SIMO converter. The current sources (I_{BH}) and (I_{BL}) are used to charge and discharge oscillating capacitor C_{OSC}. Reference voltage V_{refH} and V_{refL} limit the maximum and minimum voltage level of sawtooth signal V_{ramp}. At the initial condition, the signal POR which comes from output of reference voltage circuit is high state. The oscillating capacitor C_{osc} and resetting capacitor C_{rst} are shorted to ground, thus the output signals *RST*, *VCTB*, and V_{CLK} are disabled and set to low state. When the reference voltage is ready, the *POR* is set to low state and clock generator is enabled. At the beginning, the oscillating signals V_U and V_L is set to low state since charging voltage V_{ramp} on oscillating capacitor C_{OSC} is zero voltage. The current source (I_{BH}) starts to charge oscillating capacitor C_{OSC}. Once the charging voltage V_{ramp} on c oscillating capacitor C_{OSC} is higher than reference voltage V_{refH}, the oscillating signals V_U and V_L are set to high state and the current source (I_{BL}) starts to discharge oscillating capacitor C_{OSC}. The output resetting signal *RST* is triggered and set to high state when oscillating signal V_L sets to high state and the resetting capacitor C_{rst} has been fully charged. Therefore, output signals *VCTB* and V_{CK} starts to trigger the control logic circuit for controlling proposed sequence-II. When the oscillating signals V_U and V_L are set to high state, charging voltage V_{ramp} on oscillating capacitor C_{OSC} is discharged by current source (I_{BL}). Until charging voltage V_{ramp} is smaller than reference voltage V_{refL}, the oscillating signals V_U and V_L are set back to low state for next clock period. The frequency (f_{OSC}) of clock generator depends on the charging and discharging current sources (I_{BH}) and (I_{BL}), oscillating capacitor C_{OSC}, and the hysteresis window of reference voltage V_{refH} and V_{refL}. For achieve the controlling sequence-II in Fig. 25, the high state of clock signal is needed. That is, the ratio of

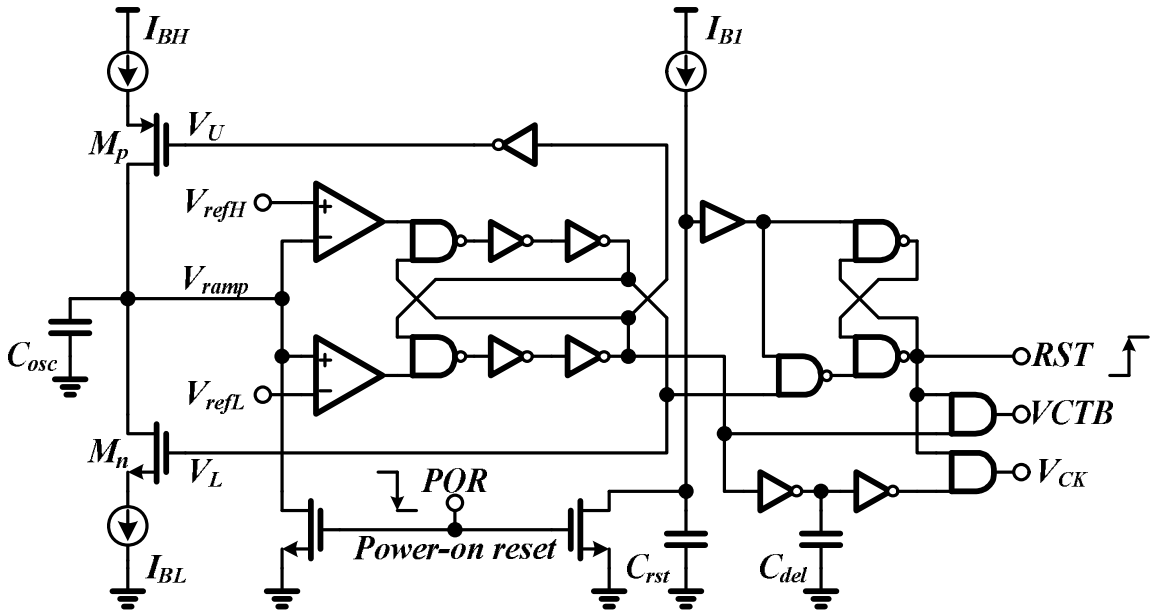


Fig. 44. The clock generator with power-on reset control machine.

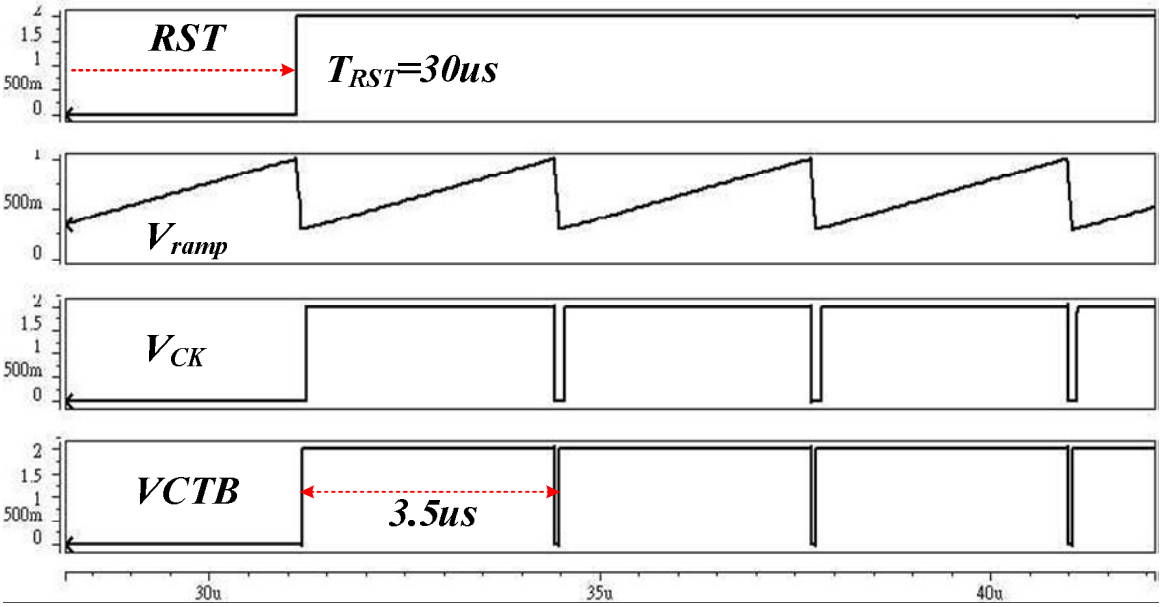


Fig. 45. The simulated waveforms of sawtooth and clock signals.

current I_{BH} to current I_{BL} is designed as 1:9 for generating 90% duty cycle. Thus, the clock frequency (f_{OSC}) is given by voltage-second balance equation in (31).

$$f_{osc} = \frac{0.9 I_{BH}}{\left(V_{refH} - V_{refL}\right) \cdot C_{osc}} \tag{31}$$

The simulated timing diagram of generated clock V_{CLK} and sawtooth signal V_{ramp} for controlling logic circuit of SIMO converter is illustrated in Fig. 45. The resetting signal *RST*

outputs the clock and synchronous signals V_{CLK} and $VCTB$ at the same time. The reset period T_{RST} sets long enough for resetting the initial state of digital flip-flop and analog control circuit.

At the power-on period of SIMO converter, the buck and boost output terminals are close to zero-voltage. Hence, the duty cycle of buck and boost terminals are extend to maximum ratio of switching cycle. Therefore, buck and boost output terminals have a possibility of overshoot issue due to highly inrush current which is accumulated in inductor L during rising transient of output terminals. Since the design limitation of controlling sequence-II in startup transition, the path 1 for buck terminals occupies whole switching duration. The situation causes the long settling time on boost terminals. To address the highly inrush current and long settling time during power-on procedure, a startup circuit which is shown in Fig. 46 is used to limit startup current and distribute the switching period among output terminals. At the initial condition, the resetting signal POR is set to high state. The startup capacitor C_{st} are shorted to ground, and feedback signals F_{BKi} and F_{BTj} are clamped to ground. When the reference voltage is ready, the resetting signal POR is set to low state and the voltage STE on startup capacitor C_{st} increases gradually. During startup procedure, the feedback signals F_{BKi} and F_{BTj} compare with the startup voltage STE to decide error signals V_{EKi} and V_{ETj}. Since the voltage STE on startup capacitor C_{st} is low and connected to the gate of MOSFET M_S in Fig. 46, the MOSFET M_S dominates one branch oferror amplifier. The duty cycle of buck and boost output terminals are limited by startup voltage STE. Once the startup voltage STE is higher than reference voltage V_{ref}, the MOSFET M_S in error amplifier turns off. Finally, the feedback loop begins to be switched to that the output voltages are regulated by reference voltage V_{ref}. The simulation result of startup circuit is shown in Fig. 47. Since the startup circuit limits the regulating voltage of output terminals smoothly, the inrush current can be eliminated. Since the delivering energy fairly distribute switching period among output terminals, the output voltages can be simultaneously regulated.

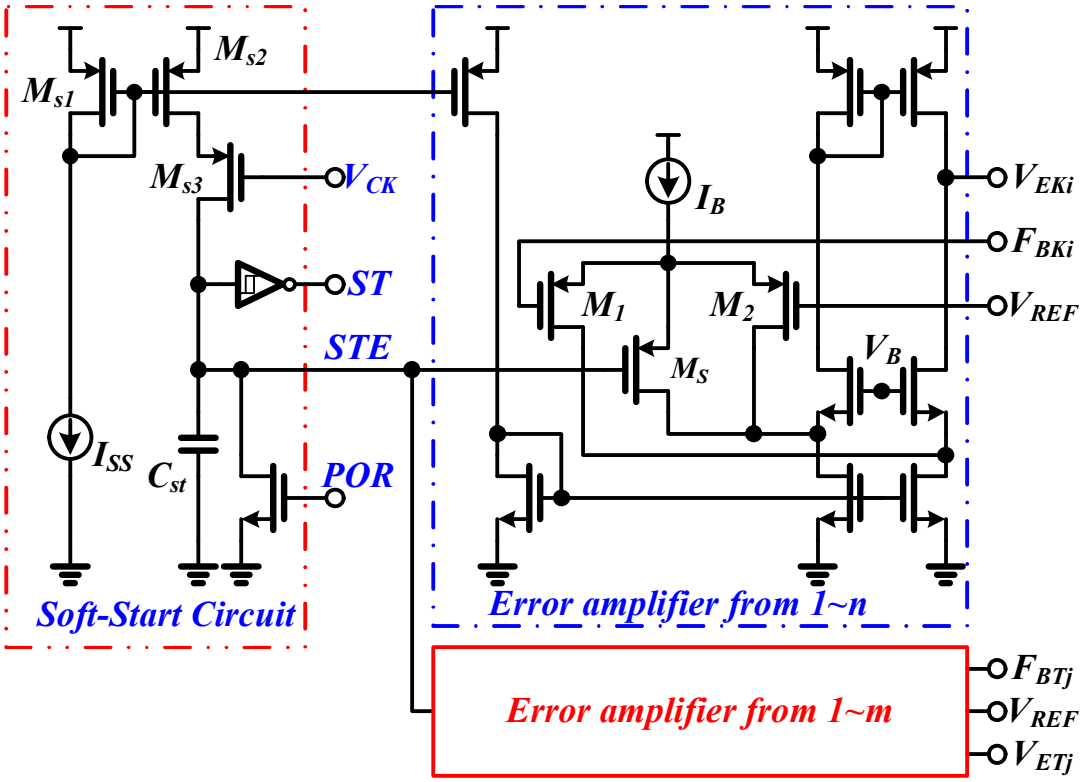


Fig. 46. The startup circuit for SIMO converter.

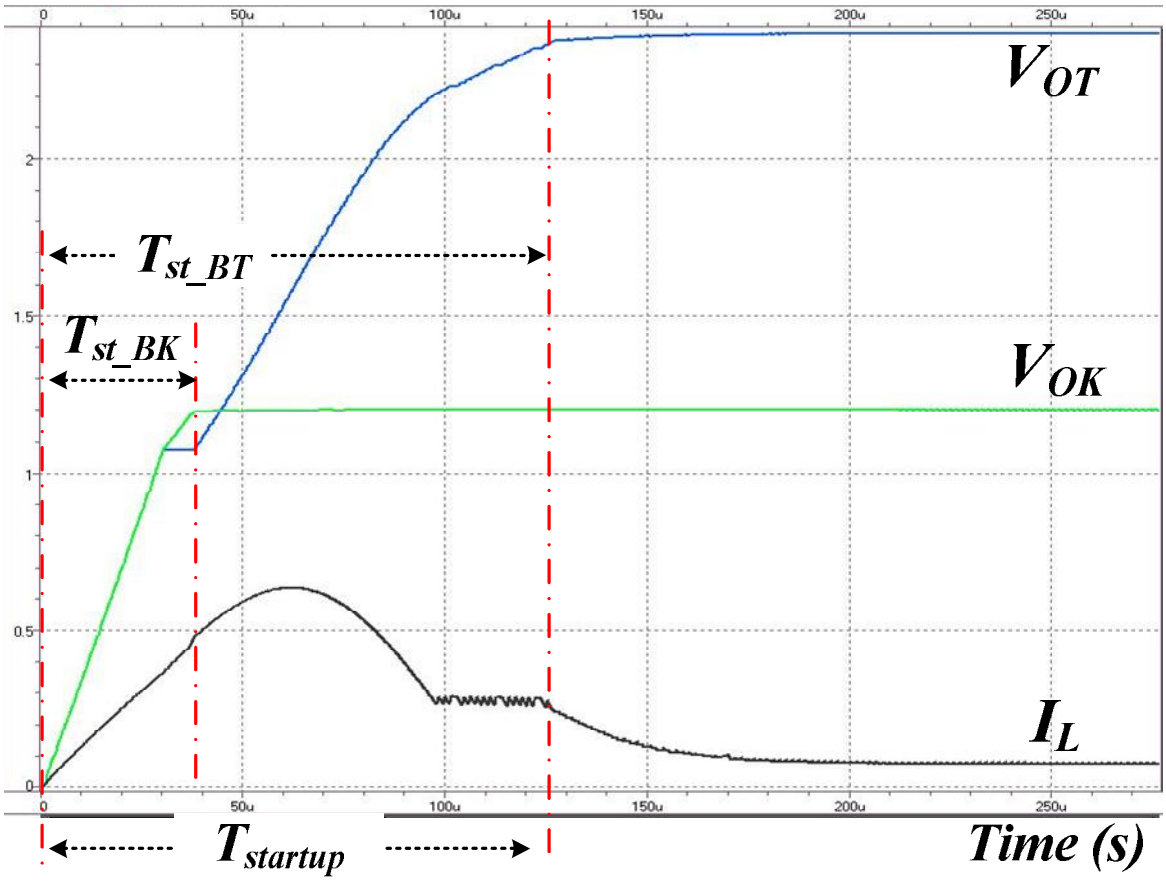


Fig. 47. The simulation result of startup circuit for SIMO converter.

3.5 Dead-time Controller and Driver

Since the control logic circuit has been generated the driving sequence according to proposed controlling sequence-II, the gate driving signals V_{SWN}, V_{SWF}, V_{SWK1}~V_{SWn}, and V_{SWT1}~V_{SWTm} of power switches take turns to turn on related power switch. For high power capability and reducing conduction losses, a large size of power switches with large parasitic capacitance on gate terminal of power switches is used. Therefore, the rising and falling time (t_r) and (t_f) of gate driving signals is depended on driving capacitance of driver. Owing to the switching transient of power switches may cause large short-through current, a duration of interleaf during switching transient of power switches is necessary. To address abnormal leakage and short-through current when switches are turning on and off, the dead-time control circuit is designed to interleave a blank time during switching transient for eliminating leakage and short-through current. Figure 48 describes the dead-time control procedure step by step. In order to achieve adaptive dead-time control, the circuit design methodology is "turn-off-first and turn-on-later", which means that the leakage can be avoided due to the turning off first of power switches. Then, charge can be delivered to suitable output terminals due to the turning on later of power switches. As illustrated in Fig. 48, the transition from path 1 to path 3 needs dead-time I process to avoid shoot-through current from buck output terminals to ground. The dead-time II process prevents boost output terminals from flowing current to ground when path 3 transits to path 4. Similarly, the dead-time III process prevents boost output terminals from flowing current to supply source when path 4 transits to path 6. Finally, the dead-time IV can prevent buck output terminals from losing charge to freewheel loop, and thereby reducing power losses at buck output terminals. Owing to the implementation of four dead-time processes, short-through current can be addressed. Furthermore, the power conversion efficiency can improved due to minimized leakage current, which comes from inadequate overlap between different power switches. However,

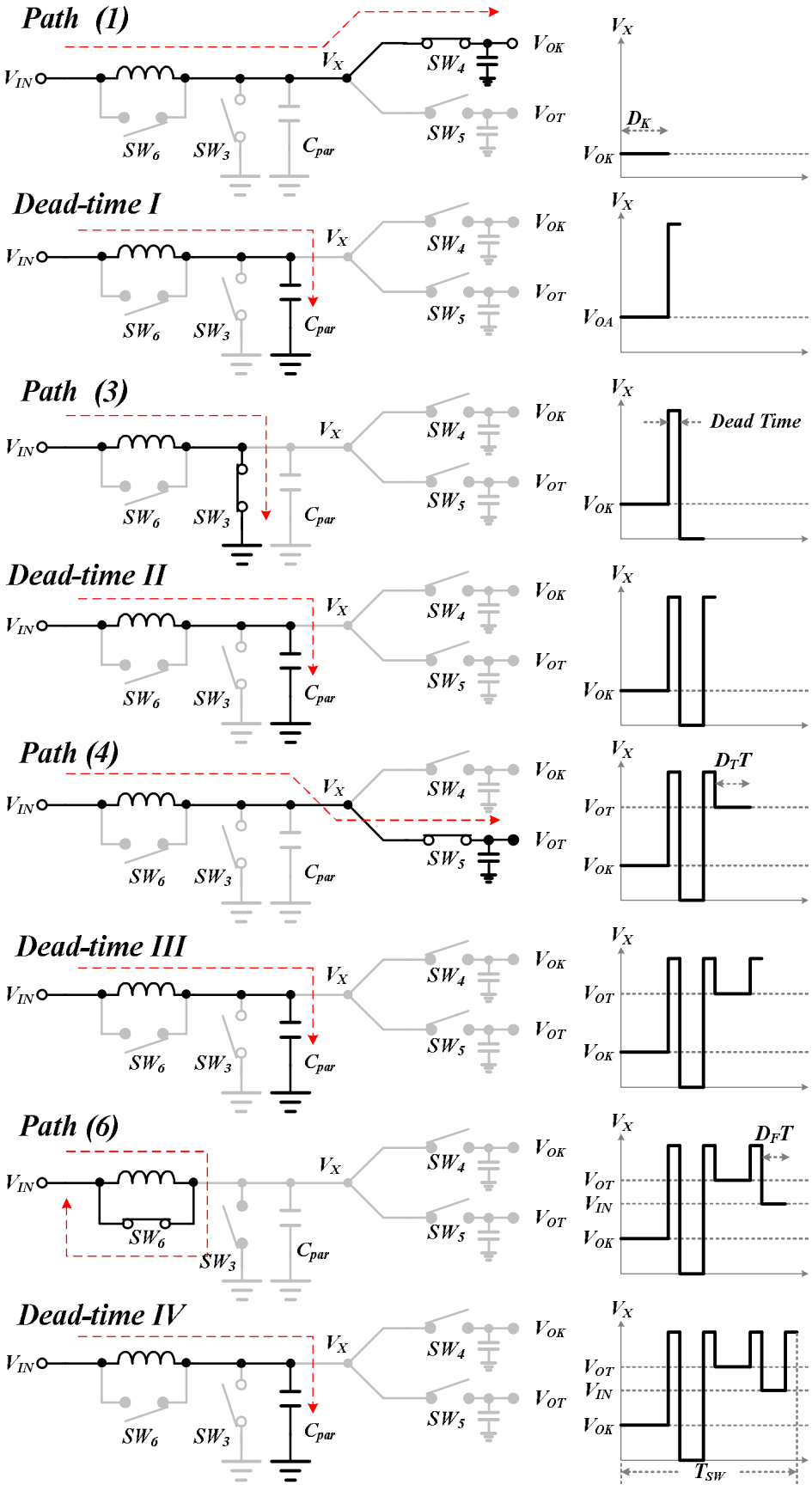


Fig. 48. The dead-time control sequence of SIMO converter.

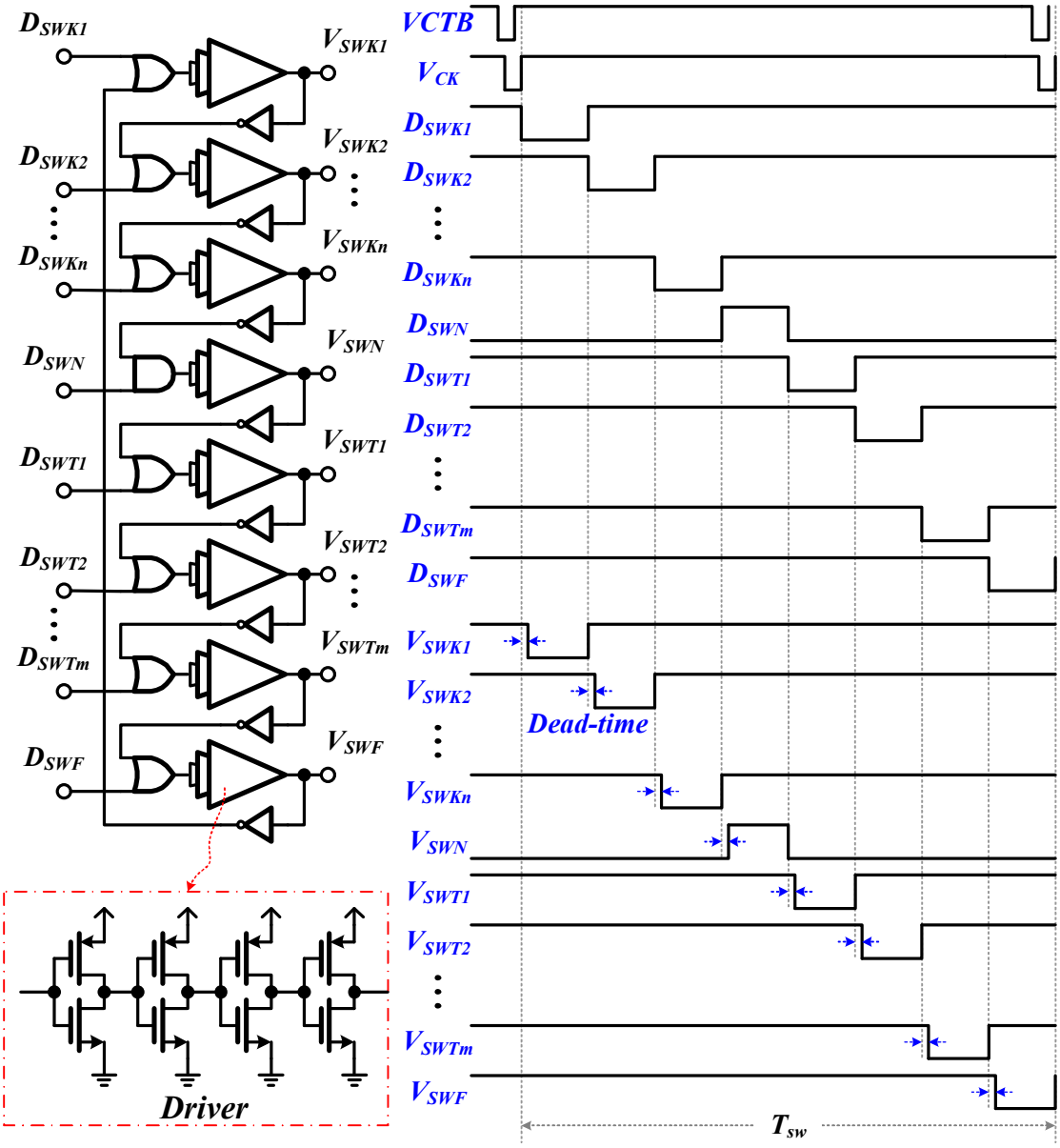


Fig. 49. The dead-time control circuit of SIMO converter.

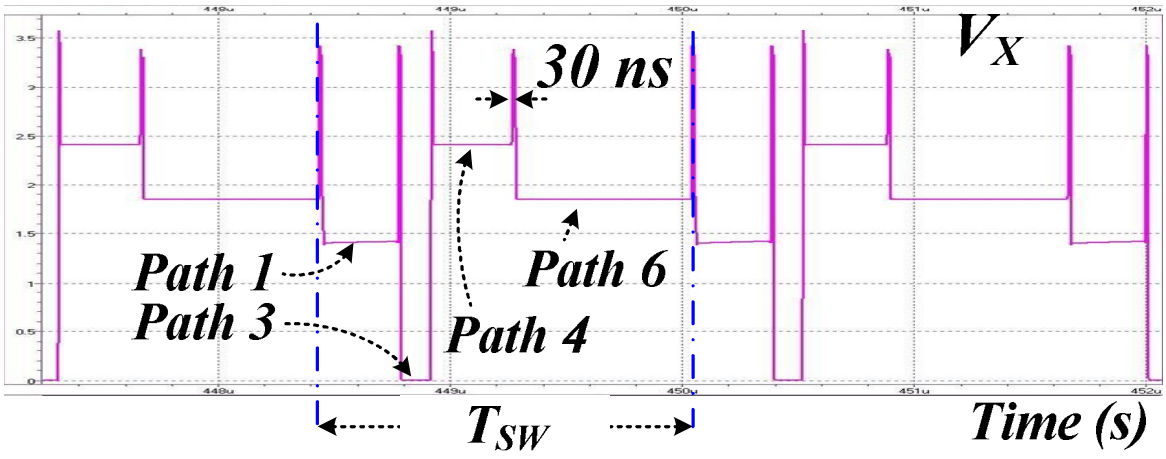


Fig. 50. The simulation result of dead-time controller.

the dead-time processes cause a voltage spike on node V_X. During the duration of dead-time process, since the inductor current (I_L) tries to keep current running the same direction and magnitude than before, a parasitic capacitor C_{par} will be charged in short period. The behavior of voltage on node VX is shown in the right-side of Fig. 48. The schematic of dead-time control circuit with driver is shown in Fig. 49. Since the control sequence-II has been scheduled the output signals D_{SWN}, D_{SWF}, D_{SWK1}~D_{SWKn}, and D_{SWT1}~D_{SWTm} of control logic circuit, the gate driving signals V_{SWN}, V_{SWF}, V_{SWK1}~V_{SWKn}, and V_{SWT1}~V_{SWTm} of power switches can be simplified to monitor the previous switching transient of power switch. The next power switch starts to turn on at the turn off state of last power switch is ensuring. Therefore, dead-time controller avoids power switches turn on at the same time. The simulation result of dead-time controller is shown in Fig. 50. The voltage spike on node V_X has been simulated which indicates the maximum dead-time is 30ns. Besides, in order to fully turn off power switches of output terminals, the supply voltage of dead-time controller and driver is connected to the highest voltage level (V_{MAX}) of boost terminals which is selected by the proposed maximum voltage selector.

3.6 Maximum Voltage Selector Circuit and Adaptive Body Switch (ABS) Circuit

To fully turn on and off power switches of output terminals, the supply voltage of dead-time controller and driver circuit must connect to the highest voltage level (V_{MAX}) of boost terminals. Therefore, a voltage comparator array usually designs into the maximum voltage selector circuit for detecting the highest output voltage (V_{MAX}). Large number of boost terminals increases higher operation current and complex circuit design for biasing voltage comparator. In order to reduce the power consumption of maximum voltage selector circuit and simplify composed structure of voltage comparator, a new and simplest multiple-input voltage comparator as shown in Fig. 51 is proposed to detect the highest voltage level (V_{MAX})

on all of boost terminals.

As illustrated in Fig. 51, transistors M_{B1}~M_{B3} and bias current (I_B) compose the biasing loop, the controlling logic circuits are biased by the maximum voltage (V_{MAX}). The biasing voltage (V_{BP}) is used to clamp the gate biasing voltage of each input terminal for comparing the detecting voltage (V_M) and input terminals V_{IN} and V_{OT1}~V_{OTj}. At the initial condition of

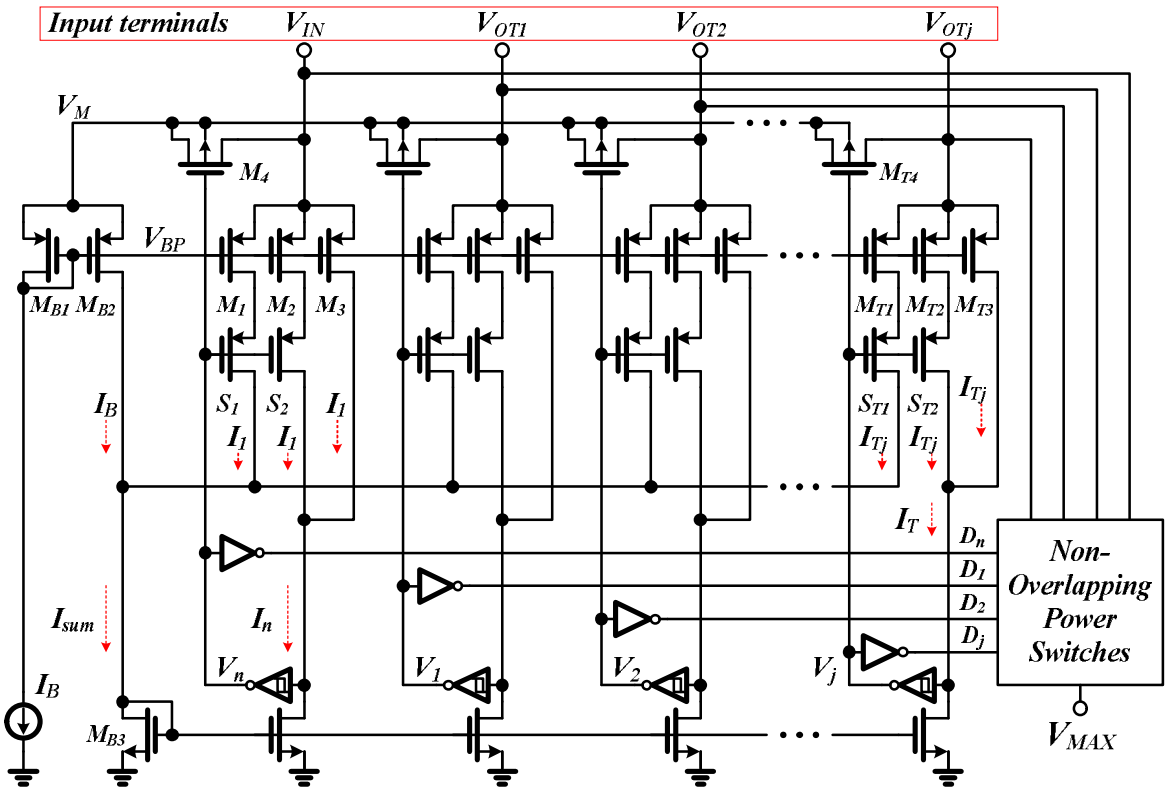


Fig. 51. The proposed maximum voltage selector circuit for dead-time and driver circuit.

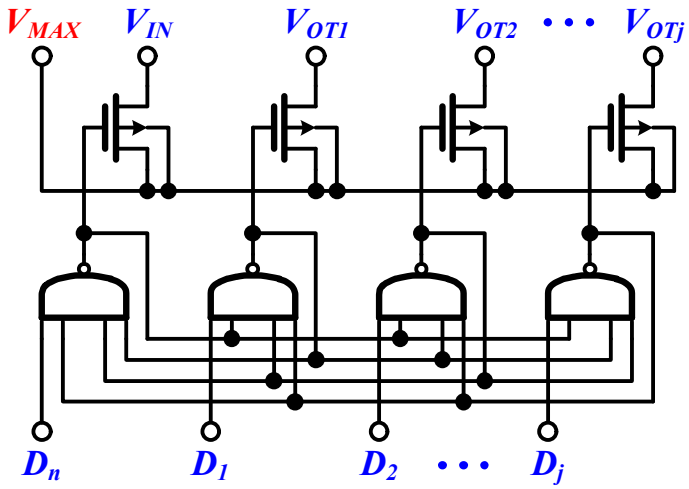


Fig. 52.The non-overlapping power switches.

power on procedure, the detecting voltage (V_M), input terminals V_{OT1}~V_{OTj}, and maximum voltage (V_{max}) are zero. The input terminal V_{IN}, which comes from battery or supply source, is only the highest voltage (V_{MAX}) in maximum voltage selector. The voltage difference between detecting voltage (V_M) and input terminal V_{IN} cause the gate-source voltage V_{GS} of transistor M_3 is higher than that of transistor M_{B1}. Therefore, the drain current (I_1) of input terminal V_{IN} is larger than biasing current (I_B). That is, the current (I_n) is larger than detecting current (I_{sum}) and the detecting signal (V_n) of detecting logic is then set to low state. Transistors S_1, S_2, and M_4 turn on, the detecting voltage (V_M) is charged closed to the input terminal V_{IN} via transistor M_4. The maximum voltage (V_{MAX}), which provides the supply voltage of driver, is connected to the input terminal V_{IN} by a non-overlapping power switches which is illustrated in Fig. 52. In the meanwhile, in order to get the information of input terminal V_{IN}, the detecting current (I_1) is added to detecting current (I_{sum}) through S_1 and the detecting current (I_n) equals to $2I_1$ for stabilizing the logic state during the input terminal V_{IN} is the highest voltage. Moreover, owing to other input terminals are smaller than detecting voltage (V_M), the input MOSFETs which connect to input terminals, such as transistors M_{T1}~M_{T3}, are biased at cut-off region. Thus, the detecting current (I_{Tj}) is zero and smaller than detecting current (I_{sum}), the logic state of detecting signals V_j is then set to high state for disabling the connection from other input terminal V_{OTj} and saving power consumption.

Owing to the detecting current (I_1) of the input terminal V_{IN} is added to detecting current (I_{sum}), the voltage difference between detecting voltage (V_M) and the next input terminal V_{OTj} must be higher enough to generate that detecting current (I_{Tj}) is larger than detecting current (I_{sum}). Therefore, when the input terminal V_{OTj} ramps up to the defined voltage level and is higher than detecting voltage (V_M), the detecting current (I_T) is larger than detecting current (I_{sum}) for generating low state of detecting signal (V_j). Since detecting signal (V_j) changes to low state, transistors S_{T1}, S_{T2}, and M_{T4} turn on, the detecting current (I_{Tj}) is added to detecting current (I_{sum}) and detecting current (I_T) equals to $2I_{Tj}$ for stabilizing low state of detecting

signal (V_j). At the same time, the detecting current (I_n) which is generated from input terminal V_{IN} is smaller than detecting current (I_{sum}) and detecting signal (V_n) sets to high state. The detecting current (I_1) then removes from detecting current (I_{sum}), the maximum voltage (V_{MAX}) disconnect to input terminal V_{IN} and then connects to input terminal V_{OTj}. In the meanwhile, the detecting voltage (V_M) is charged closed to input terminal V_{OTj} by transistor M_{T4}. Owing to the highest voltage changes to input terminal V_{OTj}, the input MOSFETs which connects to other input terminals, are biased at cut-off region. The maximum voltage selector circuit causes that only the biasing loop and the highest input terminal has biasing current. Therefore, the minimized biasing current and minimum power consumption can be achieved. The simulation result of the maximum voltage and total biasing current is shown in Fig. 53.

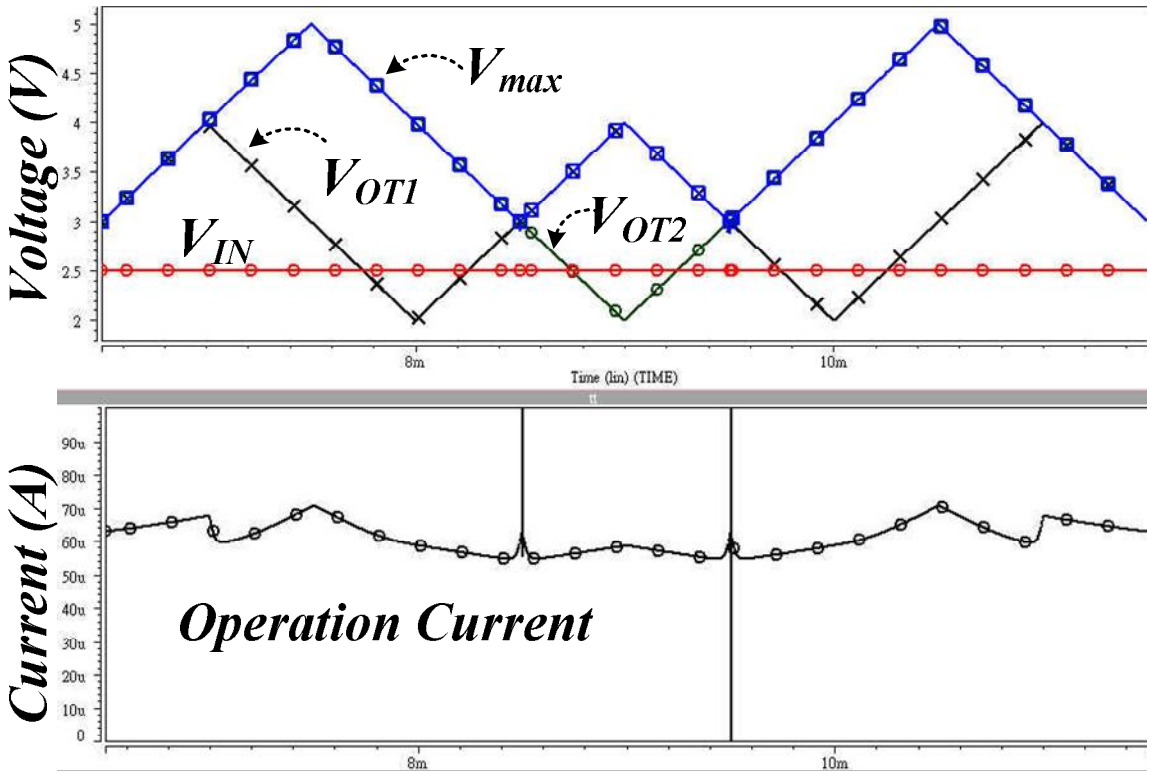


Fig. 53. The simulation result of maximum voltage selector circuit.

In CMOS fabrication technologies, single-well process is popularly used. Fig. 54 shows the cross section of single n-well CMOS process. Node B_P is the n-well biasing terminal for p-MOSFET transistor substrate and node B_N is the p-substrate biasing voltage for n-MOSFET

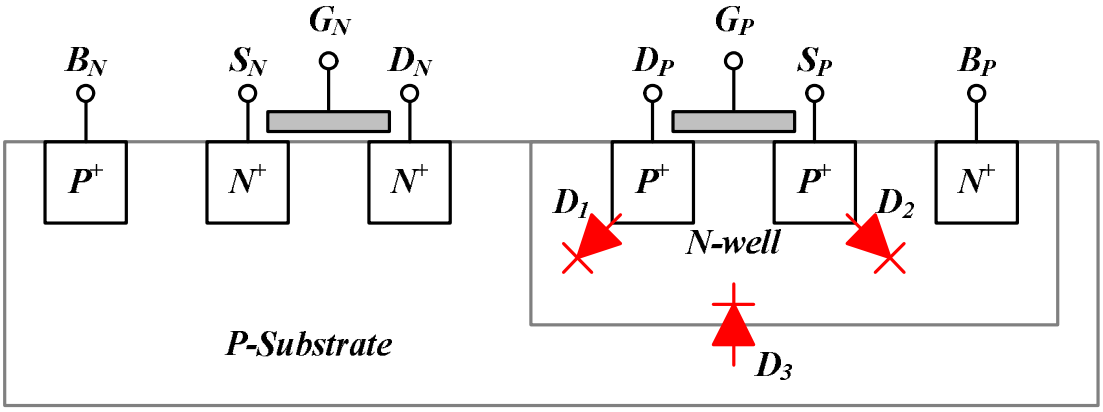


Fig. 54. The cross section of n-well CMOS process.

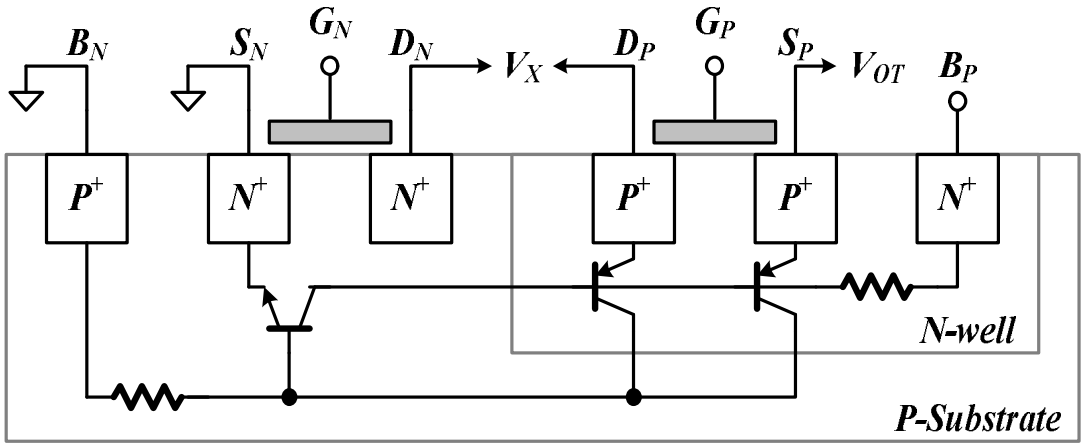


Fig. 55. The latch-up and equivalent latch-up circuit in n-well CMOS process.

transistor. To prevent the conduction of the parasitic PN junction diodes (such as D_1 and D_2) and avoid latch-up, node B_P should be connected to the highest voltage (V_{MAX}) of SIMO converter, which is the supply voltage in most cases. Similarly, node B_N should be connected to the lowest voltage of SIMO converter, which is usually the ground [43]. When the substrate voltage is improperly handled, leakage current becomes a serious problem. This is especially critical for the systems adopting variable bias at drain and source terminals. Because the voltage of drain terminal D_P of p-MOSFET transistor can be possibly higher or lower than that of source terminal S_P, the leakage problem can be hardly prevented if the substrate is tied to a fixed voltage node. More seriously, parasitic bipolar transistor in a

CMOS process form a latch-up circuit, illustrated in Fig. 55. When the voltage of node V_X is lower than that of output terminal V_{OT}, the substrate voltage in the n-well should be tied to output terminal V_{OT} to avoid leakage. However, if voltage of node V_X becomes higher than that of output terminal V_{OT}, the emitter voltage of parasitic PNP transistor will be higher than that of node B_P, and a positive current feedback loop will be activated. The risk of having devastating latch-up increases substantially.

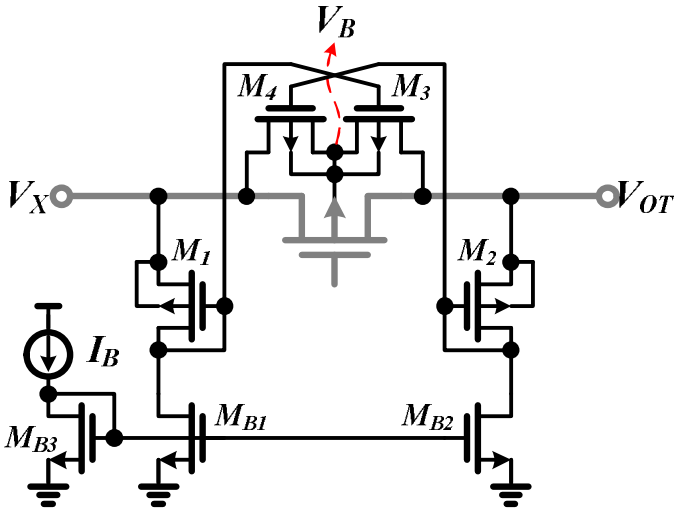


Fig. 56. The proposed ABS circuit for p-MOSFET' body bias.

Owing to the dead-time insert into the controlling sequence of SIMO converter, the voltage spike occurs on the node V_X which is shown in the right-side of Fig. 48. During the time interval of dead-time process, all of power switches turn off. Since the inductor L tries to keep current running the same direction and magnitude than before, the inductor current (I_L) turns to charge the parasitic capacitor C_{par} on node V_X. Therefore, a large volume of voltage spike appears and higher than that of output terminals. A back-to-back isolated rectifier in output multiplexers are used in [1], but sacrifice the power conversion efficiency for avoiding the lower positive output voltage would always clamp the higher one. Therefore, in order to address leakage current and potential latch-up of p-MOSFET, the adaptive body switch (ABS) circuit as illustrated in Fig. 56 is necessary and important to connect the body terminal of p-MOSFET to the highest voltage level.

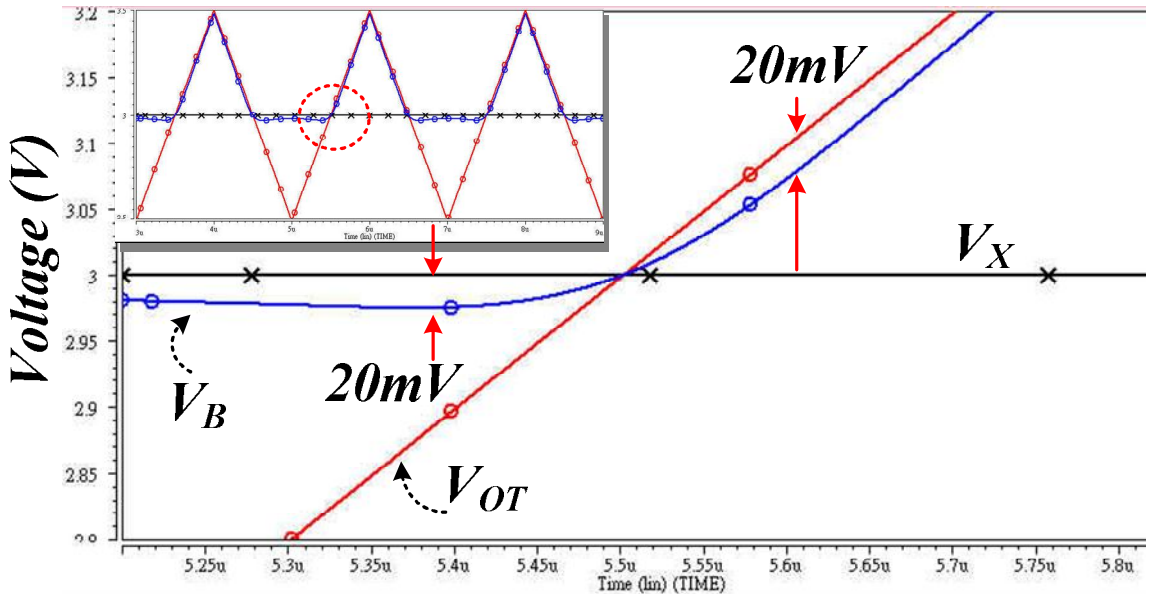


Fig. 57. The simulation result of proposed ABS circuit.

However, the different requirement with maximum voltage selector of driver, a rapidly response and ultra-low power consumption are major demand of ABS circuit. A simplest and low power consumption voltage detector is presented for rapidly selecting the maximum voltage level of body terminal during the switching duration of dead-time. Transistors M_{B1}~M_{B3} compose the biasing circuit. A symmetric common-gate input stage which separately composed by transistor input pairs M_1, M_3, and M_2, M_4 form the input voltage detector. For the operation of ABS circuit, transistor M_1 forms the diode connection and biased by transistor M_{B1}. A dropping voltage generates gate-source voltage V_{GS} of transistor M_1 and be used to bias transistor M_3. Once the gate-source voltage V_{GS} of transistor M_3 is slightly higher or lower than that of transistors M_1, the transistor M_3 can be turned on or off through the designed transconductance gm_3 of transistor M_3. Thus, full symmetric structure which is used to detect the drain and source terminals of p-MOFET is composed of transistors M_1~M_4. The biasing current clamps power consumption owing to limited value of biasing current (I_B). Transistors M_1 and M_3 form the input pair to detect the condition that voltage of output terminal V_{OT} is larger than that of node V_X and connect the output terminal V_{OT} through transistor M_3. Transistors M_2 and M_4 detect the condition that node V_X is larger than output

terminal V_{OT} and connect the node V_X through transistor M_4. Therefore, when the voltage level of node V_X is larger than that of output terminal V_{OT} during the time interval of dead-time process, transistor M_4 is turned on and the body terminal V_B connects to node V_X. Contrarily, when the voltage level of node V_X is smaller than that of output terminal V_{OT} during paths 4 or 3, the body terminal V_B connects to output terminal V_{OT}. The simulation result is shown in Fig. 57. A triangular waveform and a DC level are used to test the performance of proposed ABS circuit. The result shows only 20mV deviation from the highest voltage level and the accurately compares the voltage level of terminals V_X and V_{OT}.

3.7 Reference Voltage and Power-On Reset Circuit

For accurately regulation of multiple-output terminals over the temperature range of -40 ^{o}C~120 ^{o}C, the temperature-independent reference source is essential in SIMO converter. Two quantities having opposite temperature coefficients (TCs) are added with proper weighting, the result displays a zero TC. Thereby, we must identify two voltages that have positive and negative TCs. The forward voltage (V_{BE}) of base-emitter junction in bipolar transistor or the forward voltage (V_F) of *pn*-junction diode exhibits a negative TC. When two bipolar transistors operate at unequal current densities, then the difference between their base-emitter voltages (V_{BE}) is directly proportional to the absolute temperature. With the negative and positive-TC voltages obtained above, we can develop reference having a nominally zero-TC. Assuming that $V_{BG} = \alpha_1 V_{BE} + \alpha_2 (V_T \ln n)$, where $V_T \ln n$ is the difference between the base-emitter voltages of two bipolar transistors operating at different current densities. Since at room temperature $\partial V_{BE} / \partial T \approx -1.5mV / \partial T$ whereas $\partial V_T / \partial T \approx +0.087mV / ^{o}K$, to set $\alpha_1 = 1$ and settle $\alpha_2 \ln n$ such that $(\alpha_2 \ln n)(0.087mV / ^{o}K) = 1.5mV / ^{o}K$. That is $\alpha_2 \ln n \approx 17.2$. Equation (32) indicates that for zero-TC.

$$V_{BG} \approx V_{BE} + 17.2V_T \approx 1.25V \tag{32}$$

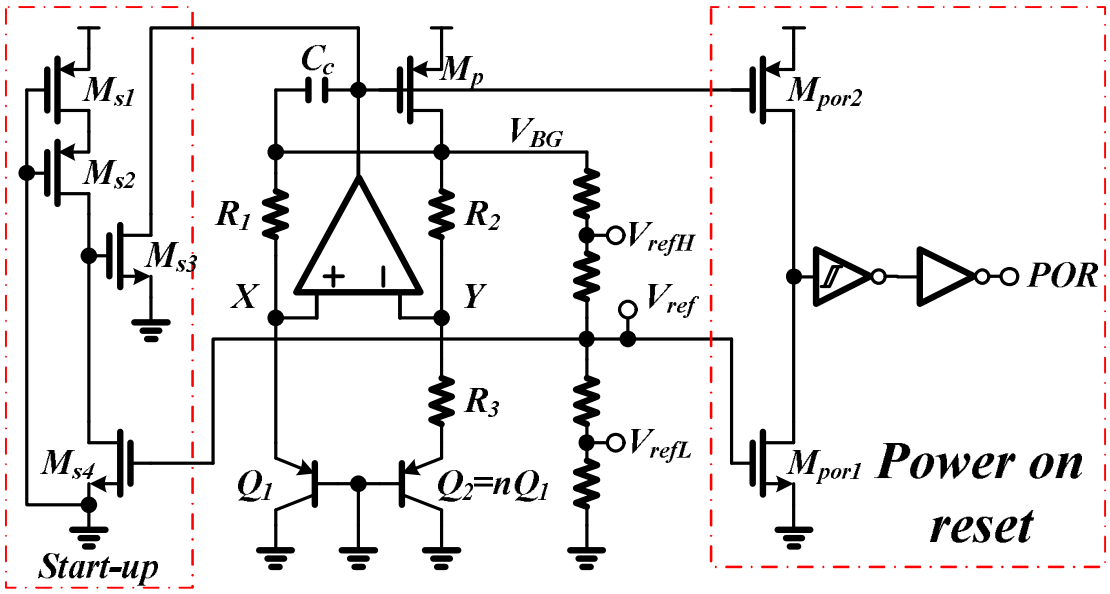


Fig. 58. The schematic of bandgap reference circuit.

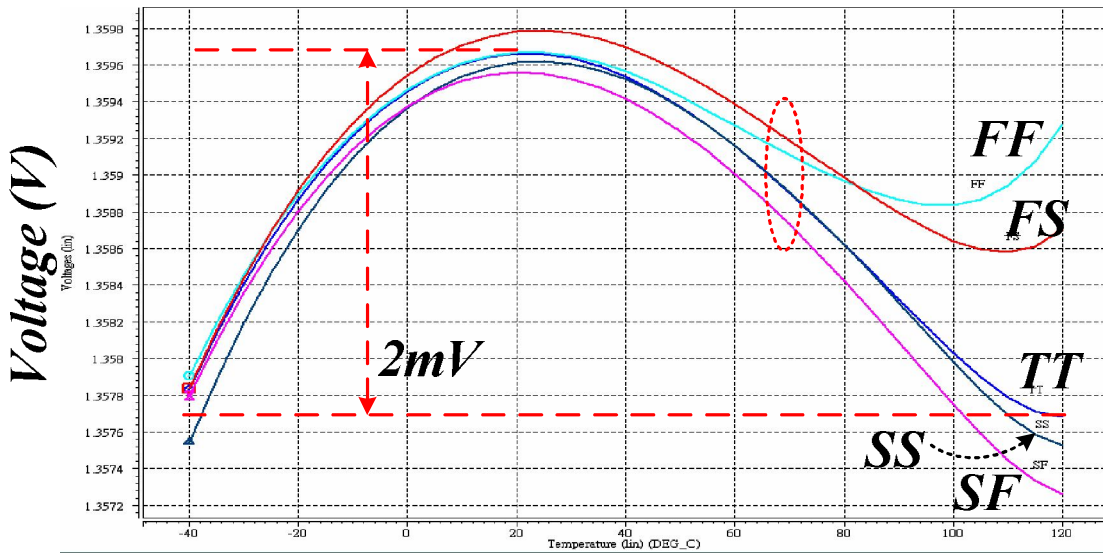


Fig. 59. The simulation result of bandgap reference circuit at five model corners.

The bandgap reference circuit is shown in Fig. 58. Error amplifier sense nodes V_X and V_Y, driving top terminal of resistors R_1 and R_2 (R_1=R_2) such that such that nodes X and Y settle to approximately equal voltage. The reference voltage (V_{BG}) is obtained at the output terminal of error amplifier. Hence an output voltage can be expressed as (33). For a zero-TC, we have $(1+R_2/R_3)\ln n \approx 17.2$.

$$V_{BG} = V_{BE2} + \left(1+\frac{R_2}{R_3}\right)V_T \ln(n) \tag{33}$$

Transistors M_{s1}, M_{s2}, M_{s3}, and M_{s4} compose startup circuit. Transistors M_{por1} and M_{por2} compose power-on reset circuit and generate output signal *POR*. Before reference voltage (V_{BG}) is ready, the output voltage (V_{ref}) is zero level. Transistors M_{s4} and M_{por1} turn off. Transistor M_{s3} turns on to pull low the gate biasing of transistors M_p and M_{por2}. The output state of power-on reset circuit switches to high state. Owing to transistor M_p turns on, the error amplifier starts to force voltage of nodes *X* and *Y* for difference of two base-emitter voltage. While the bandgap voltage (V_{BG}) is build, transistors M_{s4} and M_{por1} turn on. Therefore, transistor M_{s3} turns off and startup process is ended. The output signal *POR* of power-on reset circuit sets to low state and enables the clock generator. The simulation result with over-temperature and five corners is shown in Fig. 59.

Chapter 4

Power Comparator and Delta-Voltage Generator

4.1 Power Comparator Circuit

To smoothly switch between PWM and hysteresis operation modes, the power comparator and delta-voltage generators are proposed to decide the operation mode of SIMO converter. The inductor current waveform (I_L) as depicted in Fig. 60 precisely describes the boundary condition between the PWM and hysteresis modes. Assume that the current slopes m_{K1}~m_{Kn} and m_{T1}~m_{Tm} of the inductor current (I_L) for the buck and boost output terminals are expressed as (34) and (35), respectively. The value of suffix *i* is from *1* to *n* for buck output terminal *i* and the value of suffix *j* is from *1* to *m* for boost output terminal *j*. The operation modes and boundary condition can be determined by comparing the total charge of buck output terminals operation with total charge of multiple boost output terminals operation. Therefore, the equation (36) expresses the charge-condition in PWM mode. Equation (37) represents the charge-condition in hysteresis mode. Thus, when the total charge of buck output terminals is equal to that of boost output terminals, the boundary condition which is charge-balance condition and expresses in (38) is used to judge the operation mode of SIMO converter.

$$m_{Ki} = \frac{V_{IN} - V_{OKi}}{L} \quad \text{for buck output terminal } i \tag{34}$$

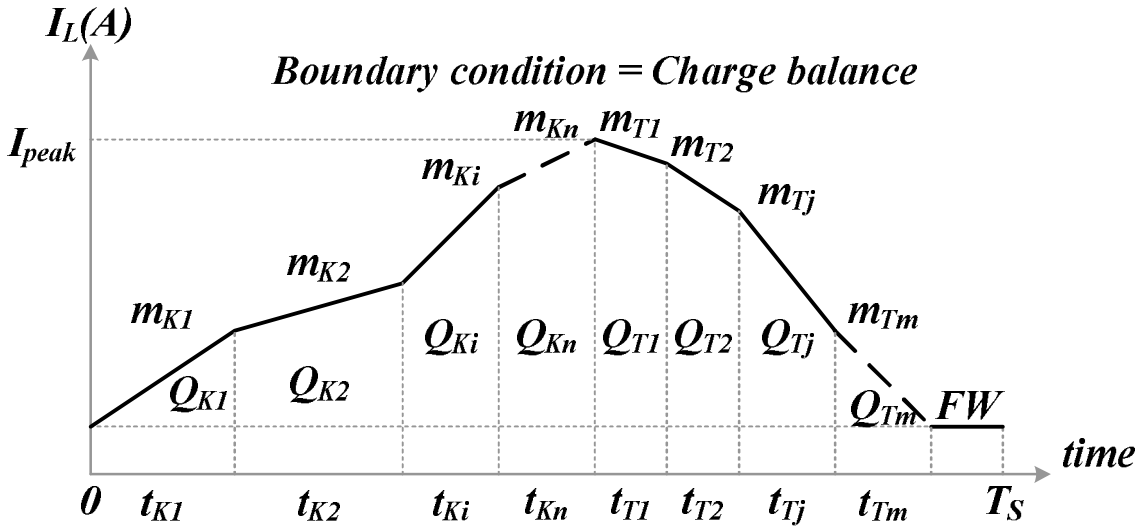


Fig. 60. the boundary condition between the PWM and hysteresis modes

$$m_{Tj} = \frac{V_{OTj} - V_{IN}}{L} \quad \text{for boost output terminal } j \tag{35}$$

$$\sum_{i=1}^{n} m_{Ki} t_{Ki} < \sum_{j=1}^{m} m_{Tj} t_{Tj} \rightarrow \sum_{i=1}^{n} Q_{Ki} < \sum_{j=1}^{m} Q_{Tj} \quad \text{for PWM mode operation} \tag{36}$$

$$\sum_{i=1}^{n} m_{Ki} t_{Ki} > \sum_{j=1}^{m} m_{Tj} t_{Tj} \rightarrow \sum_{i=1}^{n} Q_{Ki} > \sum_{j=1}^{m} Q_{Tj} \quad \text{for hysteresis mode operation} \tag{37}$$

$$\sum_{i=1}^{n} m_{Ki} t_{Ki} = \sum_{j=1}^{m} m_{Tj} t_{Tj} \rightarrow \sum_{i=1}^{n} Q_{Ki} = \sum_{j=1}^{m} Q_{Tj} \quad \text{for judgment of operation mode} \tag{38}$$

As illustrated in Fig. 61, the power comparator is used to decide which one of buck output terminals needs to enter hysteresis operation according to the largest load current. The voltage-current converters convert the differential voltage between output voltages and supply voltage into current signal for indicating current slope of inductor L. The summation current I_{mK1} and I_{mT1} of V-I converter indicate the slope values of the buck and boost output terminals, respectively. Summation current I_{mK1} is used to discharge capacitor C_1 during the buck operation, and current I_{mT1} is used to charge capacitor C_1 during boost operation in first loop. At the freewheeling stage, the sample and hold (S/H) circuit sample the voltage on capacitor C_1 and hold it on the capacitor C_2. Thus, the boundary condition is monitored by the slope

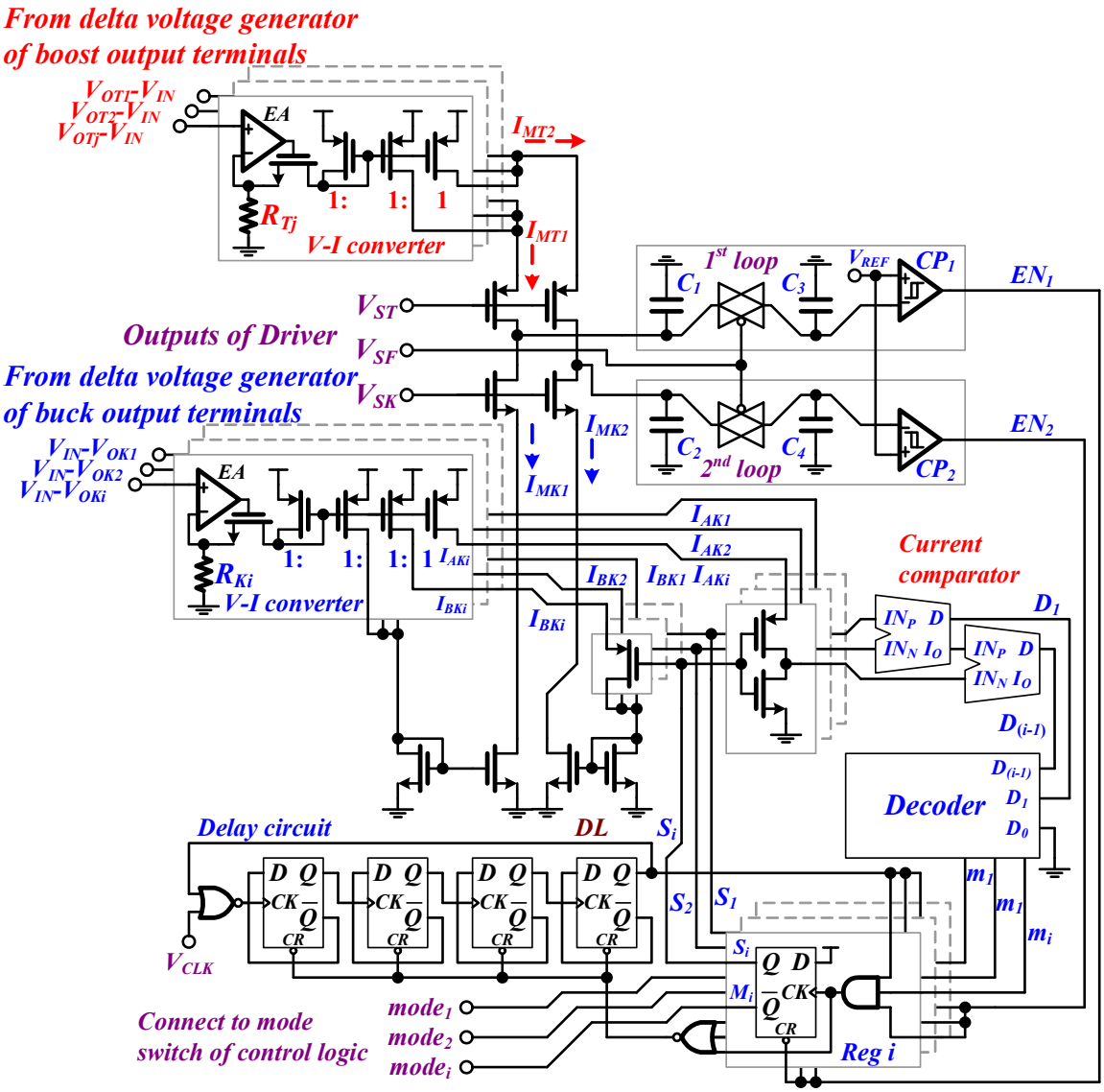


Fig. 61. The schematic of proposed power comparator circuit

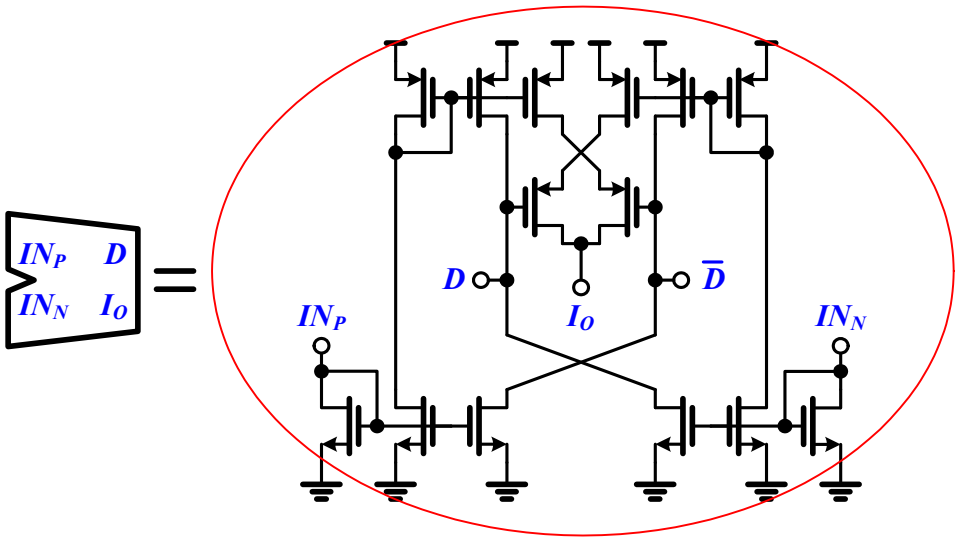


Fig. 62. The current comparator of proposed power comparator circuit.

values of buck and boost output terminals. In the operation condition of PWM mode, the value of summation current I_{MK1} is smaller than that of summation current I_{MT1}, and output signal EN_1 of comparator CP_1 is set to a low state in the first loop. That is, the power comparator circuit is disabled. The output signals M_1~M_i of registers *Reg.1*~*Reg.i* are set to a low state to disable the mode switch of control logic circuit in Fig. 40. Besides, the internal signals S_1~S_i are set to low state. The mirrored current signals I_{BK1}~I_{BKi} sum up in I_{MK2}, which is used to compare with summation current I_{MT2} of boost output terminals in second loop. The other mirrored current signals I_{AK1}~I_{AKi} of *V-I* converter are switched to detect the highest current level by current comparator which is shown in Fig. 62.

When the power level of buck output terminals are larger than that of boost output terminals, the output signals EN_1 and EN_2 of comparators CP_1 and CP_2 is set to high state. The power comparator circuit is enabled and decides the buck output terminal with highest output load condition into hysteresis mode. Thus, the mirrored current signals I_{BK1}~I_{BKi} sum up in I_{MK2}, and all mirrored current signals I_{AK1}~I_{AKi} of the delta-voltage generator for buck are separately switched to detect the highest slope by the current comparators. In the meanwhile, the generated summation current I_{MK2} compares with current I_{MT2} and outputs the high state of output signal EN_2 in the second loop. This second loop is designed to detect operating mode of each buck output according to the buck output with the largest load current selected for hysteresis mode. When the output signal EN_2 is high state, the trigger signals of registers *Reg.1*~*Reg.i* are enabled by output signal EN_2 and output signal *DL* of delay circuit. The delay circuit is enabled to avoid the oscillation of the second loop and to ensure the storage charge in the steady state when one of the buck output terminals enters hysteresis mode. Current signals I_{AK1}~I_{AKi} flow into the current comparator and generate the detecting codes D_1~$D_{(i-1)}$ during the delay period of delay circuit. The detecting code is converted to indicate which one of the buck output terminals has the highest load condition and needs to operate in hysteresis mode. The detecting code can be expressed as (39).

$$m_1 = \left(D_1 \cdot D_2 \cdot \ldots \cdot D_{(X-1)} \cdot D_X \cdot \ldots \cdot D_{(n-1)}\right),\ \ m_2 = \left(\overline{D_1} \cdot D_2 \cdot \ldots \cdot D_{(X-1)} \cdot D_X \cdot \ldots \cdot D_{(n-1)}\right),\ \ldots,$$

$$m_X = \left(\overline{D_{(X-1)}} \cdot D_X \cdot D_{(X+1)} \ldots \cdot D_{(n-1)}\right),\ \ldots,\ \ m_i = \left(\overline{D_{(i-1)}}\right) \qquad (39)$$

where the suffix X is from *1* to i. Once one of the buck output terminals is selected, m_X triggers register *Reg.X* to set the output signal $mode_X$ of power comparator to a low state. Moreover, the inverse signal S_X of output signal $mode_X$ inhibits the related current signals I_{AKX} and I_{BKX}. As a result, summation current I_{MK2} can be expressed as (40)

$$I_{MK2(n)} = I_{MK2(0)} - I_{BKX(1)} - I_{BKX(2)} - \ldots - I_{BKX(n)} \quad \text{for } n^{th} \text{ operation of second loop} \qquad (40)$$

where the suffix n is used to indicate the n operating-times of the second loop. $I_{MK2(n)}$ and $I_{BKX(n)}$ are the current signals by the n^{th} operation of the second loop according to the priority of load condition. Once current $I_{MK2(n)}$ is smaller than current I_{MT2}, output signal EN_2 of comparator CP_2 is set back to low state. That is, the charge-detection process is ended, and the proposed converter can really avoid the current accumulation and minimize the output ripples of the buck output terminals in hysteresis mode. The hysteresis mode operates until current level of summation current I_{MK1} is smaller than that of summation current I_{MT1}. The output signal EN_1 of comparator CP_1 is set to low, and the hysteresis mode is switched to PWM mode.

4.2 Delta-Voltage Generator

To generate an accurately inductor current slope signal for power comparator circuit, a novel delta-voltage generator is proposed in Fig. 63 and 64. The delta-voltage generator depend on the definitions of equations (34) and (35) to generate the different inductor current slopes for the smooth switching between hysteresis and PWM operation modes. In order to meet the input common-mode range of delta-voltage generator and measure buck and boost output voltages, two delta-voltage amplifiers with different input types are proposed for the

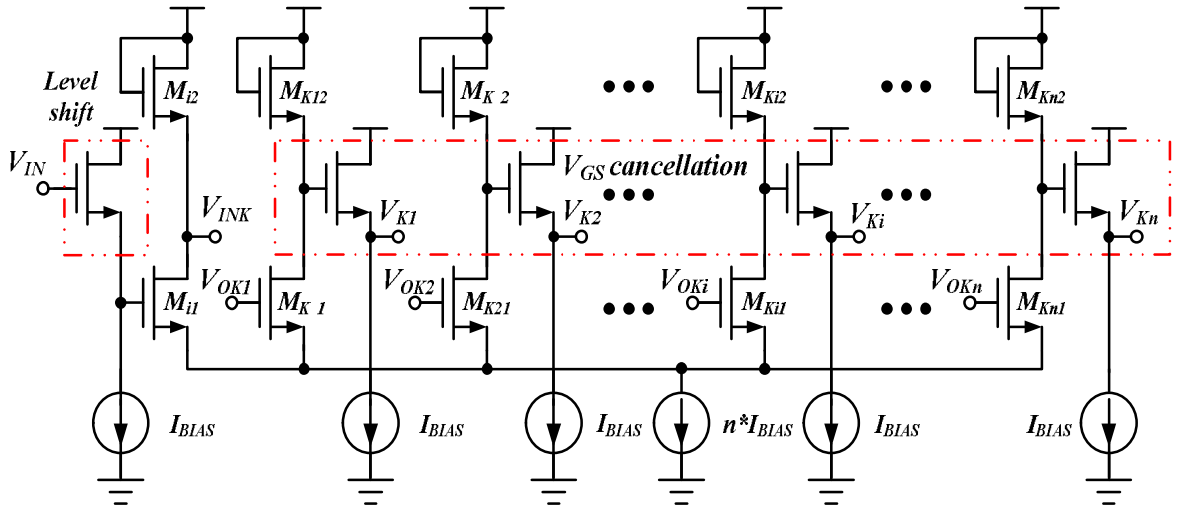


Fig. 63. The proposed novel delta-voltage generator is used to generate the intermediate value according to the multiple buck output load conditions.

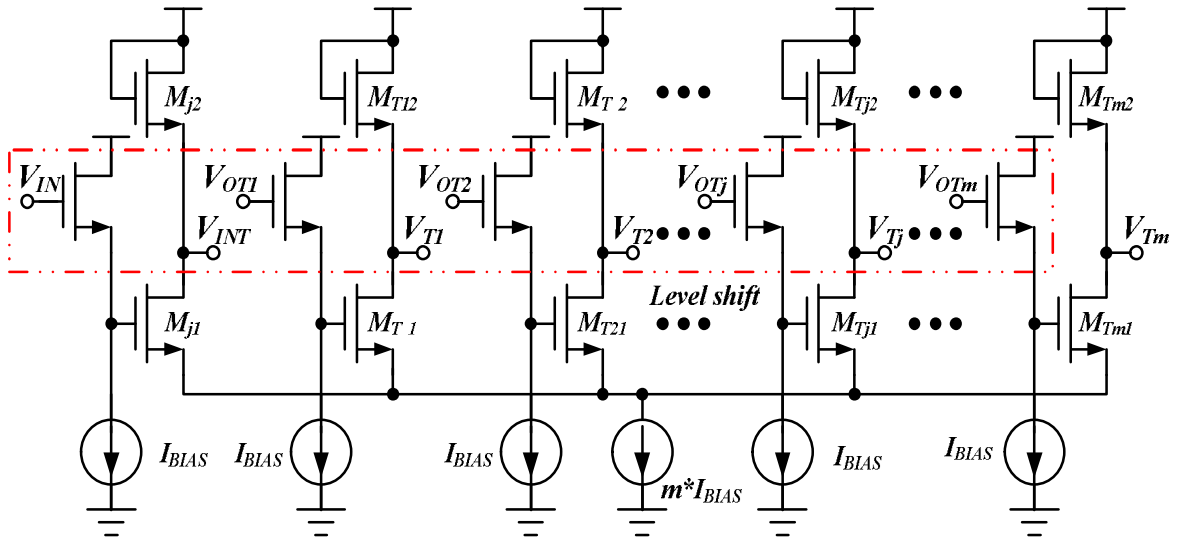


Fig. 64. The proposed novel delta-voltage generator is used to generate the intermediate value according to the multiple boost output load conditions.

amplifier with multiple-output voltages including V_{OK1}~V_{OKn} and supply voltage V_{IN} is depicted in Fig. 63. The block of the V_{GS} cancellation is used to remove the V_{GS} term in the difference voltage between V_{IN} and V_{OKi}. The delta-voltage amplifier with multiple output voltages is used to generate the intermediate values. The intermediate values V_{INK} and V_{K1}~V_{Kn} in delta-voltage amplifier of buck output terminals are expressed as (41). Similarly, for the multiple boost output terminals, the amplifier with multiple output voltages as shown

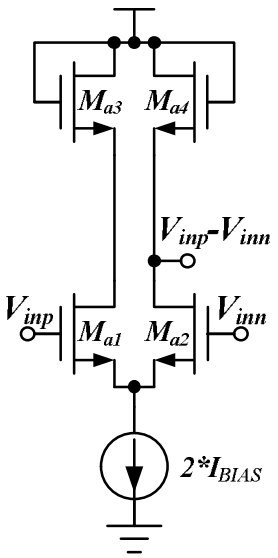


Fig. 65. The differential transconductance amplifier for the generation of the inductor current slope.

in Fig. 64 can generate intermediate values. The intermediate values V_{INT} and V_{T1}~V_{Tm} in delta-voltage amplifier of boost output terminals are expressed as (42). Thus, the current slopes m_{Ki} and m_{Tj} can be derived as (41) and (42) which are implemented by the differential transconductance amplifier as illustrated in Fig. 65. The input signals V_{inp} and V_{inn} of differential transconductance amplifier are connected to the output terminal of the delta-voltage generator. Therefore, the current slope m_{K1}~m_{Kn} and m_{T1}~m_{Tm} of buck and boost output terminals are derived as (43) and (44), respectively.

$$\begin{bmatrix} V_{INK} \\ V_{K1} \\ V_{K2} \\ \vdots \\ V_{Kn} \end{bmatrix} = \frac{1}{n} \begin{bmatrix} (1-n) & 1 & 1 & \cdots & 1 \\ 1 & (1-n) & 1 & \cdots & 1 \\ 1 & 1 & (1-n) & \cdots & 1 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \cdots & (1-n) \end{bmatrix} \begin{bmatrix} V_{IN} \\ V_{OK1} \\ V_{OK2} \\ \vdots \\ V_{OKn} \end{bmatrix} + (n-1) \times V_{GS} \tag{41}$$

$$\begin{bmatrix} V_{INT} \\ V_{T1} \\ V_{T2} \\ \vdots \\ V_{Tm} \end{bmatrix} = \frac{1}{m} \begin{bmatrix} (1-m) & 1 & 1 & \cdots & 1 \\ 1 & (1-m) & 1 & \cdots & 1 \\ 1 & 1 & (1-m) & \cdots & 1 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & 1 & \cdots & (1-m) \end{bmatrix} \begin{bmatrix} V_{IN} \\ V_{OT1} \\ V_{OT2} \\ \vdots \\ V_{OTm} \end{bmatrix} + m \times V_{GS} - \sum_{j=1}^{m} V_{GSj} \tag{42}$$

$$\begin{bmatrix} m_{K1} \\ m_{K2} \\ \vdots \\ m_{Kn} \end{bmatrix} = \begin{bmatrix} V_{K1} \\ V_{K2} \\ \vdots \\ V_{Kn} \end{bmatrix} - V_{INK} = V_{IN} - \begin{bmatrix} V_{OK1} \\ V_{OK2} \\ \vdots \\ V_{OKn} \end{bmatrix} \quad \text{for buck output terminals} \tag{43}$$

$$\begin{bmatrix} m_{T1} \\ m_{T2} \\ \vdots \\ m_{Tm} \end{bmatrix} = V_{INT} - \begin{bmatrix} V_{T1} \\ V_{T2} \\ \vdots \\ V_{Tm} \end{bmatrix} = \begin{bmatrix} V_{OT1} \\ V_{OT2} \\ \vdots \\ V_{OTm} \end{bmatrix} - V_{IN} \quad \text{for boost output terminals} \tag{44}$$

All of output voltages m_{K1}~m_{Kn} and m_{T1}~m_{Tm} of delta-voltage generator are sent to the input terminals of the power comparator circuit in Fig. 61. Therefore, the smooth transition between the PWM and hysteresis modes can be determined.

Chapter 5

Measurement Results

The proposed SIMO DC-DC converter with the LDPCC technique was implemented in TSMC 0.25μm 2P5M technology. The micrograph of the SIMO DC-DC converter with 4 output terminals is shown in Fig. 66. The supply voltage is 1.8V. The pre-defined output voltages are 1.25V and 1.35V for the two buck output terminals and 2.0V and 2.25V for the two boost output terminals, respectively. The measured inductor current waveform (I_L) of the PWM mode at heavy loads is shown in Fig. 67. The ac coupling measurement of LDPCC level V_{Ipeak} clearly shows the controlling sequence-II in the inductor current (I_L), which is similar to the description in the previous section as illustrated in Fig. 25.

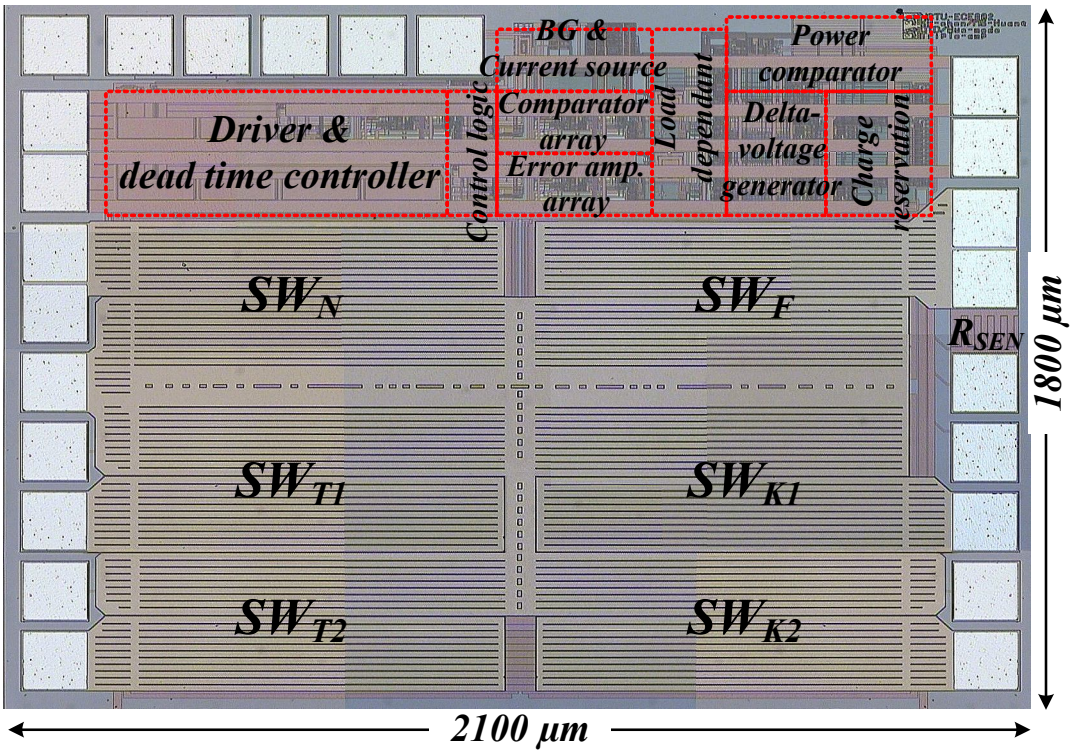


Fig. 66. Micrograph of the proposed SIMO converter and the chip size is 1800*2100μm^2.

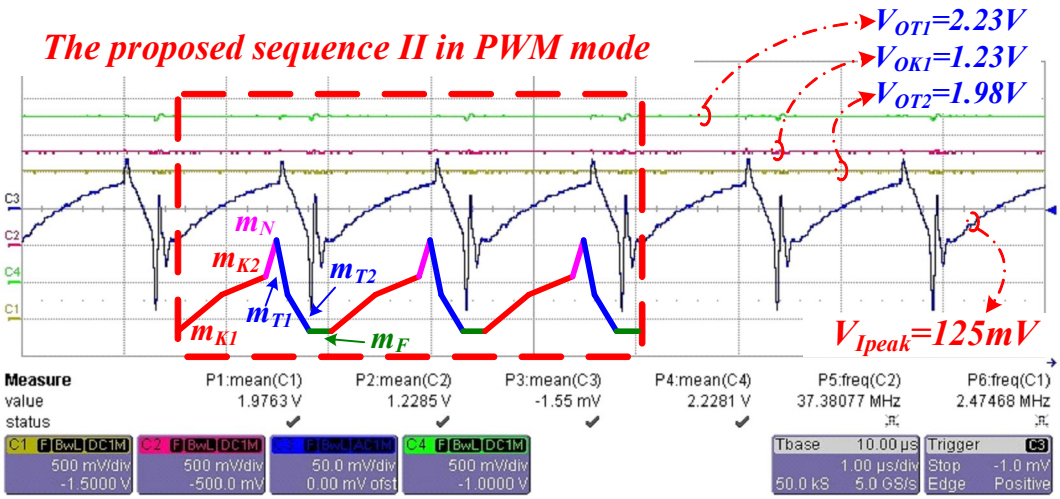


Fig. 67. The inductor current controlling sequence measured waveform with heavy loads.

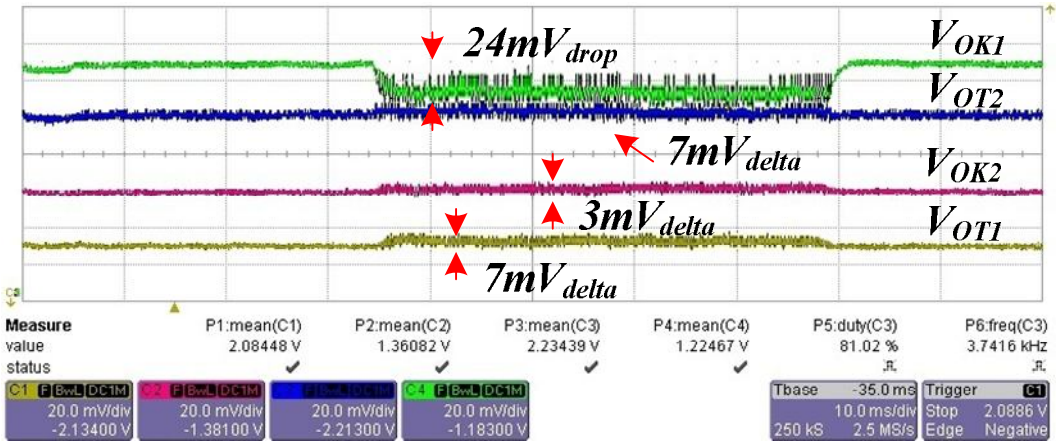


Fig. 68. The measurement of load regulation and cross-regulation when a stepping load (10mA to 100mA) at the buck output terminal VOK1.

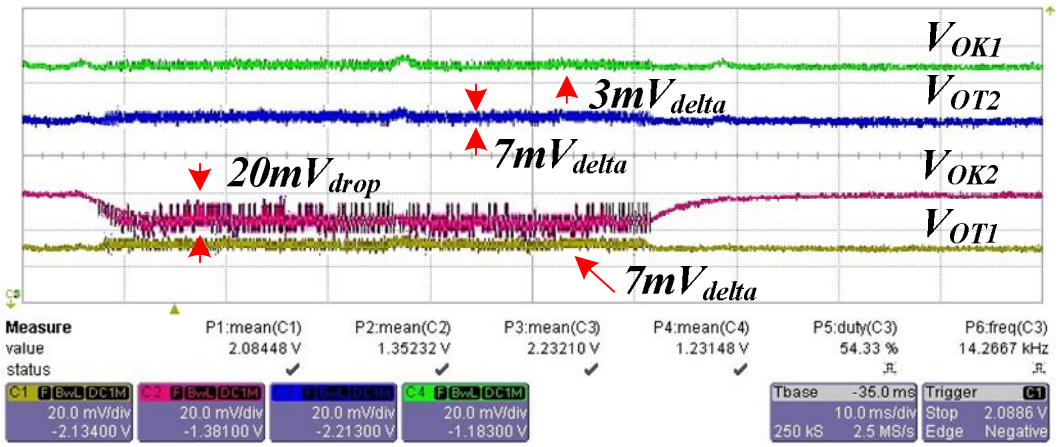


Fig. 69. The measurement of load regulation and cross-regulation when a stepping load (10mA to 100mA) at the buck output terminal VOK2.

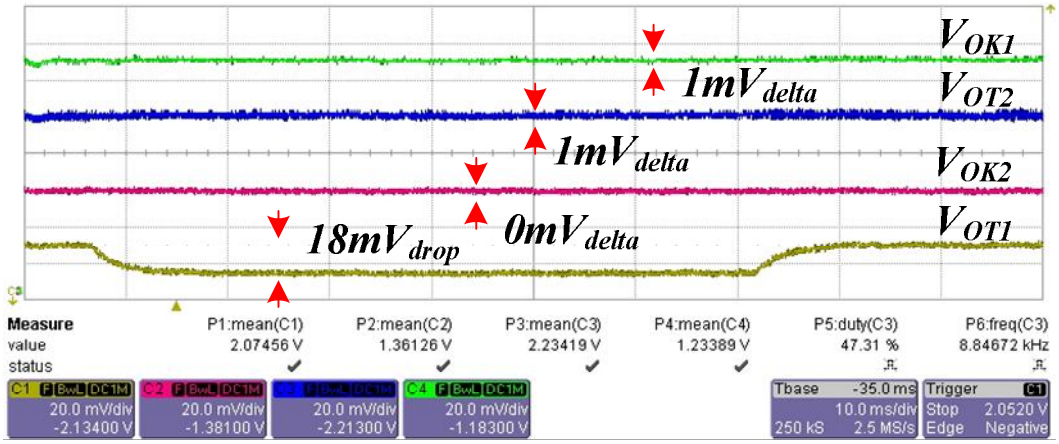


Fig. 70. The measurement of load regulation and cross-regulation when a stepping load (10mA to 100mA) at the boost output terminal VOT1.

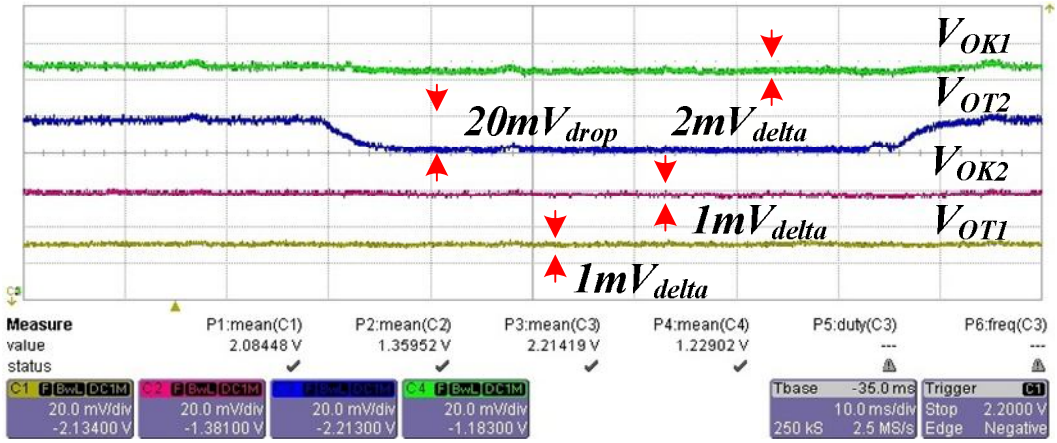


Fig. 71. The measurement of load regulation and cross-regulation when a stepping load (10mA to 100mA) at the boost output terminal VOT2.

The measurements of load transient and cross-regulation are shown in Fig. 68~71. As the measurement results which are shown in Fig. 68 and 69, a stepping load condition (10mA to 100mA) is added to buck output terminals V_{OK1} and V_{OK2}, respectively. Since the output power of buck output terminals is larger than that of boost output terminals, the hysteresis mode is enabled for avoiding the current accumulation issue. Hence, the output terminals V_{OK1} and V_{OK2} are directly regulated by path 0 which turns on the freewheeling switch M_{SWF} and isolation switches M_{SWK1} and M_{SWK2} at the same time. However, the output ripples of terminals V_{OK1} and V_{OK2} are increased by path 0 since the inductor L has been passed.

Therefore, large output capacitors C_{OK1} and C_{OK2} are necessary to reduce output ripples, but greatly decrease the transient response at stepping load transition. Besides, the noise which comes from large ripple of buck output terminals V_{OK1} and V_{OK2} couples to other output terminals and lowers lower load-regulation and cross-regulation. Similarly, a stepping load condition (10mA to 100mA) is respectively added to boost output terminals V_{OT1} and V_{OT2} which are shown in Fig. 70 and 71. Since the output power of buck terminals is smaller than that of boost terminals, the hysteresis mode is disabled and PWM mode is used to regulate output voltages. Output ripple of PWM mode is smaller than that of hysteresis mode.

Since large information was measured, the statistic charts are used to describe the performance of the proposed converter. The cross-regulation charts of the buck and boost output voltages are shown in Fig. 72 and 73, respectively. In Fig. 72, the load current of 50mA is added to the boost output terminals in order to show the cross-regulation of different operation modes. This indicates that the hysteresis mode increases the cross-regulation from 0.07% to 0.22%. Similarly, the cross-regulation of the boost output V_{OT1} is shown in Fig. 73. It is slightly increased from 0.05% to 0.35% in the hysteresis mode. It is smaller than the value of 0.79% in the pervious works. The line- and load-regulation charts of the buck output in PWM and hysteresis modes are shown in Fig. 74 and 75. In the PWM mode, the boost converter is operated at heavy loads. Contrarily, in the hysteresis mode, the boost converter is operated at light loads. The line-regulations of the buck output voltages are smaller than 0.8%/V, and the load-regulations of the buck output voltages are smaller than 2% in the two operating modes. Figure 76 and 77 show the boost output voltages in the PWM and hysteresis modes. The results depict that the line- and load-regulations between the two modes are similar. The load-regulations of the boost output voltages are smaller than 1%, and the line-regulations of the boost output voltages are smaller than 0.5%/V. The output ripples of the buck and boost output voltages are depicted in Fig. 78 and 79. In the PWM mode, the output ripple is controlled by the values of the inductor and output capacitor, and thus the

value is smaller than 4m$V_{P\text{-}P}$. In the hysteresis mode, the output ripple of the buck output voltages is increased to 22m$V_{P\text{-}P}$, and the output ripple of the boost output voltages is increased to 6m$V_{P\text{-}P}$. The power conversion efficiency is shown in Fig. 80. The PWM operation with load-dependent peak-current control has improved highly power conversion efficiency from 85% to 93%. In the hysteresis mode, due to the energy delivering path without flowing through the inductor, the conversion efficiency drops to 80%~85%. The performance of the SIMO DC-DC converter is summarized in Table II.

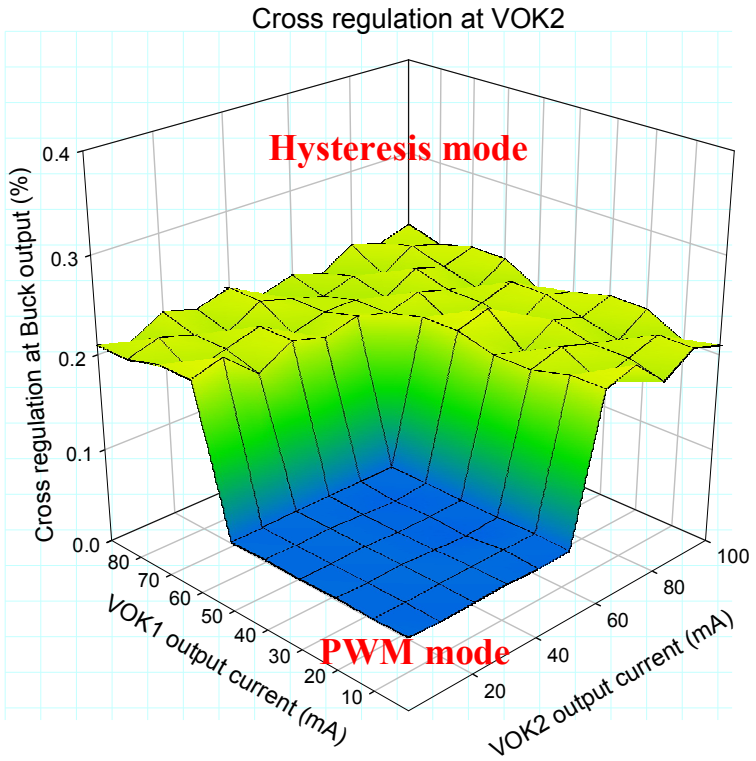


Fig. 72. The cross-regulation at the buck output V_{OK2} in the PWM and hysteresis modes.

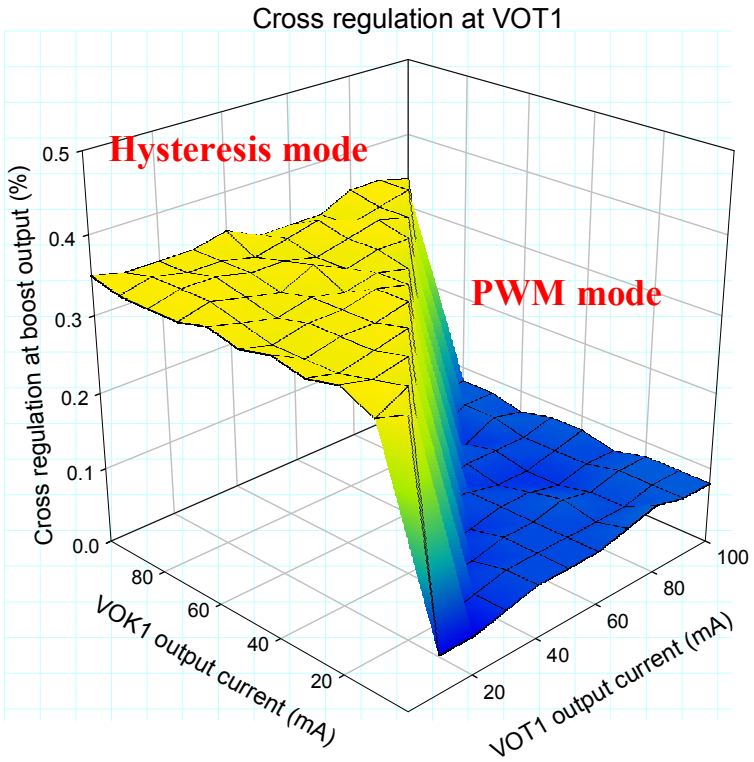


Fig. 73. The cross-regulation at the boost output V_{OT1} in the PWM and hysteresis modes.

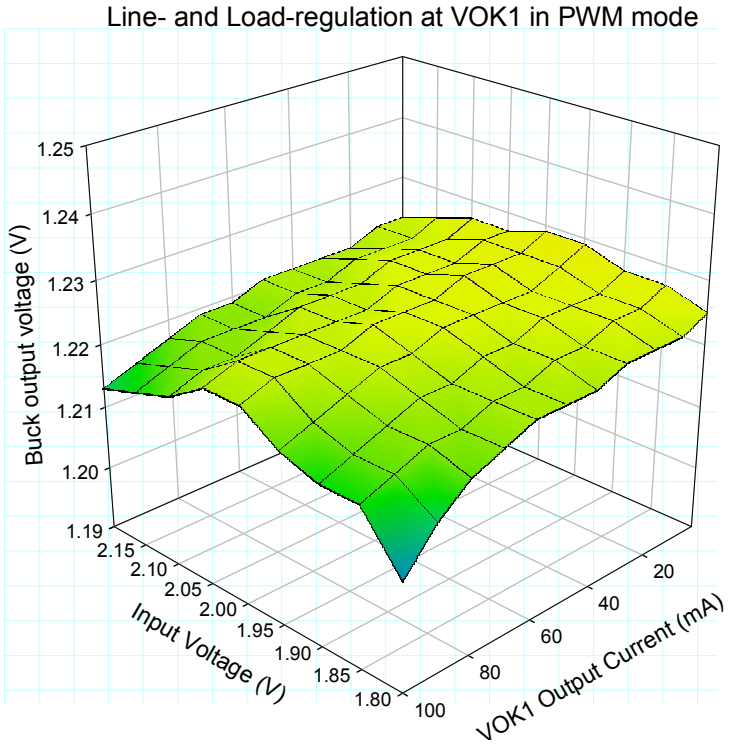


Fig. 74. The buck outputs operate in the PWM mode when boost outputs operate at heavy loads.

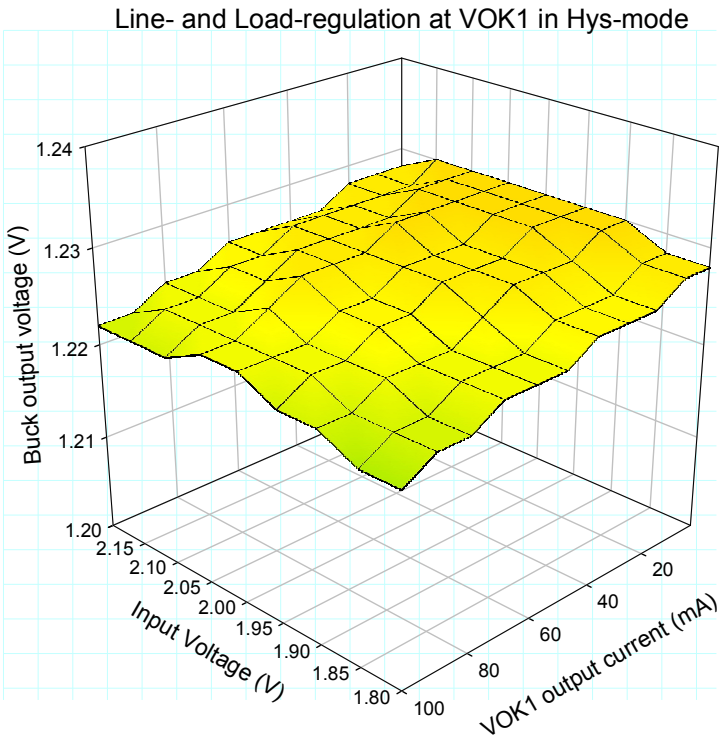


Fig. 75. The buck outputs operate in the hysteresis mode when the boost outputs operate at light loads.

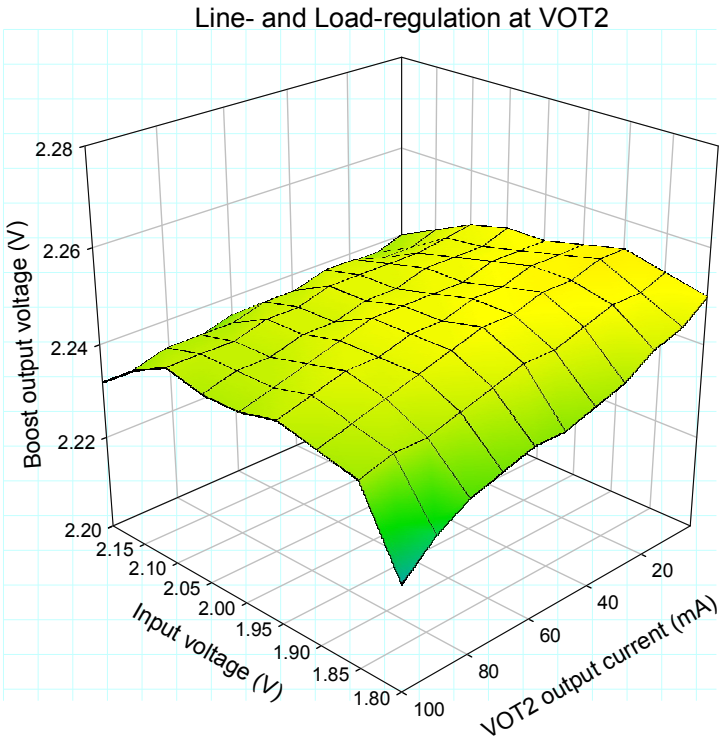


Fig. 76. The boost outputs in the PWM mode when the buck outputs operate at light loads.

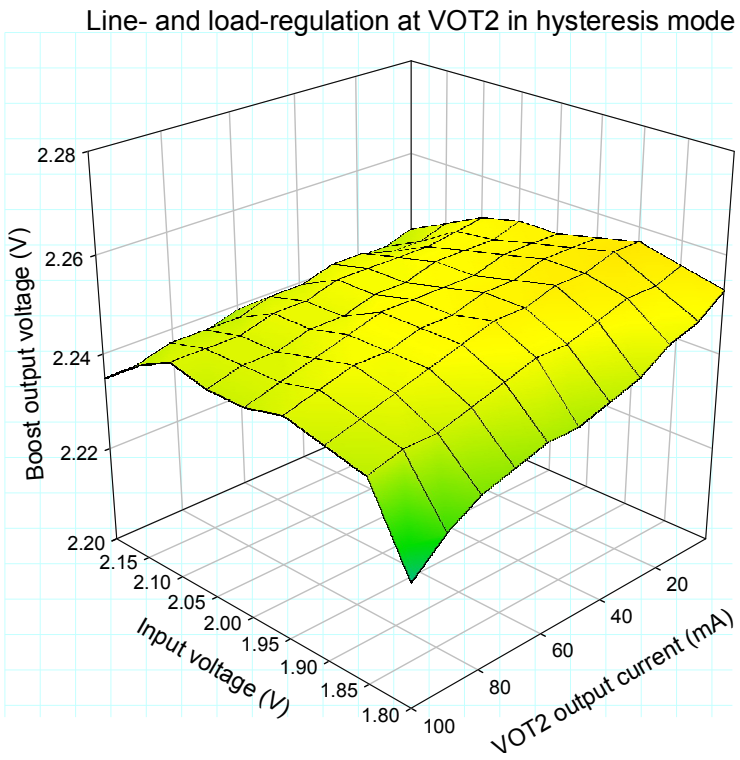


Fig. 77. The boost outputs in the hysteresis mode when the buck outputs operate at heavy loads.

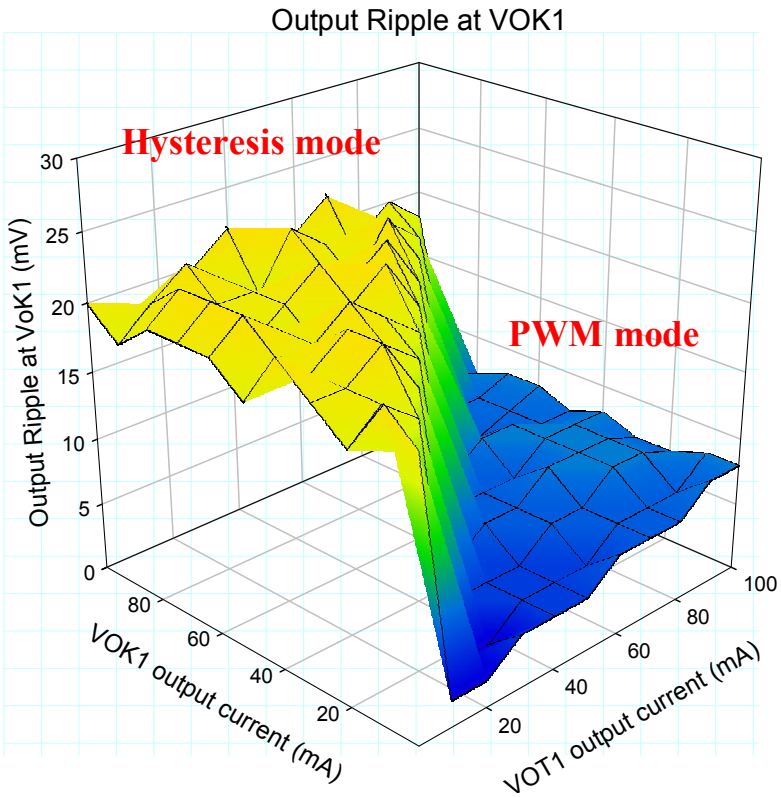


Fig. 78. The output ripples estimation of buck output in the SIMO converter.

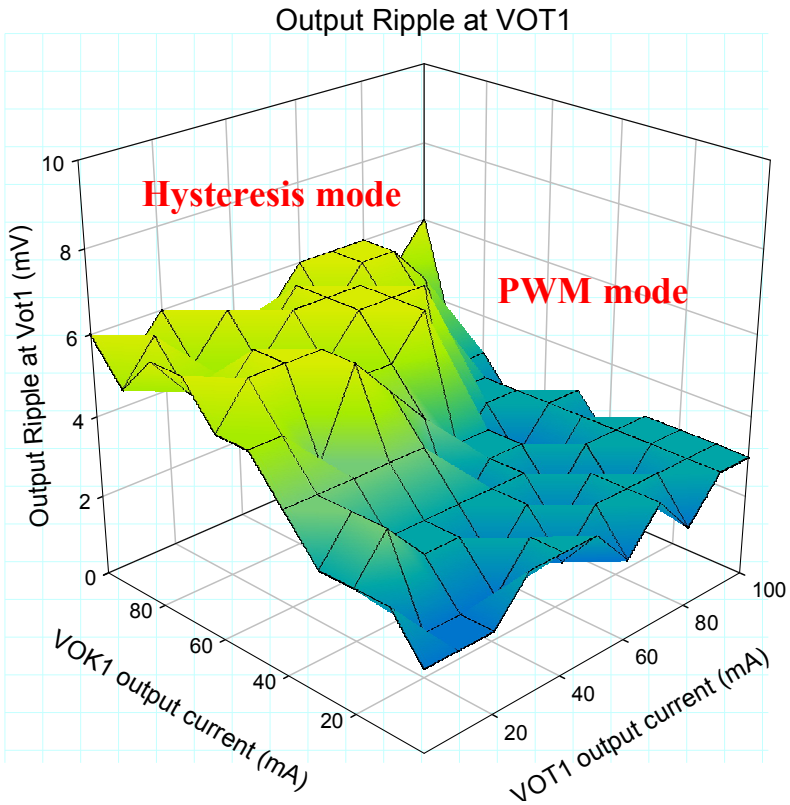


Fig. 79. The output ripples estimation of boost output in the SIMO converter.

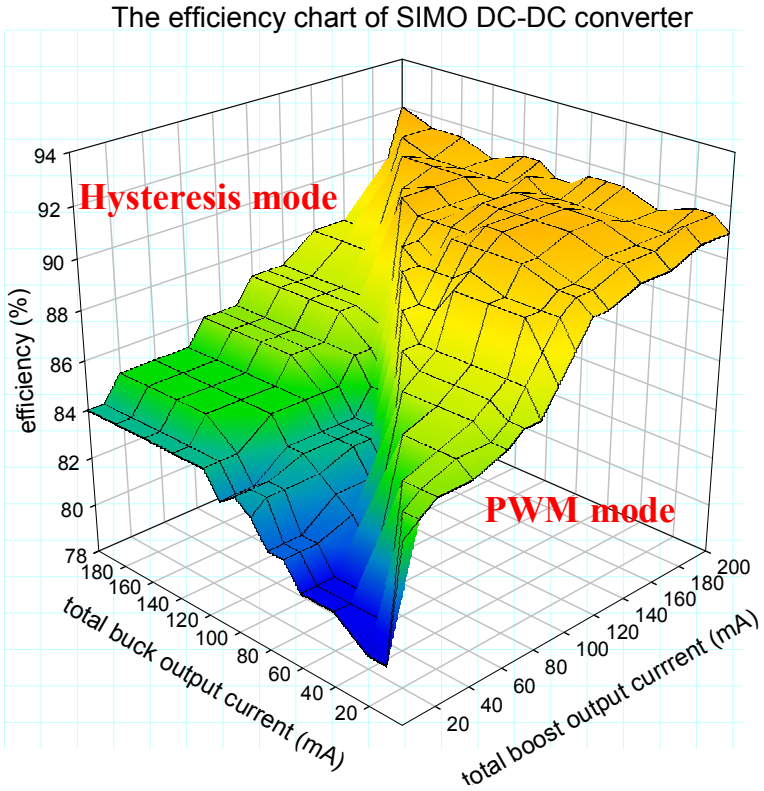


Fig. 80. The power conversion efficiency of the SIMO DC-DC converter with the LDPCC technique.

Table. II. Summary of the performance.

Supply voltage		1.8V @ temperature = 0 °C ~ 80 °C			
Inductor		10 μH (±10%)			
Filter capacitor		33 μF with low ESR (small than 50mΩ)			
Switching frequency		660 kHz			
Process		TSMC 0.25μm 2P5M CMOS			
Chip area		1800*2100μm^2			
Converters		$Buck_1$ (V_{OK1})	$Buck_2$ (V_{OK2})	$Boost_1$ (V_{OT1})	$Boost_2$ (V_{OT2})
Output voltage		*1.25V*	*1.35V*	*2.0V*	*2.25V*
Output ripples	PWM mode	*4mV*		*3mV*	
	Hysteresis mode	*22mV*		*6mV*	
Load-regulation		*2%*	*1.5%*	*1%*	*0.9%*
Line-regulation		*0.8%/V*	*0.55%/V*	*0.5%/V*	*0.4%/V*
Cross-regulation	V_{OK1} at heavy load	*NA*	*0.22%*	*0.35%*	*0.31%*
	V_{OK2} at heavy load	*0.24%*	*NA*	*0.35%*	*0.31%*
	V_{OT1} at heavy load	*0.08%*	*0.074%*	*NA*	*0%*
	V_{OT2} at heavy load	*0.16%*	*0.074%*	*0.05%*	*NA*
Conversion efficiency	PWM mode	*90%*		*93%*	
	Hysteresis mode	*80%*		*NA*	

Chapter 6

Conclusions and Future Works

6.1 Conclusions

In this thesis, the previous techniques of SIMO converter such as state-machine peak current control technique, charge-control (QC) technique, time-multiplex (TM) and PCCM technique, freewheeling current feedback control technique, and OPDC technique has been studied. Since the sub-functions of portable devices need multiple supply voltages are higher or lower than the battery potential, the SIMO converter which can simultaneously provide buck and boost output voltages becomes a very important demand in the field of power IC. The fundamental behavior of SIMO converter is used to analyze basic controlling sequence and simplify the topology of power structure. To combine the QC and PCCM technique in the minimum number of power switches, the proposed controlling sequence-II evolved into an optimal solution. Without wasting any storage charge in the inductor L, the proposed controlling sequence-II can completely distribute the storage charge among the buck and boost output terminals.

Since the high freewheeling current and long freewheeling period of PCCM technique decrease the power conversion efficiency at light load condition, the load-dependant peak-current (LDPCC) technique is proposed to ensure system stability and minimize the power conversion efficiency at load deviation and light load condition, respectively. Furthermore, the cross-regulations of buck and boost output terminals are minimized by the dynamic adjustment of LDPCC current level (I_{peak}). Owing to the proper LDPCC level (I_{peak})

adaptively controls the storage charge in form of inductor current (I_L), output terminals can be regulated stably without over- or under-charge issue.

In order to achieve the flexibility of output terminals, the proposed design of control logic has been designed into a repeatable module. According to the required supply voltages of portable device, the control logic can arbitrarily increase or decrease the number of output terminals. Since the used topology of power structure in this thesis has the current accumulation issue during output power of buck terminals is larger than that of boost terminals, the power comparator and delta-voltage generator have been proposed to address the unstable situation. While the boundary condition of current accumulation was detected by power comparator, the extra current path which is path 0 is created by turning on freewheeling switch and buck output switch at the same time. The stability of SIMO converter is achieved, but the large ripple, noise coupling, and low transient response are measured at output terminals.

Furthermore, there has advance circuit in the proposed SIMO converter. The proposed maximum voltage selector not only accurately detects the maximum voltage among supply voltage and output terminals without short through current, but also greatly reduces bias current and transistor number. The flexibility of maximum voltage selector is also achieved. On the other hand, the voltage spike on node V_X causes the possibility of leakage current and latch up loop during the switching duration of power switches. A novel adaptive body switch (ABS) circuit is proposed to adaptively and rapidly select the highest voltage level between drain and source terminal of power switch. Owing to the simplest structure of ABS circuit, the ultra low power consumption and chip area is achieved.

This thesis proposes a compact-size and high power conversion efficiency SIMO converter for portable device. The proposed SIMO converter with minimized switch transistors utilizes only one inductor component to provide multiple buck and boost output voltages. The energy stored in the inductor can effectively deliver to the buck and boost

output terminals without inductor current accumulation issue. In other words, the proposed hysteresis mode operation and the new delta-voltage generator address the current accumulation issue. Therefore, the proposed SIMO converter not only provides multiple buck and boost output voltages but also minimizes the cross-regulation within 0.35%. Furthermore, owing to the LDPCC technique, the SIMO converter achieves high conversion efficiency from 80% at light load condition to 93% at heavy load condition in the experimental results.

6.2 Future Works

The proposed SIMO converter provides the minimum cross-regulation at multiple buck and boost output terminals and higher power conversion efficiency at light load condition. The proposed hysteresis mode addresses current accumulation in inductor while the output power of buck output terminals is large than that of boost output terminals. Since those solutions only address the particular issues in the fewer power switches structure. In order to have future works on single inductor structures, there are many challenges on the studies of SIMO converter. Such as that the minimum controlling loops for reducing chip area and power consumption, the fast transient technique for stepping load transition, a new controlling algorithm for adaptive controlling storage charge in the inductor, and the modeling study of SIMO converter.

References

[1] Erich Bayer, Gerhard Thiele, "A Single-Inductor Multiple-Output Converter with Peak Current State-Machine Control," *Applied Power Electronics Conference and Exposition, 2006. APEC '06. Twenty-First Annual IEEE*, Page(s) 153-159, Mar., 2006.

[2] Suet-Chui Koon, Yat-Hei Lam and Wing-Hung Ki, "Integrated Charge-Control Single-Inductor Dual-Output Step-Up/Step-Down Converter," *IEEE International Symposium on Circuit and Systems*, Vol. 4, Page(s) 3071-3074, May, 2005.

[3] Dongsheng Ma, Wing-Hung Ki, Chi-Ying Tsui, and Philip K. T. Mok, "Single-Inductor Multiple-Output Switching Converters with Time-Multiplexing Control in Discontinuous Conduction Mode," *IEEE Journal Solid-State Circuits*, Vol. 38, No. 1, Page(s) 89-100, Jan., 2003.

[4] Edoardo Bonizzoni, Fausto Borghetti, Piero Malcovati, Franco Maloberti, and Bernhard Niessen, "A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter," *1EEE International Solid-Stat Circuits Conference*, Page(s) 526-527, Feb., 2007.

[5] Marcus W. May, Michael R. May, and John E. Willis, "A Synchronous Dual-Output Switching dc-dc Converter Using Multibit Noise-Shaped Switch Control," *1EEE International Solid-Stat Circuits Conference*, Page(s) 358-359, Feb., 2001.

[6] Pizzutelli, A. and Ghioni, M., "Novel control technique for single inductor multiple output converters operating in CCM with reduced cross-regulation," *Applied Power Electronics Conference and Exposition,* Page(s) 1502-1507, Feb., 2008.

[7] Massimiliano Belloni, Edoardo Bonizzoni, and Franco Maloberti, "On the design of single-inductor multiple-output DC-DC buck converters," *IEEE International Symposium on Circuit and Systems*, Page(s) 3049-3052, May, 2008.

[8] M. Belloni, E. Bonizzoni, E. Kiseliovas, P. Malcovati, F. Maloberti, T. Peltola, and T. Teppo, “A 4-Output Single-Inductor DC-DC Buck Converter with Self-Boosted Switch Drivers and 1.2A Total Output Current,” *1EEE International Solid-Stat Circuits Conference*, Page(s) 444-626, Feb., 2008.

[9] Ming-Hsin Huang, Ke-Horng Chen**,** and Wei-Hsin Wei “Single-Inductor Dual-Output DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices,” *IEEE Symposium on VLSI Circuits*, Page(s) 132-133, June, 2008.

[10] Dongsheng Ma, Wing-Hung Ki, and Chi-Ying Tsui, “A pseudo-CCM/DCM SIMO switching converter with freewheel switching,” *IEEE Journal of Solid-State Circuits,* Vol. 38, Issue 6, Page(s) 1007-1014, June, 2003.

[11] Young-Jin Woo, Hanh-Phuc Le, Gyu-Ha Cho, Gyu-Hyeong Cho, and Seong-Il Kim, “Load-Independent Control of Switching DC-DC Converters with Freewheeling Current Feedback,” *IEEE International Solid-State Conference*, Page(s) 446-626, Feb., 2008.

[12] Anmol Sharma and Y. Shanthi Pavan, “A single inductor multiple output converter with adaptive delta current mode control,” *IEEE International Symposium on Circuit and Systems*, Page(s) 5643-5646, May, 2006.

[13] Hanh-Phuc Le, Chang-Seok Chae, Kwang-Chan Lee, Se-Won Wang, Gyu-Ha Cho, and Gyu-Hyeong Cho, “A Single-Inductor Switching DC–DC Converter With Five Output and Ordered Power-Distributive Control,” *IEEE Journal of Solid-State Circuits,* Page(s) 2706-2714, Dec., 2007.

[14] TPS65120: Single Inductor Quadruple Output TFT LCD Power Supply. Texas Instruments, Inc., Dallas, TX, 2005. [Online]. Available: http://www.ti.com/

[15] MAX1518: TFT-LCD DC-DC Converters with Operational Amplifiers. Maxim Integrated Products, Inc., CA, 2004. [Online]. Available: http://www.maxim-ic.com/

[16] Abram P. Dancy, Rajeevan Amirtharajah, Anantha P. Chandrakasan, "High-Efficiency Multiple-Output DC-DC Conversion for Low-Voltage Systems," *IEEE Transition on VLSI Systems*, Vol. 8, No. 3, Page(s) 252-263, June, 2000.

[17] Dongsheng Ma, Wing-Hung Ki, Philip K. T. Mok, Chi-Ying Tsui, "Single-Inductor Multiple-Output Switching Converters with Bipolar Outputs," *IEEE International Symposium on Circuit and Systems*, Vol. 2, Page(s) 301-304, May, 2001.

[18] Dongsheng Ma, Wing-Hung Ki, Chi-Ying Tsui, and Philip K. T. Mok, "A single-inductor dual-output integrated DC/DC boost converter for variable voltage scheduling," *Asia and South Pacific Design Automation Conference,* Page(s) 19-20, Feb., 2001.

[19] Dongsheng Ma, Wing-Hung Ki, Chi-Ying Tsui, Philip K. T. Mok, "A 1.8V Single-Inductor Dual-Output Switching Converter for Power Reduction Techniques," *Symposium on VLSI Circuits,* Page(s) 137-140, June, 2001.

[20] Hanh-Phuc Le, Chang-Seok Chae, Kwang-Chan Lee, Gyu-Hyeong Cho, Se-Won Wang, Gyu-Ha Cho, and Sung-il Kim, "A Single-Inductor Switching DC-DC Converter with 5 Outputs and Ordered Power-Distributive Control," *IEEE International Symposium on Circuit and Systems*, Page(s) 534-620, Feb., 2007.

[21] Ming-Hsin Huang, Hong-Wei Huang, Jiun-Yan Peng, Tzung-Ling Tsai, Min-Chin Lee, Ching-Sung Wang, and Ke-Horng Chen, "Single-Inductor Dual-Output (SIDO) DC-DC Converters for Minimized Cross Regulation and High Efficiency in SoC Supplying Systems," *IEEE Midwest Symposium on Circuits and Systems,* Page(s) 550-553. Aug., 2007.

[22] Dongsheng Ma, Wing-Hung Ki, and Chi-Ying Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching," *IEEE International Solid-State Circuits Conference*, Vol. 1, Page(s) 390-476, Feb., 2002.

[23] Trevisan, D., Stefanutti, W., Mattavelli, P., and Tenti, P., "FPGA control of SIMO DC-DC converters using load current estimation," *Annual Conference of IEEE Industrial Electronics Society,* Page(s) 2243-2248, Nov., 2005.

[24] Young-Jin Woo, Hanh-Phuc Le, Gyu-Ha Cho, Gyu-Hyeong Cho, and Seong-Il Kim, "Load-Independent Control of Switching DC-DC Converters With Freewheeling Current Feedback," *IEEE Journal of Solid-State Circuits*, Vol. 43, Issue 12, Page(s) 2798-2808, Dec., 2008.

[25] Luis Benadero, Vanessa Moreno-Font, Abdelali El Aroudi, and Roberto Giral, "Single inductor multiple outputs interleaved converters operating in CCM," *Power Electronics and Motion Control Conference,* Page(s) 2115 2119, Sept., 2008.

[26] Patra, P., Samanta, S., Patra, A., and Chattopadhyay, S., "A Novel Control Technique for Single-Inductor Multiple-Output DC-DC Buck Converters," *IEEE International Conference on Industrial Technology*, Page(s) 807-811, Dec., 2006.

[27] Trevisan, D., Mattavelli, P., and Tenti, P., "Digital Control of Single-Inductor Multiple-Output Step-Down DC–DC Converters in CCM," *IEEE Transactions on Industrial Electronics*, Vol. 55, Issue 9, Page(s) 3476-3483, Sept., 2008.

[28] Sreekumar, C. and Agarwal, V., "On the hybrid automaton models and control synthesis of a single inductor, double output boost converter," *CES/IEEE International Power Electronics and Motion Control Conference*, Vol. 1, Page(s) 1-5, Aug., 2006.

[29] Kun-Yu Lin, Chun-Shih Huang, Dan Chen, Liu, K.H., "Modeling and design of feedback loops for a voltage-mode single-inductor dual-output buck converter," *IEEE Power Electronics Specialists Conference*, Page(s) 3389–3395, June, 2008.

[30] Weiwei Xu, Xiaoting Zhu, Zhiliang Hong, and Killat, Dirk, "Design of single-inductor dual-output switching converters with average current mode control," *IEEE Asia Pacific Conference on Circuits and Systems*, Page(s) 902–905, Nov., 2008.

[31] Dongsheng Ma and Wing-Hung Ki, "Fast-Transient PCCM Switching Converter With Freewheel Switching Control," *IEEE Transactions on Circuits and Systems II: Express Briefs*, Vol. 54, Issue 9, Page(s) 825–829, Sept., 2007.

[32] Sreekumar, C. and Agarwal, V., "Comparison of Mode Switched Controllers for a Pseudo Continuous Current Mode Boost Converter," *International Conference on Power Electronics, Drives and Energy Systems*, Page(s) 1–6, Dec., 2006.

[33] Shih-Min Chen, Chun-Yu Hsieh, and Ke-Horng Chen, "Challenge on compact size DC-DC buck converters with high-speed current sensor and on-chip inductors," *IEEE Midwest Symposium on Circuits and Systems*, Page(s) 670–673, Aug., 2007.

[34] Sreekumar, C. and Agarwal, V., "A Circuit Theoretical Approach to Hybrid Mode Switching Control of a Pseudo CCM Boost Converter," *IEEE International Conference on Industrial Technology*, Page(s) 791–795, Dec., 2006.

[35] Feng Su, Wing-Hung Ki, and Chi-Ying Tsui, "Ultra Fast Fixed-Frequency Hysteretic Buck Converter With Maximum Charging Current Control and Adaptive Delay Compensation for DVS Applications," *IEEE Journal of Solid-State Circuits*, Vol. 43, Issue 4, Page(s) 815–822, April, 2008.

[36] Kumar Singh, R., "A Novel Topology for Multiple Output DC-DC Converters for One Cycle Control," *International Conference on Power Electronics, Drives and Energy Systems*, Page(s) 1–7, Dec., 2006.

[37] Vazquez, N., Lopez, H., Hernandez, C., and Calleja, H., "Multiple-Output DC-to-DC based on the Flyback Converter," *IEEE International Power Electronics Congress*, Page(s) 105–108, Aug., 2008.

[38] Yuang-Shung Lee, Yuang-Shun Lin, Sung-Hsin Hsiao, and Yi-Pin Ko, "Multiple Output Zero-Current Switching Bi-directional Converter," *Annual Conference of the IEEE Industrial Electronics Society*, Page(s) 2058–2063, Nov., 2007.

[39] Chakraborty, S., Jain, A.K., and Mohan, N., "A novel converter topology for multiple individually regulated outputs," *IEEE Transactions on Power Electronics*, Vol. 21, Issue 2, Page(s) 361–369, Mar., 2006.

[40] Ramirez-Angulo, J., Lopez-Martin, A.J., Carvajal, R.G., Garimella, S.R.S., Garimella, L.M.K., and Garimella, A., "Compact multiple output linear V to I converters using split differential pairs and applications in allpass OTAs," *IEEE Electronics Letters*, Vol. 42, Issue 14, Page(s) 783–784, July, 2006.

[41] Chakraborty, S., Amit Kumar Jain, and Mohan, N., "A novel power distribution system using a central buck-based current source for multiple individually regulated outputs," *IEEE Power Electronics Specialist Conference*, Vol. 3, Page(s) 1379-1383, June, 2003.

[42] Higashi, T., Ninomiya, T., and Harada, K., "On the cross-regulation of multi-output resonant converters," *IEEE Power Electronics Specialists Conference*, Vol.1, Page(s) 18-25 April, 1988.

[43] Dongsheng Ma, "Automatic Substrate Switching Circuit for On-Chip Adaptive Power-Supply System," *IEEE Transactions On Circuits And Systems—II: Express Briefs*, Vol. 54, No. 7, Page(s) 641–645, July, 2007.

[44] Cheng-Chung Yang, Chen-Yu Wang, and Tai-Haur Kuo, "Current-Mode Converters with Adjustable-Slope Compensating Ramp," *IEEE Asia Pacific Conference on Circuits and Systems*, Page(s) 654–657, Dec., 2006.

[45] Xunwei Zhou, Donati, M., Amoroso, L., and Lee, F.C., "Improved light-load efficiency for synchronous rectifier voltage regulator module," *IEEE Transactions on Power Electronics*, Vol. 15, Issue 5, Page(s) 826–834, Sept., 2000.

[46] Mattavelli, P., "Digital control of DC-DC boost converters with inductor current estimation," *Nineteenth Annual IEEE Applied Power Electronics Conference and Exposition*, Vol. 1, Page(s) 74-80, 2004.

[47] Mengmeng Du and Hoi Lee, "A 2.5MHz, 97%-accuracy on-chip current sensor with dynamically-biased shunt feedback for current-mode switching DC-DC converters," *IEEE International Symposium on Circuits and Systems*, Page(s) 3274–3277, May, 2008.

[48] Lam, H.Y.H., Wing-Hung Ki, and Dongsheng Ma, "Loop gain analysis and development of high-speed high-accuracy current sensors for switching converters," *Proceedings of the 2004 International Symposium on Circuits and Systems*, Vol. 5, Page(s) 828-831, May, 2004.

[49] Du, Mengmeng and Lee, Hoi, "A Speed- and Accuracy-Enhanced On-Chip Current Sensor with Local Shunt Feedback for Current-Mode Switching DC-DC Converters," *6th IEEE Dallas Circuits and Systems Workshop on System-on-Chip*, Page(s) 1–4, Nov., 2007.

[50] Cheung Fai Lee and Mok, P.K.T., "A monolithic current-mode CMOS DC-DC converter with on-chip current-sensing technique," *IEEE Journal of Solid-State Circuits*, Vol. 39, Issue 1, Page(s) 3–14, Jan., 2004.

[51] Yat-Hei Lam, Suet-Chui Koon, Wing-Hung Ki, and Chi-Ying Tsui, "Integrated direct output current control switching converter using symmetrically-matched self-biased current sensors," *Asia and South Pacific Conference on Design Automation*, Page(s) 102-103, Jan., 2006.

[52] Yat-Hei Lam, Wing-Hung Ki, Chi-Ying Tsui, and Dongsheng Ma, "Integrated 0.9 V charge-control switching converter with self-biased current sensor," *IEEE Midwest Symposium on Circuits and Systems*, Vol.2, Page(s) 305-308, July, 2004.

Published Paper

◆ *International Journal Paper：*

● 2009

1. **(SCI) Ming-Hsin Huang** and Ke-Horng Chen, "Single-Inductor Multi-Output (SIMO) DC-DC Converters with High Light-Load Efficiency and Minimized Cross-Regulation for Portable Devices," *IEEE Journal of Solid-State Circuits*, Vol. 44, No. 4, Apr., 2009.
2. **(SCI) Ming-Hsin Huang**, Po-Chin Fan, and Ke-Horng Chen, "Low-Ripple and Dual-Phases Charge Pump Circuit Regulated by Switched-Capacitor Based Bandgap Reference," *IEEE Transactions on Power Electronics*, 2009, in press.

● 2008

3. **(SCI) Ming-Hsin Huang** and Ke-Horng Chen, "Single-Inductor Dual-Output (SIDO) DC-DC Converters for Minimized Cross Regulation and High Efficiency in Soc Supplying Systems," *Journal of Analog Integrated Circuits and Signal Processing*, July 2008.

◆ *International Conference Paper：*

● 2009

1. **Ming-Hsin Huang** and Ke-Horng Chen, "Single-Inductor Dual Buck-Boost Output (SIDBBO) Converter with Adaptive Current Control Mode (ACCM) and Adaptive Body Switch (ABS) for Compact Size and Long Battery Life in Portable Devices," *IEEE Symposium on VLSI Circuits*, 2009, in press.
2. Chun-Yu Hsieh, Chih-Yu Yang, **Ming-Hsin Huang**, Don-Hwan Li, Chi-Lin Chen, and Ke-Horng Chen, "A Charge-Reservoir with Buck-Store and Boost-Restore (BSBR) Technique for High Efficient Conversion and Low Cost Solution of RGB LED Display Panels," *Society for Information Display*, 2009, in press.

- **2008**

3. **Ming-Hsin Huang**, Ke-Horng Chen, Wei-Hsin Wei, "Single-inductor dual-output DC-DC converters with high light-load efficiency and minimized cross-regulation for portable devices," *IEEE Symposium on VLSI Circuits*, Page(s). 132 – 133, June 2008.

- **2007**

4. **Ming-Hsin Huang**, Hong-Wei Huang, Jiun-Yan Peng, Tzung-Ling Tsai, Min-Chin Lee, Ching-Sung Wang, and Ke-Horng Chen, "Single-Inductor Dual-Output (SIDO) DC-DC Converters for Minimized Cross Regulation and High Efficiency in SoC Supplying Systems," *IEEE International Midwest Symposium on Circuits & System,* Page(s). 550 – 553, Aug. 2007.

◆ ***National Journal Paper：***

5. **黃銘信**、陳科宏，"應用於可攜式裝置系統中的單電感雙輸出電源轉換器之最小互穩壓效應與最大輕載效率研製"，電子月刊，163 期，2009 年 2 月。

Vita

Ming-Hsin Huang was born and raised in Kaohsiung, Taiwan. He received the B.S. degree in the Electronic group of Department of Industrial Education and Technology, the M.S. degree in Department of Electrical Engineering at National Changhua University of Education, and the Ph.D. degree in the Department of Electrical and Control Engineering at National Chiao Tung University, Taiwan, in 2009. His research and specialty interests the power IC field such as compact-size DC-DC converters, charge-pumps, LED drivers, RGB-LEDs backlights, AD-DC switching power supplies and PWM ICs.