國立交通大學

資訊科學與工程研究所

碩士論文

應用於超高速傳輸正交多工分頻(VHT OFDM)系統頻率域上之時間同步器

Robust Frequency-Domain Timing Synchronizer in the Very-High-Throughput OFDM Systems

研 究 生：姜建安

指導教授：許騰尹　教授

中 華 民 國　九 十 九 年 九 月

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研 究 生：姜建安　　Student：Jian-An Jiang

指導教授：許騰尹　　Advisor：Terng-Yin Hsu

國 立 交 通 大 學

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摘要

本論文致力於研究在 128-FFT 下超高速傳輸正交多工分頻系統(OFDM)中，頻率域上的時間同步器，並以全數位多相位時脈管理元件(multiphase all-digital clock management)來調整取樣相位的方式補償取樣時脈誤差。

本論文所提出的演算法，利用收到封包的前端固定格式 preambles，與理想 preambles 之間的相關性對取樣誤差(sampling phase error)與取樣時脈偏移(sampling clock offset)作估計以及補償。殘餘的取樣時脈偏移再利用後端指標追蹤 (pilot tracking)作估計並補償使取樣誤差小於$\frac{\pi}{8}$。

本論文所提出的演算法，主要應用在 IEEE 所制定的無線網路標準 IEEE 802.11ad，所提出頻率域上的時間同步器在高斯雜訊及多路徑衰減的環境中，以封包錯誤率(PER)小於 1%為標準，效能在訊號雜訊比(SNR)失去 1.4dB 下可以達到容忍-300~400 ppm 的時脈偏移影響。

Abstract

This thesis details on the design of frequency-domain synchronizer to perform coherent sampling for 128-FFT Orthogonal Frequency Division Multiplexing (OFDM) timing recovery.

The proposed algorithm focus on timing synchronization include timing acquisition, sampling clock offset (SCO) estimation and pilot tracking scheme for residual SCO. The multiphase all-digital clock management (ADCM) is utilized to adjust sampling phases estimated by timing synchronization, rather than phase-locked or delay-locked loops, and utilize the cross-correlation power between short preambles to estimation the sampling phase error and the SCO. The pilot tracking scheme tracking the gradual phase shifts caused by residual SCO and maintaining the sampling phase error $< \frac{\pi}{8}$.

The simulation platform is 802.11ad with TGad channel. Performances are measured under the TGad channel. At 1% PER and SCO tolerance range is -300~400-ppm, the SNR loss is only 0.8~1.4 dB in frequency-selective fading. From simulation results, the frequency-domain synchronizer has wide clock offset tolerance.

致謝

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Chapter 1

Introduction

1.1 Introduction

Due to the explosive growth demand for wireless communications, the next-generation wireless communication systems are expected to provide ubiquitous, high-quality, high-speed, reliable, and spectrally-efficient. However, to achieve this objective, several technical challenges have to be overcome attempt to provide high-quality service in this dynamic environment [1].

Orthogonal frequency division multiplexing (OFDM), one of the multi-carrier modulation schemes, has become the favorite modulation technology for wireless communication because of its high spectral efficiency and simplicity in equalization. However, OFDM also has its drawbacks. The notable issues of OFDM system are more sensitive to synchronization errors than single carrier system [2], [3]. Therefore, synchronization is a major task in OFDM receiver. The duties of the synchronization include packet detection, frame synchronization, timing synchronization, and frequency synchronization.

The proposed algorithm focuses on timing synchronization. The frequency domain (FD) synchronizer contains three parts: sampling phase acquisition, SCO estimation, and pilot tracking scheme for residual SCO. The sampling phase of analog to digital converter (ADC) expect to sample at the ideal sampling position

where it has the maximum signal power. However, SCO and sampling phase offset causes analog to digital converter is not sampled at the optimum point. Therefore, the FD synchronizer estimate and compensate the majority of SCO in FD coarse SCO tracking. The FD timing acquisition determines the initial phase offset between the transmitter and the receiver. The residual SCO results in a slowly gradual phase shifts that are proportional with time. Then, the pilot tracking scheme track the gradual phase shifts and maintain the sampling phase.

The SCO compensation in this thesis is utilizing the 2^n-multiphase all-digital clock management (ADCM) to control A/D, rather than all-digital phase-locked loop (ADPLL) [9-12]. Because the large number of multiphase of ADPLL is hard to implement over several hundred MHz. a 2^n-multiphase all-digital clock management (ADCM) [15] have been adopted, which is easy to produce multiphase over GHz using an in-house digital cell library. The proposed algorithm is base on the architecture and the preamble structure of IEEE 802.11ad standard

The rest of this paper is organized as follows. In Chapter 2, a brief introduction states the system description and system model. Chapter 3 describes the proposed frequency-domain timing synchronizer include sampling phase acquisition, SCO estimation, and pilot tracking scheme. Chapter 4 shows and discusses the simulation results. Conclusions are finally drawn in Chapter 5.

1.2 Contribution

This work investigate the synchronizer in frequency-domain include timing acquisition, SCO estimation and pilot tracking scheme. The proposed SCO estimation determine the majority of SCO which up to 400~-300-ppm, and the pilot tracking scheme maintain the sampling phase error less than $\frac{\pi}{8}$.

Chapter 2

System Platform

In this chapter, the basic of OFDM is introduced. Three main blocks of wireless communication: transmitter, receiver, and channel model are described as follows.

2.1 The Basic of OFDM

OFDM is a multi-carrier modulation that achieves high data rate and combat multipath fading in wireless networks. The main concept of OFDM is to divide available channel into several orthogonal sub-channels. All of the sub-channels are transmitted simultaneously, thus achieve a high spectral efficiency. Furthermore, sub-carriers have orthogonal property and carried individual data. Their spectrum overlaps are zero. It is easy to use FFT and IFFT to implementation OFDM. However, OFDM has its drawbacks. The significant one is sensitivity to synchronization errors. The synchronization errors come from two sources. One is the local oscillator frequency difference between transmitter and receiver, and the other is the Doppler spread due to the relative motion between the transmitter and the receiver [4]. In addition, timing synchronization may affect the performance of channel estimation [5].

2.2 IEEE 802.11ad Physical Layer Specification

2.2.1 Transmitter and Receiver

The IEEE 802.11ad provides features that can support a throughput of 1Gb/s and greater. Figure 2-1 shows transmitter data path. First use FEC encoder to encodes the source data. FEC encoder supports 1/2、5/8、3/4、13/16 four kind coding rates. The interleaver provides a form of diversity to guard against localized corruption or bursts of errors. And then, the QAM mapping is used to modulate the bit stream. It supports SQPSK, QPSK, 16 QAM, or 64 QAM. After QAM mapping, IFFT is used to transfer signal from frequency domain to time domain. In 2.538GHz, there are 128 frequency entries for each IFFT, or 128 sub-carriers in each OFDM symbol, 96 of them are data carriers, 4 of them are pilot carriers, other are null carriers. After Insert Guard Interval (GI), the signal is transmitted by RF.

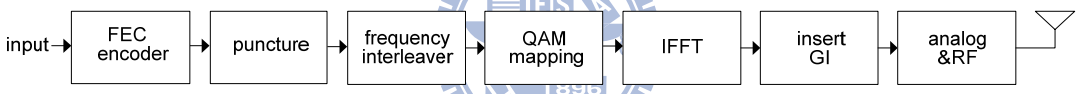
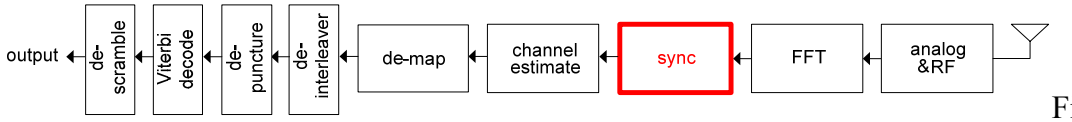


Figure 2-1: IEEE 802.11ad transmitter data path [6]

Fig Figure 2-2 shows receiver data path. The signal is received from the RF. Sync is used for synchronization, including to find when exactly the packet start, the OFDM symbol boundary and the best sample phase. After a packet is presented, FFT is used to transfer received signal from time domain to frequency domain. Channel effect will be estimated and compensated by Equalizer. IQ mismatch is also taken under consideration. After all estimation and compensation, then the bit streams are de-map, de-interleaver. Finally, it is decoded by FEC which includes de-puncturing, Viterbi decoder and de-scrambler.



Fig

Figure 2-2: IEEE 802.11ad receiver data path

2.2.2 Golay Complementary Sequence [6]

Complementary sequences which are made up of "a" and "b" parts have specific property that their out-of-phase aperiodic autocorrelation coefficients sum to zero. Each part has the length of L = 2E where E is a positive integer. The Golay complementary sequences (GCSs) $Ga_k(i)$ and $Gb_k(i)$ (i=0, 1, 2, … ,2^{k-1}) are generated using the following recursive procedure:

$$\begin{aligned} &Ga_0(i) = \delta(i) \\ &Gb_0(i) = \delta(i) \\ &Ga_k(i) = Ga_{k-1}(i) + Gb_{k-1}(i - 2^{k-1}) \\ &Gb_k(i) = Ga_{k-1}(i) - Gb_{k-1}(i - 2^{k-1}) \end{aligned} \qquad (2.1)$$

Where $\delta(i)$ is the Kronecker delta function.

The Short Training Field (STF) is constructed based on the $Ga_{128}(n)$ in the 802.11ad system, as shown in Eq. 2.1, and the Ga_{128} used in this platform as shown as Eq. 2.2.

$$Ga_{128} = \begin{bmatrix} 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 & -1 & 1 \\ 1 & -1 & -1 & 1 & -1 & 1 & -1 & 1 & -1 & -1 & -1 & -1 & 1 & 1 & -1 & -1 \\ 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 & -1 & 1 \\ -1 & 1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & 1 & 1 & 1 & -1 & -1 & 1 & 1 \\ -1 & -1 & 1 & 1 & 1 & 1 & 1 & 1 & 1 & -1 & 1 & -1 & -1 & 1 & 1 & -1 \\ -1 & 1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & 1 & 1 & 1 & -1 & -1 & 1 & 1 \\ 1 & 1 & -1 & -1 & -1 & -1 & -1 & -1 & -1 & 1 & -1 & 1 & 1 & -1 & -1 & 1 \\ -1 & 1 & 1 & -1 & 1 & -1 & 1 & -1 & 1 & 1 & 1 & 1 & -1 & -1 & 1 & 1 \end{bmatrix} \qquad (2.2)$$

2.2.3 Basic PPDU Format

A PHY protocol data unit (PPDU) is defined to provide interoperability. Figure 2-3 shows the PPDU format for the basic OFDM mode. The OFDM frame is composed of the Short Training Field (STF), the channel estimation field (CEF), the Header, OFDM symbols and optional training fields, as shown in Figure 2-2. The

STF is used for packet detection, AGC, frequency offset estimation, synchronization, indication of frame type and channel estimation.

The Golay sequences are used in the STF and CEF: $Ga_{128}(n)$, $Gb_{128}(n)$. These are a pair of complementary sequences. The subscript denotes the length of the sequences.

The STF is composed of 14 repetitions of sequences $Ga_{128}(n)$ of 128 samples each, followed by a single repetition of $-Ga_{128}(n)$. These samples have correlation properties. In this thesis, correlation techniques will be applicable for packet detection, symbol boundary detection, and timing synchronization. A detail data structure of L-STF is shown as Figure 2-3.

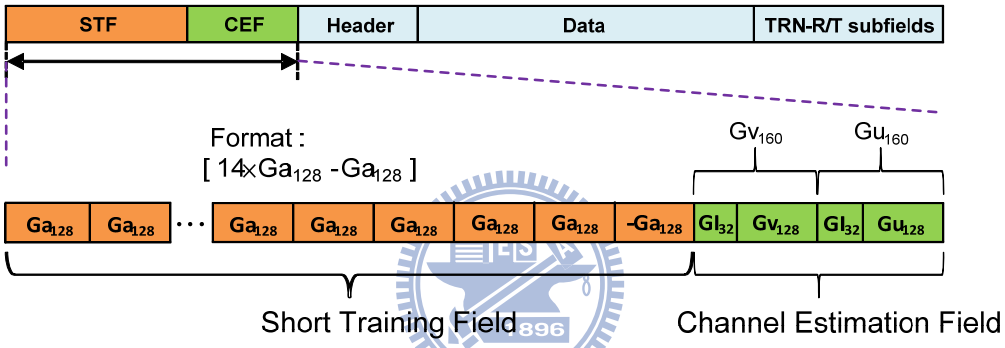


Figure 2-3: PPDU Format [6]

2.2.4 Pilot Sequence

The ideal pilots $X_{n,k}$ in our platform are inserted at tones 27, 54, 78, 105. The value of the pilots at these tones is $\left[\sqrt{1+j}, \sqrt{1-j}, \sqrt{1-j}, \sqrt{1+j}\right]$ respectively. At symbol n the pilot sequence is multiplied by the value $2\times p_n$-1, where p_n is the value generated by the polynomial $S(x) = x^{15} + x^{14} + 1$, and the sequence $x_1, x_2, \ldots x_{15}$ are set to [0, 0, 0, 0, 1, 0, 1, 0, 0, 0, 0, 1, 0, 1, 1] at the first symbol. [6]

2.3 Channel Model

There are many imperfect effects during transmitted signals through channel, such as Additive White Gaussian Noise (AWGN), carrier frequency offset (CFO), multipath, and so on. The block diagram of channel model is shown in Figure 2-4.

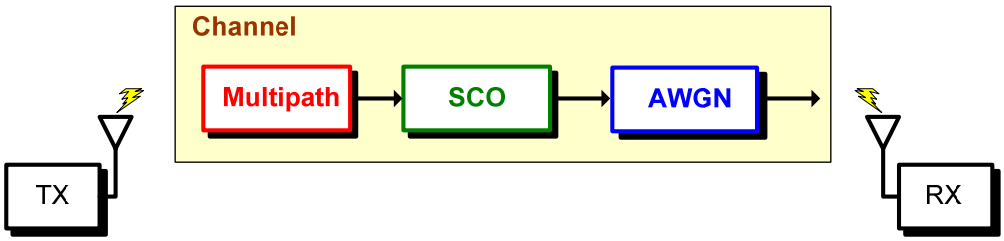


Figure 2-4: Block diagram of channel model

2.3.1 Additive White Gaussian Noise

Wideband Gaussian noise comes from many natural sources, such as the thermal vibrations of atoms in antennas, "black body" radiation from the earth and other warm objects, and from celestial sources such as the sun. The AWGN channel is a good model for many satellite and deep space communication links. On the other hand, it is not a good model for most terrestrial links because of multipath, terrain blocking, interference, etc. The signal distorted by AWGN can be derived as

$$r(t) = s(t) + n(t) \qquad (2.3)$$

Where $r(t)$ is received signal,

$s(t)$ is transmitted signal,

$n(t)$ is AWGN.

2.3.2 Multipath

Because there are obstacles and reflectors in the wireless propagation channel, the transmitted signal arrivals at the receiver from various directions over a

multiplicity of paths. Such a phenomenon is called multipath. It is an unpredictable set of reflections and/or direct waves each with its own degree of attenuation and delay. Multipath is usually described by two sorts:

A. Line-of-sight (LOS): the direct connection between transmitter and receiver.

B. Non-line-of-sight (NLOS): the path arriving after reflection from reflectors.

Multipath will cause amplitude and phase fluctuations, and time delay in the received signals. When the waves of multipath signals are out of phase, reduction of the signal strength at the receiver can occur. One such type of reduction is called the multipath fading; the phenomenon is known as “Rayleigh fading” or “fast fading.” Besides, multiple reflections of the transmitted signal may arrive at the receiver at different times; this can result in inter symbol interference (ISI) that the receiver cannot sort out. This time dispersion of the channel is called multipath delay spread which is an important parameter to access the performance capabilities of wireless systems. For a reliable communication without using adaptive equalization or other anti-multipath techniques, the transmitted data rate should be much smaller than the inverse of the RMS delay spread. A representation of Rayleigh fading and a measured received power-delay profile are shown in Figure 2-5.

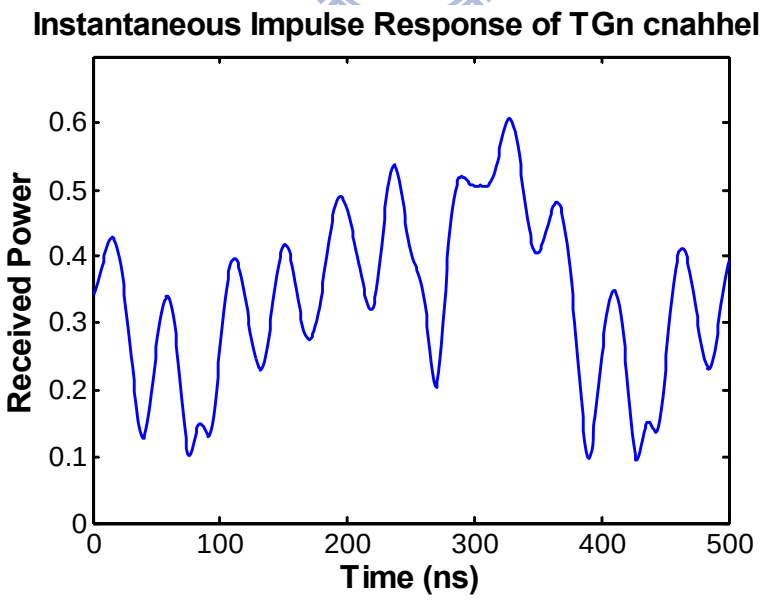


Figure 2-5: Instantaneous impulse responses

2.3.3 System Clock Offset

The clock drift means the different between the sampling frequency of the digital to analog converter (DAC) and the analog to digital converter (ADC). Because of sampling frequency offset, even if the initial sampling point is optimized, the following sampling points will still slowly shift with time. This model is using compress sinc waveform to cause the clock drift effect, and its effect can be written as

$$R(nT_s) = R_{preADC}(nT_s) * \sin c(\frac{nT_s - \Delta T_n}{T_s}) \qquad (2.4)$$

where R_{preADC} represents the ADC original output signal, ΔT_s represents shift sampling period and to get $R(nT_s)$ signal by convoluting the ADC original output signal and shifted sinc waveform. 錯誤! 找不到參照來源。6 shows the clock drift model effect. Initial can samples at optimum sampling points, then slightly incorrect sampling instants will cause the SNR degradation.

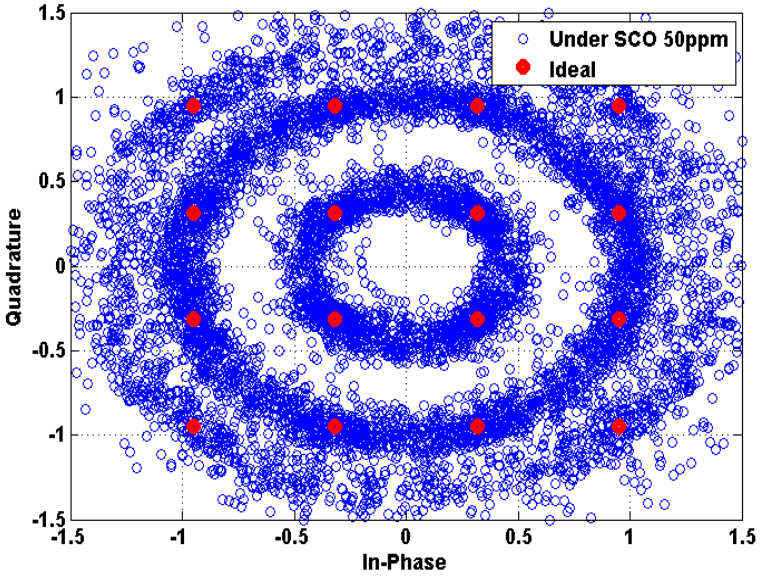


Figure 2-6: The SCO effect of 16-QAM modulation under SCO 50 ppm

Chapter 3

Timing Synchronization

3.1 Introduction

Timing synchronization plays an important role in the receiver design of OFDM. The ADC is the first stage of baseband, so it dominates the receiving signal to noise ratio (SNR). To get the highest input SNR, the ADC is hoped to sample at the eye open position where it has the maximum signal power. However, there are symbol timing offset, sampling phase shift, sampling clock offset (SCO), and carrier frequency offset (CFO), that constitutes timing synchronization errors, so timing synchronization is necessary. The duties of the synchronization include packet detection, frame synchronization, timing synchronization, and frequency synchronization. The synchronization flow is shown in Figure 3-1. In this thesis, we will focus on timing synchronization. The FD synchronizer contains three parts: Coarse SCO tracking, sampling phase acquisition, and pilot tracking for residual SCO.

Figure 3-1: The frequency domain timing synchronization flow

3.2 Coarse Sampling Clock Offset Tracking

3.2.1 Introduction

After RF down conversion and with SCO (δ) effect, all preambles and received datum ($R_{\phi,k}$) are sampled by using a fixed clock phase (Φ) which may be not the ideal sampling phase, where k is the received datum index, as shown in Figure 3-2.

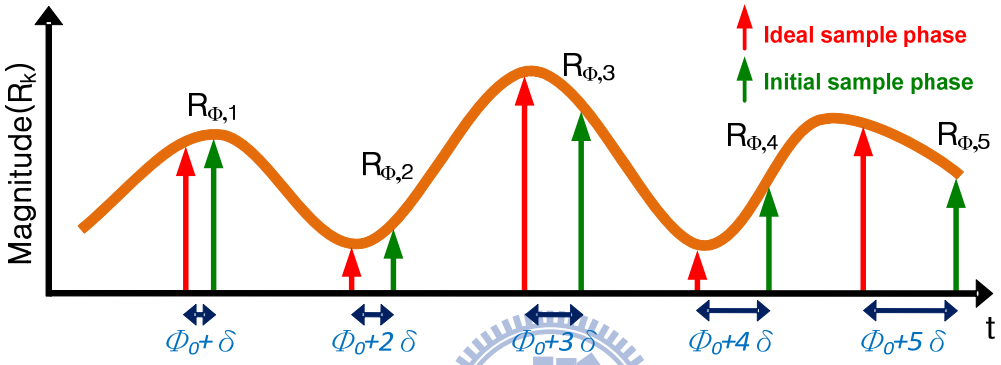


Figure 3-2: Received signals with phase error Φ

The phase error of received datum r[n] contains an initial constant phase offset (Φ_0) between the transmitter and the receiver and the phase shift has constant increment proportional to subcarrier index (k) and SCO (δ) as the symbol index (n) increases.

$$r[n] = r(nT_r) = r(n \cdot (1+\delta)T_t) = r(\mathrm{n}T_t + n\delta T_t) \qquad (3.1)$$

where T_t and T_r are the transmitter and receiver sampling period, and $n\delta T_t$ is the sampling timing offset at the n^{th} symbol signals.

In frequency domain, the received datum with the effect due to the sampling clock offset as shown in Eq. 3.2.

$$R[n;k] = \mathrm{X}_{\mathrm{n,k}}\mathrm{H}_{\mathrm{n,k}}\, e^{j2\pi nk\delta\frac{T_s}{T_u}} + \mathrm{W}_{\mathrm{n,k}} \qquad (3.2)$$

In the following chapter described two steps to find the SCO. The first step, the parallel cross-correlation is utilized to detect the symbol boundary of the received signal. The second step, the cross-correlation power of two STFs is utilized to

determine the SCO.

3.2.2 Parallel Cross-correlation

To consider the first position of the received STF, the parallel cross-correlation [13] is utilized to search for the locations of the STF which is corresponded to with the input signal, as shown in Figure 3-3.

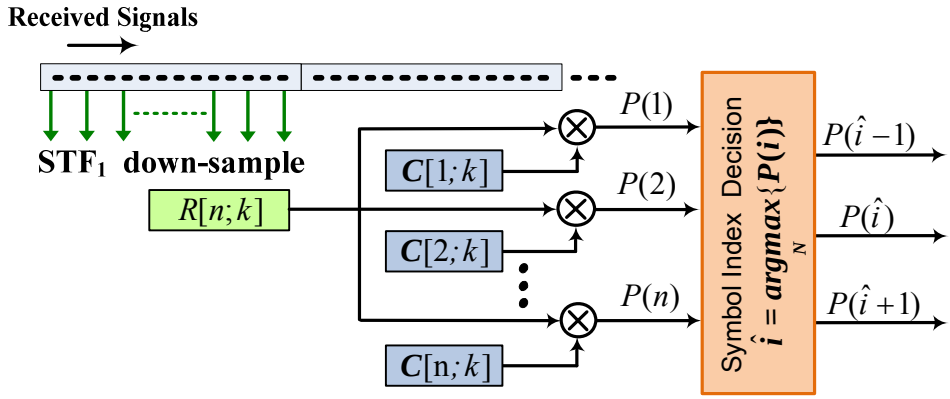


Figure 3-3: The symbol boundary detection architecture

If the c = {c(0), c(1),…, c(N-1)} is Short Training Field (STF) with N samples. To calculate the parallel cross-correlation of the received signal ($R[n;k]$) and the known STF buffer ($c[i;k]$) to be reference, the boundary correlation buffer (BCB) is designed by the ideal STF with cyclic shift like the Eq. 3.3.

$$c[i,k]=\begin{bmatrix} c_1(k) \\ c_2(k) \\ c_3(k) \\ \vdots \\ c_{i-2}(k) \\ c_{i-1}(k) \\ c_i(k) \end{bmatrix}=\begin{bmatrix} \text{STF(1)} & \text{STF(2)} & \text{STF(3)}\cdots & \cdots & \cdots & \text{STF(N-2)} & \text{STF(N-1)} & \text{STF(N)} \\ \text{STF(N)} & \text{STF(1)} & \text{STF(2)}\cdots & \cdots & \cdots & \text{STF(N-3)} & \text{STF(N-2)} & \text{STF(N-1)} \\ \text{STF(N-1)} & \text{STF(N)} & \text{STF(1)}\cdots & \cdots & \cdots & \text{STF(N-4)} & \text{STF(N-3)} & \text{STF(N-2)} \\ \vdots & \vdots & \vdots & \ddots & & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & & \ddots & \vdots & \vdots & \vdots \\ \vdots & \vdots & \vdots & & & \ddots & \vdots & \vdots \\ \text{STF(4)} & \text{STF(5)} & \text{STF(6)}\cdots & \cdots & \cdots & \text{STF(N+1)} & \text{STF(N+2)} & \text{STF(N+3)} \\ \text{STF(3)} & \text{STF(4)} & \text{STF(5)}\cdots & \cdots & \cdots & \text{STF(N)} & \text{STF(N+1)} & \text{STF(N+2)} \\ \text{STF(2)} & \text{STF(3)} & \text{STF(4)}\cdots & \cdots & \cdots & \text{STF(N-1)} & \text{STF(N)} & \text{STF(N+1)} \end{bmatrix} \quad (3.3)$$

$$C[i;k]=\sum_{n=0}^{N-1} c[i;k]\,e^{-j2\pi\frac{nk}{N}} \quad (3.4)$$

From Eq. 3.4, the FFT is utilized to get the BCB ($c[i;n]$) in frequency domain.

The frequency domain parallel cross-correlation power ($P(i)$) can be obtained by

$$P(i) = \left| \sum_{k=0}^{N-1} R[n;k] * C[i;k] \right| \qquad (3.5)$$

Due to the received signals are the most likely to the ideal STF with cyclic shift ($\hat{i}$) which the cross-correlation power ($P(\hat{i})$) is the maximum. Then, the first position of the received signals is determined as shown in Eq. 3.6.

$$\hat{i} = \arg\max_{N} \{P(i)\} \qquad (3.6)$$

Where the ideal STF with cyclic shift ($C[\hat{i};k]$) is the most likely to the received datum.

3.2.3 Coarse Sampling Clock Offset Tracking

The received signals are sampled by ideal sampling phase which the cross-correlation power is the maximum. However, the SCO results that the phase shifts (ϕ_n) has constant increment proportional to subcarrier index (k) and SCO (δ) as the symbol index (n) increase. From the relation between the cross-correlation power of the nth symbol ($P_n(\hat{i})$) and the phase error (ϕ_n), it is clear that SCO causes cross-correlation power attenuation and phase shift in the received signals.

Hence, the proposed algorithm utilizes the relation between the correlation power and the phase error to estimate the phase error caused by SCO. SCO is estimated according to the phase differences between two adjacent symbols. Figure 3-4 show the proposed coarse SCO tracking flow.

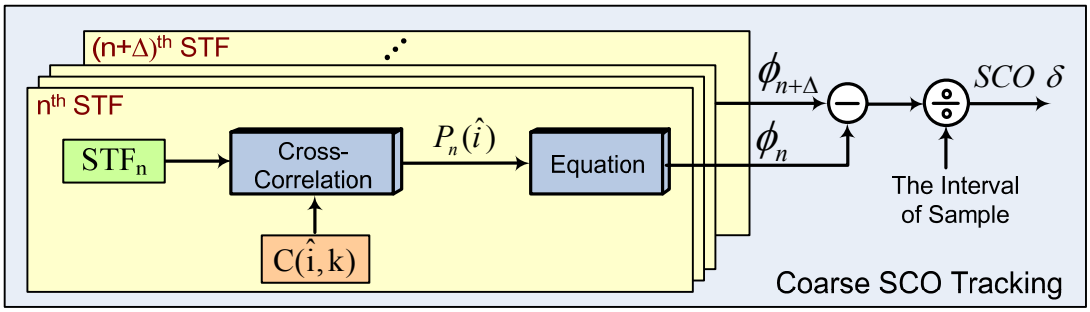


Figure 3-4: The flow of proposed sampling clock offset estimation

The algorithm includes 4 steps:

Step 1:

Utilize three ideal correlation powers to find an equation in two variables represented the relation between the cross-correlation power and the phase error. For enhance the similarity between the relation and the equation, we find four equations from ideal correlation powers, and average the coefficient of four equations,

$$P(\hat{i}) = a\phi^2 + b\phi + c \qquad (3.7)$$

Where n is the received symbol index; $\hat{i}$ is the cyclic shift of ideal STF.

Step 2:

Estimate the cross-correlation powers ($P_n(\hat{i})$) with the n^{th} symbol and the $(n+\Delta)^{th}$ symbol as shown in Eq. 3.8, where Δ is the interval of symbol index.

$$P_n(\hat{i}) = \left| \sum_{k=0}^{N-1} R[n;k] * C[\hat{i};k] \right| \qquad (3.8)$$

Step 3:

Determine the phase error (ϕ_n) by substituting the correlation power into equation.

$$\phi_n = \frac{-b \pm \sqrt{b^2 - 4a(c - P_n(\hat{i}))}}{2a} \qquad (3.9)$$

Step 4:

Estimate the SCO (δ) by utilizing the phase differences between two adjacent symbols divide the sampling interval, where T_s is the period of one symbol.

$$\delta = \frac{\phi_{n+\Delta} - \phi_n}{\Delta * T_s} \qquad (3.10)$$

3.3 Sampling Phase Acquisition

3.3.1 Frequency Domain Timing Acquisition

This section introduces 1x sampling rate timing synchronization scheme [12]. After the parallel cross-correlation and the coarse SCO tracking, the symbol boundary is known, and the majority of SCO is compensated. However, the following signals are sampled by using a fixed clock phase which may be not the ideal sampling phase. The received datum with initial phase error (Φ_0) can be obtained by Eq. 3.11.

$$r(n;\Phi_0) = x(t)\delta(t-(n+\Phi_0)T_s) \text{ and } \Phi_0 \in \boldsymbol{R},\ |\Phi_0| \leq 0.5 \qquad (3.11)$$

Where x(t) is the received signals before RF down conversion; δ(t) is the delta function; Φ_0 is the sampling error; k is the subcarrier index. Then, the FFT is utilized to get the received signal in frequency domain.

$$R(k;\Phi_0) = \sum_{n=0}^{N-1} r(n;\Phi_0)\, e^{-j2\pi\frac{nk}{N}} \qquad (3.12)$$

The Eq. 3.6 considers the cross-correlation power $P(\hat{i})$ is the maximum with the phase error. Due to the received signals which have the maximal cross-correlation power are sampled at the optimal phase.

The cross-correlation powers are utilized as timing detection (TD). The TD can be obtained by Eq.3.13.

$$\begin{aligned} TD(\hat{i},\phi_0) &= \left|\sum_{k=0}^{N-1} R[k;\phi_0] * C[\hat{i};k]\right| \\ TD(\hat{i}-1,\phi_0) &= \left|\sum_{k=0}^{N-1} R[k;\phi_0] * C[\hat{i}-1;k]\right| \\ TD(\hat{i}+1,\phi_0) &= \left|\sum_{k=0}^{N-1} R[k;\phi_0] * C[\hat{i}+1;k]\right| \end{aligned} \qquad (3.13)$$

Where $C[\hat{i};k]$ is the ideal STF with cyclic shift ($\hat{i}$) in frequency domain.

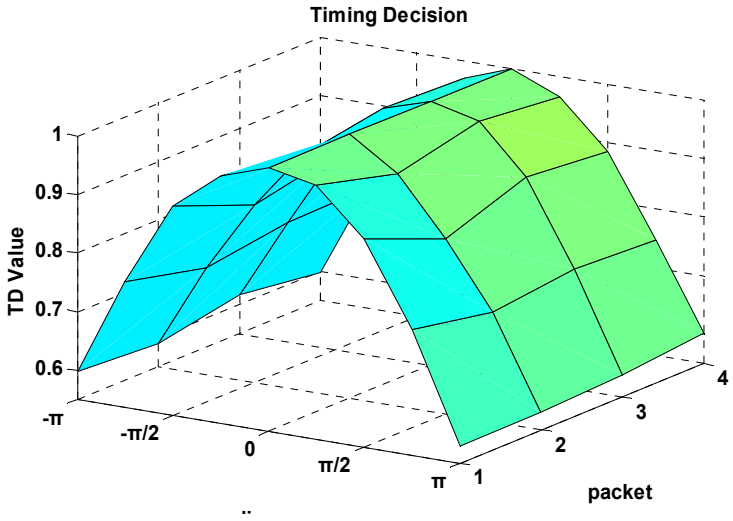


Figure 3-5: The proposed timing detection

The ADCM is utilized to control A/D to sample at different phase, as shown in Figure 3-6. The first STF is sampled at the initial phase $[\phi_0]^{th}$. Then, the phase controller adjusts the sampling clock with +π-phase changes by ADCM. After that the second STF is sampled at the phase $[\phi_0 + \pi]^{th}$.

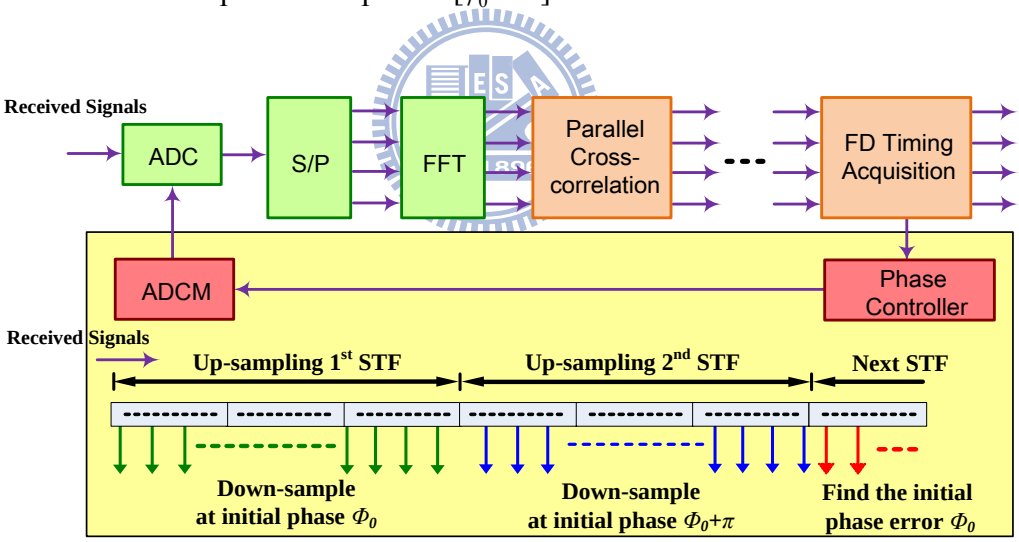


Figure 3-6: The block diagram of frequency domain timing acquisition

The frequency domain timing acquisition determines the phase error (Φ_0) on the relation between the TD and the phase error. The one of STF $C[\hat{i}-1;k]$ and $C[\hat{i}+1;k]$ which is closed to the received signals $R(k;\phi_0)$ with phase error (Φ_0) have the larger cross-correlation power than the other. When the phase error $\phi_0 \in [0 \sim \pi]$ means the STF $C[\hat{i}+1;k]$ is more closed to $R(k;\phi_0)$ than the STF

$C[\hat{i}+1;k]$. Then, $TD(\hat{i}+1,\phi_0)$ is much larger than $TD(\hat{i}-1,\phi_0)$. Similarly, when the phase error $\phi_0 \in [-\pi \sim 0]$ means $TD(\hat{i}-1,\phi_0)$ is much larger than $TD(\hat{i}+1,\phi_0)$. Define two conditions such as Eq. 3.14.

$$\Delta TD_1 = \left| TD(\hat{i},\phi_0) - TD(\hat{i}+1,\phi_0) \right|$$

$$\Delta TD_2 = \left| TD(\hat{i},\phi_0+\pi) - TD(\hat{i}+1,\phi_0+\pi) \right| \qquad (3.14)$$

When $\phi_0 \in [0 \sim \pi]$, the smaller phase error Φ_0, the larger ΔTD_1 we estimate. Therefore, the ratio of the relationship of ΔTD_1 and $TD(ideal)$ is utilized to determine the phase shift as shown as Eq. 3.15.

$$phase\_shift = \frac{TD(ideal) - \Delta TD_1}{TD(ideal)} \cdot \pi \qquad (3.15)$$

Where $TD(ideal)$ is the value ΔTD_1 in ideal sampling phase.

When $\phi_0 \in [-\pi \sim 0]$, the larger phase error Φ_0, the smaller ΔTD_2 we estimate. Therefore, the ratio of the relationship of ΔTD_2 and $TD(ideal)$ is utilized to determine the phase shift as shown as Eq. 3.16.

$$phase\_shift = \frac{\Delta TD_2}{TD(ideal)} \cdot -\pi \qquad (3.16)$$

3.4 Pilot Tracking

3.4.1 Introduction

Although the SCO in the received signals has been estimated and compensated using STF, still some residual SCO may exist. Residual SCO results in a slowly gradual phase shifts that are proportional to subcarrier indices. When the receiver operates for a long duration, the phase shifts still cause the sampling error and ICI, because the subcarriers are not orthogonal. The residual SCO estimation is inevitable in the OFDM systems.

The conventional SCO estimation methods [14] utilize the information of phase

differences between two pilots in two adjacent symbols to estimate the SCO. However, the accuracy of SCO estimation using pilots is base on the CFR and the SNR. Therefore, the following method is tracking the gradual phase shifts Φ and maintaining the sampling phase by utilizing the ADCM to control A/D in low SNR rather than estimating the SCO accurately.

3.4.2 Pilot Tracking

The normalized sampling error is defined as Eq. 3.17 where T_r and T_t are the transmitter and receiver sampling period respectively. From Eq. 3.2, the effect of received datum caused by residual SCO is obtained by Eq. 3.18.

$$\delta = \frac{T_r - T_t}{T_t} \tag{3.17}$$

$$R_{n,k} = X_{n,k} H_k e^{j2\pi k\delta' \frac{nT_s}{T_u}} + W_{n,k} \tag{3.18}$$

Where n is the symbol index, and k is the subcarrier index, δ' is the residual SCO, T_s is the total symbol duration, and T_u is the useful data portion and H_k is the channel frequency response.

The proposed scheme is estimate the phase error by tracking the phase differences $\theta_{n,k}$ between the received pilots and the ideal pilot $X_{n,k}$ with the same subcarrier index, the architecture as shown as Figure 3-7.

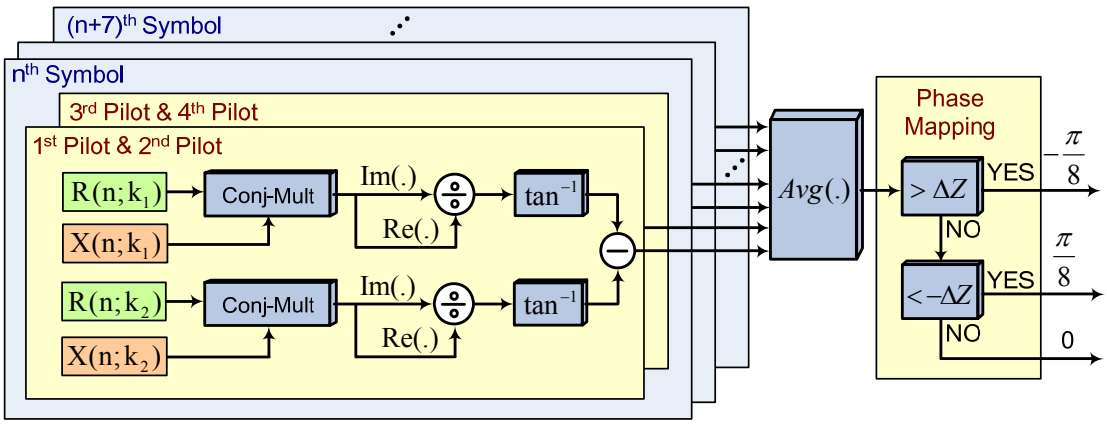


Figure 3-7: The architecture of pilot tracking scheme

$$\begin{aligned}\theta_{n,k} &= \angle(X_{n,k}R_{n,k}^{*}) \\ &= \angle(X_{n,k}(H_k X_{n,k} e^{j2\pi k\delta\frac{nT_s}{T_u}})^{*}) \\ &= 2\pi k\delta\frac{nT_s}{T_u}\end{aligned} \tag{3.19}$$

To estimate the phase differences $\Delta\theta_{n,\Delta k}$ between the pilots in the same symbol, as shown as Eq. 3.19. For decrease the effect of noise, the pilot tracking scheme averages the phase differences $\Delta\theta_{n,\Delta k}$ each eight symbols.

$$\Delta\theta_{n,\Delta k} = \theta_{n,k_1} - \theta_{n,k_2} = 2\pi\Delta k\delta\frac{nT_s}{T_u} \tag{3.20}$$

Where k_1 and k_2 are the index of the signals at the pilot tones.

After pilot tracking scheme, the sampling phase of ADC is expected that the sampling phase error is less than $\frac{\pi}{8}$. Due to the sampling phase error (ϕ_n) is $2\pi\delta nT_s$ at the n[th] symbol. Then, substitute condition into the Eq. 3.21.

$$\Delta\theta_{n,\Delta k} = 2\pi\Delta k\delta\frac{nT_s}{T_u} < \left|\frac{\pi}{8}\cdot\frac{\Delta k}{T_u}\right| \tag{3.21}$$

As a result, the pilot tracking scheme estimates the phase differences $\Delta\theta_{n,\Delta k}$ continually. When the phase differences $\Delta\theta_{n,\Delta k} \geq \frac{\pi}{8}\cdot\frac{\Delta k}{T_u}$, the ADCM is utilized to adjust the A/D sampling phase $-\frac{\pi}{8}$ changes in following received signals. Similarly, when the phase differences $\Delta\theta_{n,\Delta k} \leq -\frac{\pi}{8}\cdot\frac{\Delta k}{T_u}$, the ADCM is utilized to adjust the A/D sampling phase $+\frac{\pi}{8}$ changes in following received signals. Therefore, the pilot tracking scheme maintains that the sampling phase error of ADC is less than $\frac{\pi}{8}$.

3.5 Compensation

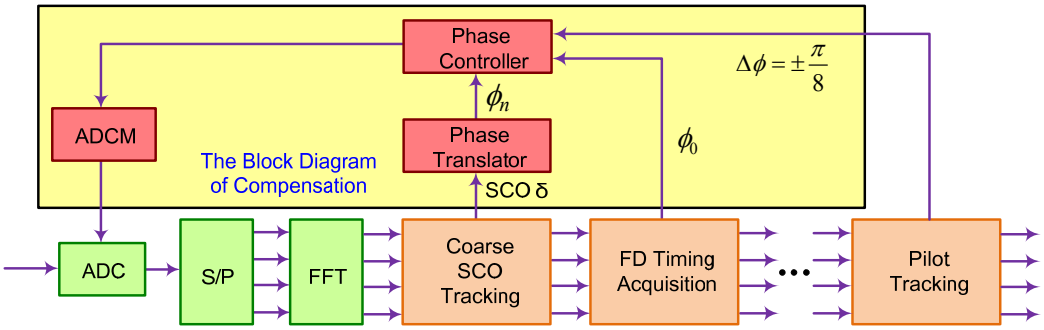


Figure 3-8: The block diagram of compensation

There are various schemes to compensate SCO, such as utilizing the interpolation techniques to resample in discrete-time domain, or rotating the FFT outputs in frequency domain, or utilizing ADPLL, ADDLL to recover ADC sampling. In the proposed algorithm, we compensate sampling phase offset and SCO in time domain with the multiphase technique which are implemented by all-digital clock management (ADCM).

After sampling phase acquisition, the algorithm outputs estimation phase Φ_0 to phase control to adjust the A/D sampling phase. Then, SCO estimation algorithm outputs a value of normalized sampling clock offset, as shown as Eq. 3.16, so we need a phase translator to get the phase offset ϕ_n correspond with the value of SCO, as shown in Eq. 3.22, where n is the data index and M is the number of multiphase.

$$\begin{aligned} nT_r - \phi_n &= nT_t \\ \phi_n &= nT_r - nT_t = n \cdot \delta \cdot T_t = n \cdot \delta \cdot M \end{aligned} \qquad (3.22)$$

In the aspect of pilot tracking, pilot tracking will output phase $\pm\frac{\pi}{8}$ to phase control according to the relation between phase differences and Eq. 3.21. Finally, phase control combines the three phase shift to ADCM.

Chapter 4

Simulation Result

We use simulation to evaluate the receiver's performance with the AWGN, multipath fading and sampling clock offset.

4.1 Simulation Platform

MATLAB is chosen as simulation language, due to its ability to mathematics, such as matrix operation, numerous math functions, and easily drawing figures. The major parameters are shown in TABLE IV.

Table 4-1 Simulation parameters

Parameter	Value
MCS Set	20
Antenna No.	1
Modulation	16 QAM
Coding Rate	3/4
PSDU Length	2048 Bytes
Carrier Frequency	60 GHz
Bandwidth	2.64 GHz
IFFT / FFT Period	48.48 *ns* (128-FFT)

Table 4-2: Simulation parameters

4.2 Simulation Result

As mention before, the multiphase generator is used to generate 16 phases between one clock cycles. In other word, the phase error 16 means that signal is delay one cycle, and the phase error 0 means that sign is at ideal phase. With different initial phase error and SNR=5, after timing synchronizer, the final phase errors are convergence into 2 phases, as shown in Figure 4.1.

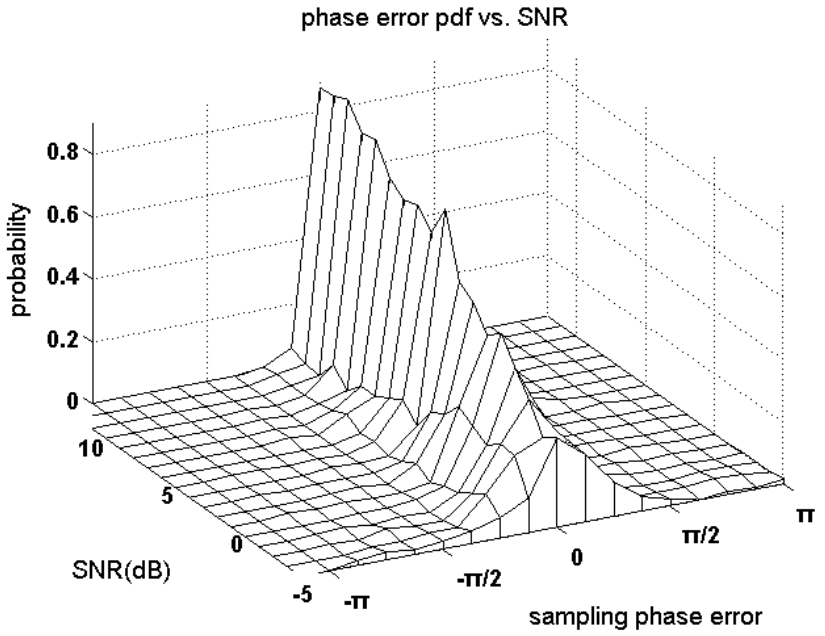


Figure 4.1: PDF of sampling phase error

Figure 4.2 shows the root mean square error of sampling phase. No synchronization means without timing acquisition to fix the unknown phase error. Those initial phase is random to generate and its RMS is about 4.5~4.8 (phase), one phase offset means the phase difference with $\frac{\pi}{8}$ in this simulation. The value of RMS is decreasing with the increasing of SNR and converges to 1.3 phases after timing acquisition with 400 ppm SCO.

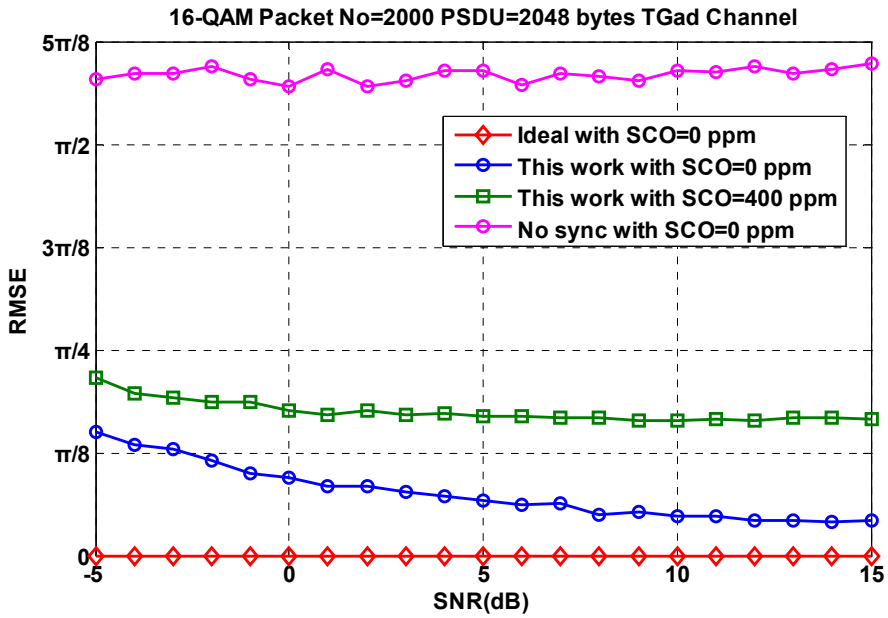


Figure 4.2: The root mean square error of sampling phase

The ideal synchronization at 1% PER, SNR is about 12.7-dB under the TGad channel. So we determine the residual SCO after SCO estimation when SNR = 12.7-dB. Figure 4.3 shows the root mean square error SCO estimation and compensation. From the simulation result, SCO estimate error are about 17-ppm of SCO = 0-ppm and 19-ppm of SCO = 400-ppm after the SCO estimation.

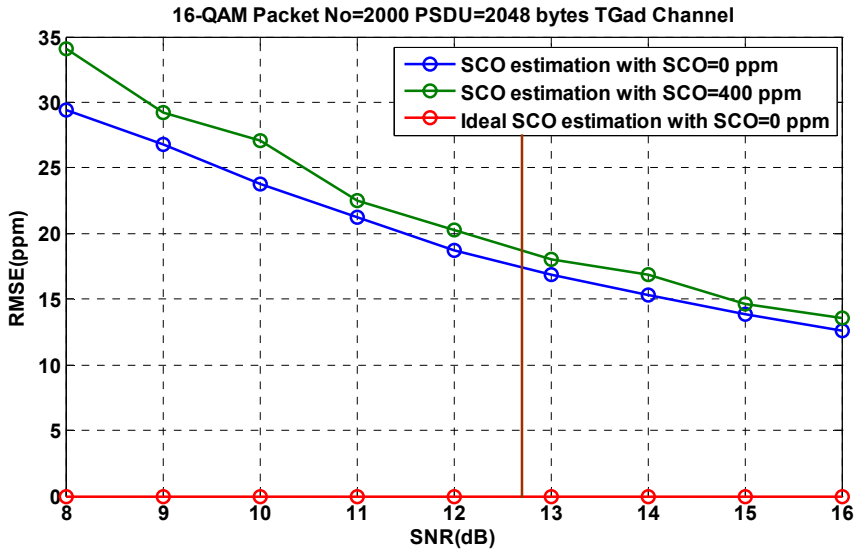


Figure 4.3: The root mean square error of after coarse SCO tracking

The required packet-error rate (PER) is 1% in 802.11ad. After timing acquisition, SCO estimation and pilot tracking scheme for residual SCO, the performance compare with perfect synchronization at 1% PER, SNR losses are about

0.7 dB of SCO = 0 ppm and 0.9 dB of SCO = 400 ppm, as shown in Figure 4.4.

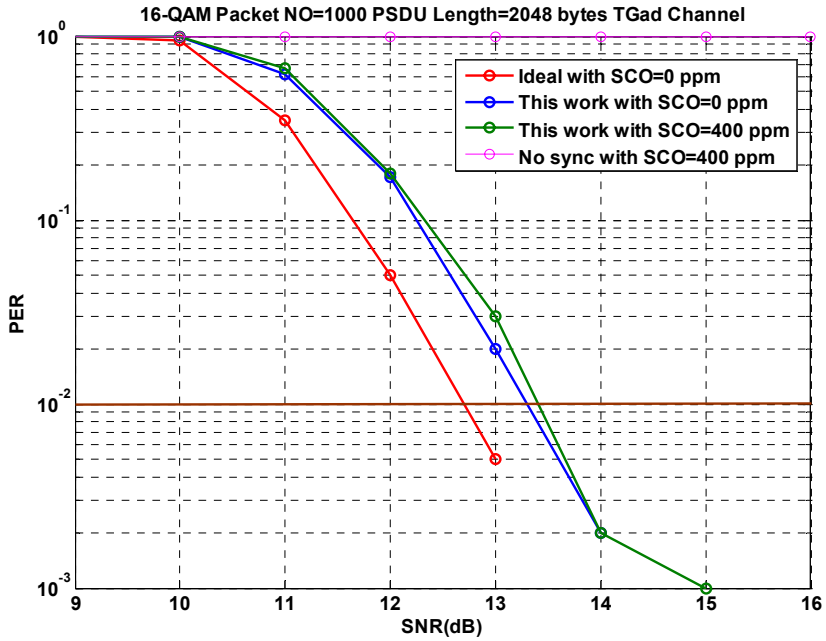


Figure 4.4: The system performance

The required packet-error rate (PER) is 1% in 802.11ad. Figure 4.5 displays the offset tolerance of the FD synchronizer include timing acquisition, SCO estimation and pilot tracking scheme with various SNR which can be as high as -300~400 ppm, much larger than the ±20 ppm in 802.11ad standard.

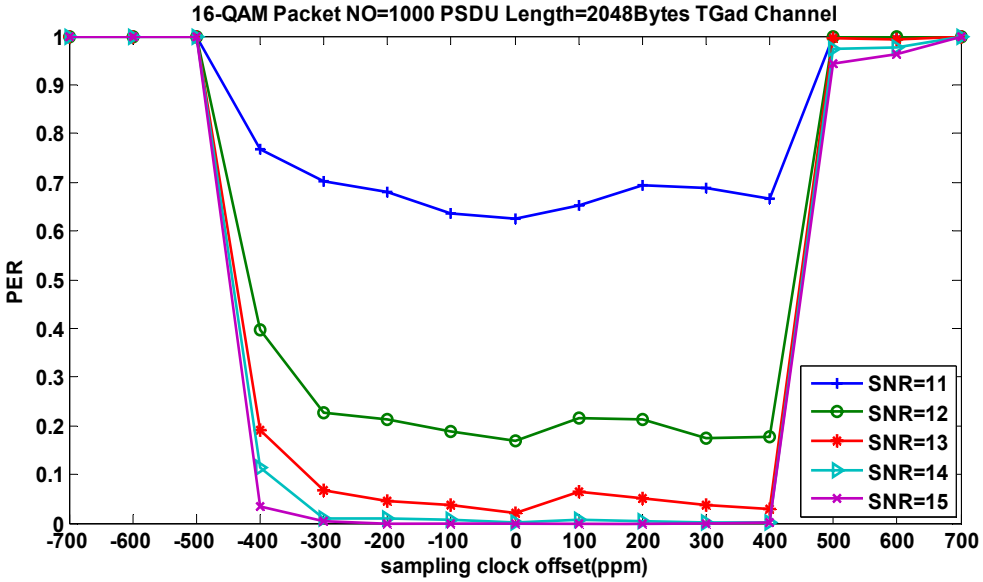


Figure 4.5: The offset tolerance of the FD synchronizer

Chapter 5

Hardware Implementation

A frequency-domain synchronizer for 128-FFT OFDM systems is implemented. Figure 5.1 shows the block diagram, and figure 5.2 shows the architecture of hardware implementations, and the input are the received data after 128-FFT. In the architecture of timing synchronizer, the algorithms are described in chapter3.

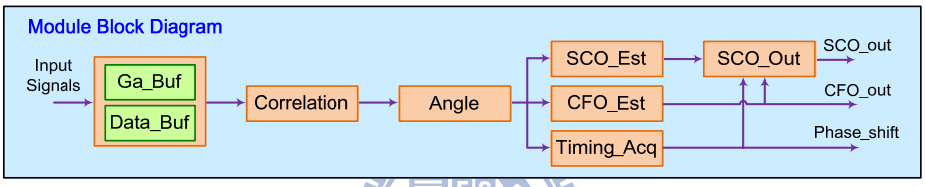


Figure 5.1: Module block diagram

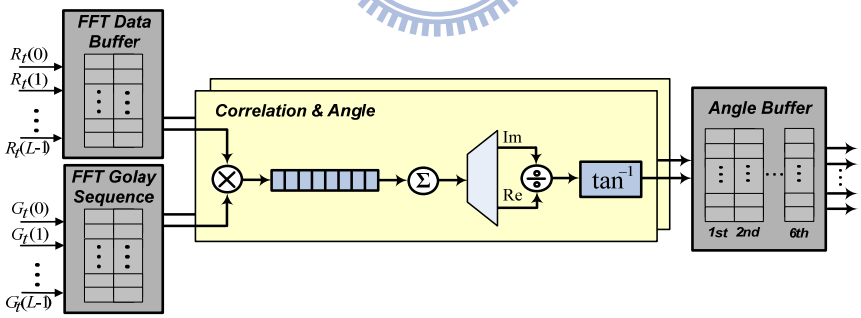


Figure 5.2(a): Part I. buffer, correlation, angle estimation

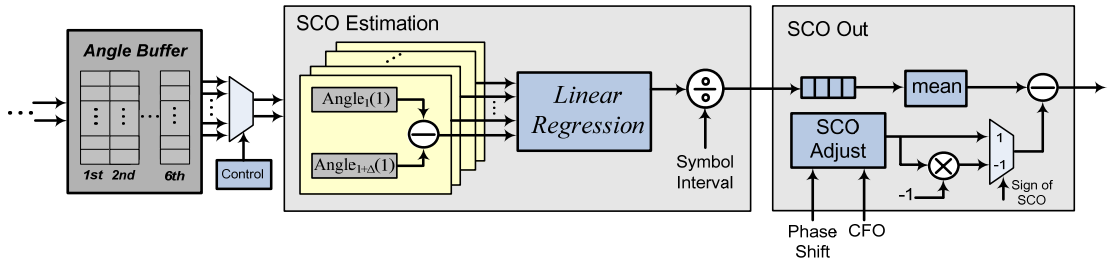


Figure 5.2(b): Part II. SCO estimation

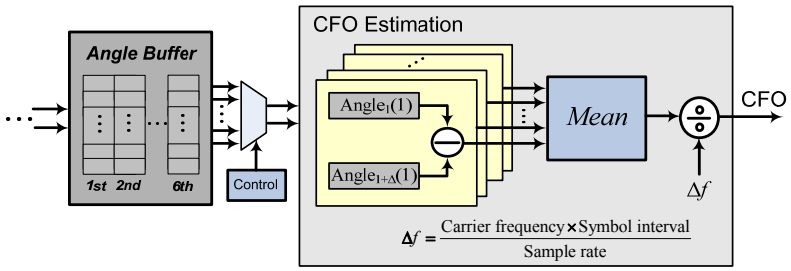


Figure 5.2(c): Part II. CFO estimation

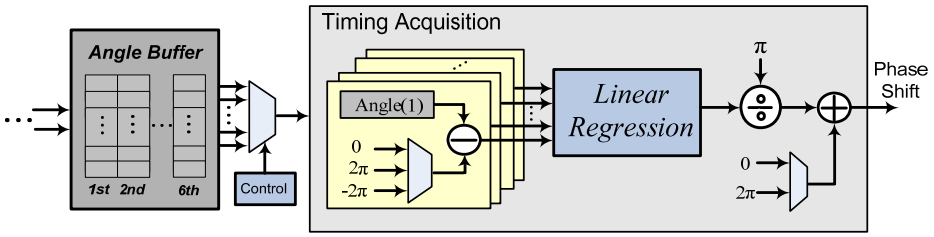


Figure 5.2(d): Part II. Timing acquisition

Hardware Specification	
Application	IEEE 802.11ad
Sample Rate	2.64 GHz
Symbol Rate(After 128-FFT)	20.625 MHz
Pipeline Clock	12 ns
Technology	65 nm CMOS

Table 5-1: Hardware specification

Module Name	Gate Count	Power
Data Buffer	41.5k	2.4294mW
Correlation	75k	1.2233mW
Angle	25k	0.5214mW
SCO Estimation	7.5k	0.2614mW
CFO Estimation	4k	0.0624mW
Timing Acquisition	5k	0.0987mW
Summary	158k	4.5966mW

Table 5-2: Synthesis report

Chapter 6

Conclusion and Future Work

This thesis, based on the architecture and the preamble structure of IEEE 802.11ad standard, investigate the frequency-domain timing synchronizer include timing acquisition, SCO estimation and pilot tracking scheme. Performances are measured under the TGad channel. At 1% PER and SCO tolerance range is -300~400-ppm, the SNR loss is only 0.8~1.4 dB in frequency-selective fading. From simulation results, the frequency-domain synchronizer has wide SCO tolerance.

We can improve the frequency-domain synchronizer by reducing complexity, the number of preamble and enhancing the accuracy of SCO estimation. In the thesis, we only consider the multipath and AWGN, and timing error. However, timing synchronization is in the first stage of receiver, there will be many several kinds of effects which are not improved yet. Hence, we have to improve the FD synchronizer again the tolerance of these effects in the future.

	[12]	[13]	[18]	[19]	This work
System Type	OFDM +64-QAM	OFDM +4-QAM	OFDM 64-QAM	OFDM 16-QAM	**OFDM +16-QAM**
Operation Domain	Frequency Domain	Frequency Domain	Frequency Domain	Time domain	**Frequency domain**
Architecture	Interpolator	Phase in Freq.	Interpolator	Interpolator	**Non-PLL ADCM (ADCM)**
Required Format	Pilot	Preamble	Preamble + Pilot	Pilot	**Preamble + Pilot**
Sampling Rate	N/A	N/A	4x	4x	1x
Cycle Count	N/A	N/A	N/A	100 symbols	**92 symbols (Include 6 preamble)**
Tolerant Range	±20ppm	400ppm	±200ppm	±100ppm	**-300 ~400 ppm**

Table 6-1: Features of the different timing recovery

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