Chapter 7
Conclusion and Future Work

7.1 Conclusion

In this thesis, we have analyzed different architectures and different algorithms. From this analysis, we designed a high-speed FFT architecture based on the radix-8 algorithm. In our design, we proposed an address generation method that can be used in both fixed and mixed radix algorithms. We also proposed a twiddle factor design with variable length. The wordlength of the twiddle factor is 12 bits for real and imaginary parts. The input and output wordlength uses 16 bits for both real and imaginary parts for variable length FFT. The variable length FFT processor was coded in Verilog and synthesized using Synopsys with TSMC 0.25 μm process. We take speed into consideration and so our performance evaluation is depicted in Table 5.21. Our proposed architecture can be used in wired communication systems like ADSL and VDSL.

7.2 Future Work

This section suggests future work with regard to the FFT processor using the following approach:

- Implement DMT based VDSL system with consideration of the problems of timing recovery, equalization, and channel coding.

- We use a fixed-point simulation for data word length. A floating-point simulation can achieve a higher precision result.
- The addition and multiplication hardware design are optimized with low cost.
- It is very important to implement low power circuitry in industry. In our FFT design, we did not emphasize low power design considerations. We think the cache memory-based FFT architecture is the best choice.