

# REFERENCES

- [1] ETSI TS 101 270-2 (V1.1.1): *Transmission and Multiplexing* <sup>TM</sup>; *Access transmission systems on metallic access cables; Very high speed Digital Subscriber Line (VDSL); Part 2: Transceiver specification.*, Feb 2001.
- [2] Chiao-Chih Chang, Min-Shu Wang, Tzi-Dar Chiueh, "Design of a DMT-based baseband transceiver for very high speed digital subscriber lines," *IEEE Asia Pacific Conference on ASIC*, pp. 367-370, August 2002.
- [3] J.M. Cioffi, et al, "Very high speed digital subscriber Lines," *IEEE Commun.Mag.*, pp.72-79, April 1999.
- [4] T. Starr, J.M. Cioffi and P.J. Siverman, *Understanding digital subscriber line Technology*, Prentice Hall, 1999.
- [5] A.V. Oppenheim R.W. Schaffer, *Discrete Time Signal Processing*, Prentice Hall Inc., 1999.
- [6] Yeong-Terng Lin, *Design and Implementation of a Variable Length FFT Processor for OFDM Systems*, NTU, Master Thesis, June 2001.
- [7] T.D, "An extended split-radix FFT algorithm," *Signal Processing Letters*, IEEE, vol.8, Issue. 5, pp. 145-147, May 2001.
- [8] L.Jia, Y.gao, and H.Tenhunen, "Efficient VLSI implementation of radix-8 FFT algorithm," to appear in the 1999 *IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (PACRIM'99)*, Canada, Aug.22-24,1999.
- [9] L.Tia, Y.Gao, J.Isoaho, and H.Tenhunen, "A new VLSI Oriented FFT Algorithm and Implementation," accepted by *11<sup>th</sup> Annual IEEE International ASIC Conference*, pp.337-341, September 1998.
- [10] H.V. Sorensen, M.T. Heideman, and C.S. Burrus, "On computing the

- split-radix FFT,” *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 34, Issue. 1, pp. 152-156, Feb 1986.
- [11] B.M.Baas, “A low-power, high-performance, 1024-point FFT processor,” *IEEE Journal of Solid-State Circuits*, vol. 34, Issue. 3, pp. 380-387, March 1999.
- [12] T. Widhe, J. Melander, L. Wanhammar, “Design of efficient radix-8 butterfly PEs for VLSI,” *IEEE International Symposium on Circuits and systems*, vol. 3, pp. 2084-2087, June 1997.
- [13] Jun-Jie Fang, *Design of FFT Processor*, NCTU, Master Thesis, August 2001.
- [14] E.E. Swartzlander, W.K.W. Young, S.J. Joseph, “A radix 4 delay commutator for fast Fourier transform processor implementation,” *IEEE Journal of Solid-State Circuits*, vol. 19, Issue. 5, pp. 702-709, Oct 1984.
- [15] G. Bi, E.V. Jones, “A pipelined FFT processor for word-sequential data,” *IEEE Transactions on Acoustics, Speech, and Signal Processing*, vol. 37, Issue. 12, pp. 1982-1985, Dec. 1989.
- [16] S. Saponara, L. Serafini, L. Fanucci, “Low-power FFT/IFFT VLSI macro cell for scalable broadband VDSL modem,” *The 3rd IEEE International Workshop on System-on-Chip for Real-Time Applications*, pp. 161-166, July 2003.
- [17] J. Lihong, G. Yonghong, H. Tenhunen, “A pipelined shared-memory architecture for FFT Processors,” *The 42nd Midwest Symposium on Circuits and Systems*, vol. 2, pp. 804-807, Aug. 1999.
- [18] B.S. Son, B.G. Jo, M.H. Sunwoo, and Yong Serk Kim, “A high-speed FFT processor for OFDM systems,” *IEEE International Symposium on Circuits and Systems*, vol. 3, pp. :III-281 - III-284, May 2002.
- [19] Jen-Chih Kuo, Ching-Hua Wen, An-Yeu Wu, “Implementation of a programmable 64~2048-point FFT/IFFT processor for OFDM-based communication systems,” *Proceedings of the 2003 International Symposium*

- on Circuits and Systems*, vol. 2, pp. II-121 - II-124, May 2003.
- [20] H.F. Lo, M.D. Shieh, and C.M. Wu, "Design of an efficient FFT processor for DAB system," *IEEE International Symposium on Circuits and Systems*, vol.4, pp.654-657, May 2001.
- [21] M. Hasan, T. Arslan, "FFT coefficient memory reduction technique for OFDM applications," *IEEE International Conference on Acoustics, Speech, and Signal Processing*, vol. 1, pp. I-1085 - I-1088, May 2002.
- [22] Ching-Chi Chang, Muh-Tian Shie, and Chorng-Kuang Wang, "A VLSI architecture of DMT based transceiver for VDSL system," *IEEE Asia-Pacific Conference on Proceedings*, pp.363-366, Aug 2002.
- [23] Sang-Chul Moon, In-Cheol Park, "Area-efficient memory-based architecture for FFT processing," *Proceedings of the 2003 International Symposium on Circuits and Systems*, vol. 5, pp. V-101 - V-104, May 2003.
- [24] E.H.Wold and A.M. Despain, "Pipeline and Parallel pipeline FFT processors for VLSI implementation," *IEEE Transactions on Computers*, C-33(5): pp.414-426, May 1984.
- [25] A.M. Despain, "Fourier transform computer using CORDIC iterations," *IEEE Transactions on Computers*, C-23(10): 993-1001, Oct.1974.
- [26] A. Sadat, W.B. Mikhael, "Fast Fourier Transform for high speed OFDM wireless multimedia system," *Proceedings of the 44th IEEE 2001 Midwest Symposium on Circuits and Systems*, vol. 2, pp. 938 – 942, Aug. 2001.
- [27] Wen-Chang Ye, Chein-Wei Jen, "High-speed and low-power split-radix FFT," *IEEE Transactions on Signal Processing*, vol. 51, pp.864-874, March 2003.
- [28] Cheng-Han Sung, Kun-Bin Lee, and Chein-Wei Jen, "Design and implementation of a scalable fast Fourier transform core," *IEEE Asia-Pacific Conference on ASIC proceedings*, pp. 295-298, Aug. 2002.