實現可變長度之FFT處理器於VDSL系統

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中文摘要

本論文是以建構VDSL中的DMT系統調變為主，而DMT系統中最重要的調變技術為FFT與IFFT。由於IFFT可由FFT來實現，所以在本論文中，我們只針對 FFT 的晶片來做研究。首先我們先比較 DFT 化成 FFT 的各種不同的algorithm，比較各種不同的algorithm後，我們決定利用 mixed radix 8+4、mixed radix 8+2、與radix 8的演算法來實現我們的晶片。在以前的FFT晶片中，大部份都是利用pipeline的架構來實現FFT晶片，而有少部份人提出了memory 的架構方式來實現，根據我們實驗與分析的結果，我們決定採用memory 的架構。在建構整個 FFT 晶片前，首先要做系統分析，系統分析我們可分三個步驟，第一個步驟我們利用Matlab模擬IC有效位元數。第二個步驟，我們將開始設計架構，系統架構分成 fft_ctrl、SRAM_model、rom_table、radix8_butterfly、address_generator、serial_parallel、fft_reorder 等。第三個步驟為驗証設計的FFT晶片是否正確。在本論我們提出新的 memory 架構，此架構具有高速、省面積的特性。我們並提出可變長度的address generator，所以我們的架構可做任意點數的FFT。

Implementation of a variable length FFT processor for VDSL system

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Abstract

In this thesis, we focus on a DMT modulation in very high-speed digital subscriber line (VDSL) communication systems. The FFT/IFFT is one of the main components in DMT systems. The IFFT can be realized by sharing hardware with the FFT hardware and so we only implement the FFT architecture. At first, we compare different FFT algorithms, and we use the radix-8 DIF FFT algorithm. The FFT lengths in VDSL are 512, 1024, 2048, 4096 and 8192 points. The radix-8 algorithm cannot deal with the 1024/2048/8192-point FFT because it only operates as an 8^n-point FFT. Therefore, we use mixed radix 8+2 and mixed radix 8+4 algorithms that can operate on 1024/2048-point data sequences using the radix-8 butterfly architecture. Before implementing the FFT hardware design, we must analyze the system requirements. There are three steps for our design flow. The first step is to determine the effective word length by using Matlab simulation. The second step is to design the architecture, which is composed of the individual components such as fft_ctrl, SRAM_model, rom_table, radix8_butterfly, address_generator, serial_parallel and fft_reorder. The third step is to verify our FFT IC design. We propose a memory-based architecture that can achieve high operating speeds and is area efficient. In addition, we design an address generation algorithm which we use in various-length FFTs. So, our proposed architecture can operate on any length FFT.