

CONTENTS

Chinese Abstract	I
English Abstract	II
Acknowledges.....	III
Contents	IV
List of Tables.....	VII
List of Figures.....	IX
Chapter 1 Introduction	1
1.1 General Introduction	1
1.2 Contributions.....	2
1.3 Overview.....	3
Chapter 2 Very High-Speed Digital Subscriber Lines.....	4
2.1 Different Types of DSL.....	4
2.2 VDSL Network.....	5
2.3 Effect of Noises for VDSL Transmission	6
2.4 DMT Modulation for VDSL.....	7
Chapter 3 Classification of FFT Processor Algorithms	10
3.1 Discrete Fourier Transform (DFT).....	10
3.2 Fixed Radix Algorithms	11
3.2.1 Radix-2 DIF FFT Algorithm.....	11
3.2.2 Radix-4 DIF FFT Algorithm.....	15
3.2.3 Radix-8 DIF FFT Algorithm.....	16
3.3 Split Radix Algorithms	19
3.3.1 Split Radix-2/4 Algorithm.....	19
3.3.2 Split Radix-2/8 Algorithm.....	21
3.4 Mixed Radix Algorithm	24
Chapter 4 Classification of FFT Processor Architectures.....	25
4.1 Pipeline Architecture.....	25

4.1.1	Single Path Delay Feedback Architecture.....	26
4.1.2	Multiple Path Delay Commutator Architecture.....	28
4.1.3	Single Path Delay Commutator Architecture.....	31
4.2	Memory-Based Architecture.....	33
4.2.1	Memory-Based Processing Method.....	34
4.2.2	Radix-2 Memory-Based Architecture.....	36
4.2.3	Radix-4 Memory-Based Architecture.....	37
4.3	Comparison of Different Architectures.....	38
Chapter 5	Implementation of the Proposed FFT Architecture.....	39
5.1	Algorithmic and Architectural design.....	39
5.2	Proposed Architecture Design.....	40
5.3	FFT Control Block Design.....	41
5.4	Serial to Parallel Design.....	42
5.5	Radix-8 Butterfly Processing Element.....	43
5.5.1	Butterfly Computation.....	44
5.5.2	Sharing the Addition Operator Hardware.....	48
5.5.3	Complex Multiplier Hardware Design.....	53
5.6	Twiddle Factor ROM Design.....	55
5.6.1	Reduced Twiddle Factor ROM Design.....	55
5.6.2	Twiddle Factor Circuit Design for Fixed FFT Length.....	61
5.6.3	Twiddle Factor Design for Our Variable FFT Length.....	62
5.7	SRAM Model Design.....	64
5.7.1	SRAM Design.....	64
5.7.2	Read /Write Data Commutator.....	67
5.8	Address Pointer Generation.....	70
5.8.1	Data Address Pointer Generation.....	70
5.8.2	Twiddle Factor Coefficient Address Pointer Generation.....	77
5.9	Hardware Implementation Rules for Address and Data Control.....	83
5.10	Data Reorder Design.....	92
5.11	Performance Evaluation.....	93
Chapter 6	FFT Chip Design Simulation and Analysis.....	94

6.1	Matlab Simulation and Analysis	94
6.1.1	Simulation for Fixed and Mixed radix FFT algorithm	94
6.1.2	Simulation of Twiddle Factor and Databus Bit Length	98
6.2	Verilog Simulation and Analysis	100
6.3	Pad Location and Floorplan	105
Chapter 7 Conclusion and Future Work		111
7.1	Conclusion	111
7.2	Future Work	111
References		113
Appendix		116
Autobiography		117

