Chapter 1
Introduction

The *Discrete Fourier Transform* (DFT) is widely used in digital signal processing (DSP) applications in recent years. The DFT is never computed directly because its computations require excessive arithmetic calculations, but instead applications use the high performance *Fast Fourier Transform* (FFT) to produce a good result within a required time. FFT algorithms decompose the fundamental calculation of the DFT of a sequence of length N into continuously smaller subsequences. Today, the FFT algorithm is applied not only in DSP, image processing and digital data transmission systems such as the DSL system, digital audio/video broadcasting and 802.11a wireless LAN, but also in biomedical electronic engineering and home networking. Therefore, the improving the efficiency of FFT architectures and algorithms is a very attractive research topic in recent years.

1.1 General Introduction

The FFT and *Inverse FFT* (IFFT) operations are used in multi-carrier modulation and demodulation techniques such as Orthogonal Frequency Division Multiplexing (OFDM) and Discrete Multi Tone (DMT). Ideally, serially transmitted data is modulated into parallel orthogonal data by using an IFFT and the received data is demodulated by using an FFT with the same structure. Hence, FFT/IFFT operations are the key issue for the successful realization of communication systems. In order to realize various applications of OFDM and DMT system, we must be able to know the transform length of the FFT. There are also many methods to implement FFT/IFFT

algorithms such as FPGA implementation or Integrated Circuit Design. The objective of our work begins with simulated using Matlab, coded using Verilog, and synthesized using the TSMC 0.25um Fabrication Process.

1.2 Contributions

FFT/IFFT processor has variable transform length of 512, 1024, 2048, 4096 and 8192 –points in VDSL system. To be able to compute variable FFT length, we must to implement FFT processor with variable length. Therefore, we propose new memory based FFT architecture to meet the throughput rate requirement of VDSL specifications. The major contributions for our proposed architecture are

(1) It can satisfy high speed and low cost.

(2) It provides simple address pointer generation to prevent conflict data and can not only be used for fixed the radix-8 architecture, but also can be used for the radix-8/4 and radix-8/2 architectures.

(3) We also propose a twiddle factor coefficient circuit design for variable lengths of 512, 1024, 2048 and 4096-points.

1.3 Overview

In this thesis, Chapter 2 begins with the background of Discrete Multi-Tone (DMT) modulation and Very High Speed Digital Subscriber Line (VDSL). Chapter 3 and Chapter 4 provide a basic introduction and characteristic of different algorithms and architectures of the FFT. Chapter 5 focuses on the proposed architecture. Chapter 6 discusses the simulation result with Matlab and Verilog. Finally, Chapter 7 summarizes our work and gives brief recommendations for future work.