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碩 士 論 文

用於溫度感應器之正比絕對溫度電流與能帶隙參考電流產生器

The Current Generators of Proportional to Absolute Temperature and Bandgap Reference for Temperature Sensor

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中華民國九十三年七月

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摘要

此論文描述了可攜於深次微米製程且以台灣積體電路公司 0.25 微米製程製成之正比絕對溫度電流與能帶隙參考電流產生器的設計與實現。此提出的電路包括了正比絕對溫度電流產生器，能帶隙參考電流產生器，功率重置電路與曲線矯正電路。此提出的正比絕對溫度電流的溫度誤差不超過攝氏一度且能帶隙參考電流的最大溫度係數為每攝氏一度變化 30 微安培。以功率重置電路取代了初始啟動電路降低了百分之九的功率消耗且曲線矯正電路改善了能帶隙參考電流 在低溫時的準確度。此提出的電路整體功率消耗為 550 微瓦特，其面積為 260 微米×200 微米。

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Abstract

This thesis describes the design and implementation of proportional to absolute temperature (**PTAT**) and bandgap reference (**BGR**) current generators, which are portable with deep sub-micron process and fabricated by TSMC 0.25μm technology. The proposed circuits consist of PTAT current generator, BGR current generator, power-on-reset (**POR**) circuit and curvature corrected circuit. The temperature error of proposed PTAT current does not exceed one degree, and the maximum temperature coefficient of proposed BGR is about 30ppm per one degree. The POR circuit replaces start-up circuit to reduce the power dissipation about 9%, and the curvature corrected circuit improves the accuracy of BGR in low temperature. The overall power dissipation of proposed design is 550μW, and the area is 260μm×200μm

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I would like to thank other mates of the laboratory and classmates of the university. They bring me a happy life when I am in graduated.

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Chapter 1 Introduction

1.1 Motivation

CMOS technologies have evolved significantly in last few years, allowing the transistors density on a chip to increase and reducing the cost of overall chip [1]. Large gate counts and high operating frequencies allied with the high performance systems led to considerable increases in temperature of overall chip. However, the overheated chips will reduce the reliability and cause parameter mismatch to impact the performance [1][2]. For these reason described above, low cost and high performance temperature sensors shown in Figure 1.1.1 are gradually required in modern VLSI systems in order to detect the temperature of overall chip [3]. In this thesis, two important blocks in temperature sensor, Proportional to absolute temperature (**PTAT**) circuits and bandgap reference (**BGR**) circuits, are implemented by TSMC 0.25μm technology and the details in our design will be described in first two chapters.

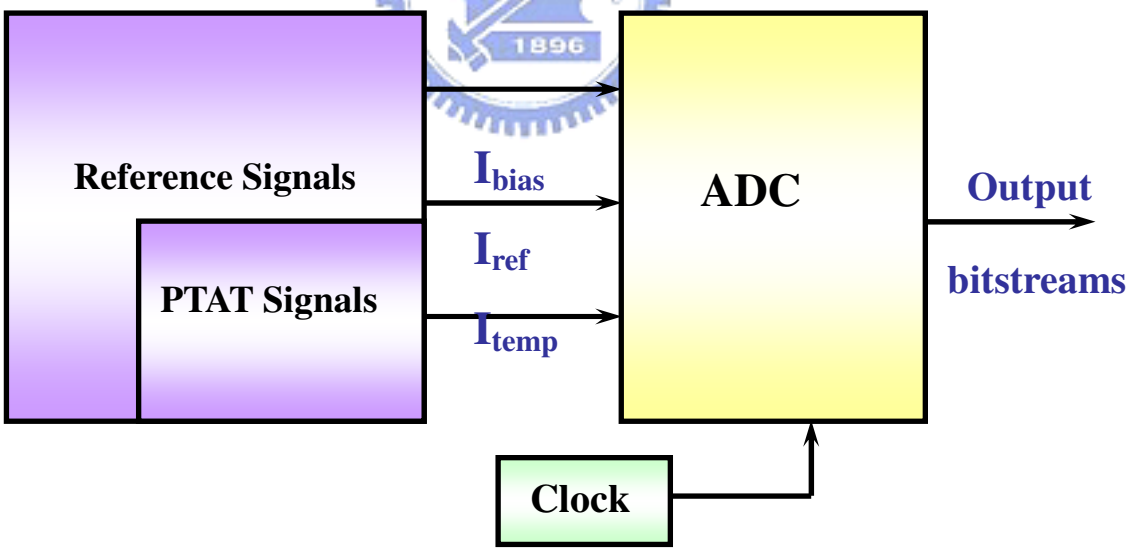

Figure 1.1.1 The Block Diagram of Temperature Sensor

PTAT is the circuit which generates signal proportional to absolute temperature and its functionality is to detect the temperature in temperature sensor. BGR is the circuit which generates a biasing signal independent of temperature and supply voltage is

provided to another block of temperature sensor, analog-to-digital convert (**ADC**), to convert analog PTAT input signals to digital one.

When analog signal is converted to digital one, the addition and minus operation of signals will be used. For voltage mode signals, to achieve these operations will cost more transistors [3]. However, current mode signals only uses one transistor to achieve these operations. The current mode signal is adopted in our design.

The PTAT and BGR current generators have been proposed [3][4], and implemented in 0.7um and 0.6um process, however, there are still some challenges for PTAT and BGR circuits as following:

(1) Additional power dissipation by start-up circuits
(2) Compatible with deep sub micron process.
(3) High accuracy of BGR signals

For (1), the demand for low power VLSI increases, the power consumption of start-up circuits of BGR will make the power consumption of overall BGR not be scaled down [5]. A simple power-on-reset (**POR**) circuit will be introduced to replace the start-up circuit to make the power consumption for starting up be zero. If the power consumption caused by start-up circuit can be eliminated, the power dissipation in PTAT and BGR can be lowered by a factor of supply voltage scaled down.

For (2), as process technologies are scaled down into the deep sub micron eras, the current generators of PTAT and BGR are necessary designed using new deep sub-micron process to integrate with other digital cores in System-on-Chip.

For (3), the accuracy of BGR is especially important for ADC block of temperature sensors [6]. For increasing the accuracy of temperature sensor, adding curvature corrected circuits is necessary. Many curvature corrected circuits have been proposed [7][8]. Their correction approaches are adding a proportional to temperature resistance in the tail of BGR cells, but increase the complexity of the circuits. For reducing the complexity, a simpler curvature corrected circuit will be presented here.

In this thesis, PTAT and BGR circuits are implemented by single-poly-five-mental (**1P5M**) TSMC 0.25um process, and proposed a simple curvature corrected circuit for better accuracy of BGR and a POR circuit for reducing start-up power.

1.2 Organization

In Chapter 2, the background of PTAT and BGR are discussed. First, Emitter-Base-Junction (**EBJ**) voltage is introduced and the temperature dependence of it is also derived. Second, several architectures of conventional PTAT and start-up circuits are introduced. Third, the ones of BGR are also introduced, too. Then, some non-ideal effects are in consideration of BGR and PTAT. Finally, summery ends this chapter.

Chapter 3 introduces our proposed design, and explains the revolution of our proposed design consisting of PTAT, BGR, curvature correction, and POR circuit used to start up PTAT and BGR. Then, some design considerations are discussed and explained. Finally, summary of our proposed design are described.

Chapter 4 introduces simulation and experiment results. First, the Hspice simulation of basic PTAT and BGR is shown, so are POR and curvature corrected circuits. Second, layout consideration and measurement setup are described. Finally, the experiment results and discussion are shown.

Chapter 5 is the conclusion and future work of this thesis which describes the summary of this proposed circuit.

Chapter 2 Background

This chapter provides the background that completely reviews the Proportional to absolute temperature (**PTAT**) and Bandgap reference (**BGR**).

PTAT is the circuit which generates voltage or current signal proportional to absolute temperature. There are two ways to achieve proportional to absolute temperature signals; the first one is to operate MOS in weak inversion region, and the second one is to use the difference between two terminals of bipolar junction transistors (**BJT**) emitter base junction (**EBJ**) voltage. The first method is difficult because the operation region of MOS in weak inversion is quite narrow. If any variation in the circuit is introduced, the operation region may drift to another one. From above discussion, the second way is adopted in our design.

BGR which generates a biasing signal independent of temperature and supply voltage is key elements in analog and mixed-mode circuit. They determine the overall accuracy in many data acquisition systems. The accuracy of temperature sensor is also mainly dependent on the quality of its reference signals.

In this chapter, first, EBJ voltage of BJT is reviewed, because the PTAT of our design which will be mentioned in the chapter 3 is implemented by the difference between EBJ voltage of two BJTs. Second, the principles of PTAT and BGR are introduced and several architectures of PTAT and BGR are also described. Third, non-ideal effects of PTAT and BGR are considered, and the techniques for reducing these effects are also described.

Before understanding the principles of PTAT and BGR, the characteristics of EBJ voltage of BJTs must be understood as section 2.1 which illustrates the details of EBJ voltage of BJTs.

2.1 Emitter Base Junction Voltage of Bipolar Junction Transistors

In this section, the EBJ voltage of BJTs will be described. As described above, BJT is a necessary part in PTAT and BGR, but MOSFETs are also used in PTAT and BGR. This indicates that both BJT and CMOS technologies must be used simultaneously in PTAT and BGR, but this solution costs too much and degrades the

performance of overall circuits. It is possible to fabricate BJTs in modern CMOS process, and such types of BJT are called “parasitic BJT”. By using parasitic BJTs, PTAT and BGR can be integrated on the same die. Since parasitic BJTs are utilized in proposed design, following section describes the types and their characteristics of CMOS parasitic BJTs.

2.1.1 Bipolar Junction in CMOS Technology

There are two types of parasitic BJT in CMOS technology, which is described as following:

(1) Lateral BJTs.

(2) Vertical BJTs

For (1), the quality of the lateral bipolar junction transistor depends on the IC fabrication, and the leakage current toward substrate is large (via the vertical BJT).

The vertical BJT shown in Figure 2.1.1 seems to be the best choice for integrator PTAT. The quality of this transistor is comparable to transistors in standard CMOS process, so vertical BJT will be adopted for our proposed design in later chapter and its EBJ voltage will be explain in later section. The main disadvantage of vertical BJT is lack of a free collector terminal, because the collector must be terminated to the most negative voltage.

c

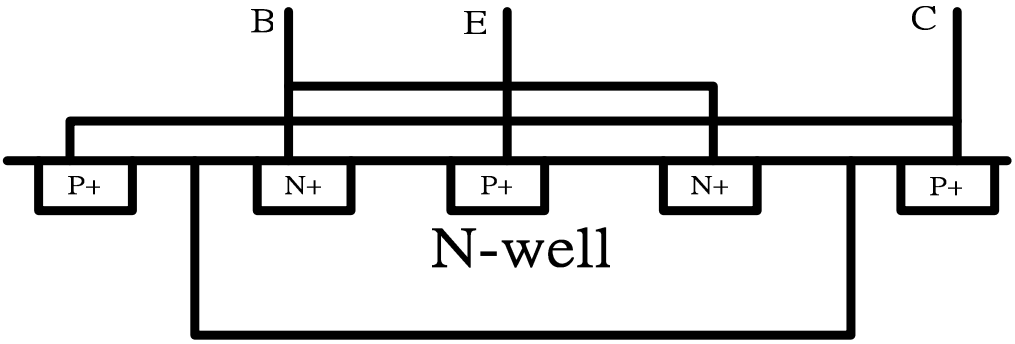

Figure 2.1.1 Substrate Vertical PNP Transistor in CMOS Technology

2.1.2 The Principle of Emitter Base Junction voltage of BJT

The EBJ voltage of BJT is simple and sensitive to temperature. It is widely used as a temperature sensing element in embedded temperature sensor. The temperature dependence of EBJ voltage is discussed in this section.

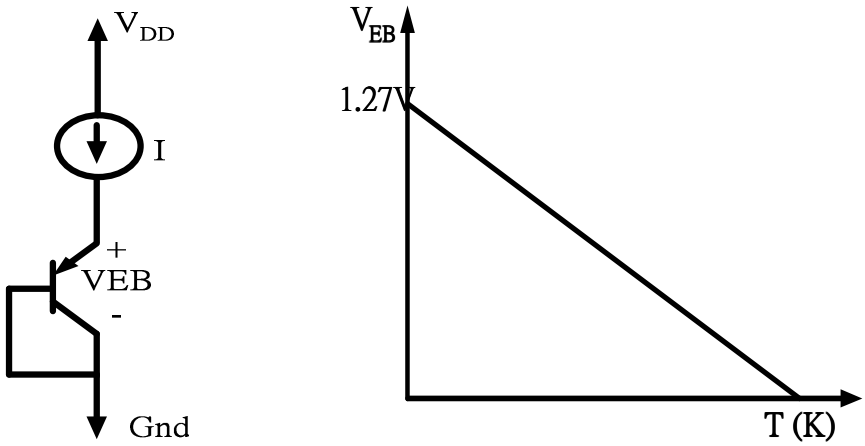

Figure 2.1.2 Collector Currents of BJT Versus Absolute Temperature T

As shown in Figure 2.1.2, the collector and base are connected so that early effect can be ignored. When the applied bias current is constant, the EBJ voltage decreases almost linearly to absolute temperature. The approximation is shown as following:

$$V_{EB}(T) = 1.27 - K_0 T \tag{2-1}$$

where K_0 is a constant about 2mV/K. It depends on the bias current and technology parameters. T represents the absolute temperature.

To understand the dependence on temperature of EBJ voltage, A detail mathematical equation is derived

$$V_{EB}(T) = U_T \ln \frac{I_C}{I_S} = \frac{kT}{q} \ln \frac{I_C}{I_S} \tag{2-2}$$

where Is represents the reverse saturation current of P-N junction, T is the absolute temperature, k is the Boltzmann's constant, and q is the electron charge. In this equation, V_{EB} seems to be proportional to absolute temperature. However, Is and Ic are strongly dependent on absolute temperature, V_{EB} is not proportional to absolute temperature. The saturation current Is can be related to the device structure by

$$I_S = B' n_i^2 T \mu' \tag{2-3}$$

$$I_C = G T^m \tag{2-4}$$

where n_i is the intrinsic minority carrier concentration, μ' is the average electron mobility in the base, and G is temperature independent quantity, However, n_i and μ' are temperature dependent, given by

$$n_i^2 = DT^3 \exp(-\frac{V_{G0}}{U_T}) \tag{2-5}$$

$$\mu' = CT^{-n} \tag{2-6}$$

where C and D are temperature independent quantities. V_{G0} is the bandgap voltage of silicon extrapolated to 0^oK. When a reference temperature is specified, the overall temperature dependence of EBJ voltage can be derived from Eq.2-3 to Eq.2-6.

$$V_{EB}(T) = V_{G0}(1-\frac{T}{T_r}) + \frac{T}{T_r}V_{EB}(T_r) - \frac{kT}{q}(4-n-m)\ln\frac{T}{T_r}$$

$$= V_{G0}(1-\frac{T}{T_r}) + \frac{T}{T_r}V_{EB}(T_r) - \frac{kT}{q}(4-n-m)(\ln T - \ln T_r) \tag{2-6}$$

where Tr is reference temperature. For T is very close to Tr, then

$$\ln T \approx 1 + \frac{1}{T_r}(T-T_r) - \frac{1}{T_r^2}(T-T_r)^2 + \frac{1}{T_r^3}(T-T_r)^3 \tag{2-7}$$

From Eq.2-6 and 2-7, Eq.2-8 can be obtained

$$V_{EB}(T) = V_{G0}(1-\frac{T}{T_r}) + \frac{T}{T_r}V_{EB}(T_r) - \frac{kT}{q}(4-n-m)(\ln T - \ln T_r)$$

$$= V_{G0} + \frac{T}{T_r}(V_{EB}(T_r) - V_{G0}) + \frac{kT}{q}(4-n-m)\ln T_r - \frac{kT}{q}(4-n-m)[1+\sum_{i=1}^{\infty}\frac{(-1)^i}{T_r^i}(T-T_r)^i]$$

$$\approx V_{G0} + A_1T + A_2T^2 + A_3T^3$$

So,

$$V_{EB}(T) \approx V_{G0} + A_1T + A_2T^2 + A_3T^3 \tag{2-8}$$

Typically, A_1 is negative number, $V_{EB}(T)$ is negative TC and almost perfectly complementary to absolute temperature because slope of $V_{EB}(T)$ versus temperature is current dependent.

After understanding the characteristics of EBJ voltage of BJT, the principle of PTAT and BGR based on BJT devices can be introduced in following sections.

2.2 Proportional to Absolute Temperature (PTAT)

After finishing introducing parasitic BJTs and the characteristics of them, the principle of PTAT using BJT device is introduced as following:

2.2.1 The Principle of proportional to Absolute temperature

As illustrated in Figure 2.2.1, when both transistors are at the same temperature T, the difference of two EBJ voltage can be derived form Eq.2-2 as :

$$V_{PTAT} = V_{EB1} - V_{EB2} = \frac{kT}{q}\ln\left(\frac{I_{C1}}{I_{C2}}\frac{I_{S2}}{I_{S1}}\right) = \frac{kT}{q}\ln\left(\frac{M}{N}\right) \quad (2\text{-}9)$$

where M is emitter area ratio, and N is current source ratio. They have no temperature dependence, and only depend on devices geometry and current source ratio.

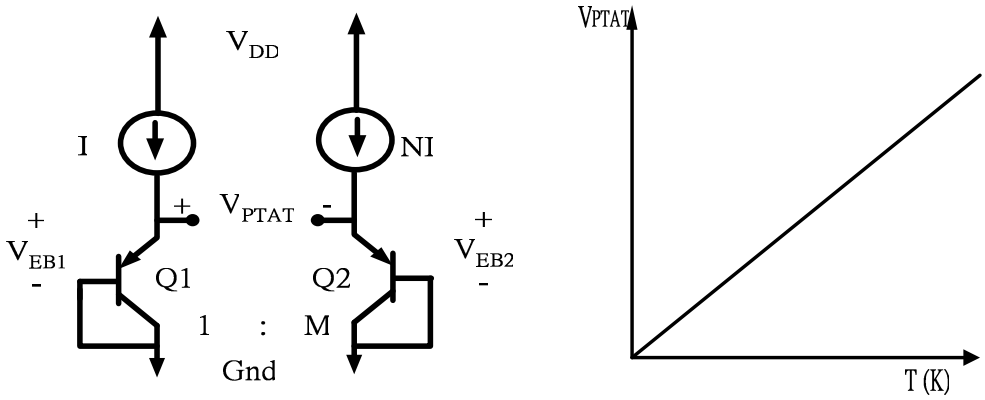

Figure 2.2.1 PTAT Voltage Versus Absolute Temperature T

From above equation, V_{PTAT} is directly proportional to absolute temperature T. The ratio kT/q is called the thermal voltage and equals to approximately 26mV at room temperature (T=300K). The TC of V_{PTAT} signal yields approximately 200uV/K for n being 10. This amplification factor, n, is set by the ratio of N and M.

2.2.2 PTAT Circuit Architecture

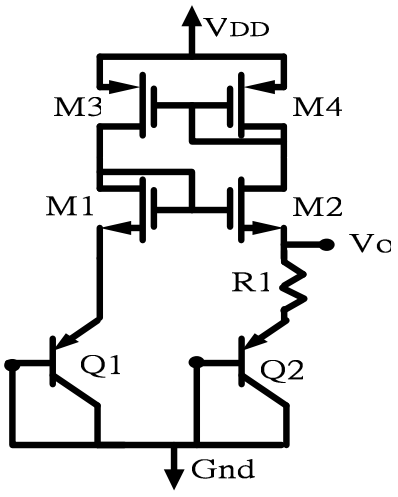

Figure 2.2.2 PTAT Voltage Using Self-Biasing Circuit

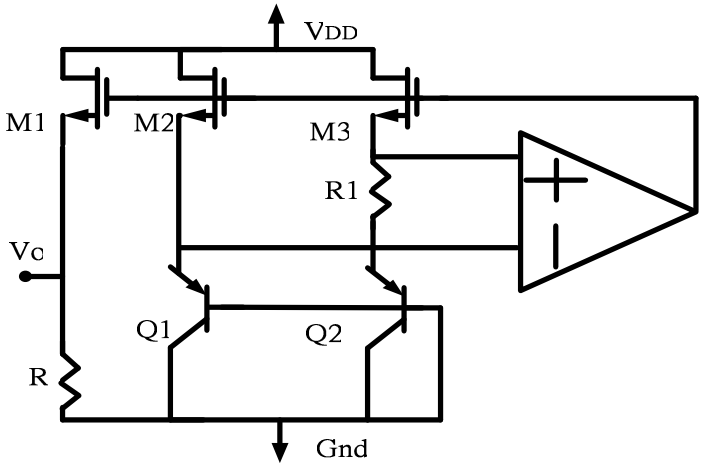

Figure 2.2.3 PTAT Voltage Using Operational Amplifier

There are two ways to achieve voltage addition and minus. The first one is using self-biasing circuit, and the second one is using operational amplifier (**Op-Amp**). Figure 2.2.2 is a PTAT voltage generated by self-biasing circuit. If M1~M4 are identical, the source voltage of M1 and M2 will be equal. The current through R1 will be proportional to absolute temperature. By using current mirror of M4 and M5, Vo be PTAT voltage. Figure 2.2.3 is also a PTAT voltage generated by operation amplifier. The topology of the operational amplifier is as following:

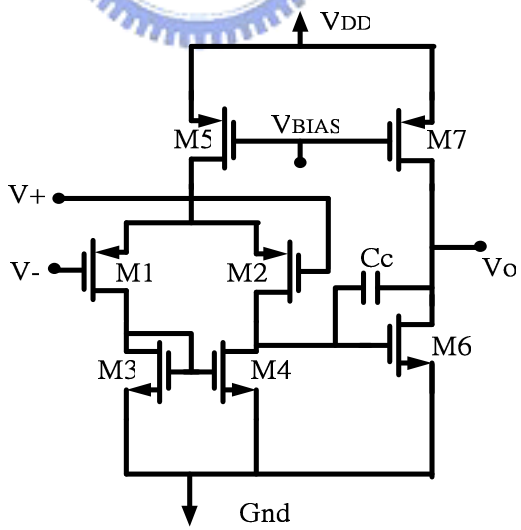

Figure 2.2.4 The Two Stage Operational Amplifier

A two stage Op-Amp is shown in the Figure 2.2.4. If the open loop gain of the Op-Amp is large enough, the gate voltage of M1 and M2 will be almost equal. Then, the drain voltage of M2 and M3 of the Figure 2.2.3 will be equal. The PTAT current is

mirrored by M1, and Vo will also be PTAT voltage. For reducing output loading effects, A voltage buffer can be added at the output, but additional offset and drift will be introduced.

2.2.3 Start-up Circuits

For the PTAT circuits shown in Figure 2.2.2 and Figure 2.2.3, they both have a second trivial steady state condition, cutoff ,when the currents of all branches are equal to zero. To prevent the PTAT circuit from settling to the wrong steady state condition (zero current state), a start-up circuit is necessary in all practical PTAT circuits. For the PTAT in the Figure 2.2.5, a start-up circuit is added to explain how the start-up circuit works.

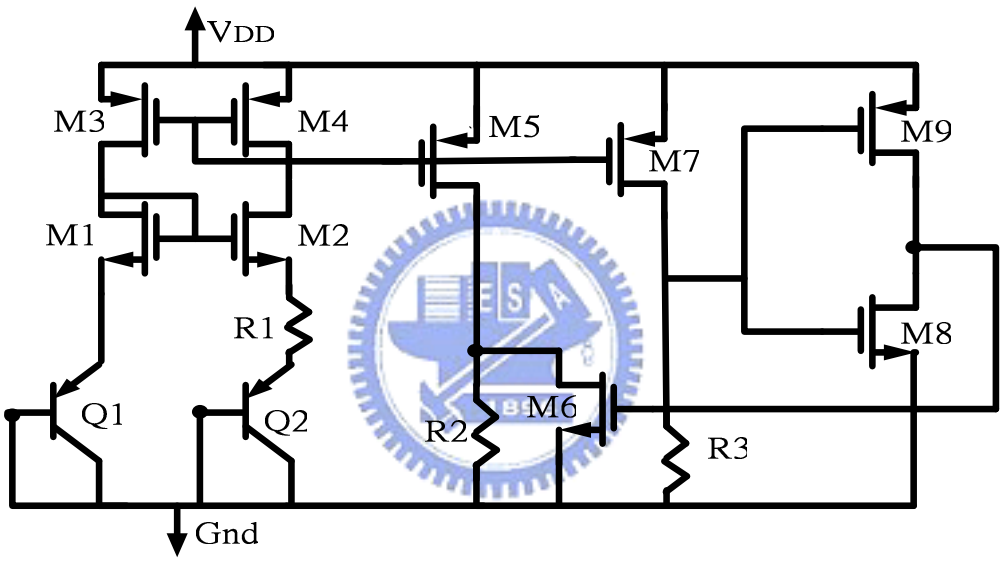

Figure 2.2.5 PTAT Circuit with Start-Up Circuit

In Figure 2.2.5, M5~M9 and R3 form a start-up circuit. When the current of M4 is zero, the gate voltage of M8 is zero. The drain voltage of M8 is V_{DD}, and M6 is on to force M5 to generate current. The PTAT circuit will move its operation region from zero current state region to normal operation one. However, adding start-up circuit will introduce a disadvantage which consumes some additional power in overall PTAT circuits, because M7-R3 branch of start-up circuit is always on. There is another start-up circuit which reduces the static power dissipation. In Figure 2.2.6, adding a capacitance starts up the PTAT circuit. When the current of M4 is zero, the supply noise will cause a signal path from V_{DD} to Gnd, and forces the circuit to enter normal operation region.

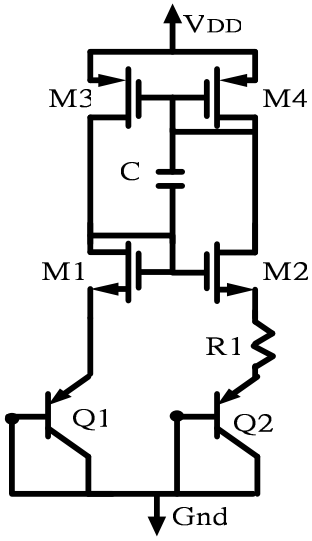

Figure 2.2.6 PTAT Circuit with Start-Up Circuit

The advantage of this start-up circuit is consuming no additional power, when the PTAT circuit enters normal operation region. It use only one capacitor, but the value of this capacitance must be large enough to ensure to establish signal path from V_{DD} and Gnd. The capacitor may have very large area. For improving this disadvantage, the capacitor can be replaced by a diode-connected NMOS. For a diode-connected NMOS, it serves capacitor as C_{gs}. In general, a MOS has smaller area than a resistor and better match. With lower and lower supply voltage, however, the PTAT in Figure 2.2.7 will fail to start up itself, because power supply may not provide enough start-up voltage. The V_{DD} must be obeyed:

$$V_{DD} \geq V_{GS3} + V_{GS5} + V_{GS2} + V_{EB1} \tag{2-10}$$

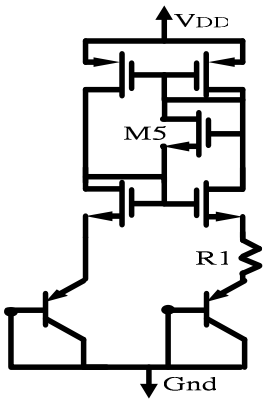

Figure 2.2.7 PTAT Circuit with Start-up Circuit

2.3 Bandgap Reference (BGR)

As described in previous section, BGR which generates a biasing signal independent of temperature and supply voltage is key elements in analog and mixed-mode circuit. To achieve the independence of temperature, a positive temperature coefficient (**TC**) signal and a negative one are both required to make the overall TC be equal to zero. After having been familiar with PTAT signal and EBJ voltage of BJTs, PTAT signal has positive TC and EBJ voltage has negative one. In the following sub-section, the two components are described to achieve BGR.

2.3.1 The Principle of Bandgap Reference

Conceptually, to achieve a BGR, it is necessary to accomplish one of the two possible functions shown in Figure 2.3.1.

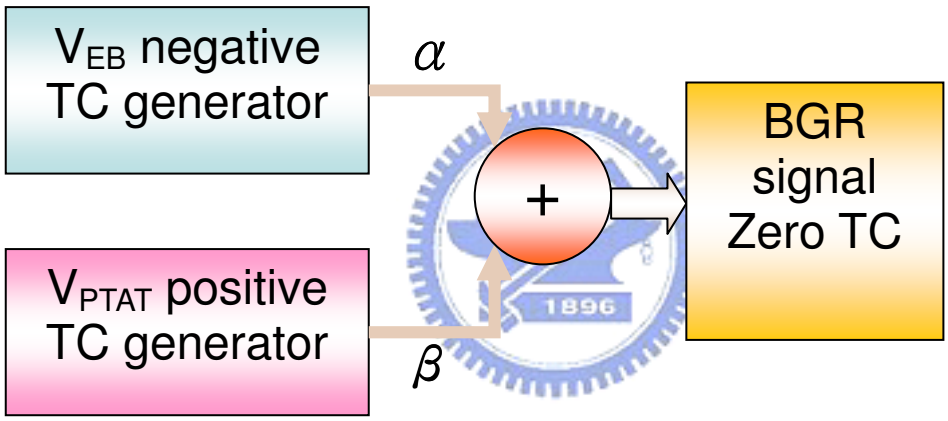

Figure 2.3.1 Block Diagram of Bandgap Reference

The first function is the signal generator of negative TC and the second one is the signal generator of positive temperature. By linear combination of these two signal, the TC of BGR signal could be zero.

For EBJ voltage of BJT, it is negative TC from Eq.2-8, but suffers from the high order nonlinearity of temperature. For PTAT signal, the difference between two terminals of BJT EBJ voltage, it has positive TC from Eq.2-9 with exact linearity.

From Eq.2-8, Eq.2-9 and Figure 2.3.1, the BGR signal is derived as following:

$$V_{bg}(T) = \alpha U_T + \beta V_{EB}(T) \tag{2-11}$$

$$\approx \alpha \frac{kT}{q} \ln(\frac{M}{N}) + \beta \times [V_{G0} + A_1 T + A_2 T^2 + A_3 T^3]$$

$$\approx \beta V_{G0} + [\alpha \frac{k}{q} \ln(\frac{M}{N}) + \beta A_1] \times T + \beta A_2 T^2 + \beta A_3 T^3 \quad (2\text{-}12)$$

By adjusting α and β to cancel the one order term of absolute temperature, and Eq.2-13 can be obtained.

$$V_{bg}(T) \approx \beta V_{G0} + \beta A_2 T^2 + \beta A_3 T^3 \quad (2\text{-}13)$$

Because βA_2 and βA_3 are far less than unity, then Eq.2-14 is obtained.

$$V_{bg}(T) \approx \beta V_{G0} \quad (2\text{-}14)$$

so, from Eq.2-14, $V_{bg}(T)$ is almost temperature independent signal. BGR circuit can be implemented according to this equation.

2.3.2 Bandgap Reference Circuit Architecture

In section 2.3.1, the principles of BGR have been introduced. In this section, our block diagram of BGR will be realized to transistor level circuits. Because CMOS technology is more popular and lower cost, MOS transistor is used to achieve self-biasing and Op-Amp in our design. In this section, three circuit architectures of BGR are introduced and shown in Figure 2.3.2 to Figure 2.3.4. The BJTs which appear in these Figures are parasitic substrate vertical BJT and compatible to CMOS technology. In Figure.2.3.2, the BGR is achieved by self-biasing circuit. M1~M4 are assumed to be identical, then

$$I_{Q1} = I_{Q2} = I_Q \quad \text{and} \quad V_{S2} = V_{S1}$$

$$I_Q R_1 + V_{EB1} = I_Q (R_2 + R_3) + V_{EB2}$$

$$I_Q = \frac{k \ln N}{q(R_2 + R_3 - R_1)} T = B_1 T \quad (2\text{-}15)$$

$$V_{bg}(T) = I_Q (R_2 + R_3) + V_{EB2}$$

$$\approx V_{G0} + [A_1 + B_1] \times T + A_2 T^2 + A_3 T^3 \quad (2\text{-}16)$$

From Eq.2-8 and Eq.2-15, Eq.2-16 can be obtained. Because A_1 is a negative real number and B_1 is positive one, $A_1 + B_1$ can be adjusted to be equal to zero. Eq.2-16 will be as:

$$V_{bg}(T) \approx V_{G0} + A_2 T^2 + A_3 T^3 \approx V_{G0} \quad (2\text{-}17)$$

Because A_2 and A_3 are far less than unity, the circuit in Figure 2.3.2 can be a BGR.

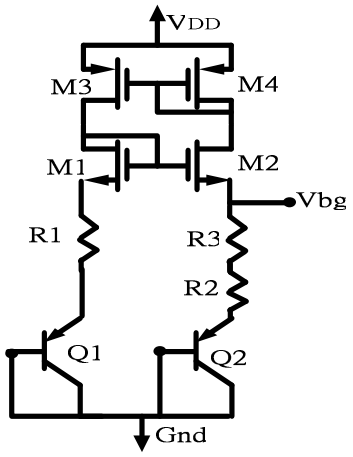

Figure 2.3.2 Bandgap Reference Circuit (I)

In Figure.2.3.3, the BGR is achieved by three resistors and one operational amplifier. If the Op-Amp is ideal and the Emitter-Base area ratio of M2 to M1 is P, then

$$V_{G1} = V_{G2} \quad \text{and} \quad I_{Q2} = \frac{kT}{qR_2}\ln P$$

Eq.2.8 can be obtained as following:

$$V_{bg} = (R_2 + R_3)I_{Q2} + V_{EB2}$$

$$\approx V_{G0} + [\frac{k}{q}(1 + \frac{R_3}{R_2})(\ln P) + A_1]T \qquad (2\text{-}18)$$

V_{bg} is a BGR voltage from Eq.2-18, if $\frac{k}{q}(1 + \frac{R_3}{R_2})(\ln P) + A_1$ is zero.

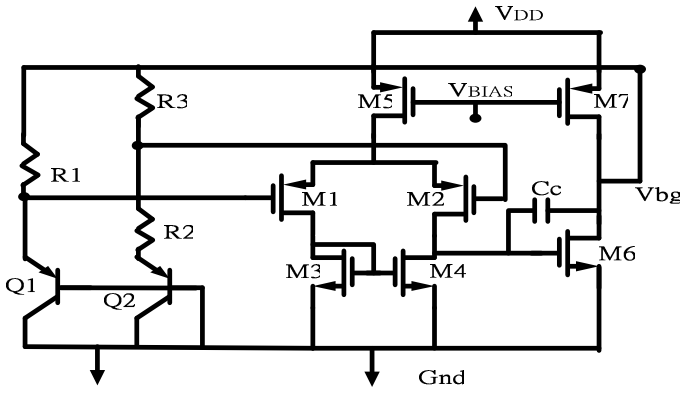

Figure 2.3.3 Bandgap Reference Circuit (II)

In Figure 2.3.3, three resistors are used in this BGR, but resistors usually are far larger area than MOS transistors and more difficult to match in IC technology. In

Figure 2.3.4, two transistors are replaced by two transistors so that the area of overall circuit can be reduced. If the Op-Amp is ideal and M1 and M2 are identical, the derivation of V_{bg} is as following:

$$I_{Q2} = \frac{kT}{qR} \ln P$$

$$V_{bg} = R_2 I_{Q2} + V_{EB2}$$

$$\approx V_{G0} + [\frac{k}{q} \ln P + A_1]T \qquad (2\text{-}19)$$

V_{bg} is a BGR voltage from Eq.2-18, if adjusting $\frac{k}{q} \ln P + A_1$ to be zero.

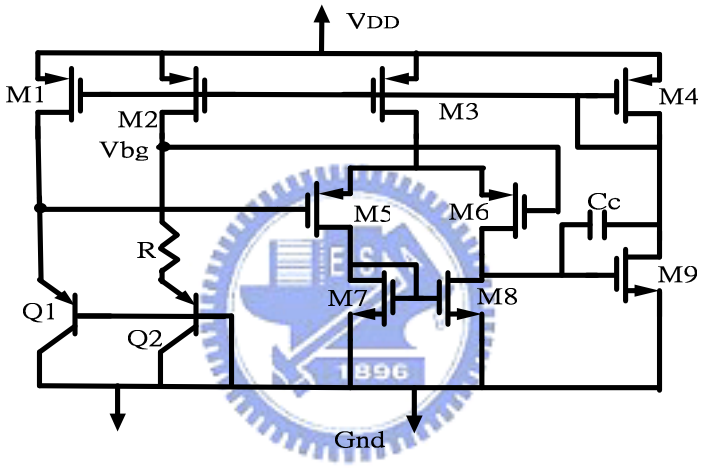

Figure 2.3.4 Bandgap Reference Circuit (III)

2.4 Non-Ideal Effect of PTAT & BGR and Their Cancellation Techniques

In previous section, the principles of PTAT and BGR are introduced and all conditions in of these circuits are assumed to be ideal, but there are two non-ideal effects including offset vltage due to device mismatches and the non-linearity of EBJs.

In this section, these non-ideal effects are described and the methods for reducing them are also introduced.

2.4.1 Offset Voltage Due to Device Mismatches

Our study of PTAT circuits in previous sections has mostly assumed the circuits are perfectly symmetric, in other words, the two sides exhibit identical properties and

bias currents. In reality, however, nominally-identical devices suffer from a finite mismatch due to uncertainties in each step of manufacturing process. Also, MOS devices exhibit threshold voltage mismatch because from Eq.2-15:

$$V_{TH} = \Phi_{MS} + 2\Phi_F + \frac{Q_{dep}}{C_{ox}} \tag{2-15}$$

where Φ_{MS} is the difference between the work function of the poly-silicon gate and the silicon substrate, $\Phi_F = \frac{kT}{q}\ln\frac{N_{sub}}{n_i}$, N_{sub} is the doping concentration of the substrate, Q_{dep} is the charge in the depletion region, and C_{ox} is gate oxide capacitance per unit area, so V_{TH} is a function of the doping levels in the channel and the gate, and these level vary randomly from one device to another.

For analyzing the effect of device mismatches, we observe that mismatches between μ, C_{ox}, W, L, and V_{TH} result in mismatches between drain current (for given V_{GS}) or gate-source voltage (for given drain current) . Intuitively, we expect that as W and L increase, their relative mismatches, $\frac{\Delta W}{W}$ and $\frac{\Delta L}{L}$, respectively decrease, so Large devices suffer from less mismatches.

For mismatches between μ, C_{ox}, W, L, and V_{TH} will result in DC offset in Op-Amps and self-biasing circuit. We first discuss the offset voltage of self-biasing shown in Figure 2.4.1 result from M1~M4 mismatches. For I_{Q1} must be equal to I_{Q2} and eliminating channel length effect, it can be assumed that

$$V_{SD3} = V_{SD4} = V_{SG4} \quad \text{and} \quad V_{DS2} = V_{DS1} = V_{GS1}$$

$$V_{TH3} = V_{TH34} + \frac{1}{2}\Delta V_{TH34} \quad \text{and} \quad V_{TH4} = V_{TH34} - \frac{1}{2}\Delta V_{TH34}$$

$$V_{TH1} = V_{TH12} + \frac{1}{2}\Delta V_{TH12} \quad \text{and} \quad V_{TH2} = V_{TH12} - \frac{1}{2}\Delta V_{TH12}$$

$$(\frac{W_1}{L_1}) = (\frac{W_{12}}{L_{12}}) + \frac{1}{2}\Delta(\frac{W_{12}}{L_{12}}) \quad \text{and} \quad (\frac{W_2}{L_2}) = (\frac{W_{12}}{L_{12}}) - \frac{1}{2}\Delta(\frac{W_{12}}{L_{12}})$$

$$(\frac{W_3}{L_3}) = (\frac{W_{34}}{L_{34}}) + \frac{1}{2}\Delta(\frac{W_{34}}{L_{34}}) \quad \text{and} \quad (\frac{W_4}{L_4}) = (\frac{W_{34}}{L_{34}}) - \frac{1}{2}\Delta(\frac{W_{34}}{L_{34}})$$

$$V_{OV3} + V_{OV1} + V_{TH3} + V_{TH1} = V_{OV4} + V_{OV2} + V_{TH4} + V_{TH2} + V_{OS}$$

then

$$V_{OS} = V_{OV3} - V_{OV4} + V_{OV1} - V_{OV2} + V_{TH3} - V_{TH4} + V_{TH1} - V_{TH2}$$

$$= \Delta V_{TH12} + \Delta V_{TH34} + \sqrt{\frac{2I_Q}{K_P(\frac{W_3}{L_3})}} - \sqrt{\frac{2I_Q}{K_P(\frac{W_4}{L_4})}} + \sqrt{\frac{2I_Q}{K_N(\frac{W_1}{L_1})}} - \sqrt{\frac{2I_Q}{K_N(\frac{W_2}{L_2})}}$$

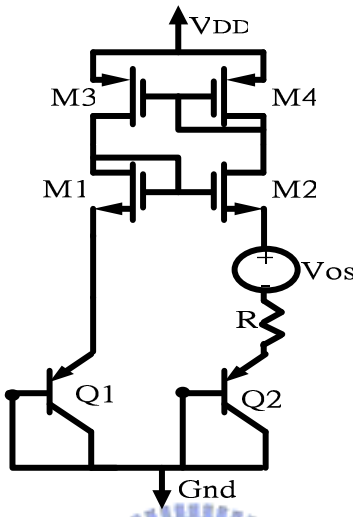

Figure 2.4.1 Offset Voltage in Self-Biasing Circuit by Mismatches

Assume these MOSFETs are square law devices, then

$$V_{OS} \approx [1 + \frac{g_{m12}}{g_{m34}}]\Delta V_{TH12} + [1 + \frac{g_{m34}}{g_{m12}}]\Delta V_{TH34} + \frac{V_{OV12} + V_{OV34}}{2}[\frac{\Delta(\frac{W_{12}}{L_{12}})}{(\frac{W_{12}}{L_{12}})} + \frac{\Delta(\frac{W_{34}}{L_{34}})}{(\frac{W_{34}}{L_{34}})}] \quad (2\text{-}16)$$

Second, the offset voltage of Op-Amp is discussed in Figure 2.4.2. The offset voltage of an Op-Amp is composed of two components:

(1) Systematic offset.

(2) Random offset.

The systematic offset voltage is caused by unequal drain voltage of M3 and M4, and it can be resolved by transistor sizing as following:

$$\frac{(\frac{W_3}{L_3})}{(\frac{W_6}{L_6})} = \frac{(\frac{W_4}{L_4})}{(\frac{W_6}{L_6})} = \frac{(\frac{W_5}{L_5})}{2(\frac{W_7}{L_7})} \quad (2\text{-}17)$$

The random offset voltage is caused by mismatches of transistors, and can be reduced by choosing longer channel devices. For analyzing it, some condition must be assumed as following:

$$V_{SD3} = V_{SD4} = V_{SG4} \quad \text{and} \quad V_{DS2} = V_{DS1} = V_{GS1}$$

$$V_{TH3} = V_{TH34} + \frac{1}{2}\Delta V_{TH34} \quad \text{and} \quad V_{TH4} = V_{TH34} - \frac{1}{2}\Delta V_{TH34}$$

$$V_{TH1} = V_{TH12} + \frac{1}{2}\Delta V_{TH12} \quad \text{and} \quad V_{TH2} = V_{TH12} - \frac{1}{2}\Delta V_{TH12}$$

$$(\frac{W_1}{L_1}) = (\frac{W_{12}}{L_{12}}) + \frac{1}{2}\Delta(\frac{W_{12}}{L_{12}}) \quad \text{and} \quad (\frac{W_2}{L_2}) = (\frac{W_{12}}{L_{12}}) - \frac{1}{2}\Delta(\frac{W_{12}}{L_{12}})$$

$$(\frac{W_3}{L_3}) = (\frac{W_{34}}{L_{34}}) + \frac{1}{2}\Delta(\frac{W_{34}}{L_{34}}) \quad \text{and} \quad (\frac{W_4}{L_4}) = (\frac{W_{34}}{L_{34}}) - \frac{1}{2}\Delta(\frac{W_{34}}{L_{34}})$$

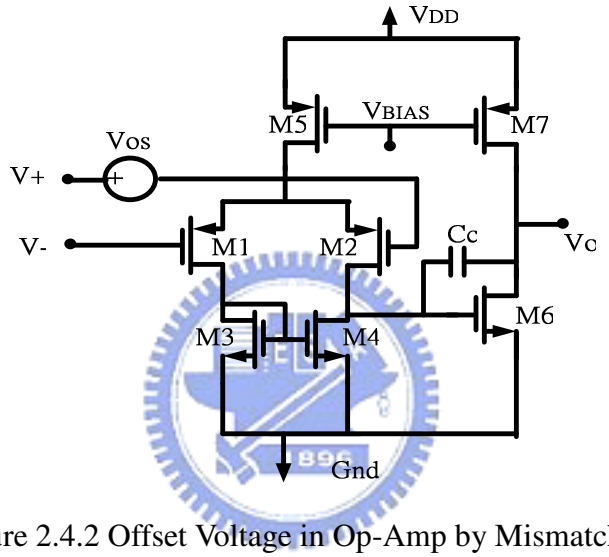

Figure 2.4.2 Offset Voltage in Op-Amp by Mismatches

$$V_{OS} \equiv V_{SG1} - V_{SG2}\,|_{V_{D3} = V_{D4}}$$

$$= V_{TH1} - V_{TH2} + \sqrt{\frac{2I_{D1}}{K_P(\frac{W_1}{L_1})}} - \sqrt{\frac{2I_{D2}}{K_P(\frac{W_2}{L_2})}} \qquad (2\text{-}18)$$

Because $\sqrt{I_{D1}} = \sqrt{\frac{K_N}{2(\frac{W_3}{L_3})}}(V_{OV3} + V_{TH3})$ and $\sqrt{I_{D2}} = \sqrt{\frac{K_N}{2(\frac{W_4}{L_4})}}(V_{OV4} + V_{TH4})$

Then Eq.2-18 will be as following:

$$V_{OS} \approx \Delta V_{TH12} + \frac{V_{OV12}}{2}[\frac{\Delta(\frac{W_{12}}{L_{12}})}{(\frac{W_{12}}{L_{12}})} + \frac{\Delta(\frac{W_{34}}{L_{34}})}{(\frac{W_{34}}{L_{34}})}] + \frac{g_{m34}}{g_{m12}}V_{TH34} \qquad (2\text{-}19)$$

From Eq.2-16 and Eq.2-18, the approximant equation of offset voltage is derived.

For reducing the offset voltage, larger devices can be chosen or layout carefully.

2.4.2 The Non-Linearity of EBJ Voltage in BJTs

In contrast to the PTAT voltage, which is highly linear function of temperature, the signal related to the EBJ voltage shows a slight non-linearity. This non-linearity has already discussed in Eq.2-8 and plots it in Figure 2.4.3 as following:

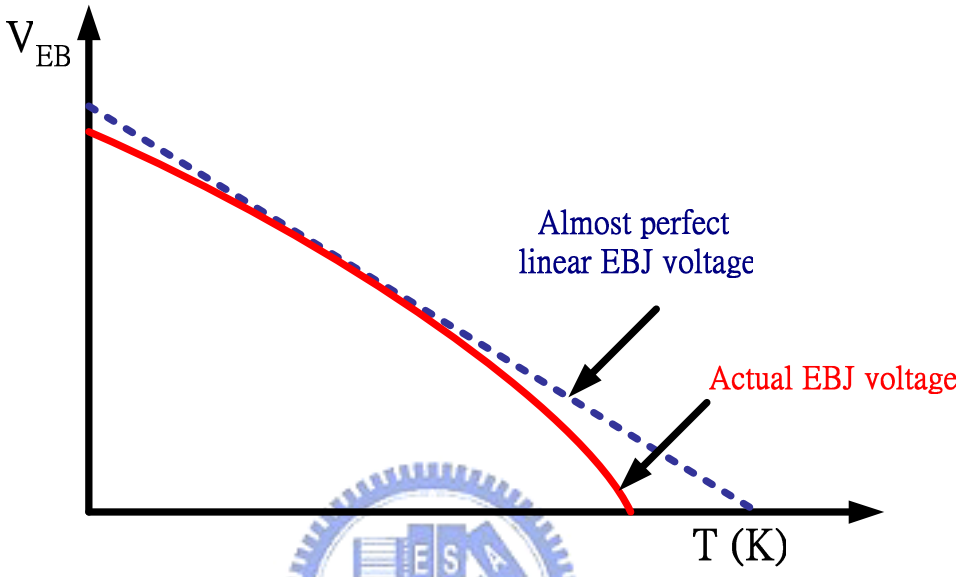

Figure 2.4.3 The EBJ Voltage versus Temperature

From Eq.2-6, it can be rewriten as following

$$V_{EB}(T) = V'_{G0} + AT + BT\ln T \tag{2-20}$$

$$= V_{G0} + A_1 T + \sum_{i=2}^{\infty} A_i T^i \tag{2-21}$$

Where A and B are negative number, and A_i is very small.

2.4.3 Curvature Corrected Techniques

Curvature correction is a technique which makes circuit to generate $T\ln T$ term to cancel $BT\ln T$ term in Eq.2-20 or to generate T^i term to cancel A_i in Eq.2.21. It is more difficult to achieve in circuit devices for the first method, so the second method is used. In Eq.2.21, the second order term of temperature is only cancelled. After canceling the second order term, more stable TC BGR voltage can be obtained as Figure 2.4.4.

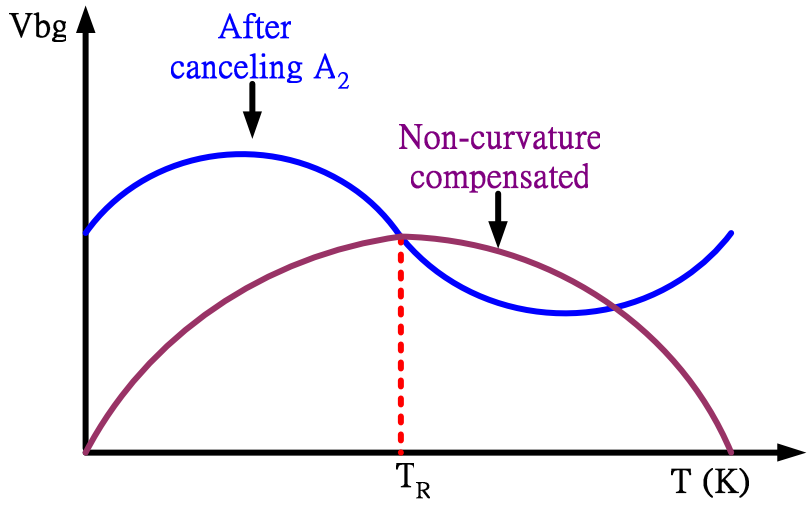

Figure 2.4.4 Curvature Correction versus Non-Curvature Correction

2.4.4 Offset Cancellation Technique

As mentioned in section 2.4.1, offset voltage results from devices mismatches in Op-Amps and self-baising circuits. The offset voltage reduces the accuracy of PTAT and BGR voltage. At low frequencies, however, flicker noise also degrades the accuracy of the reference signal, so offset cancellation techniques is required to overcome these problems. One of the offset cancellation techniques is chopper technique suited, because it is used to process continuous time signals. The block diagram of chopper circuit is described as Figure 2.4.5

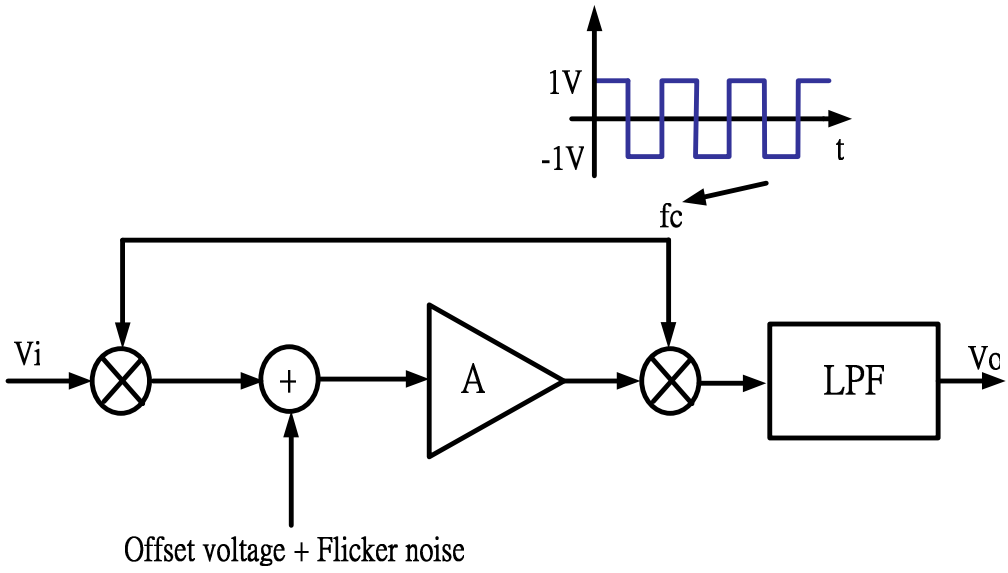

Figure 2.4.5 The Block Diagram of Chopper Circuit

Offset voltage and low frequency noise of Op-Amp will reduce accuracy of PTAT and BGR, so chopper circuit will be used to combat the effect of them. A chopper Op-Amp is presented in Figure 2.4.6, and there are two non-overlapped clock waveforms Φ1 and Φ2. When Φ1 is high and Φ2 is low, the Op-Amp is operated in normal mode. When Φ1 is low and Φ2 is high, the Op-Amp is operated in chopper mode and the Op-Amp can be equivalent to multiplying -1 at the input node and output node. its spectrum analysis is shown in Figure 2.4.7.

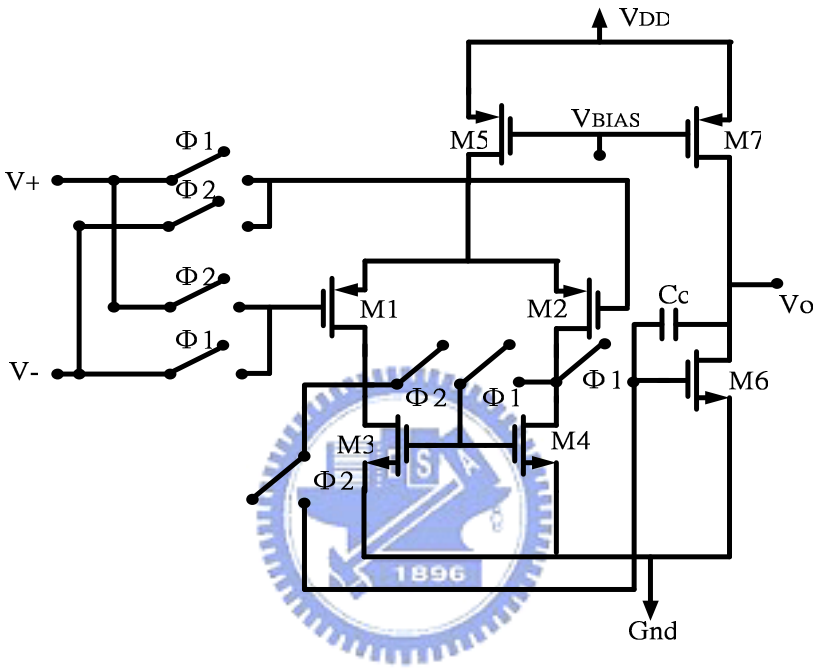

Figure 2.4.6 Chopper Op-Amp

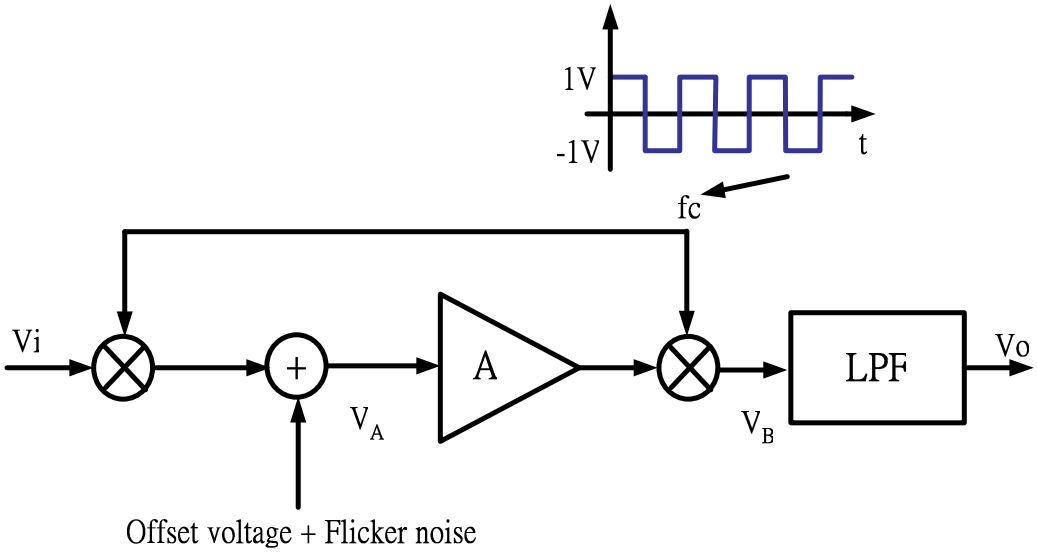

Figure 2.4.7 (a) The Block Diagrams of Chopper Op-Amp

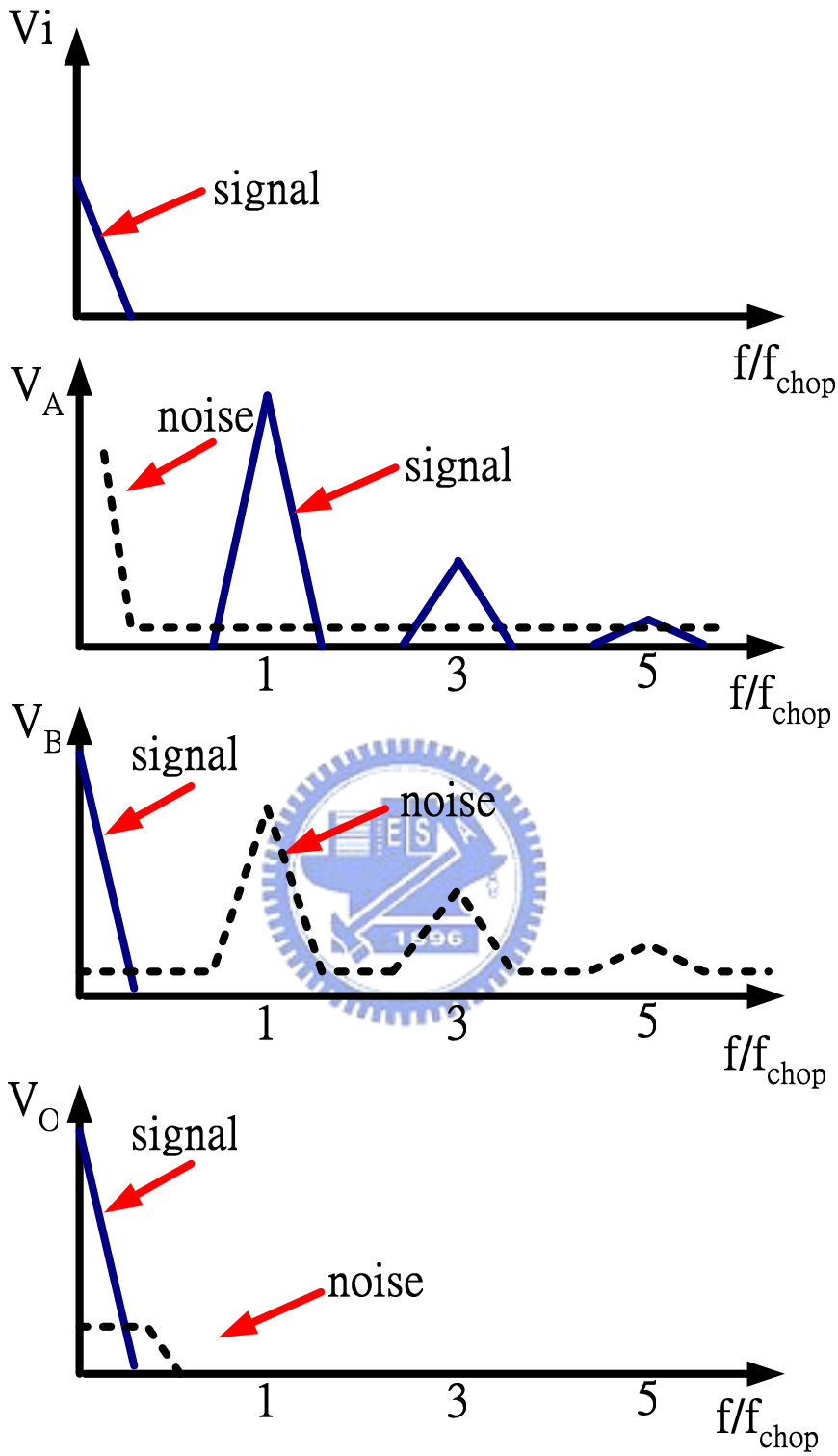

Figure 2.4.7 (b) Spectrum Analysis of Chopper Op-Amp

From Figure 2.4.7, the chopper technique modulates offset voltage and flicker noise to high frequency band and filters it by low pass filter, so the chopper technique can reduce offset voltage and flicker noise.

The offset voltage and high order temperature dependence of EBJ voltage are introduced, and the circuits which reduce their effect are also presented. When designing PTAT and BGR, these non-ideal effects must be taken care to increase the performance of PTAT and BGR.

2.5 Summary

In this chapter, the principles of PTAT and BGR have been shown and several circuit architectures and mathematics description of them are presented. However, PTAT and BGR suffer from nonlinearities due to the EBJ voltage and offset voltage, and the non-ideal effects can be reduced by curvature correction and chopper technique.

In next chapter, PTAT and BGR of our design is proposed and designed to improve their performance in some aspects and all the details will be described later. Based on these backgrounds, it is quite useful for us to get guidelines in our proposed design.

Chapter 3 Proposed Design

In Chapter 2, backgrounds of PTAT and BGR have been described. In this chapter, our new design of PTAT and BGR will be proposed. The main advantage of our proposed design is replacing start-up circuit by POR circuit to make power consumption of start-up to be zero, and the secondary advantage is realizing our design in deep sub-micron process and adding curvature circuit to improve the accuracy of BGR.

This chapter will propose our new design, and the order of sections arranges as following: First, the disadvantages of conventional PTAT and BGR in deep sub-micron processes are discussed and their operations are also explained. Second, our new design is proposed to overcome the problems caused by deep sub-micron processes. Third, the design considerations of our design are explained. Finally, the summary of our design is presented.

3.1 Design Issues of PTAT & BGR Circuits

As process technologies are scaled down into the deep sub-micron eras, conventional BGR and PTAT are not suited for deep sub-micron processes.

First, because the demand for battery operated portable increases, conventional PTAT and BGR circuits are not suited for low power requirement. As described in section 2.2.3, start-up circuits of PTAT and BGR in non-zero current state will still consume additional power. The additional power consumed by start-up circuits will become a serious bottleneck in low power systems, as the processes are scaled down to nanometer scale.

Second, the older CMOS devices followed the “square-law” MOSFET model, but the newer devices are not. An older MOSFET that can be modeled well using the level 1 model yields simulation results that match hand-calculations and provides immediate feedback to the designer to know the operation of all transistors. The level 1 model can accurately model with $L_{\min} > 5\mu m$. However, the MOSFETs in deep sub-micron processes ($L_{\min} < 0.5\mu m$), the error of level 1 square-law model is generally above 100%, this appears that the analog circuit design will be more and more difficult in shorter channel technologies.

Third, the accuracy and stability of BGR signals are very important in ADC and they influence the output bit-steams of ADC, so a curvature correction circuit is necessary in BGR circuits to increase the accuracy of temperature sensor.

Finally, for PTAT and BGR in voltage mode, the addition and minus of voltage signals must use Op-Amps and self-biasing circuits (more transistors). This will increase the complexity of circuit architecture and waste power. But the addition and minus of current signals use only one transistor (switch) to achieve them, the complexity and area of the circuit will be reduced if the current output of PTAT and BGR is adopted in our proposed design .

For these reasons described above, new PTAT and BGR must be designed to solve these problems and be integrated with thermal-aware VLSI systems in deep sub-micron processes.

3.2 Circuit Architecture of Proposed Design

This section presents our proposed design, and consists three parts described as following:

3.2.1 Basic circuits of proposed PTAT and BGR

As described in section 2.2, two architecture of PTAT circuit are introduced as following:

(1) PTAT based on self-biasing circuit. (as Figure 2.2.2)

(2) PTAT based on operational amplifier. (as Figure 2.2.3)

The first architecture is simpler than second one, but from Eq.2.16 and Eq.2.19, the first one has larger offset voltage than the second one. The offset voltage is a very important error source in PTAT and BGR design, so the first architecture is chosen for our proposed design.

In section 2.3, three circuit architectures of BGR are introduced as following:

(1) BGR using self-biasing circuit. (as Figure 2.3.2)

(2) BGR using an Op-Amp and three resistors. (as Figure 2.3.3)

(3) BGR using an Op-Amp and one resistor. (as Figure 2.3.4)

The first architecture has large offset voltage from Eq.2-16 and Eq.2-19. The second one has three resistors and has larger area than the other ones, so the third one is chosen for our proposed design.

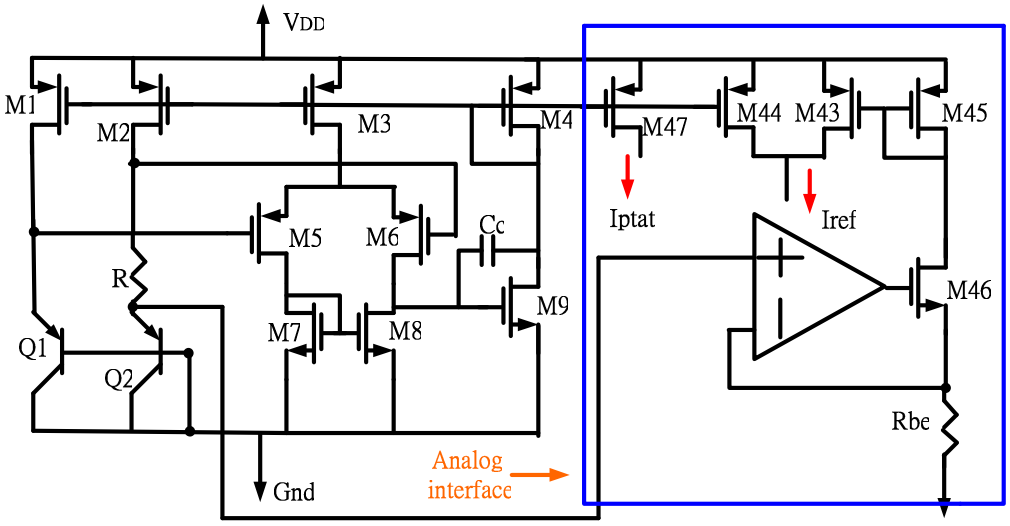

Figure 3.2.1 Proposed PTAT and BGR Architecture

Figure 3.2.1 shows the proposed circuit architecture of PTAT and BGR. The M3~M9 form an operation amplifier (Op-Amp). If the open loop gain of Op-Amp is large ,the drain voltage of M1 and M2 will be almost the same. The voltage drop cross R will be PTAT voltage.

The analog interface consists of M43~M47, an Op-Amp, and Rbe. The design of the Op-Amp is similar to M3~M9. The use of analog interface is to convert voltage signals of PTAT and BGR to current ones. First, the current cross R is PTAT current and mirrored to M47 as output PTAT current. Second, to generate a BGR current, a negative TC current must be first generated. For an EBJ voltage of BJTs, it is a negative TC voltage and connected to a source follower as input. Because the voltage gain of source follower is close to unity, an Op-Amp is added with negative feedback and the gain of source follower becomes to Eq.3-1

$$A_V \approx \frac{A \times g_{m48}}{A \times g_{m48} + g_{mb48} + \frac{1}{r_{o48}} + \frac{1}{R_{be}}} \approx 1 \qquad (3\text{-}1)$$

The voltage cross Rbe is negative TC voltage and the current cross Rbe is too. Now, the equation of the BGR current is derived as following:

$$I_{ref} = I_{43} + I_{44}$$

$$= \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} I_{45} + \frac{(\frac{W_{44}}{L_{44}})}{(\frac{W_2}{L_2})} I_2$$

$$= \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{V_{EB2}}{R_{be}} + \frac{(\frac{W_{44}}{L_{44}})}{(\frac{W_2}{L_2})} \frac{\Delta V_{EB}}{R} \tag{3.2}$$

By Eq.2-8 and Eq.2-9, rewrite Eq.3-2 as follow:

$$I_{ref} \approx \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{1}{R_{be}} (V_{G0} + \sum_{i=1}^{\infty} A_i T^i) + \frac{(\frac{W_{44}}{L_{44}})}{(\frac{W_2}{L_2})} \frac{kT}{qR} \ln M$$

$$= \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{V_{G0}}{R_{be}} + \{\frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{A_1}{R_{be}} + \frac{(\frac{W_{44}}{L_{44}})}{(\frac{W_2}{L_2})} \frac{k}{qR} \ln M\} \times T + \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{1}{R_{be}} \sum_{i=2}^{\infty} A_i T^i \tag{3.3}$$

Form Eq.3-3, the $(\frac{W_{43}}{L_{43}})$ and $(\frac{W_{44}}{L_{44}})$ can be adjusted to cancel the TC of the first order, so BGR current is obtained. Another advantage of this architecture is the output reference current can be programmable by adjusting the $(\frac{W_{45}}{L_{45}})$.

3.2.2 Power-on-Reset Circuits

As describe in section 2.2.3, BGRs have two stable operating states, given by zero current state and normal bandgap state. To avoid a stable off state, a start-up circuit is usually used. When start-up circuits are used, the main issue is that introducing additional power by some branches being on. The power consumption of start-up circuits should be zero when the BGR circuit is in normal operation. Another issue in start-up circuits is stability. When the next stage of closed loop circuit is start-up circuit, the potential for oscillation is greatly increased.

The POR circuit is shown in Figure 3.2.2, and the basic principle of POR circuit is the use of two RC circuits (Mpor1, Mpor3, C1 and C3) with different time constants. For our proposed design, the time constant of node A is smaller than the one of node B. when a battery is inserted into the system, node A approaches V_{DD} faster than node B. This voltage difference makes node C high and node D low.

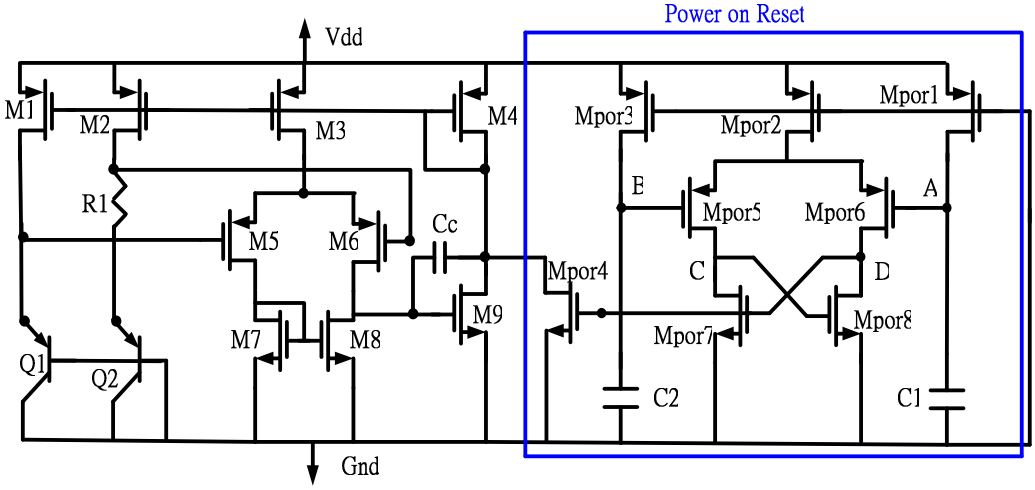

Figure 3.2.2 Power on reset circuit

This is accelerated by positive feedback transistors (Mpor7 and Mpor8) acting as a latch, and the output of the POR circuit feeds the gate of Mpor4. Because the node A has faster speed to charge its voltage to V_{DD} than node B, the voltage of the node D will be from high to low. In the process of discharging, the Mpor4 will start up the PTAT circuit. When the voltage of the node D discharge to zero, the POR circuit will be all off and consumes no power. By the way, it shows that the POR circuit is better power performance than start-up circuits.

Another advantage of this POR circuit is that the resistors are implemented by MOS operated in triode region. For this reason, the area of overall chip area can be reduced and the equivalent value of resistors are more accurate to make the RC time constant be precision.

3.2.3 Curvature Corrected Circuits

As mentioned in section 3.2.1, the first order TC of BGR current is adjusted to zero, but the high order TC terms of Iref still exist. These high order TC terms must be canceled to improve the linearity of BGR current. From Eq.3-3, the BGR current after canceling the first order TC can be obtained as following:

$$I_{ref} \approx \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})}\frac{V_{G0}}{R_{be}} + \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})}\frac{1}{R_{be}}\sum_{i=2}^{\infty} A_i T^i \qquad (3.4)$$

The goal of curvature correction is to minimize the terms of high order TC. There are three approaches of curvature corrected:

(1) Make the process parameter $4-n-m$ be zero. (See Eq.2-7 and 2-8)

(2) Generate a $T\ln T$ term to compensate reference signals. (See Eq.2-6)

(3) Approximate the $T\ln T$ by the T^2. (See Eq.3-4)

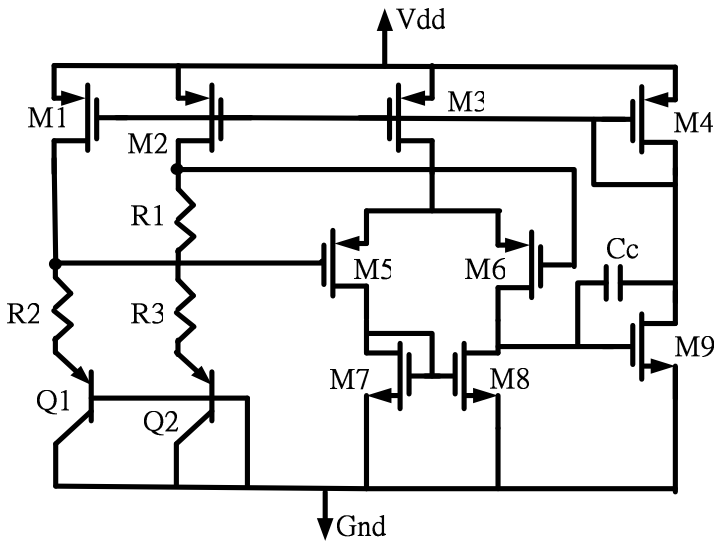

Figure 3.2.3 Curvature Corrected Circuit of V_{EB}

In the first method, the $4-n-m$ is strong dependent of process, it is impossible to make $4-n-m$ in every process be zero. In the second method, to implement the $T\ln T$ function in the circuit is very difficult. In consideration of circuit complexity and cost, the third approach is adopted. The circuit approach of implementing T^2 correction is adding a proportional to temperature resistance in the tail of BGR cells. Figure 3.2.3 is a curvature corrected circuit of our proposed design and is similar to the left part of Figure 3.2.1. The difference between them is adding two resistors in Figure 3.2.3.

The two resistors, R2 and R3, are proportional to absolute temperature and described as following:

$$R_2(T) = R_2(T_0) + TC_{R2} \times (T - T_0)$$
$$R_3(T) = R_3(T_0) + TC_{R3} \times (T - T_0) \qquad (3.5)$$

Where the TC_{Ri} is the TC of Ri, and T_0 is reference temperature.

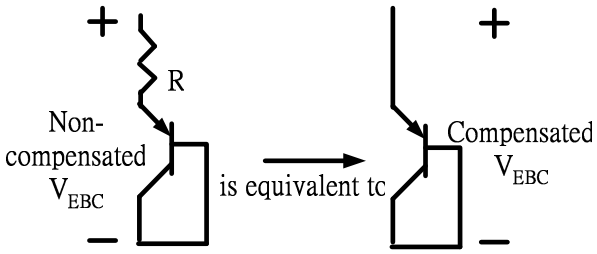

Figure 3.2.4 curvature corrected V_{EB}

From Eq.2-21 and Eq.3-5, the emitter current of BJT be I_{PTAT} and derive the corrected V_{EB} equation..

$$V_{EBC} = V_{G0} + A_1 T + \sum_{i=2}^{\infty} A_i T^i + IR$$

$$= V_{G0} + A_1 T + A_2 T^2 + \sum_{i=3}^{\infty} A_i T^i + I_{PTAT} \times [R + TC_R \times (T - T_0)]$$

$$= V_{G0} + A_1 T + A_2 T^2 + \sum_{i=3}^{\infty} A_i T^i + T \times \frac{k}{qR_1} \times [R + TC_R \times (T - T_0)]$$

$$= V_{G0} + (A_1 - \frac{kR}{qR_1} + TC_R T_0) \times T + (A_2 + \frac{k \times TC_R}{qR_1}) T^2 + \sum_{i=3}^{\infty} A_i T^i \quad (3.6)$$

For A_2 be negative and TC_R be positive, $A_2 + \frac{k}{qR_1} \times TC_R$ can be adjusted to be zero, then

$$V_{EBC} = V_{G0} + (A_1 - \frac{k}{q} \times \frac{R}{R_1} + TC_R T_0) \times T + \sum_{i=3}^{\infty} A_i T^i \quad (3.7)$$

Because the T^2 term is cancelled, the EBJ voltage is more linear, so the BGR signal is more stable. Because the V_{EB1} and V_{EB2} are both cancel the TC of second order term, the current cross R1 is still PTAT current. By this curvature correction, it will not affect other functionalities in our proposed design.

Now, the corrected Iref can be derived as following:

$$I_{ref} = I_{43} + I_{44}$$

$$= \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{V_{G0}}{R_{be}} + \{\frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{A_1}{R_{be}} + [\frac{(\frac{W_{44}}{L_{44}})}{(\frac{W_2}{L_2})} + \frac{R_2 - TC_{R2} T_0}{R_{be}}] \frac{k}{qR_1} \ln M\} \times T + \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{1}{R_{be}} (A_2 + mTC_{R2}) T^2 + \frac{(\frac{W_{43}}{L_{43}})}{(\frac{W_{45}}{L_{45}})} \frac{1}{R_{be}} \sum_{i=3}^{\infty} A_i T^i \quad (3.8)$$

From Eq.3-8, our BGR current can be more accuracy by adding two resistors

with temperature dependence.

After explaining the principle of our proposed design, design consideration of our design will be introduced.

3.3 Overall Circuits and Design Considerations

After the overall circuits of our design have been proposed, some consideration of our proposed design will be described in this section.

First, Op-Amp circuits are discussed. There are two Op-Amps in our proposed design, and the two stage Op-Amp is chosen here. In general, the open loop gain of the Op-Amp is proportional to $(g_m r_o)^2$, and it can be adjusted by these parameters (g_m and r_o) to increase open loop gain. A trick which must be taken care is that the minimum channel length of MOSFETs in our Op-Amp can be not chosen, because the r_o is proportional to channel length.

Another consideration of the Op-Amp is phase margin. In Figure 3.2.1, the next stage of Op-Amp1 is a common source (**CS**) amplifier. For Miller effect of CS amplifier, the first pole and second pole of the Op-Amp will be closer and more unstable. Because of this consideration, larger phase margin in our Op-Amp must be designed and chosen as 60 degree in our design. Our Op-Amp can be simplified to equivalent model as Figure 3.3.1 and Cc can be designed from the constrain of Op-Amp phase margin. Eq.3-9 is the equation between Cc and phase margin.

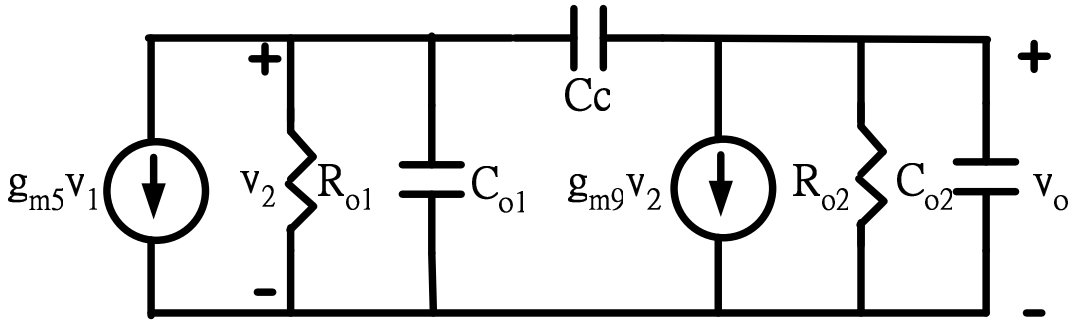

Figure 3.3.1 Equivalent Op-Amp model

$$Cc = \frac{1}{0.577} \times \frac{g_{m5}}{g_{m9}} \times (C_{o1} + C_{o2}) \tag{3.9}$$

Where C_{o1} and C_{o2} are the first stage and the second stage output capacitance.

In the BGR design, the offset voltage of Op-Amp is very critical error source. For reducing it as possible, the transistor sizing rule of Eq.2-17 must be obeyed. it can be rewriten as following:

$$\frac{(\frac{W_7}{L_7})}{(\frac{W_9}{L_9})} = \frac{(\frac{W_8}{L_8})}{(\frac{W_9}{L_9})} = \frac{(\frac{W_3}{L_3})}{2(\frac{W_4}{L_4})} \tag{3.10}$$

Increasing the emitter area ratio of Q1 and Q2 can also reduce the effect of offset voltage in Op-Amp, because the larger ratio of Q1 and Q2, the larger value of ΔV_{EB}.

Second, the design of curvature corrected circuit is discussed. In Figure 3.1.5, three resistors R1, R2 and R3 are used. For the value of R1, it should be independent of temperature. However, the materials of resistors in the process always have dependence of temperature, the lowest TC material is chosen for R1 and proportional to temperature resistance is chosen for R2 and R3,. In the analog interface of our design, Rbe, which also is independent of temperature is used. the same material of Rbe will be chosen as R1.

Finally, the POR circuit design is discussed. As described in previous section, the RC1 constant must be smaller than RC2. To achieve small value of RC1, the $(\frac{W_{POR1}}{L_{POR1}})$ is designed to be larger and operate Mpor1 in triode region to reduce the equivalent resistance of M_{POR1}. Because the behavior of the POR circuit is digital circuit, we can use the minimum channel length to increase the performance here. Another constrain of the POR circuits is the RC1 must be smaller than the half chopper interval to keep chopper circuits to work normally.

3.4 Summary

In this chapter, our new design of PTAT and BGR suit for deep sub-micron process are proposed and the output signal is current signals. Replacing the start-up circuits by POR circuits and a simple method of curvature correction are proposed, too. Using the POR circuits can reduce power consumption of overall circuits, and make our PTAT and BGR suit for low power or thermal-aware system under a tendency towards deep sub-micron process. Adding curvature corrected circuits can compensate the nonlinearities of EBJ voltage and increase the accuracy of BGR signals. Finally, some design consideration of our proposed design is explained to

achieve better performance. The overall circuits of our proposed design are shown in Figure 3.4.1.

In next chapter, simulation and experimental results will be shown. By reliable design flow and tool, our design is realized by TSMC 0.25um 1P5M technology. Measurement setup is also described. Finally, some discussion of experimental results is described.

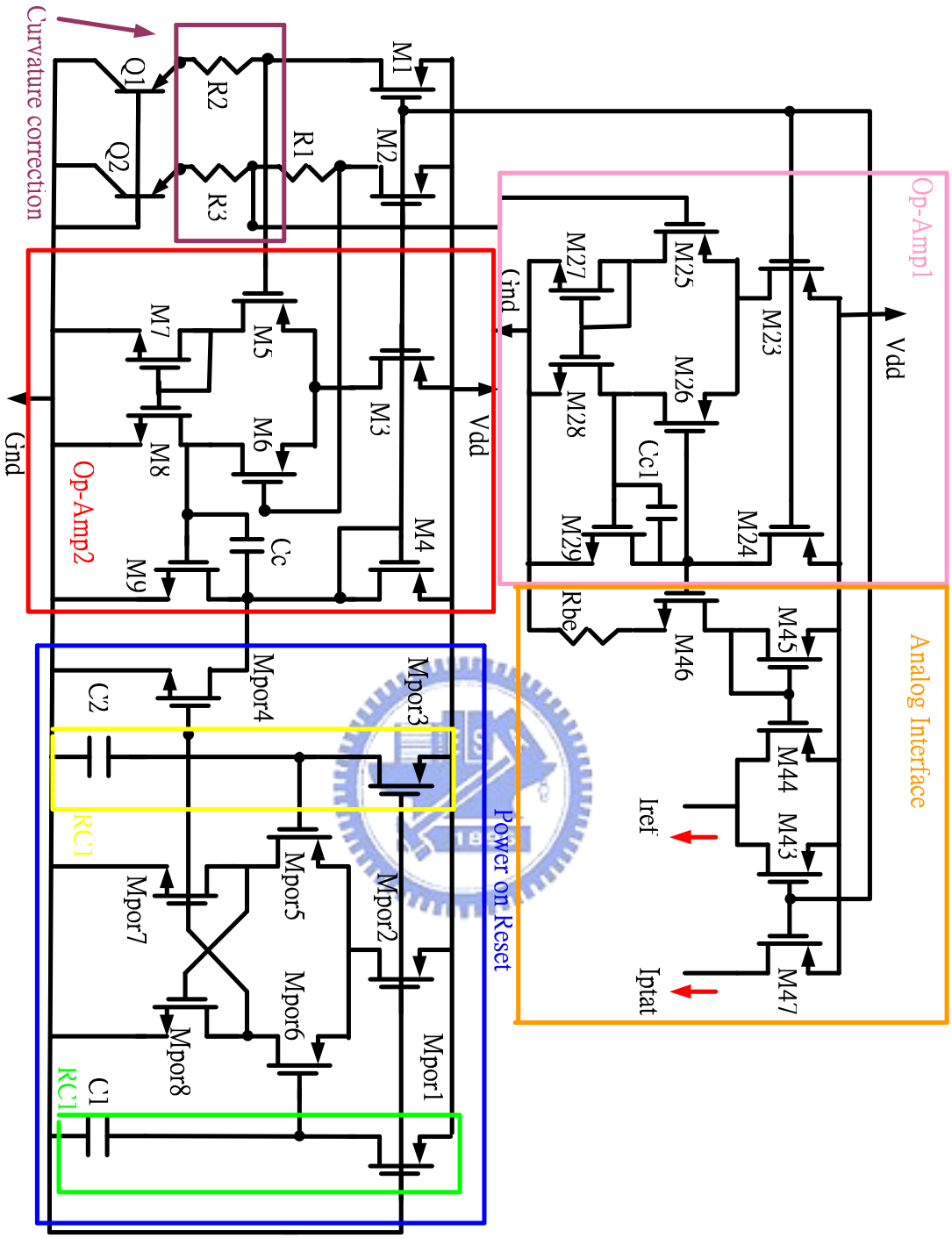

Figure 3.4.1 Overall circuits of proposed design

Chapter 4 Simulation and Experimental Results

In the previous chapter, our proposed designs have been presented and the design principles of them have been familiar with. In this chapter, the proposed design will be simulated and implemented by TSMC 0.25um 1P5M technology. The design flow used to achieve the proposed design is shown in Figure 4.1.1 can be followed. First, all functionalities of our circuits are simulated by Hspice. Second, adjusting the parameters in the proposed design optimizes performance. Third, convert the schematic of our design to layout. Finally, "Design Rule Check" (**DRC**) and "Layout VS Schematic" (**LVS)** must be checked to verify process design rule and check our layout to be the same as our schematic.

First, our Hspice simulation of all modules will be shown. It consists of PTAT, BGR, POR circuits, and curvature corrected circuits. Second, our layout of overall circuits and layout considerations is shown. Third, the measurement environment and testing setup is described. Finally, our experimental results will be shown.

4.1 SPICE simulation

Before simulating our design, all transistor sizing must be derived. All of them are described in Table 4.1.1. All transistor sizing can be derived by TSMC spice model, Kirchoff's Voltage Law (**KVL**), and Kirchoff's Voltage Law (**KCL**). It is somewhat difficult work to calculate all transistor sizing by spice model of BSIM3 Level 49, so a simpler model as level 2 can be used, then transistor size can be somewhat tuned. By the way, all transistors' size is obtained.

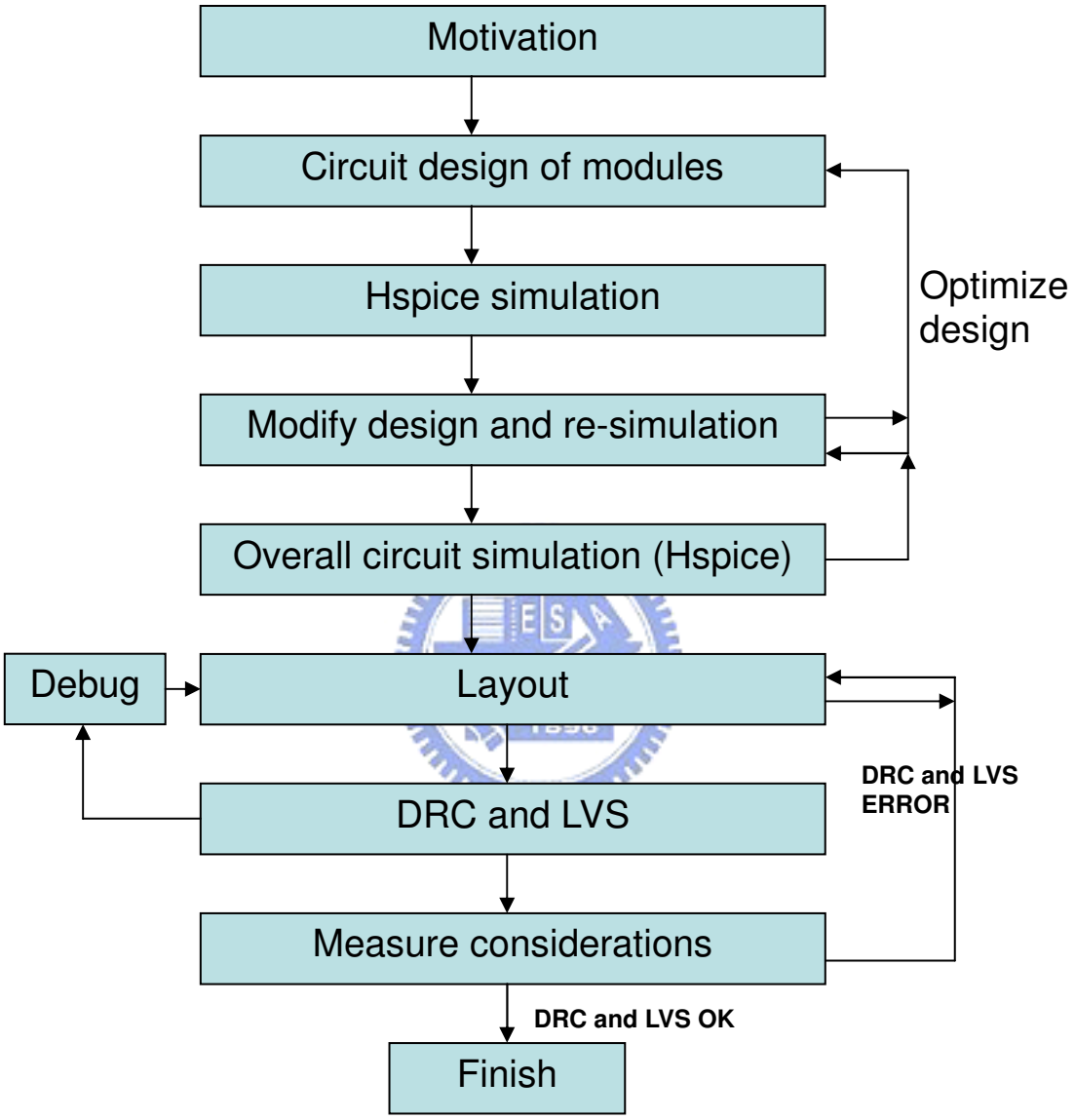

Figure 4.1.1 Chip Design Flow

MOSFET Transistors	Sizing (W/L)
M1, M2	2
M3, M4, M23, M24	2
M5, M6, M25, M26	8
M7, M8, M27, M28	2
M9, M29	4
M43	12.5
M44	10
M45	8
M46	2
M47	4
Mpor1, Mpor2	16
Mpor3	2
Mpor4	4
Mpor5, Mpor6	8
Mpor7, Mpor8	2

Table 4.1.1(a) MOSFET sizing

PNP Bipolar junction transistors	Emitter area
Q1	$25\mu m^2$
Q2	$25\mu m^2 \times 8$

Table 4.1.1(b) BJT sizing

Resistors	value
R1	4K (low TC)
R2	90 (high TC)
R3	90 (high TC)
R4	7K (low TC)

Table 4.1.1(c) Resistor sizing

4.1.1 Op-Amp Simulation

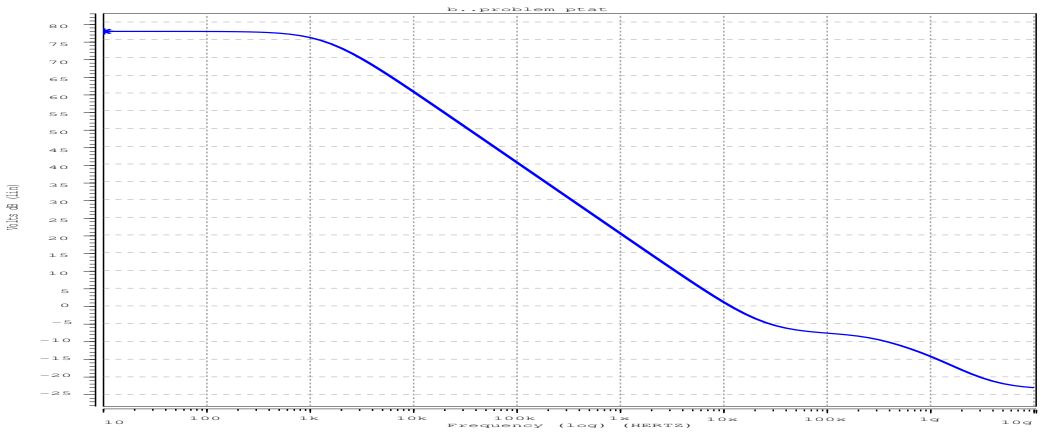

Figure 4.1.2 Op-Amp Open loop Gain

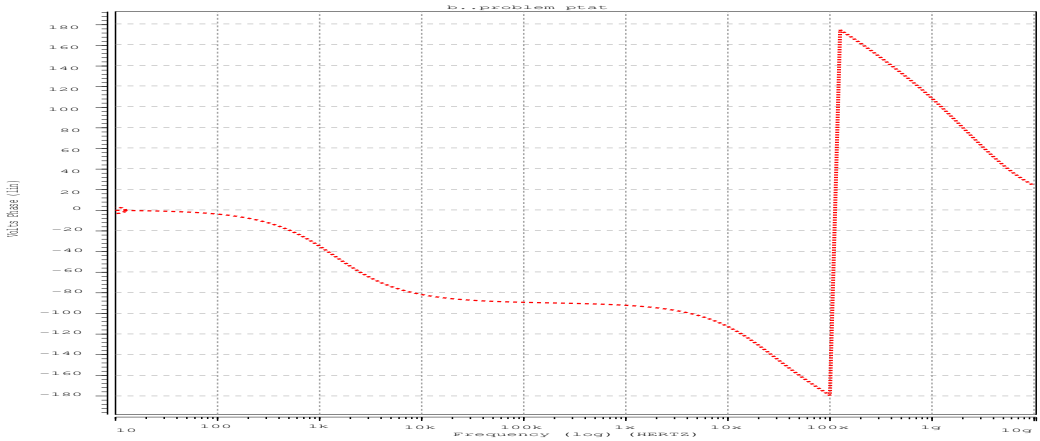

Figure 4.1.3 Op-Amp Phase Response

Our Op-Amp simulation is described in Figure 4.1.2 and Figure 4.1.3 Figure 4.1.2 show open loop gain of Op-Amp, and the open loop gain is around 78 dB. Figure 4.1.1 shows the phase response of Op-Amp, and the phase margin is around 60^{o}. In general, to achieve the virtual short circuit of the input nodes, the open loop gain needs at least 60dB. For our proposed design, the open loop gain is large enough to achieve virtual short circuit at two input nodes. For stability, it have been explained how to choose phase margin as 60^{o} in section 3.3. The 60^{o} phase margin of our Op-Amp is large enough to ensure our overall systems to be stable.

4.1.2 Basic PTAT and BGR Current Simulation

After ensuring the Op-Amp to satisfy our requirements, the simulation of basic PTAT and BGR shown in Figure 3.2.1 are presented.

Figure 4.1.4 shows the basic PTAT current and reference temperature current. The PTAT current is the drain current of M47, and the reference temperature current is regression analysis of PTAT current. The range of PTAT current is over 23.4uA to 24.8uA. To satisfy our specification of temperature error, the error of PTAT current must be known. By subtract PTAT current from reference temperature current, the PTAT current error can be approximately estimated.

Figure 4.1.5 shows the approximation error of PTAT current, the range of temperature error is over -1^{o}C to 1^{o}C. The error sources of PTAT current consist of nonzero TC of resistors and nonzero offset voltage. In Figure 4.1.4, there is an assumption that the transistors in the PTAT circuit are all matched. The temperature error of simulation is caused by nonzero TC of resistors, because the resistors all have temperature dependence in the IC processes.

Figure 4.1.6 shows the simulation of basic BGR current, and the range of current is over 112.43uA to 112.505uA. From Eq. 3-3, it shows that the output reference current is inverse proportional to R_{be}. Unfortunately, the R_{be} has nonzero TC to introduce the additional error of reference current. The material of R_{be} is P+ poly without silicide, and the TC of this material is 764ppm/K. The TC of this BGR current is around 30ppm/^{o}C over 25^{o}C to 125^{o}C, because the resistance model of the process ensures accuracy over this range.

To find the minimum supply voltage of the BGR current, Figure 4.1.7 shows the output reference current with the supply voltage varied from 0V to 3.3V. The simulation result shows that the minimum supply voltage of the proposed BGR current is 2.3V. If the supply voltage is lower than 2.3V, the BGR current will not normally work.

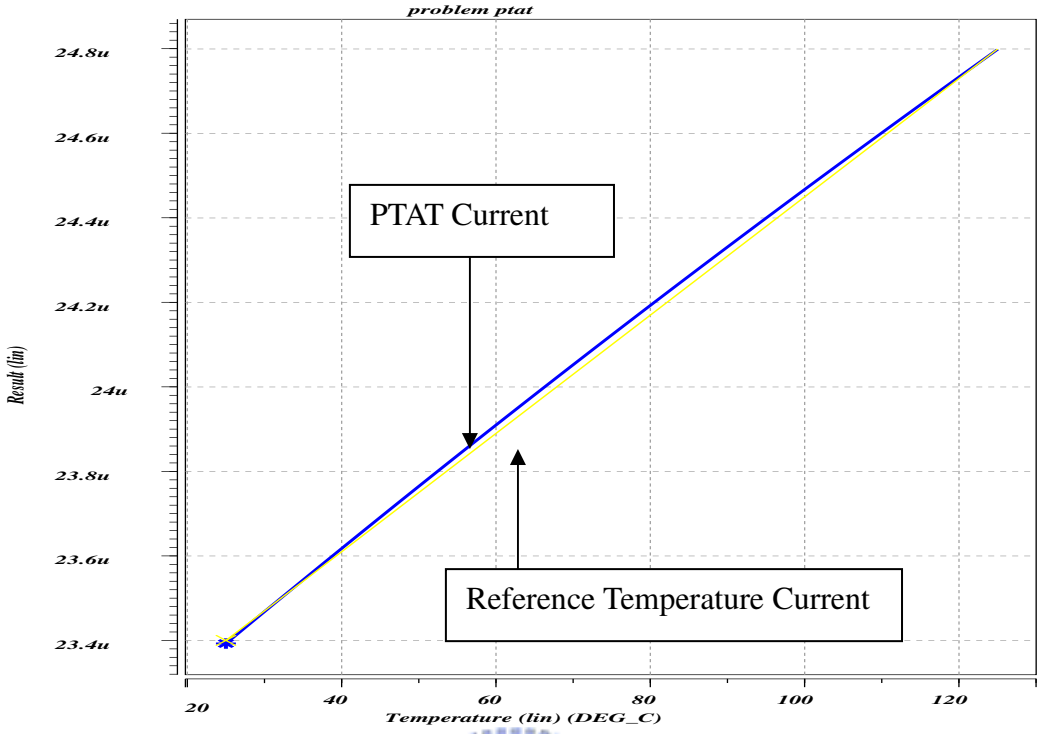

Figure 4.1.4 PTAT Current versus Reference Temperature Current

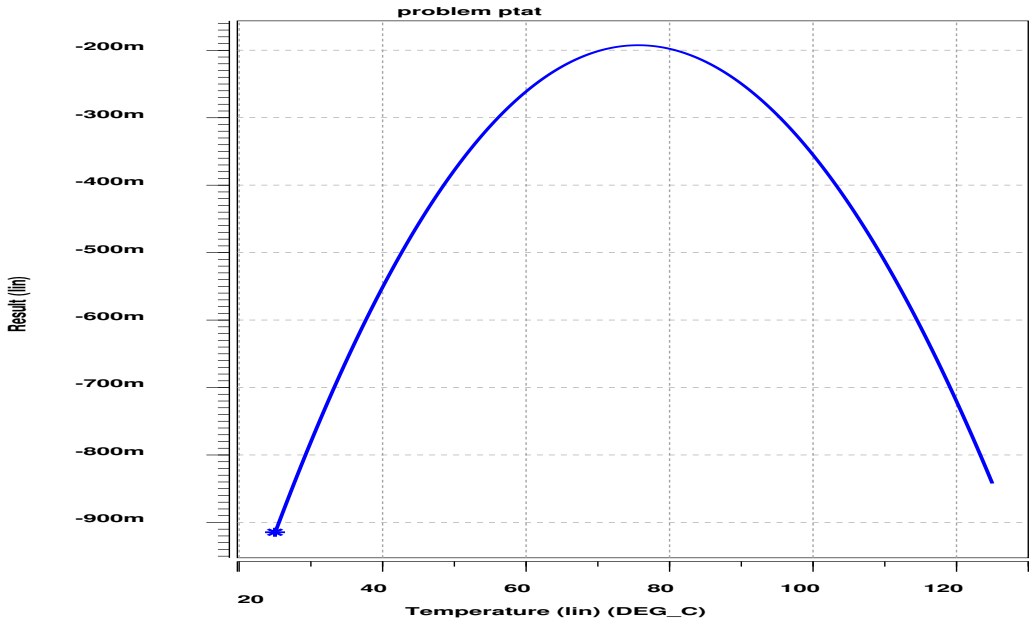

Figure 4.1.5 Basic PTAT Current Error

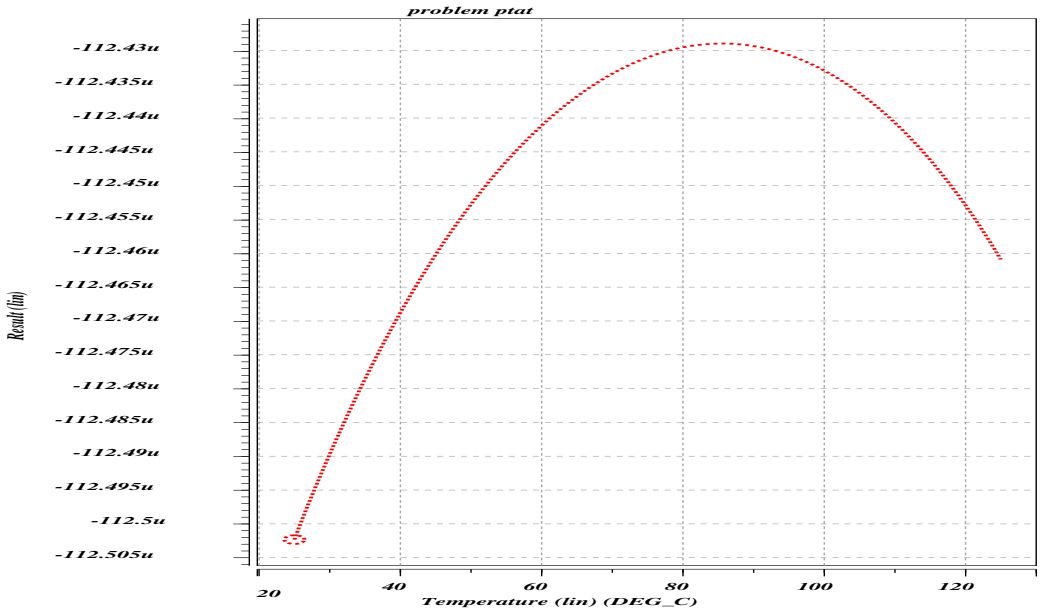

Figure 4.1.6 Basic BGR Current Error

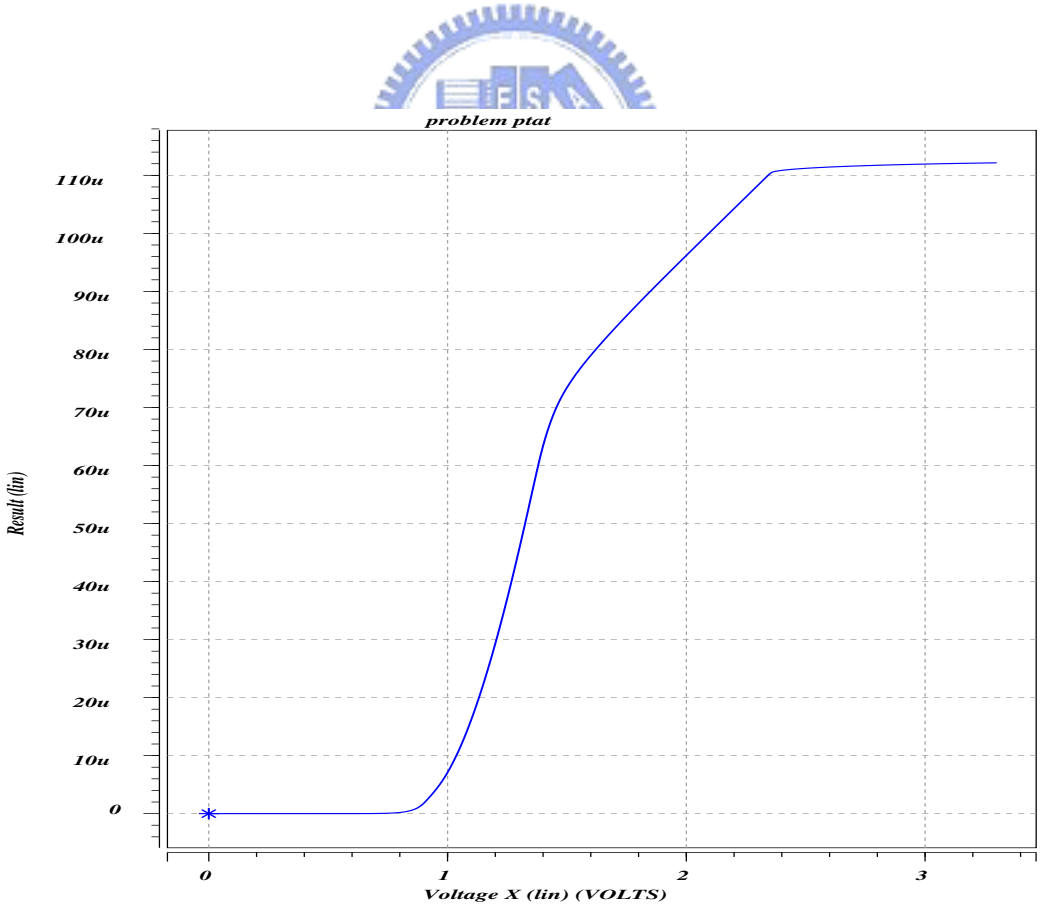

Figure 4.1.7 Bandgap Reference Current Versus Supply Voltage

4.1.3 Power-on-Reset Circuits Simulation

As described in section 2.2.3 and section 3.1.4, to prevent the PTAT circuit from settling to the wrong steady state condition (zero current state). A start-up or POR circuit is necessary in all practical PTAT circuits. However, start-up circuit consumes additional power caused by a branch being on. For less power consumption, a POR circuit is used. The simulation of POR circuit is shown that it can start up overall circuit and reduce power dissipation. The simplified POR circuit is shown in Figure 4.1.8.

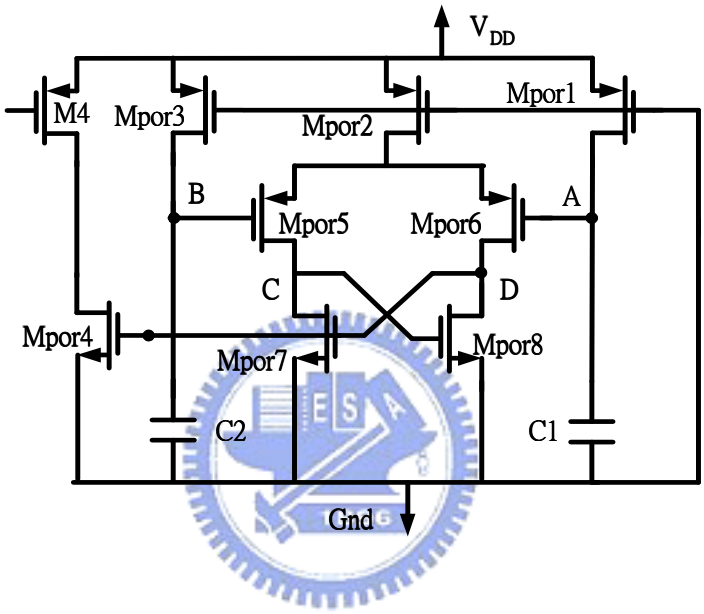

Figure 4.1.8 Simplified POR circuit

Figure 4.1.9, and Figure 4.1.10 show the simulation of POR circuit. when the power supply is on, the voltage of node A, B, C, and D are shown in Figure 4.1.9. The node A and node B both charge from 0V to V_{DD}, but the node A has less RC time constant than node B. The node A has faster speed to reach V_{DD}, so node C will latch to V_{DD} and node D will latch to 0V as described in Figure 4.1.9.

Now, let us check whether the PTAT circuits started up or not. In this Hspice simulation, the initial condition of EBJ voltage is first set to be zero. Then, the transient response is observed as Figure 4.1.10. The EBJ voltage indeed settles to the voltage of normal operation, but there is an overshoot in the transient. This is because the POR circuit consists of a latch, and that will reduce stability. For using POR circuits as start-up circuits, there is a trade off between stability and power dissipation.

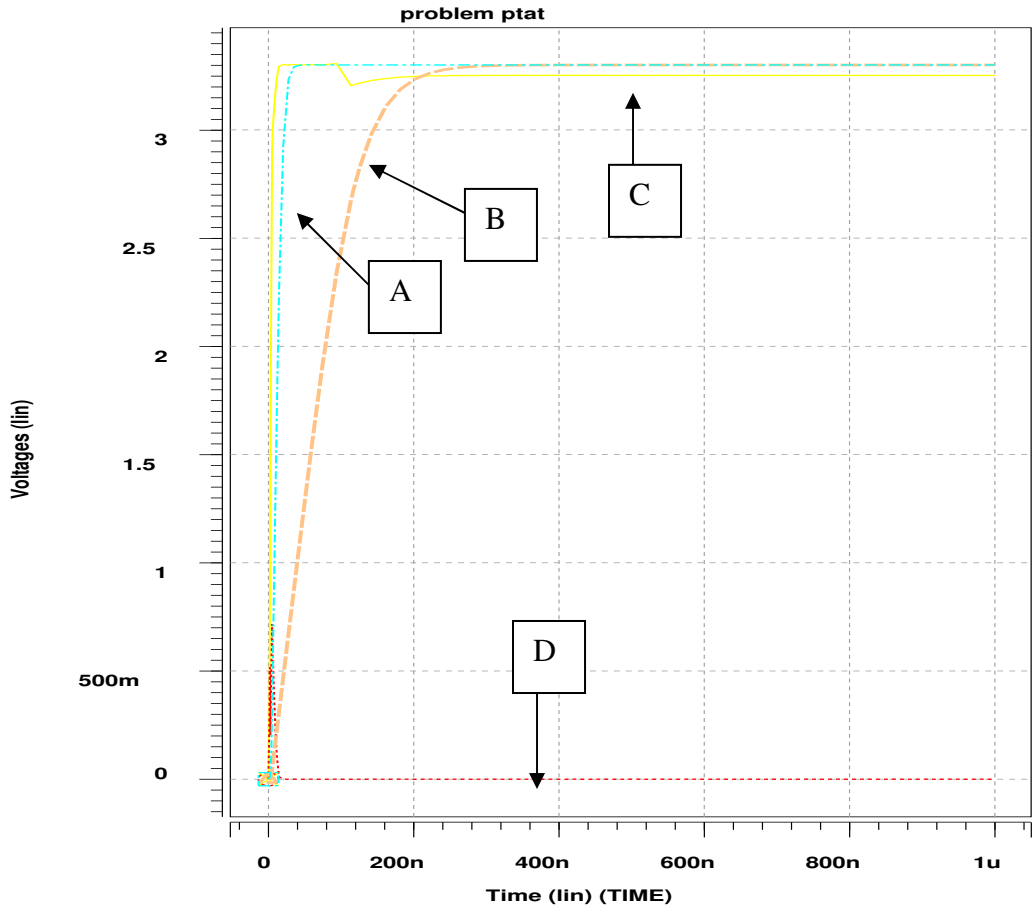

Figure 4.1.9 The Transient Response of POR Circuit

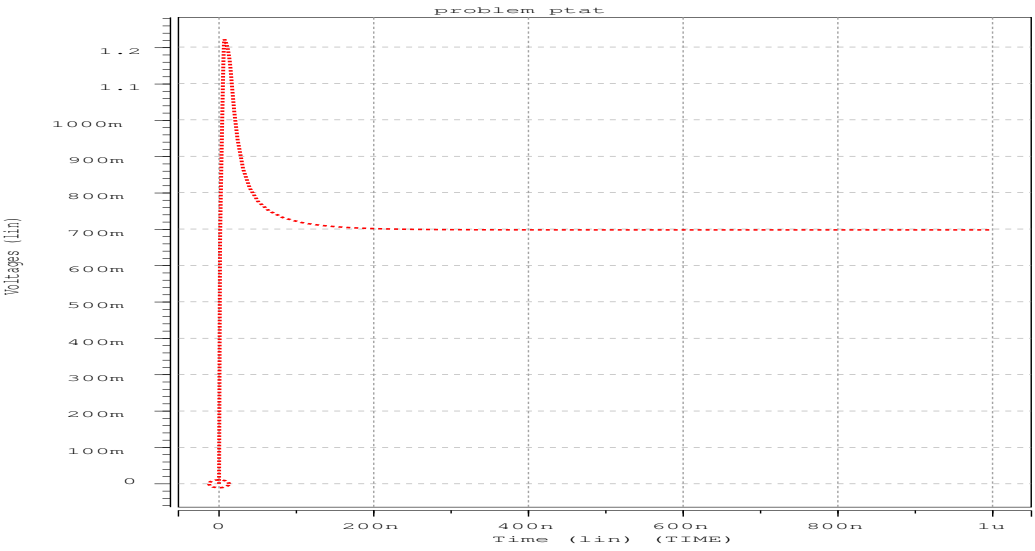

Figure 4.1.10 The Transient Response of PTAT Circuit

	Additional Power dissipation
Start-up circuit (as Figure 2.2.5 with Rs 200K)	46uA
Start-up circuit (as Figure 2.2.5 with Rs 500K)	20uW
Proposed POR circuit	0uW

Table 4.1.2 The power Dissipation of POR and Start-up Circuit

Finally, Table 4.1.2 shows the power dissipation of start-up circuit and POR circuit simulated by Hspice. From this table, it shows that the POR circuit consumes no additional power. For using start-up circuit, it consumes additional power. However, Rs can be increased to reduce current of conducting branch so that power dissipation can be reduced. The disadvantage of increase Rs will make the overall area of chip be larger. by contrast, no resistors is used in the POR circuit of proposed design, adding POR circuit in our PTAT and BGR will not consume too larger area.

After using the POR circuit, the total power dissipation of our proposed design is 515.5uW. The dissipated power saved by POR circuit is about 9%.

4.1.4 Curvature Corrected Circuit Simulation

As described in section 3.1.3, the curvature corrected circuit of out design is only adding two resistors of high TC (R2 and R3). TSMC 0.25um technology provides many kinds of resistors, the lowest TC resistor is chosen for R1 and Rbe, because these two resistor should have zero TC and there are no resistors of zero TC in this technology. The highest TC resistor is chosen for R2 and R3, because the difference of TC between R1 and R2 is larger, the correction effect will be better. Another reason of choosing these two types resistors is that their values suffer from less process variation. The characteristics of the two materials are described in Table 4.1.3.

Film	Rsh	unit	TC1	TC2
P+ poly w/o silicide	160±30	Ohm/sq	764ppm/K	N/A
N-well under STI	1100±250	Ohm/sq	3600ppm/K	11.2ppm/K

Table 4.1.3 Characteristics of Resistors in Our Design

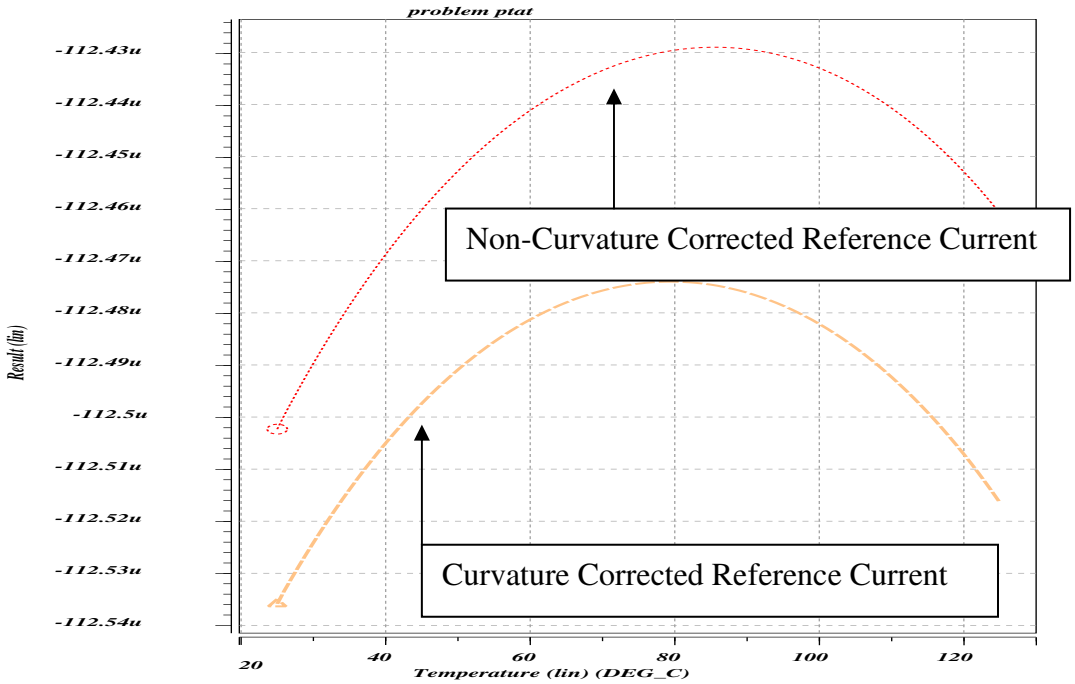

Figure 4.1.11 Non Corrected Reference Current Versus Corrected One

Figure 4.1.11 shows the current with curvature correction and the one without curvature correction, then Figure 4.1.12 shows the TC of reference current with curvature correction and the one without curvature correction. From Figure 4.1.12, it shows that the reference current with curvature correction only improves its TC under 65^{o}C. This is because the resistors of high TC has the second order TC, and the second order term of the resistor will reveal its nonlinear effect to increase the TC of BGR current. If we want to improve the nonlinearities of BGR current, we will search another material of the high TC resistor which has less the second order TC.

In this section, the simulation of proposed design is described here. The main advantages of proposed design are saving power by POR circuit and portable to deep sub-micron process. In next section, the schematic circuit of proposed design is converted to layout and the details of layout consideration are described.

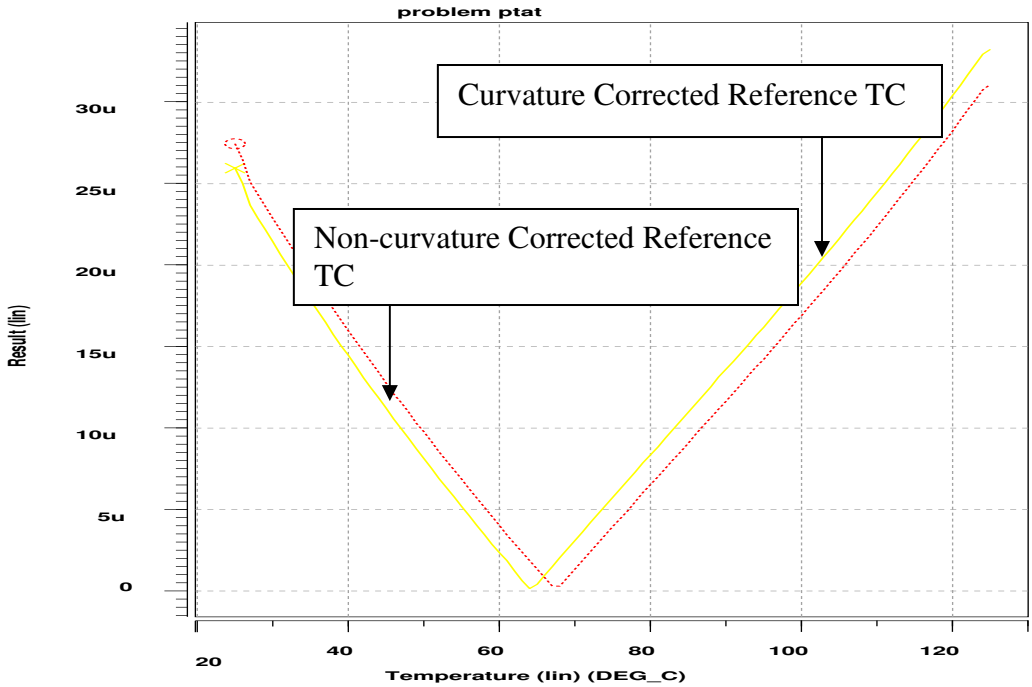

Figure 4.1.12 Non Corrected Reference TC versus Corrected One

4.2 Layout Descriptions

An experimental chip is designed and fabricated in TSMC 0.25um 1P5M CMOS technology. It is shown in Figure 4.2.1 and consists of those as follow:

(1) PTAT circuit
(2) BGR circuit
(3) Curvature corrected circuit
(4) POR circuit

The PTAT has 1^{o}C temperature resolution, and the BGR has maximum TC 30ppm/^{o}C. The power dissipation of the chip is 550uA, and the area is 260um*200um. The minimum supply voltage is 2.3V. the total information of this chip is described in Table 4.2.1 as following:

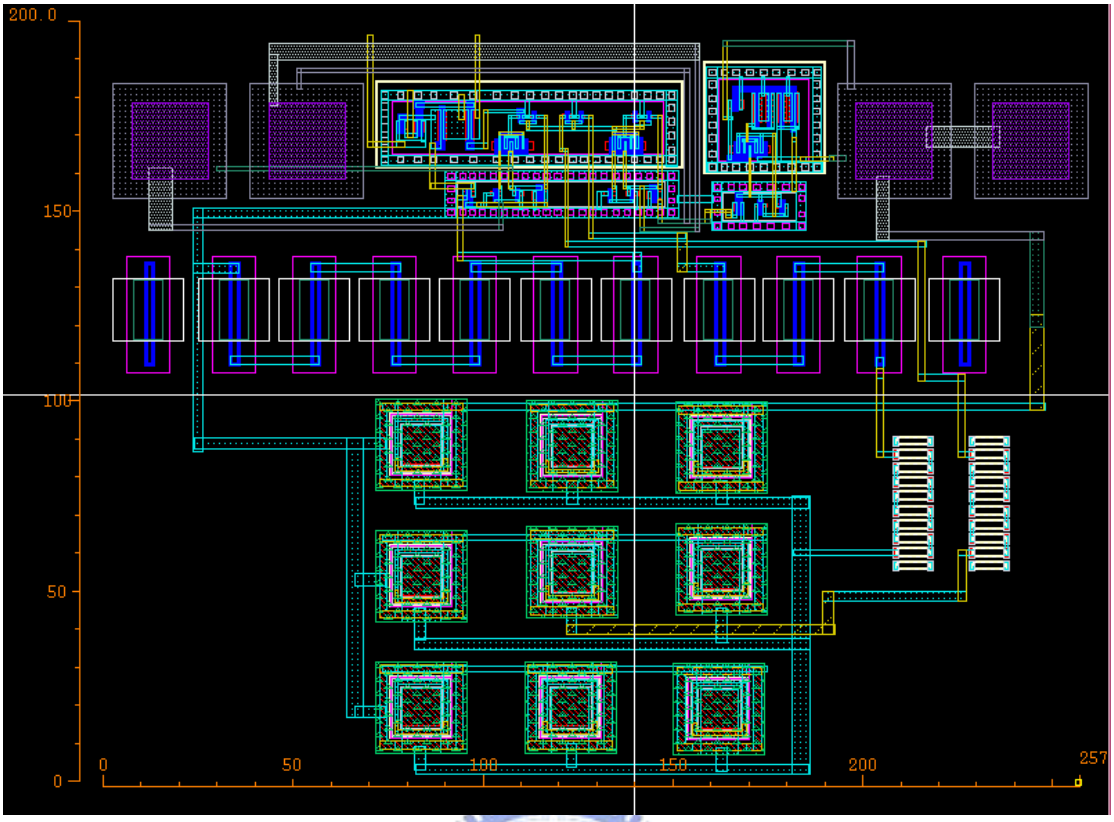

Figure 4.2.1 The Layout of Overall Circuits

Process	TSMC 0.25 process
Temperature Resolution	1°C
BGR TC	30ppm/ °C
Power dissipation	550uW
Minimum supply voltage	2.3V
Area	260um*200um

Table 4.2.1 Characteristics of Chip simulation

4.3 Measurement Setup

A testing setup for fabricated prototype chip is presented in this section, and a costumed designed printed circuit board (**PCB**) is designed and fabricated to chip. The instrumental setup is also described to measure the chip. The block diagram of the measurement environment is shown in Figure 4.3.1 as follow:

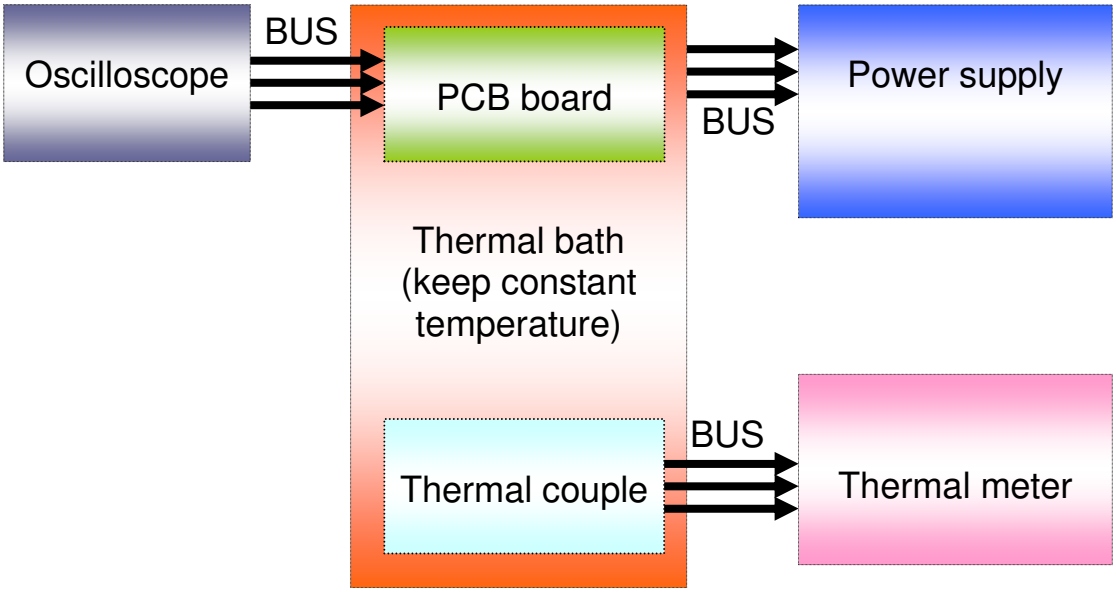

Figure 4.3.1 The Block Diagram of Measurement Environment

The components of measurement environment are described as following:

(1) Power supply

(2) Thermal bath

(3) PCB board

(4) Thermal couple

(5) Oscilloscope

For (1), power supply provides V_{DD} signal to power on overall circuit. For (2), thermal bath provides the environment that can keep a stable temperature and make the temperature be tunable. For (3), PCB board provides the interface between chips to measurement instruments. For (4), thermal couple provides to monitor the temperatures of thermal container and chips. For (5), Oscilloscope provides to observe the waveforms of output signals.

In Figure 4.3.2, it shows the picture of our PCB board which consists of chip and all the passive components. In Figure 4.3.3, it shows the real measurement environment and sets up according to Figure 4.3.1.

After ensuring the measurement environment, the experimental results will be shown in the following section.

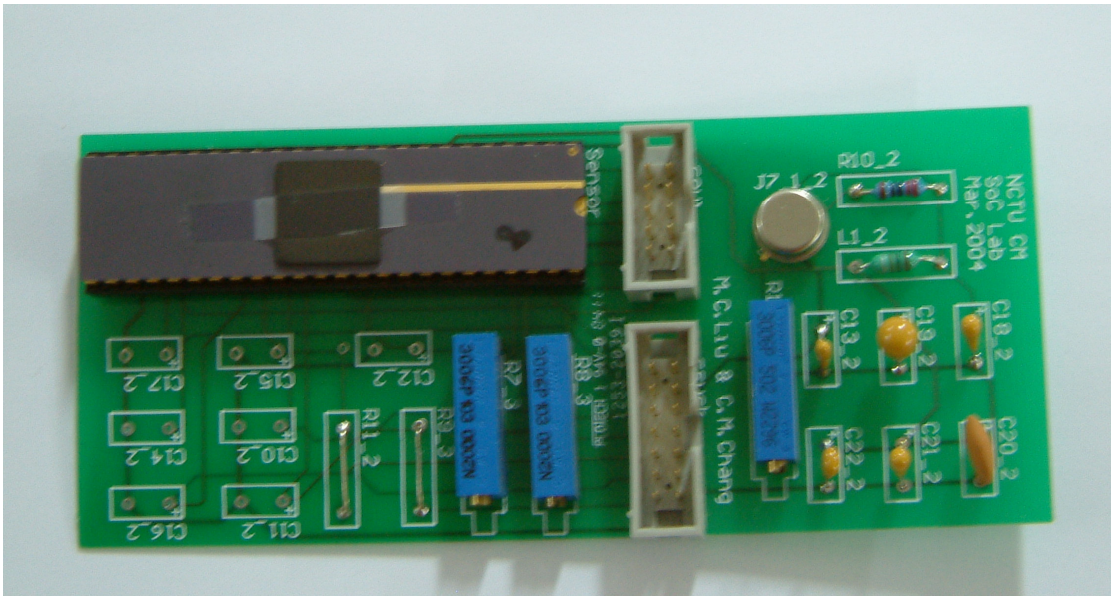

Figure 4.3.2 The PCB Board of Overall Circuits

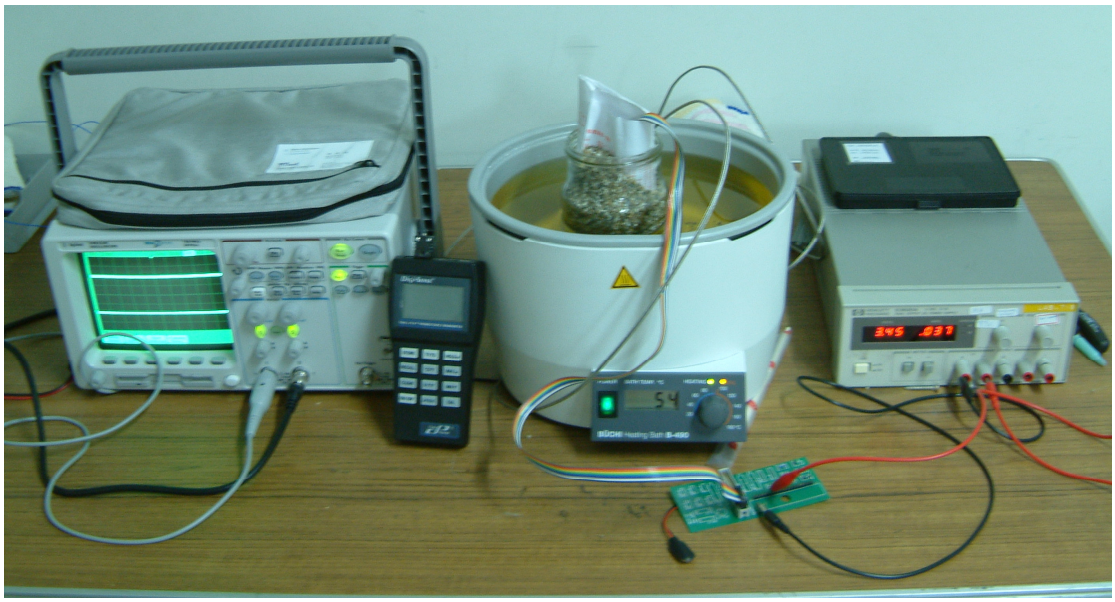

Figure 4.3.3 The Measurement Environment

4.4 Experimental Results

In this section, a part of proposed design is fabricated in TSMC mixed-signals 1P5M process and the chip consists of the basic PTAT and BGR circuits. the die photo of this chip is shown in Figure 4.4.1 as following:

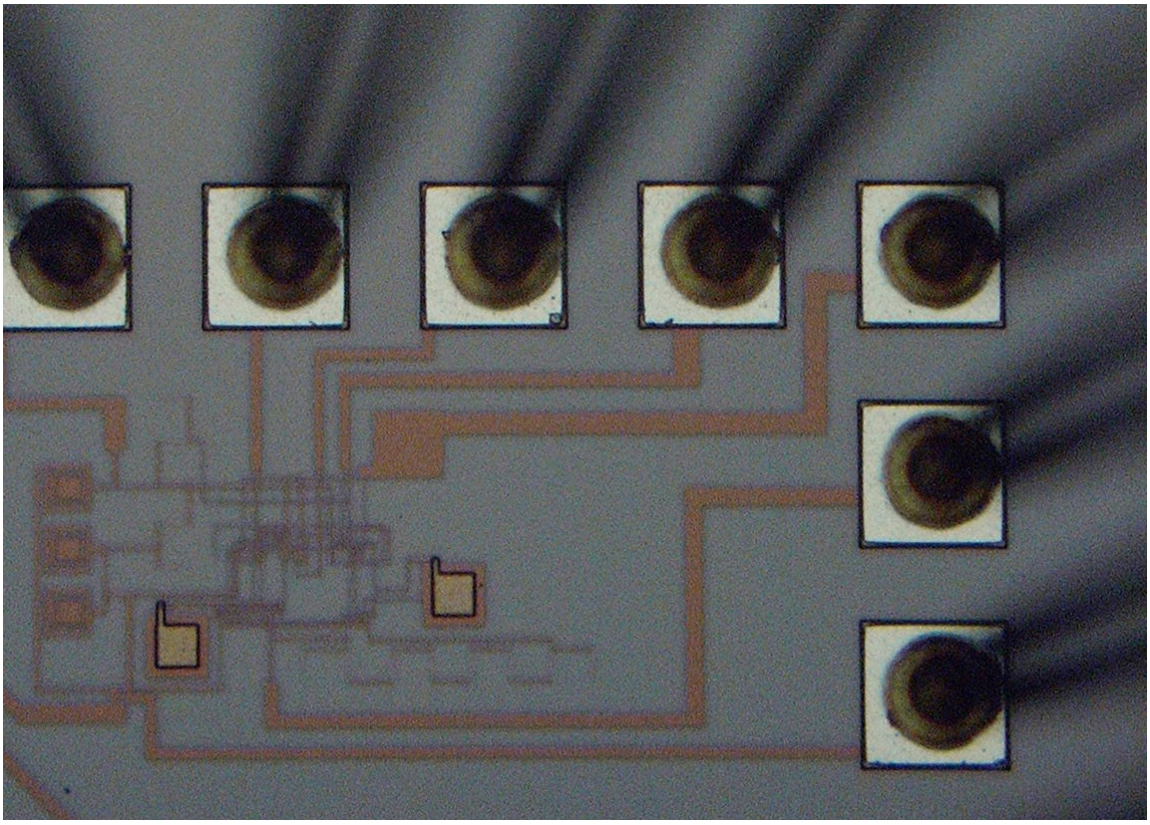

Figure 4.4.1 The Die Photo of Basic PTAT and BGR

In our proposed design, a POR circuit is added to reduce the power dissipation of start-up circuit, but it will not influence on the DC bias of original PTAT and BGR circuits. If the functionalities of this chip work successfully, adding POR circuit to the basic PTAT and BGR circuit will still work and obtain the advantage of reducing dissipated power.

Before measuring the output currents of PTAT and BGR, the DC bias of this chip must be checked to ensure that it is operated in the correct region. The DC bias of this chip is shown in Table 4.4.1 and consists with the simulation.

Pin	Name	Description	Experimental Voltage
3	VEB1	BJT1 EBJ voltage	803mV±50mV
4	GND	Ground	0±50mV
39	VEB2	BJT2 EBJ voltage	739mV±10mV
40	VRbe	Rbe voltage	717mV±50mV
41	VDD	Supply voltage	3.3V±100mV
44	VR	Drain voltage of M2	824mV±50mV
45	Vptat	PTAT voltage for Iptat	2.12V±200mV
46	Vref	Reference voltage for Iref	148mV±20mV

Table 4.4.1 The DC Bias of Chip

After ensuring the DC bias of this chip correct, PTAT measurement results are shown in Figure 4.4.2. Figure 4.4.2, which has cancelled the offset error of current, shows the comparison between these measurement results of three chips and Hspice simulation. The reason which offset error can be ignored is that the offset error can be calibrated by other techniques in thermal-aware or thermal management system.

The slopes of these four lines, which are calculated by regression analysis, indicate the TC of PTAT current, and are shown in Table 4.4.2. The TC error between measurement and Hspice simulation is very large. The error sources are described as following:

(1) Resistor Error about 14%

(2) Aspect Ratio Error about 8%

(3) Corner Error about 2%

(4) △VEB error about 21%

A error estimation is described as following:

$$\frac{Sim}{\frac{[1+R(error)]\times[1+AspectRatio(error)]\times[1+corn(error)]}{[1+\Delta V_{EB}(error)]}} = Measure \tag{4.1}$$

$$Sim = Measure\frac{[1+R(error)]\times[1+AspectRatio(error)]\times[1+corn(error)]}{[1+\Delta V_{EB}(error)]}$$

The aspect ratio error of M7 is due to the coarse layout as Figure 4.4.3. The finger technique is not used so that the ratio error is introduced.

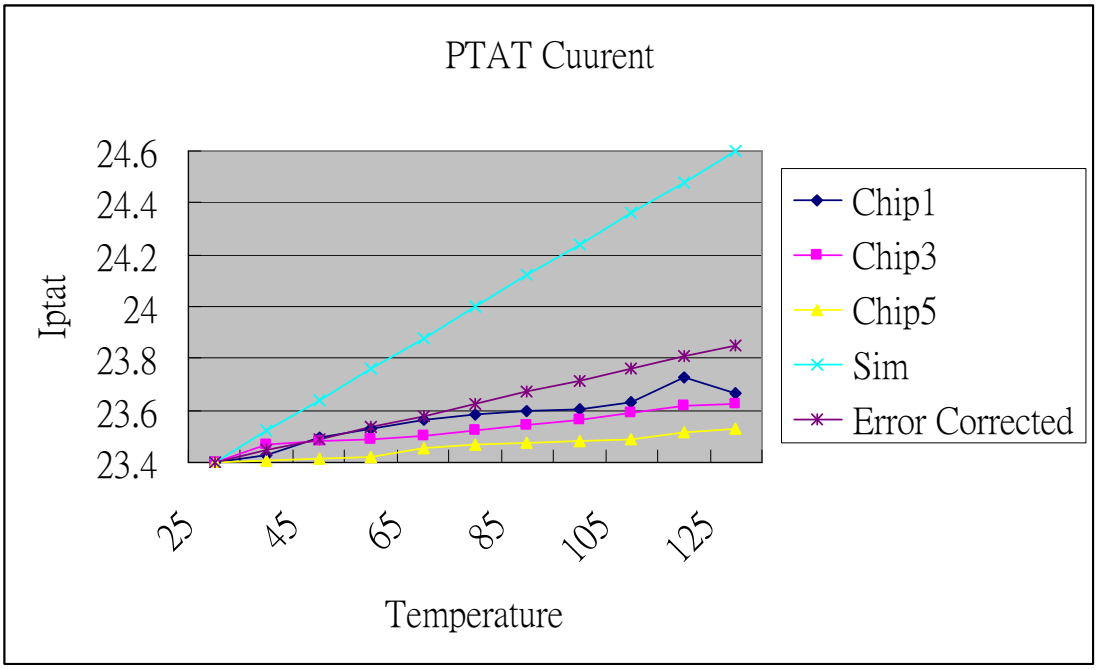

Figure 4.4.2 Measurement Results of PTAT current

	Chip1	Chip3	Chip5	Error corrected	Sim
TC (uA/^{0}K)	0.002817	0.002058	0.001317	0.00451	0.012

Table 4.4.1 The TC of measurement results and Hspice simulation

After including the error of process variation, a corrected TC is obtained and its value is shown in Table 4.4.1. the corrected TC value is very close to TC of measurement.

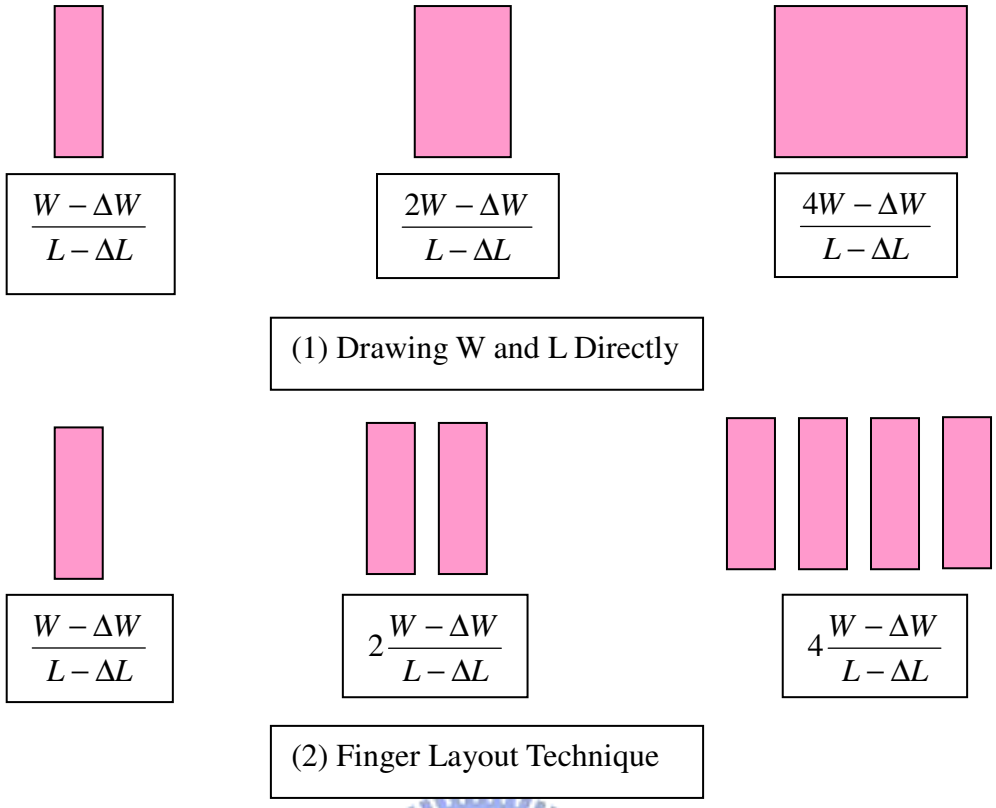

Figure 4.4.3 Wider Transistor Layout Methods

After showing and discussing the measurement results of PTAT current, the measurement of BGR current are shown in Figure 4.4.4. Figure 4.4.4 also shows the comparison between these measurement results of three chips and Hspice simulation, and the error between measurement and Hspice simulation is about 40%. The errors are caused by the same sources as the same as the reason of PTAT current.

The curvature corrected circuits is only adding small but high TC resistors in the basic PTAT and POR. The DC bias of overall circuits drifts a little after adding curvature corrected circuit. If the basic BGR works correctly, adding curvature corrected circuits in this chip will be confident of improving the accuracy of BGR current.

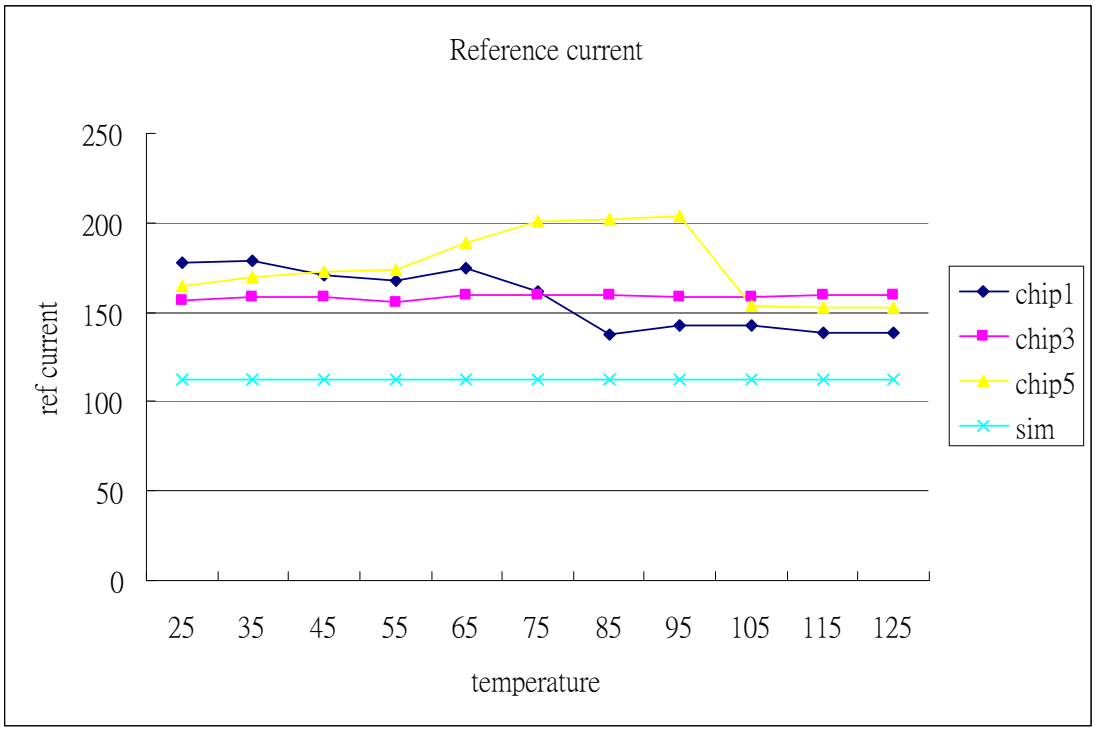

Figure 4.4.5 Measurement Results of BGR current

In this section, the measurement results of PTAT and BGR current are shown and the errors between measurement and simulation are discussed. Although the functionalities of the chip all work correctly, there still are many error sources being reduced by careful layout.

4.5 Summary

In this chapter, first, a design flow is obeyed to implement our proposed design. Second, Hspice simulation is shown and adjusting parameters of transistors to obtain the best transistor sizing. Third, layout consideration and measurement setup are described. Finally, the measurement results which are of part proposed design are shown.

In next chapter, the conclusion of this thesis is introduced and the future works of proposed design are described.

Chapter 5 Conclusion and Future Works

After simulation and the measurement of proposed design in previous chapter, the conclusion of proposed design is described in section 5.1. There are still some characteristics of proposed design to be improved, and they will be described and discussed in section 5.2.

5.1 Conclusions

In this thesis, the proposed design has successfully overcome these problems described as following:

(1) Additional power dissipation by start-up circuits

(2) Compatible with deep sub micron process.

(3) High accuracy of BGR signals

For (1), the new type POR circuit in proposed design eliminates the additional power dissipation by start-up circuits. For (2), the proposed design has been fabricated by TSMC 0.25um 1P5M process and the functionalities of PTAT and BGR have worked described in chapter 4. For (3), the curvature corrected circuit of proposed design makes the BGR be more accurate in low temperature, but the accuracy in high temperature is not improved constrained by second order TC of the corrected resistors.

From the above description, there are still defects in proposed design which can be improved to make proposed design more perfect. In next section, these issues are discussed and described.

5.2 Future Works

In this section, the insufficiencies of proposed design are described and listed below:

(1) Insert POR and curvature corrected circuits to proposed design and tape it out

(2) Make the supply voltage lower

(3) Increase accuracy of BGR

For (1), although the simulation of POR and curvature corrected circuit have verified their functionalities, they have yet been integrated with the basic PTAT and

BGR. In future, to complete and to verify overall proposed design is necessary.

For (2), because the supply voltage in modern process is lower and lower, it is necessary to modify our design to portable to low supply voltage systems.

For (3), in order to increase the accuracy of BGR, chopper technique can be added to improve the BGR accuracy.

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