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砷化鎵低噪音假晶高電子遷移率電晶體
之
銅金屬化導線製程

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Copper-Metallized Interconnects on GaAs Low Noise Pseudomorphic High Electron Mobility Transistors

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砷化鎵低噪音假晶高電子遷移率電晶體之

銅金屬化導線製程

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摘要

這篇論文研究使用在砷化鎵上面的銅金屬擴散障礙層之特性，並探討銅金屬化蕭特基接觸以及銅金屬化導線製程應用在砷化鎵元件上之可行性。在這些擴散障礙層的研究中，耐火金屬以及耐火金屬之氮化物被應用在銅金屬化蕭特基二極體以及銅金屬化導線製程之製作。

本篇研發之砷化鎵蕭特基二極體，其蕭特基結構使用銅金屬，並使用耐火金屬作為障礙層。這種蕭特基結構具有比傳統鈦/鉑/金蕭特基結構更低的串聯電阻。根據電性及材料分析，鈦/鈷/銅以及鈦/鉬/銅之熱穩定性可達攝氏四百度，而鈦/鈷/銅蕭特基結構之熱穩定性可達攝氏三百度。總而言之，銅金屬化蕭特基結構具有優良的電性及熱穩定性，並且可應用於砷化鎵元件的蕭特基金屬製程。

在本實驗中使用氮化鎢作為銅金屬化導線製程之擴散障礙層。這是由於氮化鎢和傳統製程上有高度的相容性。本實驗發展使用銅金屬化導線之砷化鎵低噪音假晶高電子遷移率電晶體之製程。此製程使用濺鍍氮化鎢作為擴散障礙層並使用鈦金屬作為附著層。製作出來的低噪音砷化鎵假晶高電子遷移率電晶體在操作頻率為十八兆赫茲時，元件噪音最低可達一點零九分貝、相關增益值可達六點九分貝。經過攝氏兩百五十度的高溫退火二十個小時以後，銅金屬以及下層的接觸金屬間並沒有金屬原子交互擴散的現象；元件特性在經過熱退火以後並未產生明顯

的變化。這個結果顯示銅金屬化空氣橋製程可以應用在低噪音假晶高電子遷移率電晶體上。

Copper-Metallized Interconnects on GaAs Low Noise Pseudomorphic High Electron Mobility Transistors

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Abstract

In this dissertation, the feasibilities of Cu-metallized Schottky contacts on GaAs and Cu-metallized interconnects for GaAs devices were studied. Diffusion barrier materials for Cu metallization on GaAs were investigated. Several refractory metals and metal nitrides were used as the diffusion barrier and applied to the Schottky contact and interconnect airbridge applications.

Schottky structures with Cu and refractory metals as the diffusion barrier for GaAs Schottky diodes were evaluated. These structures have lower series resistances than the conventionally used Ti/Pt/Au structure. Based on the electrical and material characteristics, the Ti/W/Cu and Ti/Mo/Cu Schottky structures are thermally stable up to 400 °C; the Ti/Co/Cu Schottky structure is thermally stable up to 300 °C. Overall, the Cu-metallized Schottky structures have excellent electrical characteristics and thermal stability, and can be used as the Schottky metals for GaAs devices.

For airbridge fabrication, tungsten nitride was chosen as the diffusion barrier for Cu-airbridged PHEMT due to its compatibility with the airbridge process. A GaAs pseudomorphic high electron mobility transistor (PHEMT) with Cu-metallized airbridges was successfully developed. Sputtered WNx was used as the diffusion barrier and Ti was used as the adhesion layer to avoid the peeling problem between

Au/WNx and WNx/Cu. When tested at 18 GHz, the fabricated low noise GaAs PHEMT with Cu interconnect had the lowest noise figure of 1.09 dB and the associated gain was 6.9 dB. After thermal annealing at 250^0C for 20 hours there's no interatomic diffusion between Cu and underlying contact metals and the devices showed little change in the device performance. These results show that the Cu-metallized airbridges can be used as the interconnects for low noise PHEMTs.

Chapter 1
Introduction

The Cu metallization process has become popular in Si device manufacturing and has been widely studied, but there are very few reports about Cu metallization process for GaAs-based devices [1-3]. In this work, Cu-metallized Schottky contacts and Cu-metallized interconnects for GaAs devices were studied.

Various materials have been considered for metallization of integrated circuits (IC). Au and Cu possess several remarkable features: both have low resistivity (2.2 μΩ-cm for Au; 1.67 μΩ-cm for Cu), and provide high resistance against electromigration related failures [4].

Au has not been used in metallization for Si-based devices. However, Au is extensively used for GaAs device fabrication, mainly due to its high electrical conductivity and relative chemical inertness [5]. Au metallization needs the use of adhesion layers, like Ti or Cr; and also needs the use of barrier layers such as platinum or palladium to impede its diffusion into GaAs [6].

Cu metallization is widely used as the interconnect material in the Si IC technology. This is principally because of its low resistivity (1.67 μΩ-cm), which results in a lower RC time delay, and the enhancements in the resistance of electromigration and stress-induced failures [7,8], which greatly improves the device performance and reliability. The Cu metallization process has become progressively popular in the Si IC industry ever since IBM scientists announced a remarkable advance in Cu metallization for semiconductor process in September 1997 [9–11]. Recently Cu has been widely employed by major semiconductor companies as interconnect material of the ultralarge-scale integration (ULSI) circuits, the process involves damascene patterning techniques with compatible low dielectric constant

materials [12-23].

The Ti/Pt/Au Schottky contact is the most widely used structure for the fabrication of metal-semiconductor field-effect transistors (MESFETs), high-electron-mobility transistors (HEMTs), and Schottky diodes. In this study, the top Au layer of the Schottky structure was replaced by Cu. This has the advantages of reduced electrical resistivity and production cost when compared with the use of Au. The Pt layer was replaced by the transition metals, such as W, Co and Mo, due to the better anti-diffusion capability and the electrical conductivity of these transition metals. According to the binary alloy phase diagrams [24], there is no formation of intermetallic compounds between W (Co, Mo) and Cu. Thus, the thermal stability of these Cu-metallized Schottky structure including Ti/W/Cu, Ti/Co/Cu and Ti/Mo/Cu was investigated in this study. The detailed study of Cu-metallized Schottky contacts will be described in Chapter 2.

Conventionally, plated Au was employed for airbridge interconnects on GaAs devices, including MESFETs and HEMTs. Plated Au has high electrical conductivity, is resistant to oxidation and ductile. However, Au is expensive, which causes the high cost for the GaAs device fabrication. At present, Cu is one of the most attractive materials for interconnect metallization of ULSI circuits because of its low resistivity and excellent resistance against electromigration. However, key issues need to be solved if Cu interconnections are used for GaAs device metallization:

1) It is necessary to use a thin barrier layer with good linear conformality with Cu to block Cu diffusion especially for narrow, high aspect-ratio structures.

2) A passivation layer is required to prevent the oxidation of Cu surface [25].

In this work, Cu replaces Au as the interconnect material used for the airbridges in the GaAs PHEMTs and WNx was used as the diffusion barrier. The goal of the research is to find a reliable diffusion barrier for Cu metallization of GaAs devices in

order to reduce the production cost of the GaAs devices and to provide comparable or even better thermal and electrical conductivities for the interconnects.

The major challenges for the integration of Cu metallization are the choice of suitable diffusion barrier material and the deposition techniques of the diffusion barrier and the Cu layer. The barrier layer should be as thin as possible so that it would not affect the interconnect resistance while still acting as a good barrier against Cu diffusion.

The choice of multilayer thin films needs to consider the following aspects: the electrical resistivity, mechanical stress, chemical inertness, thermal stability, adhesion characteristics, film deposition techniques, and easiness of film patterning [6].

Refractory metal is a good choice as the diffusion barrier materials. This is because of its high melting point. Its solubility in Cu was very low even though at high temperatures. However, the sheet resistance of Cu increases rapidly at 400 ℃ annealing when using a single refractory metal as the diffusion barrier, like Cu/Ta/Si, Cu/Ti/Si, and Cu/W/Si. It implies the Cu atoms diffuse into Si and forms copper silicide. The single metal diffusion barrier layer is a polycrystalline structure with grain boundaries. The grain boundaries provide fast diffusion paths for the Cu because of the high diffusion coefficient along the grain boundaries. Cu diffuses through the grain boundaries of the diffusion barrier layer easily into the Si junction region even at low annealing temperatures and causes the device failure. Refractory metal nitrides such as TiN, TaN and WNx have been investigated due to their better thermal stabilities, good adhesion, and low resistivities. Therefore, these transition metal nitrides, which have high melting points, relatively high thermal stability, chemical inertness, and low electrical resistivity, would not form metallic compounds with Cu. Some of the results of the investigations of the refractory metals and refractory metal nitrides as the diffusion barriers for Si are listed in Table 1 [26-34].

The thermal stabilities of these barrier layers with Cu are summarized in Table 1. These barrier layers include TiW, TiN, Ta, TaN, Ta-Si-N and WNx. Most barrier materials are stable with Cu up to 550 °C. The temperature is high enough for current metallization processes.

Only a few investigations of the Cu metallization process on GaAs devices have been reported [1-3, 35-41], and Ta and TaN were employed as the diffusion barriers in these papers [1–3]. In this work, we use WNx as the diffusion barrier between Cu and Au, and successfully apply WNx to the Cu metallization of the airbridge interconnects of the AlGaAs/InGaAs low noise pseudomorphic high electron mobility transistors (LN-PHEMTs). 2.5 μm Cu was electroplated on the sputtered Cu seed layer and the WNx barrier layer to form the airbridges on the Au contacted PHEMTs. The fabricated low noise PHEMTs with Cu airbridges were thermally annealed in order to evaluate the thermal stability of WNx as the barrier between Cu and underlying Au-based contacts [41].

However, the peelings off problem of the Cu airbridges were observed in certain areas of the devices. The peeling interface was observed between Au/WNx and WNx/Cu interfaces. This implies that the adhesion between these films was not good.

From conventional Au metallization, adhesion of the Au film on the oxide substrate can be improved through the deposition of an intermediate metal film (Ti, Cr, W) [42].

The most common species of adhesion film for ball-limited-metal (BLM) system under solder bumps are Ti and Cr. Ken'ichi Mizuishi *et al.* have investigated the mechanical pull-strength of the BLM layers formed under controlled-collapse solder (lead-5 wt % tin) bumps for flip-chip interconnections [43]. All BLM systems used here consist of a triple-layer deposited with Cr or Ti as an adhesive, Ni, Pt, Pd, or MO as a barrier, and Au as the surface metal. Using test chips with these BLM

systems, mechanical pull-strength values of solder-bump joints were obtained as shown in Figure 1.1. From a simple comparison between the mechanical strength values, they found that the BLM systems with Ti adhesive metal showed generally superior solder-joint strength than those with Cr, independent of the barrier metal used. This is due to the presence of the joint fracture mode which is closely related to the kind of adhesive metal used. It is also found that, with the same adhesive metal, greater solder-joint strength appears in the order of Ni, Pt, Pd, and Mo. Therefore, we decided to use Ti as the adhesion layer for our multilayer metallization system to overcome the peeling off problem of the airbridges.

As a result, new multilayer schemes, Ti/WNx/Ti/Cu, were used in this study to improve the film adhesion on Au pad and on silicon nitride passivation layer. The Ti thin films were inserted between Au/WNx layers and between Cu/WNx layers respectively. The most upper two layers, Ti/Cu, which were used extensively in solder bump fabrication as an adhesion and seed-conducting layer between electroplated Cu and WNx layers [44,45]. There are reasons for it. The adhesion is good between Ti and Au layers because Ti diffuses into Au fast, producing Au-rich intermetallic compounds [46]. The Ti/Au/Ti scheme is the traditional airbridges process for GaAs devices.

For the Ti/WNx interface, F. C. T. SO *et al.* suggested that nitrogen in the W-N layer redistributed into Ti layer after annealing at 550 °C for the Si/Ti/WNx/Al samples [47]. They attributed this redistribution of nitrogen to the stronger affinity of Ti with nitrogen than with W. It implied that the Ti layer reduces WNx to W upon annealing at 550 °C and forms a good Ti-N interface with good adhesion. For the SiNx/Ti boundary, T. W. Orent *et al.* suggested that Ti reduces the Si from the silicon nitride during deposition process and forms TiN and free Si. The free Si reacts with additional Ti at the Ti/TiN interface to form a silicide in the SiNx/Ti/Cu samples at

above 500 °C annealing and thus improve the adhesion of this material system [48]. Kazuhide Abe *et al.* introduced a Cu/Ti/TiN/Ti (similar to the Ti/WNx/Ti/Cu structure used in this study) layered damascene interconnects and investigated the electromigration resistivity of this system compared to the traditional Cu/TiN/Ti scheme [49]. Ti insertion improves the wetting property of the Cu film to the underlying TiN layer and increases the sheet resistance of the layered structure after thermal annealing. This resistance increases due to the diffusion of Ti into the Cu film and thus resulting in the reduction of the cross-sectional area of the Cu layer. The Cu damascene interconnects with Ti insertion show up to 100 times longer electromigration lifetime than those without Ti insertion [49]. Microstructures of the Cu film such as grain size, grain distribution and texture did not change for samples with or without Ti insertion. The insertion of Ti into Cu improves of the interface quality between Cu and the underlayer, which impacts the diffusivity of Cu atoms at the interface, and thus enhance the electromigration resistance of the material system.

Based on the materials studies from Si industry, new multilayer systems Ti/WNx/Ti/Cu were used for the study of Cu metallized airbridges of GaAs devices to ensure good film adhesion and diffusion barrier properties. The fabricated Cu-airbridged low noise PHEMT (LN-PHEMT) using the multilayer systems Ti/WNx/Ti/Cu shows good device characteristics. The details of the fabrication process and materials reliability analysis will be discussed in Chapter 4. The DC and RF performance of the Cu-airbridged LN-PHEMTs will be also demonstrated in Chapter 6.

In conclusions, Cu-metallized Schottky contacts and airbridges processes for GaAs PHEMT fabrication were successfully developed. Different metallization metal stacks containing Cu diffusion barrier were studied and evaluated its thermal stability and adhesion property. The results show that: Cu metallized Schottky structures on

GaAs in this study are all thermally stable up to 300 °C for Schottky contact on GaAs. The Ti/WNx/Ti/Cu structure can improve the adhesion of the airbridge efficiently, and is very suitable for the development of Cu-metallized airbridge on GaAs PHEMTs.

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TABLES

Sample	Barrier Stability	Deposition Notes	Reference
Si/TiW (100 nm)/Cu	725 °C, 30 sec.	*In-situ* Cu on TiW	[26]
Si/TiW (100 nm)/Cu	775 °C, 30 sec.	Air between Cu and TiW	
Si/TiNx (50 nm)/Cu	600 °C, 1 hr.	Sputtering	[27]
Si/TiN (50 nm)/Cu	550 °C, 1 hr.	CVD	[28]
Si/TiN (50 nm)/Cu	650 °C, 1 hr.	Plasma treated CVD	
Si/Ta (60 nm)/Cu	600 °C, 1 hr.	Sputtering	[29]
Si/Ta (50 nm)/Cu	550 °C, 30 min.	Sputtering	[30]
Si/Ta2N (50 nm)/Cu	> 650 °C, 30 min.	Sputtering	
Si/TaN (100 nm)/Cu	750 °C, 1 hr.	Sputtering	[31]
Si/TiSi2 (30 nm)/Ta–Si–N (80 nm) /Cu	900 °C, 30 min.	Sputtering	[32]
Si/W (25 nm)/Cu	650 °C, 30 min.	Sputtering	[33]
Si/W2N (25 nm)/Cu	790 °C, 30 min.	Sputtering	
Si/WN (25 nm)/Cu	500 °C, 30 min.	Sputtering	
Si/WNx (20 nm)/Cu	> 550 °C, 30 min.	PECVD	[34]

Table 1.1 Summary of the thermal stability of the barrier layers used in Si industry.

FIGURES

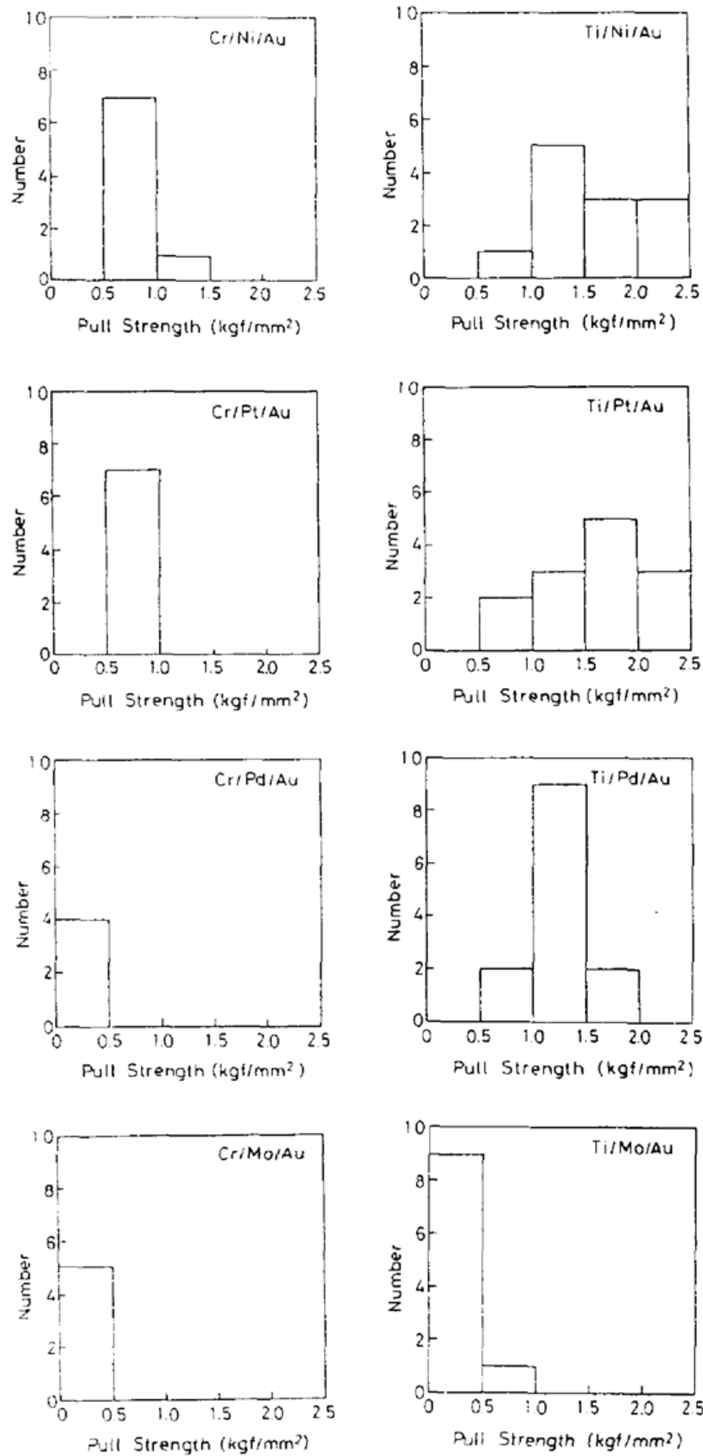


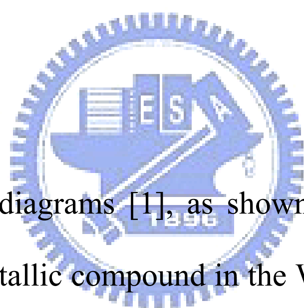
Figure 1.1 Solder-joint pull-strength values measured for test samples with various BLM systems.

Chapter 2

Study of Ti/W/Cu, Ti/Co/Cu and Ti/Mo/Cu multilayer structures as Schottky metals for GaAs diodes

In this work, Ti/W/Cu, Ti/Mo/Cu and Ti/Co/Cu Schottky structures were studied and compared with the traditionally used Ti/Pt/Au Schottky structure. The thermal stability of Ti/W/Cu, Ti/Co/Cu and Ti/Mo/Cu multilayer structures as Schottky metals for GaAs diodes were also studied. These structures were characterized by XRD, AES and sheet resistance measurement. The I-V characteristics for Schottky diodes were also discussed in this chapter.

2.1 Phase Diagrams



According to the phase diagrams [1], as shown in Figure 2.1, Figure 2.2 and Figure 2.3, there is no intermetallic compound in the W/Cu, Mo/Cu and Co/Cu binary systems. These binary systems have negligible mutual solubility. However, in the Ti/W binary system, as shown in Figure 2.4, the maximum solubility of W in αTi is approximately 0.2 at% at 740 °C and Ti has about 3 at% solubility in (βTi-W) at 500 °C. In the Ti/Mo system, as shown in Figure 2.5, the maximum solubility of Mo in (αTi) is approximately 0.4 at% at 695 °C. In general, both Ti/Mo and Ti/W systems have negligible mutual solubility [1]. Whereas, several TiCo intermetallic compounds such as Ti_2Co, TiCo and $TiCo_3$ are formed in Ti/Co system, as shown in Figure 2.6.

2.2 Sample Preparation

The MOCVD (metal-organic chemical vapor deposition) grown Si doped *n*-type

(100) GaAs with thickness of 1μm and concentration of 2.09×10^{17} cm^{-3} was used for the fabrication of Ti/W/Cu, Ti/Mo/Cu, and Ti/Co/Cu Schottky diodes. The area of the diode is 3.14 mm^2. The Ge/Au/Ni/Au ohmic metals were deposited by the electron beam evaporator and annealed by rapid thermal annealing system (RTA) at 400 °C for 60 sec. The Schottky metals were deposited by sequentially DC sputtering the Ti (1000 Å), barrier layer (= W, Co and Mo) (400 Å), and Cu (5000 Å) targets through a metal mask. The conventional Ti/Pt/Au Schottky diode was also prepared for comparison.

2.3 X-ray Diffraction Patterns (XRD)

Glancing angle X-Ray Diffraction (XRD) with Cu K_{α} radiation was used to identify the material phases. The annealing treatment was performed at temperatures up to 500 °C for 30 min. Table 2.1 is the summary of XRD analysis results for the structures after annealing at different temperatures from 200 °C to 500 °C for 30 min. The details of these results are described in the following sections.

2.3.1 The Ti/W/Cu Structure

Figure 2.7 shows the XRD patterns of the Ti/W/Cu structure. This results show that the Ti/W/Cu structure was stable after annealing at 300 °C for 30 min. However, there were compounds formed after the 30 min annealing at the temperature higher than 400 °C. CuTi phase formed at 400 °C and 500 °C due to the failure of W as the diffusion barrier for Cu. According to these results, it can be concluded that the W thin film is an effective diffusion barrier layer for Cu at annealing temperature up to 300 °C.

2.3.2 The Ti/Co/Cu Structure

Figure 2.8 shows the XRD patterns of the Ti/Co/Cu structure. This results show that the Ti/Co/Cu structure was stable after annealing at 300 °C for 30 min. However, there was compounds formed after the 30 min annealing at the temperature higher than 400 °C. Co started to react with Ti and formed the CoTi phase at 400 °C and 500 °C. According to these results, it can be concluded that the Co thin film is an effective diffusion barrier layer for Cu at annealing temperature up to 300 °C.

2.3.3 The Ti/Mo/Cu Structure

Figure 2.9 shows the XRD patterns of the Ti/Mo/Cu structure. This results show that the Ti/Mo/Cu structure was thermally stable after annealing at 300 °C for 30 min. However, there were compounds formed after the 30 mins annealing at the temperature higher than 400 °C. CuTi phase formed at 400 °C and the peaks of Cu_3Ti were found in the XRD patterns after 500 °C annealing. The formation of these intermetallic compounds was due to the failure of Mo as the diffusion barrier. According to these results, it can be concluded that the Mo thin film is an effective diffusion barrier layer for Cu at annealing temperature up to 300 °C.

2.4 Measurement and Characterization

Figure 2.10 shows the I-V characteristics of the Schottky diodes with Ti/Mo/Cu, Ti/Co/Cu and Ti/W/Cu, structures as deposited and after annealing at 200 °C for 2 min. Applying thermionic emission theory and considering series resistance, the I-V characteristic of the Schottky diode can be expressed as:

$$J = J_0\left[\exp\left(\frac{q(V - JRA_{eff})}{nkT}\right) - 1\right].$$

2.1

where saturation current density $J_0=A^*T^2exp(-q\Phi_b /kT)$, q is the electron charge, V is the applied voltage, R is the series resistance, A_{eff} is the effective area of the Schottky diode, k is the Boltzman constant, T is the absolute temperature, A^* is the effective Richardson constant of 8.0375 A $cm^{-2}K^{-2}$ for GaAs, Φ_b is the barrier height and n is the ideality factor. All the ideality factors and barrier heights were calculated within the current range of $0.01mA/mm^2$ to $0.0001mA/mm^2$.

Before the annealing treatment, the ideality factors and barrier height were 1.11/0.76 eV, 1.15/0.78 eV, 1.11/0.7 eV and 1.11/0.77 eV; after annealing at 200 °C for 2 min, the values became 1.09/0.77 eV, 1.05/0.92eV, 1.12/0.73 eV and 1.05/0.69 eV for Ti/Pt/Au, Ti/Co/Cu and Ti/Mo/Cu, Ti/W/Cu structures, respectively. The ideality factor and the Schottky barrier height remained fairly stable after annealing at 200 °C for each structure. The barrier heights after annealing fell in the range of 0.7 eV to 0.9 eV, which is in the same range as the data reported by Seghal [2].

As shown in Figure 2.11, for each diode structure at the same applied forward voltage, the diode current decreased after annealing at 200 °C for 2 min. The Ti/Co/Cu structure shows the most serious degradation (59.0 % at 0.7 V), whereas the Ti/W/Cu structure has little change in current (17.2 % at 0.7 V) after annealing treatment. The different characteristics of the I-V curves for each Schottky diode are due to the different material structures and the related series resistances of the diodes. In order to extract the series resistance of each diode from the I-V curve, a method proposed by Cheung [3] is used. Rearranging and differentiating Eq. 2.1, we can obtain

$$\frac{d(V)}{d(\ln J)} = RA_{eff}J + \frac{nkT}{q}. \qquad 2.1$$

The slope of the line of $d(V)/d(\ln J)$ vs. J is equal to RA_{eff}. Thus, we can easily determine R by Eq. (2). Figure 2.8 shows the plot of $d(V)/d(\ln J)$ vs. J of the Schottky diodes. The series resistances calculated are 39.92 Ω, 43.72 Ω, 57.41 Ω and 60.74 Ω for Ti/Co/Cu, Ti/Mo/Cu, Ti/W/Cu and Ti/Pt/Au as-deposited structures, respectively. From the data of the resistance, all the three Cu-metallized Schottky structures have lower series resistance than the conventionally used Ti/Pt/Au structure.

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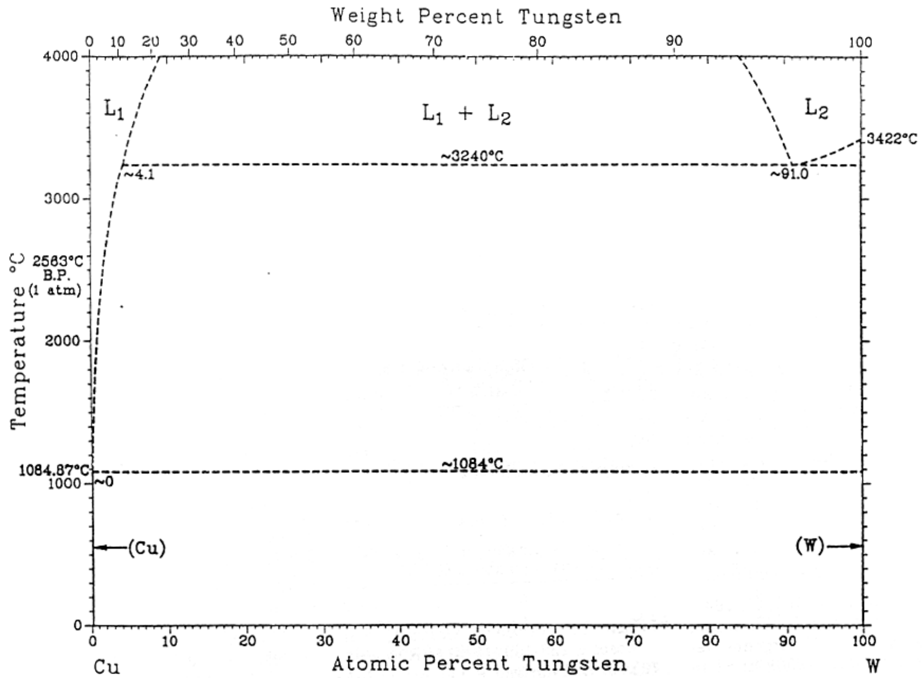
TABLES

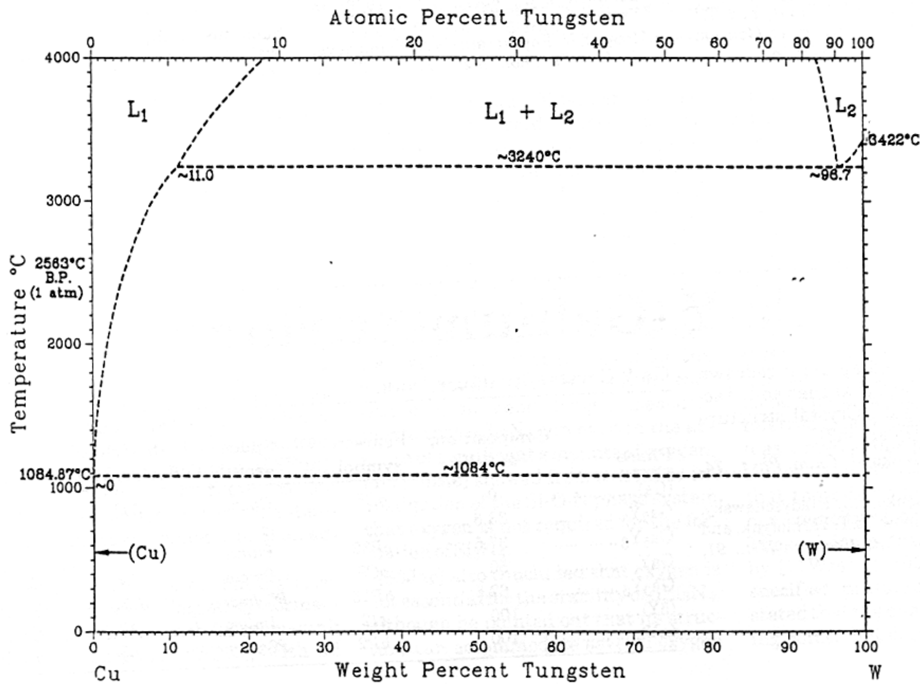
Schottky structure / Annealing Temperature (°C)	Ti/W/Cu	Ti/Mo/Cu	Ti/Co/Cu
200	Stable	Stable	Stable
300	Stable	Stable	Stable
400	Intermetallic compounds formed	Intermetallic compounds formed	Intermetallic compounds formed
500	Intermetallic compounds formed	Intermetallic compounds formed	Intermetallic compounds formed

Table 2.1 Summary of the XRD results for Ti/W/Cu, Ti/Mo/Cu and Ti/Co/Cu Schottky structures after annealing at 200 °C ~500 °C for 30 min.

FIGURES

Cu-W Phase Diagram



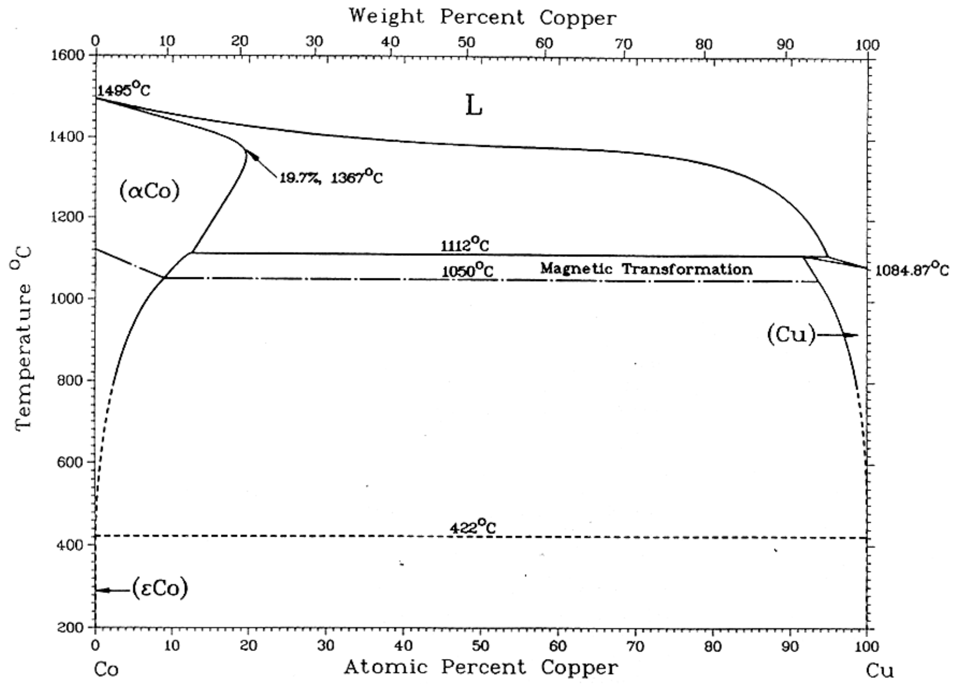


At pressure sufficient to maintain all phases in condensed form.

P.R. Subramanian and D.E. Laughlin, submitted to the APD Program.

Figure 2.1 Cu/W phase diagram. [1]

Co-Cu Phase Diagram



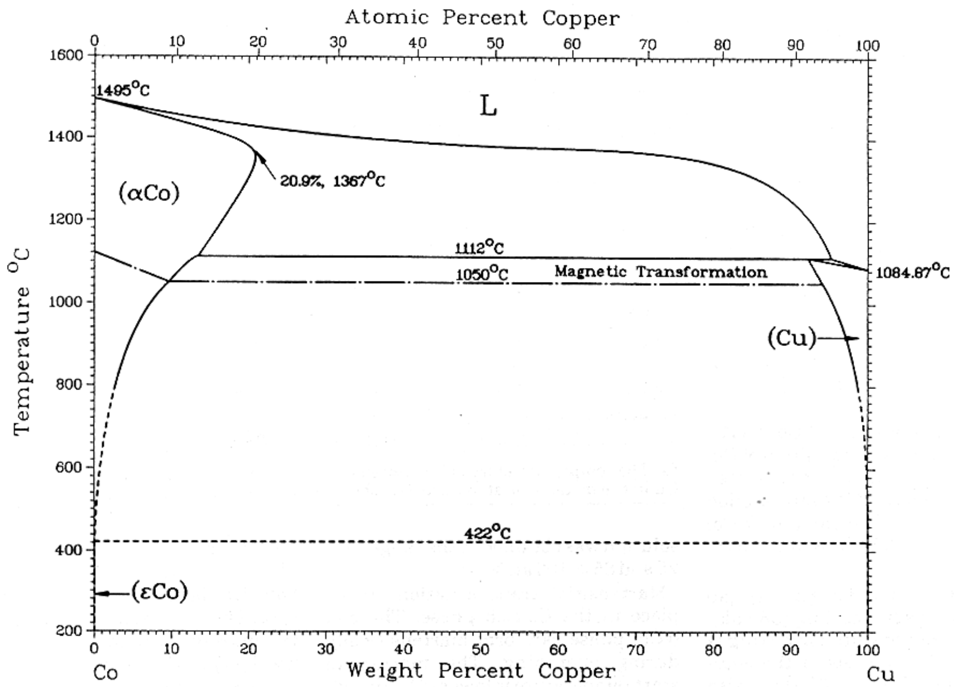
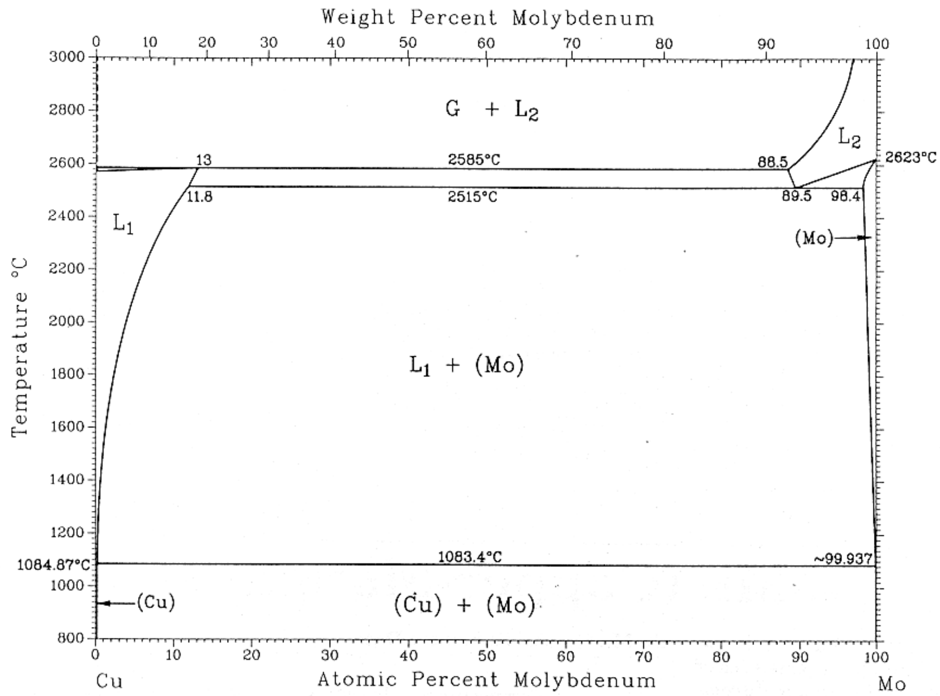
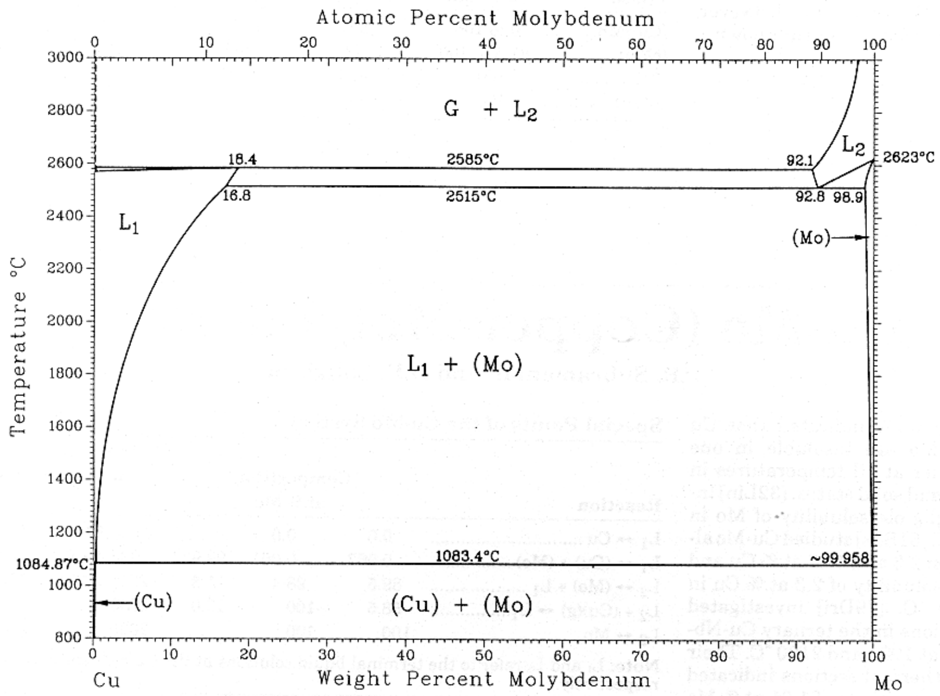


Figure 2.2 Cu/Co phase diagram.[1]

Cu-Mo Phase Diagram

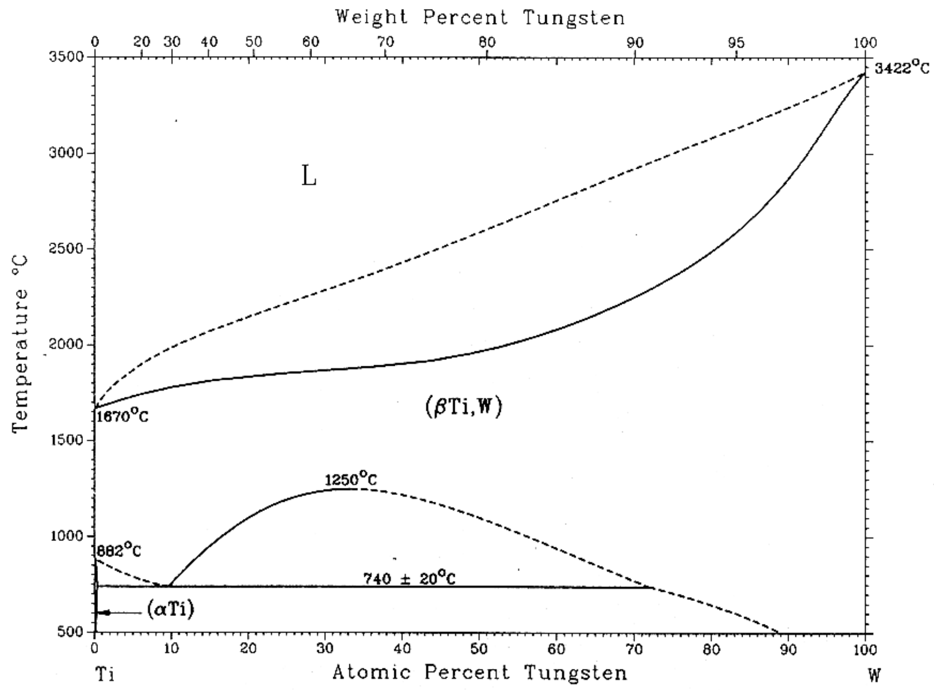




P.R. Subramanian and D.E. Laughlin, 1990

Figure 2.3 Cu/Mo phase diagram. [1]

Ti-W Phase Diagram



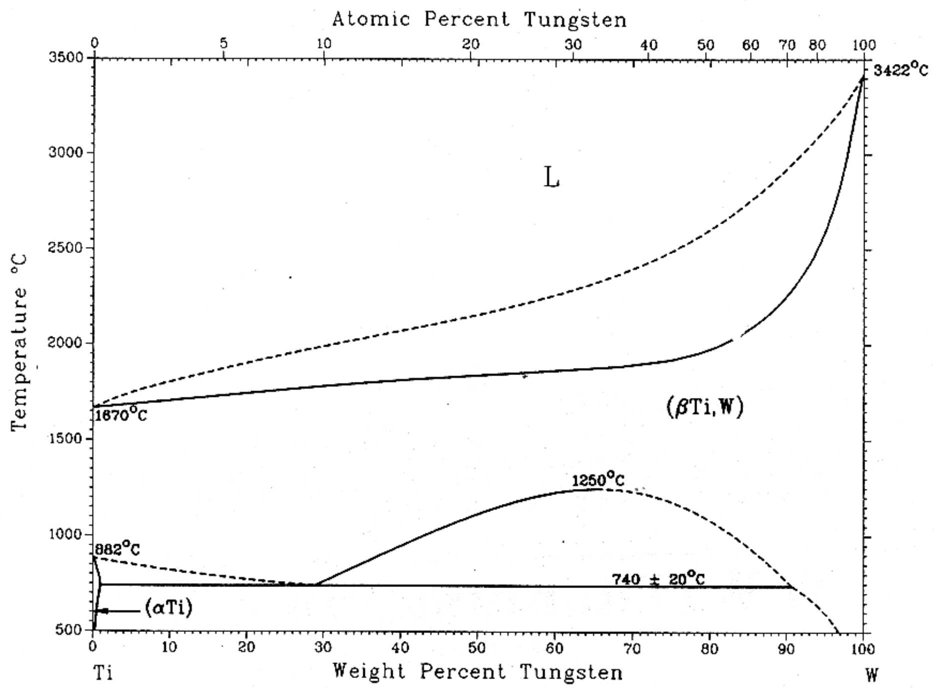
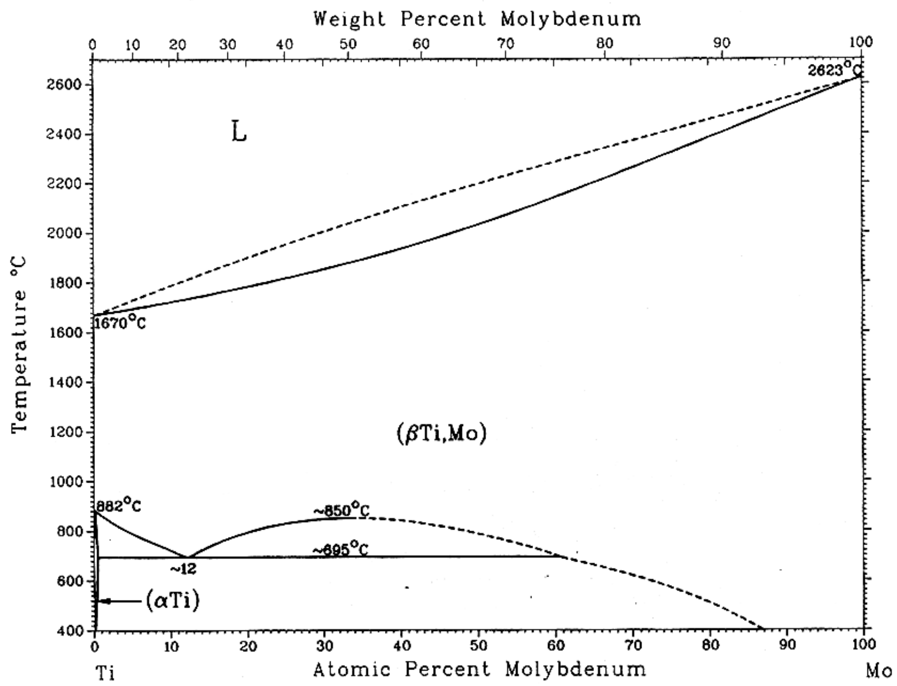
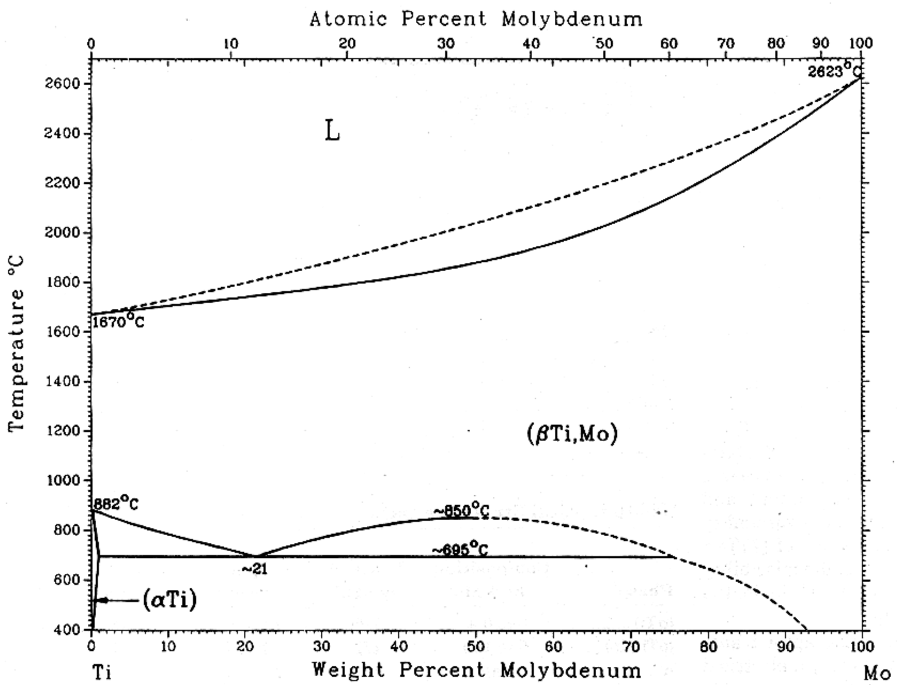


Figure 2.4 Ti/W phase diagram. [1]

Ti-Mo Phase Diagram

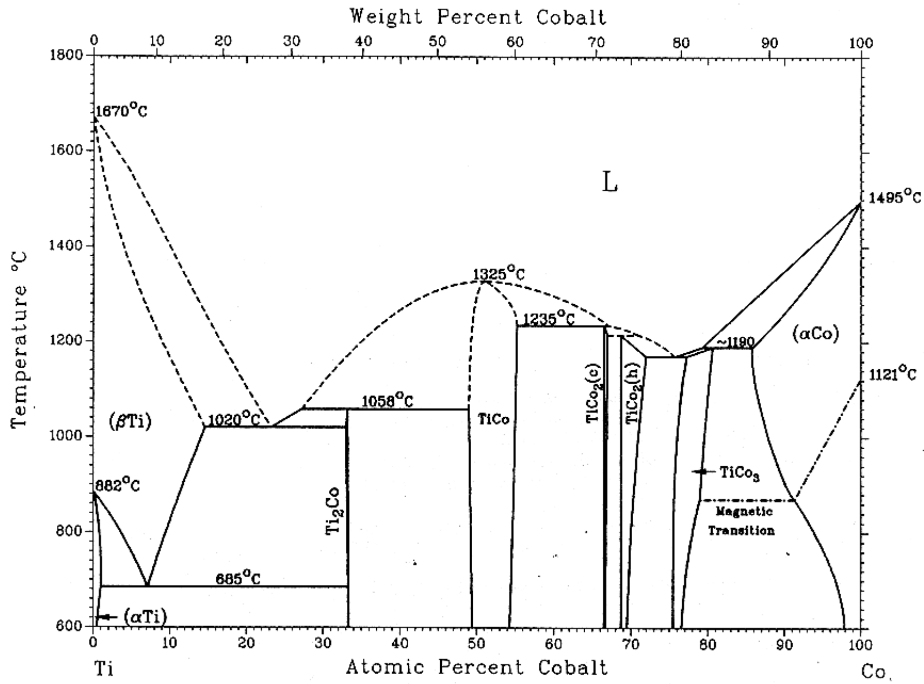


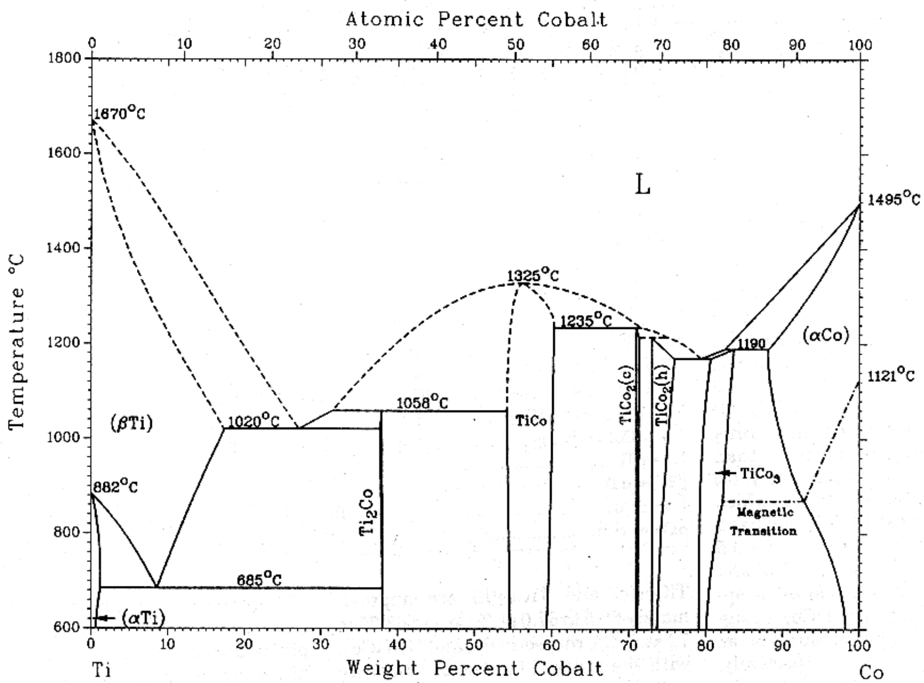


J.L. Murray, 1987.

Figure 2.5 Ti/Mo phase diagram. [1]

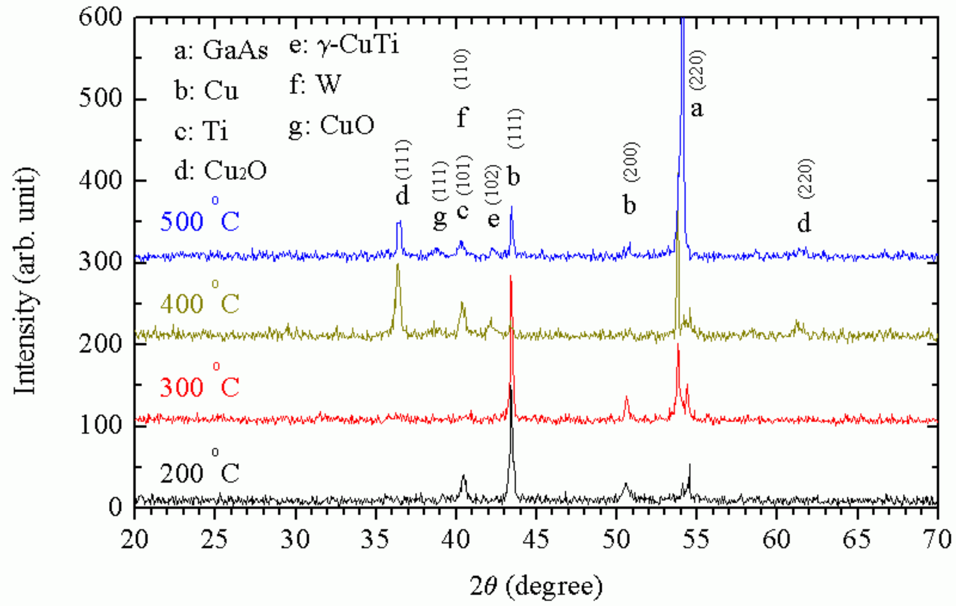
Ti-Co Phase Diagram





J.L. Murray, 1987.

Figure 2.6 Ti/Co phase diagram. [1]



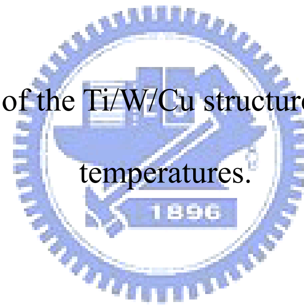
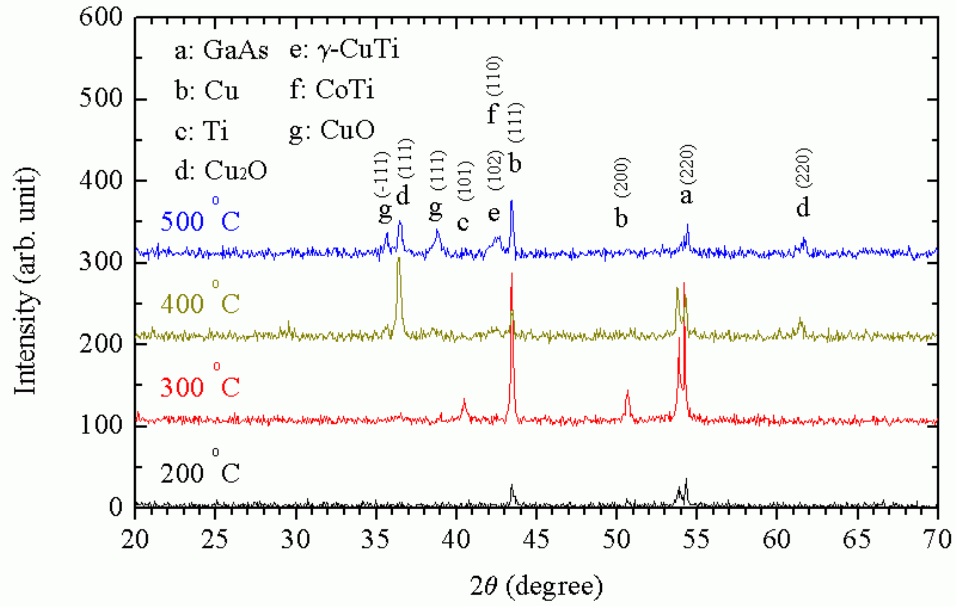


Figure 2.7 XRD results of the Ti/W/Cu structure after annealed at various temperatures.



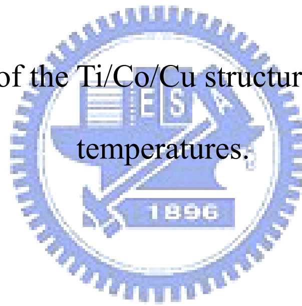
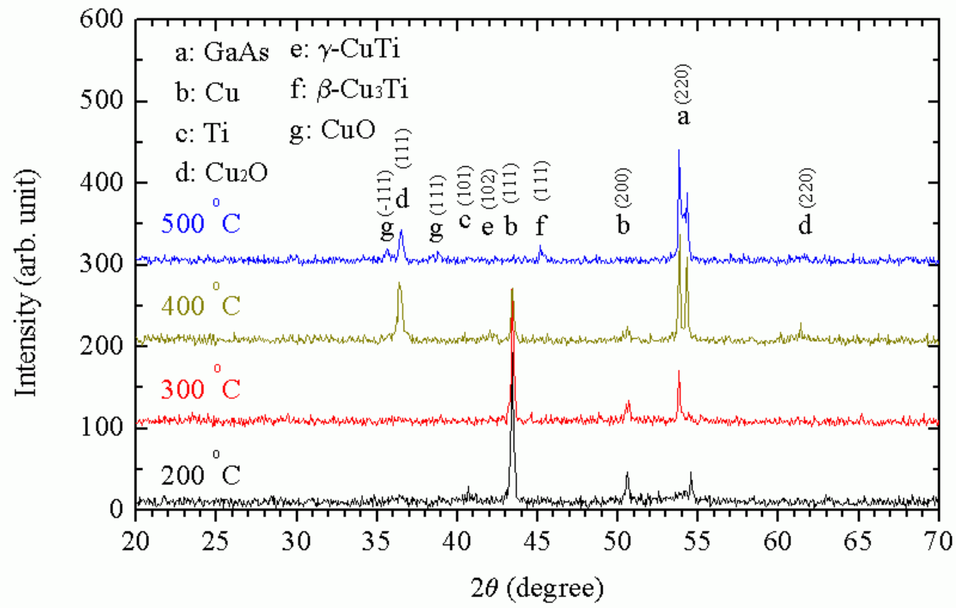


Figure 2.8 XRD results of the Ti/Co/Cu structure after annealed at various temperatures.



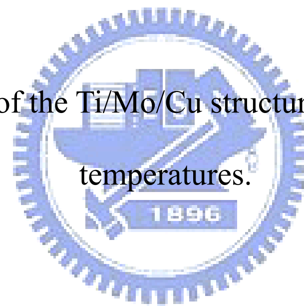


Figure 2.9 XRD results of the Ti/Mo/Cu structure after annealed at various temperatures.

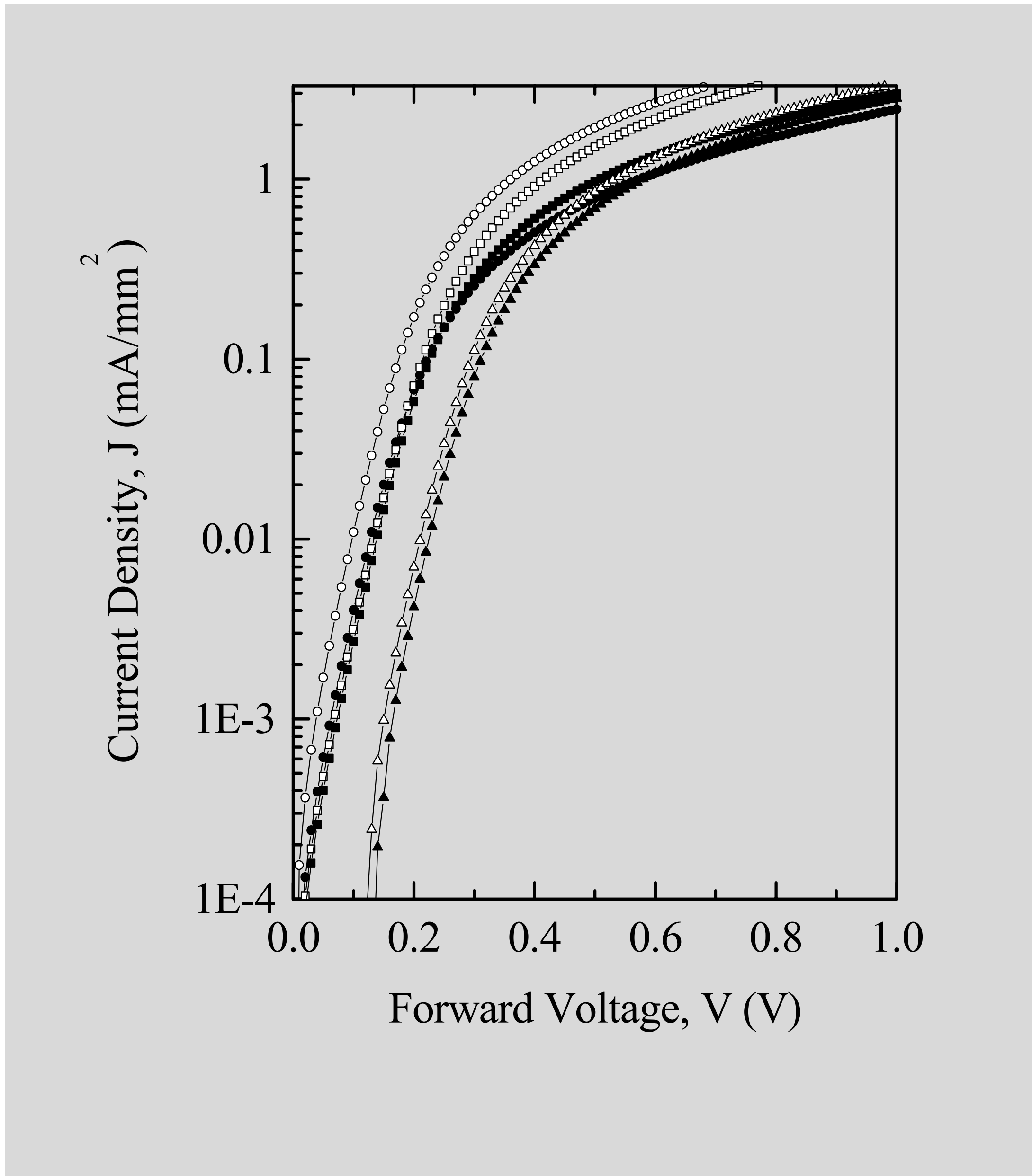


Figure 2.10 Forward I-V characteristics of Ti/W/Cu, Ti/Mo/Cu and Ti/Co/Cu structures as deposited and after annealing at 200 ℃ for 2 min

—○— Ti/Co/Cu (as deposited)

—□— Ti/Mo/Cu (as deposited)

—△— Ti/W/Cu (as deposited)

—●— Ti/Co/Cu (annealing at 200℃, 2min)

—■— Ti/Mo/Cu (annealing at 200℃, 2min)

—▲— Ti/W/Cu (annealing at 200℃, 2min)

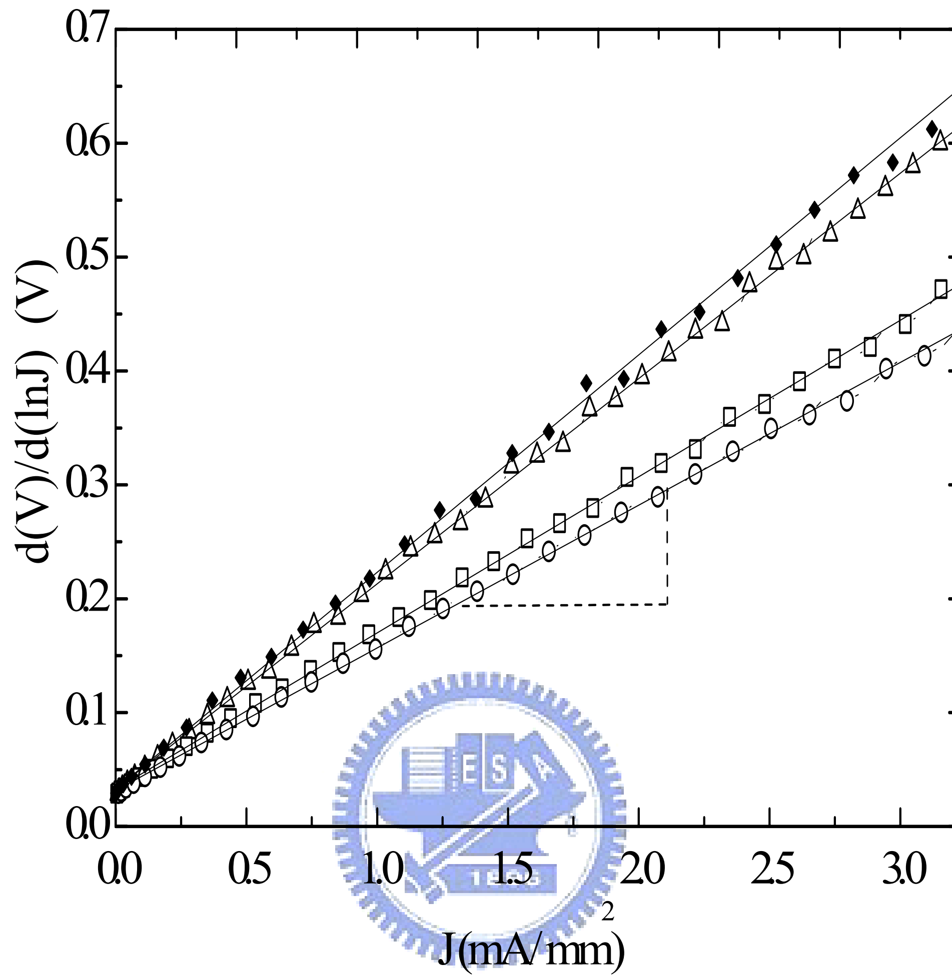


Figure 2.11 Plot of d(V)/d(lnJ) vs. J. The series resistances of the Ti/W/Cu, Ti/Mo/Cu, Ti/Co/Cu and Ti/Pt/Au Schottky structures is proportional to the slope of the fitted line

——◆—— Ti/Pt/Au (as deposited)

——△—— Ti/W/Cu (as deposited)

——□—— Ti/Mo/Cu (as deposited)

——○—— Ti/Co/Cu (as deposited)

———— Linear fitting

Chapter 3

Fabrication of Low Noise GaAs PHEMT

3.1 Pseudomorphic High Electron Mobility Transistor (PHEMT) Device Structure

PHEMT was used to evaluate the feasibility of using the Cu metallized airbridges as the interconnect metal for GaAs-based devices. AlGaAs/GaAs HEMTs were used in microwave and millimeter-wave low noise amplifier due to their superior noise performance at these frequencies in 1980's [1]. However, AlGaAs/GaAs HEMTs suffer from a low current level due to the limited sheet concentration which is lower than 10^{12} cm^{-2} and lower electron transportation characteristics. At the late 1980's, AlGaAs/InGaAs pseudomorphic HEMT with better performance was used to replace AlGaAs/GaAs HEMT as the major device used for low noise application. The larger band discontinuity and better transport characteristics in AlGaAs/InGaAs system result in higher two-dimension electron gas (2DEG) concentration with higher electron mobility and current density.

In this study, the AlGaAs/InGaAs low noise PHEMT was used and the device was grown by molecular beam epitaxy (MBE) on a 3-inch (100) oriented semi-insulating GaAs substrate. The structure is as shown in Figure 3.1. The epi-layers of the device, from the bottom to the top, are composed of a 600nm buffer, a 15nm InGaAs channel, a 2nm undoped AlGaAs spacer, a 42nm Si-doped AlGaAs donor layer and a 45nm Si-doped GaAs capping layer.

3.2 Device Process Flow

The following process flow was used to fabricate PHEMT used in this study.

1. Device Isolation (Section 3.3)

2. Ohmic contact formatin (Section 3.4)

3. Gate formation (Section 3.5)

4. Device passivation (Section 3.6)

Device passivation was followed by airbridge process. Airbridge process is not included in this flow and will be described in the following chapter.

3.3 Device Isolation

Device isolation is the first step for the PHEMT device process. There are three principal ways used to achieve device isolation: mesa etching, ion bombardment, and selective implantation [2]. In this study, mesa etching was used as the device isolation process.

Isolation confines the electrically conductive portion of the wafer to specific areas and restricts the current flow in the undesired areas. For the discrete devices such as the LN-PHEMT used in this study, this usually means that the bonding pads are formed on "inactive" electrically insulating areas.

Device fabrication started from the mesa isolation using wet etching to remove the materials from the undesired areas and form the active device mesas. This process was performed by immersion etching of the undesired areas in the HF-based solution. The active areas were masked by Shipley S1818 photo resist. The inactive areas were etched to the undoped GaAs buffer layer to provide the isolation between devices. In order to avoid the photo resist peeling during the etching of HF-based solution, the wafer surface was pre-treated before resist coating by Hexamethyldisilazane (HMDS) vapor at 150°C for 3 minutes and 30 seconds to improve the resist adhesion on the

substrate. The cross-section of the substrate after mesa isolation is shown in Figure 3.2a.

3.4 Ohmic Contact

There are two kinds of metal contacts on the PHEMT: one is ohmic contact, which forms the source and the drain electrodes, and the other is Schottky contact, which forms the gate electrode. The ohmic contact should have a linear I-V characteristic with a resistance as small as possible, and should be thermally stable.

The patterning of the ohmic metal depends on the photolithography process. Although lithography techniques are quite mature in Si industry, lithography process in GaAs processing is quite different. There are two basic metal patterning process: one is the metal etch mask process typically used in Si process. The other is the lift-off process commonly used in GaAs industry. There are some reasons for such difference. Firstly, GaAs substrate will be attacked by many metal etchants. Secondly, aluminum, which can be easily etched in relatively innocuous etchant and can also be easiliy etched by dry etch techniques, is used by Si processing as the metallization metal. Meanwhile, GaAs uses AuGeNi as Ohmic metal and TiPtAu as Schottky metal. These composite metal systems cannot be easily etched by a simple solution or dry etch techniques. In this study, lift-off process was also used for the Ohmic and Schottky metallization processes.

Karl Suss MJB3 contact aligner with xenon-mercury lamps was used as the photolithography equipment for the patterning of Ohmic metals. Xenon-mercury lamp emits deep ultraviolet (DUV) light with the wavelength in the 220-240 nm range. Glass is highly absorptive at these wavelengths, so quartz masks were employed. In this work, polymethylmethacrylate (PMMA) and its copolymer with polymethacrylic

acid (PMAA) were used as the resists for the lift-off process.

The lift-off process is illustrated in Figure 3.3. The copolymer of PMMA-PMAA was coated on the substrate firstly and then baked at hot plate at 120 °C for 90 seconds. PMMA was subsequently coated and the wafer was again hotplate-baked at 170 °C for 90 seconds. The resist is then exposed by DUV light source. Because the different light sensitivities of PMMA and PMMA-PMAA, the remaining resists formed lift off profile after exposure and development. HCl-based solution was used as the pre-metallization cleaning solution to remove the native oxide of the GaAs surface before Ohmic metallization. The Ohmic metals used were Au/Ge/Ni/Au. After metal deposition, the resist was lifted off and Ohmic metals were formed at the desired areas.

The most common method of forming Ohmic contacts on n-type GaAs is to apply an appropriate metallization scheme to the heavily doped GaAs followed by annealing process. During the annealing process, one of the constituent metals diffuses into the wafer and dopes the cap GaAs layer heavily. Many kinds of alloying systems for n-type ohmic contacts have been studied in literature. In this study, AuGe alloys were used to form the Ohmic contacts.

The Ohmic metals deposited, from the bottom to the top, were Au, germanium, nickel and Au. In the study, germanium atoms diffused into the GaAs and heavily doped GaAs during the thermal annealing process. The Au on the top is usually quite thick, this is for reducing the sheet resistance of the electrodes.

After the AuGeNiAu metallization, the contact resistance was measured by using transmission line model (TLM). The optimized conditions for thermal alloying is 400 °C for 30sec by rapid thermal annealing (RTA) method. The cross-section of the Ohmic metallization after thermal treatment is shown in Figure 3.2b.

3.5 Gate Formation

Short gate length with low gate resistance is desirable for HEMTs for high frequency and high speed applications. The most common approach for obtaining low gate resistance is the use of T-shaped gate structure. For T-gate structure, the small footprint defines the gate length and the wide top provides a low gate resistance. T-shaped gates were achieved by using a multilayer resist technique with E-beam lithography. In this study, PMMA/PMMA(MAA) were used as the resist system to form the T-shaped gates. The fabricated PHEMT in this study has a gate length of 0.25 μm.

After the gate resist development, the exposed HEMT channel was recessed to achieve the desired channel current and pinch-off voltage characteristics. That means a groove is fabricated in the exposed surface of the wafer to "recess" the gate. This process is done by wet etch technique in this study, although dry etching methods may also be used. The schematic of the HEMT with recessed gate is as shown in Figure 3.4. The gate recess profile in this study was achieved by using e-beam lithography. In such case, the opening in the PMMA-MAA layer determines the gate length; the opening of the top PMMA layer determines the width of the top portion of the T-shaped gate.

The method used to control the recess depth is to monitor the source-to-drain current during the etching process. For low noise PHEMT, the saturation current and the slope of the linear region go down as the recess groove was etched deeper and deeper. The concentration of the etchant should be adjusted to provide an etch rate that is sufficiently slow to allow good control over the recess process, thus enable the operation to approach the target current value, without overetching it. Several recess etchants were considered and tried. However, citric acid/hydrogen peroxide solution

was used because of the good process control. The wet etchant usually leaves a thin oxide on the GaAs. HCl-based solution was used to remove the surface oxide.

After gate recess process, the wafer was cleaned in the solution of $HCl:H_2O=1:10$ solution to remove the native oxide formed on the exposed wafer surface, and the gate metal Ti/Pt/Au was evaporated by E-gun evaporation. After the gate metal was formed, DC characteristics were measured. The cross-section of the HEMT after gate metallization and lift-off process is as shown in Figure 3.2c.

3.6 Device Passivation

Plasma enhanced chemical vapor deposition (PECVD) nitride was used on the sample for surface encapsulation. The major purpose of the silicon nitride protective encapsulation is simply for the surface passivation. This passivation protects the critical area of the originally exposed wafer surface from humidity, chemicals, gases, and particles. The reason why silicon dioxide was not used as the passivation dielectrics in this study is that silicon nitride is less permeable to ions than silicon dioxide, therefore the silicon nitride is relatively reliable material for device passivation.

In this study, Samco PECVD system was used for depositing silicon nitride film. The processing gases of passivation PECVD were Silane, ammonia, and nitrogen. The process condition is: process pressure: 100Pa, process temperature: 250 $^{\circ}$C and process time: 6 minutes and 30 seconds.

Passivation Vias between Au contacts and airbridge interconnects were etched by reactive ionic etcher (RIE). This process used the Plasmatherm RIE system and the etching condition was: gas pressure: 60 mT, RF power: 50 W, etching gases: CF_4/O_2, process time: 1 minute and 40 seconds and the etching depth: 1000 Å film. The DC

performances of the unfinished device with single gate finger were measured by HP4142 for preliminary device evaluation before the interconnect process. The schematic of the device after passivation and via opening is as shown in Figure 3.2d.

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FIGURES

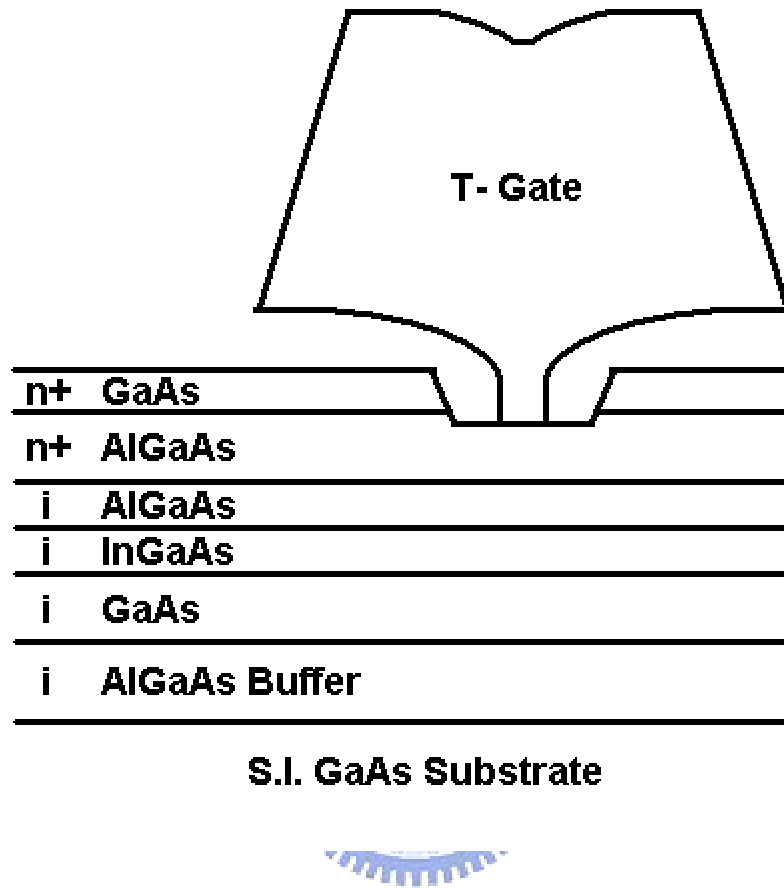
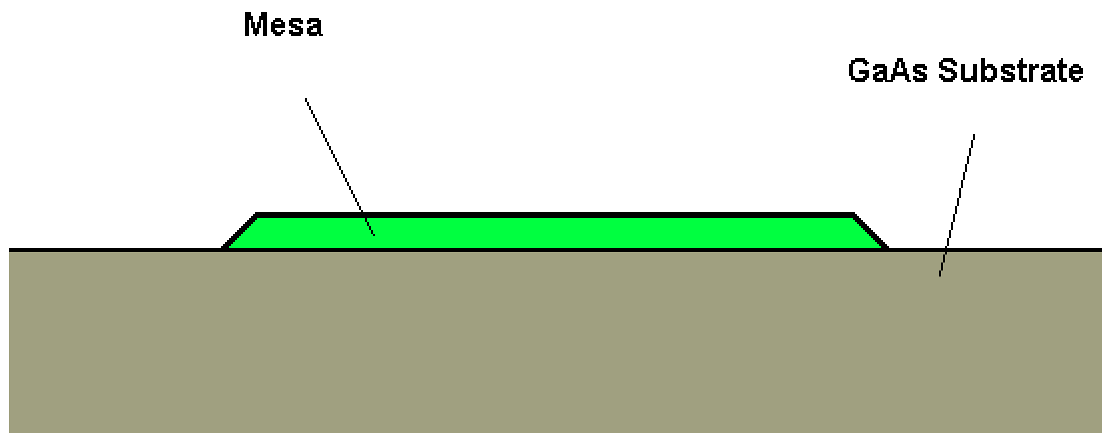


Figure 3.1 Structure of the AlGaAs/GaAs LN-PHEMT



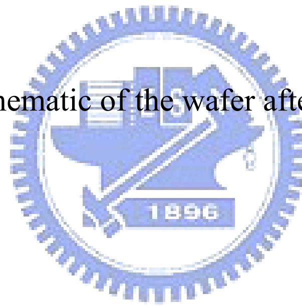


Figure 3.2a Schematic of the wafer after mesa isolation.

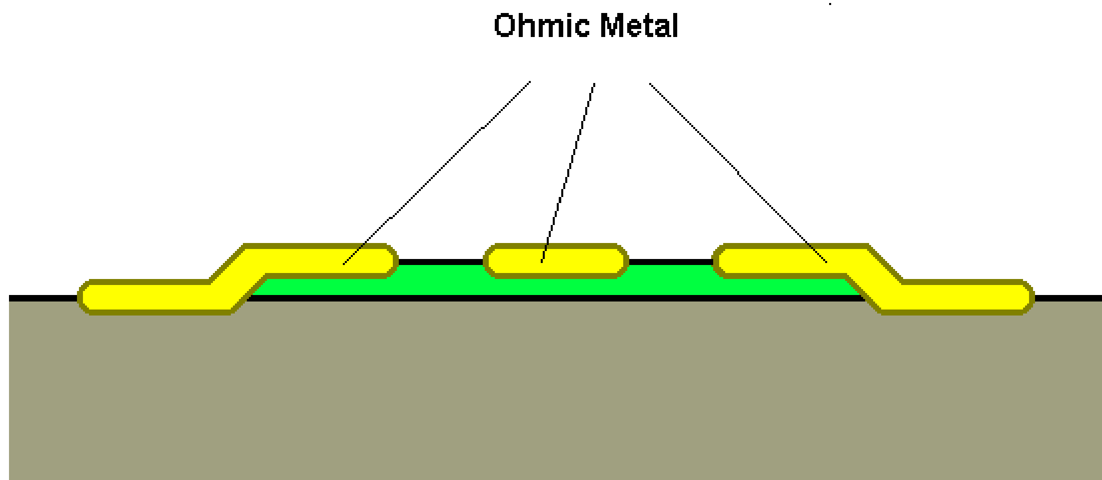


Figure 3.2b Schematic of the Ohmic contact formation on the GaAs wafer

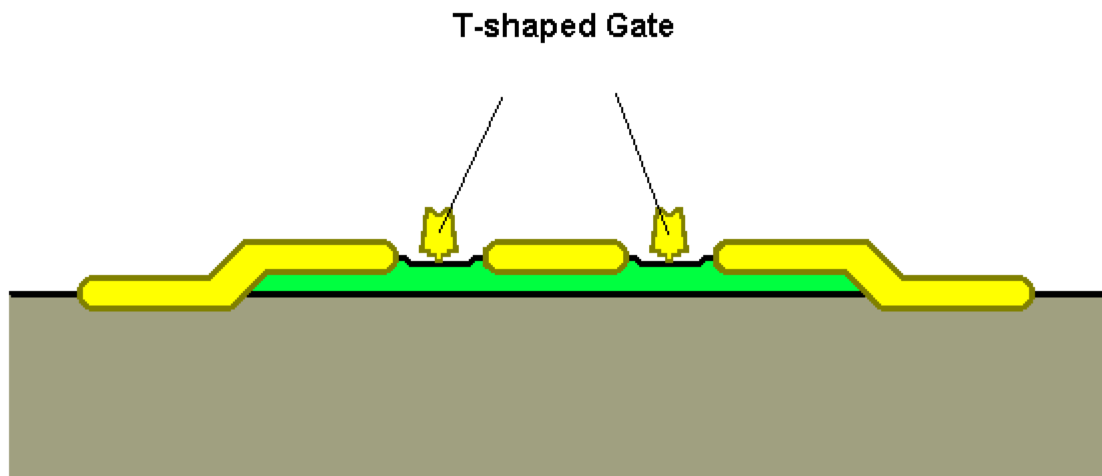


Figure 3.2c Schematic of the cross section of HEMT after gate metallization

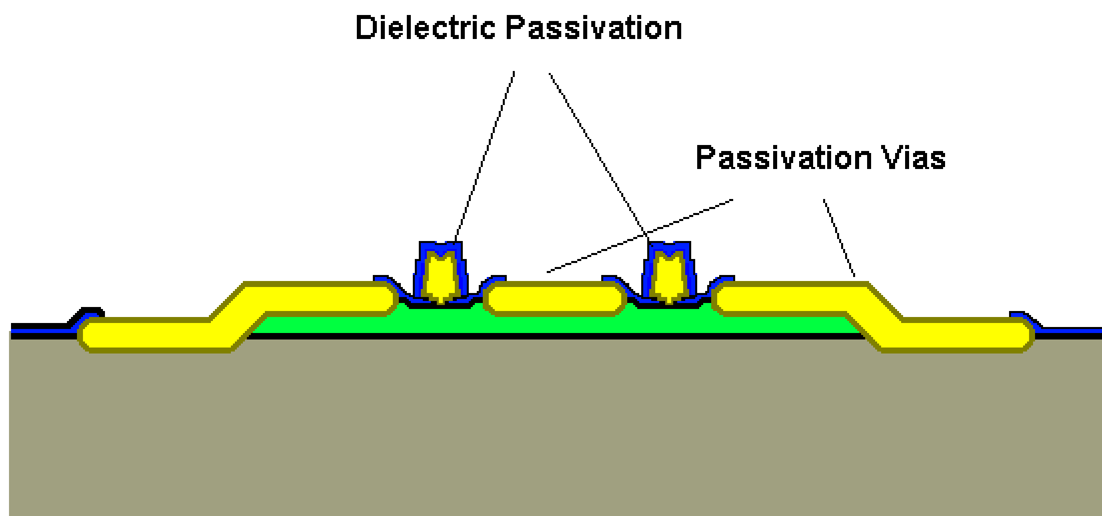


Figure 3.2d Schematic the GaAs wafer after passivation and nitride via RIE

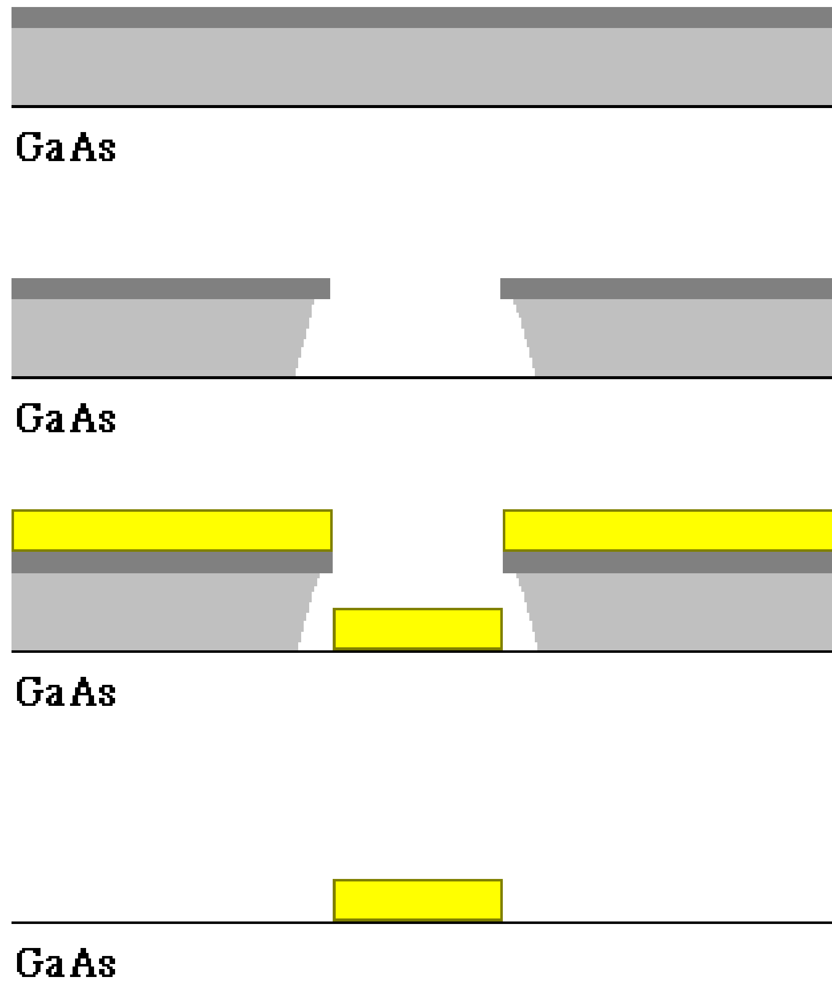


Figure 3.3 Schematic of the lift-off process for ohmic metallization formation.

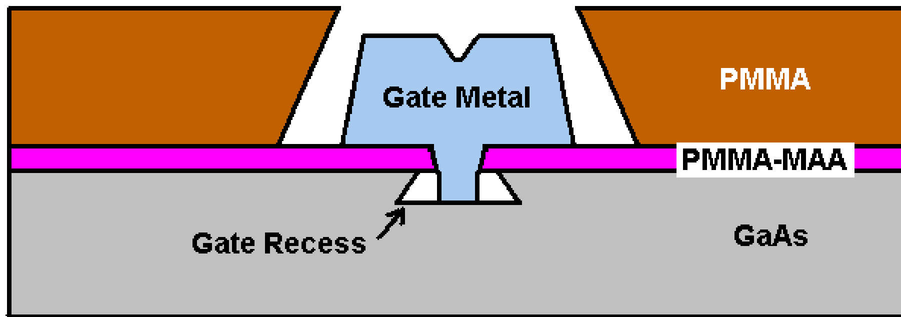


Figure 3.4 Schematic of the HEMT after recess and gate deposition, but before PMMA/PMMA-MAA lift off.

Chapter 4
Technology Development of the Cu-Metallized Airbridges

4.1 Overview

A metal interconnects with air between the metal interconnect and the wafer surface beneath is called an airbridge. Airbridges are used extensively in GaAs analog devices and MMICs for interconnections [1]. They may be used to interconnect sources of FETs, to cross over a lower level of metallization, or to connect the top plate of a MIM capacitor to adjacent metallization. The airbridges have several advantages including low parasitic capacitance, and the ability to carry substantial currents if the plated airbridge is thick enough.

Analog GaAs devices operating at high current density benefit from airbridges with thick plated metal layer. Low parasitic capacitance (between the bridge and any metallization beneath) follows from the large spacing and low dielectric constant of the intervening medium. The capacitance is a function of the thickness, and the dielectric constant of the intervening material. Air (k=1.0) has a much lower dielectric constant than any other dielectric, and the space under the airbridge tends to be greater than the thickness of typical dielectrics. These considerations mean that airbridge crossovers are less capacitive than the dielectric type by a factor (typically) of five to twenty.

Traditionally, Au is used as the interconnect metal in III-V device fabrications, mainly owing to its high electrical conductivity and better chemical inertness with no surface oxidation. Recently Cu has been used widely in Si IC interconnects due to its low resistivity and high electromigration resistance. Both the resistivity and the material cost of Cu (1.67 $\mu\Omega$-cm) are lower than those of Au (2.2 $\mu\Omega$-cm). Based on

the above advangages, Cu were used instead of Au as the airbridge metal in order to provide better thermal and electrical conductivities for the device applications.

4.2 Comparison between Au Airbridge and Cu Airbridge Processes

The process flow of airbridges used in this study is as shown in Figure 4.1. There are three main differences between the fabrications of Au airbridges and Cu airbridges: thin metal structure, electroplating and airbridge passivation.

Ti/Au/Ti structure is widely used as thin metals of Au airbridge interconnect in conventional GaAs MMIC industry. Ti layers are used as the adhesion layer between Au and photo resist. Besides, the top Ti layer confines the electroplating area and thus prevents the electroplated Au from intruding into the areas that is originally covered by photo resist. The Au layer between two Ti layers is used as the seed layer for Au electroplating.

The thin metals used for Cu-metallized airbridges on Au contacted PHEMT must prevent Cu atoms from diffusing into the Au layer. On the other hand, the adhesion of such metal system must be good enough to prevent metal peelings. Finally, Cu-metallized PHEMTs that use such a thin metal structure must have comparable, or even better electrical performance compared with the Au-metallized PHEMTs.

The seed layers for electroplating of these two airbridges are different. Evaporated Au was used as the seed layer for electroplated Au whereas the electroplated Cu used sputtered Cu as the seed metal. Cyanide-based solution was used for Au electroplating in this study. The environment of Au electroplating is tough on photo resist because the process temperature is up to 65 ˚C, which may has the risk for suffering photo resist deformation and dissolution in the electroplating solution. Compared to Au electroplating, Cu electroplating has several advantages. Cu

electroplating is less expensive, less toxic than the cyanide-based electroplating of Au. Cu electroplating of sulfuric acid system can be done at room temperature. Therefore, the photo resist can sustain of a longer process time in Cu electroplating solution than in Au electroplating solution.

4.3 Thin Metal Structure Used for Cu Airbridges on PHEMTs fabricated with Au-Metallized Contacts

Cu is one of the most common unintentional impurities in semiconductor including GaAs. It diffuses rapidly at low temperatures by interstitial diffusion process [2]. In GaAs, Cu tends to getter on to crystalline defects and acts as a double acceptor, being incorporated at a substutional lattice site as a Cu_{Ga} [3].

Au used in microelectronics is highly pure, usually 99.99% or better. One reason for the requirement of high purity Au is the rapid increase in electrical resistance as a function of impurity concentration. According to the study of Reid [4] in 1974, the resistivity of pure Au is 2.2 $\mu\Omega$/cm. However, 1 at. % of Cu alloyed with Au increases the resistivity up to 3.59 $\mu\Omega$/cm, which is 63.3 % greater than that of pure Au!

Based on these well-known characteristics, Cu is traditionally regarded as harmful to GaAs material and devices. No Cu contaminations to either GaAs or Au are allowed in the traditional PHEMT fabrication. In this study, Cu replaced Au as the metal for airbridge interconnects. In order to avoid the interatomic diffusion of Cu and Au, the diffusion barrier used in this study must be thermally stable to protect the PHEMTs with Au contacts from the Cu diffusion.

From the experiences of Si industry, refractory metal and their nitride could be used as the diffusion barrier to prevent the Cu diffusion into the underlying devices.

The detailed introductions of these refractory metals as the diffusion barriers have been described in Chapter 1. Most of these metal nitrides are thermally stable under the normal operation of GaAs devices. Among these materials, WNx was chosen as the diffusion barrier of Cu metallization upon GaAs PHEMT because of the feasibility of process integration. WNx can be etched by several chemical solutions such as hydrogen peroxide and acid-hydrogen peroxide solution. These solutions were widely used in the fabrication of GaAs devices.

4.3.1 Materials study of WNx as the Diffusion Barrier

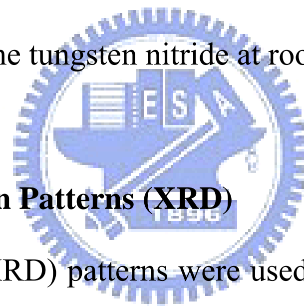
In this study, the thermal stabilities of the thin metal systems WNx/Cu on Au were studied. 400 Å WNx and 1000 Å Cu were sputtered upon the Au layer on the GaAs blanket wafers. These wafers were subsequently splitted up to four groups. Three of them were separately annealed at 350 °C, 400 °C and 450 °C for 30 minutes under nitrogen atmosphere. Auger Electron Spectroscopy (AES) and X-ray Diffraction Pattern (XRD) were then used for materials analysis of all these four different kinds of samples.

4.3.1.1 AES Depth Profile

Auger Electron Spectroscopy (AES) was used to analyze the depth profiles of Au/WNx/Cu multilayer system. The data acquisition of AES depth profile analysis combines ion beam sputtering yielding in-depth element information.

Figure 4.2a~d show the AES depth profiles of the Au/WNx/Cu multilayer system annealed at different temperatures. From the results of these profiles, the diffusion barrier WNx was thermally stable even up to 350 °C annealing for 30 minutes. When the annealing temperature was 400 °C, the profile of WNx remained changed and the Cu began to diffuse into the WNx layer. Suh [5]

suggested that amorphous WNx films with nitrogen contents of less than 18% would recrystallize when the annealing temperature was up to 450 °C, as shown in Figure 4.3. Interestingly, when the temperature was up to 450 °C, there was still little Cu in WNx but lots of Cu atoms had penetrated WNx and accumulated in the Au layer. The reason why very few Cu atoms were found in WNx could be that the W can dissolve a large amount of Cu atoms at 450 °C but have only limited solubility for Cu atoms at room temperature. When the temperature was increased to 450 °C, Cu atoms penetrate the tungsten nitride layer into the underlying Au layer. However, after the annealing temperatures were slowly decreased to room temperature, Cu atoms which were originally at the tungsten grain boundaries diffused out of the WNx layer into the Au layer because of the limited Cu solubility in the tungsten nitride at room temperature.



4.3.1.2 X-ray Diffraction Patterns (XRD)

X-ray diffraction (XRD) patterns were used to analyze the structures of the Au/WNx/Cu multilayer system after thermal annealing. The XRD patterns of this material system before and after thermal annealing are shown in Figure 4.4. When the annealing temperature was up to 450 °C, Cu started to diffuse into Au layer and formed intermetallic compounds.

4.3.1.3 Summary of the Materials study of WNx/Cu on Au

Compared the XRD patterns and the AES depth profiles, it can be concluded that the generation of these intermetallic compounds was due to that Cu atoms diffused through the WNx layer and formed several kinds of intermetallic compound with Au atoms. These intermetallic compounds have higher resistance than Cu and Au, which impact the RF performance of the

LN-PHEMT.

Although there's no obvious intermetallic compounds formed after 400 °C annealing from the XRD patterns, there exists a certain risk of interatomic diffusions because the AES depth profiles of the Cu and Au atoms showed that Cu and Au atoms started to diffuse into the WNx layer at such a temperature. From the results of XRD and Auger analysis, it can be concluded that WNx was still a good diffusion barrier between Cu and Au even after 350 °C annealing for 30 minutes under nitrogen atmosphere.

4.3.2 Adhesion Layer

At the initial stage of this study, 400 Å WNx and 1000 Å Cu were used as the diffusion barrier for the fabrication of Cu-airbridged GaAs PHEMTs. However, the problems of electroplated-Cu peelings were observed during the airbridge process and the RF measurement. The electrical characteristics of GaAs PHEMTs with WNx/Cu as the thin metal structure also showed an inferior uniformity. Figure 4.5 shows the metal peeling after RF probing and two different colors were observed at the peeling areas on the GaAs PHEMTs. The metal contacts revealed golden color. The color of the areas of nitride, which were originally covered by electroplated Cu, was brown. The nitride areas without any material covering upon it after airbridge process showed the color of light yellow. According to the inspection of this failure, the peeling structure was depicted schematically in Figure 4.6. It seemed that metals peeled between Au and WNx at the area of metal contacts while the peeling occurred between WNx and Cu at the areas of silicon nitride. Based on this assumption, it is necessary to improve the adhesion of WNx on Au and Cu on WNx for the Cu airbridge process.

The Ti/WNx/Ti/Cu multilayer system was used as the thin metal of Cu

airbridges to overcome the metal peeling issues. Two Ti layers of 300 Å thick were added separately under and upon the WNx layer to improve the adhesions. Ti was widely used as the adhesion layer in the semiconductor industry. The adhesion characteristics of Ti were introduced in Chapter 1. Ti was also used in the fabrication of conventional Au airbridges and it can be etched by the diluted hydrogen fluoride solution. The deposition and etching processes of Ti are compatible with the conventional process used in GaAs device fabrications.

Metal peelings no longer occurred on the GaAs PHEMTs fabricated with Ti/WNx/Ti/Cu. GaAs PHEMTs fabricated with different thin metal systems were sampled and the uniformities of the DC characteristics of these devices are as shown in Figure 4.7 and Figure 4.8. The average transconductance of the devices using Ti/WNx/Ti/Cu as thin metals were greater than those of the devices using WNx/Cu. The standard deviations of Gm and Vp of GaAs PHEMTs fabricated with WNx/Cu were 97 mS/mm and 0.22 V, respectively. The standard deviations of Gm and Vp of GaAs PHEMTs fabricated with Ti/WNx/Ti/Cu were 33 mS/mm and 0.14 V, respectively. GaAs PHEMTs fabricated Ti/WNx/Ti/Cu showed better uniformity in Gm and Vp than HEMT fabricated with WNx/Cu layers. The improvement on the RF performance was due to the additional adhesion layers as shown in the following chapter.

4.3.3 Thin Metal Etching

The etching selectivity of the thin metal determines the airbridge profile and metal thickness. Appropriate etchants should be chosen so that these etchants won't overetch the airbridge metal. In the conventional Au airbridge process, KI solution is used to etch the Au layer of the thin metal structure and HF solution is used to etch the Ti layers. The thickness of the thin metal Au is only 500 Å, which is much

thinner than 2 μm-thick electroplated Au. Au doesn't react with HF solution. After the thin metal etching, the thickness of the electroplated Au doesn't change too much and remains about 2 μm. Figure 4.9 shows the SEM photograph of the Au airbridges after thin metal etching.

Several etchants were chosen to etch the thin metals of the Cu airbridge. NH_4OH: H_2O_2: H_2O solution can etch both WNx and Cu and was used as the non-selective etchant of the WNx/Cu metal structure. However, the Cu etching rate is much greater than the WNx etching rate. After the thin metal etch, the Cu airbridge was seriously damaged and there were still some WNx protruding at the edges of the airbridge as shown in Figure 4.10. These WNx protrudings cause the risk of metal short and also the resistive loss of the RF performance. In order to improve the Cu airbridge profile after thin metal etching, it is necessary to develop the selective etching process to remove the thin metals.

In this study, the selective etching was used to etch the Ti/WNx/Ti/Cu multilayer system. The thin Cu metal was etched by $H_2SO_4/H_2O_2/H_2O$ solution mixed in the volume ratio of 5:6:100. Diluted HF solution was used to etch Ti layers and diluted H_2O_2 solution was used to etch WNx layer. Diluted HF solution without mixing with other chemicals didn't etch Cu too much. Although H_2O_2 solution oxidized the Cu surface, the oxidation was only on the surface. After WNx was etched in the H_2O_2 solution, HF solution was used to etch the bottom Ti layer and simultaneously removed the surface oxide of the Cu airbridge. Figure 4.11 shows the SEM photograph of the Cu airbridges after the selective thin metal etching, the bridge metal was not seriously etched and no metal protrudings were observed.

4.4 Cu Electroplating

Although these bridge structures may be fabricated using evaporation rather than plating, plating technique is more economic and widely used. It was reported that the best quality of Cu was achieved by electroplating [6]. The electroplated Cu has the larger grain size with reduced grain boundaries, which has better resistance to electromigration than Cu deposited by evaporation or sputtering.

So far, the popular Cu plating bath in semiconductor industry is sulfuric acid/Cu sulfate based; the function of $CuSO_4 \cdot 5H_2O$ is the source of Cu ions （pure Cu or phosphor Cu on the anode donate Cu ions）; H_2SO_4 will increase the electrical conductivity of the electrolyte and stabilize the concentration variation between cupric and cupreous ions; Cl^- will enhance the deposition of cupreous ions in order to generate better electroplated layers; and the function of electroplating additives is to wet the substrate surfaces and to enhance/inhibit the surface electricity. Besides, coped with the electro-chemical analysis techniques, we can get the on-line data of additives consumption and monitor the solution quality to adjust the process parameters. Selection of additives is one of the critical parts in determining the electroplating solution; suitable additives could enhance the quality, uniformity and filling performance of the electroplated Cu layer.

At present, additives of cupric sulfate electroplating solution could be separated into three categories described as follows:

1. Dispersion agents or carriers (suppressors) ：Able to be adhered or dispersed on the surface of the electroplated substrates, to inhibit the deposition rate, and lower the surface tension of solutions, to raise wetting effect, and to improve the micro-distributing ability.

2. Accelerators：Easy to be absorbed by cathodes, replacing local dispersion agents or carriers, to speed up electroplating rates of certain areas. Meanwhile, it can

also decrease the crystal size and improve the physical properties of electroplated layers.

3. Levelers：It can be absorbed and replace certain carriers and accelerators in specific high-electricity areas. The deposition rate of the area absorbed by the levelers will be dramatically decreased. We can get smooth surface by well controlling the levelers. The best performance can be achieved by well control the ratio of above three kinds of additives (as described in the Figure 4.12) [7].

The metal roughness is one of the major considerations of GaAs metallizations. Ac mutual inductive effects cause ac current to be greatest at the outside surface. Current density decreases exponentially from the surface inward. The larger the surface roughness is, the greater the resistive loss of the transmission line will be when operating at high frequency. Getting the metal surface of interconnect as smooth as possible is important to the RF performance of devices operated at high frequency [8].

Cu-plating bath of the MERCK Company was used in this study. Different electroplating current densities were evaluated and the best electroplating conditions were optimized to get a superior flatness of the Cu-metallized airbridges. The metal thickness and surface roughness of the Cu plated with different electroplating conditions are shown in Table 4.1 and Table 4.2. Figure 4.13 shows the relationship of the metal thickness to the electroplating time. Figure 4.14 shows the relationship of the surface roughness to the electroplating time. These results show that the current density to achieve the best surface flatness was 1 A/dm^2. The process time to get 2.5 μm thick electroplated Cu under the current density of 1 A/dm^2 was 10 minutes.

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TABLE

Current Density	0.5 A/dm^2	1 A/dm^2	2 A/dm^2
7 mins		1.65 μm	3.39 μm
15 mins	1.97 μm	3.1 μm	6.32 μm
30 mins	4.15 μm	6.37 μm	14 μm

Table 4.1 The metal thickness of different Cu electroplating conditions.

Current Density	0.5 A/dm^2	1 A/dm^2	2 A/dm^2
7 mins		46 Å	88 Å
15 mins	182 Å	36 Å	53 Å
30 mins	150 Å	24 Å	134 Å

Table 4.2 The surface roughness of different Cu electroplating conditions.

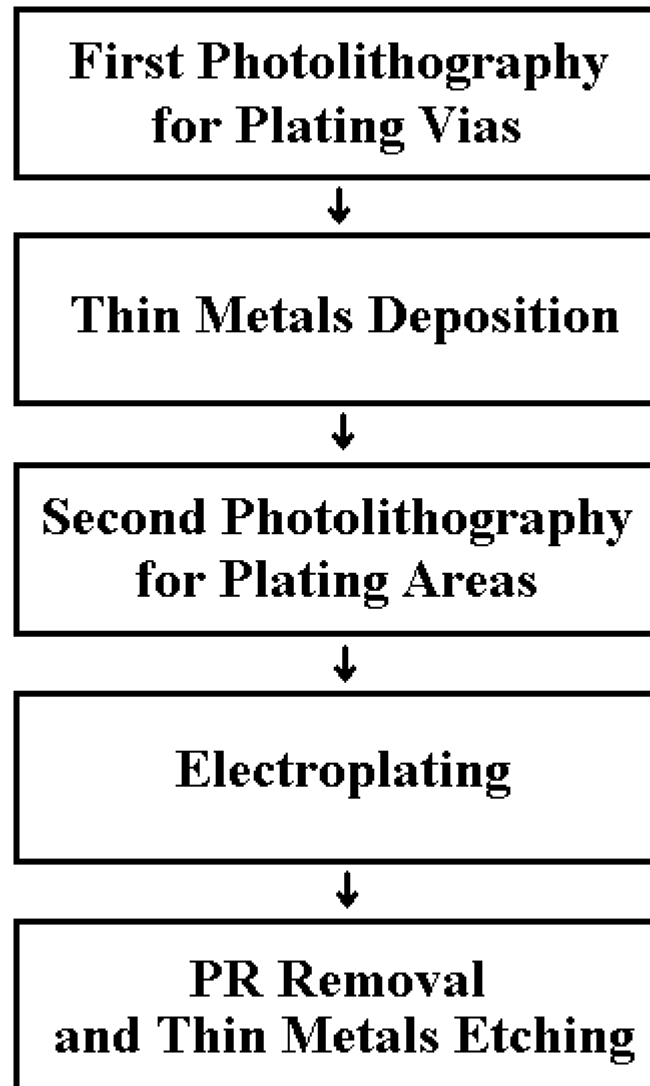


Figure 4.1 Airbridge process flow

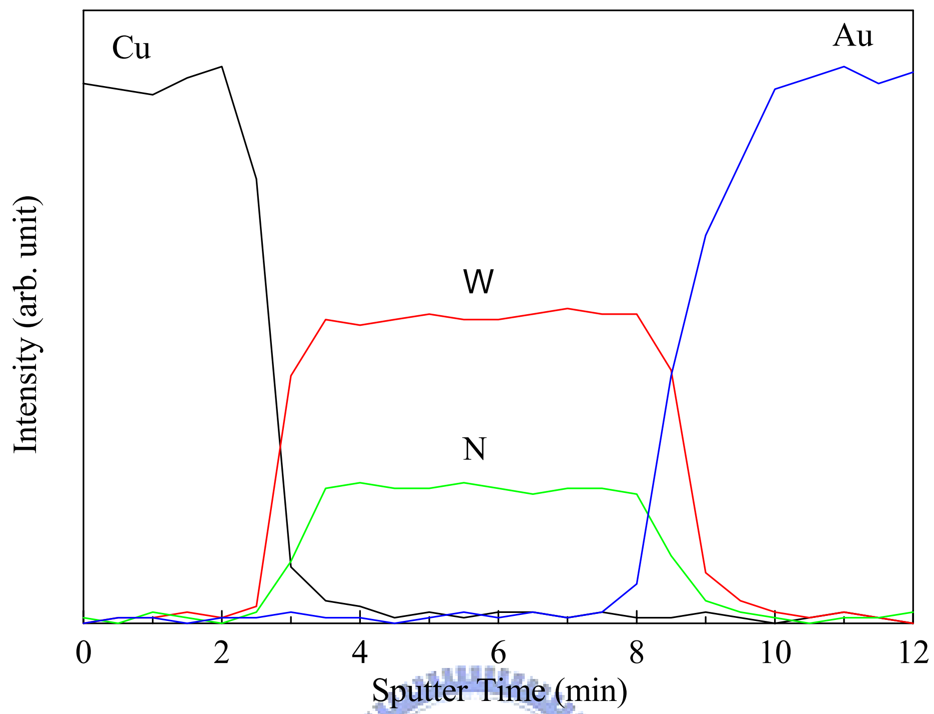


Figure 4.2a AES depth profiles of the as-deposited Au/WNx/Cu multilayer system.

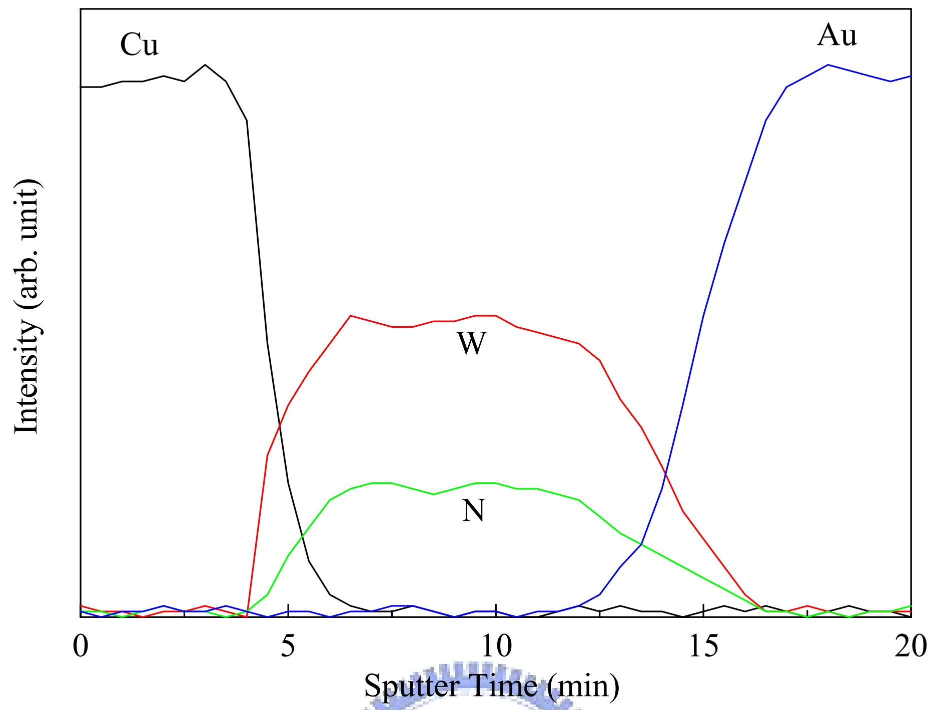


Figure 4.2b AES depth profiles of the Au/WNx/Cu multilayer system after 350°C annealing for 30min.

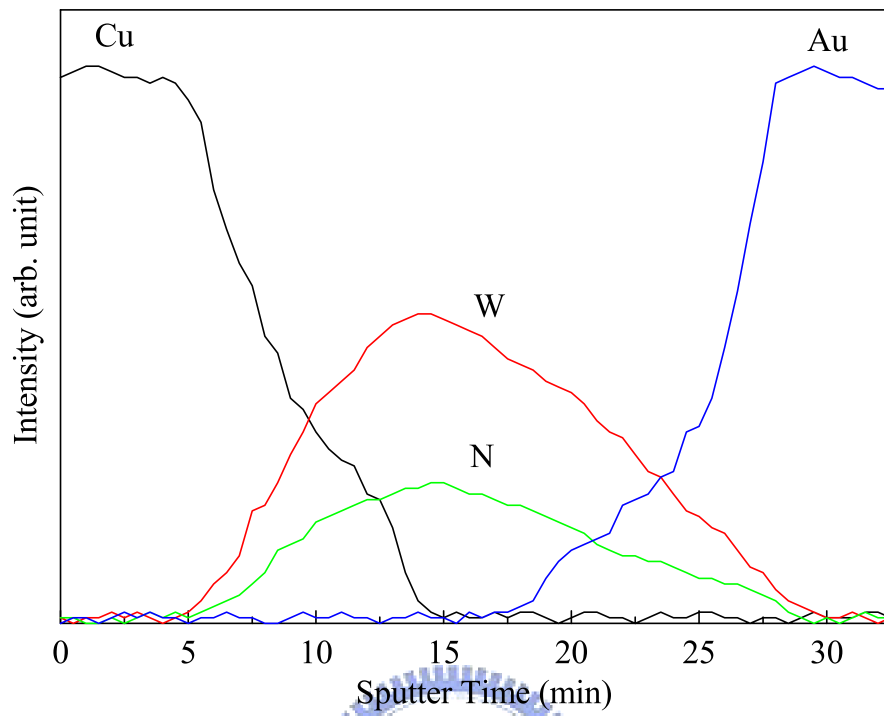


Figure 4.2c AES depth profiles of the Au/WNx/Cu multilayer system after 400°C annealing for 30min.

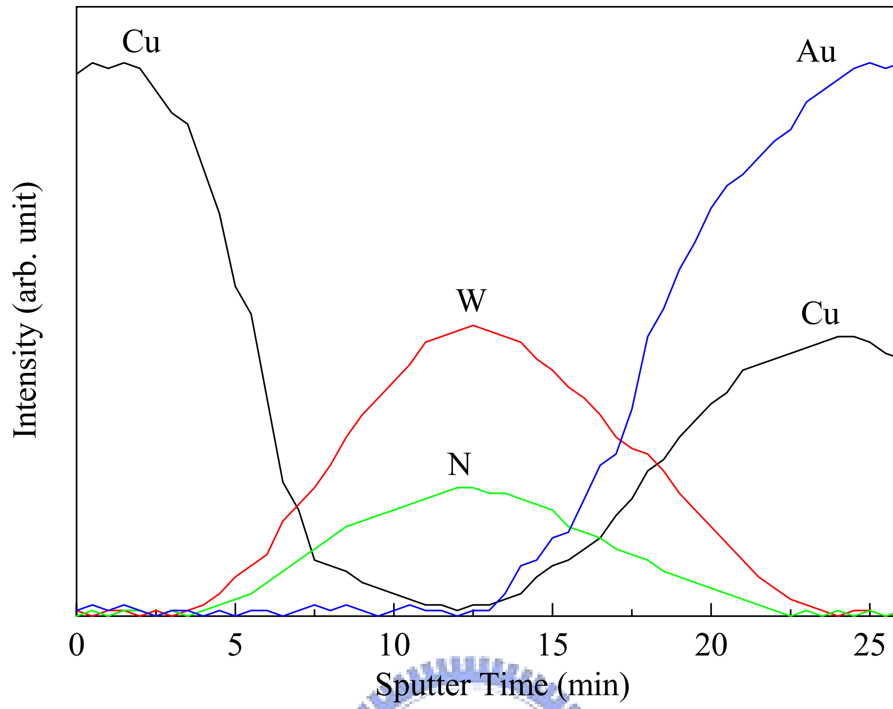


Figure 4.2d AES depth profiles of the Au/WNx/Cu multilayer system after 450 °C annealing for 30 mins.

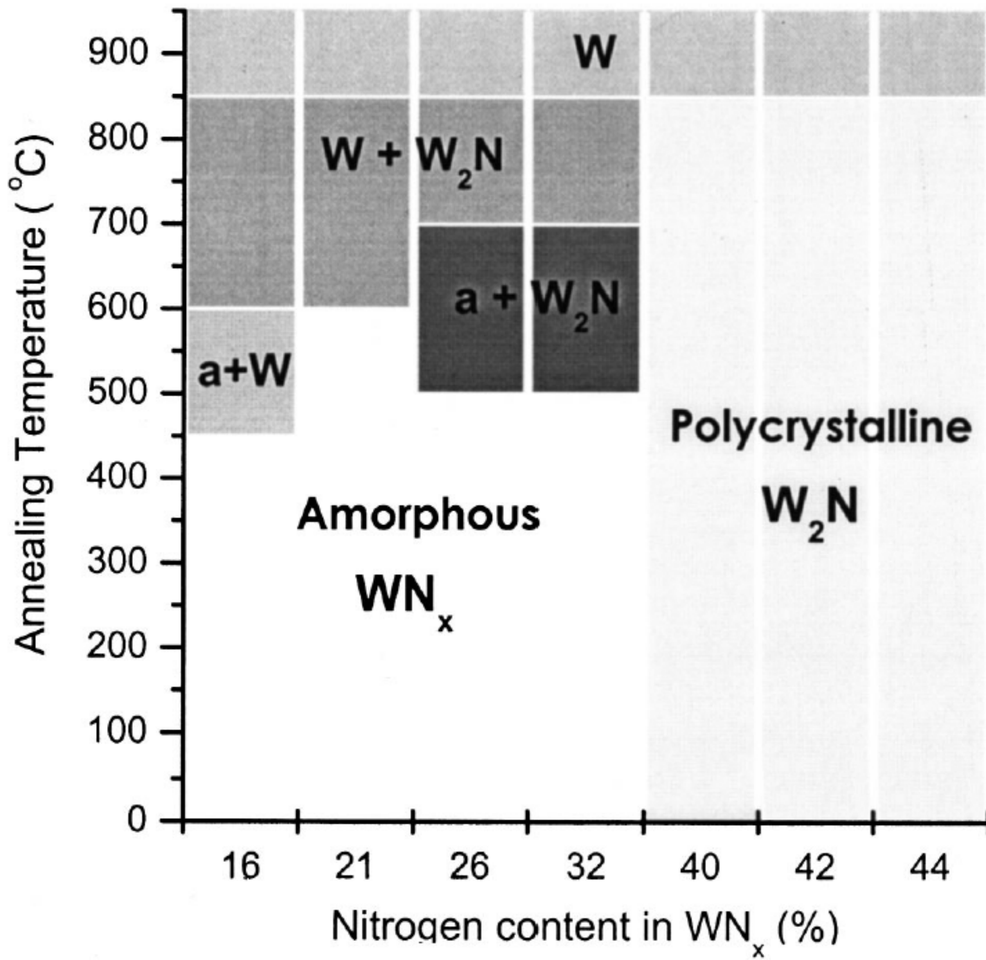


Figure 4.3 Phase map of WNx films with annealing temperature for various nitrogen contents. [5]

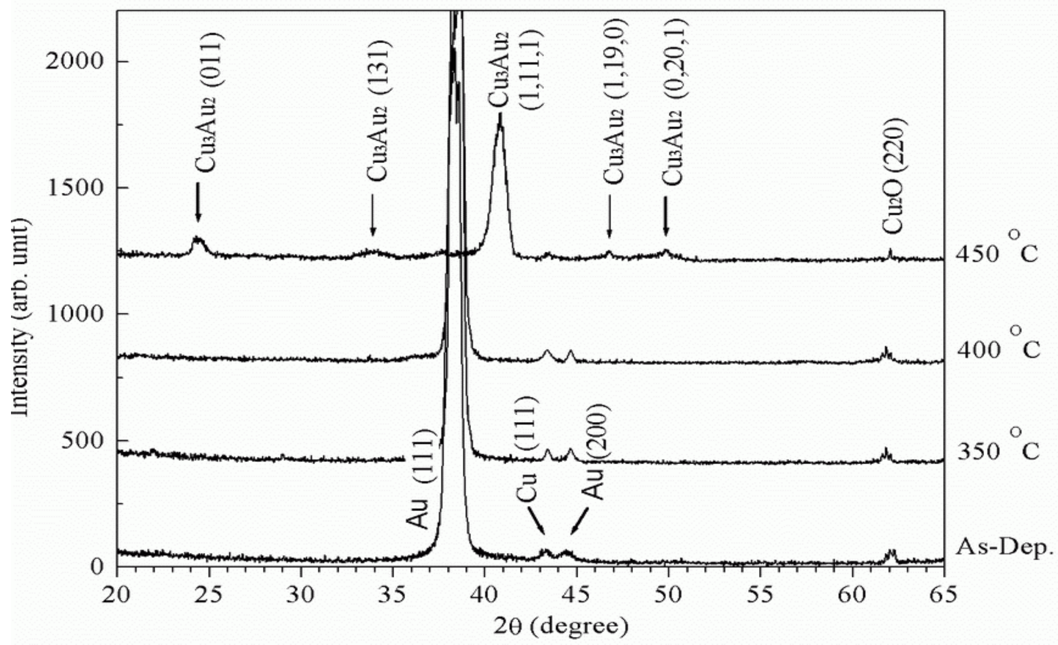
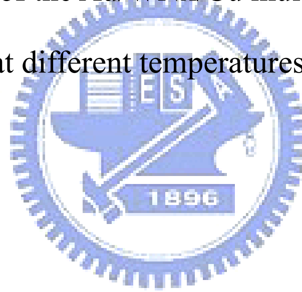


Figure 4.4 XRD patterns of the Au/WNx/Cu multilayer system after thermal annealing at different temperatures for 30 mins.



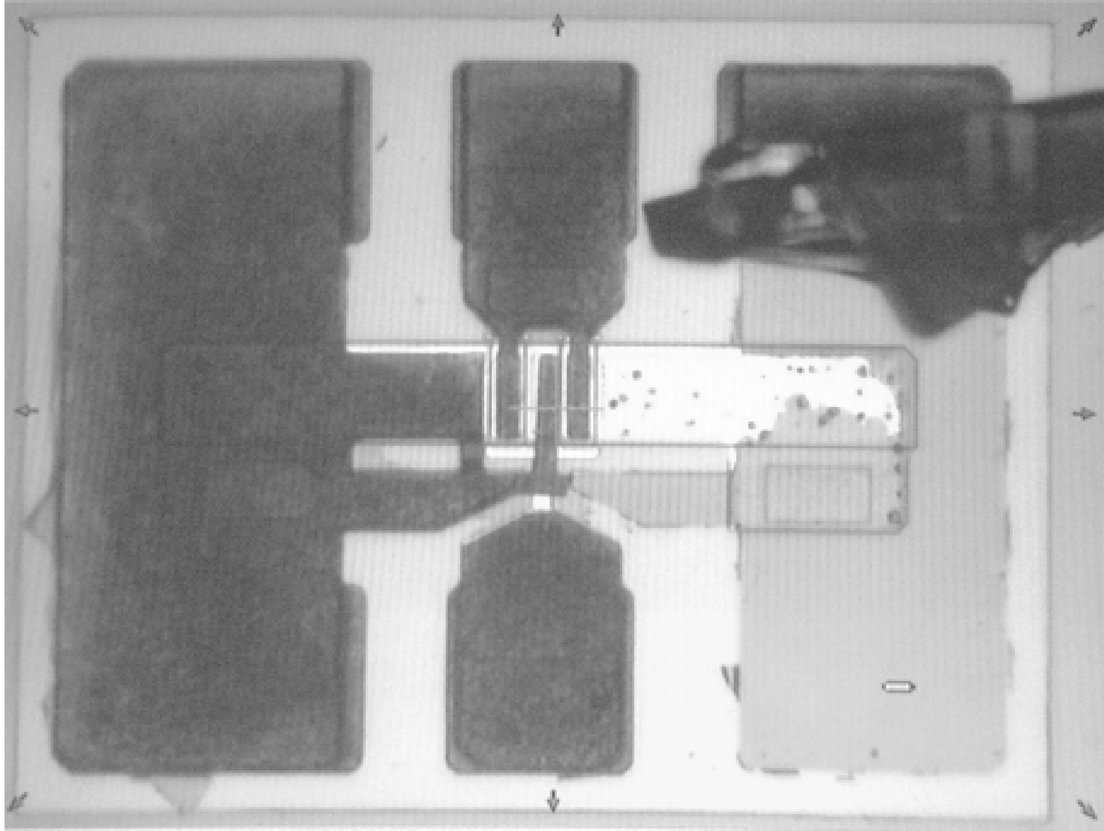


Figure 4.5 Plated Cu peeling off from the GaAs PHEMT.

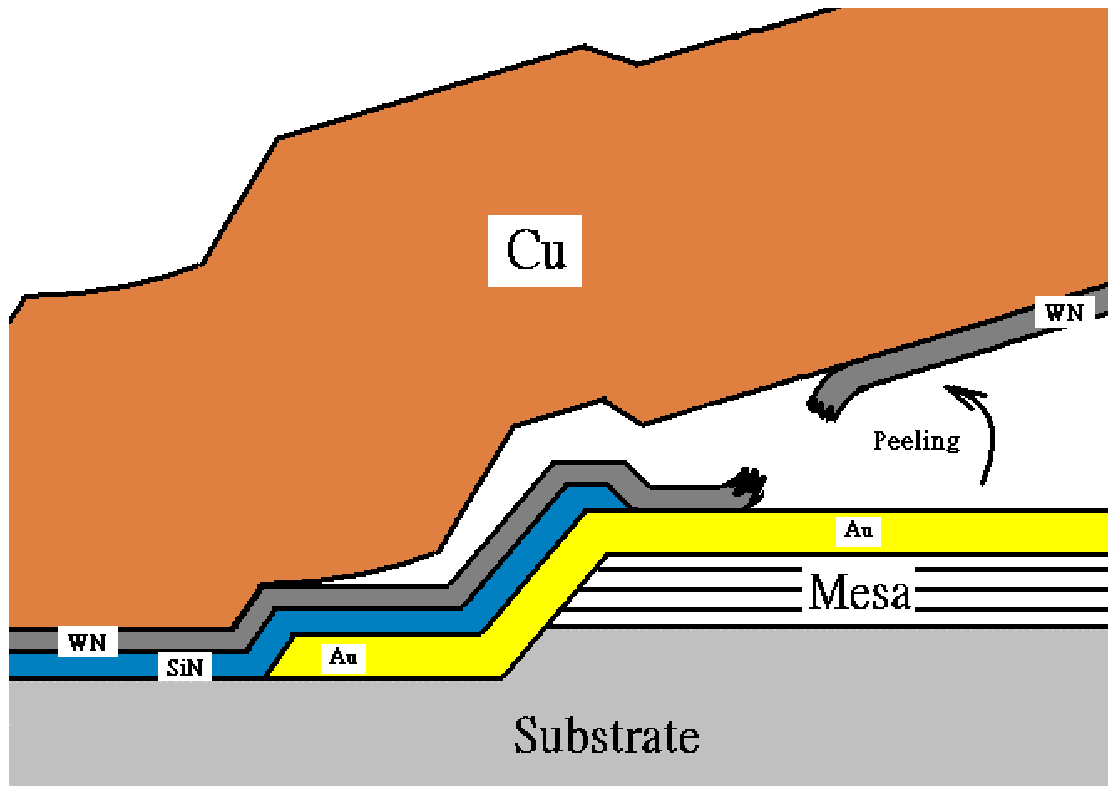
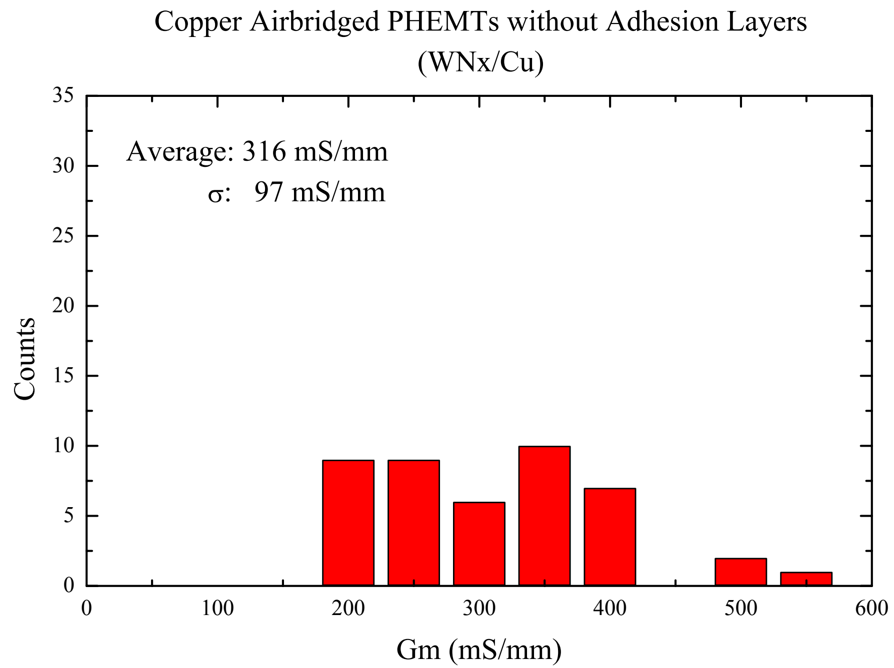


Figure 4.6 Peeling of the thin metal structure used in the Cu-airbridges.



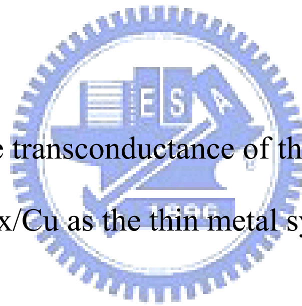
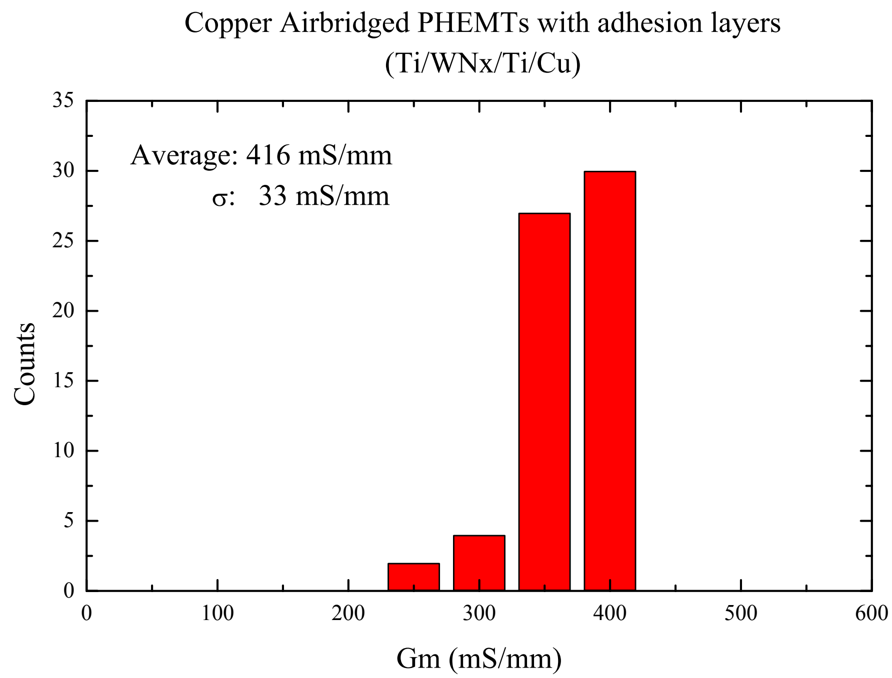


Figure 4.7a Histogram of the transconductance of the Cu airbridged PHEMTs with WNx/Cu as the thin metal system.



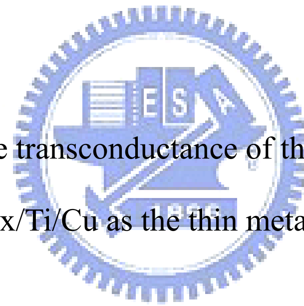


Figure 4.7b Histogram of the transconductance of the Cu airbridged PHEMTs with Ti/WNx/Ti/Cu as the thin metal system.

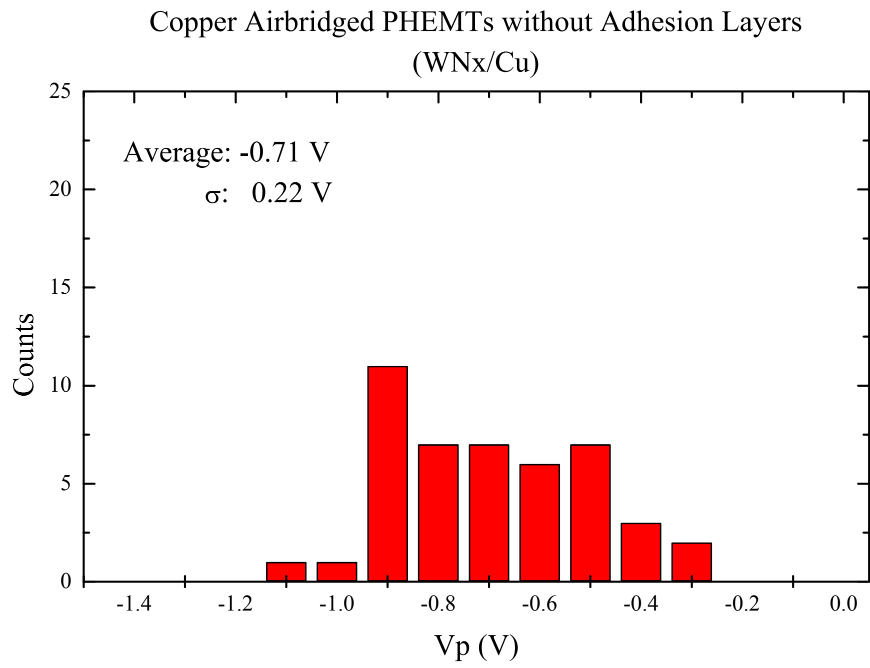


Figure 4.8a Histogram of the pinch-off voltage of the Cu airbridged PHEMTs with WNx/Cu as the thin metal system.

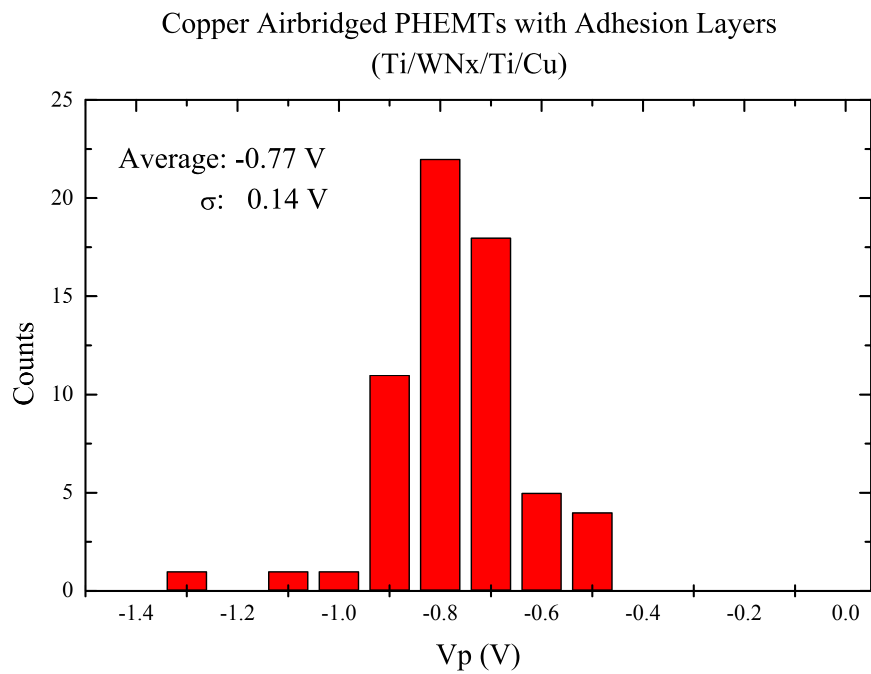


Figure 4.8b Histogram of the pinch-off voltage of the Cu airbridged PHEMTs with Ti/WNx/Ti/Cu as the thin metal system.

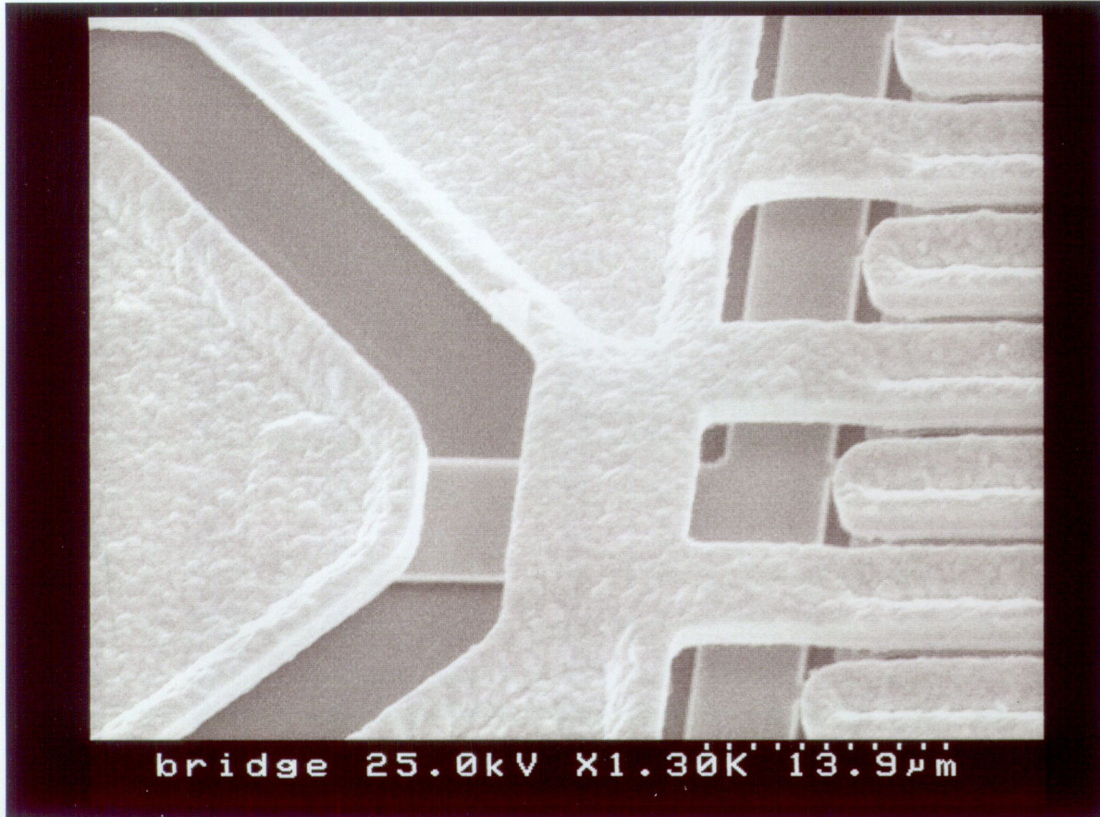


Figure 4.9 SEM photograph of the Au airbridges.

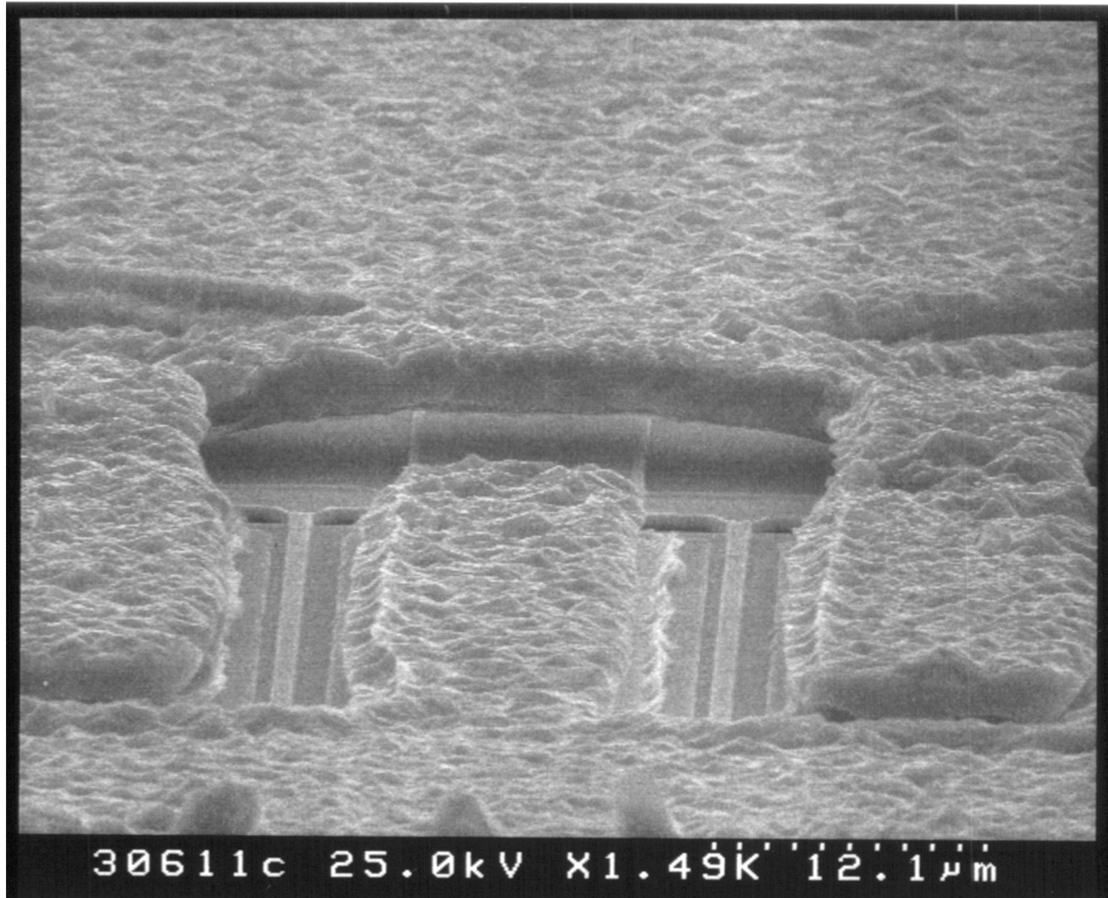


Figure 4.10 WNx protrudings at the edge of Cu airbridges after non-selective thin metal etching.

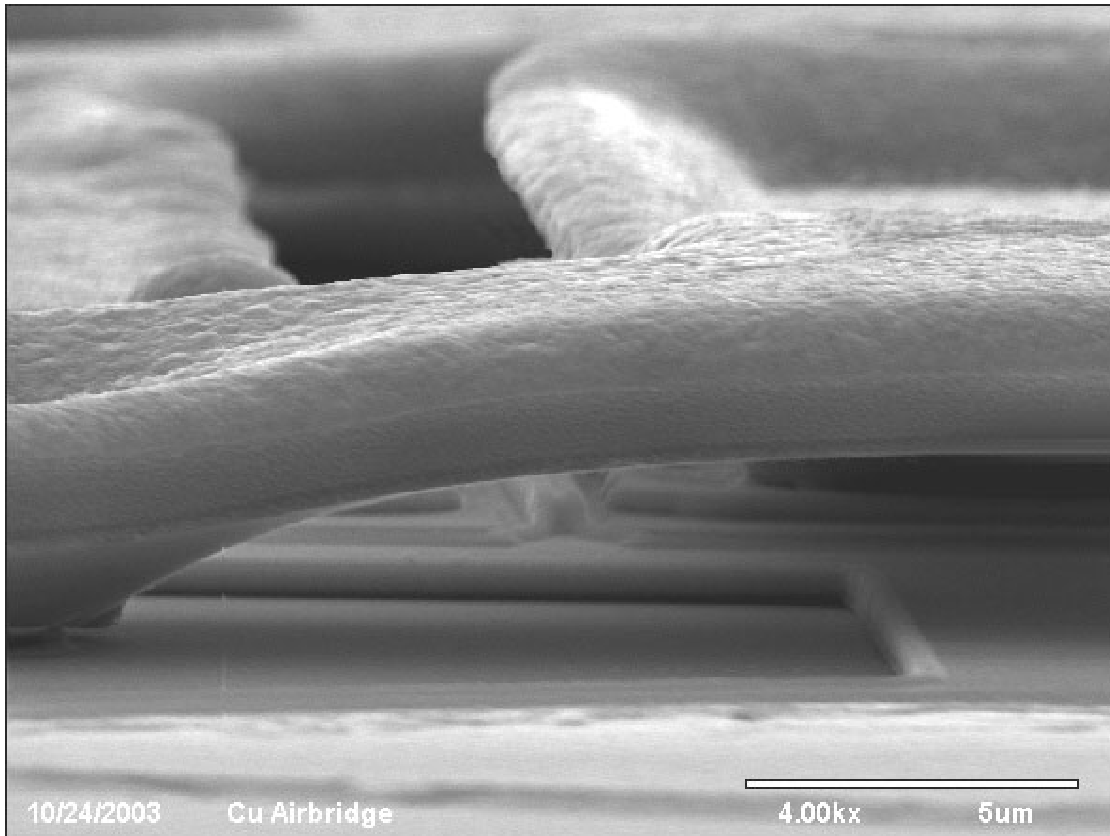


Figure 4.11 SEM photograph of the Cu airbridge after the selective thin metal etching.

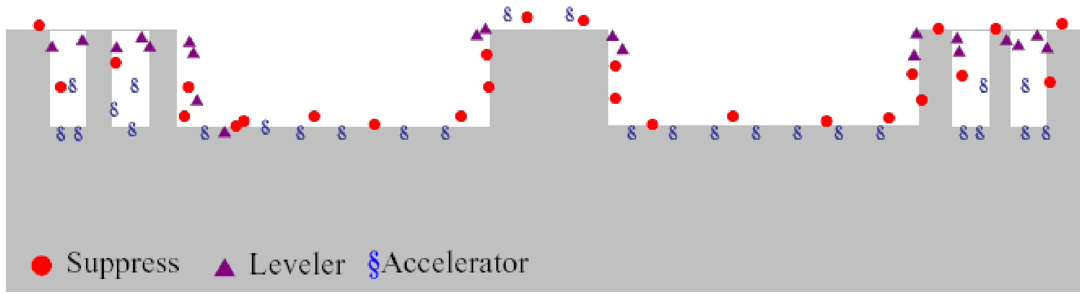
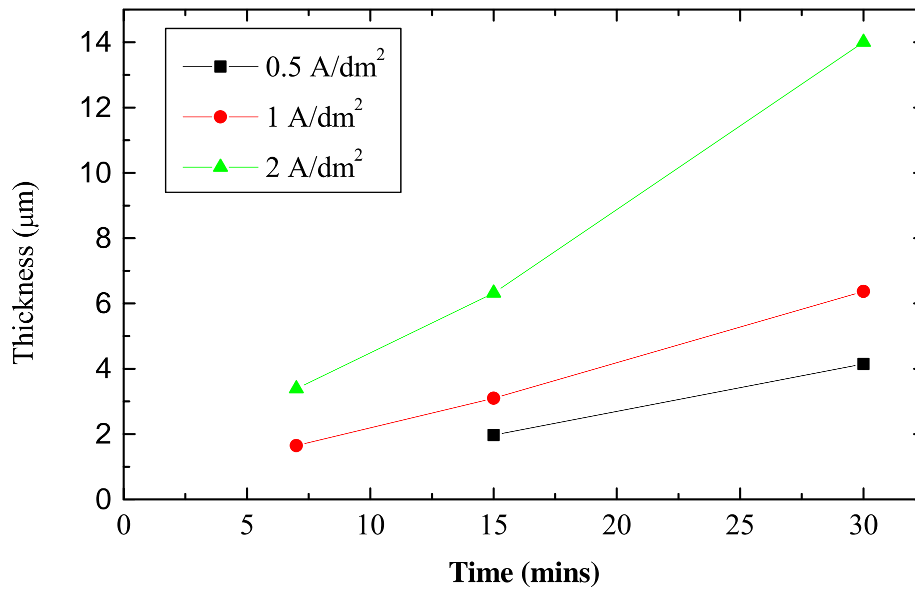


Figure 4.12 Additives distribution on the surface of electroplating Cu.



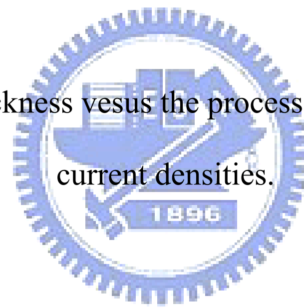
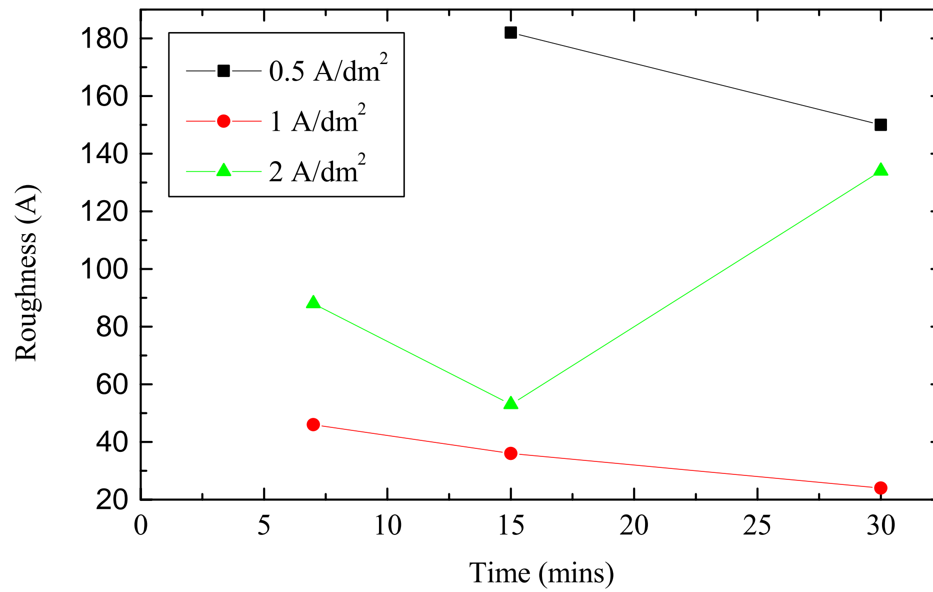


Figure 4.13 The Cu metal thickness vesus the process time for different electroplating current densities.



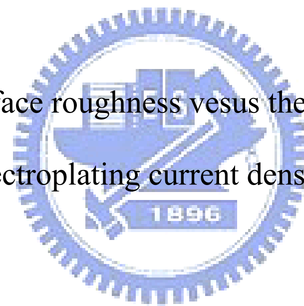


Figure 4.14 The Cu surface roughness vesus the process time for different electroplating current densities.

Chapter 5
Airbridge Interconnects Process

5.1 Airbridge Process Flow

The following process flow was used to fabricate the airbridge interconnects of the PHEMTs in this study.

1. The First Photolithography for Plating Vias.
2. Thin Metals Deposition.
3. The Second Photolithography for Plating Areas.
4. Electroplating.
5. PR. Removal and Thin Metal Etching.

The samples used in this study were as shown in Table 5.1 and the cross sections of three different points of the airbridge process are shown in Figure 5.1. Point (a) shows the active device. Point (b) is the gate metal laying on the inactive area. Point (c) is the perpendicular side view of point (b). In this study, the first layer of photo resist was coated and patterned on the wafer after the nitride via etching in the PHEMT process. The thin metal was then deposited and the second lithography defined the patterns of the photo resist for the areas for electroplating. The bridge metal was subsequently formed by electroplating. After the photo resist stripping and thin metal etching, airbridge process was completed.

5.2 Sample Preparation

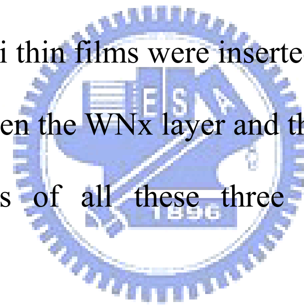
In this study, we used three LN-PHEMTs samples for airbridges study, which had the same recess current target and had similar DC characteristics before airbridges

interconnects.

The first sample, which was numbered S01A362B36, was fabricated with conventional Au airbridges for reference.

The second one, which was numbered S01A362B9, was fabricated with Cu airbridges and used WNx/Cu as the diffusion barrier and the electroplating seed layer. This sample was deposited with the silicon nitride (SiNx) by PECVD to prevent Cu surface oxidation. After deposition, the samples were annealed to investigate the thermal stability of the passivation film.

The third sample, which was numbered S01A362B25E and fabricated with Cu airibridges, used the multilayer system of Ti/WNx/Ti/Cu as the thin metal and the additional Ti metal layers were used as the adhesion layers to overcome the possible metal peeling problem. Two Ti thin films were inserted between the underlying device and the WNx layer, and between the WNx layer and the Cu seed layer.



The nitride via etchings of all these three samples were finished before proceeding airbridge process.

5.3 The First Photolithography for Plating Vias

The thickness of the first layer of resist determines the spacing between the bridge and the material beneath (usually a dielectric). The thickness of the photo resist was about 3 μm.

5.3.1 Wafer clean

In order to remove undesirable residues on the surface of GaAs Substrate, the wafer went through the following cleaning processes; 1) immersed in acetone (ACE) for 5 minutes, 2) immersed in isopropyl alcohol (IPA) for 5 minutes, and

then dried by compressed dried air (CDA) blowing.

5.3.2 PR Coating

Shipley S1818 was used as the first layer of photo resist. Firstly, the resist was coated with the spin rate of 1000 rpm for approximately 10 seconds to spread the resin on the substrate, and then, followed by a 45 seconds spin at a rate of 3000 rpm to coat the resist uniformity. The thickness was about 2.5 μm.

5.3.3 Soft Bake

After spin coating, the resist was heated at 90 °C for 120 seconds to drive out the rest solvent. The soft bake was performed on a hot plate.

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5.3.4 Exposure

The photo resist was exposed by Karl Suss MJB3 I-line aligner. The dose energy for this exposure was 225 mJ/cm^2 at the wavelength of 405 nm.

5.3.5 Development

Immersion technique was used for the development of exposed photo resist. The samples after exposure were immersed into the developer (FHD5) for 20 seconds at the room temperature and followed by D.I. water rinse. The samples were then dried by CDA blowing.

5.3.6 Descum

In order to remove the thin PR residues in the exposed region, an O_2 descum process was necessary after the photolithography. The recipe was 100W for 1 minute with O_2 45 sccm at 60 mTorr by STS inductive coupling plasma (ICP)

etcher.

5.3.7 Hard Bake

The wafer was plate-baked immediately after the ICP descum. This bake was used to evaporate the remaining solvent in the photo resist. On the other hand, the first photo resist must be sufficiently baked to prevent the "bubbling" after thin metal deposition and the lateral thermal bake of the second photolithography. In this process, the wafer was baked at 133 °C for 10 minutes (Figure 5.1b).

5.4 Thin Metal Deposition

5.4.1 Thin metals for Au airbridges

The thin metals, Ti/Au/Ti, for the Au airbridges structures were evaporated. The thicknesses of these three metal layers were 300 Å, 500 Å and 300 Å, respectively, from the bottom to the top.

5.4.2 Thin metals for Cu airbridges

The thin metal of the Cu airbridges structure was Ti/WNx/Ti/Cu with Ti as the adhesion layers, and sputtered WNx as the diffusion barrier. The thicknesses of these four metal layers were 300 Å, 400 Å, 300 Å, and 1000 Å respectively from the bottom to the top.

5.5 The Second Photolithography for Plating Areas

The second layer PR lithography step for airbridge was performed using the following process.

5.5.1 Coating photo resist

The lithography on the thin metal multilayers was performed with using positive photoresist S1818. The process steps for the photoresist coating was as following. Firstly, the spin rate up to 1000 rpm for approximately 10 seconds was used to spread the resin out from the center of the substrate; secondly, high-speed (3000 rpm) spin for 45 seconds was used to improve the uniformity. The thickness was about 2.5 μm.

5.5.2 Soft Bake

After spin coating, photo resist was heated for a short period of time to drive out the remaining solvent. The soft bake was carried out on a hot plate. Three minutes bake at 90 °C was used for the soft bake process.

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5.5.3 Exposure

After the soft bake, the wafer was cooled to room temperature for exposure. The PR. was exposed to I-line light aligner with 405nm wavelength at 360mJ/cm^2 lamp power.

5.5.4 Development

Pattern development after exposure was accomplished by immersion technique. The wafer was immersed in the developer (FHD5) for 20 seconds at room temperature, followed by rinsing in D.I. water, and then dried in nitrogen.

5.5.5 Descum

Descum is necessary to remove the polymer residue left after development.

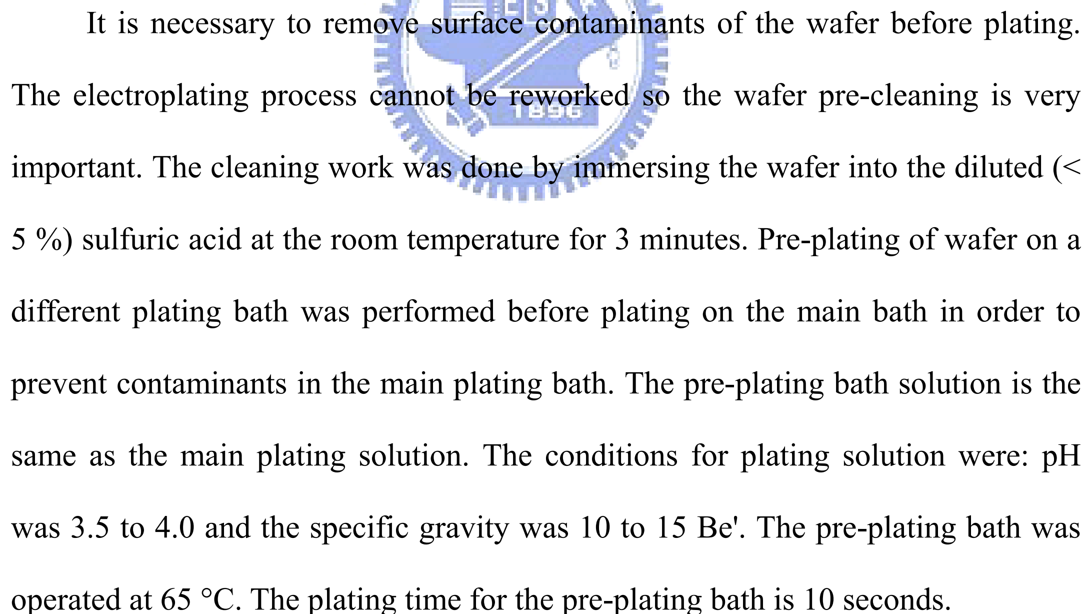
The descum was performed using O_2 gas which usually provides smooth surface on the photoresist after descum. The descum condition was 100 W for 1 minutes with O_2 45 sccm at 60 mTorr by inductive coupling plasma (ICP) processor.

5.5.6 Hard Bake

After developing the wafer was baked on a hot plate immediately. This served to further dry the film and to stabilize the side wall of the via for airbridges plating. In this process, the wafer was backed at 105 °C for 5 minutes. (Figure 5.1d)

5.6 Electroplating

5.6.1 Au Electroplating



It is necessary to remove surface contaminants of the wafer before plating. The electroplating process cannot be reworked so the wafer pre-cleaning is very important. The cleaning work was done by immersing the wafer into the diluted (< 5 %) sulfuric acid at the room temperature for 3 minutes. Pre-plating of wafer on a different plating bath was performed before plating on the main bath in order to prevent contaminants in the main plating bath. The pre-plating bath solution is the same as the main plating solution. The conditions for plating solution were: pH was 3.5 to 4.0 and the specific gravity was 10 to 15 Be'. The pre-plating bath was operated at 65 °C. The plating time for the pre-plating bath is 10 seconds.

For the Au plating bath: pH was 5.0 to 5.3 and the specific gravity was 13 to 20 Be’. The Au plating bath was kept at 65 °C during plating. The bath is an $KAu(CN)_2$ based solution. The current density was 0.3 A/dm2 and the plating time was 20 minutes for 2 μm thick Au

5.6.2 Cu Electroplating

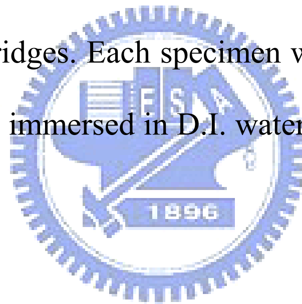
The wafer was cleaned before plating to prevent surface contamination. The wafer was dipped in the diluted sulfuric acid to remove the surface Cu oxide. However, the sulfuric acid also attacks Cu and the dipping time should not be too long. The wafer was dipped in the diluted sulfuric acid (1:10) for 5 seconds.

The current density of the Cu electroplating was 1 A/dm^2 and the plating time was 10 minutes for 2.5 μm thick Cu.

5.7 Plating PR. Removal and Thin Metal Etching

5.7.1 The Second PR. (top layer) Removal

After electroplating, the samples were immersed in ACE to remove the second photo resist of airbridges. Each specimen was etched in the solution for 30 sec. The samples were then immersed in D.I. water for 1 minute and dried by CDA blowing.



5.7.2 Thin Metals Etching

5.7.2.1Thin metals etching for Au airbridges

The thin metal structure used for Au airbridges was Ti/Au/Ti, and it can be removed by selective etching with appropriate etchants. The Ti layers were etched by diluted HF for 50 seconds. The thin layer of Au was etched by KI/I_2 solution for 15 seconds.

5.7.2.2 Thin metals etching for Cu airbridges

The thin metals used for Cu airbridges were Ti/WNx/Ti/Cu, which were deposited from bottom to top. The top layer of the thin metal is Cu. The wafer was dipped in the diluted sulfuric acid (1:10) for 5 seconds to remove the

surface Cu oxide. The thin Cu metal was then etched by $H_2SO_4/H_2O_2/H_2O$ solution mixed in the volume ratio of 5:6:100. The etching rate of this step was very high, and the etching of Cu stops at the underlying Ti as the color turned from red to grey.

Ti was also etched by mixed 1:100 HF (49 %): H_2O solution. HF is the active ingredient in this etchant, so it also etches oxides. Raising the fraction of HF in the solution increases the etching rate. Ti was readily oxidized, so it was likely to form an oxide layer from the water, which is readily etched by the HF in this solution resulting in the formation of bubbles of oxygen. The etch rate was about 12 Å, and the etch stoped as the bubbles evolved.

The diffusion barrier, tungsten nitride, was etched by diluted hydrogen peroxide. The etchant was mixed H_2O_2 (commercially 30 % by weight):H_2O in the ratio of 1:10 for 15 minutes.

5.7.3 The First PR. (bottom layer) Removal

For Au airbridges, the remained resist residual was stripped by ICP 600W/RF10W with 15sccm O_2 flow at 10 mTorr for 15 min. For Cu airbridges, however, the PR residue was stripped by ultrasonic ACE bath instead of O_2 plasma to prevent Cu contamination of ICP etcher.

For Cu-metallized airbridges, the samples were dipped in ACE for 20 minutes to remove the first photo resist for plating vias. And then the specimens were dipped in IPA for 2 min. They were finally immersed in D.I. water, and then followed by CDA drying (Figure 5.1f). The SEM photograph of the Cu airbridge is as shown in Figure 5.2

TABLE

Table 5.1 Comparison between Au airbridges and Cu airbridges process

	Au airbridges	Cu airbridges	
Sample Number	S01A362B36	S01A362B9	S01A362B25E
Nitride via	Plasma etch		
Plating via photolithography	S1818 PR. coated		
Thin metal UBM deposition	Ti/Au/Ti	WNx/Cu	Ti/WNx/Ti/Cu
Plating photolithography	S1818 PR. coated		
Pre-plating etching (Ti)	Diluted HF	×	
Airbridges electroplating	Au 2 μm	Cu 2.2 μm	
Top photo resist strip	Flood exposure + flood development		
Thin metal etching	1.Diluted HF 2.KI/I2 3.Diluted HF	Diluted NH_4OH/H_2O_2	1.Diluted H_2SO_4/H_2O_2 2.Diluted HF 3.Diluted H_2O_2 4.Diluted HF
Bottom photo resist strip	1. Acetone (1hr) 2. ICP (O_2)	1. Acetone (1hr) 2. Acetone ultrasonic 20sec.	
DC and RF measurement			

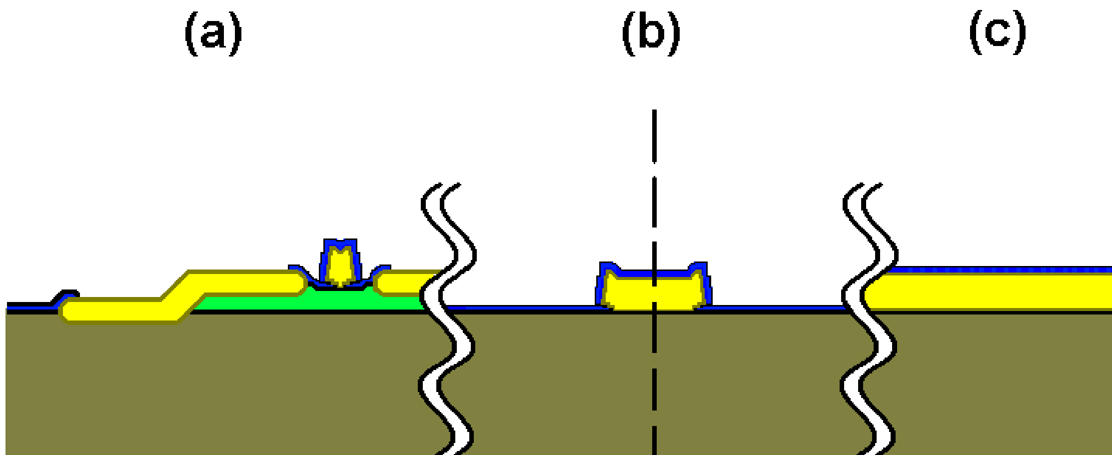


Figure 5.1a Schematic of device after passivation via etching

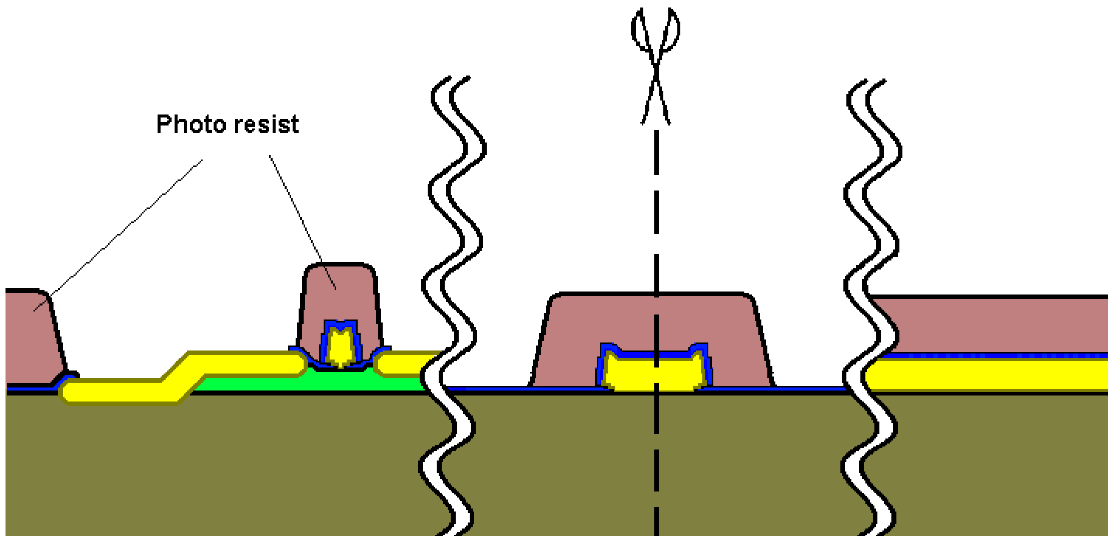


Figure 5.1b Schematic of plating via photolithography.

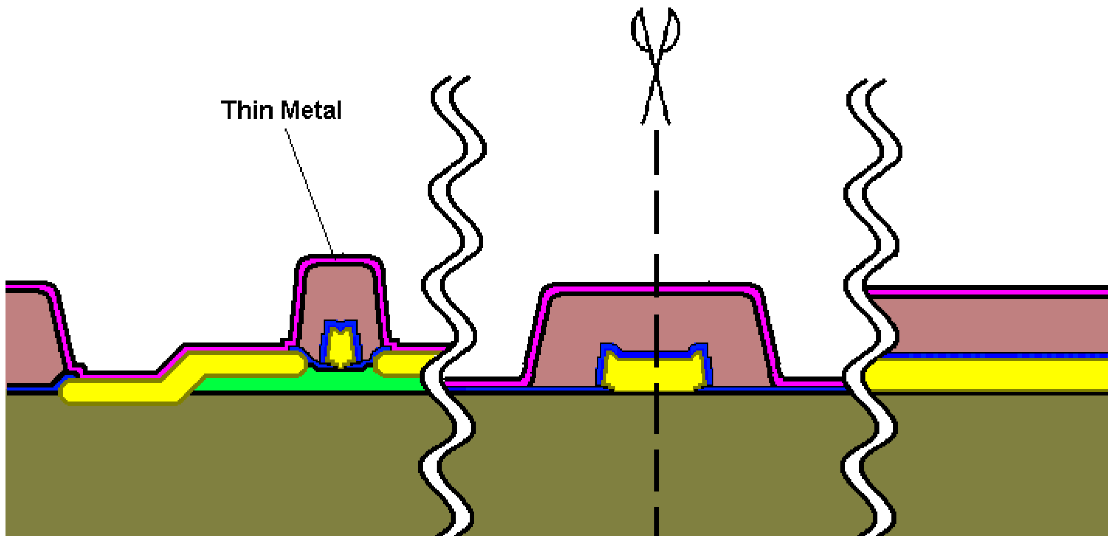


Figure 5.1c Schematic of thin metal deposition

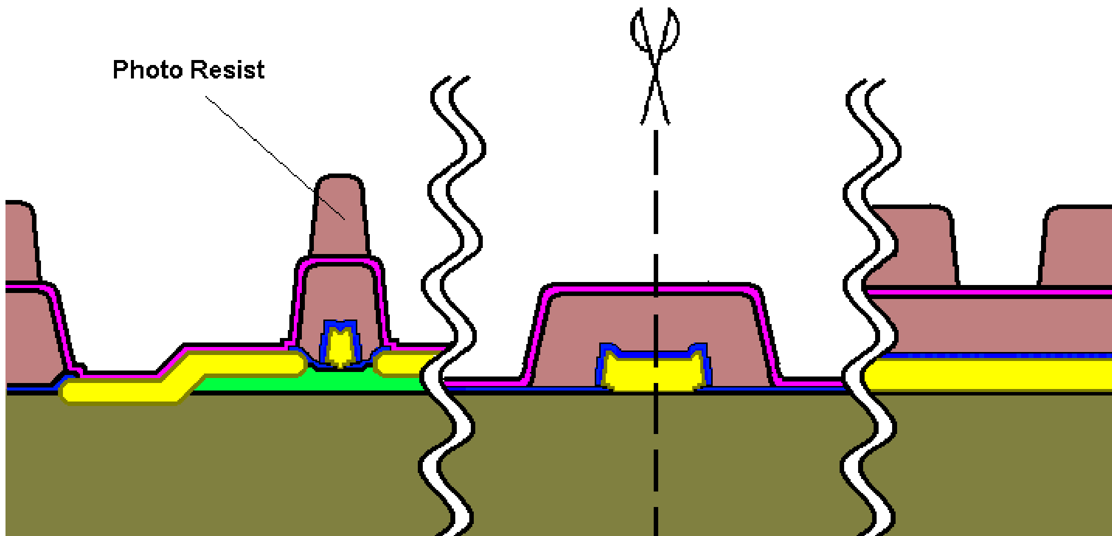


Figure 5.1d Schematic of plating photolithography

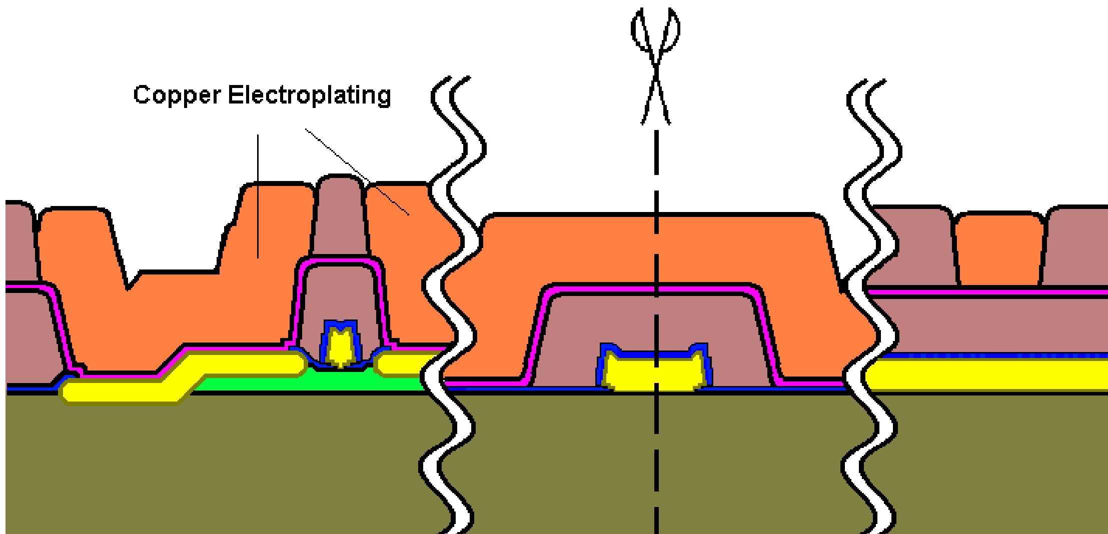


Figure 5.1e Schematic of Cu electroplating

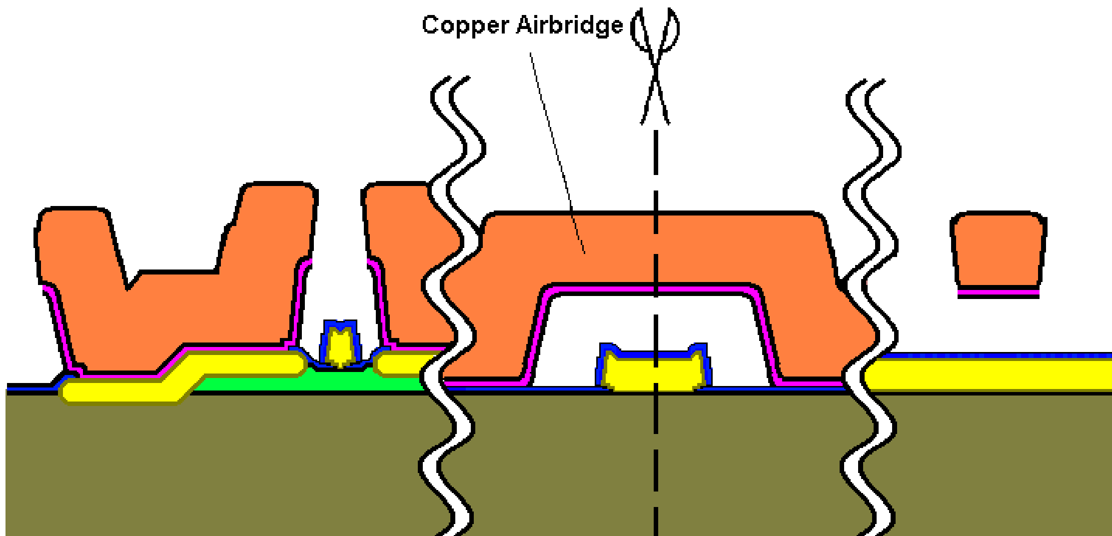


Figure 5.1f Schematic of Cu airbridges

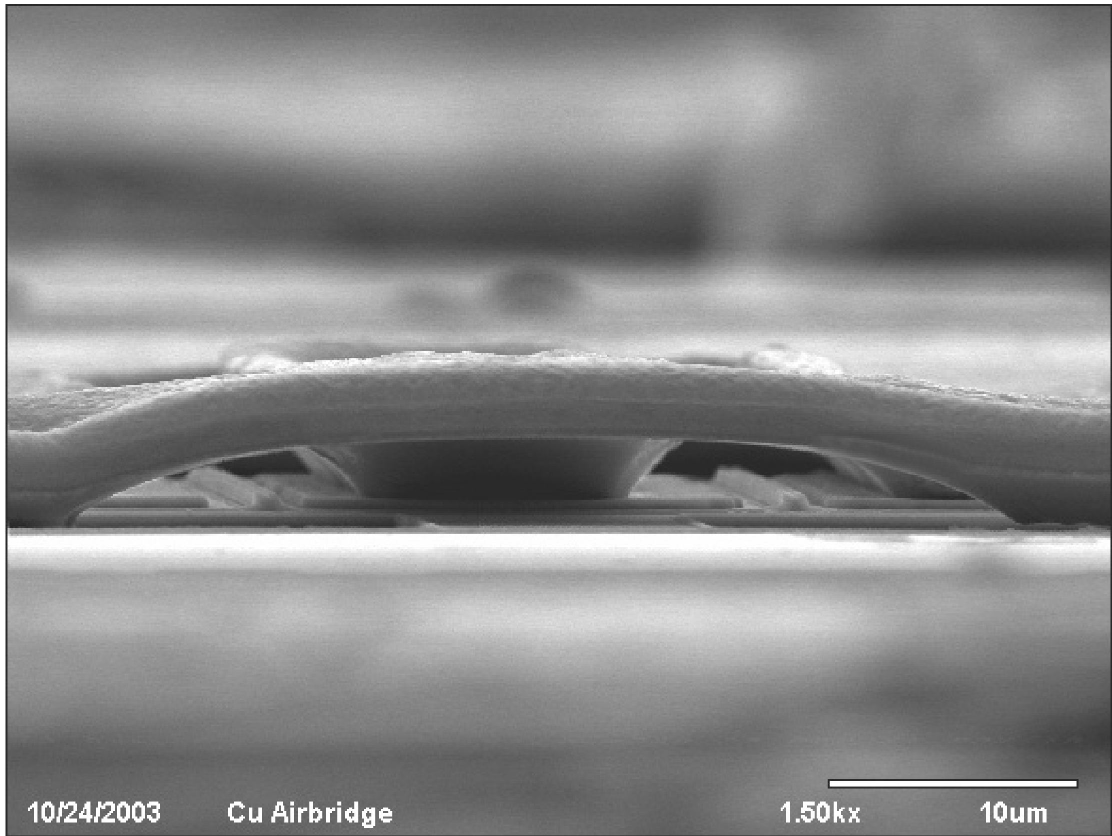


Figure 5.2 SEM photograph of the Cu airbridge.

Chapter 6
Electrical Characteristics and Thermal Stability of PHEMTs Fabricated with Cu-Metallized Airbridges

6.1 DC Characteristics

Electrical characteristics of the PHEMTs with different interconnect materials were compared to evaluate the performance of the Cu airbridged PHEMTs.

The DC characteristics on the Au-airbridged LN-PHEMT were as shown in Figure 6.1 and 6.2. The saturated drain current was about 180 mA/mm and the maximum transconductance was 452 mS/mm when biased at V_{DS}= 1.5 Volts and V_{GS} = 0 Volts.

In order to test the thermal stability of the thin WNx/Cu metals, LN-PHEMTs with Cu airbridges were annealed at 250 °C for 20 hours in the nitrogen atmosphere. The DC and RF characteristics before and after the thermal annealing were measured and compared. The comparison of the drain I-V characteristics on the same Cu-metallized LN-PHEMT with WNx diffusion barrier before and after annealing is shown in Figure 6.3 and the dependence of the transconductance on the gate bias voltage before and after annealing is shown in Figure 6.4. The saturated drain current was about 150 mA/mm and the maximum transconductance was up to 400 mS/mm when biased at V_{DS} = 1.5 Volts and V_{GS} = 0 Volts. These DC characteristics showed little change after thermal annealing. The knee voltage of the drain I-V curve remained almost the same after the thermal annealing.

The DC characteristics of the LN-PHEMT using Ti/WNx/Ti as the thin metals are shown in Figure 6.5 and Figure 6.6. The knee voltage of the device was also 0.3 Volts, which was the same as that with the WNx barrier. The Cu-airbridged LN-PHEMT with Ti adhesion layer had the saturated drain current of 180mA/mm and

the maximum transconductance of 476 mS/mm. These results show that the LN-PHEMTs fabricated with Cu airbridges have the comparable DC characteristics as those fabricated with Au airbridges.

6.2 Noise and Gain Performance

Figure 6.7 shows the noise and gain performances of the Au-airbridged LN-PHEMT. The noise was 1.09 dB and the associated gain was 9.41 dB at the operating frequency of 18 GHz.

Figure 6.8 shows the thermal stability of the noise and gain performances of the Cu-metallized LN-PHEMT with WNx/Cu as the thin metals. The noise figure of the fabricated device was 0.82dB and the associated gain was 11.11dB when tested at 12 GHz. After 250°C thermal annealing for 20 hours in the nitrogen atmosphere, the noise figure was 0.87dB and the associated gain is 10.93dB. The noise performance decayed very little after thermal annealing.

Figure 6.9 shows the noise and gain performances of the Cu-metallized LN-PHEMT fabricated with Ti/WNx/Ti/Cu as the thin metals. The noise of the device with Ti adhesion layers was 1.09 dB and the associated gain was 8.94 dB at the operating frequency of 18 GHz. The noise and gain performances of the Cu-airbridged LN-PHEMTs fabricated with Ti/WNx/Ti/Cu as the thin metals is comparable with those of Au-airbridged LN-PHEMTs.

6.3 The Unity-Current-Gain Frequency

The unity-current-gain frequency, which is also called cut-off frequency, f_T, is defined to be the frequency at which the short-circuit current gain becomes equal to 1 (0 dB). The cut-off frequency of the LN-PHEMTs with alternative airbridge processes is shown in Figure 6.10. All the curves had the similar cut-off frequency of about 70

GHz. These results show that the Cu-metallized LN-PHEMTs have the comparable RF performance of current gain as compared with the LN-PHEMTs with Au airbridges.

FIGURES

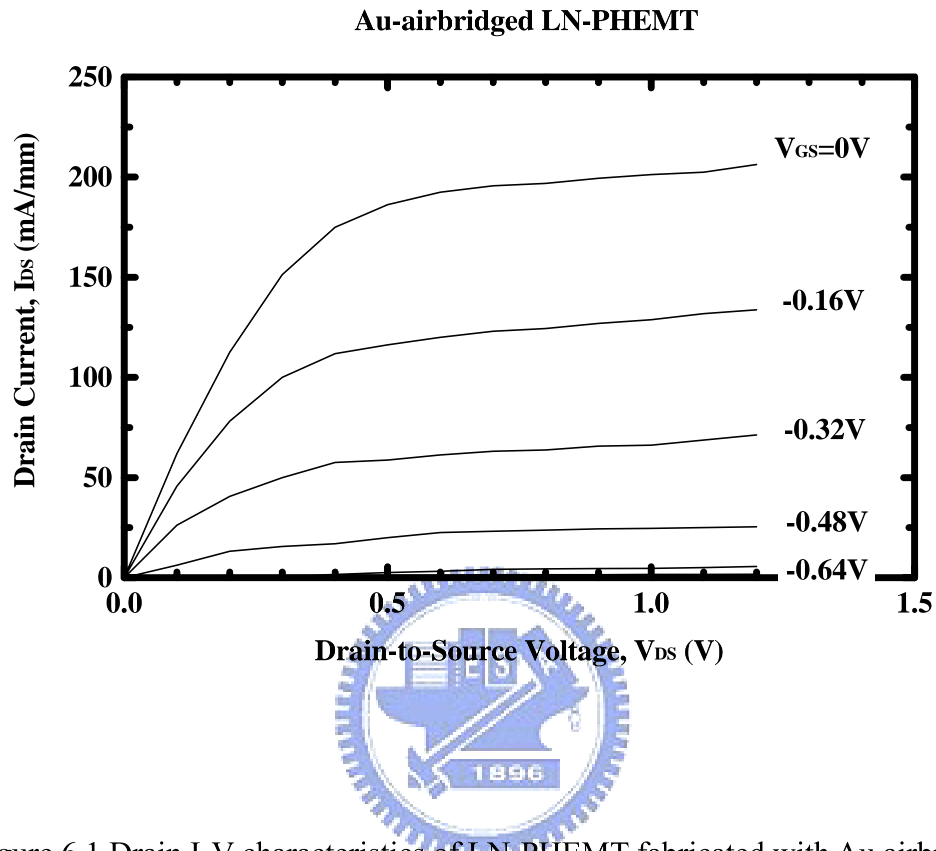


Figure 6.1 Drain I-V characteristics of LN-PHEMT fabricated with Au airbridge.

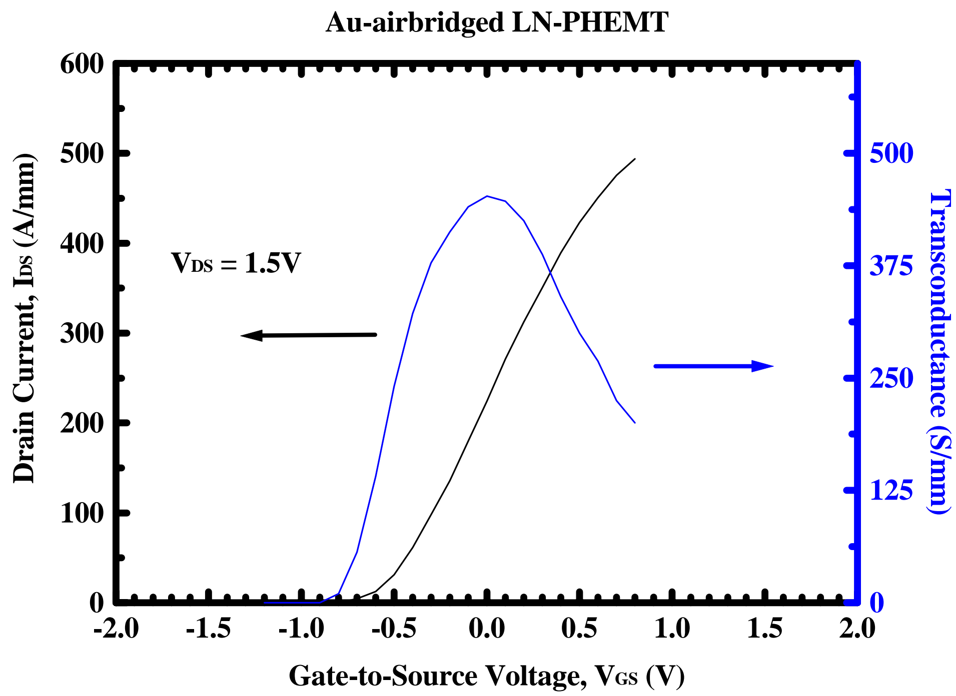


Figure 6.2 Dependence of the transconductance on the gate bias voltage of LN-PHEMT fabricated with Au airbridge.

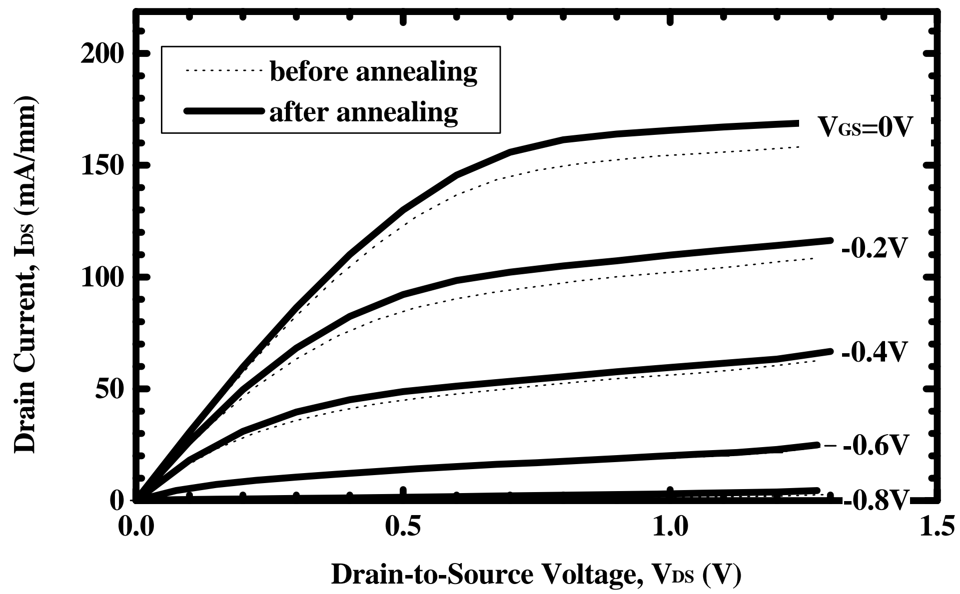
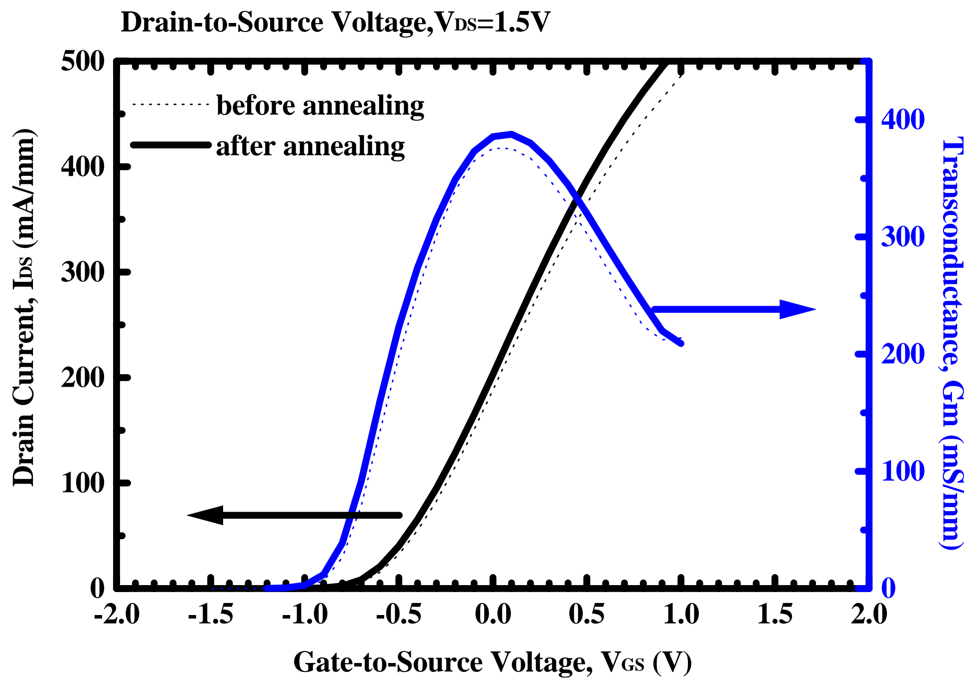


Figure 6.3 Drain I-V characteristics of LN-PHEMT fabricated with Cu airbridge before and after 250°C 30mins thermal annealing in nitrogen atmosphere.



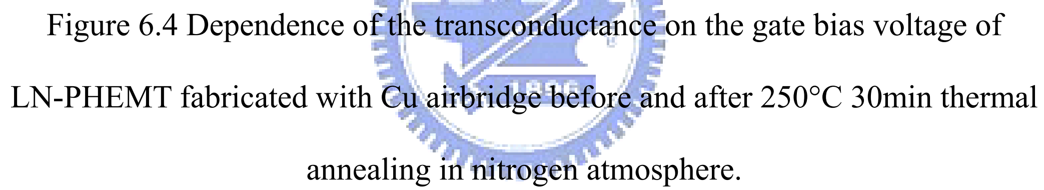
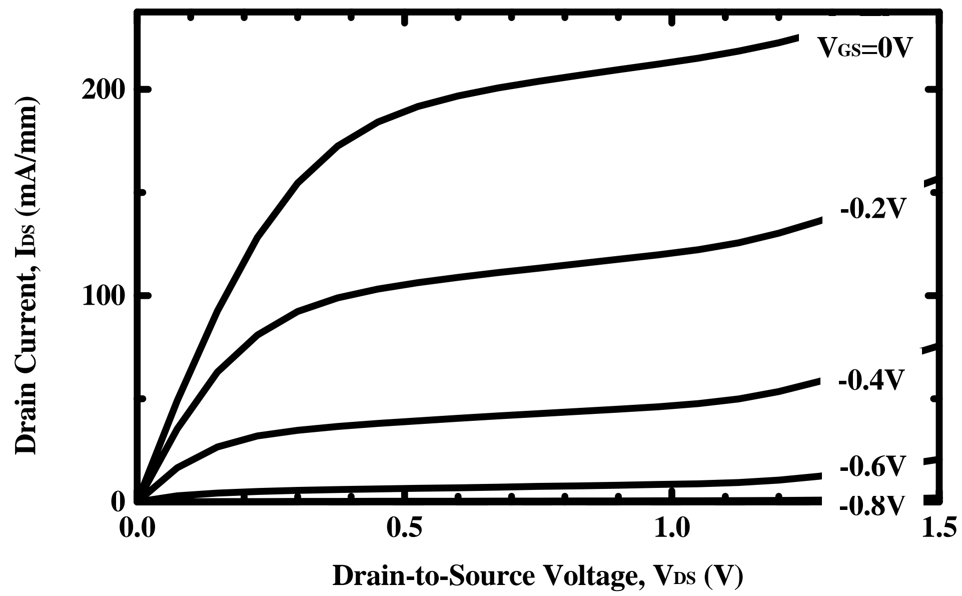


Figure 6.4 Dependence of the transconductance on the gate bias voltage of LN-PHEMT fabricated with Cu airbridge before and after 250°C 30min thermal annealing in nitrogen atmosphere.



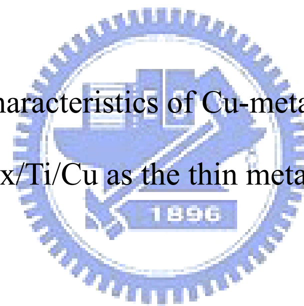


Figure 6.5 Drain I-V characteristics of Cu-metallized LN-PHEMTs with Ti/WNx/Ti/Cu as the thin metal system.

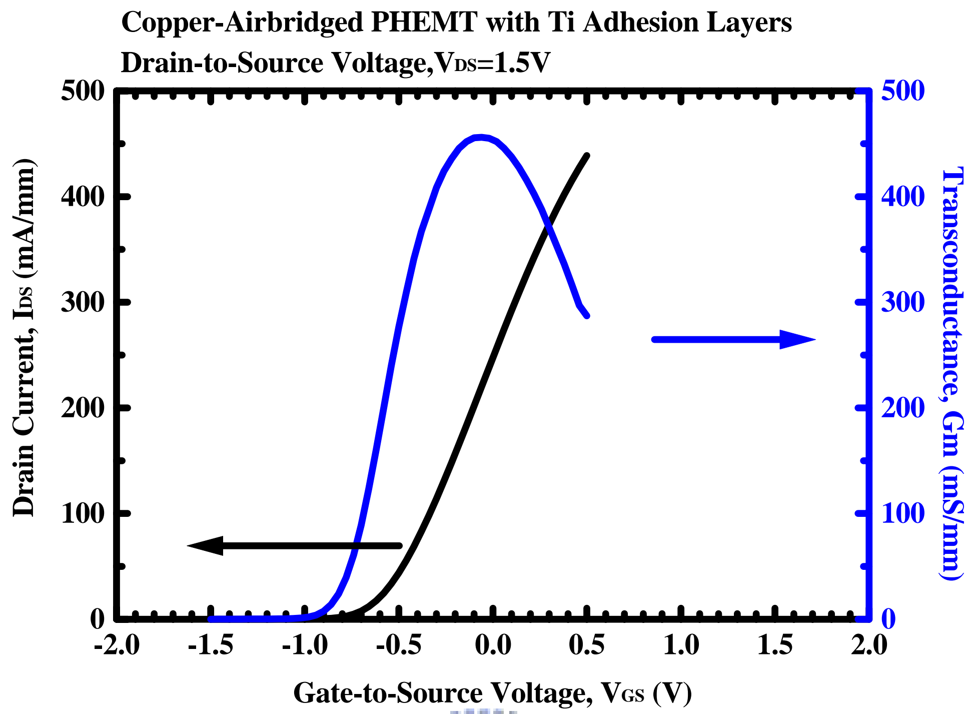


Figure 6.6 Transconductance of Cu-metallized LN-PHEMTs with Ti/WNx/Ti/Cu as the thin metal system.

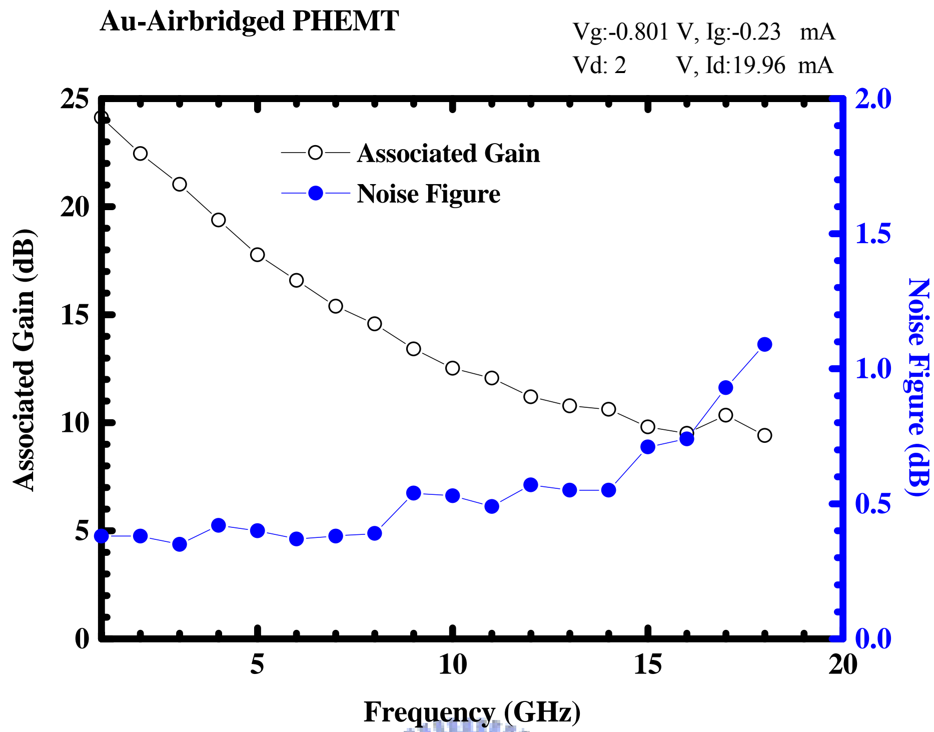


Figure 6.7 Noise and gain performance of the Au-airbridged LN-PHEMT.

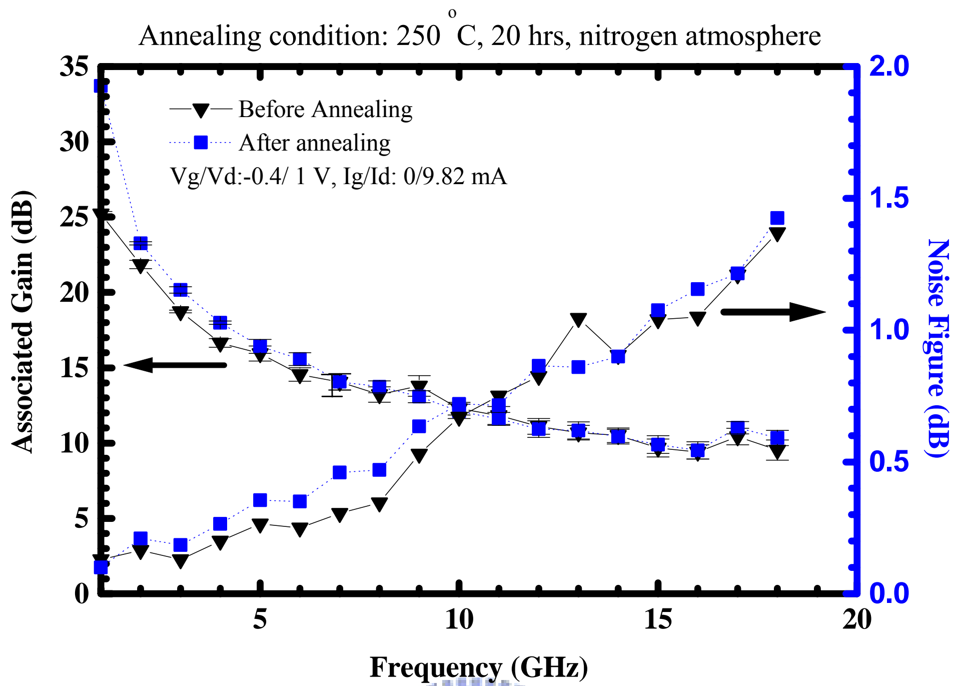


Figure 6.8 Thermal stability of the noise and gain performance of the Cu-metallized LN-PHEMT with WNx/Cu as the thin metals.

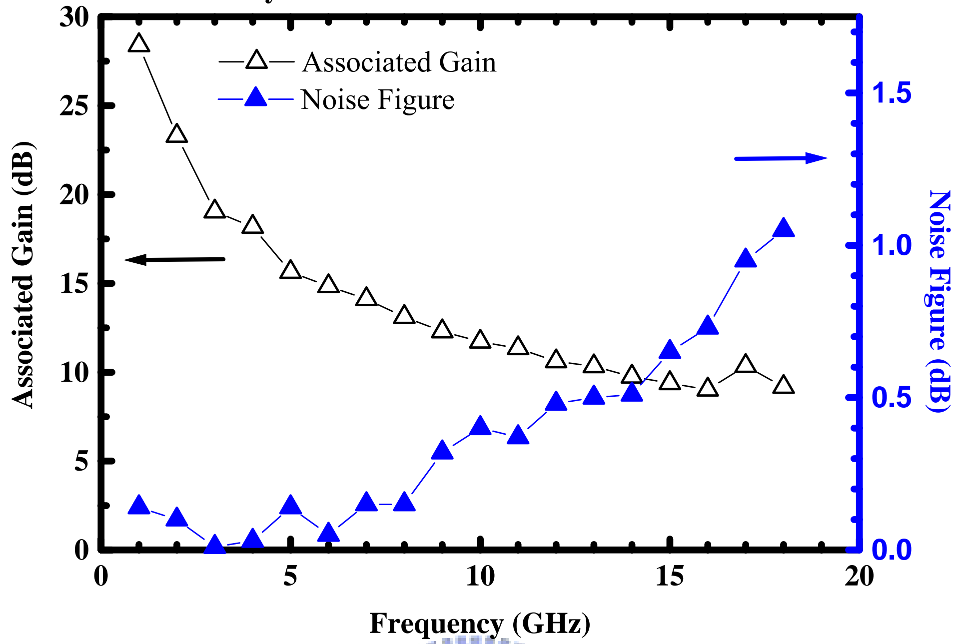


Figure 6.9 Noise and gain performance of the Cu-metallized LN-PHEMT with Ti/WNx/Ti/Cu as the thin metals.

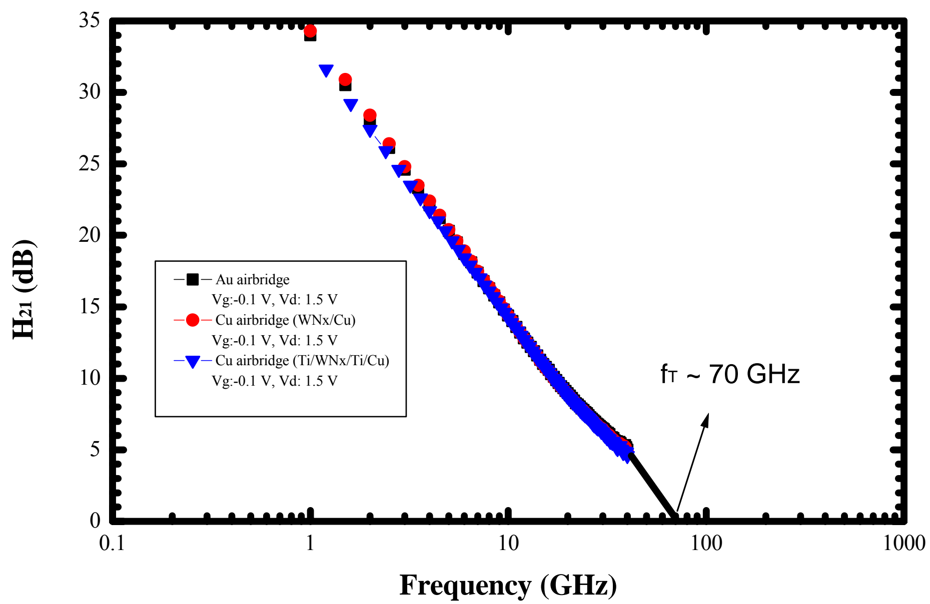


Figure 6.10 Cut-off frequency of the LN-PHEMTs with alternative airbridge processes.

Chapter 7
Conclusions

GaAs Schottky structures with Cu and refractory metal as the diffusion barriers were evaluated. Among the Cu-metallized Schottky contacts studied, the Ti/Co/Cu Schottky structure showed the lowest series resistance, but the change of the ideality factor was larger than the other structures after annealing treatment at 200 °C. From the XRD results, the Ti/W/Cu, Ti/Co/Cu and Ti/Mo/Cu Schottky structure are thermally stable after annealing up to 300 °C. Experimental results show that the Cu metallized Schottky structures have comparable electrical characteristics and thermal stability as compared to the traditional Ti/Pt/Au structure. Overall, the Ti/Co/Cu, Ti/Mo/Cu and Ti/W/Cu multilayer metal can be used as the Schottky structures for GaAs devices.

Cu airbridge process has also been successfully applied to the LN-PHEMT fabrications. In this process, WNx was used as the diffusion barrier to prevent Cu atoms from diffusing into Au layer. From the results of the AES depth profiles and the XRD patterns, WNx sustained as the diffusion barrier between Au and Cu even after thermal annealing of 350°C for 30 minutes. Although there was no evidence of intermetallic compound formation after 400 °C annealing for 30 minutes, there’s a risk of Cu diffusion into the WNx layer after longer annealing time. From the results of the materials analysis, WNx was thermally stable even up to 350 °C annealing for 30 minutes.

The LN-PHEMTs with WNx/Cu as the thin metal system had a saturated drain current of 150 mA/mm and the maximum transconductance was up to near 400mS/mm when V_{DS} was 1.5 Volts. When tested at 12 GHz, the noise figure was 0.82 dB and the associated gain was 11.11 dB. The DC characteristics and NF

performance were thermally stable even after the 250 °C annealing for 20 hours. However, this thin metal system of WNx/Cu causes the issue of plating metal peeling due to the poor adhesion between Au/WNx and WNx/Cu layers.

The plating metal peeling problem has been solved with the addition of the Ti layer to the thin metal system, i.e. Ti/WNx/Ti/Cu. The two additional Ti layers were added to enhance the adhesion between Au/WNx and WNx/Cu layers. The metal peelings no longer occur on the LN-PHEMTs fabricated with Ti/WNx/Ti/Cu metal system. The Cu-metallized LN-PHEMT with Ti adhesion layers has a saturated drain current of 180 mA/mm and the maximum transconductance of 476 mS/mm. The device shows comparable DC characteristics as the LN-PHEMT with the conventional Au airbridges. The noise figure of LN-PHEMT with Ti adhesion layer was 1.09 dB and the associated gain was 8.94 dB at 18 GHz. The cut-off frequencies of Cu-metallized LN-PHEMTs were almost the same as that of the conventional Au-metallized LN-PHEMTs. All these results show that LN-PHEMT with Cu-metallized airbridges has been successfully developed and these devices have comparable electrical performances as those with the conventional Au airbridges.

In this study, Cu-airbridged LN-PHEMTs using Ti/WNx/Ti/Cu as the thin metals have shown comparable electrical characteristics with Au-airbridged LN-PHEMTs'. However, the thermal stability evaluations of the Ti/WNx/Ti/Cu multilayer system either by materials analysis or by electrical performance analysis were not completed. It is necessary to ensure the thermal stabilities of this material system.

Also, Cu-airbridge needs a passivation layer to prevent Cu from corrosion by either humidity or oxygen atmosphere. PECVD silicon nitride can be used as the passivation layer. However, the thermal stability and the feasibility of using SiNx as the Cu airbridge passivation for GaAs LN-PHEMT fabrication still need to be evaluated in the future.