The Dielectric Reliability of Intrinsic Thin SiO_2 Films Thermally Grown on a Heavily Doped Si Substrate—Characterization and Modeling

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***Abstract*—The dielectric reliability of the intrinsic thin SiO_2 films (~110 Å) thermally grown on heavily doped n-type Si substrates has been studied by using the time-zero-dielectric-breakdown (ramp-voltage-stressed *I–V*) and time-dependent-dielectric-breakdown (constant-voltage-stressed *I–t* and constant-current-stressed *V–t*) tests. These experiments have been performed to investigate the variations of trapped electron density, interface state density, and field enhancement in a thin SiO_2 film stressed with different amounts of charges. Moreover, the temperature effects on these parameters in a thin SiO_2 film have also been studied. A theoretical model considering the effects of dynamic trapping (i.e., trapping and detrapping), positive charge generation, weak spots, and robust area is proposed to describe the conduction mechanism and dielectric breakdown of a thin SiO_2 film. Important physical parameters such as barrier height, trapped electron density, trap capture cross section, and trap generation rate have been analyzed to interpret the temperature effects.**

I. Introduction

SINCE the integration level of VLSI circuits progresses very quickly, a highly reliable thin SiO_2 film of about 100 Å is required to fabricate a small-geometry MOS device. A high-quality thin SiO_2 film with a large charge-to-breakdown-endurance or a high-field endurance is especially needed for a tunneling oxide in a FLOTOX EEPROM device. The dielectric reliability of a thicker SiO_2 film ($\geq$390 Å) has been widely studied [1]–[6]. Recently, investigations focused on the dielectric reliability of a thin SiO_2 film ($\leq$200 Å) have become prevalent [7]–[14]; however, only a few papers [9], [12] have concentrated on the high-field intrinsic reliability.

In this paper, time-zero dielectric breakdown (TZDB) using ramp-voltage-stressed *I–V* measurement and time-dependent dielectric breakdown (TDDB) using constant-voltage-stressed *I–t* and constant-current-stressed *V–t* measurements are used to study the dielectric reliability of a thin SiO_2 film of about 110 Å. The ramp-voltage-stressed TZDB data yielding a narrow breakdown histogram are used to ascertain the high-field intrinsic dielectric integrity of these thin SiO_2 films. Important parameters concerned with the dielectric reliability such as activation energies, electric field, and current density acceleration factors are derived from the TDDB as well as the TZDB data. The special features of these results as compared with earlier reports on the dielectric reliability of thick/thin SiO_2 films [1], [2], [5]–[9], [11], [12] are ascribed to the high-field endurance (~16 MV/cm) or large charge-to-breakdown endurance (~30 C/cm^2) as well as the shallow and deep bulk SiO_2 electron traps of these thin SiO_2 films.

Furthermore, a theoretical model has been proposed to describe the conduction mechanism and dielectric breakdown of a thin SiO_2 film in which the dynamic trapping (i.e., trapping and detrapping) and positive charge generation during high-field Fowler–Nordheim tunneling are considered. In addition, the weak spots and robust areas are distinguished so that the localized dielectric breakdown could be described. Finally, ramp-voltage-stressed *I–V* and high-frequency and quasi-static *C–V* measurements are performed to investigate the changes of field-enhancement factor, trapped electron density, and interface state density when a thin SiO_2 film is stressed with different amounts of charge. On the other hand, as the operation temperature increases, the electrical characteristics of a thin SiO_2 film are changed. Several important physical parameters affected by temperature variations are discussed, which include barrier height, trapped electron density, trap capture cross section, and trap generation rate.

II. Sample Preparation and Measurements

Silicon n-type wafers of ⟨100⟩ orientation with a resistivity of about 10 Ω · cm were used as the starting material to fabricate the poly-Si-gate MOS capacitors. After the standard cleaning process, a SiO_2 layer with a thickness of 500 Å was grown in dry O_2 ambient. Then, a heavily doped n$^+$ layer was formed beneath the Si–SiO_2 interface by using As implantation with a dose of 2×10^{14} cm^{-2} and an energy of 80 keV. After stripping the SiO_2 layer, a thin SiO_2 layer with a thickness of 110 ± 1 Å

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was thermally grown in dry O_2 ambient diluted with N_2 gas. An undoped poly-Si film with a thickness of 4500 Å was deposited on the oxide layer using the LPCVD reactor operated at 625°C and then doped with phosphorus dopants using a $POCl_3$ source. After aluminum metallization, the deposited aluminum film was photoengraved and etched to form the contact pattern. Besides, aluminum metallization on the back side of wafers was also performed to form the back side contact plate. Finally, all the wafers were sintered in forming gas at 450°C for 20 min.

The thickness of the SiO_2 film was measured by an autoellipsometer with a 6328-Å laser source. A C–V test was also performed to measure the thickness of the SiO_2 film and the result agrees well with that obtained by an ellipsometer. The ramp-voltage-stressed I–V and constant-voltage-stressed I–t measurements were performed using a HP4140B picoammeter. The constant-current-stressed V–t measurements were performed by using a Keithley 220 programmable current source and a Keithley 619 multimeter. Note that, except the I–V technique for bidirectional stressing, all the measurements were performed in the accumulation region. The high- and low-frequency C–V curves were measured by using a HP 4275A LCR meter and a HP4140B picoammeter, respectively. A desktop computer was implemented to control all the electrical instruments mentioned above and to manipulate all the experimental data.

III. Experimental Results of Reliability Tests

A typical ramp-voltage-stressed I–V characteristic curve for a MOS capacitor with a 110-Å thin SiO_2 film is shown in Fig. 1(a). This curve is replotted in Fig. 1(b) using the log (J/E^2) versus $1/E$ relationship, from which the Fowler–Nordheim tunneling current can be recognized. The ramp-voltage-stressed I–V measurement has been used as a useful method to determine the important trapping parameters, such as trapping density (N_t) and trap capture cross section (σ_t) [15]–[17]. Following the method proposed by Chen and Wu [17], the effective total trapping density (N_t) and trap capture cross section (σ_t) are evaluated to be 8.3×10^{12} cm^{-2} and 4.7×10^{-20} cm^2, respectively, and the recombination capture cross section (σ_i) is 1.5×10^{-18} cm^2.

The ramp-voltage-stressed I–V measurement has been widely used in the dielectric reliability concerns to indicate the TZDB [3], [5], [8]–[14], [18]–[21]. Besides, in order to quickly and easily obtain the results, the ramp-voltage-stressed I–V measurement has been suggested to replace the constant-voltage-stressed I–t measurement as a guide to predict the TDDB [3], [5], [19], [20]. Since the ramp voltage is related to the time with a ramping rate, the TZDB is conceptually not time-zero but time-dependent. Fig. 2(a) shows the ramp-voltage-stressed I–V characteristic curves with the ramping rate ranging from 0.01 to 1 V/s. From this figure, it can be found that the criterion of dielectric breakdown can be chosen to be the point where the current increases abruptly. There are two

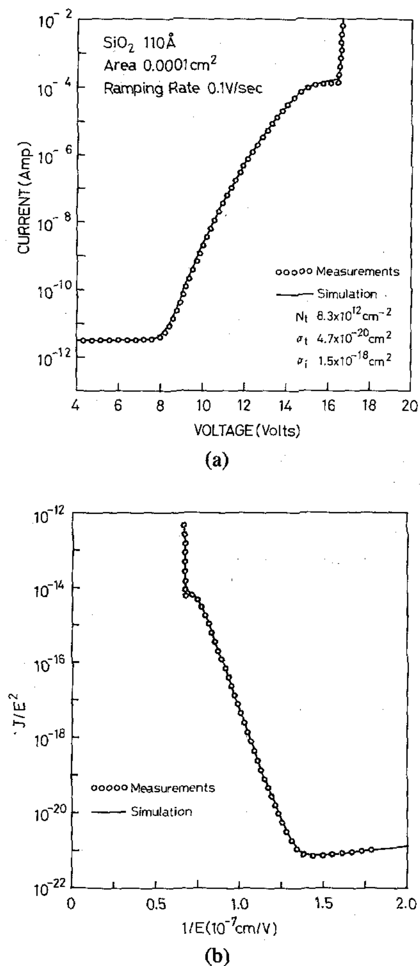
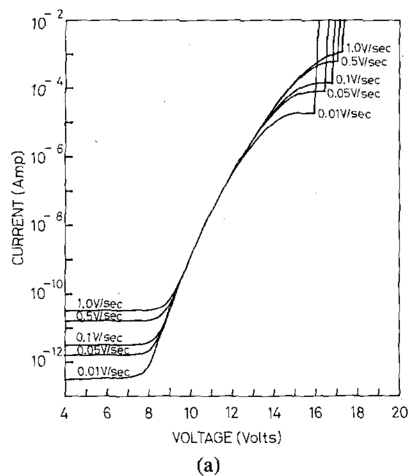


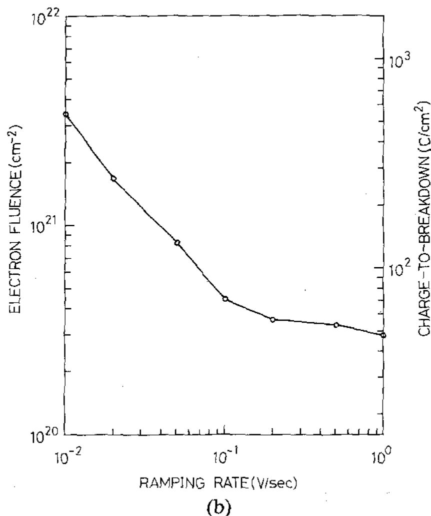
Fig. 1. The ramp-voltage-stressed I–V characteristic curve plotted in (a) the I versus V chart and (b) the log (J/E^2) versus $1/E$ chart.

features deserving attention from this figure: first, a constant displacement current I_d is concerned with a ramping rate γ via the relationship $I_d = C_{ox}\gamma$, and is the dominant current prior to the appearance of Fowler–Nordheim tunneling current; second, both the breakdown current and voltage increase with increasing the ramping rate. Furthermore, the total electron fluence (e/cm^2) before the occurrence of breakdown is found to be correlated with the ramping rate, as shown in Fig. 2(b). As can be seen, the electron fluences increase about one order of magnitude when the ramping rate decreases from 1 to 0.01 V/s.

In order to determine the dielectric breakdown histogram under a ramp-voltage stress, 103 MOS capacitors (randomly selected) were tested with a ramping rate fixed at 0.5 V/s and the results are shown in Fig. 3. Since the breakdown electric fields are all above 14.4 MV/cm and are mainly concentrated at 15.8 MV/cm, a high-field intrinsic dielectric breakdown can be assumed and thus the low-field defect-related breakdown caused by impurities, pin holes, microcracks, and particulates can be discarded. Compared with previous reports focused on the reliability of thin SiO_2 films ranging from 60 to 200 Å [7]–[14], the intrinsic integrity of this work is noticeable because of its extremely large charge to breakdown (>30 C/cm^2).



(a)



(b)

Fig. 2. (a) The ramp-voltage-stressed I-V characteristic curves with the ramping rate changing from 0.01 to 1 V/s and (b) the charge-to-breakdown (or electron fluence) versus the ramping rate.

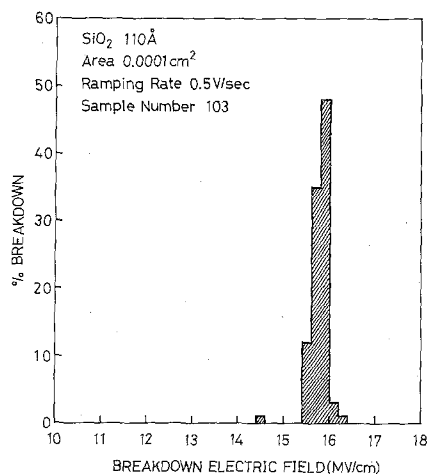


Fig. 3. Breakdown distributions under a ramp-voltage-stressed TZDB test. No dielectric breakdown occurs under an electric field of 10 MV/cm.

The constant-voltage-stressed TDDB has been extensively accepted to indicate the oxide breakdown reliability [1], [2], [4], [5], [8]–[12], [18], [21]. A general expression for the failure density function $f(t)$ showing the fraction of a population of samples that fail at a given time t can be approximately written as [1]

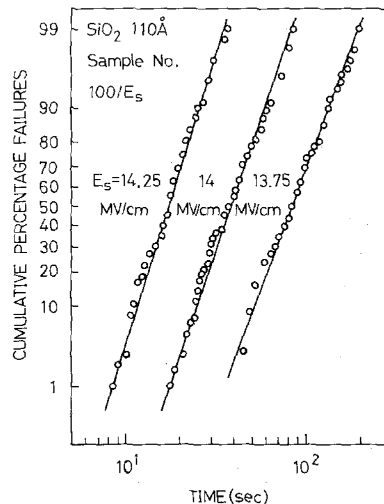


Fig. 4. Time-dependent dielectric-breakdown data for three different electric fields.

TABLE I
THE MEAN AND VARIANCE OF THE STRAIGHT LINES SHOWN IN FIG. 4

E_S (MV/cm)	μ_0	σ_0
13.75	2.058	0.170
14.00	1.695	0.145
14.25	1.354	0.135

$$f(t) = \frac{1}{\sqrt{2\pi} \cdot \sigma_0 t} \exp\left[-\frac{1}{2}\left(\frac{\ln t - \mu_0}{\sigma_0}\right)^2\right] \quad (1)$$

where μ_0 and σ_0 represent the mean and variance of the distribution, respectively.

The cumulative density function $F(t)$ demonstrating the cumulative percentage of sample that fail in the range from $t = 0$ to t can be calculated as

$$F(t) = \int_0^t f(t)\, dt. \quad (2)$$

It is expected that a straight line would be obtained when the cumulative density function $F(t)$ is plotted on a logarithmic normal probability chart.

Extremely high electric fields (13.75, 14, and 14.25 MV/cm) were used to stress the 110-Å MOS capacitors, and the currents were monitored to observe the TDDB. The test capacitors were arranged in a mesh, and the total number of samples was chosen to be 100. Fig. 4 shows the results of the TDDB tests, in which the cumulative density function $F(t)$ is plotted on a log normal chart. It can be seen that the straight lines can be obtained in the very high electric field region. The mean and variance extracted from these curves are listed in Table I.

The electric-field-acceleration factor (A_{EF}) for the TDDB between two stress fields has an empirical form

$$A_{EF} = \exp\left(\frac{E_0 - E_s}{E_{EF}}\right) \quad (3)$$

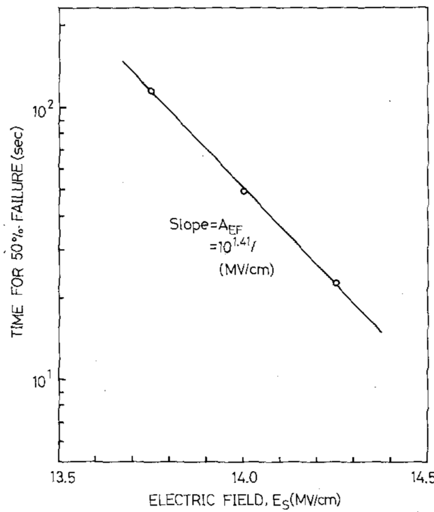


Fig. 5. Log time to reach 50-percent failure as a function of the electric field.

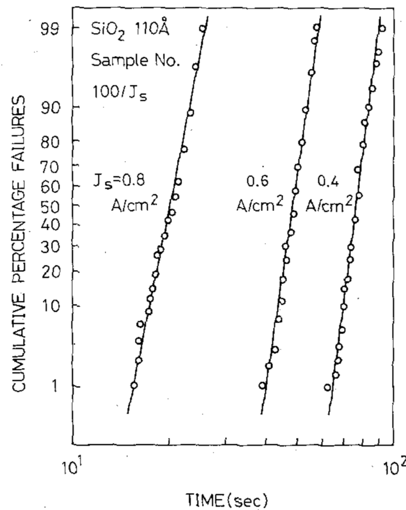


Fig. 6. Time-dependent dielectric-breakdown data for three different current densities.

where E_s is the stressing field, E_0 is the desired operating field, and E_{EF} is a constant determined from the experimental work.

The time for 50-percent failure shown in Fig. 4 is chosen to plot against the stressing field so that the electric-field-acceleration factor (A_{EF}) can be obtained and is shown in Fig. 5. The slope of the curve gives an electric-field-acceleration factor (A_{EF}) of $10^{1.41}/(MV/cm)$.

In addition to constant-voltage stress, constant-current stress can also be used as a method to define the TDDB. Mesh-arranged MOS capacitors with a total number of 300 were tested under three current density biases (0.4, 0.6, and 0.8 A/cm^2) and the variations of voltage across a thin oxide layer was monitored to observe the TDDB. Fig. 6 shows the cumulative density function $F(t)$ plotted on a logarithmic normal probability chart. It is interesting to note that straight lines are obtained. The calculated mean and variance of these curves are listed in Table II. The time for a 50-percent failure with respect to the current

TABLE II
THE MEAN AND VARIANCE OF THE STRAIGHT LINES SHOWN IN FIG. 6

J_S (A/cm^2)	μ_o	σ_o
0.4	1.347	0.050
0.6	1.713	0.039
0.8	1.907	0.033

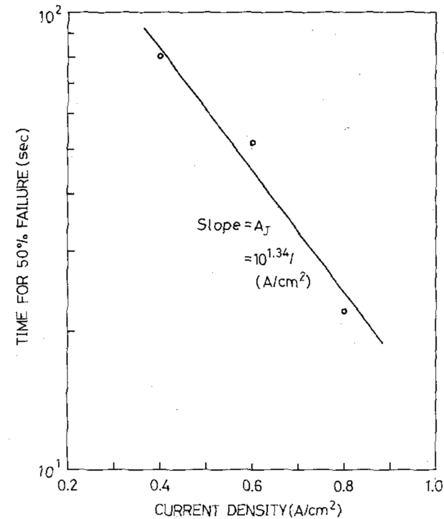


Fig. 7. Log time to reach 50-percent failure as a function of the current density.

density is plotted in Fig. 7. From the slope of this curve, the current-density acceleration factor (A_J) is calculated to be $10^{1.34}/(A/cm^2)$.

Since the ramp-voltage-stressed TZDB and the constant-voltage-stressed and constant-current-stressed TDDB's are all substantially dependent on time, the temperature effects of these three stress methods become interesting. It is well known that the thermal acceleration factor (A_T) can be derived from an Arrhenius equation

$$A_T = \exp\left[\frac{E_a}{k_B}\left(\frac{1}{T_s} - \frac{1}{T_0}\right)\right] \tag{4}$$

where T_s is the stress temperature, T_0 is the desired operating temperature, k_B is the Boltzmann's constant, and E_a is the activation energy.

As the temperature increases from 25 to 275°C, the breakdown voltage under a ramp-voltage stress decreases. A ramp voltage with a ramping rate fixed at 0.1 V/s was used to stress the mesh-arranged MOS capacitors. Twenty MOS capacitors were tested at each temperature period and the average value of breakdown voltage was registered. Fig. 8 shows the results of breakdown voltage (V_{BD}) with respect to $1/T$. It is very interesting to find that two straight lines appear, one above 150°C and the other below 150°C. The activation energies can be extracted from the slope of these curves, which gives 0.21 eV (≤ 150°C) and 0.64 eV (> 150°C).

From the constant-voltage-stressed and constant-current-stressed TDDB's, both show a faster time to breakdown when the temperature increases. At each tempera-

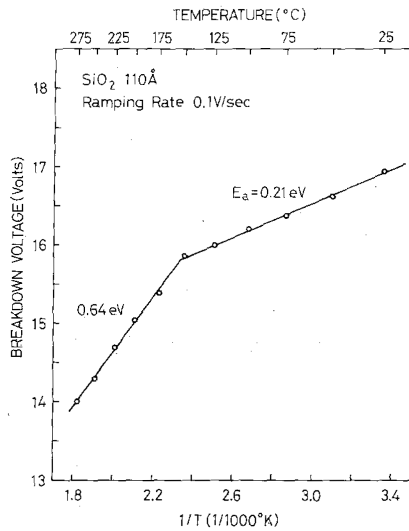


Fig. 8. The Arrhenius plot for the breakdown voltage deduced from ramp-voltage-stressed TZDB data.

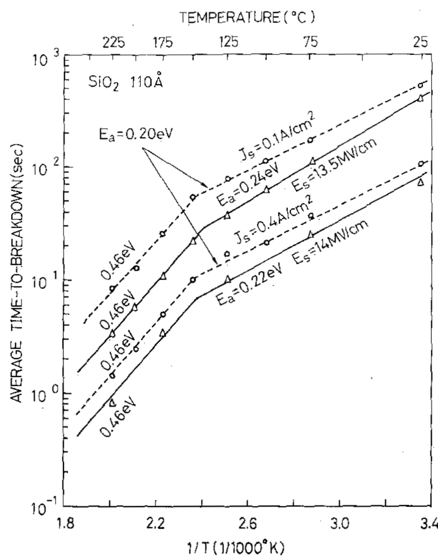


Fig. 9. The Arrhenius plots for the average time to breakdown deduced from constant-voltage-stressed and constant-current-stressed TDDB data.

ture period, 20 MOS capacitors were stressed under either a constant voltage or a constant current, and the average value of time-to-breakdown was recorded. Fig. 9 shows the results of the constant-voltage-stressed TDDB with electric fields of 13.5 and 14 MV/cm as well as the constant-current-stressed TDDB with current densities of 0.1 and 0.4 A/cm^2. Similar to the results of the ramp-voltage-stressed TZDB, there are two activation energies for each stress condition. The activation energies deduced from Figs. 8 and 9 are summarized in Table III. It is interesting to find that different stress methods always give the same trend for the temperature effect. This fact suggests that the lifetime of dielectric films can be predicted by the ramp-voltage-stress method.

IV. Theoretical Model

In general, electrons will become hot when the magnitude of the electric field across an oxide film is larger than 4 MV/cm and the steady-state energy relaxation distance has been found to be 23–40 Å [22], [23]. As the electric field increases further (e.g., >9 MV/cm), scattering mechanisms other than longitudinal optical phonon scattering are responsible for maintaining the average electronic energy equal to or larger than 4 eV with respect to the bottom of the SiO_2 conduction band [22], [23]. Several mechanisms have been suggested to dissipate the excess energy in a thin SiO_2 film, which are trap-to-band impact ionization [24], band-to-band impact ionization [25], [26], and acoustic phonon scattering [22], [23].

For a thin SiO_2 film, a localized electric field may occur, which may be due to Si–SiO_2 interface roughness [27], nonuniform trap distribution, dopant impurity segregation from poly-Si grain boundary region [28], highly mobile sodium [29], and other positive charges [30]. It has been shown that a thin oxide film under a high-field stress may aggregate positive charges near the Si–SiO_2 interface. These positive charges may be due to the drift of positive ions resulted from hot-electron impact ionization [26], the diffusion of neutral species such as atomic hydrogen [31], [33] or excitons [34] created by bond-breaking through energetic avalanche-injected electrons and then trapped by the dangling bonds at the interface, and the broken bond at the interface during the passage of heating electrons [35]–[37].

For a high-quality thin oxide film grown on a heavily doped silicon substrate as described in the previous section, the breakdown mechanism under a high-field stress is mainly due to the intrinsic breakdown, and the defect-related breakdown will be screened out in the proposed model. It is assumed that the localized electric field exists in the weak spots; the positive charges resulted from all the sources mentioned above may aggregate near the SiO_2–Si interface within the weak spots. Futhermore, the weak spots can collect the positive ions generated by hot-electron impact ionization, and these generated positive ions may drift and then aggregate near the Si–SiO_2 interface within the weak spots. Therefore, the localized electric field in the weak spots will be further enhanced and dielectric breakdown would be initiated in the weak spots. However, in the robust area the accumulation of positive charges near the Si–SiO_2 interface is assumed to be due to the diffusion of neutral species and the broken bond at the interface. According to the above descriptions, the weak spots and robust areas of a thin SiO_2 film in a biased silicon-gate MOS capacitor structure are shown in Fig. 10(a). The energy-band diagrams describing the weak spots and robust areas are shown in Fig. 10(b) and (c), respectively. From the energy-band diagram, as electrons tunnel from the Si-substrate into the SiO_2 conduction band under high-field stress, electron trapping as well as positive charge generation would occur. Using the charge sheet model, the trapped electron and generated positive charge centroids can be located at $\overline{X}_n$ and $\overline{X}_p$, respectively. Note that the distribution of the weak spots may be nonuniform and the localized field enhancement may be different among the weak spots; a statistical (or logarithmic

TABLE III
THE ACTIVATION ENERGIES DEDUCED FROM FIGS. 8 AND 9

Stress Method	Stress Condition		Activation Energy E_a(eV)	
			≤150°C	>150°C
Ramp-voltage-stress TZDB	γ=0.1 V/sec		0.21	0.64
Constant-voltage-stress TDDB	E_s	13.5 MV/cm	0.24	0.46
		14.0 MV/cm	0.22	0.46
Constant-current-stress TDDB	J_s	0.1 A/cm^2	0.20	0.45
		0.4 A/cm^2	0.20	0.46

normal) distribution for the dielectric breakdown events is adopted.

Since the excess positive charges resulted from the generated positive ions due to hot-electron impact ionization are accumulated near the SiO_2–Si interface within the weak spots, a positive regenerative process that will result in the dielectric breakdown of a thin oxide film is then initiated. Therefore, it is assumed that a thin oxide film would break down if the excess positive charge density near the SiO_2–Si interface within the weak spots reaches a critical value. This critical value is process-dependent and can be determined from comparisons between the measured ramp *I–V* characteristics and the developed model.

When a constant current flows through a thin SiO_2 layer, the variation of voltage across this layer depends on the extent of electron trapping and positive charge generation. In general, it is known that electron trapping would enlarge the variation of voltage, while positive charge generation would reduce it. Fig. 11 shows the change of voltage under different constant-current stresses. As can be seen, the voltage increases steadily until dielectric breakdown takes place. Since the voltage across the oxide layer does not saturate, trap generation plays an important role during this process. If a constant and finite trap generation rate g, which is defined as number of traps generated per electron flow, is assumed [38], the variation of voltage across a thin oxide layer can be easily calculated. Based on our previous analysis [46]. the variation of voltage across a thin oxide layer for a constant-current stress can be expressed by

$$\Delta V^+(t) = \frac{q}{\epsilon_{ox}}(T_{ox} - \overline{X}_n)\left\{\frac{jg}{q}t - \frac{g}{\sigma_g}\left[1 - \exp\left(-\frac{\sigma_g j}{q}t\right)\right] + N_t\left[1 - \exp\left(-\frac{\sigma_t j}{q}t\right)\right]\right\} \quad (5)$$

where N_t and σ_t are the total trapping density and trap-capture cross section pertaining to the original traps, respectively; σ_g is the trap capture cross section pertaining to the generated traps; j is the constant current density; ϵ_{ox} is the dielectric permittivity of the thin SiO_2 films; and q is the electronic charge.

Once electrons are trapped in a thin SiO_2 film, the anode field is enhanced by

$$\Delta E_a(t) = \frac{q}{\epsilon_{ox}}\left\{\frac{jg}{q}t - \frac{g}{\sigma_g}\left[1 - \exp\left(-\frac{\sigma_g j}{q}t\right)\right] + N_t\left[1 - \exp\left(-\frac{\sigma_t j}{q}t\right)\right]\right\}. \quad (6)$$

Trap-to-band and/or band-to-band impact ionization could be initiated if the anode field attains a threshold value, for instance, 15 MV/cm for band-to-band impact ionization [39]. The total positive charges $\theta_{it}^+(t)$ generated from the impact ionization process can be written as

$$\theta_{it}^+(t) = \frac{j}{q}\int_0^t\left[\int_{T_t}^{T_{ox}} \alpha dx\right]dt \quad (7)$$

where α is the impact ionization coefficient.

Using a standard form for the impact ionization coefficient, we have $\alpha = \alpha_0 \exp(-H/E)$, where α_0 and H are the constants determined by the kinds of impact ionization, and E is the electric field. Putting this expression into (7) we obtain

$$\theta_{it}^+(t) = \frac{\alpha_0 j}{q}\int_0^t\left[(\overline{X}_n - T_t)\exp\left(-H/E_m(t)\right) + (T_{ox} - \overline{X}_n)\exp\left(-H/E_a(t)\right)\right]dt$$

where $E_m(t)$ and $E_a(t)$ are the electric fields in the middle region and the anode, respectively, which have been calculated in [17] and [46].

Taking electron recombination with these positive charges into consideration, the rate equation can be expressed as

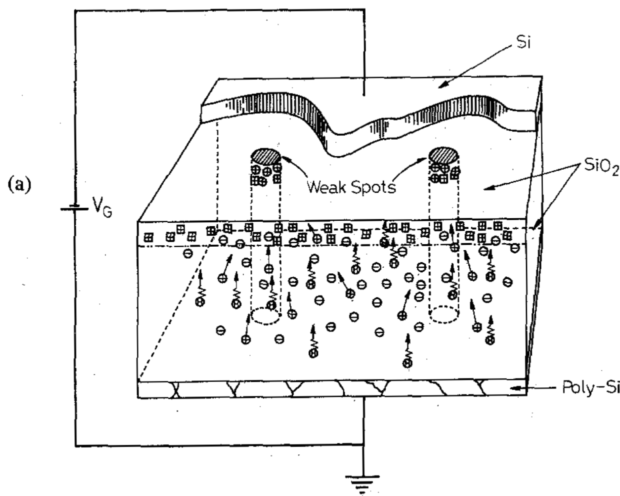
$$\frac{dn_i(t)}{dt} = \frac{\sigma_i j}{q}\left[\theta_i^+(t) - n_i(t)\right] \quad (8)$$

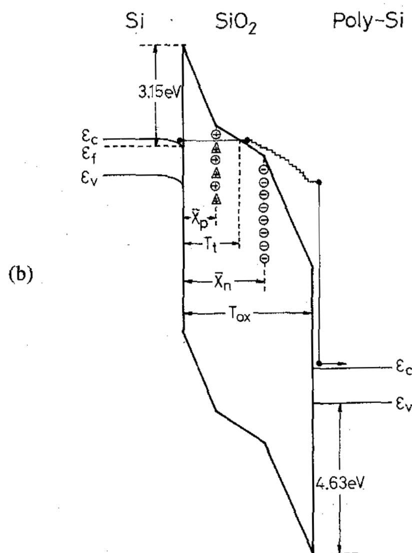
and

$$\theta_i^+(t) = \theta_{it}^+(t) - n_i(t) = \frac{\theta_{it}^+(t)}{2 - \exp\left(-\frac{\sigma_i jt}{q}\right)} \quad (9)$$

where $n_i(t)$ is the density of the recombined electrons, and σ_i is the recombination capture cross section.

Based on the assumption that the positive ions generated from impact ionization will aggregate near the cath-





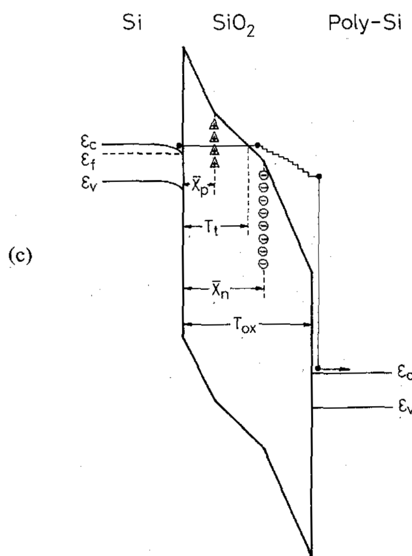


Fig. 10. (a) Theoretical model showing electron trapping, positive charge generation, weak spots, and robust area; (b) energy-band diagram of the weak spots; and (c) energy-band diagram of the robust area. ⊖ represents the trapped electron; ⊕ represents the positive ions generated from impact ionization and other hot-electron scattering; ⊕ represents the neutral species; and △ and ⊞ represent the positive charges generated from the diffusion of neutral species and the broken bond at the interface.

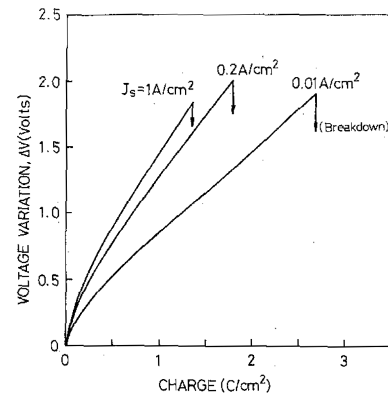


Fig. 11. The variation of voltage versus the flow charges for three constant-current densities.

ode region within the weak spots, the variation of voltage across a thin SiO_2 film becomes

$$\Delta V(t) = \frac{q}{\epsilon_{ox}} (T_{ox} - \bar{X}_n) \left\{ \frac{jg}{q} t - \frac{g}{\sigma_g} \left[1 - \exp\left(-\frac{\sigma_g j}{q} t \right) \right] + N_t \left[1 - \exp\left(-\frac{\sigma_t j}{q} t \right) \right] \right\} - \frac{q}{A_{r0}\epsilon_{ox}} (T_{ox} - \bar{X}_p) \left[\frac{\theta_{it}^{+}(t)}{2 - \exp\left(-\frac{\sigma_i j}{q} t \right)} \right] \quad (10)$$

where A_{r0} is the ratio of the weak spots area and the total area (i.e., A_w/A).

Although the breakdown mechanisms have been proposed by considering only a small to moderate rate of impact ionization [40]–[43], the accumulation of positive ions near the cathode region within the weak spots does give a good criterion for dielectric breakdown.

V. Experimental Results and Discussions

A. Electron Trapping and Positive Charge Generation

In order to demonstrate electron trapping and positive charge generation, constant-current stress together with ramp-voltage-stressed I–V as well as high-frequency and quasi-static C–V measurements have been performed. Fig. 12(a) shows the I–V characteristics of a thin SiO_2 MOS capacitor stressed with different amounts of charge. Electron trapping can be clearly seen from the positive shift of the stressed I–V curves with respect to the fresh one. However, the shape of these stressed I–V curves deviates from the typical form of Fowler–Nordheim tunneling current as compared with the fresh one. Considering the band diagrams shown in Fig. 10(b) and (c), the Fowler–Nordheim tunneling current density through the robust area and the weak spots can be given by [46]

$$j(t) = \frac{q^2(\mu E_c)^2 m}{16\pi^2 \hbar \Phi_b m^*} \cdot \frac{\pi C k_B T}{\sin(\pi C k_B T)} \cdot \{T_t\} \quad (11)$$

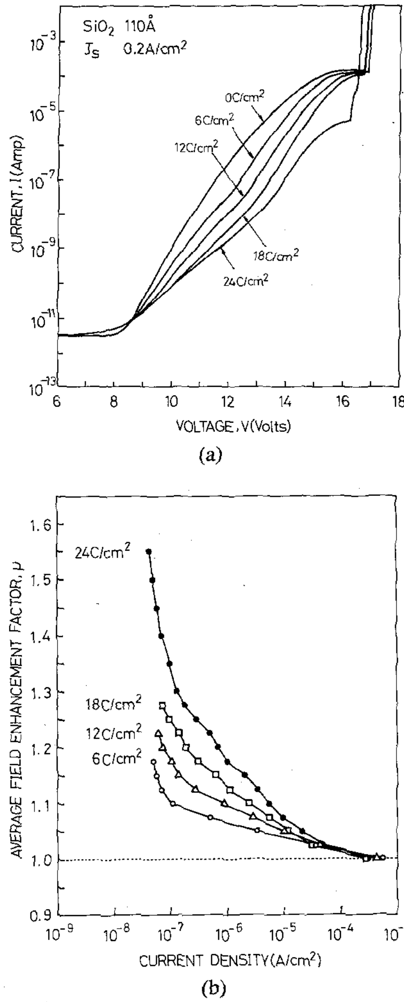


Fig. 12. (a) The ramp-voltage-stressed I–V characteristic curves with and without a constant-current stress and (b) the average field-enhancement factor versus the current density for the stressed I–V curves shown in (a).

and

$$T_t = \exp\left\{-\frac{4\sqrt{2m^*q}}{3\hbar\mu}\left[\frac{\Phi_b^{3/2}}{E_c} + (\Phi_b - E_c\overline{X}_p)^{3/2}\left(\frac{1}{E_m} - \frac{1}{E_c}\right)\right]\right\} \quad (12)$$

$$C = \frac{2\sqrt{2m^*q}}{\hbar\mu}\left[\frac{\Phi_b^{1/2}}{E_c} + (\Phi_b - E_c\overline{X}_p)^{1/2}\left(\frac{1}{E_m} - \frac{1}{E_c}\right)\right] \quad (13)$$

where $\hbar$ is Planck's constant divided by 2π; m^* is the effective mass of tunneling electrons in a SiO_2 film and is assumed to be 0.5 m; Φ_b is the barrier height; T is the temperature; and μ is the field-enhancement factor, which may be different for the robust area and the weak spots.

The total current across the oxide layer can be written as [17]

$$I = C_{ox}\gamma + qA\frac{d\theta_{it}^+(t)}{dt} + j_wA_w + j_rA_r \quad (14)$$

where j_w and j_r are the current densities across the weak spots and the robust area, respectively; A is the total area; A_w and A_r are the area of the weak spots and the robust region, respectively.

Assuming the A_w is equal to 10^{-6} Å, the field-enhancement factor μ of the stressed I–V curves shown in Fig. 12(a) can be simulated [47] and is shown in Fig. 12(b). The field-enhancement factor is increased with the amounts of the stressed charges, and this is attributed to the positive charges generated near the Si–SiO_2 interface. The decrease of the field-enhancement factor as the electric field increases has been proposed [44]; therefore, it is not surprising that the field-enhancement factor decreases with increasing the current density.

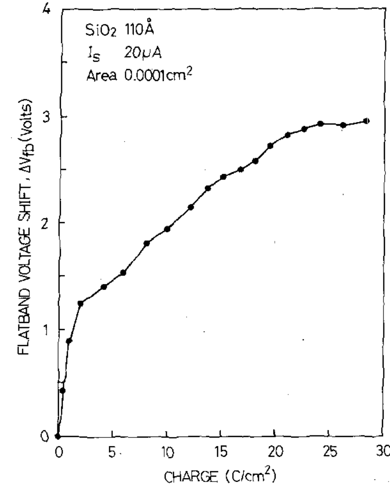


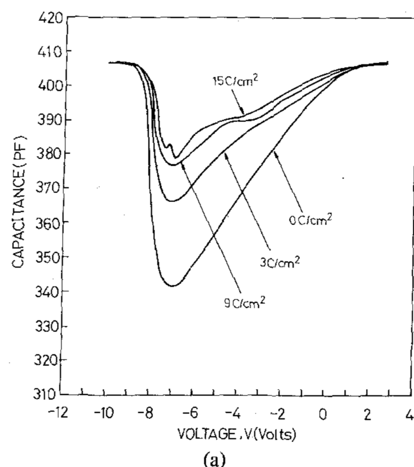
Fig. 13. The flat-band-voltage shift versus the stressed changes under 1-MHz high-frequency C–V measurements.

The flat-band-voltage shift ΔV_{fb} deduced from high-frequency (1-MHz) C–V measurements for a thin SiO_2 MOS capacitor stressed to different extends is shown in Fig. 13. As can be seen, the flat-band-voltage shift increases abruptly right after stressing and reaches a saturation value when the total charge flow is above 24 C/cm^2. The flat-band-voltage shift is correlated with the trapped electron density $n_t(t)$ by

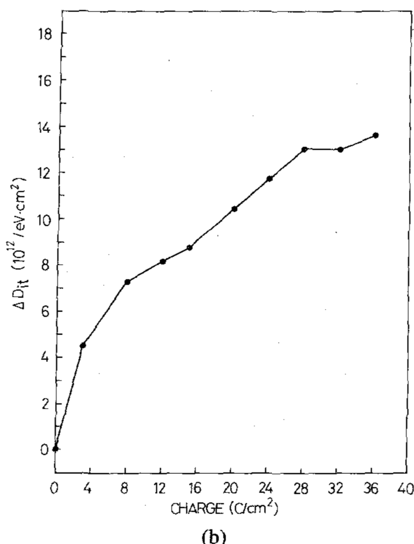
$$\Delta V_{fb} = \frac{qn_t(t)}{\epsilon_{ox}}(T_{ox} - \overline{X}_n). \quad (15)$$

Using the bidirectional I–V measurement [38], the trapped electron centroid $\overline{X}_n$ was found to be 74.8 Å in the high charge flow region. Therefore, the trapped electron density can be calculated, and a saturation value of 1.78×10^{13} cm^{-2} is derived. This slightly large value is reasonable when considering both the trapping and detrapping processes [24].

The quasi-static C–V curves for the thin SiO_2 MOS capacitors stressed with different amounts of charge are shown in Fig. 14(a). It can be seen that the interface-state density D_{it} increases with increasing the stressed charges. Fig. 14(b) shows the variation of the interface-state density with respect to the stressed charges. Although the turn-around effect, which shows the compensation between the trapped electrons and the positive interface-state



(a)



(b)

Fig. 14. (a) The quasi-static $C-V$ curves for the MOS capacitors stressed with different amounts of charges and (b) the change of the interface-state density versus the stressed charges.

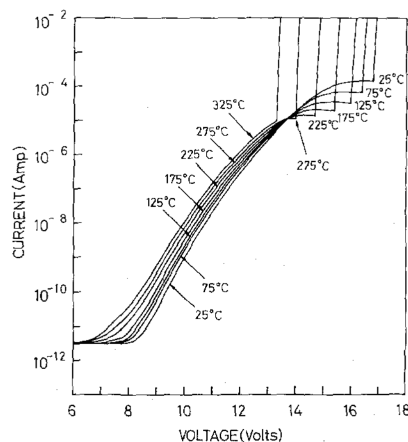


Fig. 15. The ramp-voltage-stressed $I-V$ characteristic curves for different temperatures.

charges during high-field tunneling [31], [45], does not appear in the flat-band-voltage shift as shown in Fig. 13, the saturation of flat-band-voltage shift indicates that the contribution of positive interface-state charges still cannot be neglected. Since both the field-enhancement factor and the interface-state density are increased as the stressed charges are increased, field enhancement due to the aggregation of positive charges near the $Si-SiO_2$ interface can be ascertained.

B. Temperature Effects

When the temperature increases, the charge-to-breakdown is greatly reduced and the activation energies have been obtained as shown in Figs. 8 and 9. In order to observe the variations of physical parameters with respect to the temperature, the ramp-voltage-stressed $I-V$ measurements have been performed at various temperatures ranging from 25 to 325°C. Fig. 15 shows the results of these measurements, in which the trapping ledges can be clearly observed. The conduction mechanism across the thin SiO_2 films obeys the Fowler–Nordheim tunneling mechanism and the related equation is (11). Since the Fowler–Nordheim tunneling current is essentially temperature-insensitive, the larger leakage current shown in Fig. 15 as the temperature increases can be ascribed to the reduction of the barrier height. The barrier height has been calculated by using (11) through (14), and the result is shown in Fig. 16(a). It is interesting to find that a nearly linear relationship exists between the barrier height and the temperature. The slope of this straight line has been calculated to be -5.2×10^{-4} eV/°C. Another feature of merit deserving attention is the trapping effect as well as the dielectric breakdown, which can be seen from the trapping ledges shown in Fig. 15. Some important hints yielded from this figure are as follows: 1) Due to the shrinkage of the trapping-ledge width, the number of trapped electrons decreases as the temperature increases. 2) Due to the descent of the trapping ledge, the capture cross section pertaining to the effective traps becomes large as the temperature increases. 3) Due to the acceleration of di-electric breakdown, the trap-generation rate concerned with dielectric breakdown may be accelerated as the temperature increases. Here, we can postulate that the shallow-electron traps in the bulk oxide with smaller activation energy become inefficient due to thermal field emission at high temperature, and the deep-electron traps with large activation energy available for capturing electrons become dominant when the temperature increases. Besides, the enlargement of the trap capture cross section at high temperature may be due to the larger capture capability of deep electron traps at that temperature or the increase of the total amount of electron traps when considering that some of them may be detrapped via a thermal field-emission process right after electron trapping. The trap capture cross section extracted from Fig. 15 is shown in Fig. 16(b).

The acceleration of the trap generation rate with respect to various temperatures can be observed from the $V-t$ curves shown in Fig. 17, in which the thin oxide is stressed with 0.1 A/cm^2. It is shown that the voltage across the thin oxide film changes very quickly at high temperature, which is mainly due to the increase of the

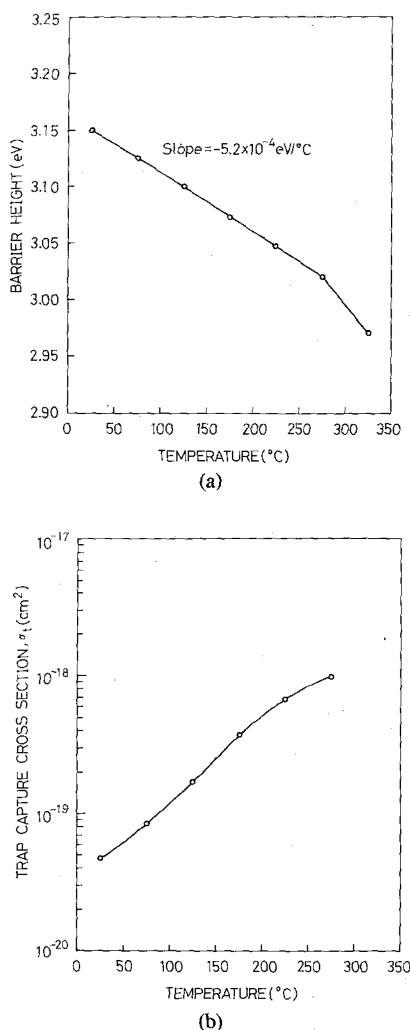


Fig. 16. (a) The barrier height versus the temperature and (b) the trap capture cross section σ_t versus the temperature as deduced from Fig. 15.

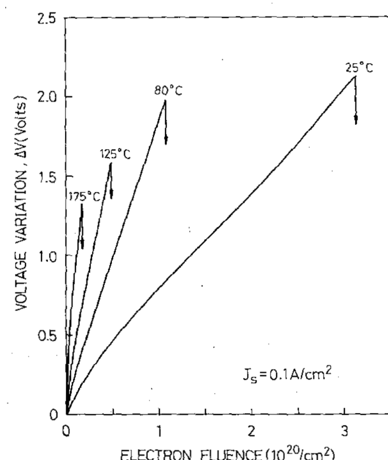


Fig. 17. The variation of voltage versus electron fluence for different temperatures.

trap generation rate g. However, the increase of the trap generation rate may result from hydrogens released from the bonded configurations of Si-H and Si-OH [32] as the temperature increases. This fact would lead to not only the electron traps but also the highly mobile hydrogen ions. Since the generated electrons can enhance the anode field and the highly mobile hydrogen ions can accelerate the positive regeneration process, the dielectric breakdown of a thin oxide film is then sped up.

VI. Summary

The dielectric reliability of the intrinsic thin SiO_2 films thermally grown on a heavily doped n-type Si substrate has been studied. Both the TZDB (ramp-voltage-stressed I–V) and the TDDB tests (constant-voltage-stressed I–t and constant-current-stressed V–t) of these thin SiO_2 films have been performed, and the results show the same trend under different stress methods. Under the TZDB test, the charge-to-breakdown (or electron fluence) is found to be larger for a smaller ramping rate. A histogram of the TZDB data with a ramping rate of 0.5 V/s shows that most of the test samples have breakdown fields in the range of 15.4 to 16.4 MV/cm. The activation energies deduced from the TZDB measurements are 0.21 eV ($\leq 150°C$) and 0.64 eV ($> 150°C$). On the other hand, constant-voltage-stressed and constant-current-stressed TDDB data satisfy the logarithmic normal distribution. The electric-field-acceleration factor A_{EF} and current-density-acceleration factor A_J are found to be $10^{1.41}/(\text{MV/cm})$ and $10^{1.34}/(\text{A/cm}^2)$, respectively. The activation energies are found to be 0.23 ± 0.01 eV ($\leq 150°C$) and 0.46 eV ($> 150°C$) under the constant-voltage-stressed TDDB measurements, and 0.20 eV ($\leq 150°C$) and 0.46 eV ($> 150°C$) under the constant-current-stressed TDDB measurements. To compare with other reliability data on SiO_2 films, Table IV lists the electric-field-acceleration factor A_{EF} and the activation energy E_a presented in earlier papers. As can be seen, the electric-field-acceleration factor derived from this work is smaller than those published. Moreover, there are two distinct activation energies that are different from those obtained previously. The smaller electric-field-acceleration factor may be due to the high-field-endurance (e.g., ~ 16 MV/cm) or large charge-to-breakdown endurance (e.g., $\sim 30\ \text{C/cm}^2$) of our high-quality intrinsic thin SiO_2 films. The smaller (for temperatures $\leq 150°C$) and larger (for temperatures $> 150°C$) activation energies are attributed to the shallow-bulk SiO_2 electron traps that dominate at low temperature and deep-bulk SiO_2 electron traps that dominate at high temperature, respectively.

A theoretical model has been proposed to describe the conduction mechanism and dielectric breakdown of an intrinsic thin SiO_2 film. In this model, dynamic trapping (i.e., electron trapping and detrapping) and positive charge generation are considered. Moreover, the weak spots and robust areas are included to describe the well-known localized breakdown phenomenon. The positive charges generated from the diffusion of neutral species and the broken bond at the interface during the passage of heating electrons are assumed to aggregate near the Si–SiO_2 interface in both the weak spots and robust areas. On the other hand, the positive ions originated from trap-to-band and/or band-to-band impact ionization and other

TABLE IV
THE ELECTRIC-FIELD-ACCELERATION FACTOR (A_{EF}) AND ACTIVATION ENERGY (E_a) PRESENTED IN EARLIER PAPERS

Reference	Gate Materials	T_{ox} (Å)	Temp (°C)	A_{EF} (1/(MV/cm))	E_a (eV)
Crook [1]	Poly-Si	≥400	25 ∿ 160	10^{7}	0.3 ∿ 0.35
Anolick et al. [2]	Al	450	85 ∿ 250	$10^{1.5\pm0.49}$	2.1
Domangue et al. [5]	Poly-Si	390	25 ∿ 150	$10^{2.0}$	0.36
Tathuma [6]	Poly-Si	400	∿	$10^{1.7}$	0.26
Willians et al. [7]	Poly-Si	100∿200	∿	10^{4}	1.0
Hirayama et al. [8]	Poly-Si	100∿400	∿	$10^{5.6}$	∿
Baglee [9]	Poly-Si	100	25 ∿ 150	$10^{1.85}$∿$10^{2.0}$	0.3
Yamabe [11]	Poly-Si	200	20 ∿ 250	$10^{2.5}$	0.3
Hokari [12]	Poly-Si	60∿100	170∿250	$10^{1.74}$∿$10^{1.90}$	1.0 ∿ 1.1
This Work	Poly-Si	110	25 ∿ 275	$10^{1.41}$	0.23±0.01 (≤150°C) 0.46 (>150°C)

hot-electron scatterings are assumed to drift toward the Si–SiO_2 interface in the weak spots where the electric fields are locally enhanced. Consequently, the accumulation of more positive charges in the weak spots would reinforce the original field enhancement, and leads to a positive regeneration process that forms the criterion of dielectric breakdown for TZDB and TDDB. Furthermore, the statistical (or logarithmic normal) distribution for the dielectric breakdown events is due to nonuniform weak spot distribution and different field enhancement among the weak spots.

Using high-frequency and quasi-static C–V measurements, the trapped electron density and interface-state density are found to increase with increasing the amount of charge flow. Furthermore, the field-enhancement factors have been evaluated for the thin SiO_2 films stressed with different amounts of charge by using the ramp-voltage-stressed I–V technique. The field-enhancement factors are found to be larger with a larger amount of charge flow. This fact is consistent with the results of C–V measurements.

Finally, the temperature effects of an intrinsic thin SiO_2 film are investigated. As the temperature increases, the electrical characteristics of a thin SiO_2 film are changed. The sources to force this change are due to the variations of the following physical parameters: 1) The barrier height is found to decrease when the temperature increases, and a linear relationship with a slope of -5.2×10^{-4} eV/°C is obtained. 2) The number of trapped electrons becomes less when the temperature increases. This is ascribed to the thermal field-emission effect that makes the shallow-bulk SiO_2 electron traps inefficient. 3) The capture cross section subjected to the effective traps becomes large when the temperature increases. This is ascribed to the larger capture capability of deep-electron traps at high temperature or the increase of the total amount of electron traps when considering that some of them detrapped via thermal field emission process right after electron trapping. 4) The trap generation rate is found to increase when the temperature increases and this will result in a faster dielectric breakdown at high temperature.

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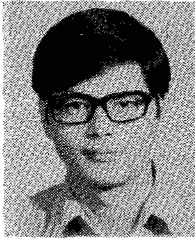

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