國立交通大學

電機學院　電機與控制學程

碩士論文

降低寄生元件效應的固定導通時間控制於使用陶瓷電容的降壓電源轉換器

Reduction of Parasitic Component Effect in Constant On-Time Control for Buck Converter with Multi-layer Ceramic Capacitors

研究生：徐貴園

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中華民國一百零一年八月

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摘　　要

近年來隨著可攜式產品的需求逐漸增加，用來提供可攜式產品系統電源且具有小體積以及高效能的電壓穩壓器變得越來越重要。實際應用中固定導通時間控制法的電壓穩壓器常被使用，因為具有幾項優點，如系統結構簡單、快速暫態反應，以及在輕負載時具有高效率的優點。一般來說，固定導通時間控制法的穩壓器是利用輸出端訊號的漣波來穩壓，基本上須使用較大等效串聯電阻的輸出電容才可有效控制系統。由於低成本的優勢，積層陶瓷電容目前被廣泛的使用於消費性電源管理晶片，但是積層陶瓷電容的等校串聯電阻卻很小。在傳統的控制法使用具有小等效串聯電阻的輸出電容時，由於輸出端訊號的漣波幾乎僅有電容的成分，故漣波很小系統易受雜訊影響。

因此，本文提出新的固定導通時間控制法電壓穩壓器架構，可提高雜訊容限寬度，可消除輸出電容上的等效串聯電感及小等效串聯電阻效應。並且由於導通時間可隨輸入及輸出電壓調整，操作在連續導通模式時的系統切換頻率可以在廣泛的輸入電壓裡維持幾乎定值。模擬結果顯示出輸出電壓漣波維持約 2 mV，在負載變動範圍為 0 到 600 mA 時。此時使用的等效串聯電阻小於 5 mΩ。

Reduction of Parasitic Component Effect in Constant On-Time Control for Buck Converter with Multi-layer Ceramic Capacitors

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ABSTRACT

In recent years, with the increasing demand of portable products, used to provide system power of portable products with small size and high performance voltage regulator becomes more and more important. Constant on-time control regulators are preferred in practice for several important advantages, such as simple system structure, fast response time and high efficiency for light load. In general, constant on-time control regulators regulate their output voltage based on the ripple component in the output signal. Basically, requires the use of large equivalent series resistance (ESR) of the output capacitance can be effectively controlled system. As a low-cost advantage, multilayer ceramic capacitors (MLCC) are widely used in consumer power management chip, but its equivalent series resistance is very small.

In conventional constant on-time control with small ESR value on the output capacitor, the regulator is easily affected by the noise due to small output ripple, which is dominated by the ripple on the output capacitor.

Therefore, this paper proposes new constant on-time control regulator structure can improve the noise margin, to eliminate the equivalent in series inductance (ESL) and the small equivalent series resistance (ESR) effect. Furthermore, since the on-time period is set simply by input and output voltages, the switching frequency in continuous conduction mode (CCM) operation is relatively constant over a wide input voltage range. Simulation results show that the output ripple keeps around 2mV, when load current step is 600mA and ESR is smaller than 5mΩ.

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貴園 于 仲夏

國立交通大學

中華民國一百零一年八月

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Chapter 1

Introduction

1.1 Background of Regulators

In recent years, the portable and battery powered products such as tablet PC, personal digital assistants (PDA), cellular phones, etc., are increasingly demanded more and more. System's lifetime time is a factor to enhance the worth of the electronic devices in consumer's market. However, there are many difficulties and limitations to increase the capacity of stored energy device liked as battery equipment. Consequently, power management has become more popular and important subject. That is, how to extend the system operation time and use energy efficiently is a critical issue that engineers mostly concerned.

Furthermore, power management ICs should be essentially designed under the consideration of accomplishing high performance, high-efficiency and low-cost. For meeting these requirements, there are many different kinds of power management architectures could be used, such as buck converter, boost converter, low drop-out (LDO) linear regulator and charge pump, operating with step-up, step-down or inverting voltage. Take cell phone for example, the basic power management system diagram of cell phone is shown in Fig. 1 [1]. The core system includes control unit, processor and many power devices integrated. The control unit can control the state of power device such as sleep, shutdown or active. In this way, we can enhance the operation time and make the power dissipation minimized. This is the reason why the power management system becomes more and more considerable, especially for portable devices.

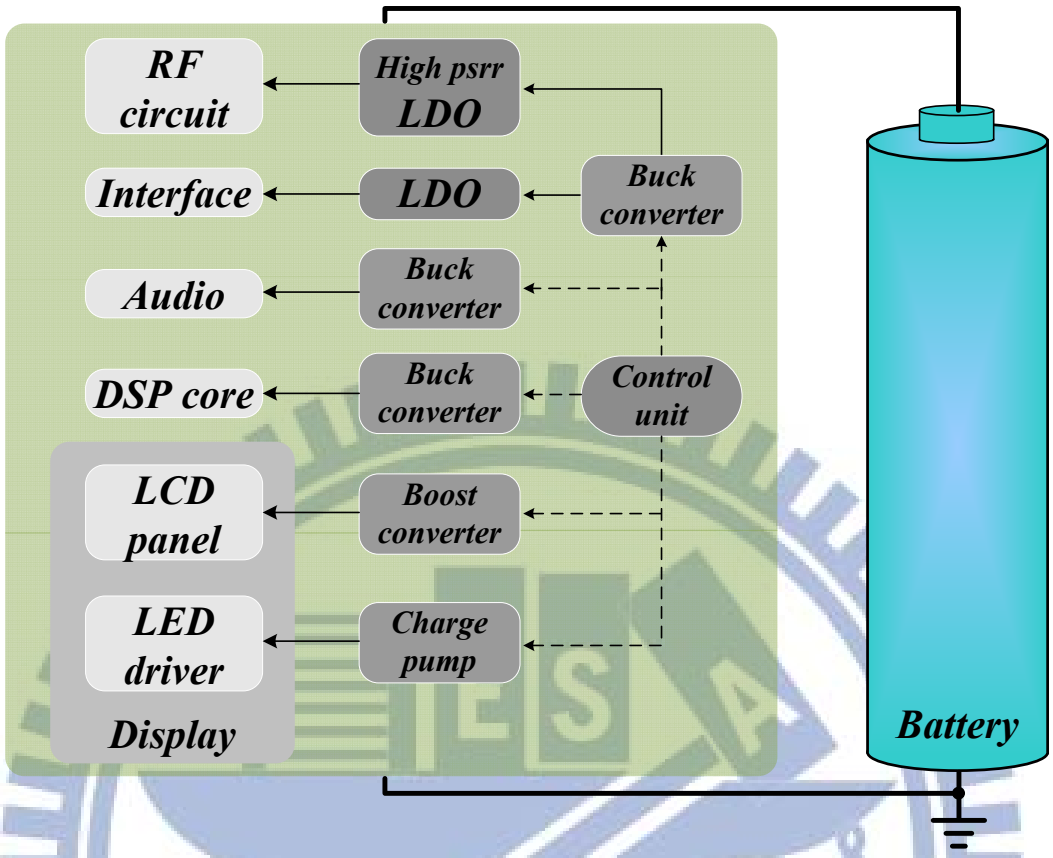


Fig. 1. Power management system diagram of cell phone.

1.2 Categorization of Power Supply Circuit

In this section, power management circuits which can classify into three different techniques are introduced including: switching regulators, switching capacitor circuits, and linear regulators. These function and structures are described at the following subsections. Finally, a brief comparison will be given about three types of voltage regulators.

1.2.1 Linear Regulators

The linear regulator generally used in small range voltage conversion and low load current condition. It is with ripple-less output voltage with respect to the other types of power

management IC's [1].

[2]-[4]. Also, the linear regulator is featured of requires smaller layout area, footprints and simple architecture and low drop-out voltage to provide high efficiency and high performance.

The basic structure of linear regulator is illustrated in Fig. 2. It is also named as low drop-out (LDO) voltage regulator because there is a drop out voltage across pass device which is between the regulated output voltage and the input supply voltage. The linear regulator consists of an error amplifier to control the gate voltage of the pass transistor and correct the difference between reference signal (V_{FB}) and output. These devices are constructed in a negative feedback configuration to maintain the output voltage irrespective of load current and input voltage variations. In this way, this kind of regulator that output ripple and noise can be minimized because the regulator does not need switching operation. The efficiency is proportional to the difference of output voltage and input voltage. In other words, the lower dropout voltage, the higher efficiency can be abstained. The supply load ability and dropout voltage depend on the pass device's size. As the result, the size cost and performance is critical trade-off issue for linear regulator.

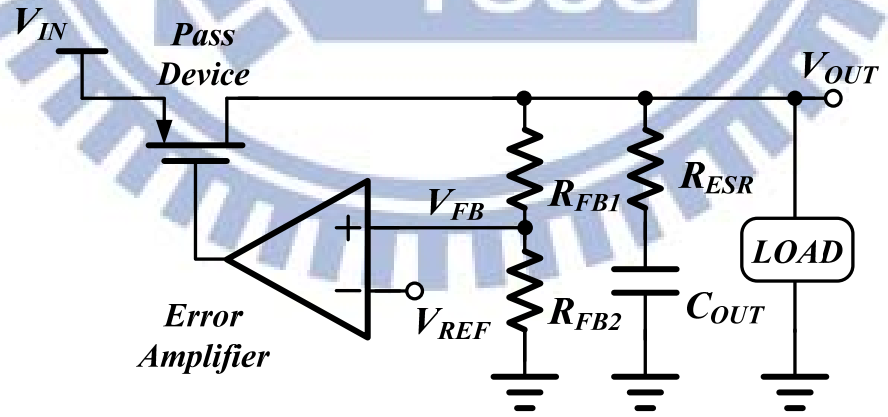


Fig. 2. The schematic of a low drop-out linear regulator.

1.2.2 Charge Pump

The switching capacitor circuits are usually used to obtain a dc voltage higher or inverting than the supply voltage in low load current applications [5]-[8] and it's often named as charge pump. The methodology of charge pump circuit is using MOSFET as capacitors and switches as energy storage devices.

Fig. 3 illustrated a switching capacitor voltage-doubler circuit. The structure consists of power stage with a fly capacitor (C_f) and four switches. The oscillator is receives and controlled the signal from Error amplifier *(EA)* and generates the oscillation frequency that corresponds to difference voltage between the feedback node after the divided resistors and reference voltage (V_{REF}).

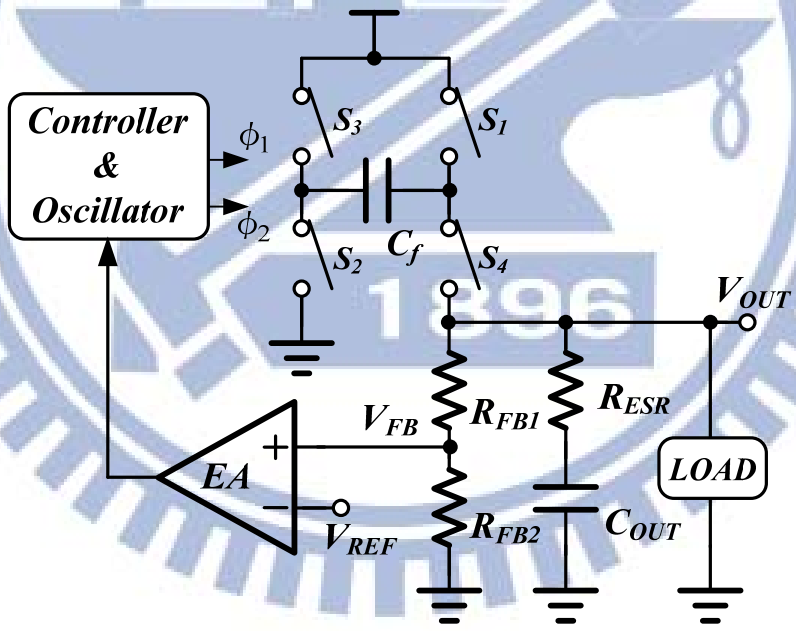


Fig. 3. The schematic of a close loop switching capacitor voltage doubler.

The control circuit is switched in complementary or differential phases such that the required multiple output voltage were maintained. As the result, during the first phase Φ_1 of switching period the switches S_1 and S_2 is turned on. In this period, the fly capacitor C_f is charged to V_{IN} while connecting to the fly capacitor C_f between the input voltage V_{IN} and ground. During the second interval of phase Φ_2, the switches S_3 and S_4 is turned on and the

switching S_1 and S_2 is turned off. The fly capacitor then is connected between V_{OUT} and V_{IN}. The output voltage equals twice of V_{IN} because of the voltage across fly capacitor is V_{IN}. In order to maintain the output voltage, there are many ways to modulate the voltage of switching capacitor circuits such as Makowski, Dickson, MPVD, TPVD charge pumps. However, due to digital rail-to-rail switching clock control, the charge pump suffers from output noise problems and EMI.

1.2.3 Switching Regulators

As shown in Fig. 4, the simple architecture of buck converter with low pass filter and two switches. The power stage consists of inductor and capacitor components for energy storage and conversion is like as low pass filter. Switching regulators are widely used in power supply systems because of its excellent advantages of high conversion ratio, high power efficiency and programmable [9]-[13]. But the noise and EMI problems become critical due to the switching operation.

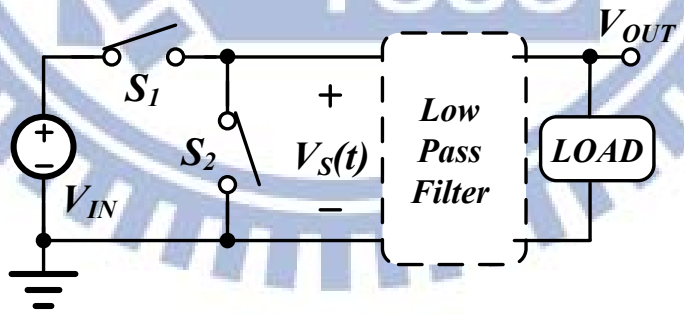


Fig. 4. The simple architecture of buck converter.

Fig. 5 shows the general form of the pulse signal. When the first phase of S_1 closed, the $V_S(t)$ equals to the source voltage V_{IN}. In the contrary, when the second phase of S_2 closed, the $V_S(t)$ equals the ground voltage – zero. Through the low pass filter that consisted with a capacitor and an inductor, the dc component of a periodic waveform is equal to its average

value via Fourier analysis. Hence, the dc value of $V_S(t)$ is

$$V_s = \frac{1}{T_s}\int_0^{T_s} V_s(t)dt = DV_{in} \tag{1}$$

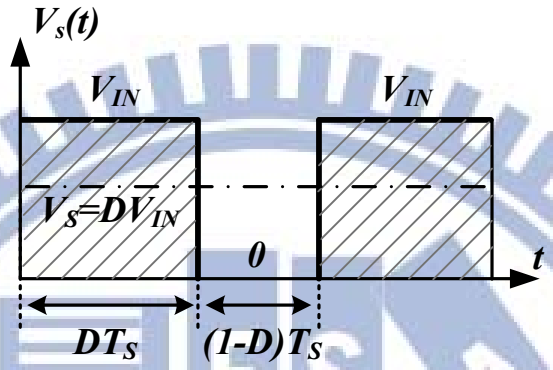
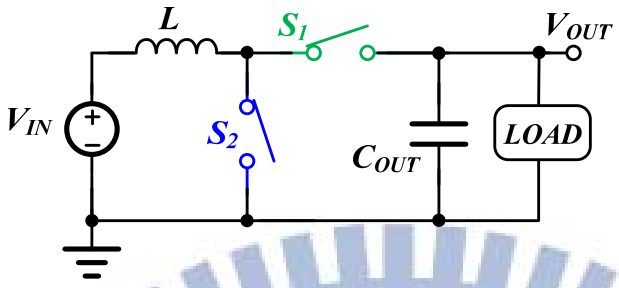
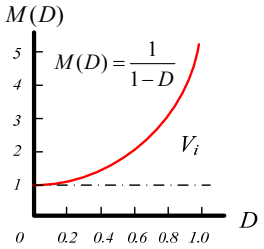
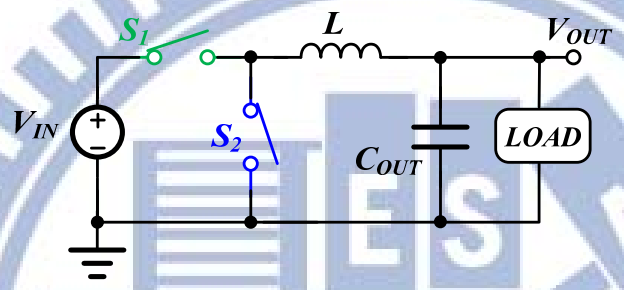
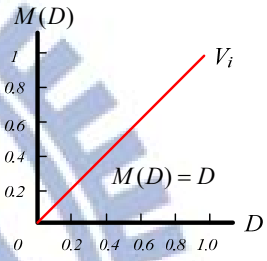
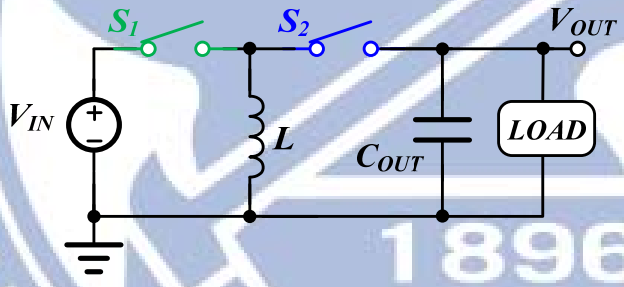
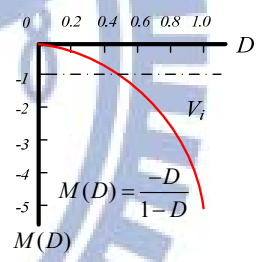


Fig. 5. The periodic waveform in Fourier analysis.

Therefore, the switching regulators can classify into three basic topologies as functional works. Listed in Table I, there are the architecture of boost, buck and fly-back converters.

Table I: Three architecture of switching regulators

	Architecture	Conversion Curve
Boost		
Buck		
Fly-Back		

The first regulator, boost converter, is featured of stepping up the input voltage with respect to output node. The conversion ration *M(D)* is expressed as *M(D)=1/(1-D)*. The second regulator named as buck converter is featured of stepping down the input voltage with respect to output node. The conversion ration *M(D)* is expressed as *M(D)=D*. The last regulator named as fly-back converter also called buck-boost converter is featured of stepping up or down the input voltage with respect to output node. The conversion ratio *M(D)* is written as *M(D)=-D/(1-D)*.

Linear regulators compared with switching regulator that has advantage of high efficiency because that it constructs by MOSFET as switches and inductor, capacitors as

energy storage components. When the switch transistor operated in triode region, it's seen as shot device with little voltage drop across it and it leads to little power dissipation as conduction loss.

On the other hands, there are disadvantages of witching regulator. The control circuit determined time sequence that the structure more complexity than the linear regulators. Also, requirement of discrete components such as capacitors and inductor costs more PCB area. Furthermore, the bandwidth limits the transition response time and the clock signal lead to output noise. These performances are all worse than the linear regulators.

Table II list the comparison table between linear regulators, switching regulators and charge pumps.

Table II: Comparisons of the different power supply circuits.

	Linear Regulators	***Switching Regulators***	***Charge Pumps***
Regulation Type	Buck only	Buck/Boost	Buck/Boost
Noise	Low	High	Medium
Power Capability	Medium	High	Medium
Footprint Area	Compact	Large	Moderate
Complexity	Low	High	Medium
Efficiency	Low	High	Medium
Cost	Low	High	Medium

1.3 Design Motivation

High-quality power supplying converters are demanded for portable devices such as digital cameras, cell phones and other multimedia equipment. That is, efficiency, recovery time, line/load regulation and are treated as important issues in providing a good power supply. Power converter regulates the output voltage as supply voltage and avoids unstable variation in case of load transient which may cause deteriorate or abnormal operation the performance of portable devices.

Switching converters using the output voltage ripple as the PWM ramp signal have been widely used to extend the battery life due to the simple control mechanism [14][15]. Besides, the response time of line and load transient is fast due to large control loop bandwidth. Its control method is usually called ripple-based control [16][17]. Ripple-based control methods include hysteretic control, constant on-time control, and constant off-time control. The hysteretic control is widely used for buck converter to achieve a fast transient response, and the circuitry of the hysteretic control method is compact without complexity. But the major disadvantage of the hysteretic control is the noise effect on the output voltage ripple. This noise can prematurely terminate or initiate a switching period. Another drawback is the switching frequency is affected by parasitic parameters and can change a lot with different input and output voltage.

The constant on-time control operates at a relatively constant frequency without a oscillator due to the on-time period is set by input supply voltage and output voltage, and it does not require error amplifier and loop compensation network, leads to a fast line and load transient response due to its wide control bandwidth. However, the stability is limited with equivalent series resistance (ESR) of output capacitor and output capacitor. If the constant on-time control would be applied in using a low equivalent series resistance of output

capacitor, we must find the ways to compensate the constant on-time control. Especially, with small equivalent series resistance, the output ripple become smaller and the element of equivalent series inductor (ESL) of output capacitor may lead to considerable effect on stability. Consequently, the solution to enhance noise the margin is an important issue to discuss.

1.4 Thesis Organization

The concepts of DC-DC buck converter is organized in chapter 2. The basic ripple-based control of witching converter is introduced in chapter 3. Proposed converter with increase noise margin technology is illustrated in chapter 4. Circuit implementation of the proposed technique is described in chapter 5. Finally, simulation results, conclusion and future work are made in chapter 6.

Chapter 2

Basic Definition Principles of DC-DC Buck Converters

2.1 General Specifications

There are many specifications and performances of DC-DC converter and required recognition. The following subsections are detail described including significant specifications such as line regulation, load regulation and transient response. Moreover, loss and power efficiency are illustrated.

2.1.1 Line Regulation

Line regulation is a steady-state performance of input voltage variation related to output accuracy. The equation (2) is expressed as below. It can be considered as immunity from input noise. A better line regulation value has more robustness against to supply variation.

$$\text{Line Regulation} = \frac{\Delta V_{OUT}}{\Delta V_{IN}} \quad (mV/mV) \tag{2}$$

2.1.2 Load Regulation

Load regulation is the steady-state performance that related to output voltage accuracy.

It's the result that estimates the ratio of output voltage variation at different load condition. The equation (3) is expressed as below. That is, when the converter has more immunity from output impedance variation but that has smaller load regulation value.

To get better regulation, the higher system loop gain is required. However, the stability is scarified which is tradeoff between output precision.

$$\text{Load Regulation} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} \quad (mV / mA) \tag{3}$$

2.1.3 Transient Response

The transient response is dynamic performance estimated. A good transient response implies that a small voltage variation and faster settling time on output node when output loading changes.

System bandwidth is a one of the factors related transient response. Wide bandwidth implies small voltage drop and faster transient response. It can separate into two fields about time domain and frequency domain analysis.

In frequency domain, literature about [18]-[20], used to position the pole and zero location when transient was occurred. When suffering a load step current variation, it moved the domain pole to higher frequency to get the higher unit gain bandwidth (UGB). In other words, the faster transient response had higher unit gain bandwidth. Therefore, the following describes the characteristics of transient response. It analyzed with output capacitor, equivalent series resistor of capacitor, transient time and so on.

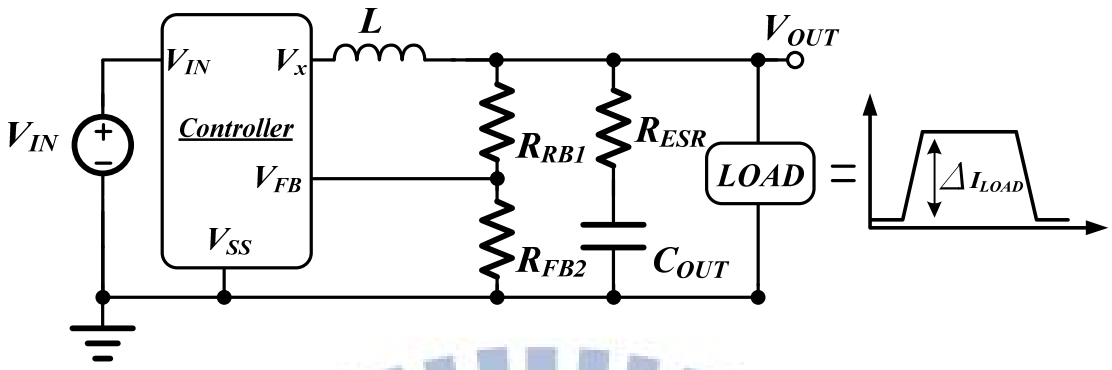


Fig. 6. System diagram of buck converter with dynamic load response.

In time domain analysis, the system diagram of buck regulator with dynamic load transient shows in Fig. 6. There are controller, inductor L, output capacitor (C_{OUT}) and equivalent series resistor (ESR) of capacitor R_{ESR}, feedback resistor divider (R_{FB1}, R_{FB2}). Fig. 7 depicts the transient waveform of output voltage with load current variation. When the load current from light to heavy and transient response happens, the transient period of t_1 is determined by the bandwidth restricted. System is too late to extent the duty cycle so that delivers insufficient inductor current to output noted. Therefore, the output capacitor does as current source to sustain the output current requirement. As a result, the voltage drops and its value V_{drop} can be formulated in (4).

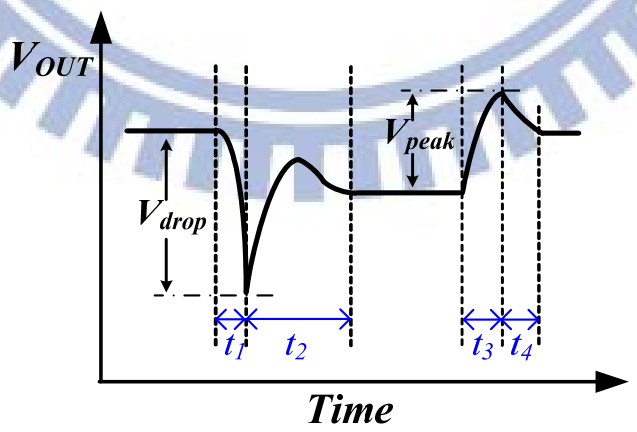


Fig. 7. Transient waveform of output voltage at load current variation.

$$V_{drop} = \frac{\Delta I_{OUT} \cdot t_1}{C_{OUT}} + V_{ESR} \quad , \quad V_{ESR} = \Delta I_{OUT} \cdot R_{ESR} \tag{4}$$

At this transient period t_1, the voltage drop V_{drop} equal to the summation of the variation of charges on capacitor and the V_{ESR}. The V_{ESR} is the equivalent series resistance of capacitor and product value of output current variation. The period of t_2 is dependent on the time requirement of the high side transistor to charge the output capacitor to regulated voltage. The summation of t_1 and t_2 is known as "Recovery Time". Contrarily, when the load transient is from heavy to light that will occurs the voltage peak V_{peak} of overshoot. When the transient response occurs, the t_3 *is* transient period with too much current which is supplied from high side transistor. The system is too late to reduce the duty cycle that decrease inductor current into output node and the system bandwidth also restricted the speed of feedback response. As a result, the output goes toward high and overshoot V_{peak} is formulated as below.

$$V_{peak} = \frac{\Delta I_{OUT} \cdot t_3}{C_{OUT}} + V_{ESR} \quad , \quad V_{ESR} = \Delta I_{OUT} \cdot R_{ESR} \tag{5}$$

At this transient period, the V_{peak} equals to the summation of variation of charges on capacitor and the V_{ESR}. During the period t_4, the redundant energy on output capacitor is consumed from light load and discharged through feedback resistor. As the result, the output voltage goes back to regulated level gradually.

2.2 Losses and Efficiency Analysis

Power loss of switching regulators is the combination of the switching loss and the MOSFET's conduction loss as shown in equation (6). The power loss is important factor to determine efficiency and it is briefly introduced as following.

$$P_{MOSFET} = P_{SW} + P_{COND} \tag{6}$$

2.2.1 Quiescent Loss

The quiescent loss also called as static loss that was consumed by other controllers of switching regulators. The smaller quiescent loss also causes higher efficiency.

$$P_Q = V_{IN} \cdot I_Q \tag{7}$$

The other power losses that don't be mentioned above obeyed the rules of I^2R.

2.2.2 Switching Loss

The switching interval begins when the high-side MOSFET driver turns on and begins to supply current power MOSFET's gate to charge its input capacitance. The switching loss is involved of the charge on the parasitic capacitor of switching node. Therefore, there is no switching loss until V_{GS} reaches the low-side MOSFET's V_{TH}.

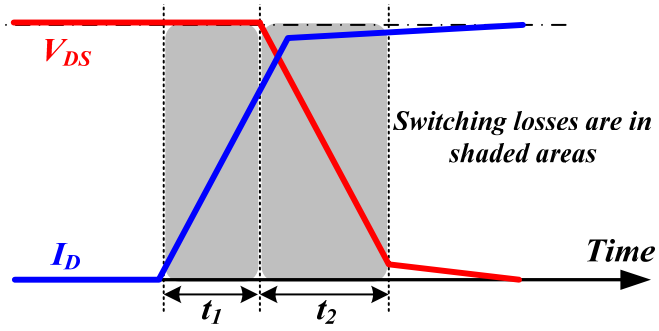


Fig. 8. Transient waveform of V_{DS} and I_D curve in switching losses on power MOSFET.

When V_{GS} reaches V_{TH}, the input capacitance of gate is being charged and the MOSFET's drain current I_D is rising up linearly until it reaches the current I_L which is presumed to be I_{LOAD}. During this period (t_1) the MOSFET is sustaining the entire input voltage V_{IN} across it, the energy in MOSFET during t_1 is:

$$P_{t_1} = t_1 \cdot (\frac{V_{IN} \cdot I_{LOAD}}{2}) \tag{8}$$

Sequentially, as the beginning time of second period t_2, the current flowing through high-side MOSFET is I_{LOAD}, and the V_{DS} begins to fall. All of the gate current will be going to recharge C_{GD}. C_{GD} is similar to the "Miller" capacitance of transistor, so t_2 could be thought of as "Miller time". During this time the current is constant as I_{LOAD} and the voltage is falling fairly linearly from V_{IN} to 0, therefore:

$$P_{t_2} = t_2 \cdot (\frac{V_{IN} \cdot I_{OUT}}{2}) \tag{9}$$

The total switching loss for any given edge is just the power that occurs in each switching interval, multiplied by the duty cycle of the switching interval:

$$P_{SW} = (\frac{V_{IN} \cdot I_{OUT}}{2}) \cdot (t_1 + t_2) \cdot F_S \tag{10}$$

2.2.3 Conduction Loss

The conduction loss is mainly related to high-side transistor loss and low-side transistor

loss. High-side conduction loss is calculated straightforward that is just the I^2R loss timing the MOSFET's duty cycle as below:

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot \frac{V_{OUT}}{V_{IN}} \tag{11}$$

Where $R_{DS(ON)}$ is at the maximum equivalent resistor on operation MOSFET.

In the same way, low-side conduction loss is determined as (12).

$$P_{COND} = I_{OUT}^2 \cdot R_{DS(ON)} \cdot (1 - \frac{V_{OUT}}{V_{IN}}) \tag{12}$$

2.2.4 Efficiency

The efficiency of switching regulator is defined as the ratio of the output power consumption and input power supplies, which is formed as below equation (13):

$$E_{ff} = \frac{P_{OUT}}{P_{IN}} = \frac{P_{OUT}}{P_O + P_{SW} + P_{COND} + P_Q + P_{Else}} \times 100\% \tag{13}$$

The total power consumption of input power supplies is involved of the output consumption (P_O), switching loss (P_{SW}), conduction loss (P_{COND}), quiescent loss (P_Q), and other losses (P_{Else}) in parasitic elements. A high efficiency results in a high performance extending the battery life.

Chapter 3

Output-Ripple-Based Control of Switching Converter

3.1 Introduction of Output-Ripple-Based Control

The output-ripple-based control commonly refers to the DC-DC converters that use the output ripple voltage as pulse width modulation (PWM) information. Fig. 9 shows a general DC-DC buck converter block diagram with the output-ripple-based control. The output state of feedback voltage V_{FB} compares with the reference V_{REF} signal to determine the operation of charging and discharging phases at power stage.

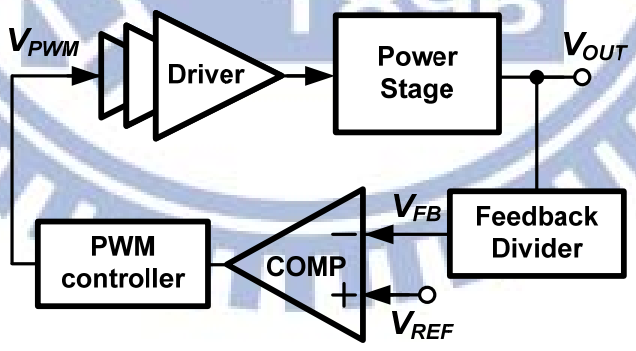


Fig. 9. Architecture of the COT control in the DC-DC buck converter.

The simple output-ripple-based control without complex compensation has the advantage of low cost. Especially, large bandwidth owing to the utilization of a comparator guarantees fast transient response. Furthermore, as operating at light load, the switch frequency is automatically adjusted by the implementation of a zero current detector (ZCD)

according to the output load without the need of additional complex frequency tuner. That is, the convertor acts as variable frequency modulation (VFM) and saves significantly switching loss to maintain good efficiency at light loads for portable power electronics. Consequently, the output-ripple-based control becomes one considerable choice among many power management designs.

The advantages of the constant on-time control can be summarized as follows.

(a) Self-oscillating without any oscillators.

(b) Simple structure without error amplifier.

(c) High efficiency at light load.

(d) Fast transient response.

However, the practical problems and limitations are suffered from as follows.

(a) Jitter behavior due to low noise immunity.

(b) EMI issue because of poorly defined switching frequency.

(c) Sub-harmonic instability due to inappropriate output capacitor application.

(d) Inadequate DC regulation due to the nonlinear loop control.

Three kinds of basic output-ripple-based control method of buck converter including hysteretic control, constant off-time control and constant on-time control are introduced in the following.

3.2 Hysteretic Mode Control

The architecture of the hysteretic mode control is shown in Fig. 10. This control methodology make the output oscillate within a predefined error band called hysteresis band or hysteresis window (V_H).

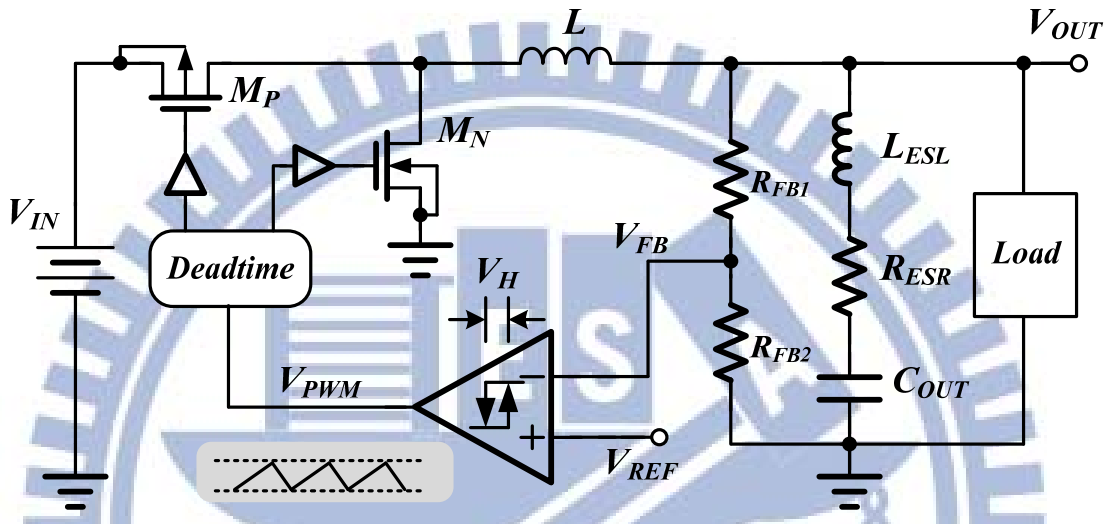


Fig. 10. The DC-DC buck converter with the hysteretic mode control.

The hysteresis window of the hysteretic comparator determines the on/off time of the DC-DC buck converter when the moment at the comparator output state changes as illustrated in Fig. 11. The high side power switch turns off when the V_{OUT} rises to the higher bound, $V_{REF}+V_H$ and turns the switch on to charge the inductor while the V_{OUT} falls below a lower bound. The switching frequency and output ripple therefore directly depends on the difference between the upper and lower reference threshold.

Equation (14)(15) express the operation frequency and also represents the major disadvantage of the hysteretic control which there is a very large variation in switching frequency depending on the variable Equivalent Series Resistance (ESR) of capacitor, output voltage, input voltage and output inductor. Consequently, it's difficult to define operation frequency in comparison with other control techniques.

$$f_{SW} = \frac{R_{ESR}}{V_{H(eff)}L}\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \tag{14}$$

$$V_{H(eff)} = V_H(1 + \frac{R_{FB2}}{R_{FB1}}) - \frac{L_{ESL}}{L}V_{IN} + T_{OFF}\frac{V_{IN} - V_{OUT}}{L}R_{ESR} + T_{ON}\frac{V_{OUT}}{L}R_{ESR} \tag{15}$$

But the hysteresis controllers are still favored in audio applications owing to their high linearity and simple design.

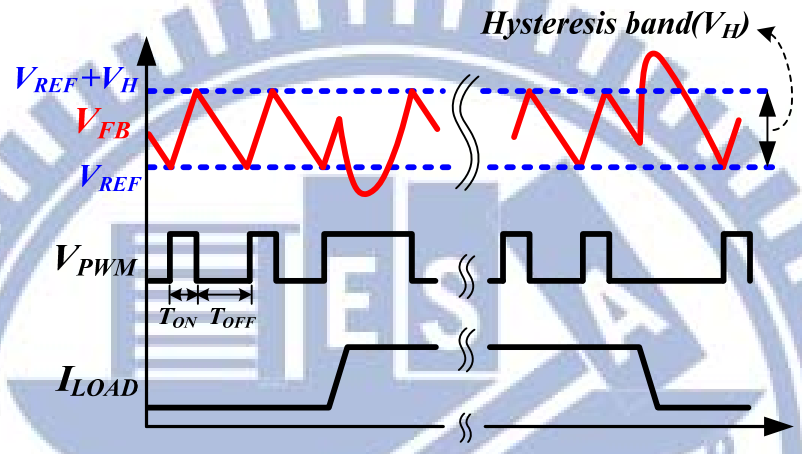


Fig. 11. The DC-DC buck converter with the hysteretic mode control waveform.

3.3 Constant Off-Time Control

The approach of constant off-time control is similar to constant on-time control as illustrating in Fig. 12. In normal operation, the system initiates an off-time period when the feedback voltage V_{FB} rises above the reference voltage V_{REF}. Also, this control technique is called “peak control”.

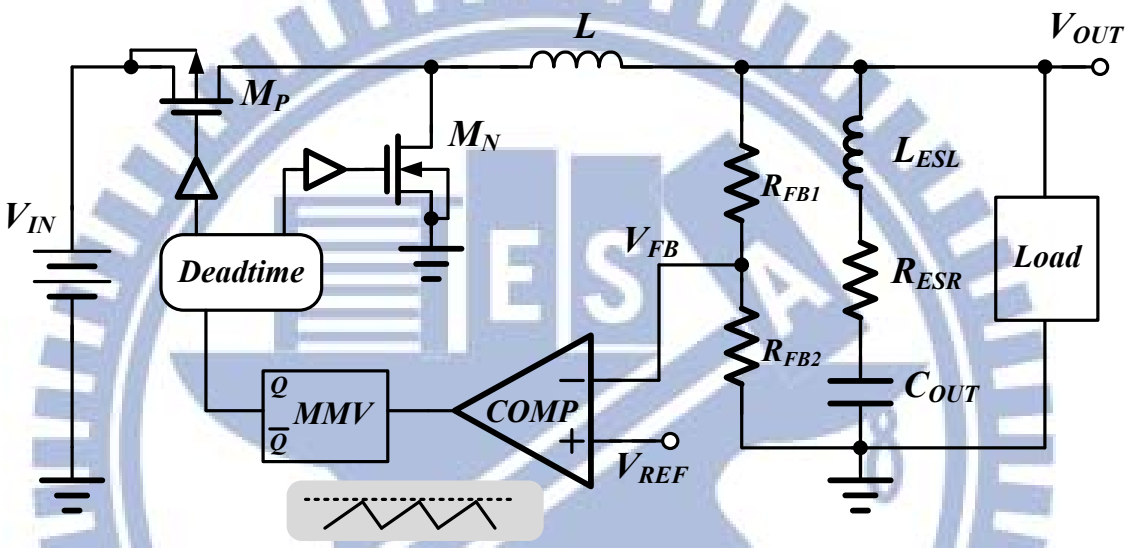


Fig. 12. The DC-DC buck converter with Constant off-time control scheme.

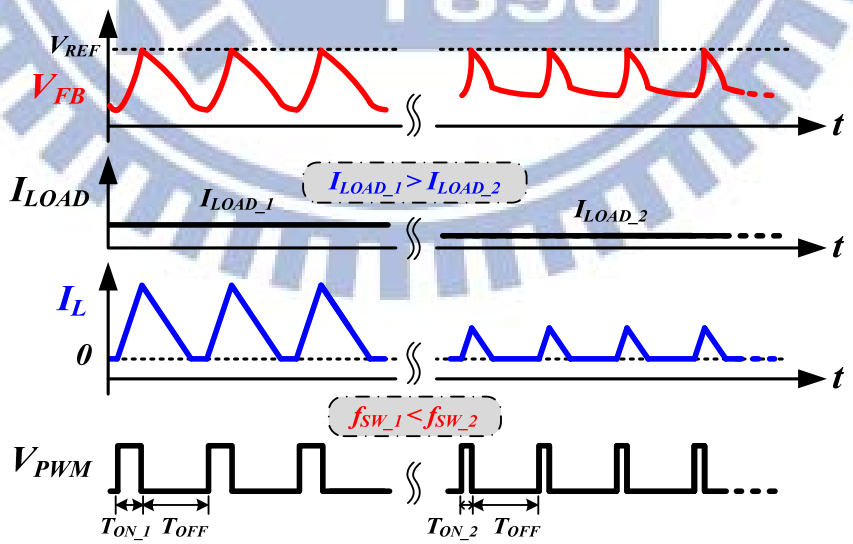


Fig. 13. The DC-DC buck converter with constant off-time control waveform in DCM.

However, constant on-time control is more popular than constant off-time control in application of power management system. The reason is that the switching frequency in DCM operation of constant off-time control is inversely proportional to the load current (i.e., the switching loss is considerable and deteriorates to poor efficiency.). Waveform shown in Fig. 13 is the constant off-time control operating in DCM.

3.4 Constant On-Time Control

As shown in Fig. 14, the basic constant on-time control structure consists of a comparator and mono-stable multi-vibrator (MMV), with the output voltage feedback compared with an internal reference. MMV is a circuit to generate a constant on-time and to adjust adaptively itself to variable using condition such as input supply voltage and output voltage. The constant on-time control method is a modification of hysteretic control that operates at a relative constant frequency without an oscillator.

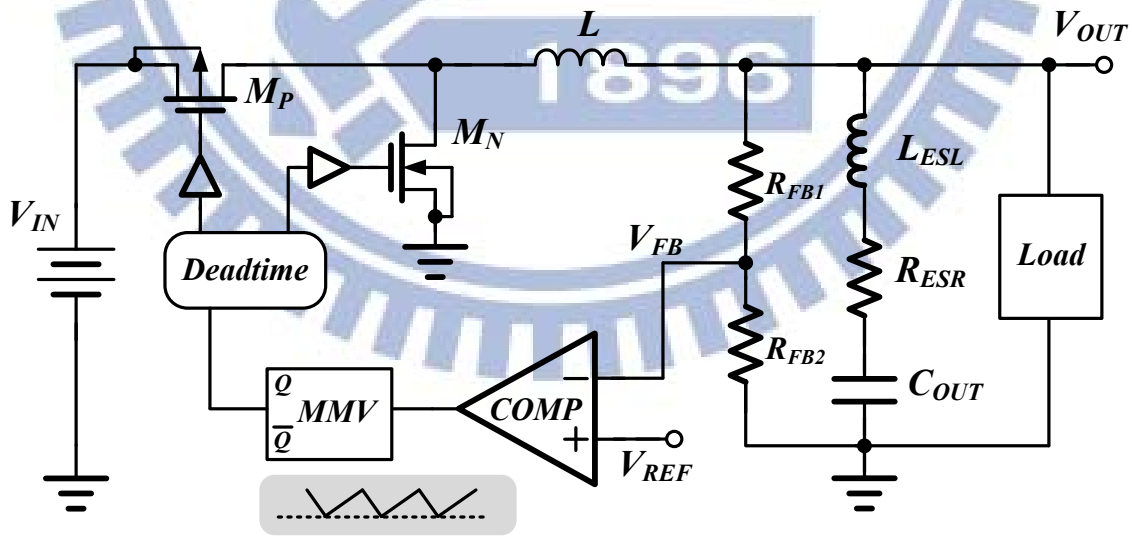


Fig. 14. The DC-DC buck converter with constant on-time control scheme.

When the feedback voltage V_{FB} falls below the reference voltage V_{REF} initiated on-time period. Thence, it is also commonly referred to as “valley control”. The high side power

switch stays on for the programmed on-time (T_{ON}), causing the feedback voltage to rise above the reference voltage. After the on-time period, the power switch remains off until the feedback voltage falls below the reference voltage and repeats the cycle again and again. The switching frequency as equation (16) of constant on-time in control continuous conduction mode (CCM) is easier to define than hysteretic mode control.

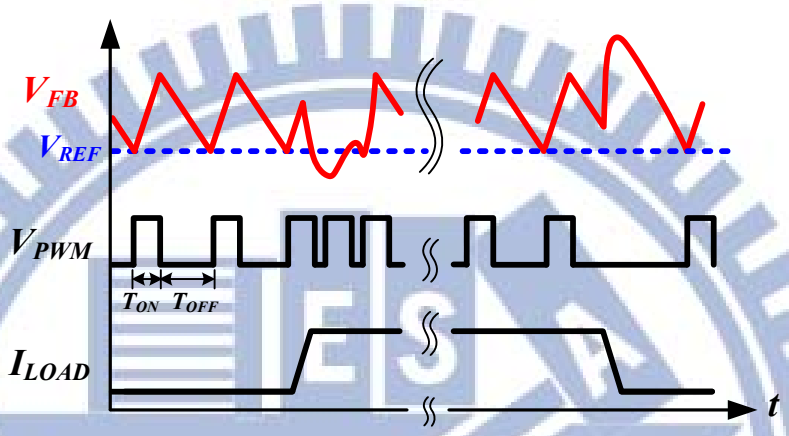


Fig. 15. The DC-DC buck converter with constant on-time control waveform in CCM.

Equation (16) shows the switching frequency is only related the output voltage, T_{ON} and input voltage. T_{ON} can be designed to compensate the variation and will discuss in Chapter 4.

$$f_{SW} = \frac{V_{OUT}}{V_{IN} T_{ON}} \tag{16}$$

In the contrary, while in discontinuous conduction mode (DCM) experienced at light loads, the frequency will vary according to the load condition, similar to the operation in PFM mode [25]. This leads to good transient response and high efficiency.

Fig. 16 shows the waveforms of constant on-time control in DCM operation, inductor current I_L raises to peak value during the fixed on-time period, and it falls back to zero before feedback voltage V_{FB} reaches valley voltage V_{REF}. When V_{FB} reaches V_{REF}, the next on-time period is introduced. Therefore, the lighter load, the longer time the energy delivers to output

from charging at one on-time period. In other words, switching frequency of constant on-time control is dependent on load current condition in DCM operation.

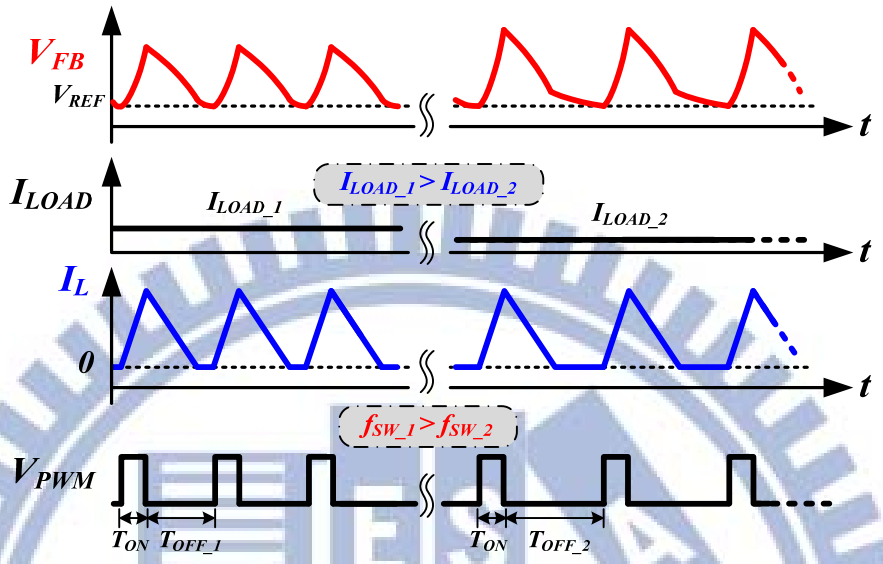


Fig. 16. The DC-DC buck converter with constant on-time control waveform in DCM.

Chapter 4

Constant On-Time Control with Increase Noise Margin Technology

4.1 Conventional Constant On-Time Control Buck Converter

The basic concept of constant on-time control is introduced in chapter 3. Besides, constant on-time control is more popular than constant off-time control owing to the conversion efficiency at light loads. In this section, we will describe the on-time control and analyze the system stability of constant on-time control in time-domain and frequency-domain, respectively.

As shown in Fig. 17, the output voltage ripple caused by the inductor current ripple contains three major terms, which are V_{ESL}, V_{ESR}, and V_{COUT} due to the parasitic effect on the output capacitor C_{OUT}. The V_{ESR} and the V_{ESL} are represented the voltage ripples cause by the equivalent series resistance (ESR) and the equivalent series inductance (ESL). The V_{COUT} is the voltage ripple of capacitor.

Under the same output capacitor value, different ESR value results in different output ripple. If the output ripple value is not large enough, it will decrease the system stability. In other words, there is a rule to determine the system stability by the product of the ESR and the C_{OUT}. The product needs to be large enough to guarantee the system stability. That is, it will limit the selection of the output capacitor. The inexpensive multi-layer ceramic capacitor

(MLCC) will be excluded due to its low ESR. However, the MLCC is one of the suitable choices owing to it low cost [22][23][24]. Thus, it becomes one important issue to overcome this problem. In this paper, increase noise margin technology is proposed to ensure the stability when the MLCC is utilized.

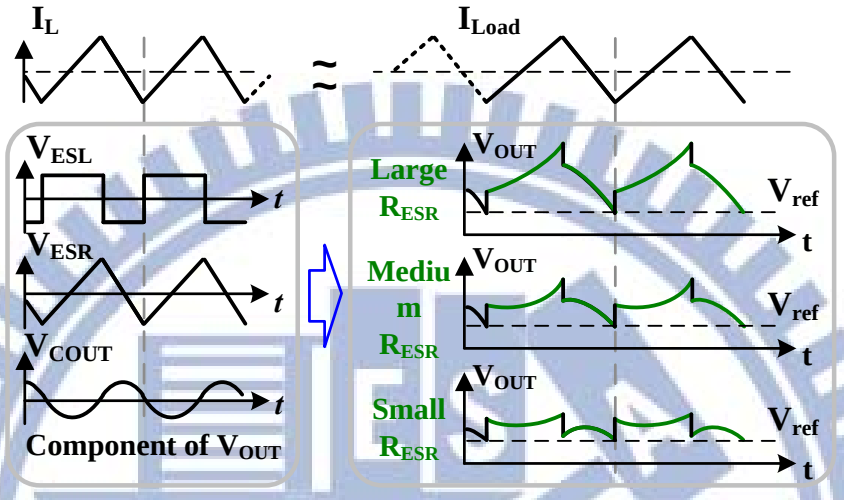


Fig. 17. The relationship between the output voltage ripple and the inductor current under different ESR value.

Another factor affecting the stability of the factors, equivalent series inductance (ESL).The ESL will distort the feedback control signal V_{FB} by the voltage step, V_{ESL}, as shown in (17) and (18). It results in the on-time timer might be trigger at the incorrect time. As depicted in Fig. 18, the V_{ESL} is proportional to the V_{IN} and the L_{ESL}. It will discuss in Chapter 4.1.2.

$$v_{ESL} = v_{ESL-p} + \left| v_{ESL-n} \right| = \frac{V_{in}}{L} \cdot L_{ESL} \tag{17}$$

$$\text{where } v_{ESL-p} = \frac{V_{in} - V_{out}}{L} \cdot L_{ESL} \text{ and } v_{ESL-n} = \frac{-V_{out}}{L} \cdot L_{ESL} \tag{18}$$

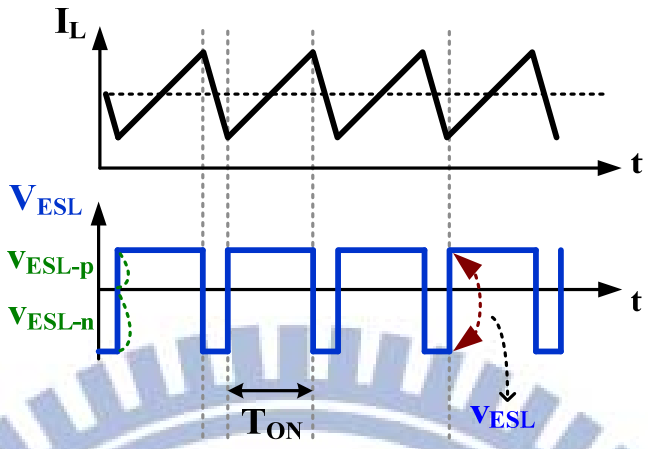


Fig. 18. The ESL effect at the output voltage.

4.1.1 On-Time Control

For maintaining the switching frequency constant, the adaptive on-time circuit adjusts the on-time period according to output voltage V_{OUT} and supply voltage V_{IN}, as shown in Fig. 19.

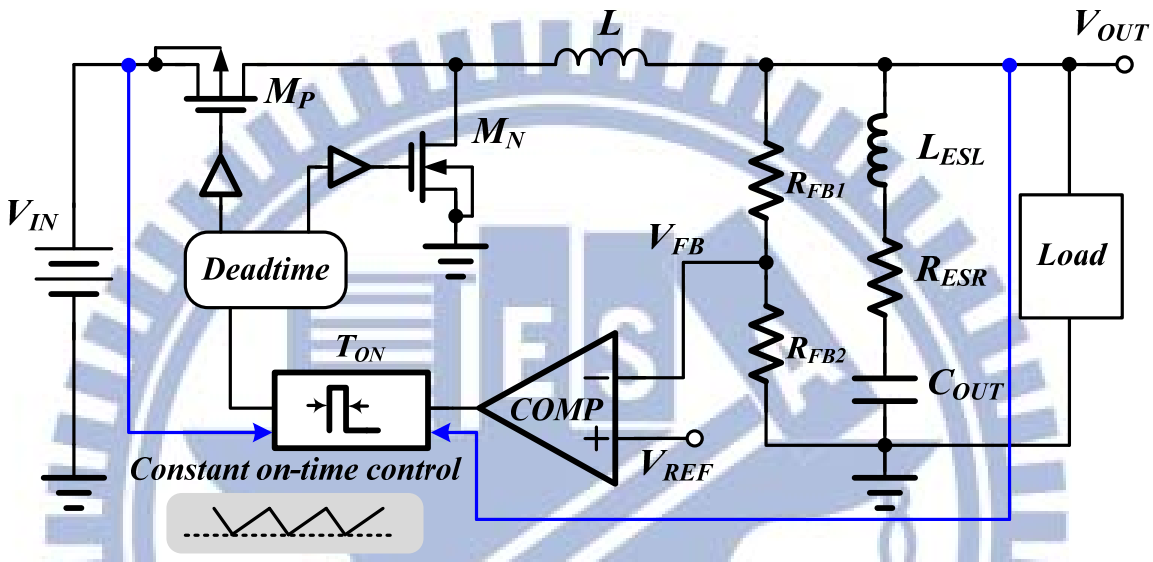


Fig. 19. On-time control DC-DC buck converter scheme.

As the above mentioning, the switching frequency is determined by (16). If the on-time (T_{ON}) is directly proportional to output voltage and inversely proportional to input voltage (19), then its switching frequency will be pseudo fixed frequency (20).

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \text{Constant} \tag{19}$$

$$f_{SW(NEW)} = \frac{V_{OUT}}{V_{IN} \cdot \left(\frac{V_{OUT}}{V_{IN}} \cdot \text{Constant} \right)} = \text{Constant} \tag{20}$$

4.1.2 Analysis Stability Criteria of Constant On-Time Control

In conventional constant on-time control with small ESR value on the output capacitor, the converter is easily affected by the noise due to small output ripple, which is dominated by the ripple on the output capacitor. Besides, the loop phase delay may further decrease the system stability owing to the double-pulse problem. As illustrated in Fig. 20, the delayed output voltage, V_{OUT}, is unable to reach the reference voltage, V_{ref}, even after the first constant on-time period. Consequently, the second constant on-time is inserted after the minimum off-time period to raise V_{OUT} higher than V_{ref}. The constant on-time control can't regulate the output voltage within one switching cycle and thus induces the double-pulse problem. That is, the system needs two or more switching periods to regulate the output voltage. The output voltage ripple is increased to ensure the system stability due to the decreased switching frequency.

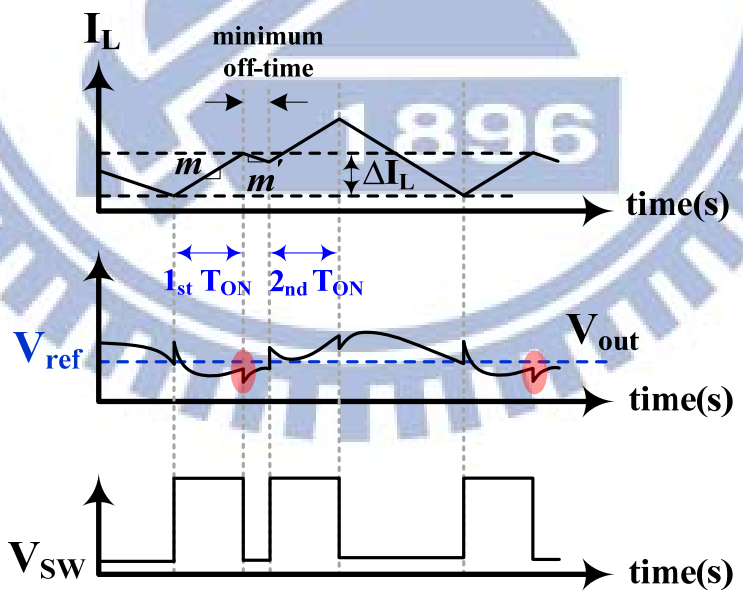


Fig. 20. Small ESR caused double-pulse problem.

In Fig. 20, the slope of the inductor current are *m* and *m'*, which are expressed in (21) and (22), during the on-time period and minimum off-time.

$$m = \frac{dI_L}{dt} = \frac{V_{IN} - V_{OUT}}{L} \tag{21}$$

$$m' = \frac{-V_{OUT}}{L} \tag{22}$$

The value of V_{OUT} for time=t can be calculated as shown in (23). R_{ESR} is the ESR on output capacitor. L_{ESL} is the ESL on the output capacitor. ΔI_L is the inductor current variation during one on-time period.

$$V_{OUT}(t) = V_{ref} + R_{ESR}mt + \frac{1}{C_O}\int(-\Delta I_L + mt)dt + L_{ESL}m' \tag{23}$$

The output ripple is composed of three components including ESR part, capacitor part and ESL part. In (23), the second term indicates the contribution of the ESR while the third term represents the ripple on the output capacitor. The last term indicates the contribution of the ESL. To ensure the system can be regulated for each switching cycle. At t=T_{ON}, the value of $V_{OUT}(T_{ON})$ needs to be larger than V_{ref} as shown in (24).

$$V_{OUT}(T_{ON}) - V_{ref} = R_{ESR}mT_{ON} - \frac{mT_{ON}^2}{C_O} + \frac{mT_{ON}^2}{2C_O} + L_{ESL}m' > 0 \tag{24}$$

The arrangement of (24) can be expressed in (25).

$$R_{ESR}C_O - \frac{L_{ESL}C_O}{T_{ON}} \cdot \left(\frac{V_{OUT}}{V_{IN} - V_{OUT}}\right) > \frac{T_{ON}}{2} \tag{25}$$

That is, the time constant, $R_{ESR}C_O$, must be larger than half of on-time period to ensure the system stability. Consequently, the ripple contributed by the ESR dominates the whole output ripple to guarantee the system stability. Therefore, a large ESR is utilized in the conventional constant on-time control at the sacrifice of large output ripple. However, for certain applications of output capacitor combination, as the total ESL of the output capacitor becomes larger, the double-pulse problem will appear as shown in Fig. 21. At the beginning of the minimum off-time, the voltage across ESL will step down since the negative slope of inductor current. If the voltage spike on the ESL is larger enough to let the output voltage smaller than V_{ref}, the second constant on-time period will appear. Large ESL will cause the system unstable due to large step voltage on ESL.

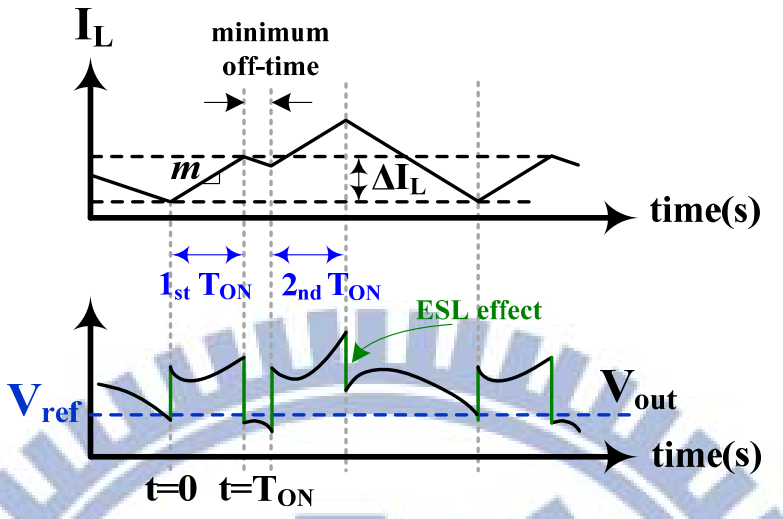


Fig. 21. Large ESL caused double-pulse problem.

4.2 Proposed Constant On-Time Control Buck Structure

The concept of the switched noise filter is to add a small offset to the capacitor voltage in each switching period. From the Fig. 22 to the Fig. 25, shows the proposed constant on-time control DC-DC converter with increase noise margin technology.

In the circuit of Fig. 22 (a constant on-time buck converter with valley control), the feedback voltage through the differentiator generates a differential signal. And during the on time the V_S is pulled up to $V_{ref}+V_{OS}$ with a switch. Fig. 23 shows the same circuit, but here the V_S is pulled up to $V_{ref}+V_{OS}$ during the minimum off time. Fig. 24 and Fig. 25 show a different method of establishing the offset in the same converter. The circuit in Fig. 24 generates the offset by charging the noise filter capacitor with a switched current source during the on time. The circuit in Fig. 25 generates the offset by charging the noise filter capacitor during the minimum off time. The above methods can be easily modified for use in constant on-time control buck converter.

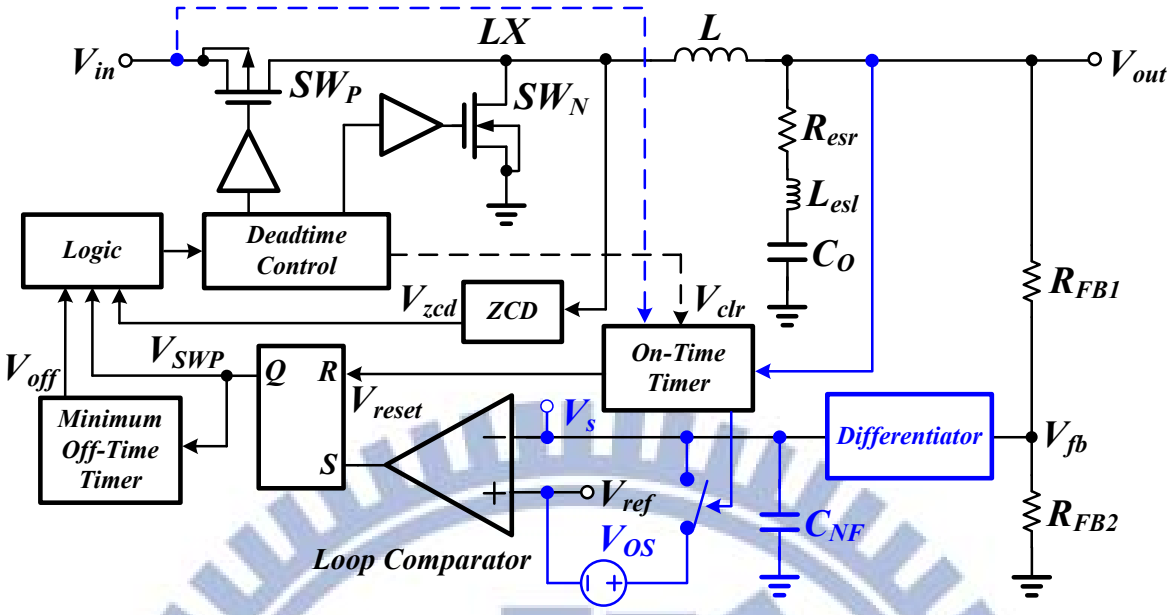


Fig. 22. Increase noise margin technology (a) offset voltage applied by switch during the on time.

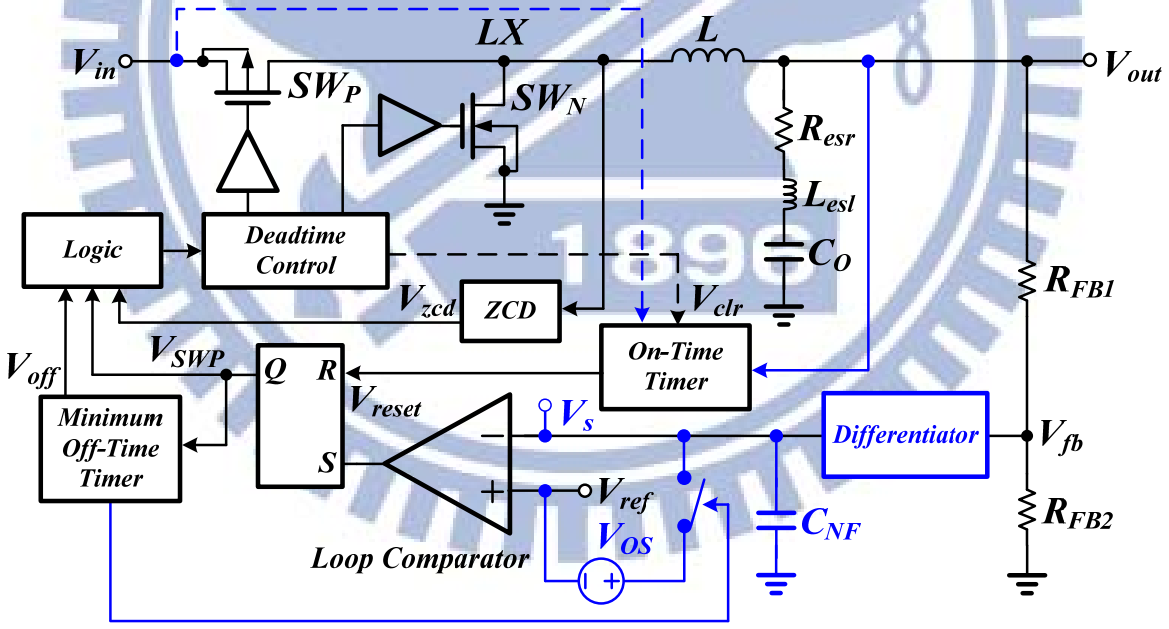


Fig. 23. Increase noise margin technology (b) offset voltage applied by switch during the minimum off time.

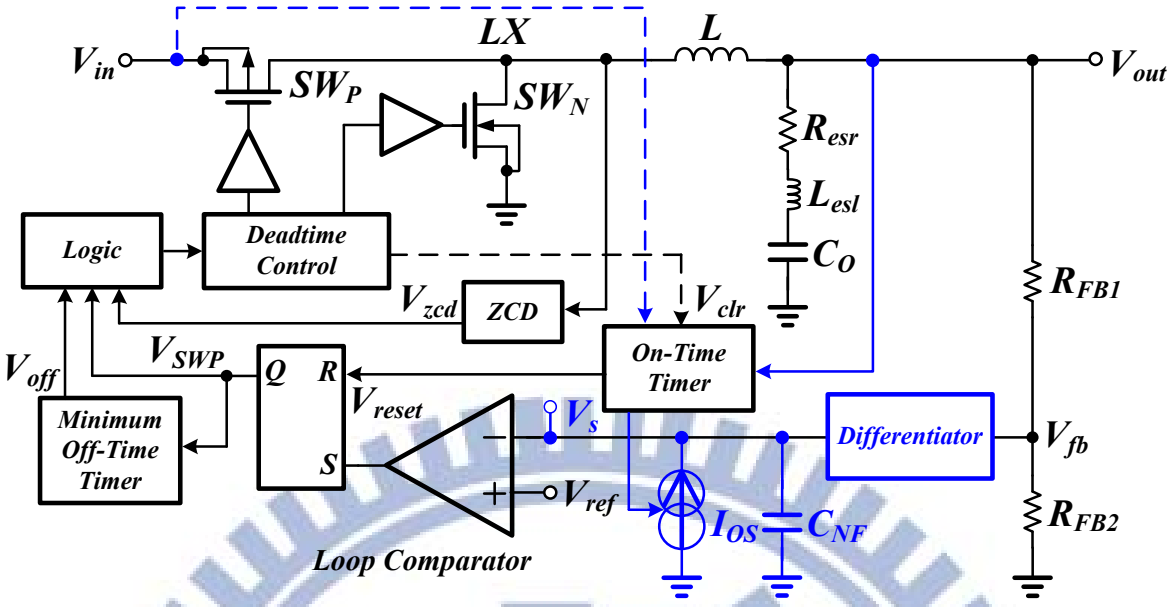


Fig. 24. Increase noise margin technology (c) offset voltage established by switched current source during the on time.

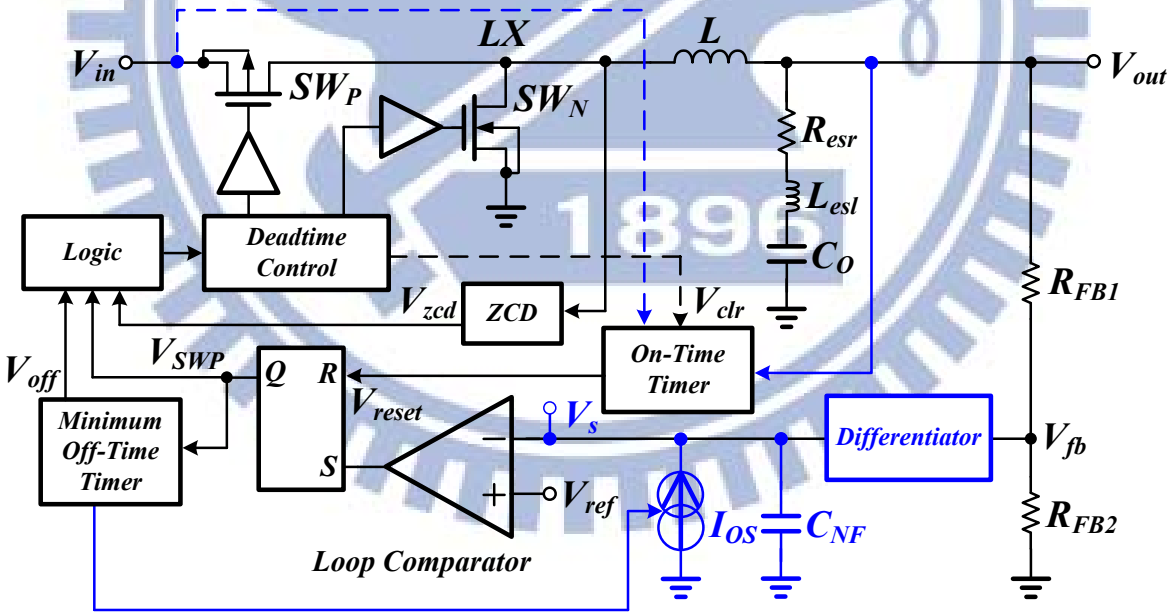


Fig. 25. Increase noise margin technology (d) offset voltage established by stitched current source during the minimum off time.

The proposed increase noise margin technology is the V_{fb} through the differentiator generates a differential signal and through the noise filter capacitor.

During the on time or minimum off time the noise filter capacitor is charged up to V_{ref} + V_{OS} with a switch. The signal (V_S) to get the inductor current information and it can be viewed as a ramp signal, providing good noise immunity for system operation. As the Fig. 26, it shows the effect of the switched noise filter and differentiator on the noise margin.

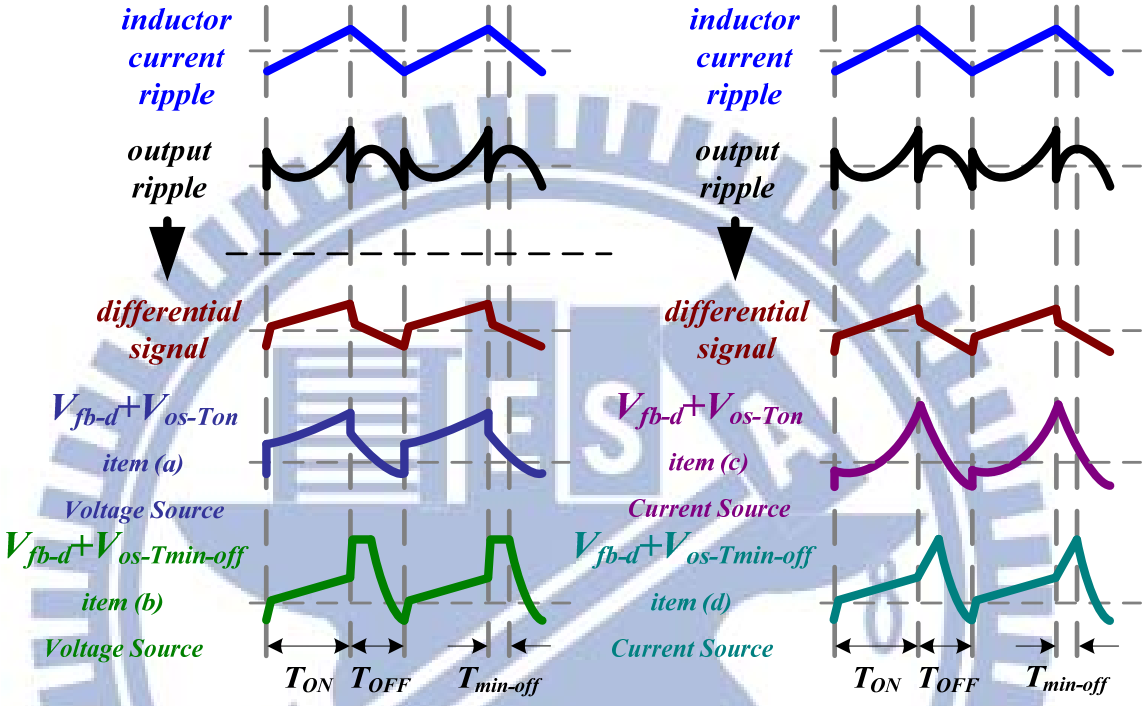


Fig. 26. Shows the effect of the switched noise filter and differentiator on the noise margin.

Chapter 5

Circuit Implementation

5.1 The Circuit of Increase Noise Margin Technology

The proposed structure is depicted in Fig. 27 and Fig. 28. The differentiator is composed of M_1-M_9, C_1-C_2, and OP1. Differentiating feedback voltage V_{fb} through the capacitor C_1, the inductor current can be derived. V_d is composed of ESR and inductor current ripple information. However, V_d has unwilling distortion due to equivalent series inductor effect of output capacitor. The expressions of V_{fb} and V_d are shown in (26) and (27), respectively.

$$V_{fb} = k\left[R_{ESR} I_L + \frac{1}{C_O}\int I_L dt + L_{ESL}\frac{dI_L}{dt} \right] \tag{26}$$

$$V_d = V_d' = \tau k\left[R_{ESR}\frac{V_{IN} - V_{OUT}}{L} + \frac{I_L}{C_O} + L_{ESL}\frac{d^2 I_L}{dt^2} \right] \tag{27}$$

The k is the feedback ratio and τ is a constant generated in the procedure of differentiation. The unwilling ESL effect caused by L_{ESL} is a high frequency component, which will result in a surge on the differential voltage V_d. To avoid this problem, a capacitor C_2 is introduced at the gates of transistors M_6 and M_7. Therefore, the current I_L flowing into M_7 is filtered by C_2. That is, the high frequency component of V_d has been eliminated. Then, the equivalent series inductor effect can be reduced. After that, the current I_H flowing into M_8 is mirrored to M_9, and I_H is the deduction of I_{HL} about I_L. That is, I_H contains high frequency component of V_d. The low frequency component current I_L can be obtained by deducting I_H

from I_{HL}. The voltage V_2 would therefore contain low frequency component only, eliminating the equivalent series inductor effect of output capacitor. And for power supply rejection that add the cascode circuit (M_a-M_d).

The current mirror circuit is composed of M_{13}-M_{15}, R_3, R_4 and OP3. The V_3 is proportional to enlarge the V_2 signal it's for common-mode feedback circuits (CMFB) input node. The CMFB circuit is composed of M_{16}-M_{18}, R_5 and OP4, the input nodes are V_3 and V_S. And the V_4 is feedback node that adjusts the V_S voltage for convergence differences between the corners. The V_S is not only proportional to enlarge by V_2 but also is controlled by CMFB feedback node, and compare with feedback voltage V_{fb}. The proportional to enlarge circuit is composed of M_{10}- M_{12}, R_1, R_2 and OP2. Besides, the offset voltage is provided by the voltage source is not generated by the current source. The current mirror circuit is composed of M_{19}-M_{21}, R_5 and OP5. It is proportional to narrow the V_{add} signal and add the voltage to V_S during the on time or minimum off-time that controlled by M_V.

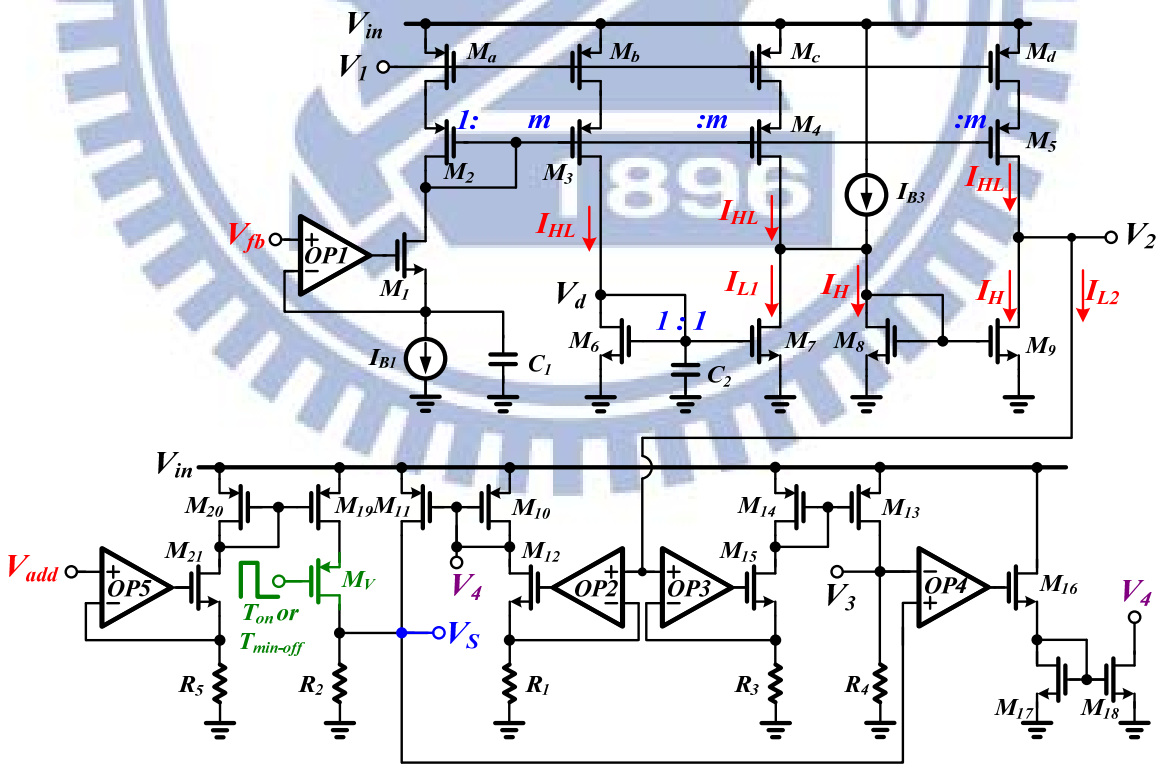


Fig. 27. Increase noise margin technology (a) and (b), the V_S is pulled up to V_{fb} + V_{OS} with a switch during the on time or minimum off-time.

Basically, most of the circuit structures of Fig. 28 the same with Fig. 27. But, the generate the offset voltage by charging the noise filter capacitor with a current source (I_{B2}), and the current source control by M_1 during the on time or minimum off-time.

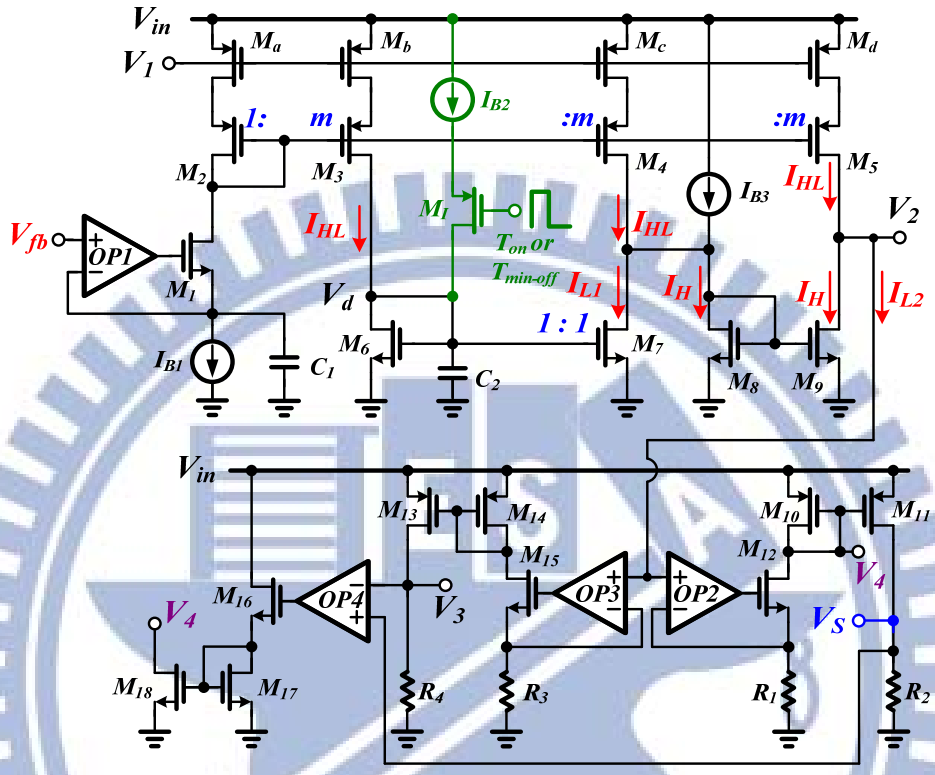


Fig. 28. Increase noise margin technology (c) and (d), generates the offset by charging the noise filter capacitor with a switched current source during the on time or minimum off-time.

Chapter 6

Simulation Results, Conclusions and Future Work

6.1 Simulation Results

The specifications of the proposed converter are listed in Table III.

Table III: Performance of the COT converter

Process	UMC 0.25μm
Supply voltage (V_{IN})	3.3V
Output voltage(V_{OUT})	1.8V
Load range (I_{LOAD})	0mA – 600mA
Inductor	4.7 μH
Output Capacitor	10 μF MLCC
R_{ESR}	5mΩ
L_{ESL}	2nH
Operation frequency (CCM)	1.5MHz
Output ripple @ I_{LOAD}=600mA	2mV

From the Fig. 29 to Fig. 32 shows the steady-state of simulation results at different load current condition when the converter operates in the DCM and CCM. Fig. 29 and Fig. 31 are show the increase noise margin technology (a) and (c), V_{offset} is 10mV, and the converter correctly operates in the DCM without the double-pulse problem when 2nH of ESL and 5mohm ESR exist at output capacitor. The output voltage ripple is about 2mV due to small ESR. Fig. 30 and Fig. 32 are show the same condition as above, but the converter correctly operates in the CCM. Here is no double-pulse problem. The output voltage ripple is about

2mV. Furthermore, the switching frequency reduces for power saving when the load current decrease in the DCM.

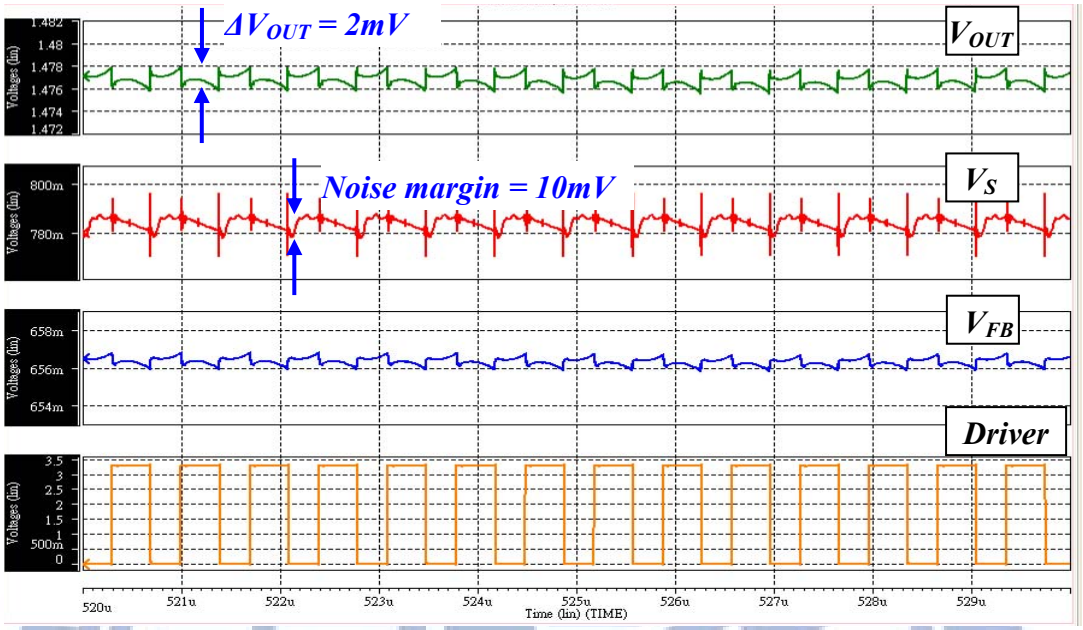


Fig. 29. Increase noise margin technology (a), V_{offset} : 10mV, no load

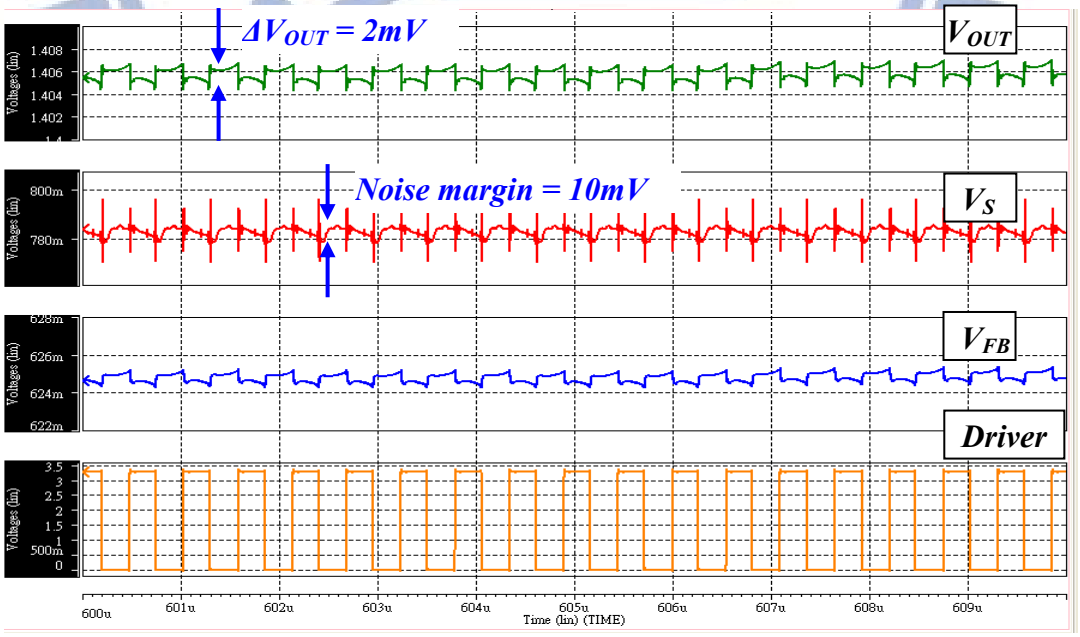


Fig. 30. Increase noise margin technology (a), V_{offset} : 10mV , I_{LOAD}=600mA

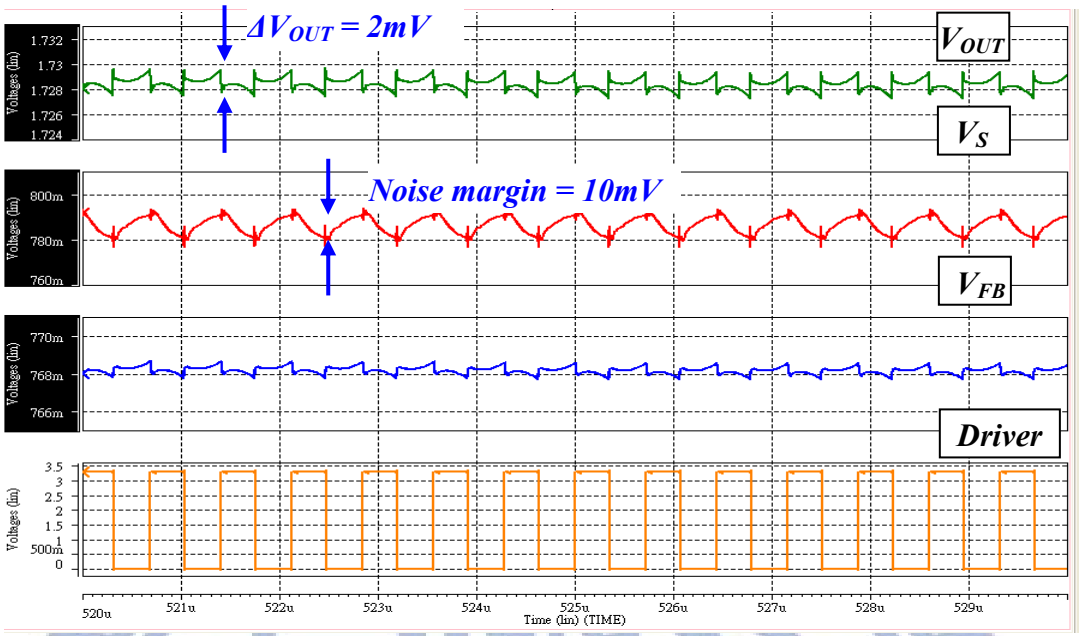


Fig. 31. Increase noise margin technology (c), V_{offset} : 10mV, no load

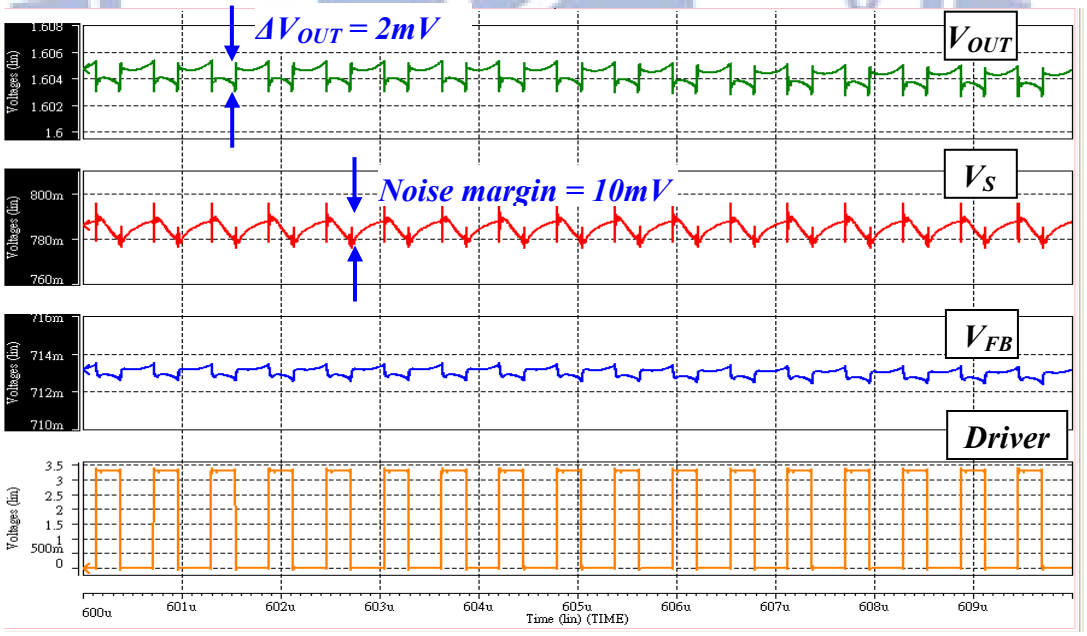


Fig. 32. Increase noise margin technology (c), V_{offset} : 10mV, I_{LOAD}=600mA

From the Fig. 33 to Fig. 36 shows the load transient response of simulation results when the converter operates from DCM to CCM. The increase noise margin technology provides good noise margin for constant on-time control system to operate correctly with low ESR exist at output capacitor. But in increase noise margin technology (b) and (d), if the offset voltage is not big enough system will become unstable.

The simulation result is as the table IV. The increase noise margin technology provides the stable output, but it's got larger load regulation. The circuit adds the increase noise margin technology or not, that is trade-off between stability and Load regulation.

Table IV: Simulation Result Table

	No Load	I_{LOAD} = 600mA
Simulation item (a)	$V_{OUT-RIPPLE}$ = 2mV output voltage stable V_{OUT} = 1.477V	$V_{OUT-RIPPLE}$ = 2mV output voltage stable V_{OUT} = 1.405V
Simulation item (b)	Unstable $T_{MIN-OFF}$ is too short noise margin too small V_{OUT} = 1.52V	Unstable $T_{MIN-OFF}$ is too short noise margin too small V_{OUT} = 1.46V
Simulation item (c)	$V_{OUT-RIPPLE}$ = 2mV output voltage stable V_{OUT} = 1.729V	$V_{OUT-RIPPLE}$ = 2mV output voltage stable V_{OUT} = 1.605V
Simulation item (d)	Unstable $T_{MIN-OFF}$ is too short noise margin too small V_{OUT} = 1.76V	Unstable $T_{MIN-OFF}$ is too short noise margin too small V_{OUT} = 1.73V

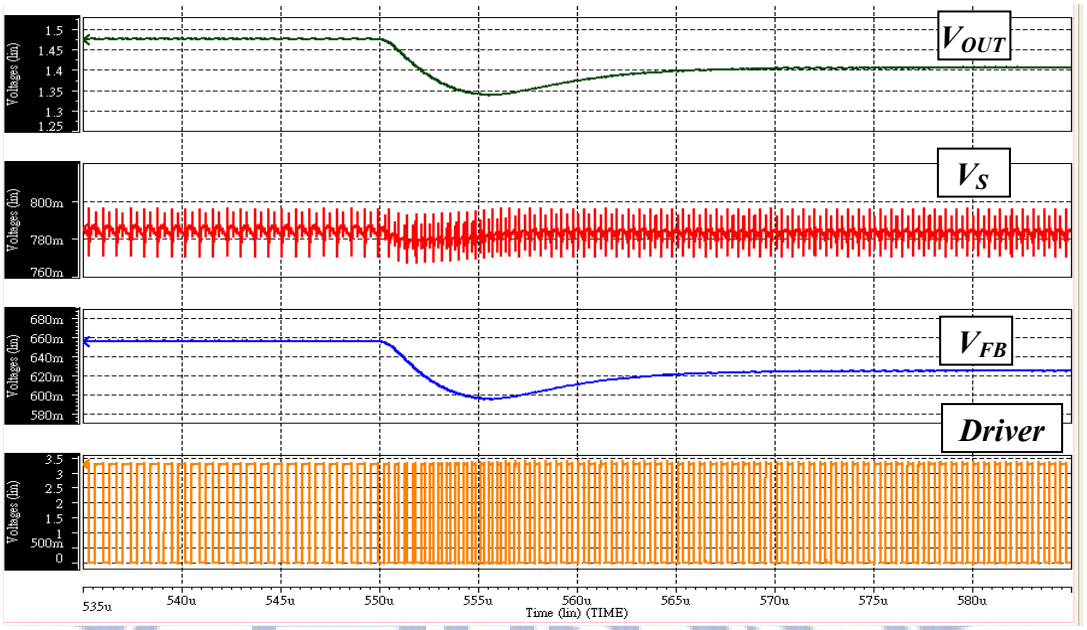


Fig. 33. Increase noise margin technology (a), V_{offset} : 10mV , I_{LOAD}=0 to 600mA

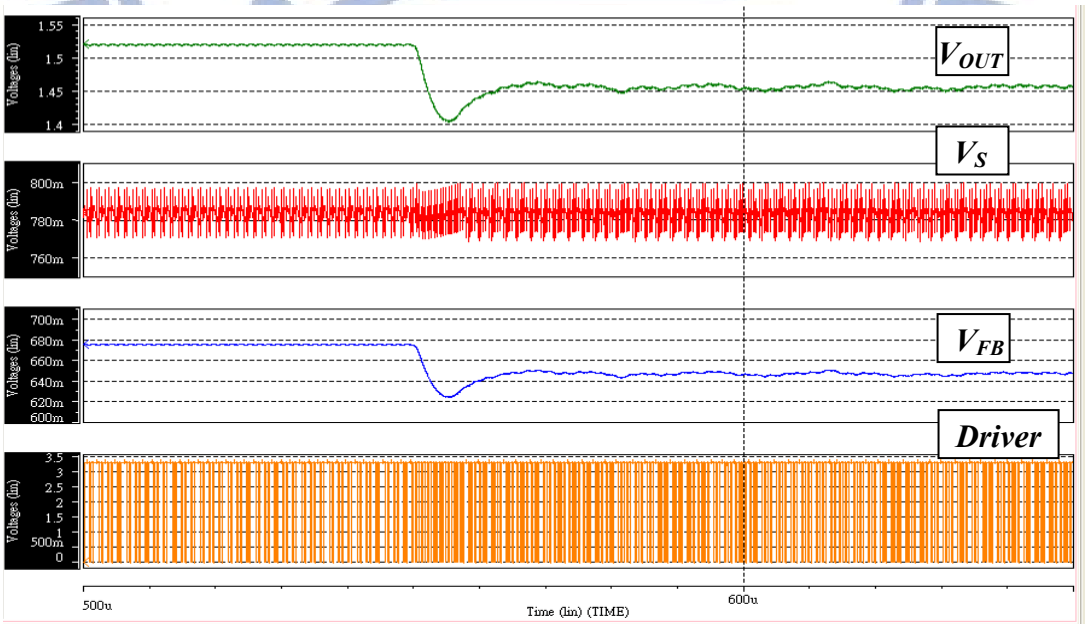


Fig. 34. Increase noise margin technology (b), V_{offset} : 10mV , I_{LOAD}=0 to 600mA

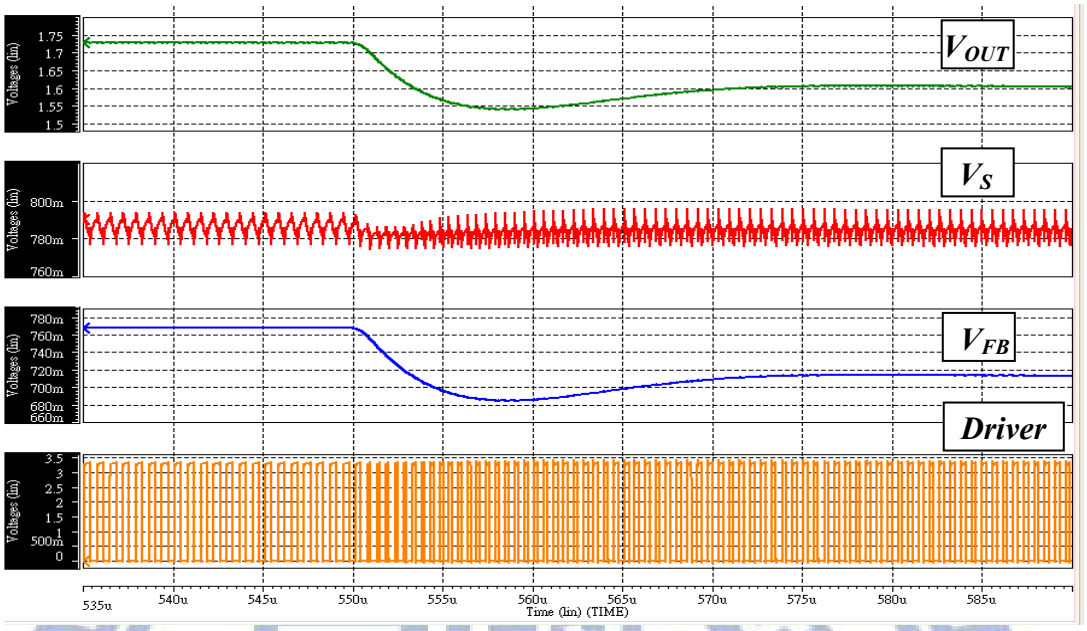


Fig. 35. Increase noise margin technology (c), V_{offset} : 10mV, I_{LOAD}=0 to 600mA

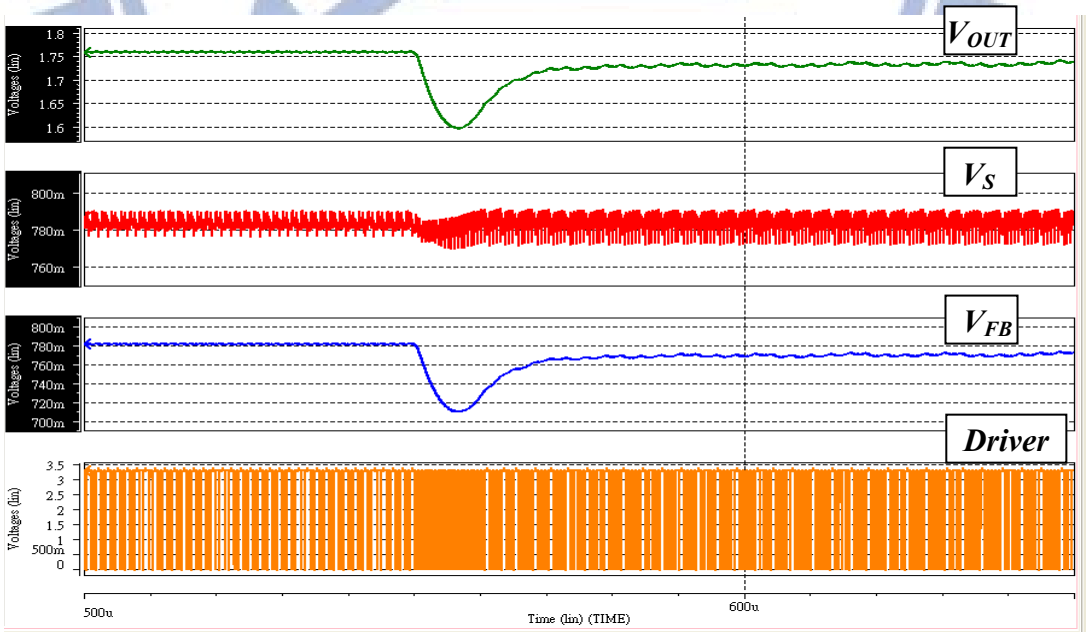


Fig. 36. Increase noise margin technology (d), V_{offset} : 10mV, I_{LOAD}=0 to 600mA

6.2 Conclusions

The noise margin technique is proposed in this thesis to eliminate equivalent series inductor (ESL) and equivalent series resistor (ESR) effect and and remove the dependency of output ripple induced by ESR in constant on-time control DC-DC converter of output capacitor. The noise margin technique is add the offset voltage during the on time or minimum off time is proposed structure for constant on-time control DC-DC buck converter. Because the noise margin at the comparator input node has been increased, so it can avoid the noise. The system can operate correctly even that very small ESR exists at output capacitor both in CCM and DCM.

6.3 Future Work

This thesis proposes a solution for constant on-time control DC-DC buck converter with using MLCC as output capacitor. The proposed increase noise margin technology not only removes the small ESR issue but also aims to eliminate ESL effect of the output capacitor. But, the output voltage DC level is not accurately defined. Because, that the magnitude of the offset voltage will affect the output voltage accuracy. There can add the cancel the offset voltage effect technique from V_{ref}. Finally, the experimental result should be presented to prove simulation result of whole system is matching.

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