An Analytic I–V Model for Lightly Doped Drain (LDD) MOSFET Devices

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Abstract—An analytic I-V model for lightly doped drain (LDD) MOSFET devices is presented. In this model, the n^- region is considered to be a modified buried-channel MOSFET device, and the channel region is considered to be an intrinsic enhancement-mode MOSFET device. Combining the models of these two regions, the drain current in the linear/saturation regions and the saturation voltage can be calculated directly from the terminal voltages. In addition, the parameters used in the channel region can be extracted by a series of least square fittings. According to comparisons between the experimental data measured from the test transistors and the theoretical calculations, the developed I-V model is shown to be valid for wide ranges of channel lengths.

NOMENCLATURE

$V_{gs}(V_{ds})$	External gate (drain) to source voltage.
V_{BG}	Substrate bias.
$V_d'(V_s')$	Intrinsic drain (source) voltage.
$V_d''(V_s'')$	n^--n^+ junction voltage in the drain (source) side.
$V_{g1}(=V_g-V_s')$	Intrinsic gate–source voltage.
$V_{d1}(=V_d'-V_s')$	Intrinsic drain–source voltage.
$V_{d2}(=V_d''-V_d')$	Voltage drop in the n^- region near the drain side.
$V_{g2}(=V_g-V_d')$	Voltage across the gate and the intrinsic drain.
$V_{d3}(=V_d''-V_s)$	Voltage across the n^+ source and the n^--n^+ junction.
$V_{d4}=V_d'-V_s$	Voltage across the n^+ source and the intrinsic drain.
I_{ds}	Drain current in the linear region.
$L(W)$	Effective channel length (width).
L_{mask}	Mask channel length.
$V_{FB}(V_{FBn})$	Flat-band voltage of the active channel (n^- region) device.
$\phi_{s,\text{inv}}$	Surface potential at strong inversion condition.
$t_{ox}(C_{ox})$	Oxide thickness (capacitance per unit area).
$\epsilon_{si}(\epsilon_{ox})$	Dielectric permittivity of the bulk semiconductor (oxide).
α,η	Empirical constants of the electron mobility in the inversion layer of the active channel device.
V_{sl}	Saturation velocity.
E_c	Critical electric field ($E_c=l/\beta=V_{sl}/\mu_n$).
$V_T(V_{T0})$	Threshold voltage for biased conditions (at zero drain voltage).
μ_n	Maximum electron mobility in the inversion layer of the active channel device.
$\mu_b(\mu_s)$	Effective electron mobility of the conducting charge in the bulk (surface) of the n^- region.
$Q_b(Q_s)$	Conducting charge density in the bulk (surface) of the n^- region.
μ_{eff}	Effective electron mobility in the channel region.
N_d	Doping concentration of the n^- region.
r_n	Junction depth of the n^- region.
l_1	Effective length of the spacer.
l_2	Effective overlapped length of the n^- region with respect to the gate.
$\bar{C}(C(x))$	Average (effective) capacitance per unit area of the surface charge layer in the n^- region.
$\Delta r_n(\Delta r_{ne})$	(Effective) depletion depth of the bulk in the n^- region with respect to the substrate.
N_a	Effective substrate concentration.
V_{bi}	Built-in voltage of the n^-–substrate junction.
W_d	Effective depletion depth of the substrate with respect to the n^- region.
$f_b(f_{b0})$	Geometrical factor of the bulk in the n^- region for biased conditions (at zero drain voltage).
ΔL_d	Depletion length at the channel depletion edge due to the n^- region in the drain side.
$V_{DSAT}(V_{dsat})$	Saturation source–drain voltage for the whole device (in the channel region).

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$\Delta L_1(\Delta L_2)$	Channel-length-modulation factor in the channel (n^-) region.
I_{DSAT}	Drain current in the saturation region.
I_{dsat}	Drain current at the onset of the saturation condition.
Y_d	Depletion width in the channel region.
R_{nd} (R_{ns})	Resistance of the n^- region near the drain–source side.
R_d (R_s)	Parasitic resistance of the drain–source.

I. Introduction

THE LIGHTLY DOPED drain (LDD) structure can reduce the high-field effects in scaled down devices by introducing n^- regions between the channel and the n^+ source–drain [1]. Since part of the high electric field can be absorbed into the n^- regions, the LDD MOSFET devices exhibit higher breakdown voltage, flatter threshold voltage versus channel-length relation, lower substrate and gate currents, and lower channel-length modulation effect [1], [2]. However, the n^- regions give large parasitic resistances that can cause the reduction of device transconductance and the increase of saturation voltage [2]. These large parasitic resistances are bias-controlled and share the appreciable voltage drop, especially when the channel length is short and the drain voltage is large.

In general, the behavior of the LDD structure can be characterized by the two-dimensional numerical method [3]. However, it consumes much longer computational time and is very difficult and impractical for circuit analysis use in a CAD system. Therefore, the analytic model is necessary to avoid the complicated computation. Recently, Duvvury *et al.* [4] have proposed an analytic I–V model in which the parasitic resistances of the n^- regions are considered to have constant values. However, this model is not valid for the I–V characteristics with different applied gate and substrate biases. More recently, Lai and Sun [5] have also proposed an analytic I–V model, in which the drain current cannot be calculated directly from the terminal voltages. This model is not suitable for circuit simulation. In addition, the parasitic resistance of the n^- region near the source is assumed to have a constant value.

In this paper, an analytic I–V model is proposed, in which the drain current can be calculated directly from the terminal voltages and the parasitic resistances of the n^- regions are bias/structure-dependent. In Section II, the mobility and I–V models in the channel region developed by Wu and Daih [6] are adopted. These models are well established and have good agreement with the experimental results. The parasitic resistance of the n^- region is derived based on a buried-channel MOSFET model with a modified charge-sharing scheme and an effective capacitance. Combining these two models, the analytic expressions in the linear region can be obtained. Moreover, the analytical forms for the terminal saturation voltage and the saturation current considering the effect of channel-length modulation are also derived from the above models. In Section III, we demonstrate that the parameters used in the active channel region can be obtained from a series of extraction techniques. In Section IV, comparisons between the experimental results and the theoretical calculations are made and satisfactory agreements are obtained. In Section V, conclusions are given.

II. The I–V Model

The schematic diagram and the equivalent circuit of a MOSFET device with an LDD structure are shown in Fig. 1(a) and (b), respectively. It is shown that an intrinsic enhancement-mode MOSFET is placed in the middle and both of the n^- regions are taken to be buried-channel MOSFET's. Note that R_s and R_d are the parasitic resistances including n^+ diffusion, contact, and wiring series resistances, which are considered to have constant values.

A. The I–V Characteristics in the Linear Region

The current equation for the intrinsic enhancement-mode MOSFET in the linear region can be written as [6], [10]

$$I_{ds} = \frac{\mu_n C_{ox} W\left[V_{g1} - V_T(V_{d1}) - \frac{1}{2}V_{d1}\right]V_{d1}}{L\left\{1 + \frac{\alpha C_{ox}}{2\epsilon_{si}}\left[V_{g1} + V_T(V_{d1}) - 2(V_{FB} + \phi_{s,\text{inv}}) - \frac{1}{2}V_{d1}\right] + \left(\eta + \frac{\beta}{L}\right)V_{d1}\right\}} \tag{1}$$

where $V_T(V_{d1})$ is the threshold voltage that is a function of V_{d1}; all other notations have been defined in [6].

In the linear region, the drain–source voltage is small. Therefore, we may linearize the threshold voltage with respect to V_{d1} and the drain current can be expressed in [10]

$$I_{ds} = \frac{\mu_n C_{ox} W(V_{g1} - V_{T0} - aV_{d1})V_{d1}}{L\left\{1 + \frac{\alpha C_{ox}}{2\epsilon_{si}}\left[V_{g1} + V_{T0} - 2(V_{FB} + \phi_{s,\text{inv}}) - bV_{d1}\right] + \left(\eta + \frac{\beta}{L}\right)V_{d1}\right\}} \tag{2}$$

where $a = \frac{1}{2} - k$; $b = \frac{1}{2} + k$, and k is the slope of the threshold voltage with respect to V_{d1} at zero drain bias. The parameters used above can be obtained from a series

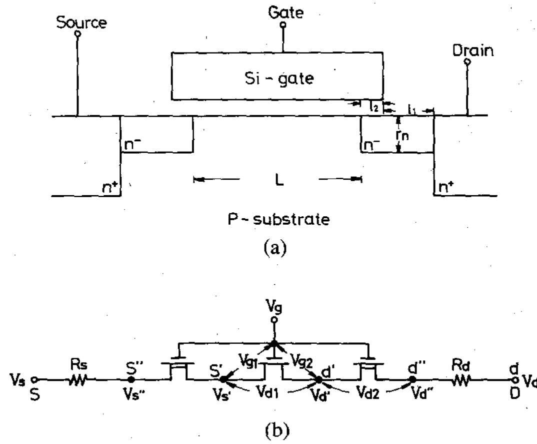

Fig. 1. (a) The schematic diagram of the LDD structure; (b) the equivalent circuit of the LDD MOSFET.

of extraction techniques as will be discussed in Section III.

Taking the n⁻ region to be a buried-channel MOSFET, the drain current can be expressed as

$$I_{ds} = W(\mu_b Q_b + \mu_s Q_s) \frac{dV(x)}{dx} \tag{3}$$

where Q_b and Q_s are the conducting charge densities in the bulk and the surface, respectively.

It's assumed that the drain voltage is small and the depleted charges in the bulk of the n⁻ region are caused by the substrate. Then, Q_b and Q_s in the drain side can be expressed as

$$Q_b = qN_d(r_n - \Delta r_n) \tag{4}$$

$$Q_s = C(x)[V_{g2} - V_{FBn} - V(x)] \tag{5}$$

where $C(x)$ is the effective capacitance per unit area of the surface charge layer and is a function of position (see Appendix A); Δr_n is the depletion depth of the bulk in the n⁻ region with respect to the substrate and is a function of the potential; N_d is the average doping concentration in the n⁻ region.

Taking N_a as the effective substrate concentration, Δr_n can be expressed by

$$\Delta r_n = \left\{\frac{2\epsilon_{si} N_a [V_{bi} + V_{BG} + V_{d4} + V_{(x)}]}{qN_d(N_a + N_d)}\right\}^{1/2} \tag{6}$$

where V_{bi} is the built-in voltage of the n⁻-substrate junction and V_{BG} is the substrate bias.

Integrating (3) across the two ends of the n⁻ region near the drain, the result is (see Appendix B)

$$I_{ds}(l_1 + l_2) = W[\mu_b qN_d(r_n - \Delta r_{ne})V_{d2} + \mu_s \overline{C}(V_{g2} - V_{FBn} - \tfrac{1}{2} V_{d2})V_{d2}] \tag{7}$$

where $\overline{C}$ is the average capacitance per unit area of the surface charge layer and depends on the structure of the n⁻ region; Δr_{ne} is the effective depletion depth of the bulk in the n⁻ region with respect to the substrate. Note that

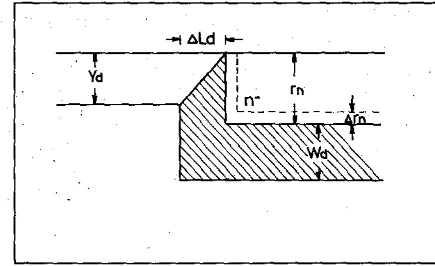

Fig. 2. The schematic structure for calculating the geometrical factor of the bulk in the n⁻ region.

the effective depletion depth of the substrate with respect to the n⁻ region (W_d) can be obtained by multiplying the factor N_d/N_a to Δr_{ne}. The result can be expressed as

$$W_d = \left[\frac{2\epsilon_{si} N_d (V_{bi} + V_{BG} + V_{ds})}{qN_a(N_d + N_a)}\right]^{1/2}. \tag{8}$$

As the drain voltage is large, the depleted charges exist not only in the n⁻/substrate junction but also in the n⁻/channel junction. From the concept of the charge-sharing scheme as shown in Fig. 2, the depleted charges in the bulk of the n⁻ region have the same amount of charges depleted in the substrate and channel regions (which are plotted as the shaded region). Based on this geometrical consideration, the conducting charge density in the bulk of the n⁻ region expressed in (7) should be modified as [7], [8]

$$qN_d(r_n - \Delta r_{ne}) \rightarrow qN_d r_n f_b \tag{9}$$

where f_b is the geometrical factor of the bulk in the n⁻ region and can be expressed as

$$f_b = 1 - \frac{N_a\left\{W_d(l_1 + l_2) + \frac{\Delta L_d}{2}[2(W_d + r_n) - Y_d]\right\}}{N_d r_n(l_1 + l_2)} \tag{10}$$

where

$$\Delta L_d = r_n\left[\left(1 + \frac{2W_d}{r_n}\right)^{1/2} - 1\right]. \tag{11}$$

Using the following relations:

$$V_{d2} = I_{ds}R_{nd} \tag{12}$$

and

$$V_{g2} - V_{FBn} - \tfrac{1}{2}V_{d2} = V_{gs} - V_{ds} - V_{FBn} + I_{ds}(R_d + \tfrac{1}{2}R_{nd}) \tag{13}$$

we can get a quadratic equation for R_{nd} that is

$$A_1 R_{nd}^2 + B_1 R_{nd} + C_1 = 0 \tag{14}$$

where

$$A_1 = \tfrac{1}{2} W \mu_s \overline{C} I_{ds} \tag{15}$$

$$B_1 = W[\mu_b q N_d r_n f_b + \mu_s \overline{C}(V_{gs} - V_{ds} - V_{FBn} + R_d I_{ds})] \quad (16)$$

$$C_1 = -(l_1 + l_2). \quad (17)$$

In general, $B_1^2 >> 4A_1C_1$, and R_{nd} can be approximated by

$$R_{nd} = \frac{l_1 + l_2}{W[\mu_b q N_d r_n f_b + \mu_s \overline{C}(V_{gs} - V_{ds} - V_{FBn} + R_d I_{ds})]}. \quad (18)$$

Note that the term $R_d I_{ds}$ cannot be neglected in the high-current condition and can be approximated as

$$R_d I_{ds} = \frac{\mu_n C_{ox} W}{L}(V_{gs} - V_{T0}) V_{ds} R_d. \quad (19)$$

As expressed in (10), f_b is a function of the bias conditions. By linearizing the geometrical factor at the zero drain bias as the same method used for the threshold voltage [6], the result is

$$f_b = f_{b0} - S V_{ds} \quad (20)$$

where

$$f_{b0} = f_b(V_{ds} = 0) \quad (21)$$

and

$$S = \left| \frac{df_b}{dV_{ds}} \right|_{V_{ds}=0}. \quad (22)$$

Putting (19) and (20) into (18), the resistance of the n$^-$ region in the drain side can be expressed as

$$R_{nd} = \frac{l_1 + l_2}{W[\mu_b q N_d r_n f_{b0} + \mu_s \overline{C}(V_{gs} - V_{FBn}) - G V_{ds}]} \quad (23)$$

where

$$G = \mu_b q N_d r_n S + \mu_s \overline{C}\left[1 - R_d \frac{\mu_n C_{ox} W}{L}(V_{gs} - V_{T0})\right]. \quad (24)$$

The resistance of the n$^-$ region near the source side can be derived by the same method. In the general case, $V_{gs} - V_{FBn}$ is much greater than $I_{ds} R_s$. Therefore, the $I_{ds} R_s$ term can be neglected, and the result can be expressed as

$$R_{ns} = \frac{l_1 + l_2}{W[\mu_b q N_d r_n f_{b0} + \mu_s \overline{C}(V_{gs} - V_{FBn})]}. \quad (25)$$

Using the following terminal relations:

$$V_{g1} = V_{gs} - I_{ds}(R_{ns} + R_s) = V_{gs} - I_{ds} R_{st} \quad (26)$$

and

$$V_{d1} = V_{ds} - I_{ds}(R_{ns} + R_s + R_{nd} + R_d) = V_{ds} - I_{ds} R_t \quad (27)$$

the I_{ds} can be calculated from the following equations:

$$A_2 I_{ds}^2 + B_2 I_{ds} + C_2 = 0 \quad (28)$$

and the solution is

$$I_{ds} = \frac{-B_2 + (B_2^2 - 4A_2C_2)^{1/2}}{2A_2} \quad (29)$$

where

$$A_2 = \frac{\alpha C_{ox}}{2\epsilon_{si}}(bR_t - R_{st}) - \left(\eta + \frac{\beta}{L}\right) R_t + \frac{R_t}{L}\mu_n C_{ox} W(aR_t - R_{st}) \quad (30)$$

$$B_2 = 1 + \frac{\alpha C_{ox}}{2\epsilon_{si}}[V_{gs} + V_{T0} - 2(V_{FB} + \phi_{s,\text{inv}}) - bV_{ds}] + \left(\eta + \frac{\beta}{L}\right) V_{ds} + \frac{R_t}{L}\mu_n W C_{ox}(V_{gs} - V_{T0}) - \frac{V_{ds}}{L}\mu_n C_{ox} W(2aR_t - R_{st}) \quad (31)$$

$$C_2 = -\frac{\mu_n C_{ox} W}{L}(V_{gs} - V_{T0} - aV_{ds}) V_{ds} \quad (32)$$

and $R_{st} = R_{ns} + R_s$ and $R_t = R_{ns} + R_s + R_{nd} + R_d$ since A_2, B_2, and C_2 are expressed in terms of the terminal voltages. Therefore, the I_{ds} can be obtained directly if the external bias conditions are given.

B. *The Saturation Voltage*

As the drain voltage is increased, the electric field in the channel region near the drain will reach the critical electric field E_c and will result in the saturation velocity V_{sl} for electrons. The saturation current at the saturation voltage can be expressed as

$$I_{d\text{sat}} = W\mu_{\text{eff}} C_{ox}[V_{g1} - V_{T0} - (1 - k)V_{d\text{sat}}]E_c \quad (33)$$

where $V_{d\text{sat}}$ and μ_{eff} are the saturation voltage and the effective mobility in the channel region. Using $V_{g1} = V_{gs} - I_{d\text{sat}}(R_s + R_{ns})$, the $I_{d\text{sat}}$ term that includes the effects of the parasitic resistance of the source can be expressed by

$$I_{d\text{sat}} = W\mu_{\text{eff}} C_{ox} \frac{[V_{gs} - V_{T0} - (1 - k)V_{d\text{sat}}]E_c}{1 + W\mu_{\text{eff}} C_{ox}(R_s + R_{ns})E_c}. \quad (34)$$

From (2), $I_{d\text{sat}}$ can also be expressed as

$$I_{d\text{sat}} = W\mu_{\text{eff}} C_{ox} \frac{(V_{gs} - V_{T0} - aV_{d\text{sat}})V_{d\text{sat}}}{L + W\mu_{\text{eff}} C_{ox}(R_s + R_{ns})V_{d\text{sat}}}. \quad (35)$$

Equating (34) and (35), the saturation voltage in the channel region can be solved by the following equation:

$$A_3 V_{d\text{sat}}^2 + B_3 V_{d\text{sat}} + C_3 = 0 \quad (36)$$

where

$$A_3 = (k - \tfrac{1}{2}) + \tfrac{1}{2} E_c W\mu_{\text{eff}} C_{ox}(R_{ns} + R_s) \quad (37)$$

$$B_3 = (1 - k)E_cL + (V_{gs} - V_{T0}) \quad (38)$$

$$C_3 = -(V_{gs} - V_{T0})E_cL. \quad (39)$$

The solution for (36) can be expressed by

$$V_{dsat} = \frac{-B_3 + (B_3^2 - 4A_3C_3)^{1/2}}{2A_3}. \quad (40)$$

Note that V_{dsat} is calculated from the terminal voltage. Putting (40) into (2), the saturation current (I_{dsat}) can be obtained.

The saturation voltage in the terminal end (V_{DSAT}) can be expressed as

$$V_{DSAT} = V_{dsat} + I_{dsat}(R_{ns} + R_s + R_{nd} + R_d). \quad (41)$$

Putting (23), (25), and (40) into (41), the V_{DSAT} can be solved by the following equation:

$$A_4V_{DSAT}^2 + B_4V_{DSAT} = C_4 = 0 \quad (42)$$

where

$$A_4 = -WG \quad (43)$$

$$B_4 = W\{\mu_b qN_d r_n f_{b0} + \mu_s \overline{C}(V_{gs} - V_{FBn}) + G[V_{dsat} + I_{dsat}(R_s + R_{ns} + R_d)]\} \quad (44)$$

$$C_4 = -W[\mu_b qN_d r_n f_{b0} + \mu_s \overline{C}(V_{gs} - V_{FBn})] \cdot [V_{dsat} + I_{dsat}(R_s + R_{ns} + R_d)] - I_{dsat}(l_1 + l_2). \quad (45)$$

Note that G in (43) and (44) has been given in (24).

The solution for (42) can be expressed by

$$V_{DSAT} = \frac{-B_4 + (B_4^2 - 4A_4C_4)^{1/2}}{2A_4}. \quad (46)$$

From (46), it is clearly seen that the saturation voltage (V_{DSAT}) is also expressed in an analytic form and can be calculated from the terminal voltages.

C. Channel-Length Modulation

In the saturation region, the pinchoff point will move toward the source side as the drain voltage is increased. Therefore, the effective conducting length of the inversion layer in the channel region becomes shorter. This phenomenon increases the slope of the saturation current, especially for the short-channel devices. Due to the n^- region, the space-charge region may extend into the n^- region near the drain, then, part of the voltage is shared by this region. Therefore, the channel-length-modulation effect should be less pronounced as compared to that of the conventional devices. The diagram showing the pinchoff point is shown in Fig. 3.

The current in the saturation region, considering the effect of channel-length modulation, can be expressed as

$$I_{DSAT} = \frac{I_{dsat}}{1 - \frac{\Delta L_1}{L}} \quad (47)$$

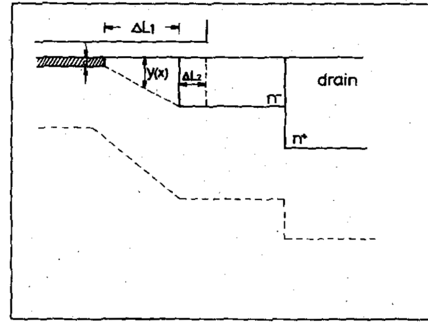

Fig. 3. The schematic diagram for showing the channel-length-modulation effect.

where I_{DSAT} is the saturation current in the saturation region; ΔL_1 can be calculated directly from the terminal voltage and is shown in Appendix C. Note that ΔL_1 is equal to zero at the onset of saturation condition.

III. Experiments and Parameter Extraction Techniques

A. Fabrication Data and Measurements

Experimental Si-gate n-channel MOSFET's with LDD structures were fabricated by using a set of test structures with the mask channel length varied from 2 to 12 μm and a mask channel width of 55 μm. The silicon substrates used were of ⟨1, 0, 0⟩ orientation and the resistivity range was about 15–25 Ω·cm. The device fabrications were carried out in a production line of the Electronics Research and Service Organization (ERSO), Industrial Technology Research Institute (ITRI), and the process sequence was quite standard. The double-channel-boron implantations were performed by using the shallow implantation with an energy of 25 keV and a dose of $7.5 \times 10^{11}/cm^2$ and the deep implantation with an energy of 150 keV and a dose of $4 \times 10^{11}/cm^2$, all through the gate oxide with a thickness of 250 Å. The over-etching technique for the polysilicon gate was taken to obtain the submicrometer-channel-length devices. The n^- regions of the LDD structure were formed by implanting the phosphorus ions with an energy of 30 keV and a dose of $1 \times 10^{13}/cm^2$. After depositing the CVD oxide on the polysilicon gate, the sidewall spacers were formed by using directional RIE. Then, the source–drain n^+ regions were implanted with an energy of 60 keV and a dose of $6 \times 10^{15}/cm^2$.

The gate oxide thickness (250 Å) of the fabricated LDD devices was measured by the controlled sample after the gate oxide growth using an ellipsometer and checked by the fabricated MOS capacitor using the C–V measurement. The junction depths of n^- and n^+ regions and the width of the spacer were measured by the auto-spreading resistance probe and SEM cross section analyses. The junction depth in the n^- region (r_n) is 0.25 μm and that in the n^+ region (R_j) is 0.35 μm. The spacer width (l_1) is about 0.45 μm and the lateral n^- diffusion depth (l_2) is about 0.2 μm. The threshold voltages and I–V characteristics of the fabricated LDD devices were measured by

TABLE I
THE EXTRACTED PARAMETERS FOR SIMULATING THE THRESHOLD VOLTAGES

T_{ox} (Å)	N_{AB} (cm^{-3})	N_{AS} (cm^{-3})	N_{AD} (cm^{-3})	Y_s (μm)	W_b (μm)	R_j (μm)	V_{FB} (V)
250	9×10^{14}	4.77×10^{16}	8.33×10^{15}	0.155	0.48	0.35	-0.745

using a microcomputer-controlled HP-4140B picoampere meter.

B. Parameter Extraction Techniques

1) Parameters in the Threshold Voltage: The threshold voltage (V_{T0}) of the fabricated LDD devices was determined by the extrapolation of the linear conductance with respect to different applied gate voltages with a low source–drain voltage (50 mV). Using the threshold voltage model developed by Wu *et al.* [8], the parameters in the threshold voltage model including V_{FB} and the channel doping profile with the step profile approximation for the double-channel-boron implantations can be easily extracted from the fabricated long-channel MOSFET by using the measured threshold voltages under different substrate biases, as described in [8]. The extracted parameters are listed in Table I. From Table I, the extracted $N_{AS} Y_s$ product is $7.394 \times 10^{11}/cm^2$, which is quite close to the implanted boron dose of $7.5 \times 10^{11}/cm^2$ for the shallow implantation through the 250-Å gate oxide. Similarly, the extracted $N_{AD} W_B$ product is $3.998 \times 10^{11}/cm^2$, which is in excellent agreement with the implanted boron dose of $4 \times 10^{11}/cm^2$ for the deep implantation. Based on the extracted parameters, $\phi_{s,\text{inv}}$ can be computed by the model in [8].

2) Other Parameters in the Channel Region: In order to extract the parameters in the channel region, the bias-controlled effects of the n^- region must be eliminated. Therefore, the parameters in the channel region must be extracted from the fabricated long-channel MOSFET devices with a lower gate voltage and a low source–drain voltage, for example, $0.5 \le V_{gs} - V_{T0} - \frac{1}{2}V_{ds} \le 7$ V and $V_{ds} = 0.05$ V. In this case, the resistance in the channel region is much larger than that in the n^- regions, and the parasitic resistances can be considered to have average values. At lower source–drain voltage ($V_{ds} = 0.05$ V), the source–drain current is about in the microampere range and the voltage drop across the n^- regions can be neglected, i.e., $V_{g1} \cong V_{gs}$, $V_{d1} \cong V_{ds}$. Under the above conditions, the total resistance can be obtained from (1) and is written as

$$R_T = R_{ns}^0 + R_s + R_{nd}^0 + R_d + \frac{L\alpha}{2W\mu_n\epsilon_{si}} + \frac{L}{W\mu_n C_{ox}} \cdot \left\{ \frac{1 + \frac{\alpha C_{ox}}{\epsilon_{si}}\left[V_{T0} - (V_{FB} + \phi_{s,\text{inv}})\right]}{V_{gs} - V_{T0} - \frac{1}{2}V_{ds}} \right\} \tag{48}$$

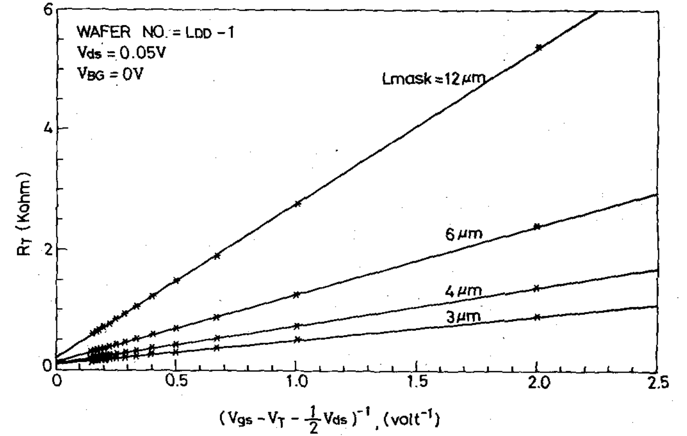

Fig. 4. The R_T versus $(V_{gs} - V_{T0} - 1/2\, V_{ds})^{-1}$ relation for different mask lengths.

where R_{ns}^0 and R_{nd}^0 are the resistances of the n^- regions at zero drain voltage, and V_{T0}, V_{FB}, and $\phi_{s,\text{inv}}$ have been determined from the threshold voltages.

Plotting R_T versus $(V_{gs} - V_{T0} - \frac{1}{2}V_{ds})^{-1}$ for different mask lengths with the same channel width ($W = 55$ μm), a set of the straight lines can be obtained by the least squares method as shown in Fig. 4. The slope (named SLOPE1) and the intercept in the vertical coordinate (named CUT1) can be expressed as

$$\text{SLOPE1} = \frac{L}{W\mu_n C_{ox}} \left\{ 1 + \frac{\alpha C_{ox}}{\alpha_{si}}\left[V_{T0} - (V_{FB} + \phi_{s,\text{inv}})\right] \right\} \tag{49}$$

$$\text{CUT1} = R_{ns}^0 + R_s + R_{nd}^0 + R_d + \frac{L\alpha}{2W\mu_n\epsilon_{si}} \tag{50}$$

where $L = L_{\text{mask}} - \Delta L$ is the effective channel length; L_{mask} is the mask length.

Using the same method for the CUT1 versus L_{mask} relation as shown in Fig. 5, the slope (named SLOPE2) and the intercept in the vertical coordinate (named CUT2) can be written as

$$\text{SLOPE2} = \frac{\alpha}{2W\mu_n\epsilon_{si}} \tag{51}$$

$$\text{CUT2} = R_{ns}^0 + R_s + R_{nd}^0 + R_d - \frac{\alpha\Delta L}{2W\mu_n\epsilon_{si}}. \tag{52}$$

Taking

$$a = \frac{1}{W\mu_n C_{ox}} - \frac{\alpha}{W\mu_n\epsilon_{si}}(V_{FB} + \phi_{s,\text{inv}}) \tag{53}$$

TABLE II
THE EXTRACTED AND AFTER-ADJUSTED PARAMETERS USED IN THE CHANNEL REGION

	μ_n (cm^{-2}/v-s)	α (cm/v)	ΔL (μm)	η (1/v)	β (cm/v)	R_s, R_d (Ω)	μ_{eff} (cm^2/v-s)
From Parameter Extraction	593.05	8.00×10^{-7}	1.32	2.05×10^{-2}	4.51×10^{-5}	13	550
After Adjustments	570.00	8.00×10^{-7}	1.32	2.05×10^{-2}	4.90×10^{-5}	13	550

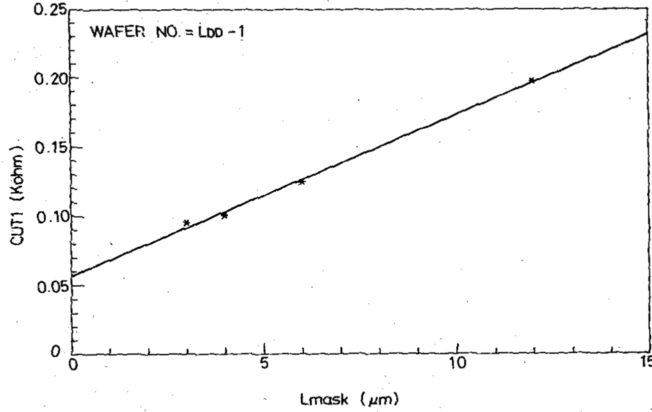

Fig. 5. The CUT1 versus L_{mask} relation to obtain CUT2 and SLOPE2.

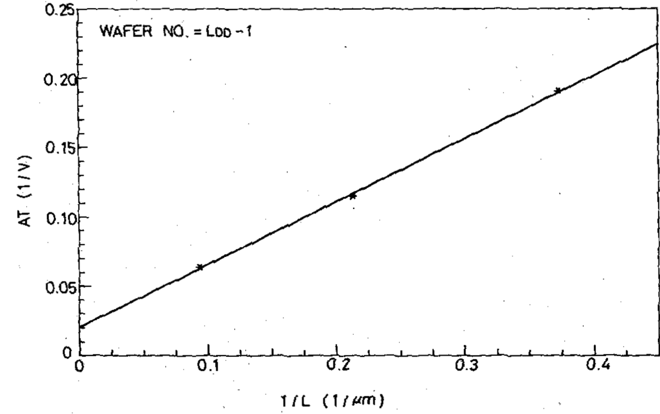

Fig. 7. The AT versus L^{-1} relation to obtain η and β.

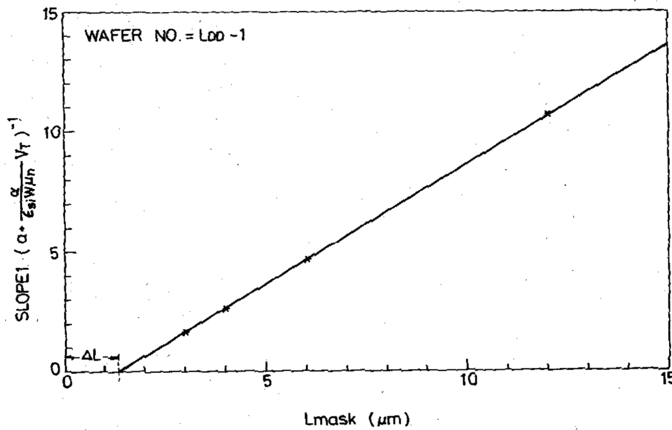

Fig. 6. The SLOPE1 $(a + \alpha/\epsilon_{si} w\mu_n V_{T0})^{-1}$ versus L_{mask} relation. ΔL can be obtained from the intercept in the horizontal coordinate.

and applying the least squares method again to the SLOPE1 versus $(a + \alpha V_{T0}/W\mu_n\epsilon_{si}) \cdot L_{mask}$ relation, ΔL and a can be determined by the iterative calculations and the SLOPE1 $\cdot$ $(a + \alpha V_{T0}/W\mu_n\epsilon_{si})^{-1}$ versus L_{mask} relation is plotted in Fig. 6. Using (51) and (52), μ_n, α, ΔL, R_p $(= R_{ns}^0 + R_s + R_{nd}^0 + R_d)$ can be solved. The extracted parameters are given in the second row of Table II.

For long-channel devices, the major part of the voltage drop is in the channel region and the resistances of the n$^-$ regions near the source–drain can be assumed to be the same, i.e., $R_{ns}^0 + R_s = R_{nd}^0 + R_d = R_p/2$. To determine the parameters η and β, the drain current is measured for each of the long-channel devices ($L_{mask} \gtrsim 4$ μm) at the drain voltage less than the saturation voltage. Using (2), (26), and (27), we can obtain the value of $AT(=\eta + \beta/L)$ for each device with different channel lengths. Plotting the AT versus $1/L$ relation as shown in Fig. 7, η and β can be obtained from the slope and the intercept in the vertical coordinate. Therefore, the critical field and saturation velocity can be determined by $E_c = \beta^{-1}$ and $V_{sl} = \mu_n/\beta$.

The sum of contact resistance and spreading resistance due to the n$^+$ diffusion islands ($R_s + R_d$) was extracted from the fabricated devices without n$^-$ spacers by using the extrapolation method as shown in 2) for $R_{ns}^0 = R_{nd}^0 = 0$ and the extracted $R_s(=R_d)$ is listed in Table II. The effective mobility (μ_{eff}) used in (35) was obtained by using the average value of the effective mobility with the extracted parameters for the gate voltage changed from 0 to 5 V.

3) Parameters in the n$^-$ Region: Since the parameters r_n, l_1, and l_2 were determined by the SEM cross section and spreading analyses, the average doping concentration in the n$^-$ region can be estimated by the measured doping profile and the average value for a step profile approximation is $N_d \cong 2.5 \times 10^{17}/\text{cm}^3$ as shown in Table III. The calculated effective dose in the n$^-$ region $(N_d r_n)$ is $0.625 \times 10^{13}/\text{cm}^2$, which is in reasonable agreement with the total phosphorus dose of $10^{13}/\text{cm}^2$ implanted across the gate oxide with an energy of 30 keV. Based on the known N_d value, the average mobility in the bulk n$^-$ region (μ_b) can be obtained from the following empirical expression [11]:

TABLE III
PARAMETERS USED IN THE n^- REGION

μ_b (cm^2/v-s)	μ_s (cm^2/v-s)	N_d (cm^{-3})	r_n (μm)	l_1 (μm)	l_2 (μm)	V_{FBn} (V)
542.74	542.74	2.5 x 10^{17}	0.25	0.45	0.2	-0.5

$$\mu_b = \frac{1360 - 92}{1 + \left(\dfrac{N_d}{1.3 \times 10^{17}}\right)^{0.91}} + 92. \qquad (54)$$

The calculated μ_b is 542.74 cm^2/V · s, which is shown in Table III. For simplicity, the surface mobility in the accumulation layer of the n^- region (μ_s) is assumed to be the same as the calculated μ_b. The average doping concentration in the channel region (N_a) is chosen to be $N_{AS} + N_{AB}$, which is equal to the average doping concentration in the channel for shallow boron implantation. However, the average doping concentration (N_a) under the n^- region is chosen to be $N_{AD} + N_{AB}$, which is equal to the average doping concentration under the gate for deep boron implantation when $r_n + W_d < Y_s + W_b$; when $W_d > Y_s + W_b - r_n$, the average doping concentration under the n^- region can be calculated by $N_a = [N_{AD}(Y_s + W_b - r_n) + N_{AB} W_d]/W_d$, which may occur as the backgate is large. The flat-band voltage in the n^- region (V_{FBn}) is determined by the best fitting in the low drain current and is found to be equal to -0.5 V. The major contribution of V_{FBn} is found to add an offset current at low gate voltage for the I–V characteristics.

IV. Comparisons Between Experimental Results and Simulations

As described in Section III, the parameters in the threshold-voltage model [8] for double-channel-boron implantations have been extracted from the fabricated long-channel MOSFET's. Similarly, the threshold-voltage model developed in [8] for short-channel devices can be used to simulate the threshold voltages of the fabricated short-channel LDD devices. Using the parameters listed in Table I, comparisons between the measured threshold voltages and the simulation results are shown in Fig. 8, in which the shortest effective channel length is 0.68 μm. It is clearly seen that satisfactory agreement has been obtained for wide ranges of channel lengths and applied substrate biases and the discrepancy for shorter channel-length devices operated at higher substrate biases is mainly due to the simplified charge-sharing scheme used in the threshold-voltage model.

In order to simulate the I–V characteristics of the fabricated LDD devices, the extracted parameters shown in Tables II and III should be used. However, two parameters (μ_n and β) listed in Table II have been slightly adjusted in order to have the best fittings for the I–V characteristics of shorter channel-length devices, and the adjusted parameter values are given in the third row of Table II. The slight adjustments for μ_n and β are understandable because the original μ_n and β values have been extracted from the fabricated long-channel devices and the hyperbolic mobility model used has been known to overestimate the scattering-limited velocity ($V_{sl} = \mu_n/\beta$) for shorter channel-length devices if the extracted μ_n and β values are used. Therefore, the slight adjustments for μ_n and β will slightly sacrifice the simulation accuracy for long-channel devices but will produce better simulation results for shorter channel devices. Figs. 9 and 10 show comparisons of the I–V characteristics between the experimental data and the developed model for longer channel lengths ($L > 4$ μm), in which the asterisks shown in the figures indicate the calculated saturation voltages for the corresponding gate voltages. Similarly, comparisons for shorter channel lengths ($L = 1.18$ and 0.64 μm) are shown in Figs. 11 and 12. It is clearly seen that agreement

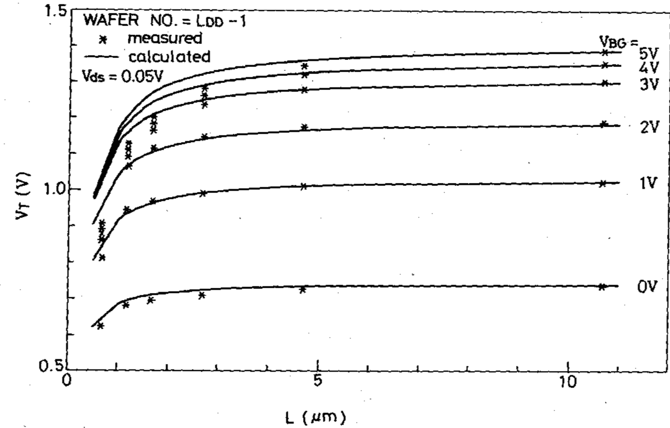

Fig. 8. Comparisons between the measured threshold voltages and the theoretical calculations at $V_{ds} = 0.05$ V.

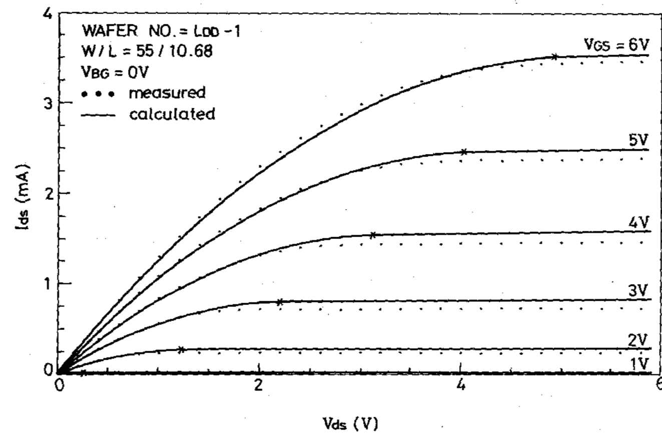

Fig. 9. Comparisons between the measured and calculated I–V characteristics for $L = 10.68$ μm with $V_{BG} = 0$ V.

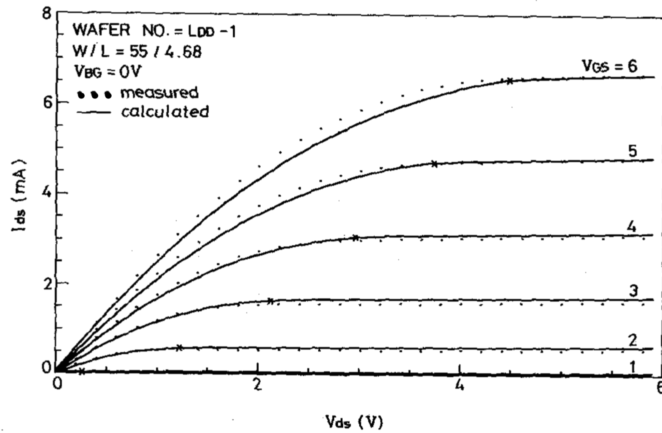

Fig. 10. Comparisons between the measured and calculated *I–V* characteristics for $L = 4.68$ μm with $V_{BG} = 0$ V.

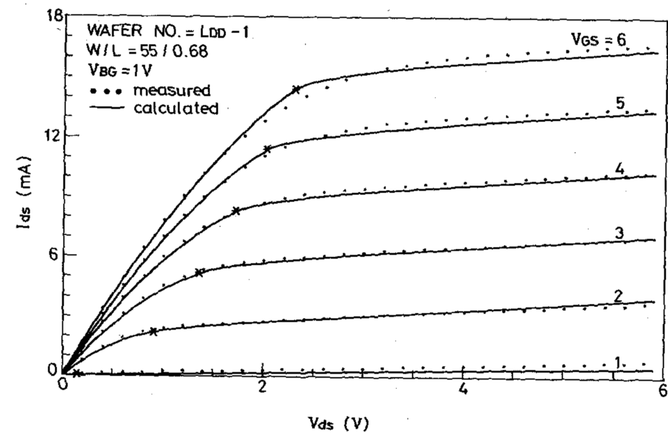

Fig. 13. Comparisons between the measured and calculated *I–V* characteristics for $L = 0.68$ μm with $V_{BG} = 1$ V.

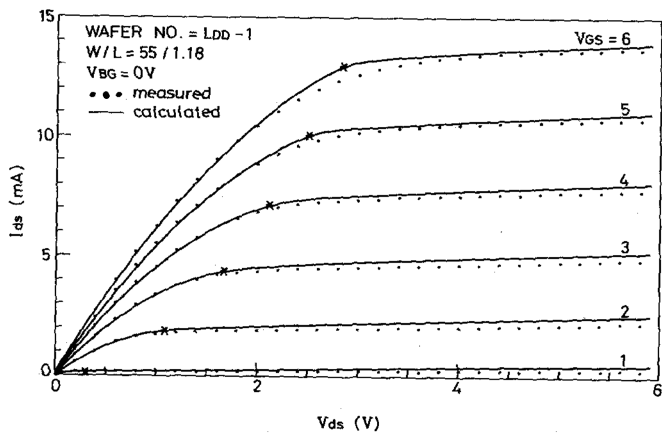

Fig. 11. Comparisons between the measured and calculated *I–V* characteristics for $L = 1.18$ μm with $V_{BG} = 0$ V.

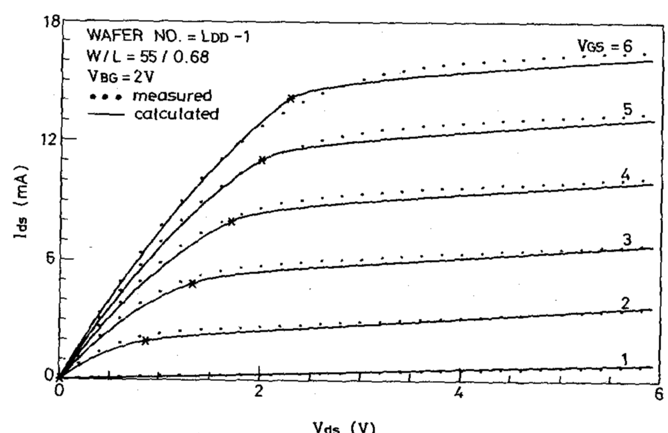

Fig. 14. Comparisons between the measured and calculated *I–V* characteristics for $L = 0.68$ μm with $V_{BG} = 2$ V.

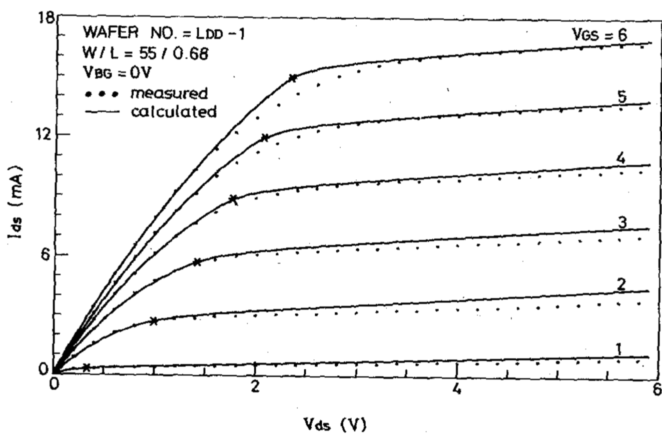

Fig. 12. Comparisons between the measured and calculated *I–V* characteristics for $L = 0.68$ μm with $V_{BG} = 0$ V.

between the experimental data and the simulation results becomes better as the channel length is reduced, as expected from the adjusted β and μ_n values. Note that for all simulated channel lengths, the maximum error is no more than 9 percent and the global error is less than 5 percent (only 3 percent for $L = 0.68$ μm). In order to show the effects of substrate bias on the *I–V* characteristics, comparisons for an effective channel length of 0.64 μm with different applied substrate biases ($V_{BG} = 1$ and 2 V) are shown in Figs. 13 and 14. Similarly, satisfactory agreement between the experimental data and the simulation results is obtained for different applied substrate biases. The global error for $V_{BG} = 1.0$ V is 2 percent and that for $V_{BG} = 2.0$ V is 3.5 percent.

V. Conclusions

In this paper, an analytic *I–V* model for MOSFET's with an LDD structure has been developed by considering the n^- region as a modified buried-channel MOS device and the channel region as an intrinsic enhancement-mode MOSFET. Although the developed model looks complicated, it is a structure/process-oriented model. Moreover, the drain current is explicitly expressed in terms of terminal voltages and, therefore, the drain in the linear/saturation regions and the saturation voltage can be directly calculated from the known terminal voltages. In order to verify the accuracy of the developed *I–V* model, the test devices with the LDD structure fabricated by a standard process have been measured and the methods for extracting the model parameters are presented. It has been shown that satisfactory agreement between the experimental *I–V*

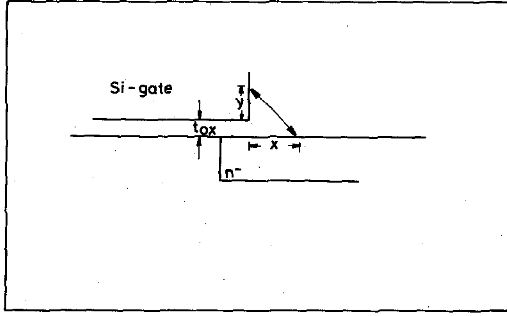

Fig. 15. The schematic diagram for calculating the effective capacitance ($C(x)$) for the surface charge layer in the n$^-$ region.

characteristics and the simulation results has been obtained for wide ranges of channel lengths and applied biases by using a set of parameters. Therefore, the developed model can be used for device design and circuit analysis in a CAD system.

Appendix A

Assuming that the line of the electric field is straight as shown in Fig. 15, the normal electric field at the surface of the n$^-$ region with respect to the gate can be expressed by

$$E_N(x, y) = \frac{\epsilon_{ox}(y + t_{ox})}{x^2 + (y + t_{ox})^2}\left[V_{g2} - V_{FBn} - V(x)\right]. \tag{A1}$$

It is assumed that the effective capacitance is defined at the condition of the maximum electric field with respect to y. Using

$$\left.\frac{dE_N}{dy}\right|_{y=y_0} = 0 \tag{A2}$$

and

$$y_0 = x - t_{ox} \tag{A3}$$

the maximum electric field can be expressed as

$$\begin{aligned}\max E_N(x) &= \frac{\epsilon_{ox}}{2x}\left[V_{g2} - V_{FBn} - V(x)\right]\\ &= C(x)\left[V_{g2} - V_{FBn} - V(x)\right]\end{aligned} \tag{A4}$$

where $C(x)$ is the effective capacitance per unit area for $t_{ox} \le x \le l_1$. For $0 \le x \le t_{ox}$, the maximum electric field is obtained by $y_0 = t_{ox}$. For $-l_2 \le x \le 0$, the electric field is assumed to be uniform along the n$^-$ region. Then, the effective capacitance per unit area can be expressed as

$$C(x) = \begin{cases} \dfrac{\epsilon_{ox}}{t_{ox}}, & -l_2 \le x \le 0 \\ \dfrac{\epsilon_{ox} t_{ox}}{x^2 + t_{ox}^2}, & 0 \le x \le t_{ox} \\ \dfrac{\epsilon_{ox}}{2x}, & t_{ox} \le x \le l_1. \end{cases} \tag{A5}$$

Appendix B

From (3)–(6), we can get the following results:

$$\begin{aligned} I_{ds}(l_1 + l_2) = W\Bigg[&\mu_b q N_d\left(r_n V_{d2} - \int_0^{V_{d2}} \Delta r_n dV\right)\\ &+ \mu_s \overline{C}\left(V_{g2} - V_{FBn} - \frac{1}{2}V_{d2}\right)V_{d2}\Bigg] \end{aligned} \tag{B1}$$

where

$$\begin{aligned}\int_0^{V_{d2}} \Delta r_n dV &= \frac{2}{3}\left(\frac{2\epsilon_{si}N_a}{qN_d(N_a + N_d)}\right)^{1/2}\left[(V_{bi} + V_{BG} + V_{d3})^{3/2}\right.\\ &\quad \left. - (V_{bi} + V_{BG} + V_{d4})^{3/2}\right]\\ &\cong \left(\frac{2\epsilon_{si}N_a}{qN_d(N_a + N_d)}\right)^{1/2}(V_{bi} + V_{BG} + V_{ds})^{1/2}V_{d2}\\ &= \Delta r_{ne} V_{d2}\end{aligned} \tag{B2}$$

and

$$\begin{aligned}\overline{C} &= \frac{\displaystyle\int_0^{V_{d2}} C(x)\left[V_{g2} - V_{FBn} - V(x)\right]dV}{\displaystyle\int_0^{V_{d2}}\left[V_{g2} - V_{FBn} - V(x)\right]dV}\\ &\cong \frac{\displaystyle\int_{-l_2}^{l_1} C(x)(x + l_2)\,dx}{\displaystyle\int_{-l_2}^{l_1}(x + l_2)\,dx}\\ &= \frac{\dfrac{\epsilon_{ox}}{t_{ox}}l_2^2 + \epsilon_{ox}t_{ox}\left[\ln(2) + \dfrac{\pi}{8}\dfrac{l_2}{t_{ox}}\right] + \epsilon_{ox}\left[(l_1 - t_{ox}) + l_2\ln\left(\dfrac{l_1}{t_{ox}}\right)\right]}{(l_1 + l_2)^2}.\end{aligned} \tag{B3}$$

Note that (B3) is derived by considering the case that the n^- region is partially overlapped by the Si gate. For the extreme case that the n^- region is just outside the silicon gate, (B3) is still valid and the result can be obtained by setting l_2 equal to zero. For the case of $l_1 = 0$, the average capacitance is equal to the gate-oxide capacitance.

Appendix C

Referring to Fig. 3, the one-dimensional Poisson's equation in the pinchoff region can be expressed as follows [9]. For $-\Delta L_1 \le x < 0$, we have

$$\frac{d^2V(x)}{dx^2} = \frac{1}{\epsilon_{si}}\left[qN_{AB} + \frac{J(x)}{V_{sl}}\right] \tag{C1}$$

$$J(x) = \frac{I_{dsat}}{Wy(x)} \tag{C2}$$

$$y(x) = \frac{r_n - d}{\Delta L_1}x + r_n. \tag{C3}$$

For $0 < x \le \Delta L_2$, we have

$$\frac{d^2V}{dx^2} = \frac{1}{\epsilon_{si}}\left[-qN_d + \frac{J(x)}{V_{sl}}\right] \tag{C4}$$

$$J(x) = \frac{I_{dsat}}{Wr_n} \tag{C5}$$

where d is the thickness of the inversion layer that can be calculated by

$$d = \frac{k_BT}{q|E_s|} \tag{C6}$$

where the surface electric field (E_s) can be calculated from [8].

The boundary conditions can be written by

$$V(x)\big|_{x=-\Delta L_1} = V_{dsat} \qquad \frac{dV}{dx}\bigg|_{x=-\Delta L_1} = E_c$$

$$V(x)\big|_{x=0} = V_{d1} \qquad \frac{dV}{dx}\bigg|_{x=0^-} = \frac{dV}{dx}\bigg|_{x=0^+}$$

$$V(x)\big|_{x=\Delta L_2} = V_{d0} \qquad \frac{dV}{dx}\bigg|_{x=\Delta L_2} = E_c. \tag{C7}$$

Using the boundary conditions in (C7), Poisson's equation can be solved and the result is

$$V_{d0} - V_{dsat} = E_c\left(1 - \frac{A}{B}\right)\Delta L_1 + \frac{1}{\epsilon_{si}}\left(C - \frac{A^2}{2B}\right)\Delta L_1^2 \tag{C8}$$

where

$$A = qN_{AB} + \frac{I_{dsat}}{WV_{sl}(r_n - d)}\ln\left(\frac{r_n}{d}\right) \tag{C9}$$

$$B = -qN_d + \frac{I_{dsat}}{WV_{sl}r_n} \tag{C10}$$

$$C = \frac{qN_{AB}}{2} + \frac{I_{dsat}r_n}{WV_{sl}(r_n - d)^2}\left[\ln\left(\frac{r_n}{d}\right) - \left(1 - \frac{d}{r_n}\right)\right]. \tag{C11}$$

It is assumed that the resistance of the n^- region near the drain where the electric field does not reach the critical field E_c can be approximated by

$$R'_{nd} = R_{nd}\frac{l_1 + l_2 - \Delta L_2}{l_1 + l_2} \tag{C12}$$

where R_{nd} is equal to the resistance at the saturation voltage.

Using $V_{d0} = V_{ds} - I_{dsat}(R_s + R_{ns} + R_d + R'_{nd})$, ΔL_1 can be solved from the following equation:

$$V_{ds} - I_{dsat}(R_s + R_{ns} + R_d + R_{nd}) - V_{dsat} = \frac{I_{dsat}R_{nd}A}{(l_1 + l_2)B}\Delta L_1 + E_c\left(1 - \frac{A}{B}\right)\Delta L_1 + \frac{1}{\epsilon_{si}}\left(C - \frac{A^2}{2B}\right)\Delta L_1^2. \tag{C13}$$

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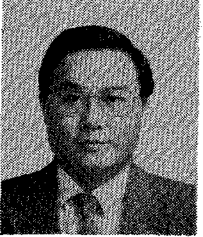

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