The Effects of Thermal Nitridation Conditions on the Reliability of Thin Nitrided Oxide Films

HONG-HSIANG TSAI, LIANG-CHONG WU, CHING-YUAN WU, MEMBER, IEEE, AND
CHENMING HU, SENIOR MEMBER, IEEE

Abstract—**MIS capacitors on n-type silicon substrate with thin oxide films thermally nitrided in NH_3 gas ambient at different temperatures and for different times have been fabricated. The effects of nitridation temperature and time on the properties of the thin nitrided oxide films have been examined and analyzed by using a constant current stress. It is found that the oxide films nitrided at 900°C exhibit much improved total charge to breakdown and interface trap generation if proper nitridation time is used. The superior characteristics of the fabricated nitrided oxide films using the proposed optimum conditions are suitable for existing CMOS/VLSI applications.**

I. INTRODUCTION

THE GROWTH of high-quality and more reliable thin-gate insulators is an important issue in future scaled MOS/VLSI technology. Recently, the oxynitride films fabricated by nitriding thermally grown thin oxide have been considered to be a valuable alternative to pure silicon dioxide films for MOS/VLSI application. Many activities in the study of oxynitride have been focused on compositional analysis and electrical characterization of the as-grown nitrided oxide films [1]–[6]. However, only a few results on the reliability performance of the thin nitrided oxide films have been reported [7].

In this letter, MIS capacitors with thin nitrided oxide films prepared at various nitridation conditions have been examined under a constant Fowler–Nordheim tunneling current stress. The dependencies of endurance properties such as total charge to breakdown, flat-band voltage shift, and interface trap generation on the nitridation conditions have been analyzed. The optimum nitridation condition for obtaining a high-quality thin gate insulator has also been demonstrated.

II. SAMPLE PREPARATION

The MIS capacitors used in this study were fabricated on 15–25-Ω·cm n-type (100)-oriented silicon wafers by using the conventional polysilicon-gate self-aligned MOS process including local oxidation (LOCOS) technique. The gate oxide with a thickness of 250 Å was grown by dry O_2 oxidation at 920°C and *in-situ* annealed at the same temperature in N_2 ambient for 30 min. The grown gate oxide films were then transferred to another furnace and thermally nitrided in NH_3 gas ambient at 900, 1000, 1100, and 1150°C for 0, 0.5, and 3 h. The wafers were loaded into the furnace at 900°C, then ramped to the desired nitridation temperature for nitridation, and finally ramped down for unloading. A LPCVD polysilicon layer of about 4500 Å was deposited and then doped by arsenic ion implantation. After subsequent drive-in step at 1000°C, the proper lithographic steps and a self-aligned implantation of boron ions with a dose of 2×10^{15} cm^{-2} at 30 keV were carried out, which resulted in a p^+ region formed around the polysilicon gate edge. Using a double photoresist technology, the counterdoping of As-doped polysilicon gate with born implant can be easily prevented. After the deposition of CVD SiO_2, all wafers were reflowed at 1038°C for 30 min to obtain a smooth surface morphology for good metallization step coverage. The process steps including contact etching, metallization, and forming gas annealing at 430°C were then performed to obtain the final MIS capacitor structures with an area of 250×250 μm^2.

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

The fabricated MIS capacitors were first measured for the interface state density and the flat-band voltage, and then stressed with a constant current density to examine the endurance properties. During the constant current stress, the interface trap generation, the flat-band voltage, and the charge to breakdown were monitored. The measured results are discussed below.

A. Total Charge to Breakdown

Table I shows the total charge to breakdown Q_{bd} under a constant substrate-injected current stress of 10 mA/cm^2 for 250-Å thin oxide films nitrided at various temperatures and times. For the pure oxide case, the Q_{bd} observed under a lower constant current stress of 1 mA/cm^2 is only 0.3 C/cm^2; if the stress current is 10 mA/cm^2, the Q_{bd} will be an order of magnitude lower than that of the 1-mA/cm^2 case. This is mainly due to oxide degradation induced by the 1038°C high-temperature step [8]. On the other hand, the samples with the oxide nitrided at 900°C for both 0.5 and 3 h have much higher resistance against the 1038°C high-temperature step, and

---

Manuscript received October 6, 1986; revised January 16, 1987. This work was supported by a grant from the Electronics Research Service Organization (ERSO), Industrial Technology Research Institute (ITRI), Taiwan, Republic of China.

H.-H. Tsai and L.-C. Wu are with the Institute of Electronics, College of Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China, and the IC Development Center, Electronics Research and Service Organization (ERSO), Industrial Technology Research Institute (ITRI), Hsin-Chu, Taiwan, Republic of China.

C.-Y. Wu is with the Institute of Electronics, College of Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, Republic of China.

C. Hu is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

IEEE Log Number 8613761.

0741-3106/87/0400-0143$01.00

TABLE I
DEPENDENCE OF TOTAL CHARGE-TO-BREAKDOWN Q_{bd} ON THE NITRIDATION TEMPERATURE AND TIME OF THE NITRIDED GATE INSULATORS

The stress current density for pure oxide is 1 mA/cm^2 and that for nitrided oxide is 10 mA/cm^2.

Nitrid. Temp. / Nitrid. Time	900 °C	1000 °C	1100 °C	1150 °C	SiO$_2$
0.5 hour	40.8 C/cm^2	0.2 C/cm^2	0.3 C/cm^2	1.2 C/cm^2	0.3 C/cm^2
3 hour	18.7 C/cm^2	–	1.5 C/cm^2	5.2 C/cm^2	

TABLE II
DEPENDENCE OF NITRIDATION-INDUCED NEGATIVE FLAT-BAND VOLTAGE V_{fb} OF THE UNSTRESSED CAPACITORS ON THE NITRIDATION TEMPERATURE AND TIME

Nitrid. Temp. / Nitrid. Time	900 °C	1000 °C	1100 °C	1150 °C	SiO$_2$
0.5 hour	-0.987V	-1.237V	-0.512V	-0.410V	-0.167V
3 hour	-1.363V	——	0.174V	0.227V	

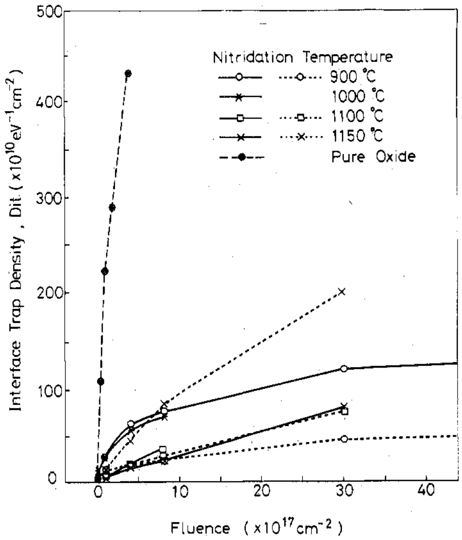

Fig. 1. Interface trap density generation as a function of the substrate-injected electron fluence of 0.5- (solid lines) and 3-h (dotted line) nitridation at various temperatures. The stress current density for pure oxide is 1 mA/cm^2 and that for nitrided oxide is 10 mA/cm^2.

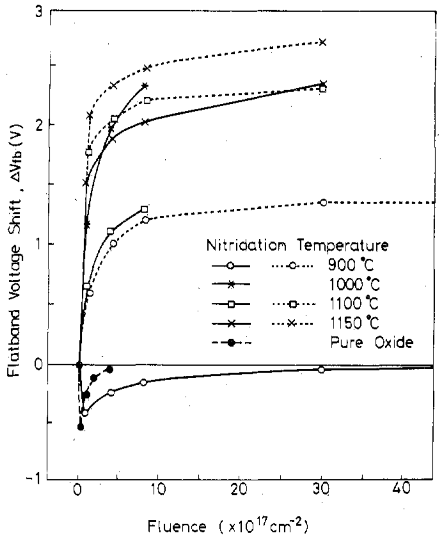

Fig. 2. Flat-band voltage shift as a function of the substrate-injected electron fluence for 0.5- (solid lines) and 3-h (dotted lines) nitridation at various temperatures. The stess current density for pure oxide is 1 mA/cm^2 and that for nitrided oxide is 10 mA/cm^2.

therefore exhibit much higher Q_{bd} than that of the pure SiO$_2$ film. For nitridation temperatures higher than 900°C, the Q_{bd} is always much smaller than that of the 900°C case and appears to slightly increase with increasing nitridation temperature and time. However, the nitrided oxide films always show longer operating lifetime than the pure SiO$_2$ films.

B. Interface Trap Density Generation

The generation of the interface trap density D_{it} as a function of the injected electron fluence for the nitridation times of 0.5 and 3 h, monitored during the constant current stress, is shown in Fig. 1. For the case with 0.5-h nitridation (solid lines), it is found that the generation of the interface traps can be much reduced by thermal nitridation and higher nitridation temperatures exhibit lower D_{it} generation. The reduction of D_{it} generation seems to correlate with the degree of nitridation for the SiO$_2$ films. On the other hand, the case with 3-h nitridation (dotted lines) exhibits a reverse trend for the D_{it} generation when compared to that of the 0.5-h nitridation case. For the case of 3-h nitridation, the lower nitridation temperature provides a lower D_{it} generation. Moreover, the generation of D_{it} for the 900°C nitridation case is largely reduced to one-third of the value for 0.5-h nitridation while that for the 1150°C nitridation case is increased to about two times. It appears that a higher degree of nitridation can effectively reduce the D_{it} generation, but too high a temperature for 3-h nitridation may degrade the quality of the nitrided oxide. However, it is very clear that the nitrided silicon dioxide always shows more improvement in the generation of the interface trap density compared to the pure silicon dioxide.

C. Flat-Band Voltage Shift

The flat-band voltages V_{fb} of the unstressed MIS capacitors are shown in Table II. It is clearly seen that for the same nitridation time, the negative V_{fb} shift can be induced by the nitridation at lower temperature. The nitridation temperature-dependent flat-band voltage shift ΔV_{fb} as a function of the injected electron fluence for the nitridation times of 0.5 and 3 h, corresponding to Fig. 1, is shown in Fig. 2. The saturation tendency of the ΔV_{fb} shift in the higher fluence region observed in Fig. 2 exhibits the typical trap filling process. For the case of 0.5-h nitridation (solid lines), all of the nitridation temperature cases except the 900°C case always show much higher positive V_{fb} shift than the pure SiO$_2$ case. In the case of 900°C nitridation for 0.5 h, it is shown that the ΔV_{fb} shift with a small shift level and a turnaround behavior similar to that of the pure SiO$_2$ is believed to be due to lower nitridation level. On the other hand, the ΔV_{fb} shift for 3-h nitridation (dotted lines) is increased regularly with increasing nitridation temperature. Therefore it can be concluded that the higher the nitridation temperature or the longer the nitridation time is, the larger the ΔV_{fb} shift will be. The higher degree of nitridation can evidently create more electron traps in the bulk of the oxynitride, which could be a drawback with respect to improvement of the D_{it} generation. However, it is clear that nitridation at 900°C for a proper amount of time, for example 0.5 h, can substantially reduce the D_{it} generation, with the ΔV_{fb} shift as small as that of the pure SiO_2 films.

IV. SUMMARY

It has been shown that the endurance properties of the nitrided oxide films exhibit a strong dependency on nitridation temperature and time. In general, the thermally nitrided oxide films can provide higher total charge to breakdown, much reduced interface trap generation, and increased electron trapping compared to the pure SiO_2 films. However, the 250-Å oxide films nitrided at 900°C exhibit much higher total charge to breakdown without increasing electron trapping if proper nitridation time is adopted, indicating conditions that are suitable for future MOS/VLSI applications.

ACKNOWLEDGMENT

The authors would like to express special thanks to Dr. C. T. Shih and Dr. C. C. Chang for helpful discussions and support.

REFERENCES

[1] J. Amano and T. Ekstedt, "Characterization of thermally nitrided silicon dioxide," *Appl. Phys. Lett.*, vol. 41, p. 816, 1982.
[2] F. H. P. M. Habraken, A. E. T. Kuiper, and Y. Tamminga, "Thermal nitridation of silicon dioxide films," *J. Appl. Phys.*, vol. 53, p. 6996, 1982.
[3] Y. Yoriume, "Distribution of nitrogen in thermally nitrided SiO_2," *J. Vac. Sci. Technol.*, vol. B1, p. 67, 1983.
[4] T. Ito, T. Nakamura, and H. Ishikawa, "Effect of thermally nitrided SiO_2 (nitroxide) on MOS characteristics," *J. Electrochem. Soc.*, vol. 129, p. 184, 1982.
[5] Y. Hayfuji and K. Kajiwara, "Nitridation of silicon and oxidized-silicon," *J. Electrochem. Soc.*, vol. 129, p. 2102, 1982.
[6] M. M. Moslehi, C. J. Han, K. C. Saraswat, C. R. Helms, and S. Shatas, "Compositional studies of thermally nitrided silicon dioxide (nitroxide)," *J. Electrochem. Soc.*, vol. 132, p. 2189, 1985.
[7] S. Chang, N. Johnson, and S. Lyon, "Capture and tunnel emission of electrons by deep levels in ultrathin nitrided oxides on silicon," *Appl. Phys. Lett.*, vol. 44, no. 3, p. 316, 1984.
[8] S. Holland and C. Hu, "Correlation between breakdown and process-induced positive charge trapping in thin thermal SiO_2," *J. Electrochem. Soc.*, vol. 133, p. 1705, 1986.