A New Structure-Oriented Model for Well Resistance in CMOS Latchup Structures

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Abstract—**A new analytical model has been developed to deal with the parasitic well resistance in CMOS structures. This model also provides a closed-form expression for the induced potential drop in the well due to the action of an emitter in the substrate, and is expressed in terms of the structure parameters in the well, the well sheet resistance, and the current density across the well–substrate junction. Based on the developed model, the calculated potential drops for various structures have been compared with the experimental results and good agreement has been obtained. Furthermore, the steady-state collector current of an active parasitic lateral bipolar transistor, which is used to trigger the parasitic vertical bipolar transistor into the latchup, has been calculated using the developed model. The calculated triggering currents in excess of 1 mA have a maximum error of 20 percent when compared with the experimental results measured from various structures. This error may be improved by taking into account the accurate position-dependent well sheet resistance. Therefore, the developed model becomes an efficient design tool for protecting the devices in the well from being disturbed by an active emitter in the substrate.**

I. Introduction

In a CMOS circuit, the majority-carrier current in the well injected by an active emitter in the substrate can produce a resistive potential drop in the well. This potential drop may trigger the CMOS circuit into the latchup state and causes permanent damage on the related devices. Even if this potential drop is not sufficient to trigger the latchup, it may result in the malfunction of the circuit such as the leakage current discharging a charge-storage node located within the well. Therefore, it is valuable to develop a model to calculate the majority-carrier current required to induce a given potential drop in the well. Pinto and Dutton [1] have presented the accurate analysis in this respect using full two-dimensional numerical simulation. To greatly improve the computational efficiency, however, it is desirable to use a simple method with considerable accuracy. Traditionally, such a method has been presented with the well sheet resistances multiplied by the corresponding numbers of squares in the pinched well [2]. The accuracy of this method in the prediction of the steady-state triggering current for latchup has been verified experimentally [3]. However, this method is not applicable for the case of the topside well contact placed close to the well edge, i.e., the guard ring in the well. In this paper, a new analytical model is presented to perform the work in a more accurate manner. Based on the developed model, calculated results such as the induced potential drop in the well and the steady-state triggering current for latchup are compared with the experimental data measured from various fabricated structures.

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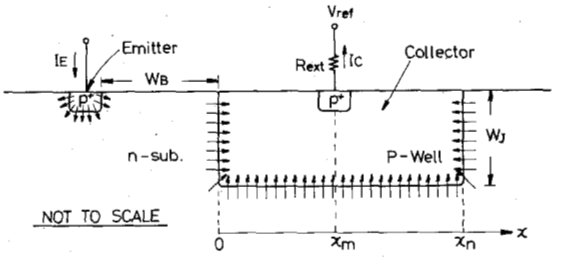

Fig. 1. Cross-sectional view of a parasitic p-n-p transistor in the p-well CMOS circuits. The holes are injected from the active emitter into the substrate, some of which are collected by the p-well.

II. Model

Fig. 1 shows a cross section of a lateral p-n-p transistor that is used to represent a parasitic bipolar device in the p-well CMOS circuits. Moreover, this transistor uses a long-stripe shape geometry with the stripe length denoted as l_E. As this transistor is operated in the active regime, its p^+-emitter injects the holes into the substrate, some of which are collected by the well–substrate junction and become the majority carriers in the well. Fig. 1 also shows that not only the sidewall of the well–substrate junction but also the bottom side of the well–substrate junction contribute to the collection of the holes. This feature is included in the proposed model shown in Fig. 2 where the position-dependent current source labeled $J_\perp(x)\, l_E\, dx$ accounts for the total collector current across the bottom area of $l_E\, dx$ and the current sources labeled I_0 and I_0' represent the collector currents across the left-hand and right-hand sides of the well–substrate junction, respectively. Note that $J_\perp(x)$ is the position-dependent collector current density per unit area across the bottom side and dx is the incremental length in the x-direction. The model uses a one-dimensional distributed network to appropriately represent the parallel flow lines of the majority-carrier current in the pinched well. In addition, the resistance labeled R_{ext} in Fig. 2 represents the contact resistance.

Using the superposition principle, the potential drop in the well based on Fig. 2 can be shown to be

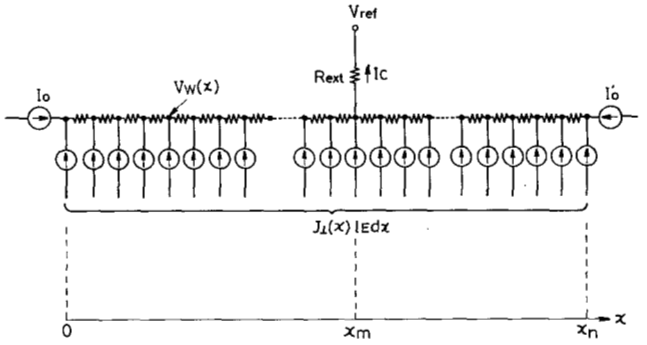

Fig. 2. The new model used to calculate the induced potential drop or equivalently the well resistance.

in the bulk case, while for the epi case the lightly doped epitaxial layer uses a doping of 10^{15} cm^{-3} and the heavily doped substrate uses a doping of 4×10^{19} cm^{-3}. It has been found [5] through this numerical procedure that the greatly suppressed $J_\perp(x)$ for the epi case as shown in Fig. 3 is mainly due to Auger recombination inherent in the heavily doped substrate rather than the consequence of reflection action at the high–low junction. From Fig. 3, it is observed that $l_E J_\perp(x)$ can be appropriately represented by $be^{-ax} I_0$ where a and b are the positive constants. In a similar way, we make $I_0' = cI_0$ where c is a positive constant. Consequently, the well transfer resistance can be expressed in a more compact manner by

$$V_w(x) - V_{\text{ref}} = \begin{cases} \left(I_0 + \int_0^x l_E J_\perp(x')\,dx'\right) R_{T1}(x) + \int_x^{x_m} l_E J_\perp(x')\,R_{T1}(x')\,dx' + I_c R_{\text{ext}}, \\ \qquad \text{for} \quad 0 \le x \le x_m \\ \left(I_0' + \int_x^{x_n} l_E J_\perp(x')\,dx'\right) R_{T2}(x) + \int_{x_m}^{x} l_E J_\perp(x')\,R_{T2}(x')\,dx' + I_c R_{\text{ext}}, \\ \qquad \text{for} \quad x_m \le x \le x_n \end{cases} \tag{1}$$

where the voltage $V_w(x)$ minus V_{ref} is the position-dependent potential drop in the well. Note that R_{T1} and R_{T2} in the above equations are expressed by

$$R_{T1}(x) = \int_x^{x_m} \rho_\square \frac{dx'}{l_E}$$

and

$$R_{T2}(x) = \int_{x_m}^{x} \rho_\square \frac{dx'}{l_E} \tag{2}$$

where $\rho_\square$ is the position-dependent well sheet resistance and dx'/l_E represents the incremental number of squares. Furthermore, the total collector current I_c can be expressed by

$$I_c = I_0 + \int_0^{x_n} l_E J_\perp(x)\,dx + I_0'. \tag{3}$$

Therefore, the transfer resistance [4] denoted as $R_w(x)$ in the well can be obtained by using (1) divided by (3). Note that the special case of $J_\perp(x) = 0$ and $I_0' = 0$ in the above expressions for $0 \le x \le x_m$ represents the traditional method for calculating the well resistance.

A two-dimensional numerical procedure [5] has been performed on the structure shown in Fig. 1 and the calculated result for the integral of $J_\perp(x)$ is shown in Fig. 3. This numerical procedure primarily includes 1) the solution of the low-level minority-carrier injection equation in the substrate with the appropriate boundary conditions; 2) the effects of Auger recombination, Shockley–Read–Hall recombinations, and energy-gap shrinkage; and 3) the effects of the reflection action at the high–low junction of the epi case. A substrate doping of 10^{15} cm^{-3} is used

$$R_w(x) = \begin{cases} \dfrac{\rho_\square\left\{\left(1 + \dfrac{b}{a}\right)(x_m - x) + \dfrac{b}{a^2}\left(e^{-ax_m} - e^{-ax}\right)\right\}}{l_E\left\{1 + \dfrac{b}{a}\left(1 - e^{-ax_n}\right) + c\right\}} + R_{\text{ext}}, \\ \qquad \text{for} \quad 0 \le x \le x_m \quad \text{and} \\ \dfrac{\rho_\square\left\{\left(c - \dfrac{b}{a}e^{-ax_n}\right)(x - x_m) + \dfrac{b}{a^2}\left(e^{-ax_m} - e^{-ax}\right)\right\}}{l_E\left\{1 + \dfrac{b}{a}\left(1 - e^{-ax_n}\right) + c\right\}} + R_{\text{ext}}, \\ \qquad \text{for} \quad x_m \le x \le x_n \end{cases} \tag{4}$$

Note that (4) has been developed using a constant $\rho_\square$ throughout the well. In a similar way, an analytical expression more complex than (4) can be easily derived for the case of position-dependent sheet resistance along the well.

III. Results and Discussion

To judge the validity of the proposed model, several fabricated structures based on standard p-well CMOS technology are presented. These structures are formed on the same bulk wafer with a well sheet resistance of about 11 kΩ/□ determined by an auto-spreading resistance probe. Moreover, these structures use long-stripe-shape geometries with a stripe length (l_E) of 150 μm so that the present two-dimensional simulation space is allowed to appropriately represent the actual three-dimensional case.

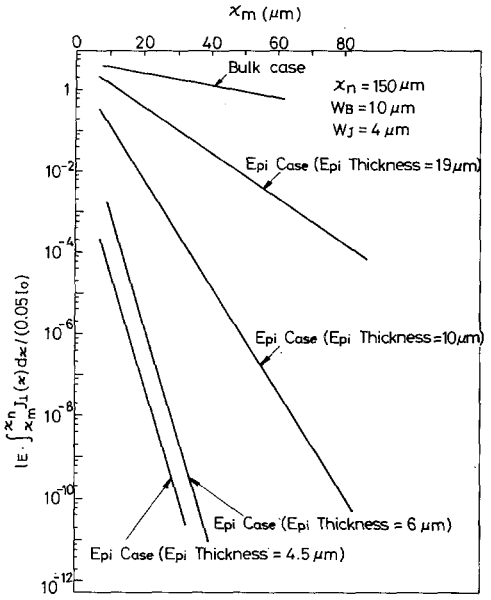

Fig. 3. The calculated $J_\perp(x)$ in the integral form as a function of x_n for the structure shown in Fig. 1 [5].

The experimental results for these structures and the simulated results based on the developed model are presented as follows.

A. Resistance Potential Drop

One of the fabricated structures used to investigate the induced potential drop in the well is shown in Fig. 4 where the values of relevant dimensions are indicated in details. There are three different definitions for terminal connections shown in Fig. 4: 1) the terminal V_{cl} is floating and the terminal V_{c2} is connected to the collector terminal; (2) the terminal V_{c2} is floating and the terminal V_{c1} is connected to the collector terminal; and (3) both the terminals V_{c1} and V_{c2} are connected to the identical collector terminal. The potential drop in the first terminal connection is defined as the voltage V_{c1} minus V_{c2} due to the current I_{c2}, while in the second terminal connection the potential drop is the voltage V_{c2} minus V_{c1} due to the current I_{c1}. Furthermore, the third terminal connection is used to verify the model on the correlation between I_{c1} and I_{c2} under the condition of $V_{c1} = V_{c2}$.

By fitting the integral of $be^{-ax} I_0$ to the numerical results of the bulk case in Fig. 3, we obtain $a = 0.03\ \mu m^{-1}$ and $b = 0.006\ \mu m^{-1}$ for $j_\perp(x)$, and in a similar way we have $c = 0.006$ for I_0' [5]. These numerically fitted data are used throughout the paper. The case of the first terminal connection has been calculated using (4) with $x = 1\ \mu m$, $x_m = 39.5\ \mu m$, and $x_n = 43\ \mu m$ for $R_{ext} = 0$ and 10 Ω. The calculated results are shown in Fig. 5 where the experimental results are also shown for comparisons. From Fig. 5, it can be seen that the model has yielded results that are in good agreement with the experimental data. The case of the second terminal connection is shown

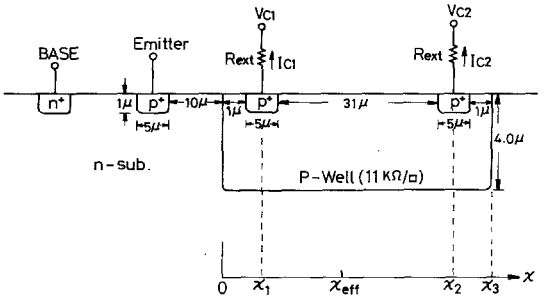

Fig. 4. The fabricated structure with the detailed relevant dimensions in order to verify the model.

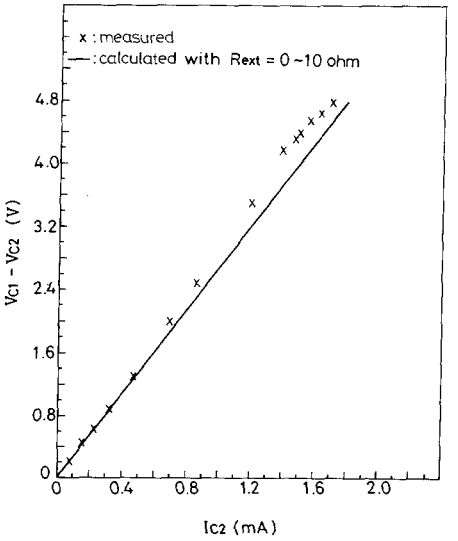

Fig. 5. The calculated and measured V_{c1} with respect to V_{c2} as a function of I_{c2} for Fig. 4 with $I_{c1} = 0$.

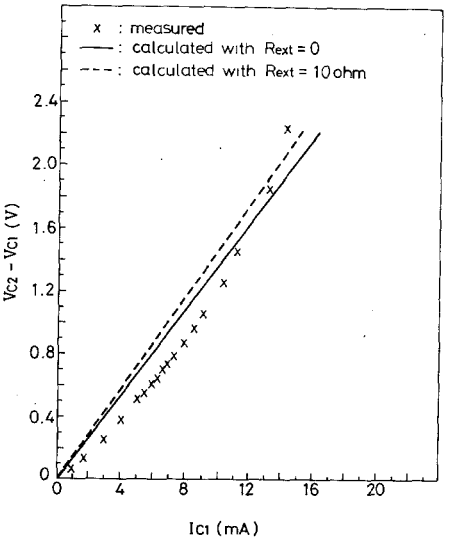

Fig. 6. The calculated and measured V_{c2} with respect to V_{c1} as a function of I_{c1} for Fig. 4 with $I_{c2} = 0$.

in Fig. 6 where the calculated results have been obtained using (4) with $x = 42\ \mu m$, $x_m = 3.5\ \mu m$, and $x_n = 43\ \mu m$ for $R_{ext} = 0$ and 10 Ω. As can be seen from Fig. 6, the

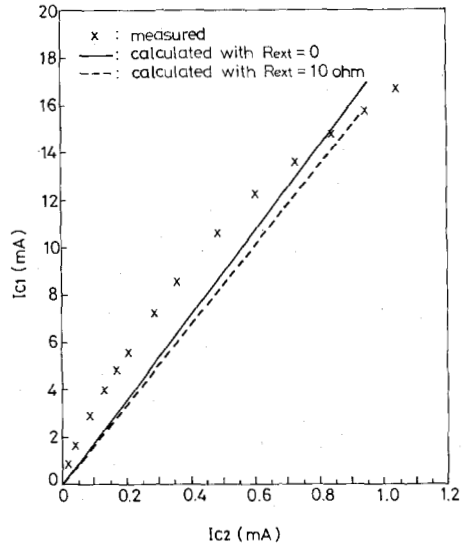

Fig. 7. The calculated and measured I_{c1} as a function of I_{c2} for Fig. 4 with $V_{c1} = V_{c2}$.

calculated results agree closely with the experimental data. Comparisons between Figs. 5 and 6 show that the spacing between the topside well contact and the emitter in the substrate should be less than that between the emitter in the well and the emitter in the substrate so that the induced potential drop under the emitter in the well can be greatly reduced for a given majority-carrier current. Furthermore, Fig. 7 shows the case of the third terminal connection where the calculated results have a maximum error of 30 percent when compared with the experimental data. The calculated results in Fig. 7 are based on the determination of a point labeled x_{eff} between the two topside well contacts by solving the following equation:

$$V_w(x_{\text{eff}}^-) - V_{c1} = V_w(x_{\text{eff}}^+) - V_{c2} \tag{5}$$

where

$$V_w(x) = \begin{cases} \left[\int_x^{x_{\text{eff}}} l_E J_\perp(x')\,dx'\right] \int_{x_1}^{x} \rho_\square \frac{dx'}{l_E} + \int_{x_1}^{x} l_E J_\perp(x') \left[\int_{x_1}^{x'} \rho_\square \frac{dx''}{l_E}\right] dx' + I_{c1}R_{\text{ext}} + V_{c1}, \\ \qquad \text{for} \quad x_1 \le x \le x_{\text{eff}}^- \\ \left[\int_{x_{\text{eff}}}^{x} l_E J_\perp(x')\,dx'\right] \int_{x}^{x_2} \rho_\square \frac{dx'}{l_E} + \int_{x}^{x_2} l_E J_\perp(x') \left[\int_{x'}^{x_2} \rho_\square \frac{dx''}{l_E}\right] dx' + I_{c2}R_{\text{ext}} + V_{c2}, \\ \qquad \text{for} \quad x_{\text{eff}}^+ \le x \le x_2. \end{cases}$$

Equation (5) states that the potential drop at the point x_{eff} is unique under $V_{c1} = V_{c2}$. Furthermore, the collector current density for $x < x_{\text{eff}}$ contributes to I_{c1} and the collector current density for $x > x_{\text{eff}}$ contributes to I_{c2}, i.e.

$$I_{c1} = I_0 + \int_0^{x_{\text{eff}}} l_E J_\perp(x)\,dx$$

and

$$I_{c2} = \int_{x_{\text{eff}}}^{x_3} l_E J_\perp(x)\,dx + I_0'. \tag{6}$$

By substituting $l_E J_\perp(x) = be^{-ax} I_0$ and $I_0' = cI_0$ into (5) and (6), and using a constant $\rho_\square$, we have

$$x_{\text{eff}} = \frac{1}{a} \ln \left\{ \frac{\rho_\square (x_2 - x_1) + 2R_{\text{ext}} l_E}{\rho_\square \frac{1}{a}(e^{-ax_1} - e^{-ax_2}) + \left(1 + \frac{a}{b} - \frac{ac}{b} + e^{-ax_3}\right) R_{\text{ext}} l_E} \right\} \tag{7}$$

$$I_{c1} = I_0 \left\{ 1 + \frac{b}{a}(1 - e^{-ax_{\text{eff}}}) \right\} \tag{8}$$

$$I_{c2} = I_0 \left\{ \frac{b}{a}(e^{-ax_{\text{eff}}} - e^{-ax_3}) + c \right\} \tag{9}$$

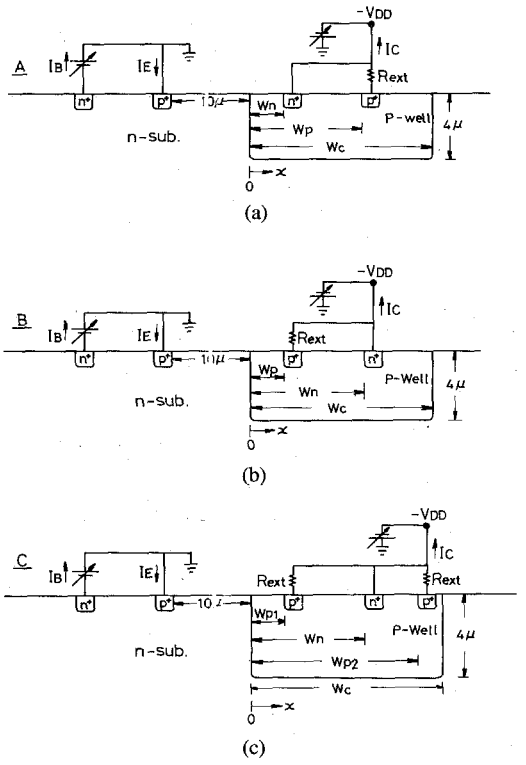

Fig. 8. The fabricated structures used to verify the accuracy of the model with respect to the steady-state triggering current. The relevant dimensions are shown in Table I.

and

$$R_w(x) = \begin{cases} \dfrac{\rho_\square \dfrac{b}{a}\left(x_1 e^{-ax_{\text{eff}}} - x e^{-ax_{\text{eff}}} + \dfrac{1}{a} e^{-ax_1} - \dfrac{1}{a} e^{-ax}\right) + \left[1 + \dfrac{b}{a}(1 - e^{-ax_{\text{eff}}})\right] R_{\text{ext}} l_E}{l_E\left\{1 + \dfrac{b}{a}(1 - e^{-ax_3}) + c\right\}}, \\ \qquad \text{for} \quad x_1 \le x \le x_{\text{eff}} \\ \dfrac{\rho_\square \dfrac{b}{a}\left(x_2 e^{-ax_{\text{eff}}} - x e^{-ax_{\text{eff}}} + \dfrac{1}{a} e^{-ax_2} - \dfrac{1}{a} e^{-ax}\right) + \left[\dfrac{b}{a}(e^{-ax_{\text{eff}}} - e^{-ax_3}) + c\right] R_{\text{ext}} l_E}{l_E\left\{1 + \dfrac{b}{a}(1 - e^{-ax_3}) + c\right\}}, \\ \qquad \text{for} \quad x_{\text{eff}} \le x \le x_2. \end{cases} \tag{10}$$

where $R_w(x)$ is defined as the potential drop ($V_w(x) - V_{c1}(=V_{c2})$) divided by the sum of I_{c1} and I_{c2}. Note that the calculated results in Fig. 7 have been obtained using $x_1 = 3.5\ \mu$m, $x_2 = 39.5\ \mu$m, and $x_3 = 43\ \mu$m. Moreover, an analytical model more complex than (7)–(10) can be easily derived in a similar way for the case of position-dependent sheet resistance along the well. Based on the above results, it is concluded that the developed model is capable of yielding design rules for locating the devices on the appropriate regime within the well, so that the induced potential drop due to an active emitter in the substrate is too small to cause the malfunction of the devices.

B. Steady-State Triggering Current

Several structures like those shown in Fig. 8 have been characterized with respect to the steady-state triggering current. This current is defined as the collector current of the lateral p-n-p transistor to initiate the latchup. The measured triggering current labeled $I_{c\|,\text{trg}}$ for each structure is listed in Table I where the corresponding structure parameters are also shown. Note that the structure labeled $C - 1$ in Table I has the guard ring in the well and has the largest triggering current among the illustrated structures. Based on the developed model, the corresponding

TABLE I
THE STRUCTURE PARAMETERS FOR FIG. 8 AND THE CALCULATED WELL RESISTANCES AND MEASURED STEADY-STATE TRIGGERING CURRENTS

Structure Notation	W_{p1}* (μm)	W_{p2}* (μm)	W_n (μm)	W_c (μm)	x** (μm)	R_w(ohm)+ cal.	R_w(ohm)++ cal.	$I_{c\parallel,trg}$(mA) exp.
A - 1	37	37	18	43	18	1526	1536	0.44
A - 2	37	37	9	43	9	2137	2147	0.28
A - 3	156	156	1	171	1	11113	11123	0.064
B - 1	1	1	18	43	23	108	118	4.0
B - 2	1	1	22	43	27	120	130	4.8
C - 1	1	37	18	43	18	33	39	10.6

*: $W_{p1}=W_{p2}$ represents the case shown in Fig. 8(a) and Fig. 8(b).

**: x denotes the position where the emitter edge locates and is used to calculate R_w.

+: The calculated result under $R_{ext}=0$.

++: The calculated result under $R_{ext}=10$ ohm.

well resistances have been calculated and are shown in Table I. To calculate the steady-state triggering current, the following expression has been used [3]:

$$I_{c\parallel,trg} = V_{BE\perp,on}/R_w \qquad (11)$$

where $V_{BE\perp,on}$ represents not only the induced potential drop in the well but also the turn-on voltage across the base–emitter junction of the vertical n-p-n transistor. The correlations between the measured triggering current and the inverse of the calculated R_w for each structure in Table I are established in Fig. 9. The calculated results using (11) are shown in Fig. 9 with $V_{BE\perp,on} = 0.5$ V. It can be seen from this figure that there is a maximum error of 20 percent between model result and experimental data for the structure labeled $C - 1$. This error may be due to 1) the assumed constant sheet resistance $\rho_\square$ when using (7)–(10), and 2) the fluctuations of the well sheet resistance of the fabricated devices. Usually the sheet resistance under the emitter in the well is greater than that elsewhere in the well. Moreover, according to Troutman and Hargrove [4], the insertion of an emitter in the substrate can drastically alter the substrate transfer resistance. Therefore, the application of (7)–(10) using a constant sheet resistance determined outside the emitter in the well may overestimate the triggering current as shown in Fig. 9 for the structure labeled $C - 1$. However, a constant sheet resistance determined under the emitter in the well may lead to the underestimation of the triggering current and in this respect the simple model may be useful for the worst case design. Nevertheless, it is very helpful to use the general expressions shown in this paper as long as the position-dependent well sheet resistance has been accurately determined. Note that the choice of $V_{BE\perp,on} = 0.5$ V in (11) is based on the fact that, as the emitter current of the vertical n-p-n transistor is negligibly small with re-

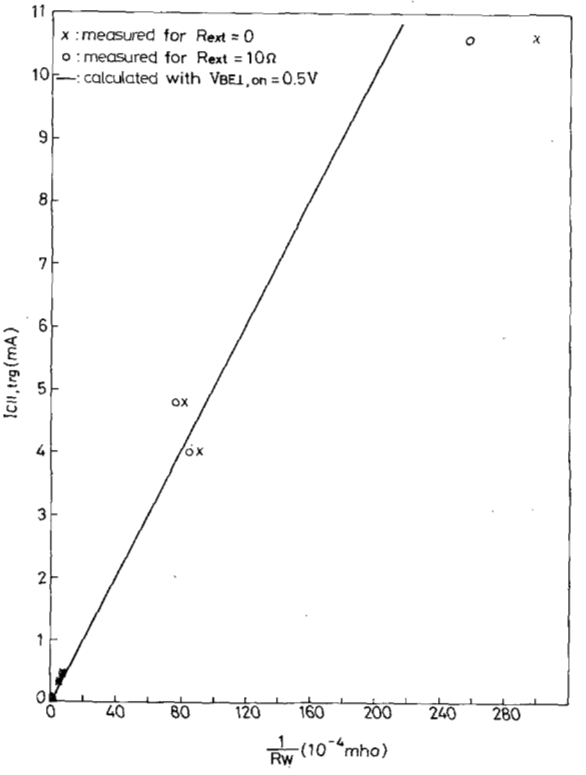

Fig. 9. The calculated and measured steady-state triggering currents $I_{c\parallel,trg}$ versus $1/R_w$ for the structures in Table I.

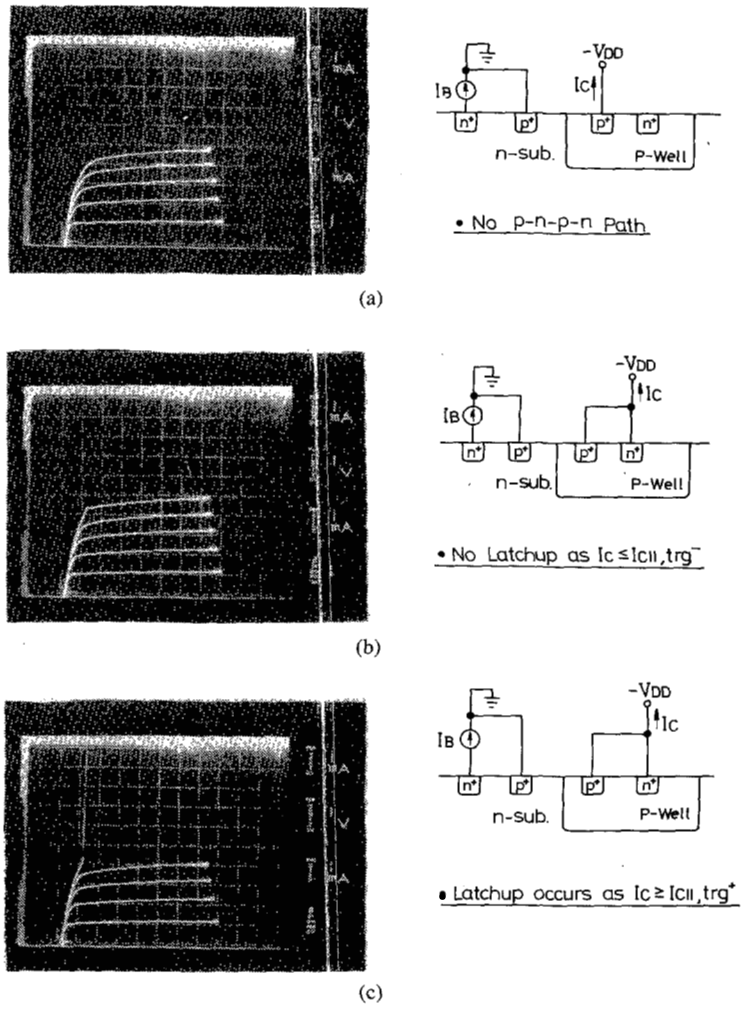

Fig. 10. The measured collector I–V characteristics of the lateral p-n-p transistor for the structure labeled B-2 with the absence of the vertical n-p-n transistor for (a) and with the presence of the vertical n-p-n transistor for (b) and (c).

spect to $I_{c\|,\mathrm{trg}}$, its base–emitter voltage is smaller than $V_{BE\perp,\mathrm{on}}$ of about 0.5 V. This is verified by Fig. 10, which shows the measured collector I–V characteristics of the lateral p-n-p transistor for the structure labeled $B-2$ with different terminal connections. Fig. 10(a) shows the operating regime of the independent lateral p-n-p transistor while Fig. 10(b) and 10(c) shows the behavior of the lateral transistor that is located in a complete p-n-p-n path. Fig. 10(b) is obtained for the collector current ranging between 0 and $I_{c\|,\mathrm{trg}}$ above which the latchup will occur. The curves in Fig. 10(b) are nearly identical to those in Fig. 10(a), irrespective of the connection of the n^+ emitter to the $-V_{DD}$ terminal. Now as a very small current is added to the original base current of Fig. 10(b) in order to make the uppermost curve slightly approach a critical value of $I_{c\|,\mathrm{trg}}$, latchup occurs as shown in Fig. 10(c). Note that the curves in Fig. 10(a) and (b) are nearly identical to those in Fig. 10(c) for a collector current less than $I_{c\|,\mathrm{trg}}$ since the corresponding base currents are nearly identical between Fig. 10(a), (b), and (c). Therefore, the accuracy of the proposed model has been confirmed despite of its simplicity.

Finally, a fabricated structure like Fig. 8(b) with $W_p = 156\ \mu\mathrm{m}$, $W_n = 165\ \mu\mathrm{m}$, and $W_c = 171\ \mu\mathrm{m}$ is used to illustrate the application of the model and to establish design rules that provide normal operation for the devices in the well under the action of an emitter in the substrate. The well resistance for this structure has been calculated to be 14.4 Ω for $R_{\mathrm{ext}} = 10\ \Omega$; as a result, the collector current of the lateral p-n-p transistor to trigger the latchup is 35 mA using (11) with $V_{BE\perp,\mathrm{on}} = 0.5$ V. Therefore, the corresponding emitter current of the lateral p-n-p transistor is greater than 3.5 A since the common-emitter current gain of the lateral p-n-p transistor has been empirically estimated to be less than 0.01 (see Fig. 11). Such a large current may damage the devices prior to latchup. It has been verified experimentally that this structure is free from latchup due to the strong forward-biased emitter in the substrate, as shown in Fig. 11. In addition, this structure has been experimentally found to burn out as the emitter current of the lateral p-n-p transistor exceeds about 200 mA. Note that to preclude the latchup under the action of an emitter in the substrate, a large value of W_p is required for the bulk structure in Fig. 8(b) while this value may be

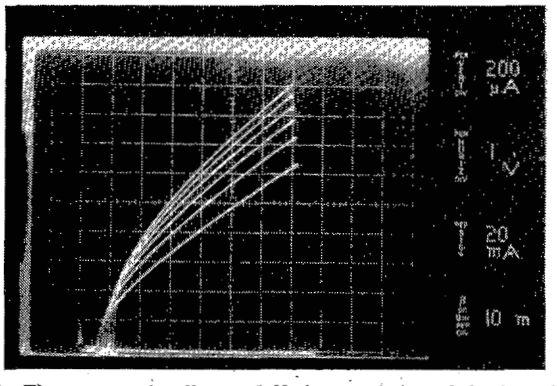

Fig. 11. The measured collector I–V characteristics of the lateral p-n-p transistor with the presence of the vertical n-p-n transistor for the structure in Fig. 8(b) with $W_p = 156\ \mu m$, $W_n = 165\ \mu m$, and $W_c = 171\ \mu m$. No latchup is observed.

significantly reduced for the same structure based on the epi wafer. This can be seen from Fig. 3 that the current density $J_\perp(x)$ across the bottom side of well–substrate junction is greatly suppressed for the epi case.

IV. Conclusion

A new structure-oriented model has been presented to calculate the resistance potential drop in the well of CMOS structures due to the action of an emitter in the substrate. In a step-by-step manner, the simulated results using the developed model for various structures have been found to be in good agreement with the experimental data of the induced potential drop in the well and the steady-state triggering current for latchup. Moreover, the model is capable of yielding design rules in order to prevent the devices in the well from being disturbed by an active emitter in the substrate.

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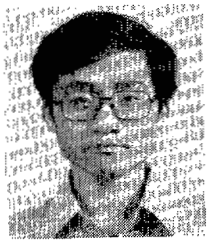

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