Chapter 4 Experimental Results

The measurement of the fabricated IP is presented in this chapter. It is presented in Section 4.1 that the testing equipment sets up with designed printed circuit board (PCB) and taped-out chip. The implementation of the custom-design PCB is shown in Section 4.2. The testing results of TMU and MLC are shown in Section 4.3. After the functionality of TMU worked, the testing results of TAPM are shown in Section 4.4. The experimental results of taped-out chip are summarized in Section 4.5.

4.1 Measurement Environment

The environment of measurement is shown in this section. The explicit measurement set-up is presented in Figure 4.1.1. The two equipments, test pattern generator and logic analyzer, are essential for testing taped-out chip. In the previous chapter, the parallel-to-serial interfaces connect with 8-bit parallel input of temperature sensors in TMU. Thus, the serial input is required for sensors. As the shadow blocks of this figure indicates, the test pattern generator instead of a variety of sensors is adopted to drive TMU because there are not serial input sensors in the electronic market. At measurement stage, thermal models of SoC design in reality are not temporarily considered, and a simple algorithm can be chosen to program TMU. There are three testing path in this figure; One, as the thin-line arrow shows, the test patterns are driven into TMU from the master interface ; another, as dotted-line arrow shows, test patterns are driven into TMU from the slave interface; the other, as

broken-line arrow shows, test patterns are directly driven into TMU. According to selection of testing path, the output signals of TMU are observed by logic analyzer. Agilent 1692A Logic Analyzer is used to sample digital signals and Acute PG2050 is used to generate specific test patterns. The actual situation of measurement is shown in Figure 4.2.2.

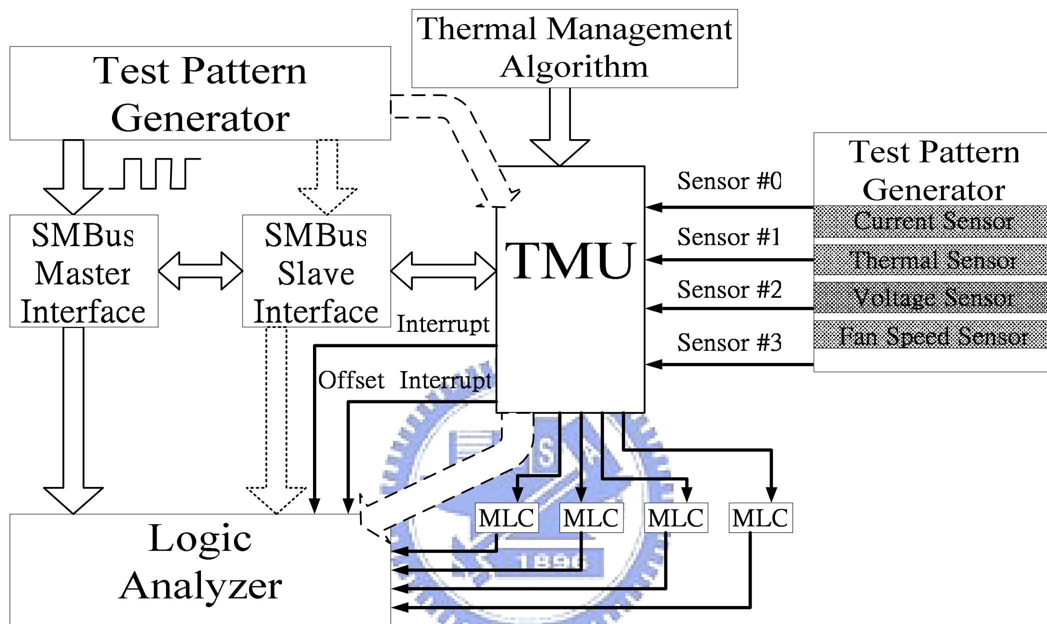


Figure 4.1.1 Testing Set-Up

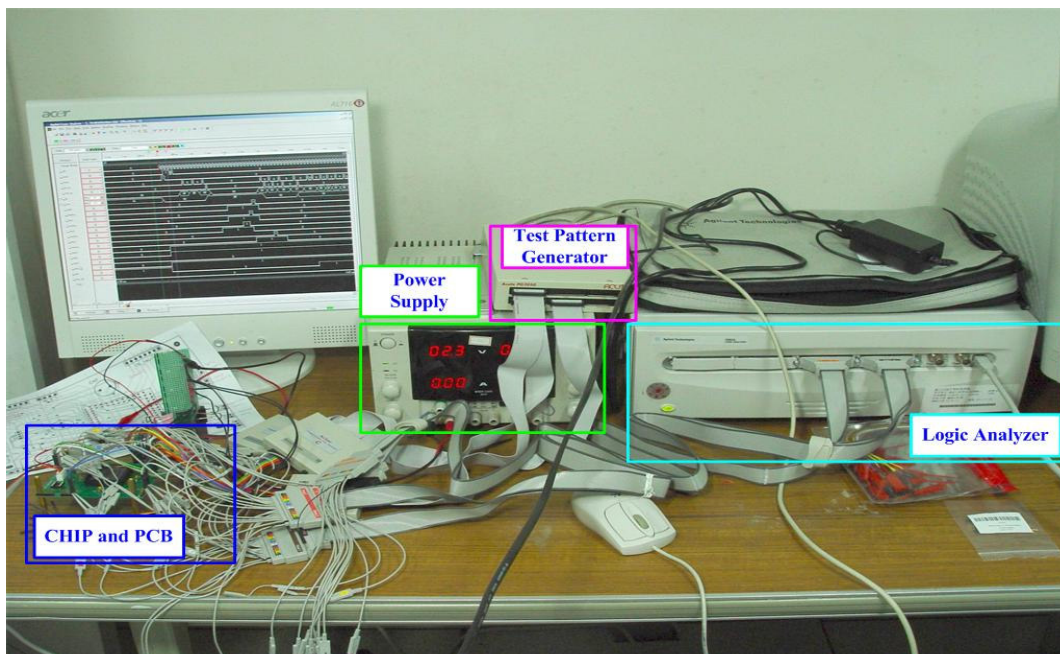


Figure 4.1.2 Photograph of Testing Environment

4.2 Printed Circuit Board Design

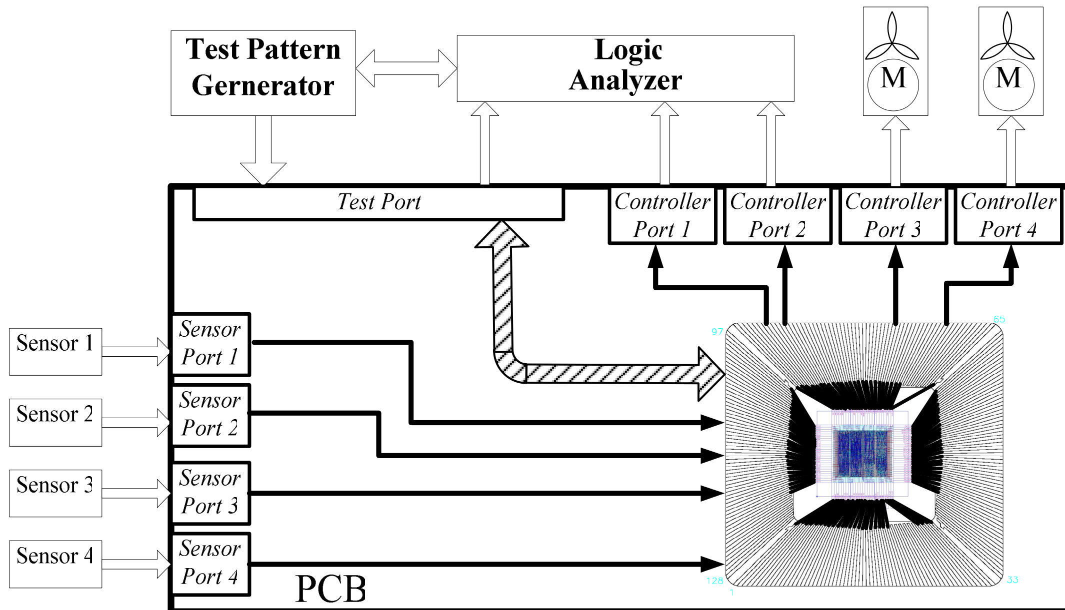
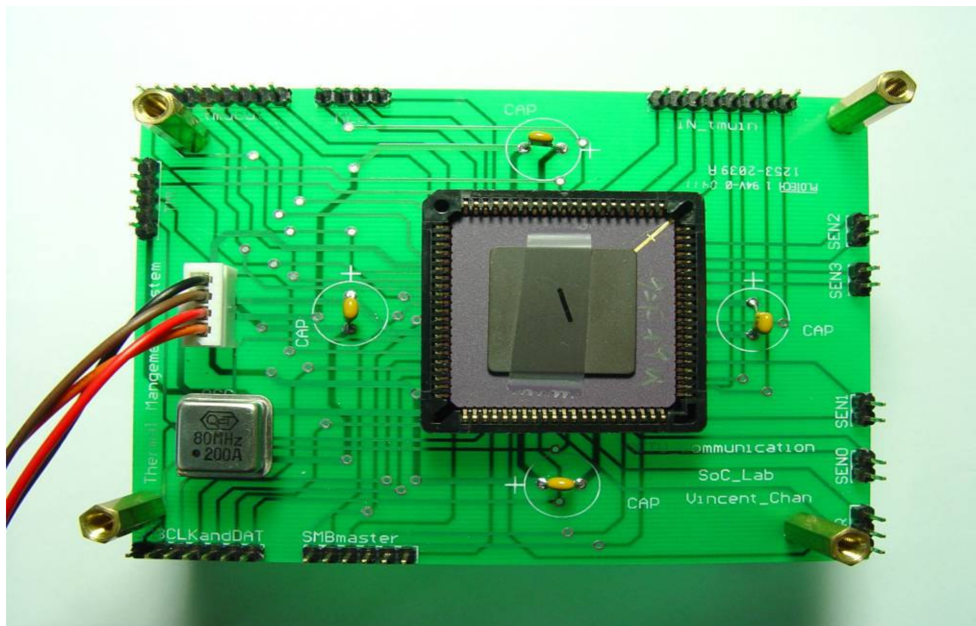


Figure 4.2.1 PCB Circuit Implementation

PCB circuit design issues are proposed in this section. In Figure 4.2.1, a full-custom PCB is implemented in order to test taped-out chip. This PCB design should take account of operating frequency and power supply for this chip on a board. Thus, some capacitors are placed on power line to regulate voltages, and clock line as well as power line is thickened to avoid crosstalk phenomenon. Protel 99SE is used to implement two-layer board, which is followed by fabricated in specialized PCB manufacturer. In Copper Clad Laminate (CCL), FR-4 clad laminate is popularly applied in the implementations of computer components and peripheral components, such as hard disk and main-board, so it is used to be the material of this board. The thickness of this board is 20 mil (1mil = 0.04mm), and tin material is used to implement circuit lines. This PCB can provide a mature testing platform for taped-out chip. The PCB floorplanning and subcomponents are diagrammatically shown in Figure 4.2.2.



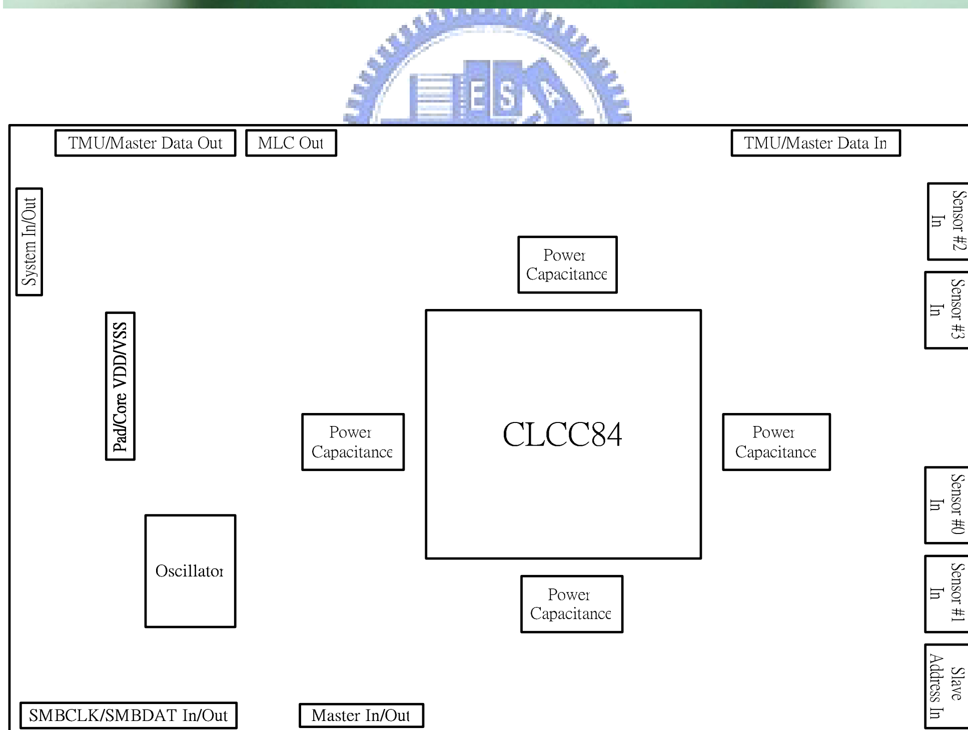


Figure 4.2.2 Photograph of Taped-out Chip on PCB

4.3 Testing Results of Thermal Management Unit

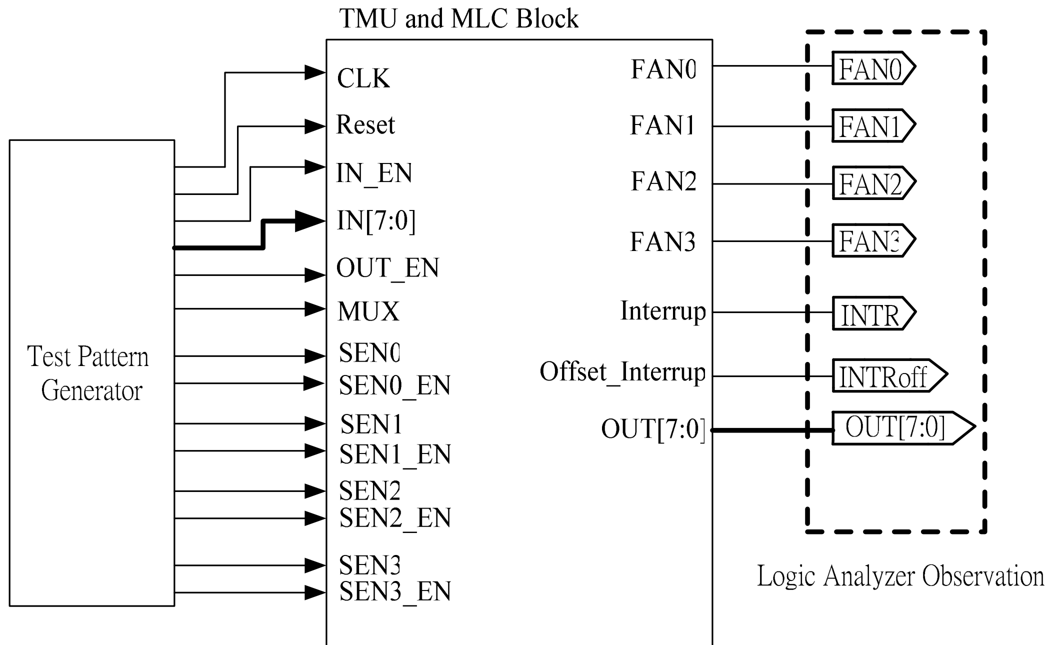


Figure 4.3.1 Testing TMU & MLC Block

The testing results of the TMU and MLC are shown in this section. In Figure 4.3.1, the blocks diagram of testing TMU and MLC is presented, which is indicated what I/O ports of TMU and MLC block are driven by test pattern generator and observed by logic analyzer. These I/O ports are described in Table 3.4.1 and Table 3.4.2 in previous chapter. The four kinds of test patterns, 00h, 55h, AAh and FFh, must be read from and written into specified registers of TMU in order to ensure that these programmable registers are able to normally store data. The sampling digital waveforms by logic analyzer are shown in next pages. As these digital waveforms indicate, when the reset is accessed, the states of TMU are initialized. The input “mux” is assigned low status “0” in order to test TMU block.

In Figure 4.3.2~6, after the four test patterns are stored in controller registers, the assigned value is read from the specified registers. In Figure 4.3.7~10, the four test

patterns is serially written into the temperature registers and any four different test patterns among sensors are written into temperature registers in Figure 4.3.11. After assigned value is stored in temperature register, we read from them.

In Figure 4.3.12~15, the test patterns of (offset) high threshold registers are the same as (offset) low threshold registers. The four patterns are assigned into the (offset) threshold registers. In Figure 4.3.16, the different test patterns are assigned into the (offset) high threshold and low threshold register. Similarly, after each of test patterns stored, the assigned value is read from (offset) high/low threshold registers.

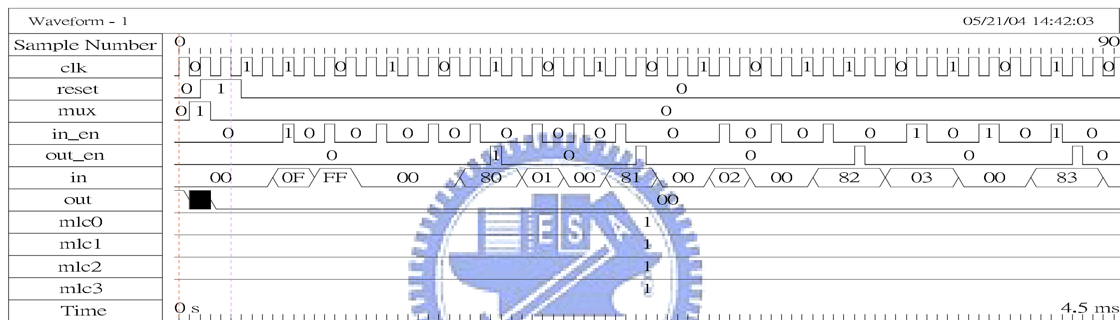


Figure 4.3.2 Testing Controller Registers by 00h Pattern

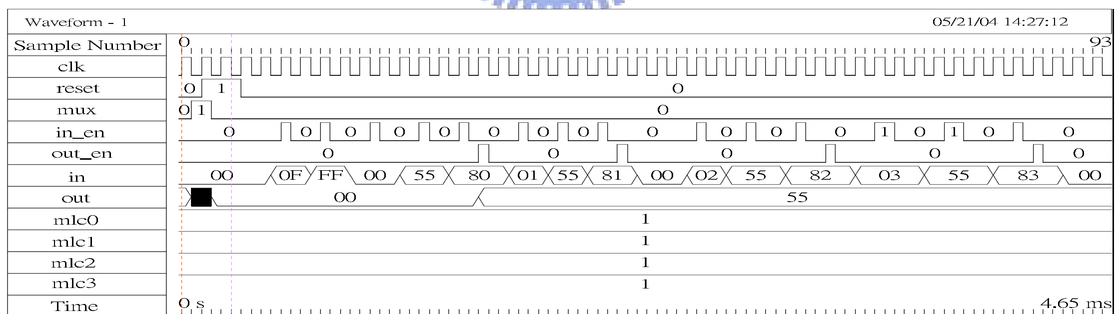


Figure 4.3.3 Testing Controller Registers by 55h Pattern

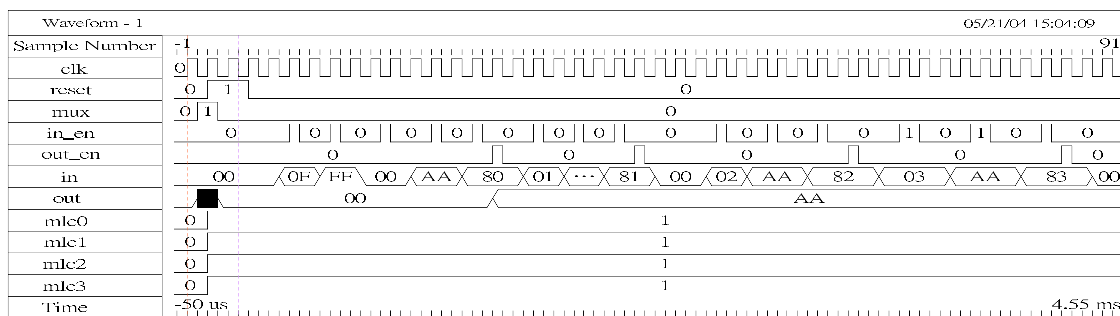


Figure 4.3.4 Testing Controller Registers by AAh Pattern

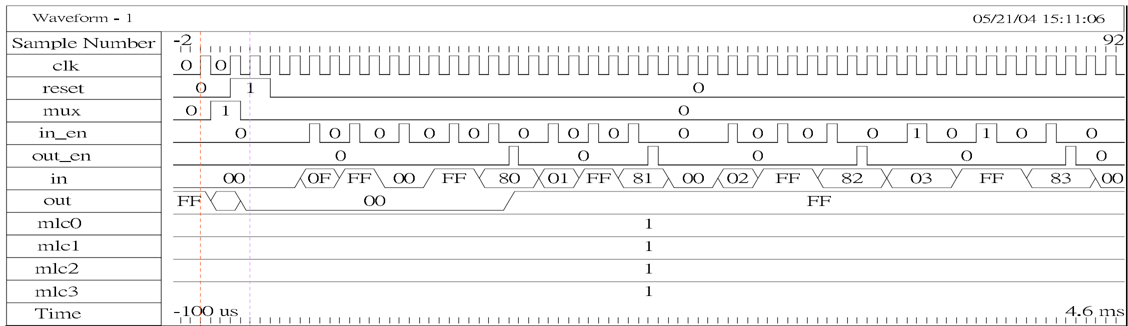


Figure 4.3.5 Testing Controller Registers by FFh Pattern

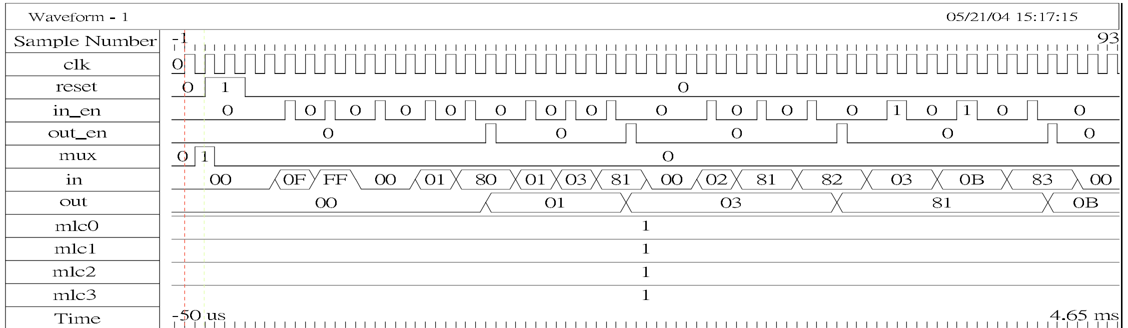


Figure 4.3.6 Testing Controller Registers by Different Patterns

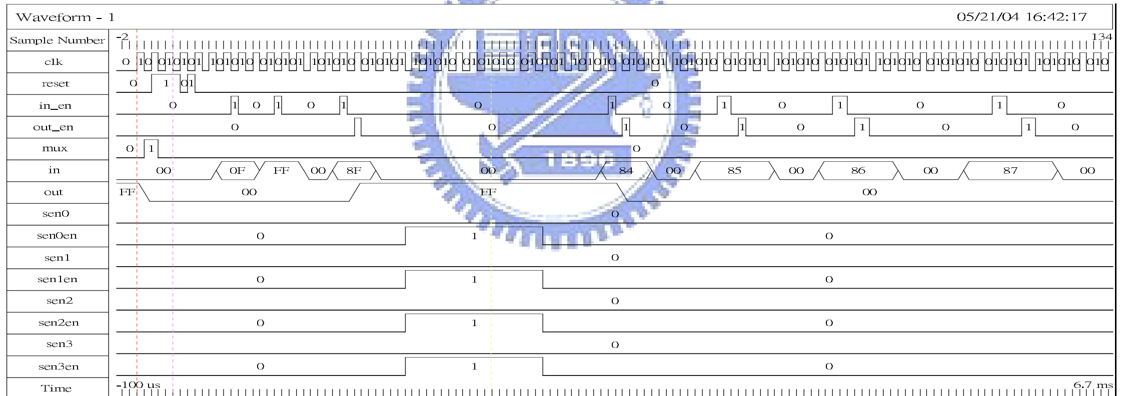


Figure 4.3.7 Testing Temperature Registers by 00h Pattern

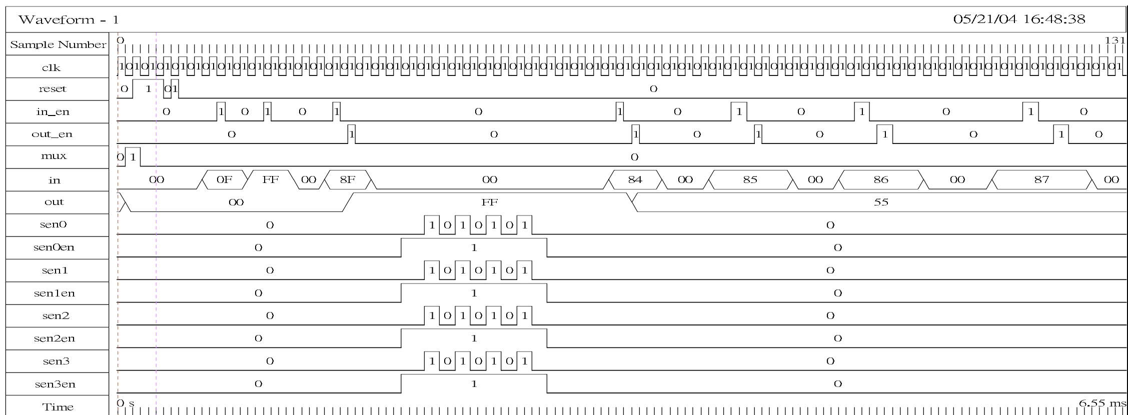


Figure 4.3.8 Testing Temperature Registers by 55h Pattern

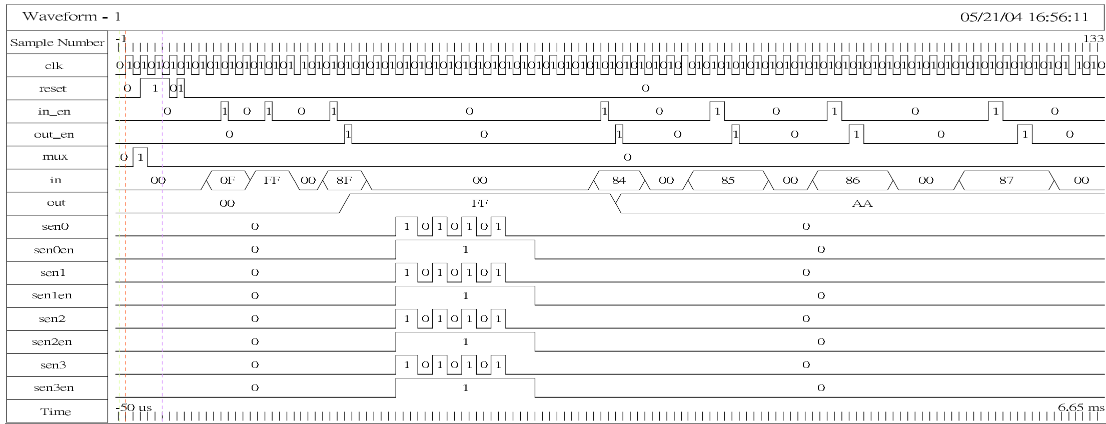


Figure 4.3.9 Testing Temperature Registers by AAh Pattern

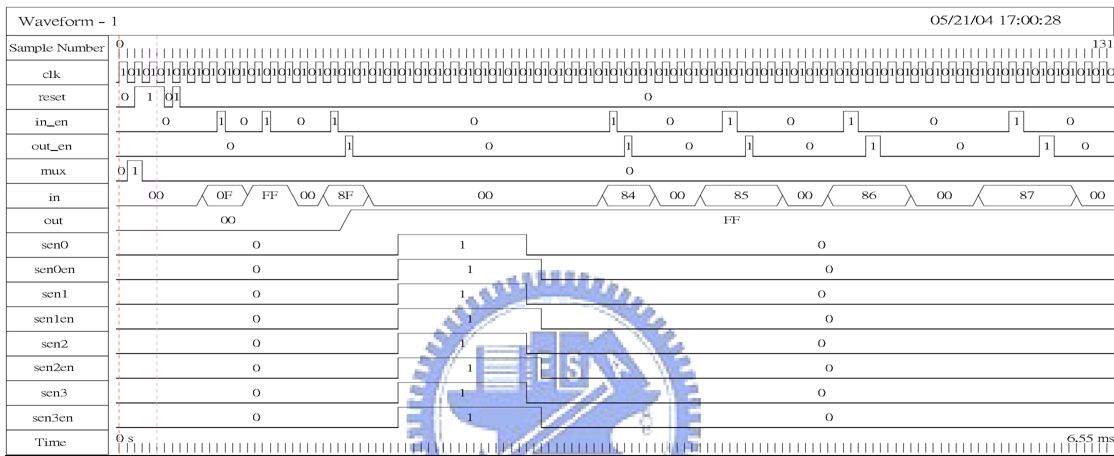


Figure 4.3.10 Testing Temperature Registers by FFh Pattern

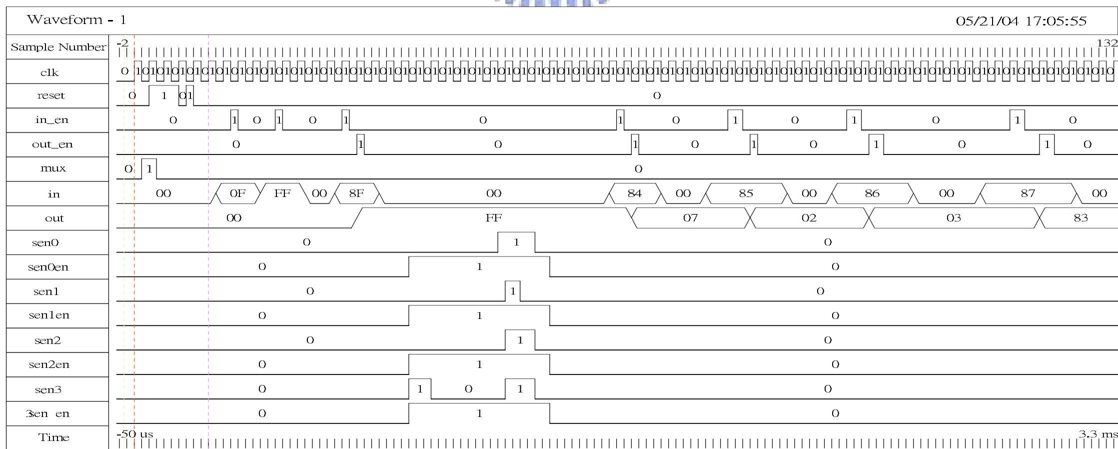


Figure 4.3.11 Testing Temperature Registers by Different Patterns

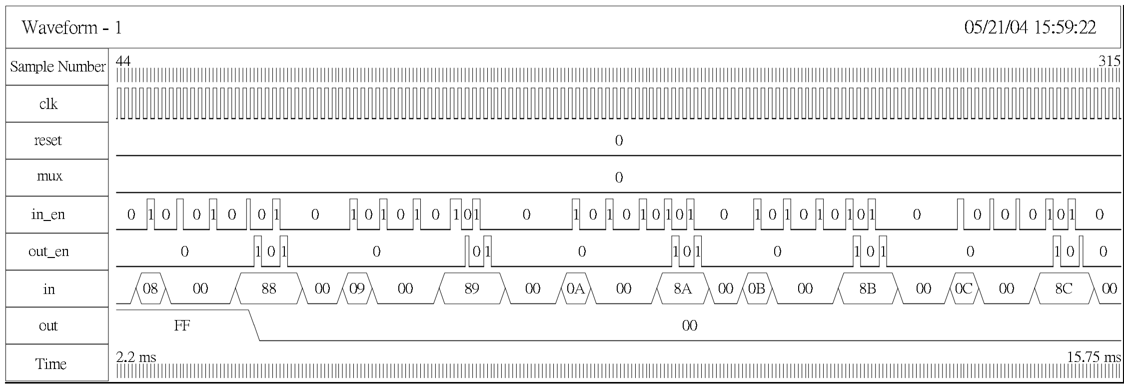


Figure 4.3.12 Testing (Offset) Threshold Registers by 00h Pattern

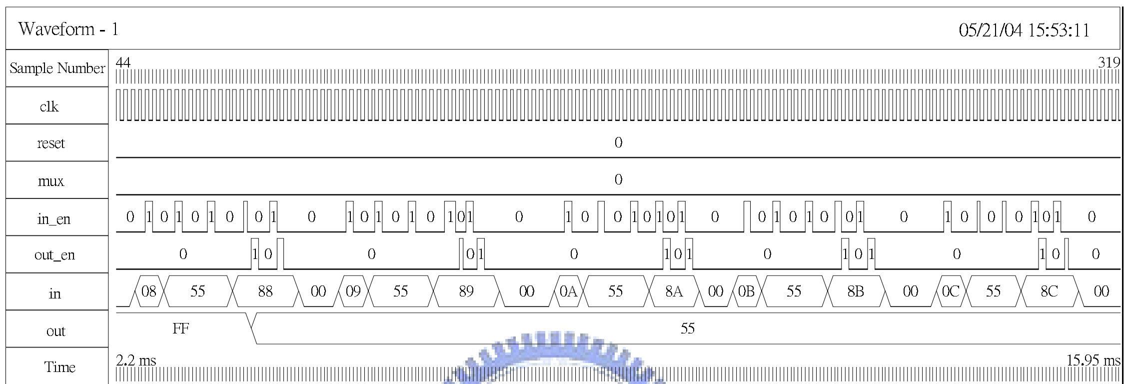


Figure 4.3.13 Testing (Offset) Threshold Registers by 55h Pattern

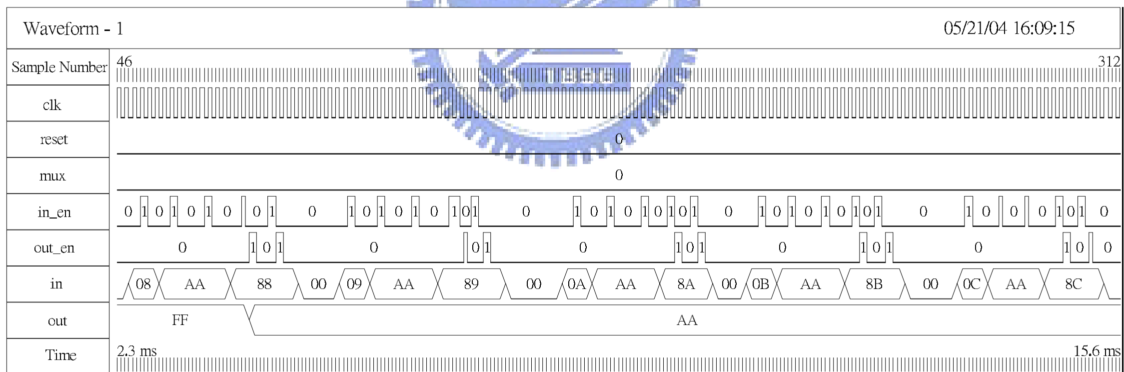


Figure 4.3.14 Testing (Offset) Threshold Registers by AAh Pattern

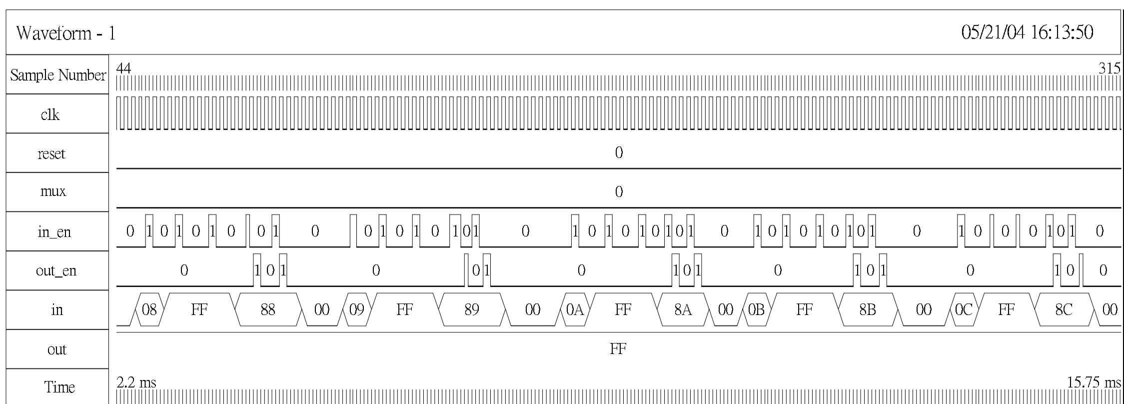


Figure 4.3.15 Testing (Offset) Threshold Registers by FFh Pattern

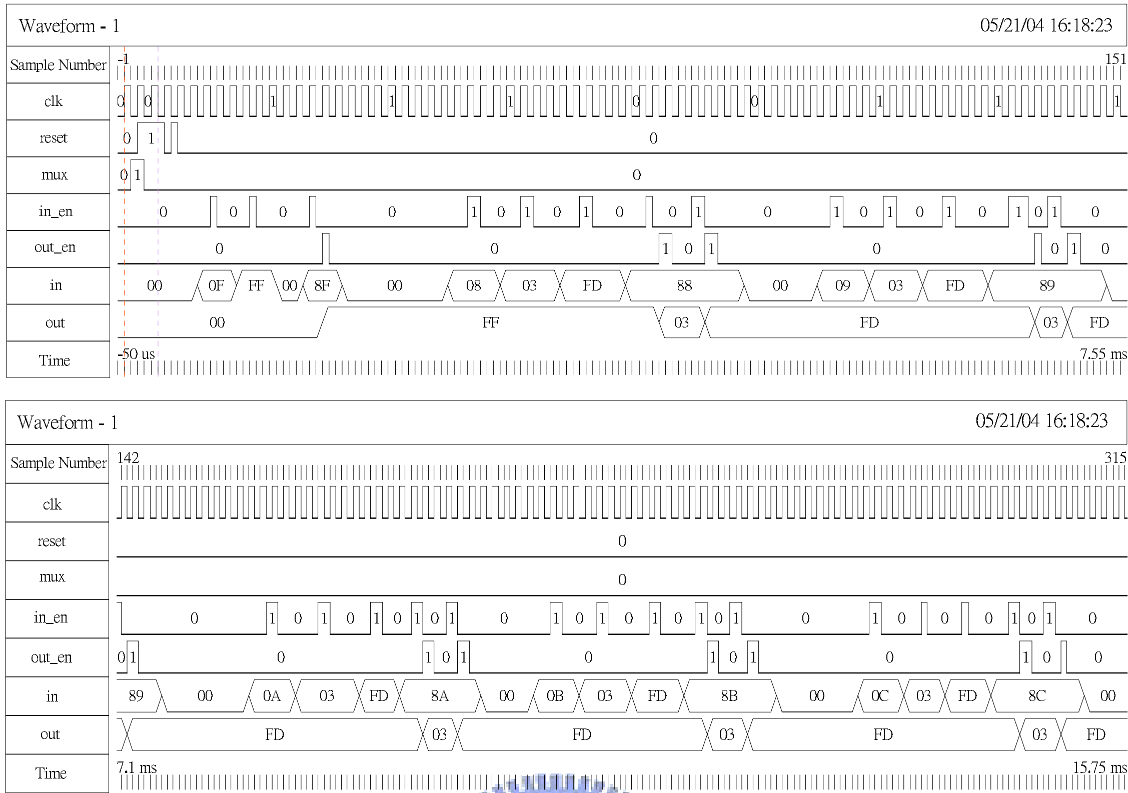


Figure 4.3.16 Testing (Offset) High/Low Threshold Registers by Different Patterns

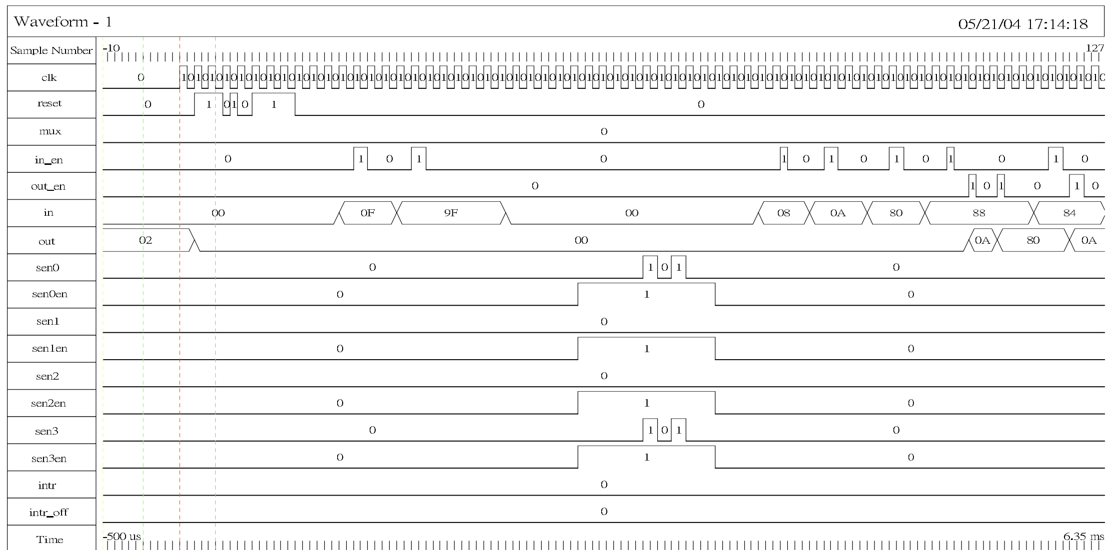
In Figure 4.3.17, sensor0 and sensor3 are adopted to test interrupt generator in order to ensure that interrupt and offset interrupt are trigger when local overheating (the local overheating of sensor0 or sensor3) or offset overheating (the offset overheating of sensor0 and sensor3) happened. The detailed testing result is described as following paragraphs:

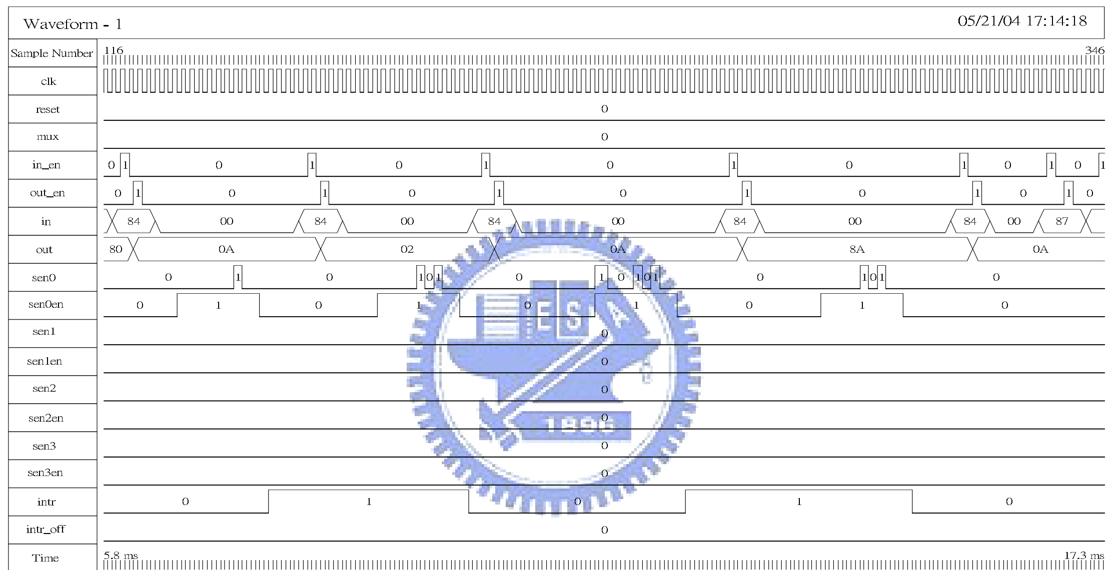
When reset is accessed at the sample number 2, the states of TMU are initialized. From the sample number 22 to 43, the configuration of TMU is set in order to use two sensors, the sensor0 and sensor3. The input "sen0en~sen3en" is accessed 9 cycle; the first 8 cycle is serial input 8bits, and the serial-to-parallel interface transmits 8bits data into temperature registers of TMU at the final cycle. From the sample number 54 to 74, the serial-to-parallel interface of sensor0 and sensor3 are serial input "0Ah", and

the others of sensor1 and sensor2 are serial input “00h” since the sensor1 and sensor2 is not used.

From the sample number 80 to 102, the high threshold of sensor 0, “80h”, and low threshold of sensor 0, “0A”, are set by input “in”, and the assigned value is read from threshold register 0 at the sample number 108 and 113. At the sample number 123, the temperature of sensor0, “0Ah”, is read from the temperature register 0. After sensor0 serially changed from the sample number 132 to 151, the interrupt is accessed at the sample number 154 due to local underflow, and its changed temperature read from the temperature register 0 at the sample number 166. The sensor0 serially changes again at the sample number 179, which is within specified temperature. Thus, the interrupt signal ends at the sample number 199, and the changed temperature is read from temperature register 0 at the sample number 206. The sensor0 thirdly serially changes at the sample number 228, the interrupt is accessed again at the sample number 250 due to local overflow, and the changed temperature is read from temperature register 0 at the sample number 262. The sensor0 fourthly serially changes from the sample number 281 to 302, the interrupt ends at the sample number 302 since the temperature of senor0 is no longer local overheating, and its changed temperature is read from temperature register 0 at the sample number 316. At the sample number 337, the temperature of sensor 3, “0Ah”, is read from the temperature register 3.

The offset high/low threshold is set from the sample number 342 to 359. The temperature of sensor 3, ”02h”, is serially changed from sample number 362 to 382; the offset interrupt is accessed at the sample number 384 due to offset overflow and underflow of sensor0 and sensor3. The sensor3 serially changed again from the sample number 406 to 425, the offset interrupt ends at the sample number 427 since the temperature of senor0 and sensor3 are no longer offset overheating.





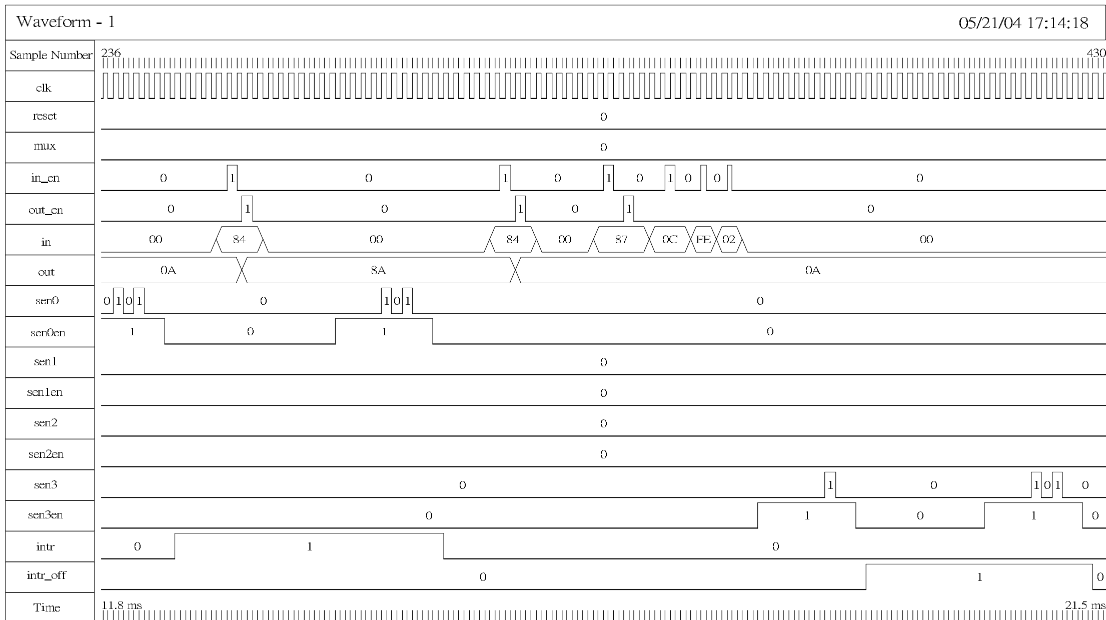


Figure 4.3.17 Testing Interrupt and Offset Interrupt Functions

4.4 Testing Results of Thermal-Aware Power Management Systems

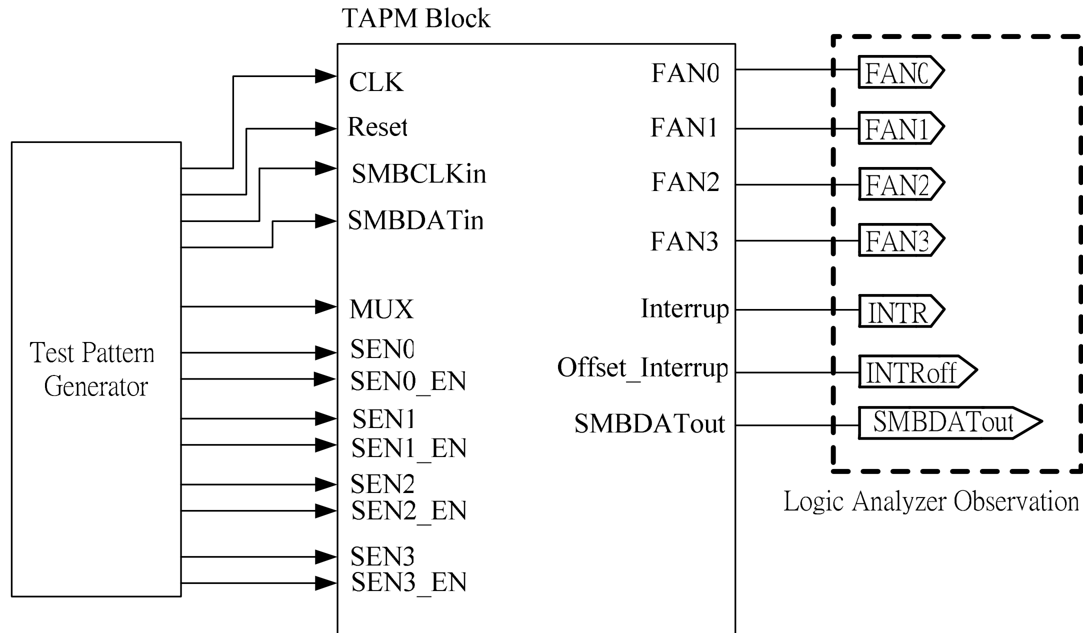


Figure 4.4.1 Testing TAPM Block

The testing results of the TAPM are shown in this section. In Figure 4.4.1, the blocks diagram of testing TAPM is presented, which is indicated what I/O ports of TAPM block are driven by test pattern generator and observed by logic analyzer. The signal description of these I/O ports is presented in Table 3.4.4. The output “SMBDATout”, input “SMBCLKin” and “SMBDATin” are the I/O ports of SMBus. This testing focuses that test patterns are transmitted into and assigned value received from TMU by SMBus.

In Figure 4.4.2, the test pattern is stored in the controller register 0 by the write byte protocol of SMBus from the sample number 3052 to 3396, and the assigned value is read from the controller register 0 by read byte protocol of SMBus from the sample number 3496 to 3956. The testing results of other controller registers and the (offset) threshold registers are shown in Figure 4.4.3~5 and Figure 4.4.6~10,

respectively. Their expositions are presented in Table 4.4.1, which are same as the explanations of Figure 4.4.2 above.

In Figure 4.4.11, before the sample number of 193485, the system configuration is set. From the sample number of 196931 to 196950, the temperature of sensor0 and sensor3 serially change. From the sample number of 210627 to 303199 and 320342 to 412913, the temperature register 0 and temperature register 3 is read by read byte protocol of SMBus. Similarly, in Figure 4.4.12, testing manner of sensor1 and sensor2 is the same as sensor0 and sensor3.

In Figure 4.4.13, the testing results of system integration is the same as the simulation in Figure 3.3.6. The description of this figure can refer to the explanation of Figure 3.3.6. The Zoom in the sensors changed in Figure 4.4.13 is shown in Figure 4.4.14~16.

Table 4.4.1 Expositions for Figure 4.4.2~10

	Write Protocol Range	**Read Protocol Range**	**Register Name**
Figure 4.4.2	3052 to 3396 *write byte protocol*	3496 to 3956 *read byte protocol*	Controller Register 0
Figure 4.4.3	2848 to 3192 *write byte protocol*	3291 to 3752 *read byte protocol*	Controller Register 1
Figure 4.4.4	3598 to 3942 *write byte protocol*	4042 to 4503 *read byte protocol*	Controller Register 2
Figure 4.4.5	3050 to 3392 *write byte protocol*	3494 to 3953 *read byte protocol*	Controller Register 3
Figure 4.4.6	3249 to 3699 *write word protocol*	3772 to 4359 *read byte protocol*	Threshold Register 0
Figure 4.4.7	2842 to 3296 *write word protocol*	3368 to 3959 *read byte protocol*	Threshold Register 1
Figure 4.4.8	2844 to 3293 *write word protocol*	3365 to 3955 *read byte protocol*	Threshold Register 2
Figure 4.4.9	2844 to 3295 *write word protocol*	3367 to 3955 *read byte protocol*	Threshold Register 3
Figure 4.4.10	2615 to 3067 *write word protocol*	3138 to 3728 *read byte protocol*	Offset Threshold Register

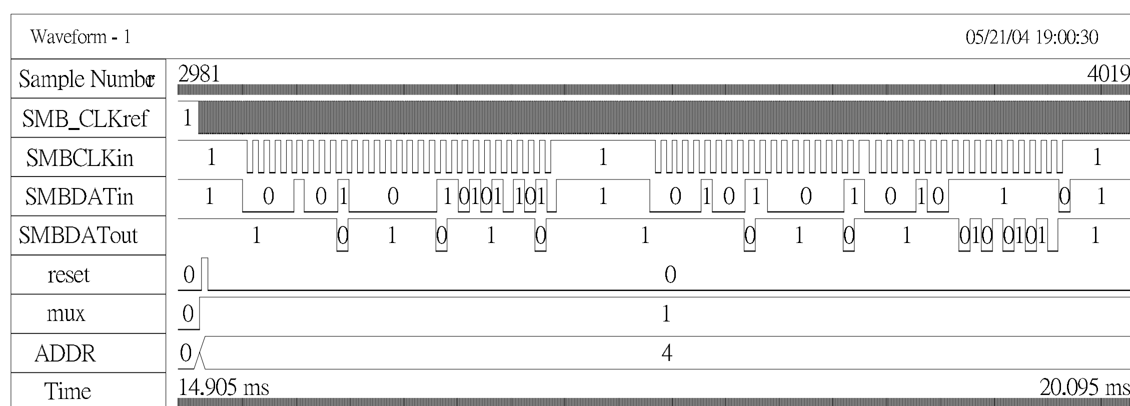


Figure 4.4.2 Testing Controller Register 0 by SMBus (Test Pattern AAh)

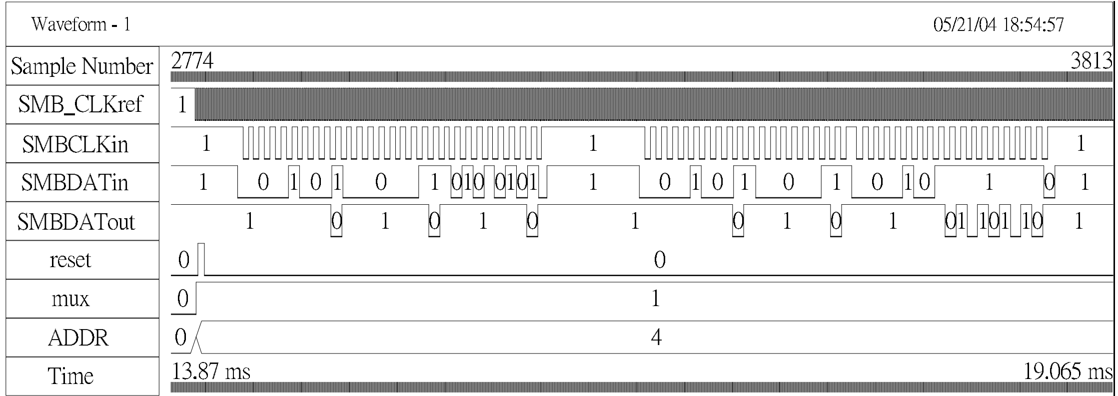


Figure 4.4.3 Testing Controller Register 1 by SMBus (Test Pattern AAh)

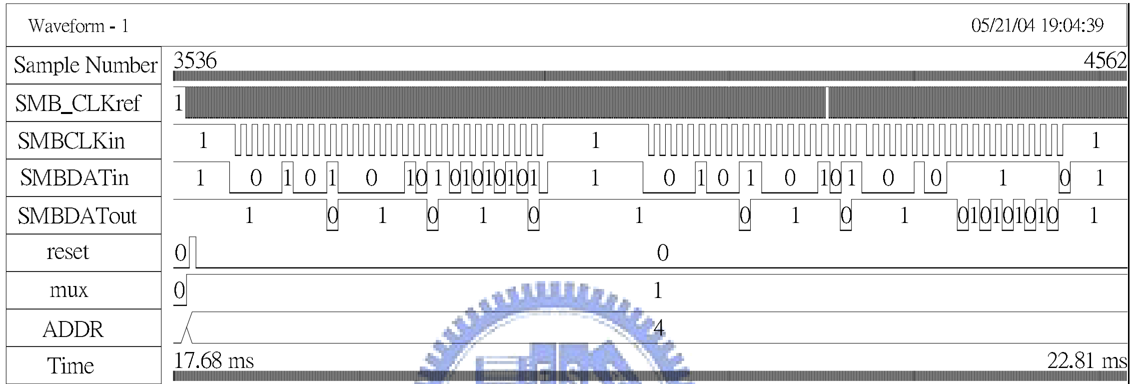


Figure 4.4.4 Testing Controller Register 2 by SMBus (Test Pattern AAh)

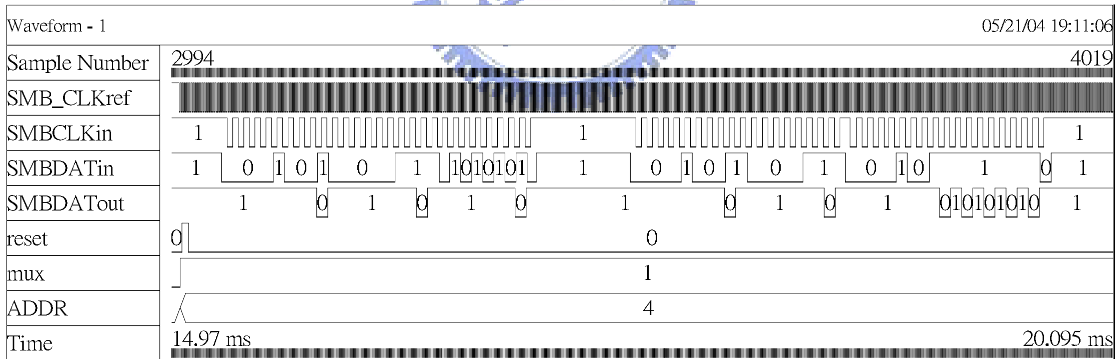


Figure 4.4.5 Testing Controller Register 3 by SMBus (Test Pattern AAh)

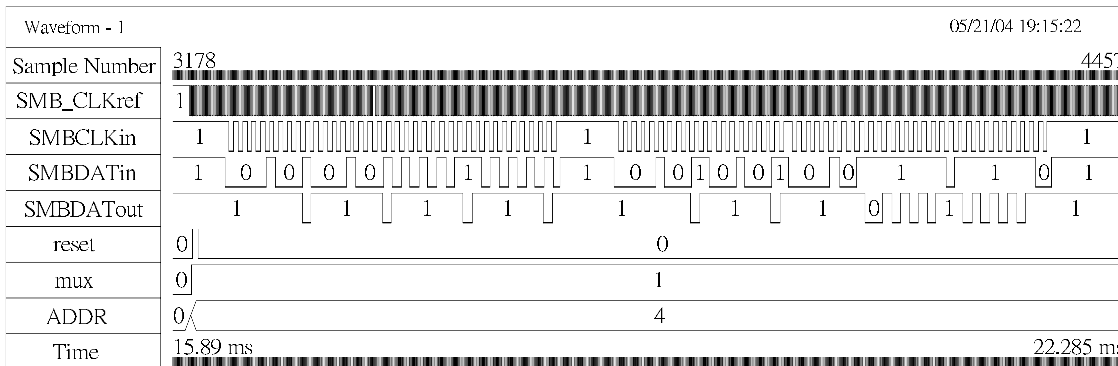


Figure 4.4.6 Testing Threshold Register 0 by SMBus (Test Pattern 55h & AAh)

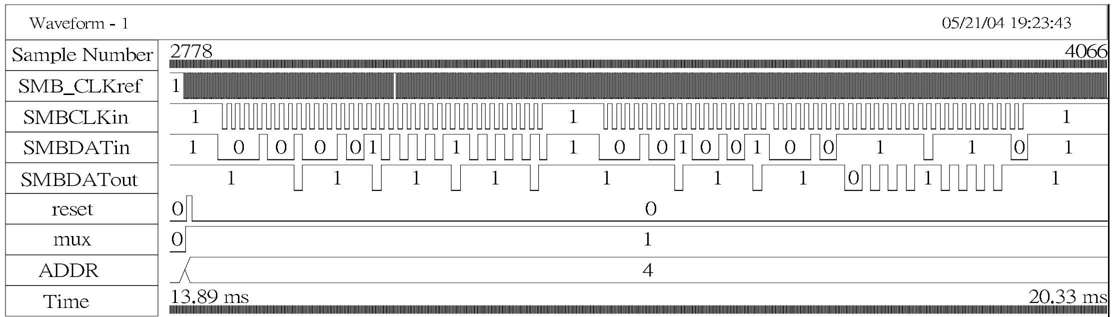


Figure 4.4.7 Testing Threshold Register 1 by SMBus (Test Pattern 55h & AAh)

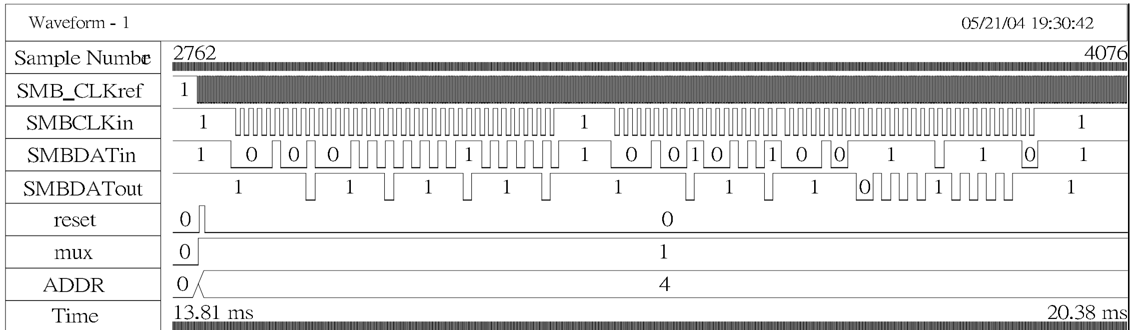


Figure 4.4.8 Testing Threshold Register 2 by SMBus (Test Pattern 55h & AAh)

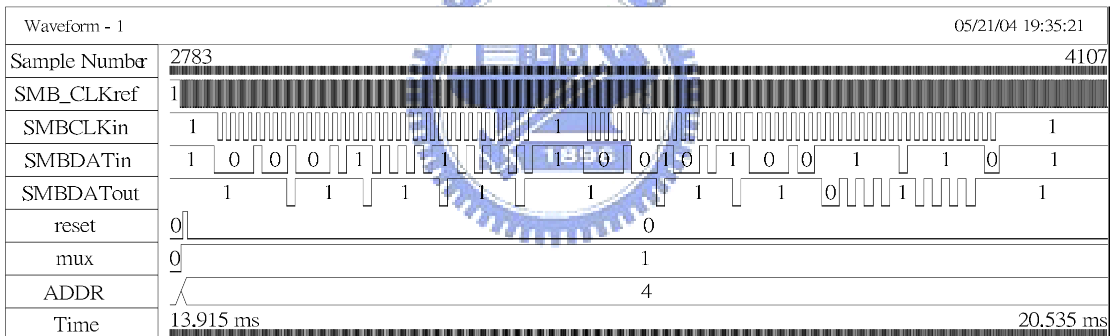


Figure 4.4.9 Testing Threshold Register 3 by SMBus (Test Pattern 55h & AAh)

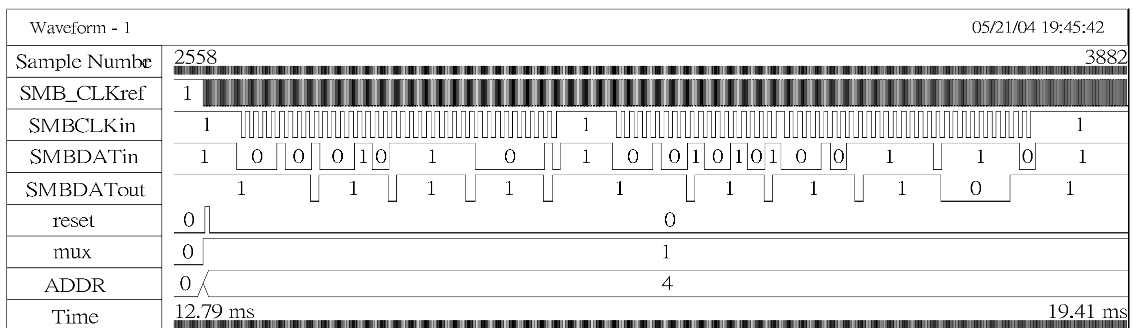


Figure 4.4.10 Testing Offset Threshold Register by SMBus (Test Pattern 55h & AAh)

Figure 4.4.11 Testing Temperature Register 0/3 by SMBus (Test Pattern 80h/FFh)

Figure 4.4.12 Testing Temperature Register 1/2 by SMBus (Test Pattern C0h/D5h)

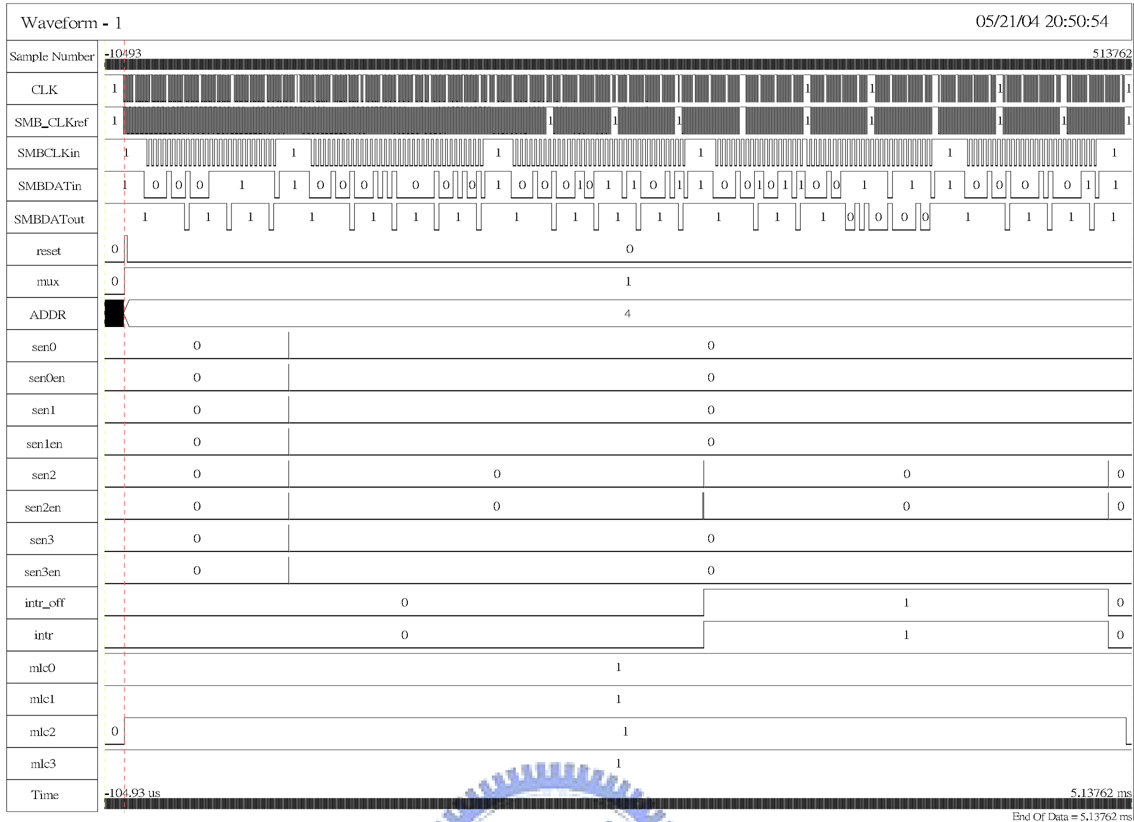


Figure 4.4.13 Testing Interrupt and Offset Interrupt by SMBus

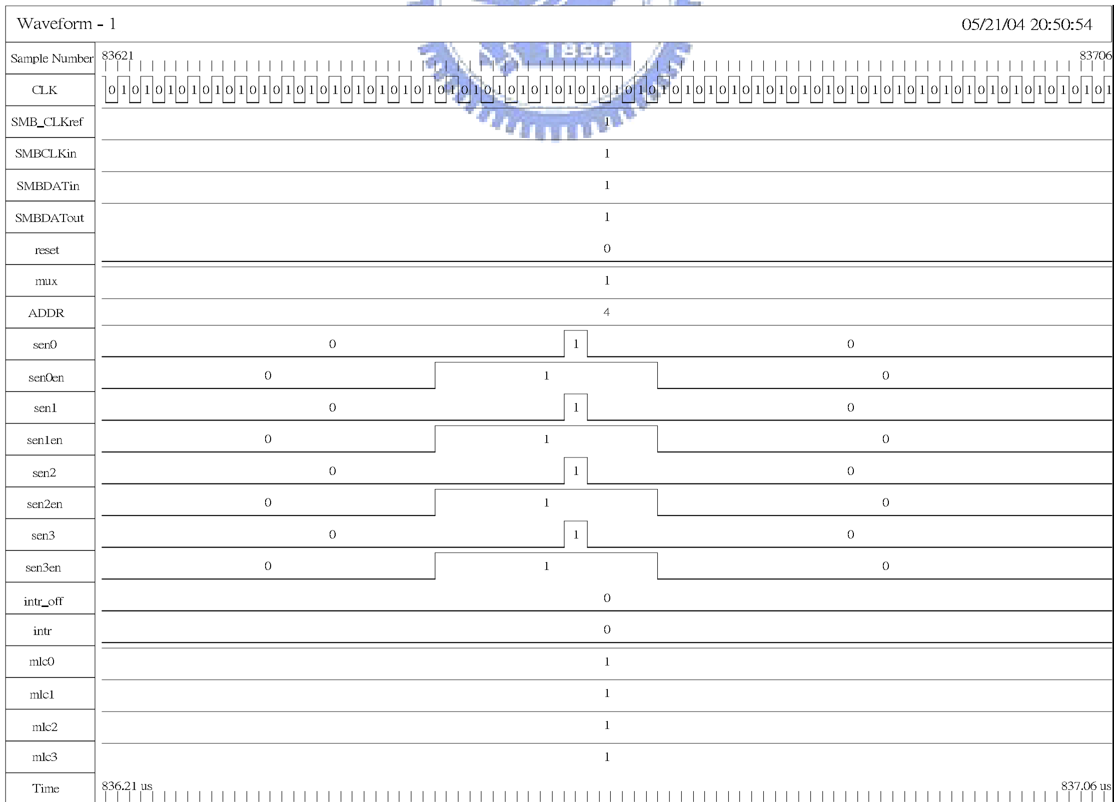


Figure 4.4.14 Zoom in Sensors Firstly Change in Figure 4.4.13

Figure 4.4.15 Zoom in Sensors Secondly Change in Figure 4.4.13

Figure 4.4.16 Zoom in Sensors Thirdly Change in Figure 4.4.13

4.5 Summary

The proposed designs are summarized in this section. The die microphotograph and the region of standard cell for this taped-out chip are shown in Figure 4.5.1. The actual performance of TAPM is presented in Table 4.5.1 based on testing results. For these testing data, we discuss as following viewpoints:

Firstly, the highest operating frequency of whole system simulation is more than actual operation. In measurements, the test pattern generator only provides highest operating frequency as 50M Hz, so oscillators are adopted to provide clock for whole system in order to testing TAPM over this frequency. Two kinds of oscillator, 100MHz and 80 MHz, are ever used to testing with taped-out chip. For 100M Hz, the slave interface replies not acknowledge (NACK) pulses to master interface, so it is critical block for 100MHz operating frequency to make whole system break down. Another 80M Hz, whole system can normally work. For the operating frequency between 80M Hz and 100M Hz, the general oscillators are incapable of providing, so whole system cannot test in these ranges. Thus, this chip operation frequency is possible over the 80Mz

Secondly, the master interface is implemented by Finite State Machine (FSM). For testing master interface in taped-out chip, FSM always stay in the IDLE state due to state machine unsteady. The second-generation TAPM is modified for these unsteady states.

The behaviors of TAPM, including chip areas, operation frequency and power consumption, are matched expectable ranges. For design and implementation of TAPM are concluded in next chapter.

Table 4.5.1 Actual System Perfromance

Thermal Management Unit Operating Frequency	80M Hz
SMBus Operating Frequency	400K Hz
SMBus Data Transaction Frequency	66.6K Hz
Multi-level Controller Operating Frequency	8K Hz
Power Consumption	15m W (Current about 6m A)

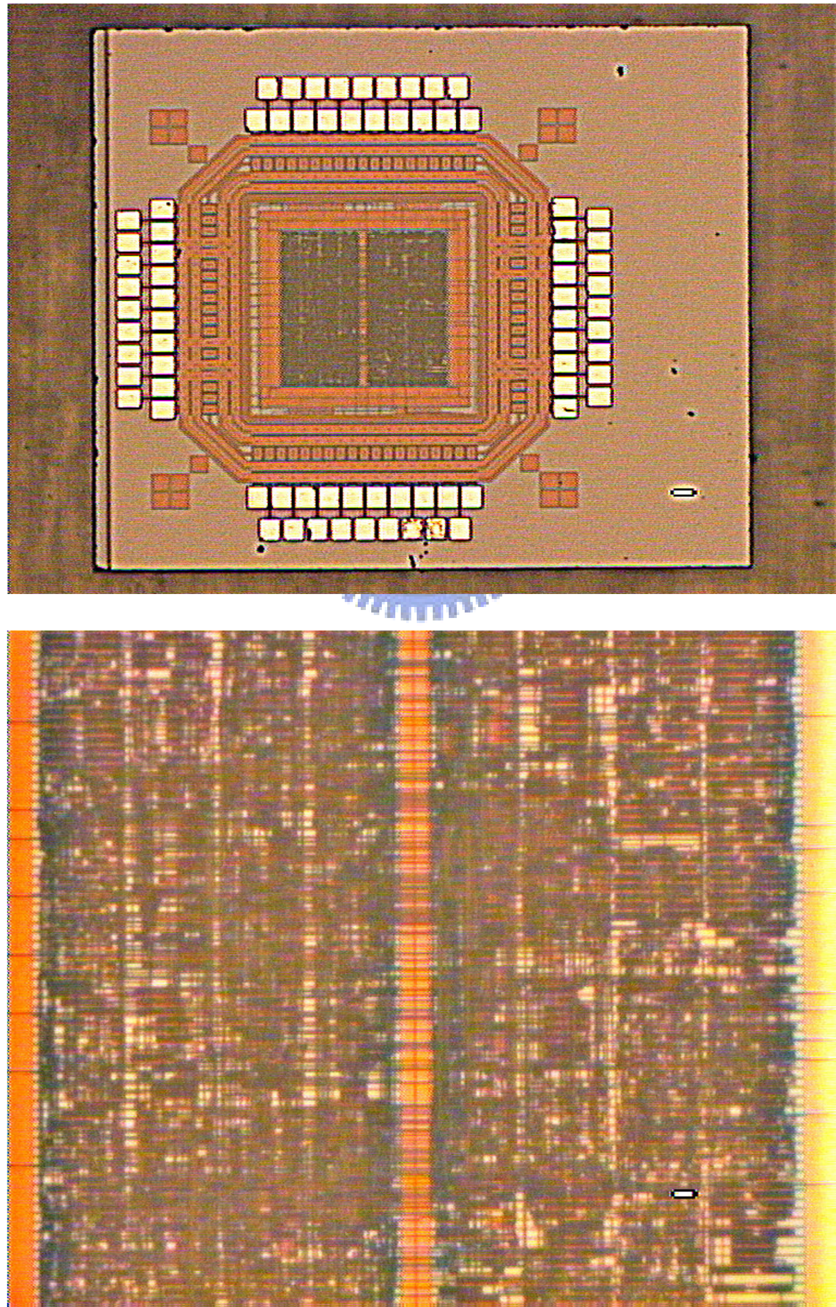


Figure 4.5.1 Die Microphotograph

Chapter 5 Conclusion & Future Works

A novel thermal-aware power management system for system-on-chip designs has been designed. The components of proposed system have been successfully designed and implemented in TSMC 0.25 um (1P5M) CMOS through CIC, Taiwan. Each component of proposed design is encapsulated to a Soft-IP as well. With above design, system architects are able to incorporate on-chip power-controls and sensors to achieve nominal power dissipation and ensure the targeting system working within specification. With proper utilization of the proposed design, the system not only prevents failure but also enhances performance by controlling each component's operating speed with feedback from the sensors. With little system overhead and minimum hardware requirements, this design yields intricate control and optimal management as well as provides the flexibility to support different management schemes. The significant contributions of this research are:

1. Proposes the system-level architecture of TAPM as shown in Figure 1.1.
2. Integrates TMS with SMBus to name TAPM Soft-IP.
3. Provides actual performance according to testing results for TAPM.
4. Provides fully documents and verilog codes to know about TAPM system information.

Based on Figure 2.1.1, the temperature sensors unit and PC&AC unit is helpful to strengthen the functionality of TAPM for SoC design. Thus, the future works of this

research should include at least two directions:

1. The on-chip temperature sensors should be developed for SoC design. As shown in Figure 5.1.1, the TAPM is integrated with on-chip temperature sensors that need low power and high accuracy analog to digital converters (ADCs) in order to precisely transform detected analog signal to digital signal. Such circuits expand the functionality of the TAPM and enable TAPM to get accuracy on-chip temperature value.

Figure 5.1.1 Building Blocks of Temperature Sensor with TAPM

2. The power control mechanisms such as voltage islands are helpful for SoC designs. The concept of voltage islands is to supply multi-level and scalable voltage in a single chip as shown in Figure 5.1.2. Each of functional units is separated with different islands according individual power characteristics in order to scale suitable voltage level. TAPM is integrated with voltage islands to enhance power management ability in order to reduce power consumption of the chip.

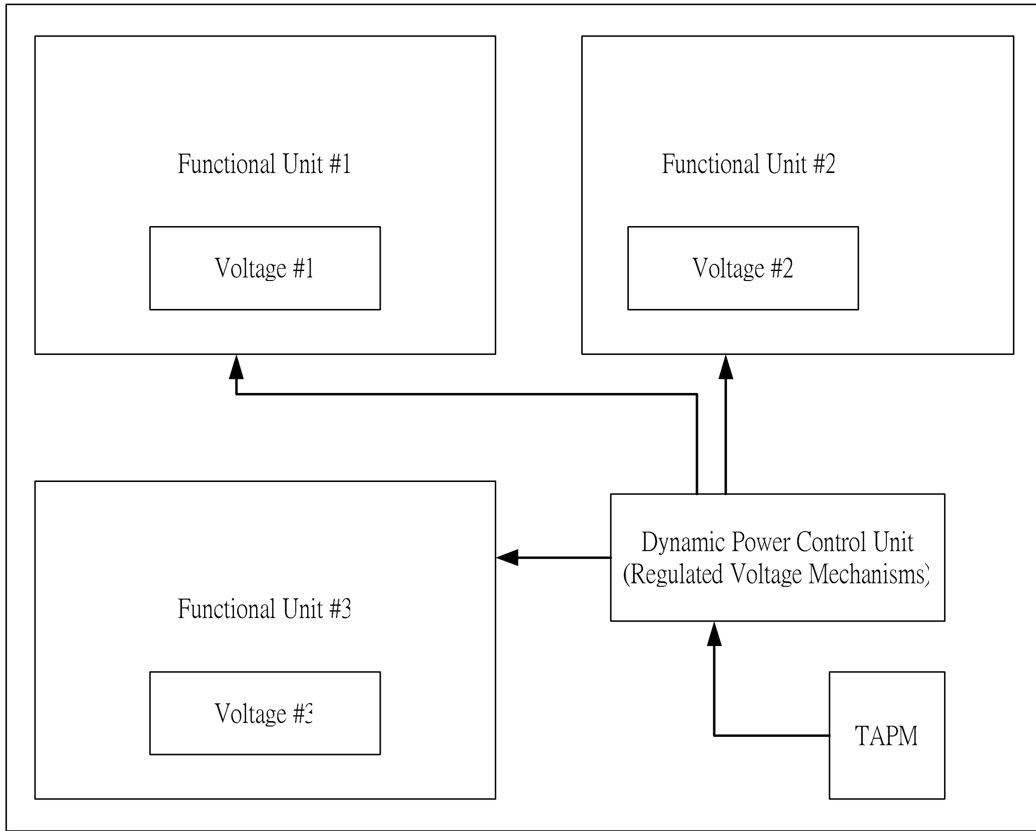
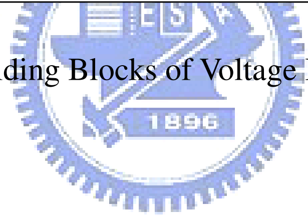


Figure 5.1.2 Building Blocks of Voltage Island with TAPM



Bibliography:

[1] Chip Implementation Center, Taiwan, http://www.cic.org.tw.

[2] L. Cai, P. Kritzinger, M. Olivares, and D. Gajski, "Top-Down System Level Design Methodology Using SpecC, VCC and SystemC," presented at Automation and Test in Europe Conference and Exhibition, 2002.

[3] M. Keating and P. Bricaud, *Reuse Methodology Manual for System-on-a-Chip Designs*, Third Edition ed: Kluwer Academic Publishers, 2002.

[4] H. Chiueh, J. Draper, and J. Choma, Jr., "A Dynamic Thermal Management Circuit for System-on-Chip Designs," presented at 2001 International IEEE Conference on Electronics, Circuits, and Systems, Malta, Sep, 2001.

[5] H. Chiueh, J. Draper, and J. Choma, Jr., "A Thermal Management System and Prototyping for System-on-Chip Designs," presented at Southwest Symposium on Mixed-Signal Design, Austin, Texas, Feb, 2001.

[6] H. Chiueh, "A Thermal Management Design for System-on-Chip Circuits and Advanced Computer Systems," Ph.D dissertation, University of Southern California, 2002.

[7] W. Wolf, *Modern VLSI Design System-on-chip Design*, Third Edition ed: Prentice Hall Semiconductor Design Series, 2002.

[8] "System Management Bus (SMBus) Specification," Version 2.0 ed. SBS Implementation Forum, August 3, 2000,

[9] "AMBA Specification," Rev 2.0 ed. ARM Corporation, May 13, 1999, http://www.arm.com.

[10] "CoreConnect Bus Architecture, A 32-, 64-, 128-bit core on-chip bus standard." IBM Microelectronics, 1999, http://www.ibm.com.

[11] "EC. Interface Specification." MIPS Technologies Corporation, 2000, www.mips.com.

[12] Y. Chang, "Design and Implementation of Interface Circuit for Thermal Management Systems," Master Thesis, National Chiao Tung University, Taiwan, 2003.

[13] H. Chiueh, L. Luh, J. Draper, and J. Choma, Jr., "A Novel Fully Integrated Fan Controller for Advanced Computer Systems," presented at Southwest Symposium on Mixed -Signal Design, San Diego, California, 2000.

[14] H. Ho, "A Fully Integrated Multi-Level Controller for System-on-Chip Thermal Management Designs," Master Thesis, National Chiao Tung University, Taiwan, 2003.

[15] D. E. Lackey, P. S. Zuchowski, T. R. Bednar, D. W. Stout, S. W. Gould, and J. M. Cohn, "Managing Power and Performance for System-on-chip Designs using Voltage Islands," IBM Microelectronics Division Essex Junction, 2002.

[16] Chinhung Chan, Yucheng Chang, Hsichi Ho and Herming Chiueh "A Thermal-Aware Power Management Soft-IP for Platform-based SoC Designs," presented at VLSI/CAD Symposium, Taiwan, 2004.

[17] Chinhung Chan, Yucheng Chang, Hsichi Ho and Herming Chiueh "A Thermal-Aware Power Management Soft-IP for Platform-based SoC Designs," presented at the International Symposium on System-on-Chip Tampere, Finland, November 16-18, 2004.

Appendix A: The Defined Read/Write Commands for TMU

Command [7:0]	R/W	Source/Purpose Register	Function
0000_0000b	W	FANC0[7:0]	Fan Controller 0
1000_0000b	R		
0000_0001b	W	FANC1[7:0]	Fan Controller 1
1000_0001b	R		
0000_0010b	W	FANC2[7:0]	Fan Controller 2
1000_0010b	R		
0000_0011b	W	FANC3[7:0]	Fan Controller 3
1000_0011b	R		
0000_1000b	W	THRES0[15:0]	High/Low Threshold of Sensor 0
1000_1000b	R		
0000_1001b	W	THRES1[15:0]	High/Low Threshold of Sensor 1
1000_1001b	R		
0000_1010b	W	THRES2[15:0]	High/Low Threshold of Sensor 2
1000_1010b	R		
0000_1011b	W	THRES3[15:0]	High/Low Threshold of Sensor 3
1000_1011b	R		
0000_1100b	W	OFF_THRES[15:0]	Offset High/Low Threshold of the Sensors
1000_1100b	R		
0000-1111b	W	CONFIG[7:0]	Configuration
1000_1111b	R		
1000_0100b	R	TEMP0[7:0]	Temperature of Sensor 0
1000_0101b	R	TEMP1[7:0]	Temperature of Sensor 1
1000_0110b	R	TEMP2[7:0]	Temperature of Sensor 2
1000_0111b	R	TEMP3[7:0]	Temperature of Sensor 3
1000_1101b	R	REPORT0 [15:0]	Underflow/Overflow Temperature Report
1000_1110b	R	REPORT1 [15:0]	Underflow/Overflow Offset Temperature Report

Appendix B: Configuration & Report Registers Assignments

Register	Bit Assignment	Function
Report 0 Register	0~3	Sensor 0~3 underflow
	4~7	Sensor 0~3 overflow
	8~15	Reserved for future using
Report 1 Register	0~1	Reserved for future using
	2	Offset underflow between sensor 2 and sensor 3
	3	Offset underflow between sensor 1 and sensor 3
	4	Offset underflow between sensor 1 and sensor 2
	5	Offset underflow between sensor 0 and sensor 3
	6	Offset underflow between sensor 0 and sensor 2
	7	Offset underflow between sensor 0 and sensor 1
	8~9	Reserved for future using
	10	Offset overflow between sensor 2 and sensor 3
	11	Offset overflow between sensor 1 and sensor 3
	12	Offset overflow between sensor 1 and sensor 2
	13	Offset overflow between sensor 0 and sensor 3
	14	Offset overflow between sensor 0 and sensor 2
	15	Offset overflow between sensor 0 and sensor 1
Configuration Register	0	Threshold enable
	1	Offset enable
	2	Interrupt enable
	3	Offset Interrupt enable
	4~7	Sensor 0~3 enable