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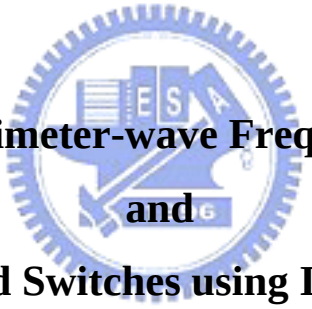
碩 士 論 文

使用砷化銦鎵假型高速電子移動電晶體之

單晶毫米波倍頻器及新式寬頻開關之設計



Design of Millimeter-wave Frequency Doubler

and

New Broadband Switches using InGaAs pHEMT

研 究 生：陳揚裕　　(Yang-Yu Chen)

指導教授：鍾世忠 博士 (Dr. Shyh-Jong Chung)

中華民國 九十三 年 六 月

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摘要

這篇論文中展示了使用砷化銦鎵假型高速電子移動電晶體之單晶毫米波的兩種電路，包含一個 35 轉 70 GHz 的毫米波二倍頻器及兩個寬頻開關。首先，仔細描述了倍頻器的設計方法，再利用 B 類的操作點去完成一個在輸入為 1 dBm 時有其最大的轉換增益為 -8.4dB 的 35 轉 70 GHz 之二倍頻器，此設計在其中心頻率 35 GHz 附近有 1 GHz 左右的頻寬而且有著平坦的轉換增益。其次，也詳盡的描述了寬頻毫米波開關的設計方法並且展示一個從 24 到 65 GHz 的單刀單擲開關與一個從 30.5 到 64.5 GHz 的單刀雙擲開關之實例。24 到 65 GHz 的單刀單擲開關之設計有小於 3dB 的介入損耗與大於 30dB 的隔絕度，在中心頻率為 44.5 GHz 處有 41 GHz 的頻寬與平坦的介入損耗。30.5 到 64.5 GHz 的單刀雙擲開關有小於 6dB 的介入損耗與大於 30dB 的隔絕度，在中心頻率為 47 GHz 處有 34 GHz 的頻寬與平坦的介入損耗。

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ABSTRACT

Two kinds of MMIC circuits using InGaAs pHEMT are exhibited in this thesis, including a 35-to-70 GHz millimeter-wave frequency doubler and two broadband switches. First, the design methodology of the frequency multiplier is fully described. The class B operation was employed to achieve the 35-to-70 GHz frequency doubler with measured maximally conversion gain of -8.4 dB for 1 dBm input power. This design has 1 GHz bandwidth centered at 35 GHz for a flat conversion gain. Secondly, the design methodology of broadband millimeter-wave switches is shown in detail, along with the demonstrations of a 24-to-65 GHz SPST switch and a 30.5-to-64.5 GHz SPDT switch. For the designed 24-to-65 GHz SPST switch, the measured insertion loss is less than 3 dB and the isolation is better than 30 dB. It has 41 GHz bandwidth centered at 44.5 GHz for a flat insertion loss. For the design of 30.5-to-64.5 GHz SPDT switch, the measured insertion loss is less than 6 dB and the isolation is better than 30 dB with a total bandwidth of 34 GHz centered at 47 GHz for a flat insertion loss.

ACKNOWLEDGMENTS

本篇論文可以順利完成，首先要感謝我的指導教授鍾世忠博士，在我的研究過程中提供了一個資源充足的實驗室，老師豐富的學識、待人處世的寬厚和對研究上的執著與熱忱，不但使我在學識與修養方面更上一層樓，也讓我學會以更嚴謹的態度面對浩瀚無涯的研究世界。同時要感謝口試委員瞿大雄教授、張志揚教授及陳浩暉教授的不吝指導得以使此篇論文更為完善；此外，要特別感謝張教授在V-BAND量測上所給予的協助。

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Chapter 1

INTRODUCTION

1.1 Motivation

A monolithic microwave/millimeter-wave integrated circuit (MMIC) is a microwave or millimeter-wave circuit, in which the active and passive components are fabricated on the same semiconductor substrate like gallium arsenide (GaAs) or indium phosphide (InP). The operating frequency can range from several to hundred GHz. The GaAs pseudomorphic high electron mobility transistor (pHEMT) is the most commonly available HEMT technology. The term “pseudomorphic” comes from the fact that the device channel is generally formed from InGaAs. The utilization of GaAs pHEMT technology have advanced performance and is capable of meeting the demands of most millimeter-wave wireless applications including local multipoint distribution system (LMDS), high speed local area networks (LAN’s), satellite communications, astronomy observations, automotive collision avoidance radar system, and military use [1].

In order to realize the frequency source of the millimeter-wave radar applications, a MMIC frequency doubler is required. The frequency doublers make it feasible to generate the voltage-controlled oscillator (VCO) signal which permits the use of standard components for low phase noise signal generation at lower frequency. A significant advantage would be achieved when all radio frequency (RF) components can be integrated on the same chip; therefore, this circuit is a crucial component to perform a single-chip millimeter-wave transceiver MMIC.

In the other hand, a broadband millimeter-wave switch can also be employed for diverse applications. It controls the signal flow of the integrated circuit. The

switch is also a key component to accomplish the system-on-chip (SOC) or system-on-insulator (SOI).

1.2 Organization

This thesis was devoted to the design of Millimeter-wave frequency doubler and new broadband switches using InGaAs pHEMT. It consists of six chapters Chapter 1 gives the introduction of the MMIC design for various applications and the organization of this thesis.

In Chapter 2, we will deal with the design methodology of frequency multiplier. The nonlinear devices characteristics are described; in the meantime, different biasing points and architectures with appropriate matching and biasing circuits are discussed to obtain an excellent performance of the frequency doubler.

Chapter 3 exhibits a 35-to-70 GHz frequency doubler using InGaAs pHEMT based on the theory which is introduced in Chapter 2. The special measurement techniques used in the millimeter-wave frequency range are also detailed for the circuit characterization. Last of all, both the simulated and measured results will be brought to comparison.

In Chapter 4, the design methodology of broadband switches will be introduced, along with various switching devices and switch configurations that will be presented. The Fisher's equivalence is also described for the wideband switches design.

Chapter 5 demonstrates a 24-to-65 GHz SPST switch and a 30.5-to-64.5 GHz SPDT switch using InGaAs pHEMT. These designs utilize the Fisher's equivalence as described in Chapter 4 to achieve the wideband performance.

Chapter 6 will combine the summary and indicates some suggestions for the MMIC design in the future.

Chapter 2

DESIGN METHODOLOGY OF FREQUENCY MULTIPLIER

2.1 Overview

It is an extremely difficult and inefficient progress to generate signal sources directly in the millimeter-wave frequency range. On the contrary, it is feasible to realize a low phase noise VCO with some standard components at low frequency. Therefore, we usually utilize the VCO to generate the signal source at low frequency then convert it to the millimeter-wave frequency via a frequency multiplier. The design methodology of frequency multiplier will be introduced in this chapter.

2.2 Nonlinear Devices

In contrast to the operation of power amplifiers and oscillators, which may be visualized as an essentially linear circuit problem perturbed by nonlinear effects, frequency multiplication relies specifically on the nonlinear device behavior as the basic operation mechanism. Therefore, one of the most essential portions in frequency multiplier design is the nonlinear device. In general, there are tow choices. One is passive diodes and the other is active FETs.

Passive Diodes The Schottky barrier diode (SBD) has been the primary nonlinear device for millimeter-wave frequency multiplier [2]. Fig. 2.1(a) shows the general structure of a SBD and Fig. 2.1(b) indicates its equivalent circuit. Also indicated are the key equations defining the nonlinearities, C_j and R_j, which are responsible for the multiplying operation. The parasitic series resistance, R_s, has to be minimized, in order to achieve high diode cut-off frequency and low multiplier conversion loss. This requires a low resistance current path within the diode

structure, which is implemented by a highly doped active layer below the cathode.

Active FETs FETs are widely used in MMIC frequency multipliers, as many monolithic foundry processes are based on the MESFET/HEMT structure. Consequently, FET frequency multipliers can be fabricated on the same chip with other FET-based circuits, such as amplifiers, oscillators, mixers and switches, to form integrated subsystems. In the large-signal modeling [3] shown in Fig. 2.2, the following six elements were assumed to be nonlinear: R_{fs}, R_{fd}, C_{gs}, C_{gd}, G_m and G_{ds}. However, the values of R_{fs} and R_{fd} remain very large and do not contribute to the generation of higher harmonics when the input power level is not large enough to cause the gate of the Schottky junction to conduct in the forward direction. Furthermore, active FET frequency multipliers offer the potential to achieve conversion gain. Generally, they also require less input power, have higher isolation and give comparable noise performance to diode frequency multipliers.

2.3 Biasing Points Considerations

In a frequency multiplier design with passive diodes, the biasing point chosen from 0V to several hundred millivolts is generally acknowledged. It can generate higher harmonics caused by the current clipping of the diodes.

By contrast, the biasing point selection, in a frequency multiplier design with active FETs, is more complicated. Among the four major nonlinearities considered in Section 2.2, the transconductance (G_m) and the output conductance (G_{ds}) are the major elements which cause the drain current clipping and generate higher harmonics. The capacitances (C_{gs} and C_{gd}) can be considered as parasitic elements which degrade the device gain and isolation at high frequencies. Following the quasi-static approximation of [4], the current at the drain port can be expressed as

$$I_{ds}(v_{gs},v_{ds}) = \int_{vT}^{vgs} g_m(v,v_{ds})dv + \int_0^{vds} g_{ds}(v_T,v)dv \quad , \qquad (2.1)$$

where v_T is a gate bias value determined for best convergence from large to small signal S-parameter under small signal excitation. From (2.1), it can be inferred that there are two possible ways to generate higher harmonics: one usage is the nonlinearity of G_m and the other is that of G_{ds}, Fig. 2.3(a) shows the behavior of I_{ds} versus V_{gs} and V_{ds}, and Fig. 2.3(b) indicates I_{ds}, G_m versus V_{gs} characteristics of the FETs. Each biasing point is further discussed in the following.

2.3.1 Class A

For a class A amplifier operation [5], the quiescent gate voltage must be selected so that the drain current is set to $I_{d0} = I_{DSS}/2$ and the drain voltage is set to $V_{d0} = (BV_{ds}-V_k)/2$, which corresponds to a biasing point of point A in Fig. 2.3(a). The resultant maximum G_m is shown in Fig. 2.3(b). Small-signal class A operation is linear as illustrated in Fig. 2.4(a), while large-signal class A operation introduces some nonlinearities in the output signal as illustrated in Fig. 2.4(b). As depicted in Fig. 2.4(b), the nonlinear trapezoidal wave function x(t) can be expressed as

$$x(t) = \begin{cases} 0 & 0 \le t \le \frac{c}{2} \quad and \quad T_0 - \frac{c}{2} \le t \le T_0 \\ \frac{A}{T_0/2 - c}(t - \frac{c}{2}) & \frac{c}{2} \le t \le \frac{T_0}{2} - \frac{c}{2} \\ A & \frac{T_0}{2} - \frac{c}{2} \le t \le \frac{T_0}{2} + \frac{c}{2} \\ -\frac{A}{T_0/2 - c}(t - T_0 + \frac{c}{2}) & \frac{T_0}{2} + \frac{c}{2} \le t \le T_0 - \frac{c}{2} \end{cases} \qquad (2.2)$$

$$x(t) = x(t + T_0) .$$

According to the Fourier series expansion [6], the Fourier coefficients X_n of the trapezoidal wave function x(t) can be expressed as

$$X_n = \begin{cases} \frac{1}{2} & n = 0 \\ -\frac{2\cos(\frac{ncp}{T_0})}{n^2 p^2 (1-\frac{2c}{T_0})} & n = \pm 1, \pm 3, \pm 5 \ldots \end{cases}, \quad (2.3)$$

the trapezoidal wave is composed of odd harmonic frequencies exclusively. Hence it appears that, in large-signal class A operation the output signal contains only odd harmonics of the fundamental signal. Consequently, the class A biasing condition is the favored choice when designing a tripler and other odd order multipliers.

2.3.2 Class B

For a class B amplifier operation [5], the bias is arranged to shut off the output device half of every cycle. In other words, the quiescent gate voltage must be set to $V_{g0} = V_p$, and the drain voltage is set to $V_{d0} = (BV_{ds}-V_k)/2$, which the biasing point is the same as point B, as shown in Fig. 2.3(a), near the pinch-off voltage as shown in Fig. 2.3(b). As illustrated in Fig. 2.5, when a sinusoidal signal is injected into a class B amplifier, the output signal will be half rectified, which is caused by the drain current clipping. As depicted in Fig. 2.5, the half-rectified sinusoidal wave function x(t) can be expressed as

$$x(t) = \begin{cases} A\sin w_0 t & 0 \le t \le \frac{T_0}{2} \\ 0 & \frac{T_0}{2} \le t \le T_0 \end{cases} \quad (2.4)$$

$$x(t) = x(t + T_0).$$

According to the Fourier series expansion, the Fourier coefficients X_n of the half-rectified sinusoidal wave function x(t) can be expressed as

$$X_n = \begin{cases} \dfrac{A}{p\,(1-n^2)} & n = 0,\pm 2,\pm 4... \\ 0 & n = \pm 3,\pm 5... \\ -\dfrac{jA}{4} & n = 1 \\ \dfrac{jA}{4} & n = -1 \end{cases}, \qquad (2.5)$$

except for the fundamental, the half-rectified sinusoidal wave is composed of even harmonic frequencies exclusively. Hence it appears that, in class B operation the output signal contains only even harmonics of the fundamental signal. Therefore, the class B biasing condition is the favorite choice when designing a doubler, quadrupler or other even order multipliers.

The operation of a class B amplifier has a smaller time-averaged transconductance value than a class A amplifier. The pinch-off point B, however, has a lower C_{gs} value, smaller power consumption and is free of forward conduction current at the gate. Point B is preferable to A for high frequency operation due to the lower leakage current through C_{gs}; the conductance associated with C_{gs} becomes more significant at high frequencies and the leakage currents through the capacitance degrade the device gain and conversion gain.

2.3.3 Resistive Concept

Another possible biasing point corresponds to point C as indicated in Fig. 2.3(a). Here, the variation of G_{ds} is the major factor to generate higher harmonics of the drain current. The channel of a FET, at low drain voltage, is a very linear resistor. It becomes significantly nonlinear only when the drain voltage becomes great enough to accelerate the electrons to their saturated drift velocity. In most FETs, this occurs at a few tenths of a volt to one volt, depending on the gate voltage. Therefore, at normal small-signal voltage of a few millivolts, the FET's resistive channel G_{ds} is

very linear. The resistance of this linear channel can be varied by applying a large signal to the gate. The large signal changes the depth of the depletion region under the gate and consequently the resistance of the entire channel. When the gate voltage drops below V_p, the FET's cutoff voltage, the resistance is virtually infinite; when the gate voltage reaches its maximum value, the channel resistance is very low, usually a few ohms. The range of resistances is entirely adequate to achieve good performance of producing higher harmonics, in which the concept is similar to the resistive mixer design theory [7]. However, the efficiency of generating higher harmonics is better with G_m than G_{ds}.

2.4 Frequency Multiplier Design

2.4.1 Architectures of Frequency Multipliers

In general, there are two different methods to design a frequency multiplier [8]. One is single-ended and the other is balanced.

Single-ended "Single-ended" means the usage of a single nonlinear device. Fig. 2.6 indicates the circuit of a single-ended FET frequency multiplier. This FET can generate higher harmonics to achieve a better multiplication with an appropriate bias.

Balanced Fig. 2.7 illustrates the circuit of a balanced FET frequency multiplier. Like the single-ended configuration, it also needs an applicable bias. Moreover, the balanced configuration can be used to reduce the unwanted fundamental frequency, in which the cancellation is caused by the 180^o out-of-phase.

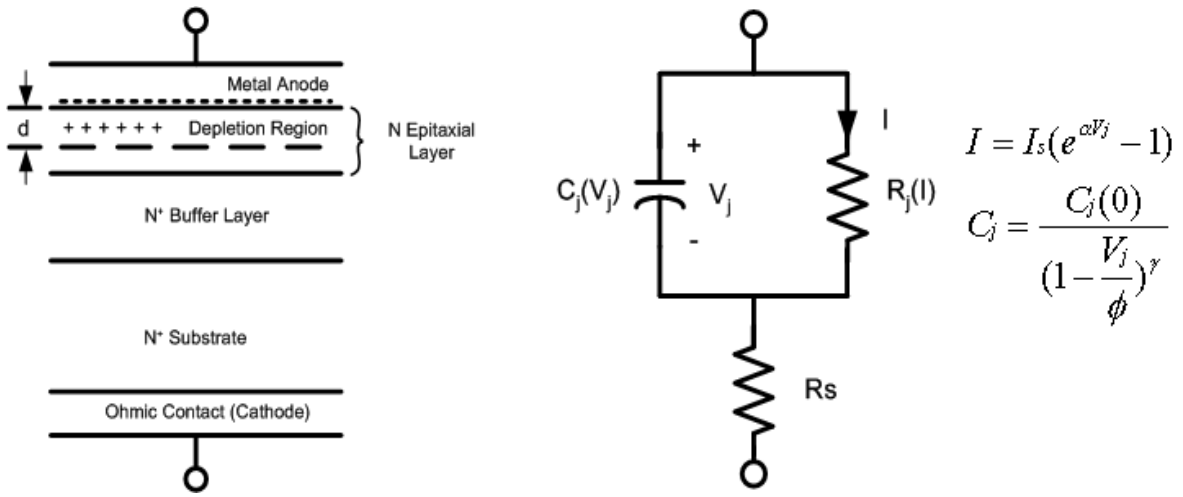
The balanced configuration has several advantages over the single-ended circuit. One is the nature of the phase cancellation for the fundamental frequency. The second advantage is that, like other balanced circuits, the FET balanced

frequency multiplier has greater bandwidth and 3 dB output power than the single-ended circuit. The third is that it is often easier to realize the load impedance of a balanced frequency multiplier than that of a single-ended circuit. Nevertheless, there are many drawbacks of the balanced configuration. The unit uses two FETs, consumes more DC power, and occupies larger chip area than that of the single-ended circuit. The usage of the coupler and combiner circuits, in a balanced configuration, is the other major die area consumption.

2.4.2 Input and Output Matching Network Configurations

The device-circuit interaction not only at the fundamental frequency, but also at the harmonic frequencies, is very crucial to the multiplication process. Although in the case of a frequency doubler it is mainly the fundamental frequency and its second harmonic to be concerned with, this still leaves transistor input and output impedance matching conditions at both these frequencies to be accounted for as potentially influential design considerations, in addition to the general dependence on the drive levels [9], [10].

The basic FET frequency doubler configuration is shown in Fig. 2.8, exhibiting a FET in common source configuration flanked by matching networks which match the gate-source port of the device to the generator at the fundamental frequency and the device drain-source port to the external load at the second harmonic frequency. A more rigorous design must be capable of undesired harmonics suppression such as a quarter-wavelength short-circuited stub, with respect to fundamental frequency, at the gate-source port of the device to suppress second harmonic frequency leakage and a quarter-wavelength open-circuited stub, with respect to fundamental frequency, at the drain-source port of the device to suppress fundamental frequency leakage. In addition, biasing circuits for the gate-source and drain-source port are also involved.



(a) (b)

Fig. 2.1 The Schottky barrier diode (SBD) with (a) general structure, (b) its equivalent circuit.

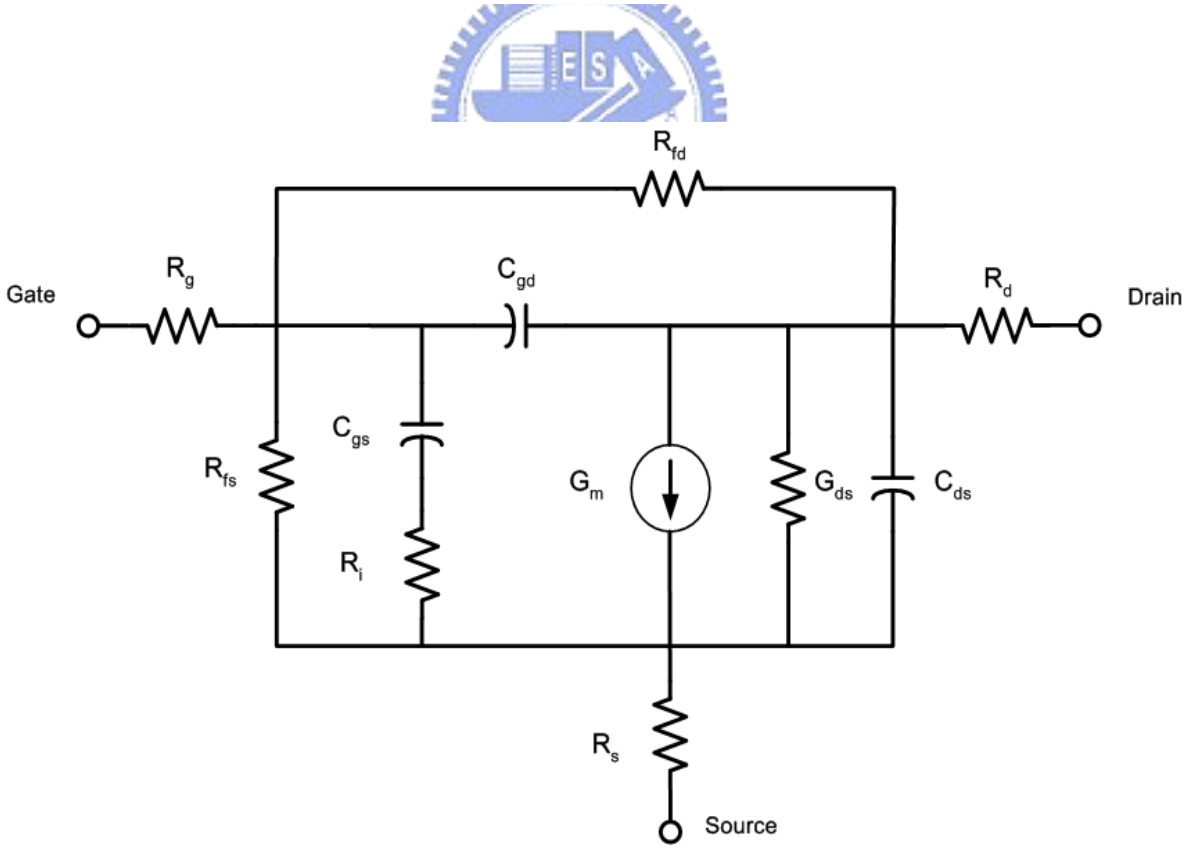
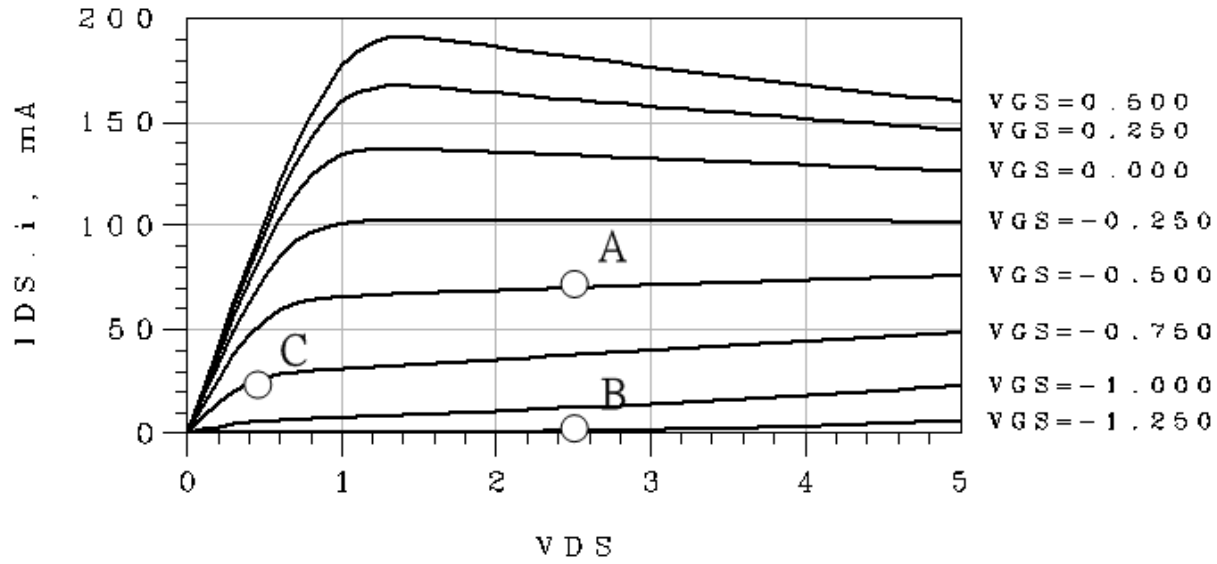
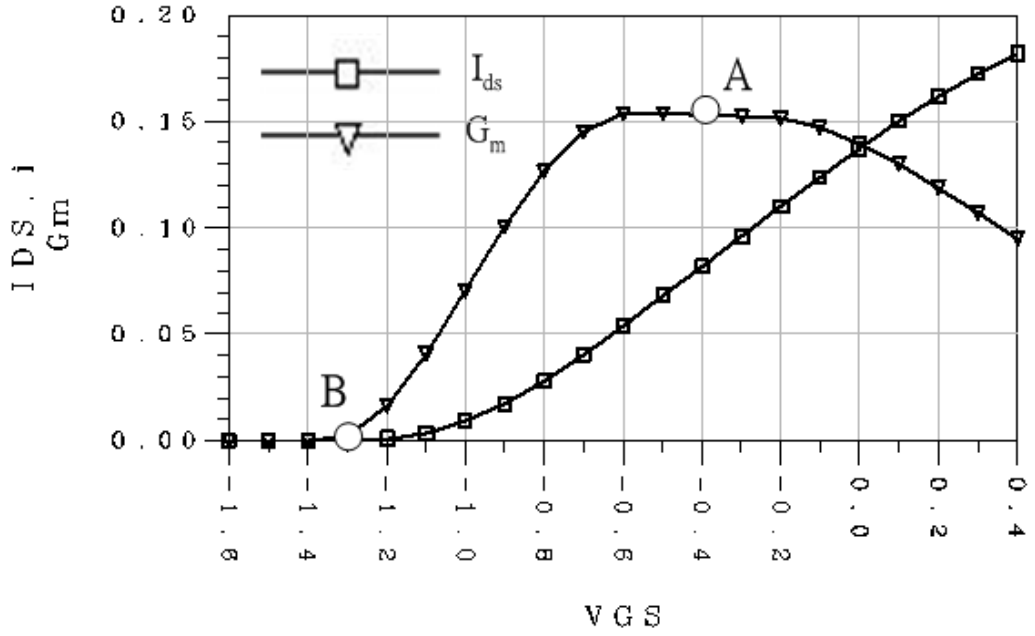


Fig. 2.2 The large-signal model of a FET

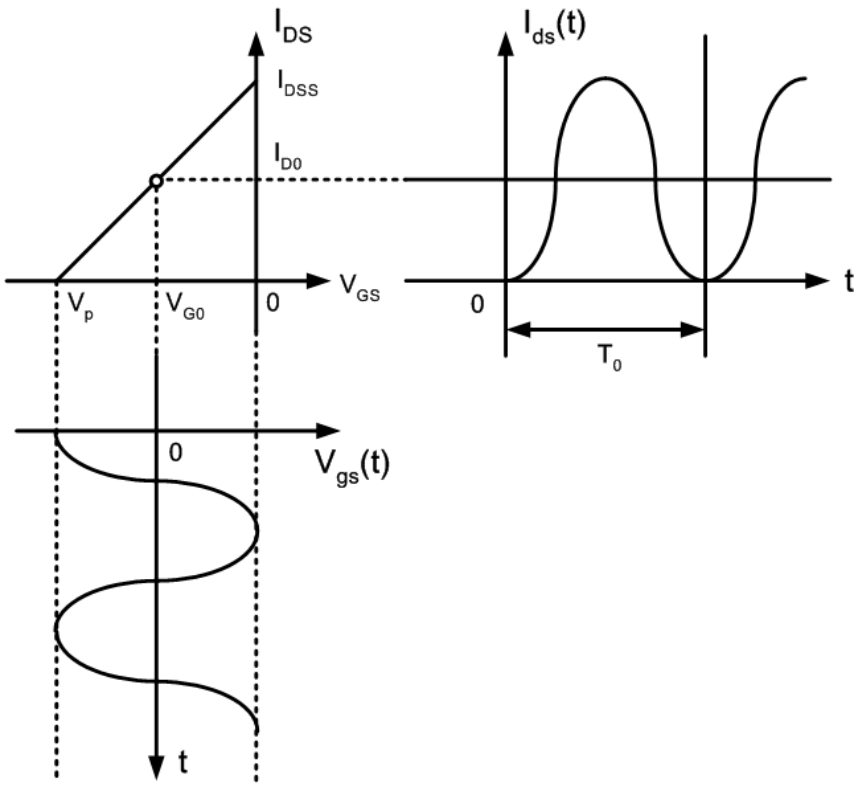


(a)

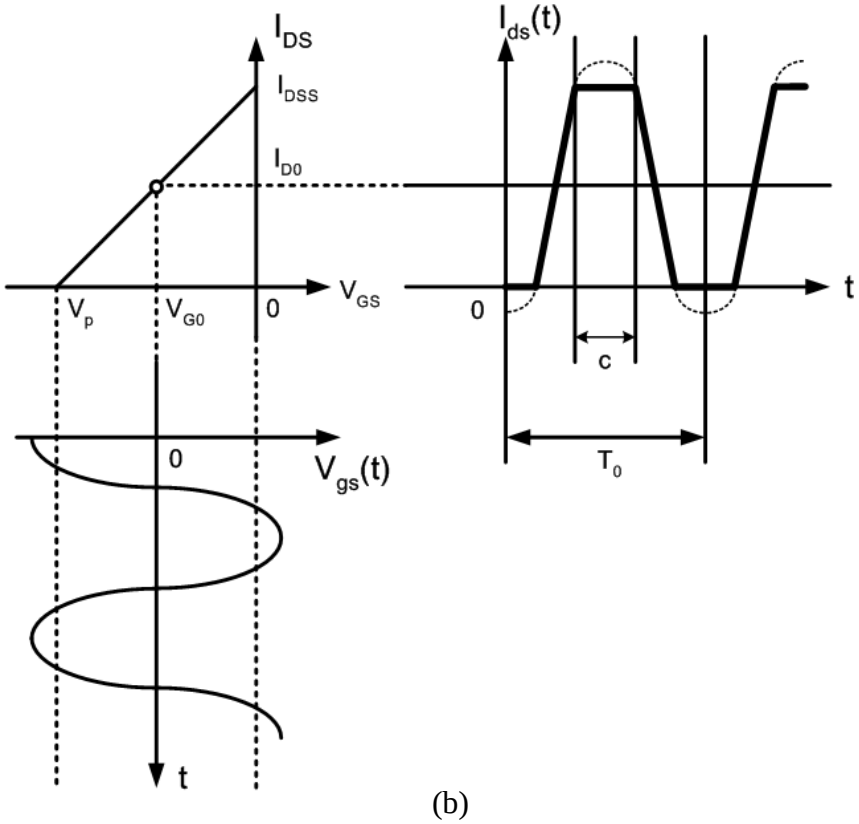


(b)

Fig. 2.3 DC characteristics of the FET. (a) I_{ds} versus V_{gs} and V_{ds}, (b) I_{ds} and G_m versus V_{gs} at V_{ds} = 1.5 V.



(a)



(b)

Fig. 2.4 Class A operation with (a) small-signal, (b) large-signal.

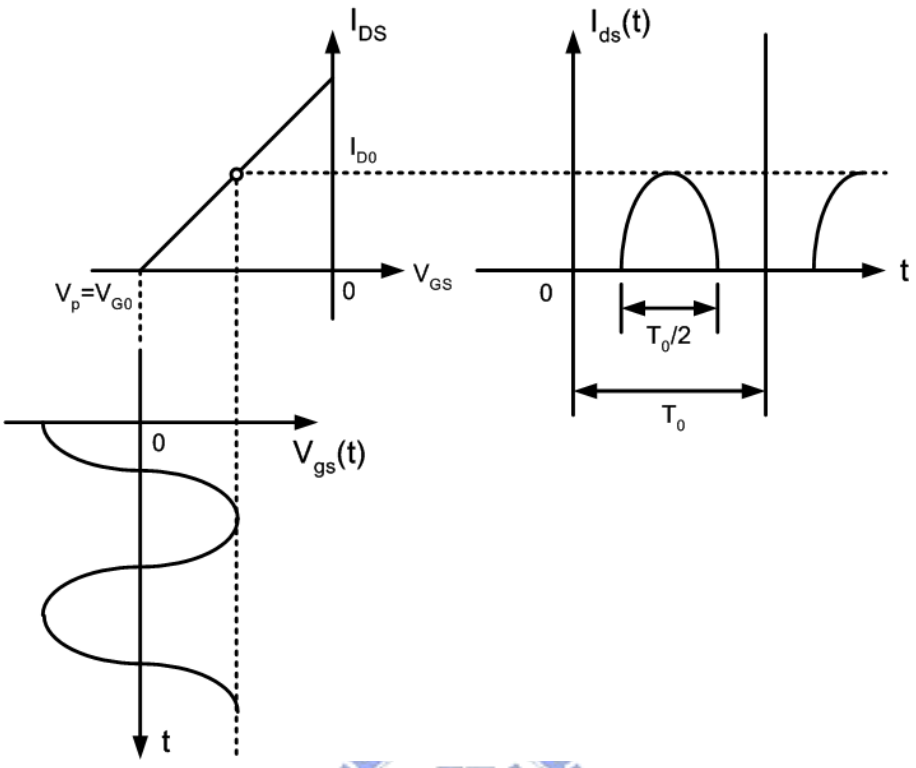


Fig. 2.5 Class B operation.

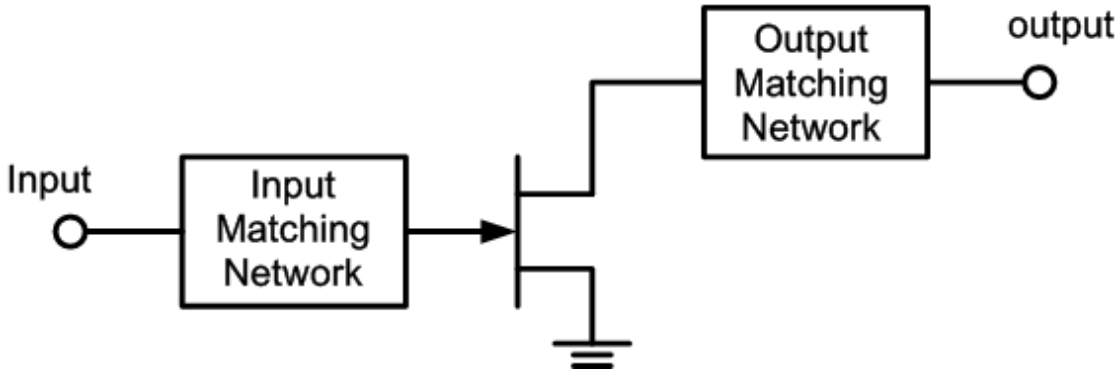


Fig. 2.6 The single-ended configuration of a frequency multiplier.

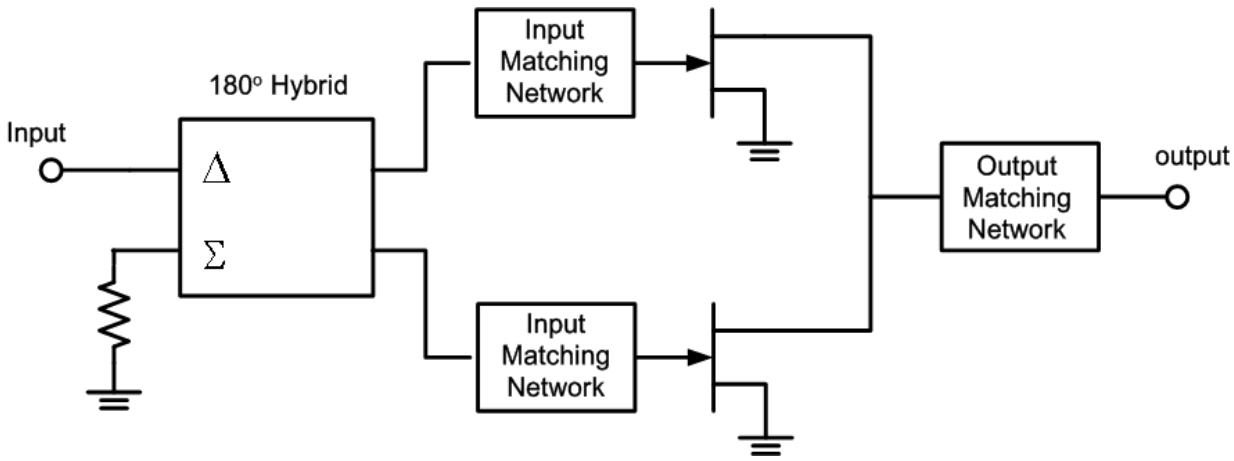


Fig. 2.7 The balanced configuration of a frequency multiplier.

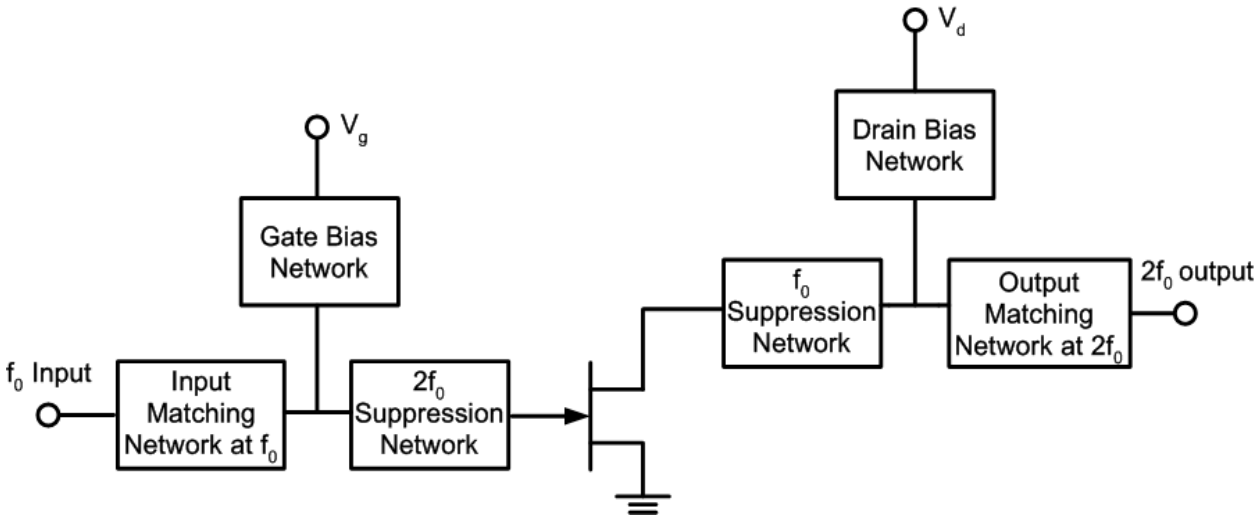


Fig. 2.8 The basic configuration of a frequency doubler.

Chapter 3

FREQUENCY MULTIPLIER USING INGAAS PHEMT

3.1 Overview

Based on the analysis and design methodology described in Chapter 2, this chapter demonstrates a 35-to-70 GHz millimeter-wave frequency doubler using InGaAs pHEMT. The fabrication, design and simulations of the circuit will be presented in the following. The measurement considerations are also specified in detail and the measured results are depicted in the last section.

3.2 MMIC Foundry Description

The pHEMT device used in this design is fabricated by WIN Semiconductor Corp. with a standard 0.15-um high-power InGaAs pHEMT MMIC process. The process employs a hybrid lithographic approach using direct-write electron beam (E-beam) lithography for sub-micron T-gate definition and optical lithography for the other process steps. The pHEMT devices are grown using molecular beam epitaxy (MBE) on 6-inch semi-insulating (SI) GaAs substrates. The pHEMT device has a typical unit current gain cutoff frequency (f_t) of 85 GHz and maximum oscillation frequency (f_{max}) of 200 GHz. The peak DC transconductance (G_m) at -0.45 V gate-source voltage is 495 mS/mm. The gate-drain breakdown voltage is 10 V, and the maximum drain current at 0.5 V gate-source voltage is 650 mA/mm. Other passive components include thin-film resistor (TFR), mesa-resistor (epitaxial layer), metal-insulator-metal (MIM) capacitors, spiral inductors, and air-bridges. The wafer is thinned to 100 um for the backside metal plating and reactive ion etching (RIE) via-holes are used for DC grounding.

3.3 35-to-70 GHz Frequency Doubler using InGaAs pHEMT

3.3.1 Circuit Design

Fig. 3.1 indicates the schematic diagram of the 35-to-70 GHz frequency doubler. In order to minimize the chip area and the DC power consumption, the single-ended frequency doubler configuration was adopted. This circuit was designed using microstrip transmission lines. The nonlinear device is an InGaAs pHEMT with 4 x 75 um gate width. An effective way to employ an InGaAs pHEMT as a frequency doubler is to use it as a half-wave rectifier which is described in Section 2.3.2. Consequently, the operating condition near the pinch-off region (V_{gs} = -0.95V, V_{ds} = 1.45V) with 14.5 mW power consumption was chosen to generate higher even harmonic power level. One quarter-wavelength open-circuited radial stub functions as a 35 GHz bandstop filter to reject the fundamental frequency at drain. The radial stub has wider bandwidth and higher rejection of more than 20 dB. The gate bias is injected through a thin-film resistor connected to a decoupling MIM capacitor and a high impedance transmission line. This resistor stabilizes the InGaAs pHEMT at low frequencies. The combination of the resistor, capacitor and high impedance transmission line impedance is equivalent to a quarter-wavelength to yield the open condition at the input line. The decoupling circuit for the drain bias is realized via the similar method. The input port, with a DC blocking MIM capacitor, was matched to receive maximum power at the fundamental frequency of 35 GHz. The output port, with a DC blocking coupled-line, was matched to deliver maximum power at second harmonic frequency of 70 GHz. The matching networks at the input and output of the circuit are achieved using 50Ω open-circuited stubs. A layout of the 35-to-70 GHz frequency doubler with chip size of 2 x 1 mm^2 is accomplished by

the Cadence tools and is depicted in Fig. 3.2.

3.3.2 Simulated Results

The nonlinear InGaAs pHEMT model used in the simulation is a HP EEsof scalable nonlinear HEMT model (EE_HEMT model) provided by the foundry. The 35-to-70 GHz frequency doubler performance is simulated via the harmonic balance technique implemented in the commercial computer-aided design (CAD) software Agilent Advanced Design System (ADS). All the matching, biasing and other passive circuits are simulated through an electromagnetic (EM) full-wave simulator SONNET.

Conversion and rejection performances are the important specifications for a frequency doubler design. The definition of conversion gain is that the second harmonic output power minus the fundamental input power. The fundamental rejection is defined as the fundamental output power minus the fundamental input power, and the third harmonic rejection is defined as the third harmonic output power minus the fundamental input power. They are usually expressed in decibels. The simulated conversion gain, fundamental rejection, third harmonic rejection and output power versus input power from -10 to 15 dBm at input frequency of 35 GHz are plotted in Fig. 3.3 and Fig. 3.4. It is observed that, for an input power level at 3 dBm, the conversion performance achieves a maximum conversion gain of -6.5 dB. The saturated output power at 70 GHz is almost 0 dBm for 15 dBm input power. Fig. 3.5(a) and Fig. 3.5(b) also indicate the simulated conversion gain, fundamental rejection and third harmonic rejection as a function of input frequency from 32 to 38 GHz with an input power level of 1 and 6 dBm. It has around 1 GHz bandwidth centered at 35 GHz for a flat conversion gain. The simulated small-signal S-parameters from 20 to 50 GHz and 60 to 80 GHz, illustrated in Fig. 3.6(a) and Fig

3.6(b), give some assurances that the input and output ports are matched to nearly 50Ω standard. Fig. 3.7 shows the simulated large-signal S-parameters from 30 to 40 GHz with input frequency of 35 GHz and output frequency of 70 GHz for 1 dBm input power.

3.3.3 Measurement Considerations

In the millimeter-wave frequency range, two significant concerns of the 35-to-70 GHz frequency doubler should be taken into account. One is the power measurement and the other is the stability assurance.

Power Measurement To acquire the absolutely accurate power level at 70 GHz, a V-band waveguide power sensor is required. The power sensor calculates each power value of the in-band frequencies resulting in a total power level. Accordingly, only the 70 GHz signal can exist to guarantee an accurate measurement. Indeed, a power meter, with calibrated calibration factors (CF) at each frequency, must be connected to the power sensor to depict the value of the measured power level.

Stability Assurance The stability assurance is the key point to certify the accuracy for the power measurement. A spectrum analyzer (SA) can be used to verify whether the undesired oscillation occurs or not. Nevertheless, the commercially available SAs are not capable of directly measurement up to the V-band, W-band or higher frequencies. An external harmonic mixer should be applied with the SA to perform the down-conversion of the V-band, W-band or higher frequencies down to the lower frequency band. Therefore, we can still validate the frequency spectrum of the V-band, W-band or higher frequencies via the commercially available SAs and external harmonic mixers with the calibrated conversion loss (CL) and reference level offset. The harmonic mixing causes many

mixer products ($mf_{RF} \pm nf_{LO}$) at the intermediate frequency (IF) output. As a result, within a single harmonic band, a single input signal can produce multiple responses on the analyzer display as illustrated in Fig. 3.8 (in this case, the 76 GHz signal is valid), only one of which is valid. These responses come in pairs, where members of the valid response pair are separated almost to $2f_{IF}$ and either the right-most (for negative harmonics) or left-most (for positive harmonics) member of the pair is the correct response. To identify the actual signals from the undesired images and spurs, a frequency-shift method can be applied. The altered quantity of the actual signals must consist with the shift of the radio frequency (RF) or local oscillator (LO) when either the RF or LO frequency is shifted. Otherwise, the remains are the undesired images and spurs. For some newer types of the SAs, identification of valid responses is achieved by simply turning on the signal-identification (SIG ID) feature.

3.3.4 Measured Results

The 35-to-70 GHz frequency doubler was measured via on-wafer probing. Fig. 3.9(a) and Fig. 3.9(b) illustrate the test setups used for the circuit characterization. The former is established for power measurement and the latter verifies the stability assurance. A microphotograph of the 35-to-70 GHz frequency doubler is shown in Fig. 3.10.

The measured conversion gain, fundamental rejection, third harmonic rejection and output power versus input power from -10 to 15 dBm at input frequency of 35 GHz are plotted in Fig. 3.11 and Fig. 3.12. It is observed that, for an input power level at 1 dBm, the conversion performance achieves a maximum conversion gain of -8.4 dB. The saturated output power at 70 GHz is -2.6 dBm for 15 dBm input power. Fig. 3.13(a) and Fig. 3.13(b) also indicate the measured conversion gain, fundamental rejection and third harmonic rejection as a function of input frequency

from 32.5 to 37.5 GHz with an input power level of 1 and 6 dBm. It has almost 1 GHz bandwidth centered at 35 GHz for a flat conversion gain. The measured small-signal S-parameters from 20 to 50 GHz and 75 to 80 GHz, illustrated in Fig. 3.14(a) and Fig. 3.14(b), give some agreements with that the input and output ports are matched to nearly 50Ω standard.

As discussed in Section 3.3.3, stability assurance is an important factor to guarantee the accuracy of the power measurement. Fig. 3.15 and Fig. 3.16 depict the frequency spectrum from 58 to 75 GHz and 75 to 110 GHz. Only the 70 and 105 GHz signals are valid and the others are images and spurs. It can be confirmed by the RF-shift technique. When the fundamental 35 GHz input signal was shifted by 1 MHz, not only the second harmonic 70 GHz output signal was shifted by 2 MHz as illustrated in Fig. 3.17(a), but also the third harmonic 105 GHz output signal was shifted by 3 MHz as illustrated in Fig. 3.17(b). If an oscillating signal appears within 58 to 110 GHz, the shift must be zero caused by the unchanged LO frequency. For example, the 61.2 and 78.09 GHz signals are shifted by 1.75 and 2.258 MHz as indicated in Fig. 3.17(c) and Fig 3.17(d). Consequently, they are not actual signals. Similarly, the others which are verified by RF-shift, are also images and spurs except for the 70 and 105 GHz signals. Fig. 3.18(a) indicates none of the low frequency oscillations from DC to 40 GHz. The 35 GHz signal is the leakage from the input signal. A more rigorous inspection from DC to 1 GHz frequency spectrum is shown in Fig 3.18(b). Therefore, we can confirm that this 35-to-70 GHz frequency doubler is stable for the above frequency bands. Furthermore, if a low frequency oscillation caused by the impurity of power supply or other defects occurs, an out-of-chip capacitor can be added to the drain or gate port to eliminate the oscillation.

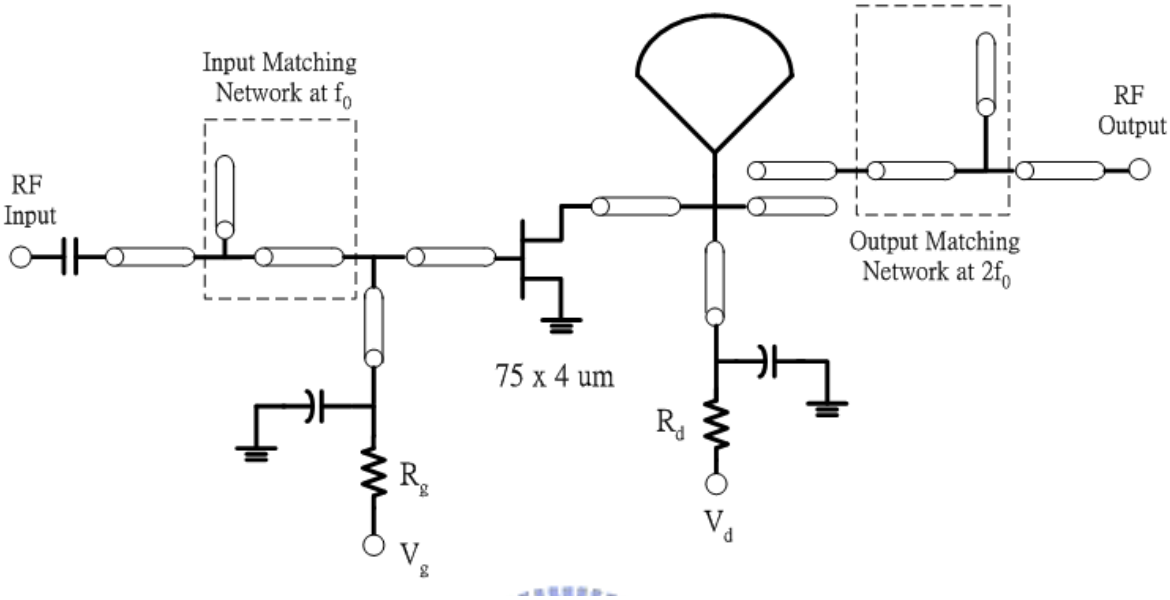


Fig. 3.1 The schematic diagram of the 35-to-70 GHz frequency doubler.

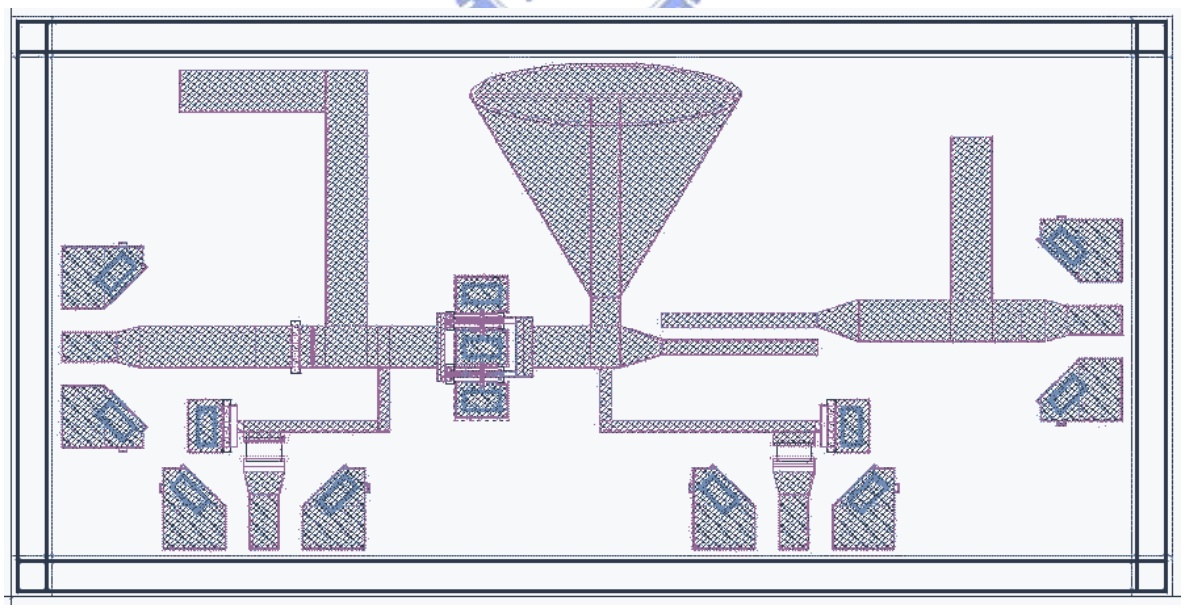


Fig. 3.2 Layout of the 35-to-70 GHz frequency doubler.

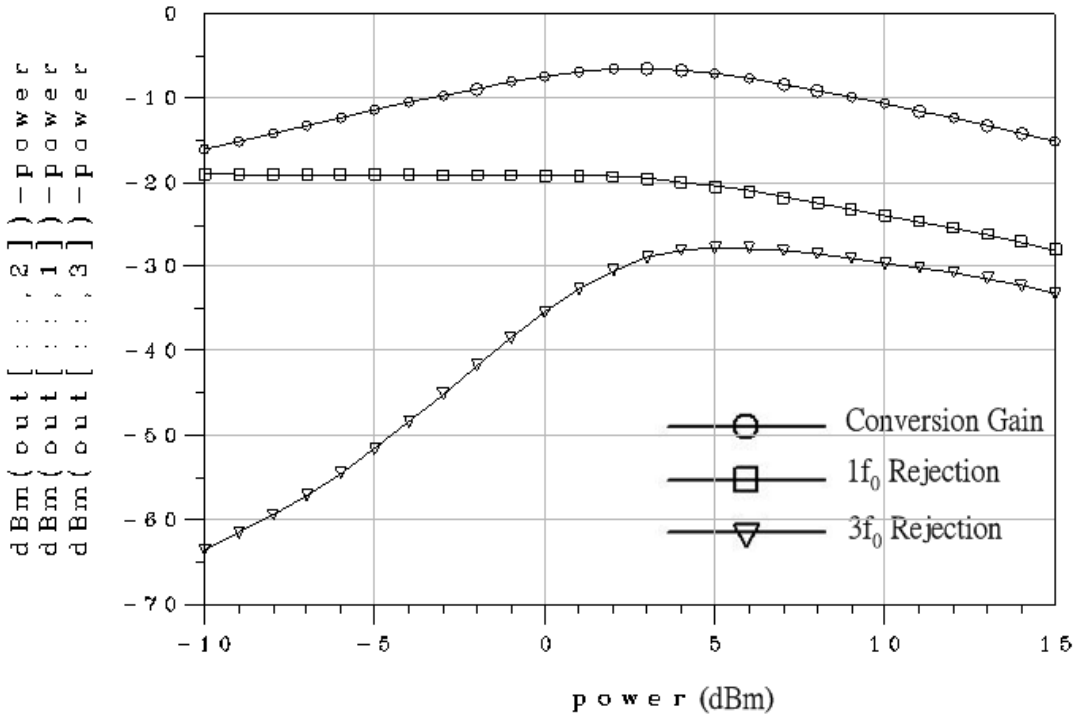


Fig. 3.3 The simulated conversion gain, $1f_0$ and $3f_0$ rejection versus input power of the 35-to-70 GHz frequency doubler.

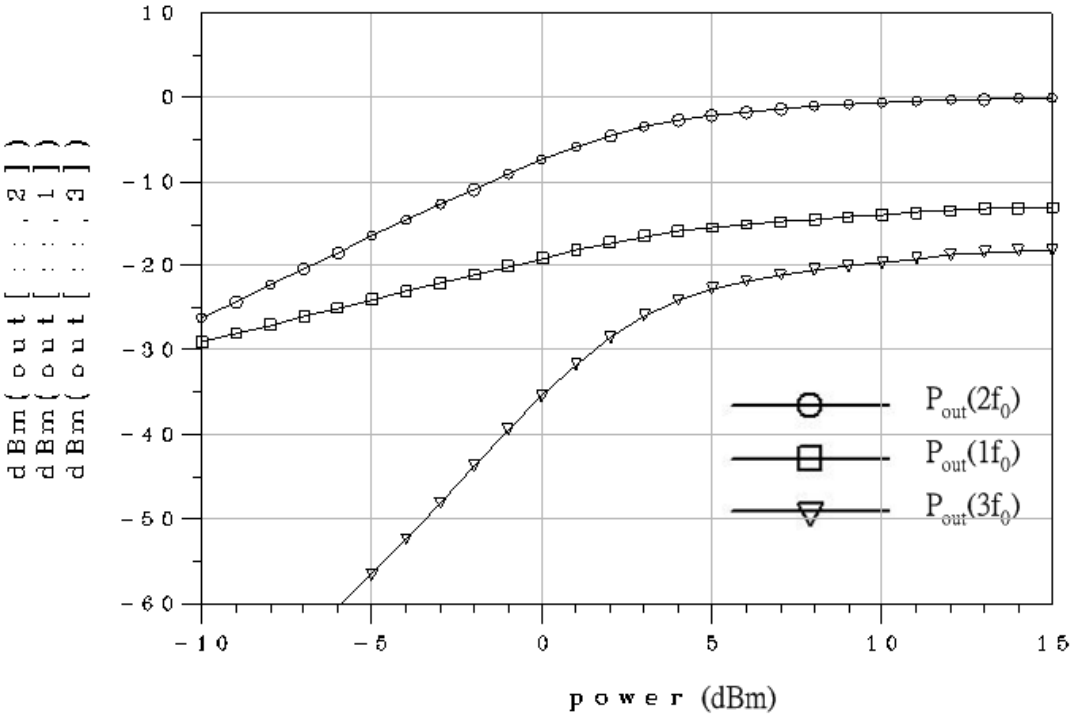
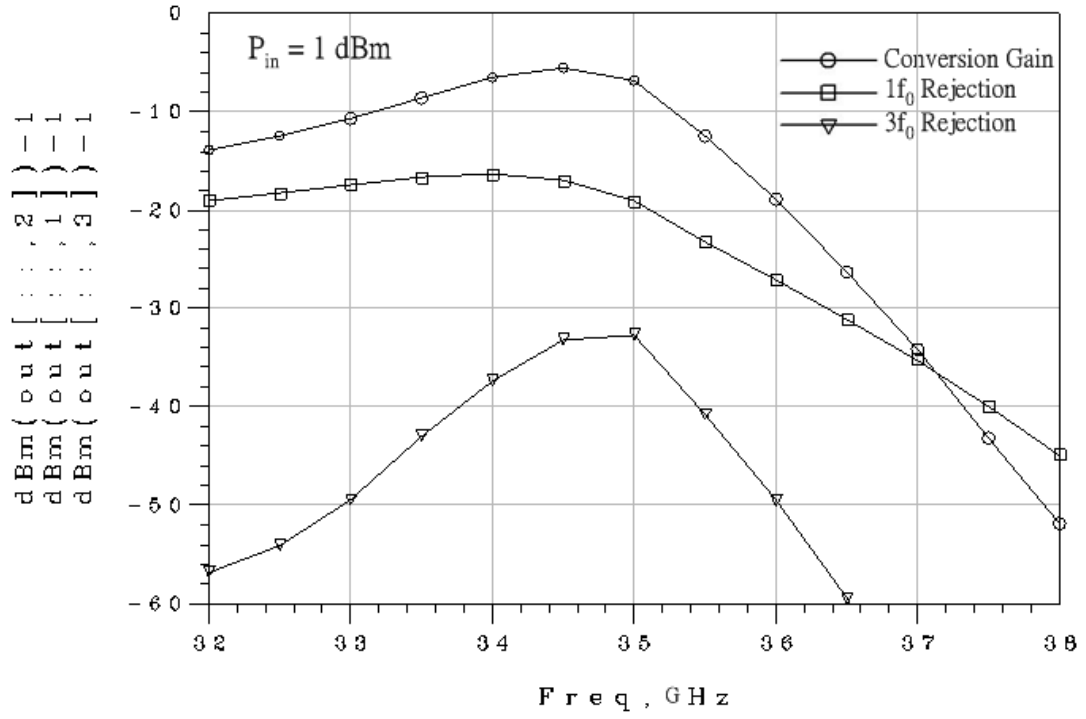
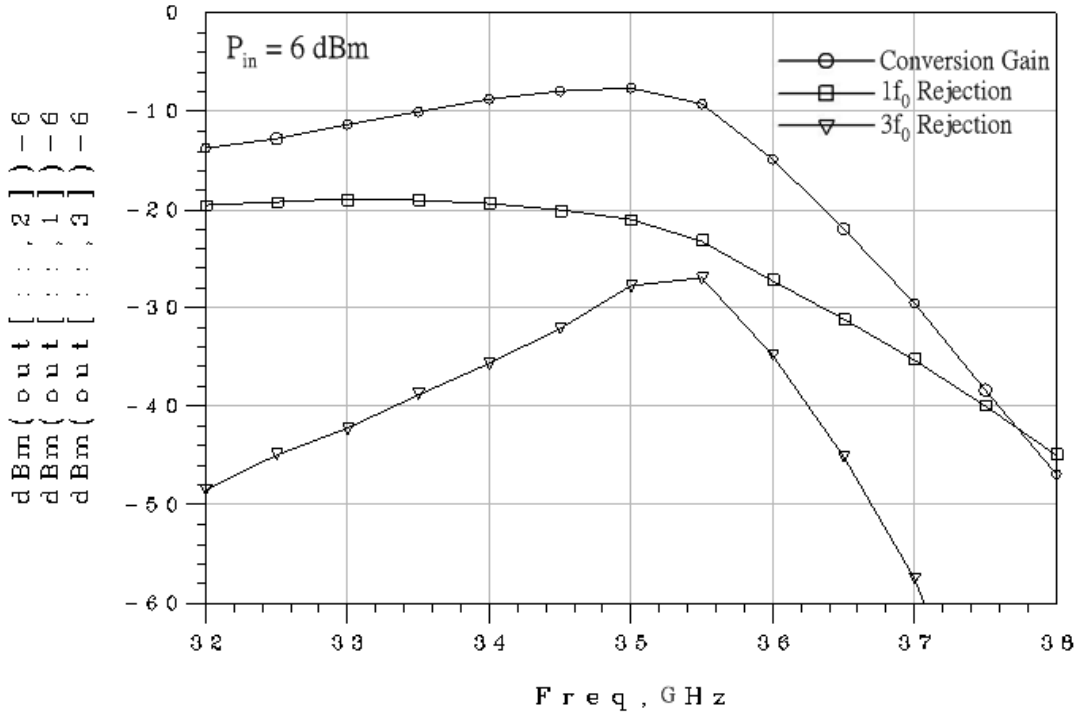


Fig. 3.4 The simulated output power versus input power of the 35-to-70 GHz frequency doubler.

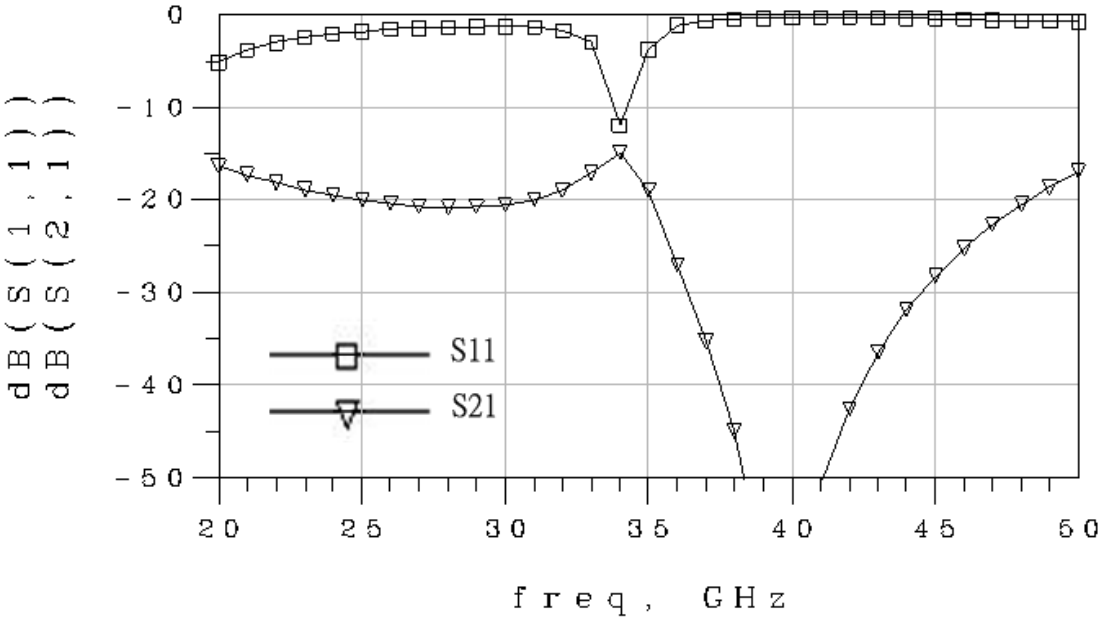


(a)

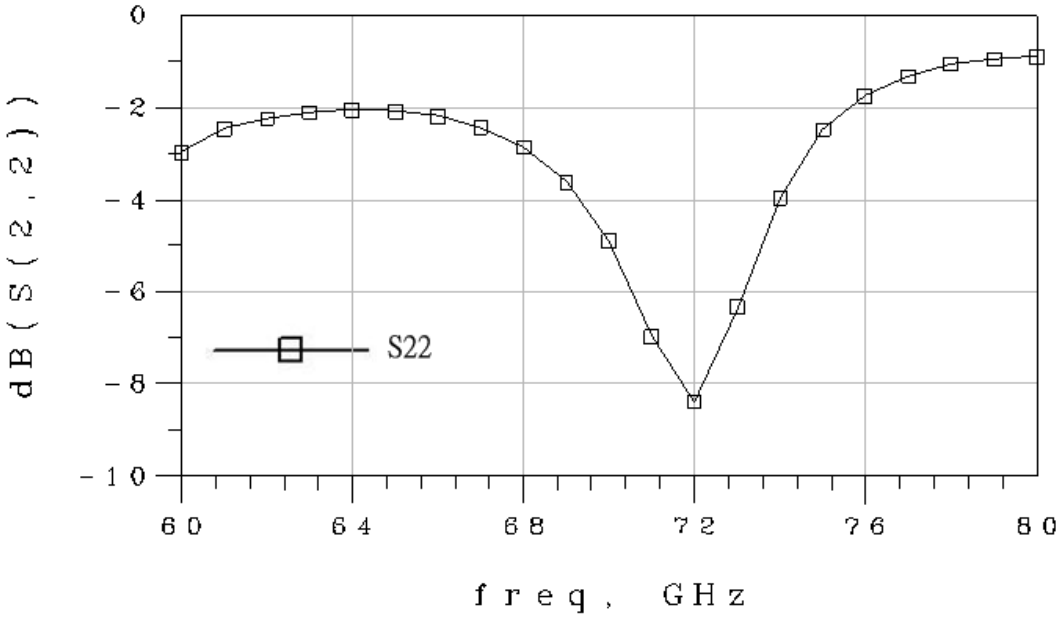


(b)

Fig. 3.5 The simulated conversion gain, $1f_0$ and $3f_0$ rejection versus frequency of the 35-to-70 GHz frequency doubler at (a) P_{in} = 1dBm, (b) P_{in} = 6dBm.



(a)



(b)

Fig. 3.6 The simulated small-signal S-parameters of the 35-to-70 GHz frequency doubler. (a) From 20 to 50 GHz for S11 and S21, (b) from 60 to 80 GHz for S22.

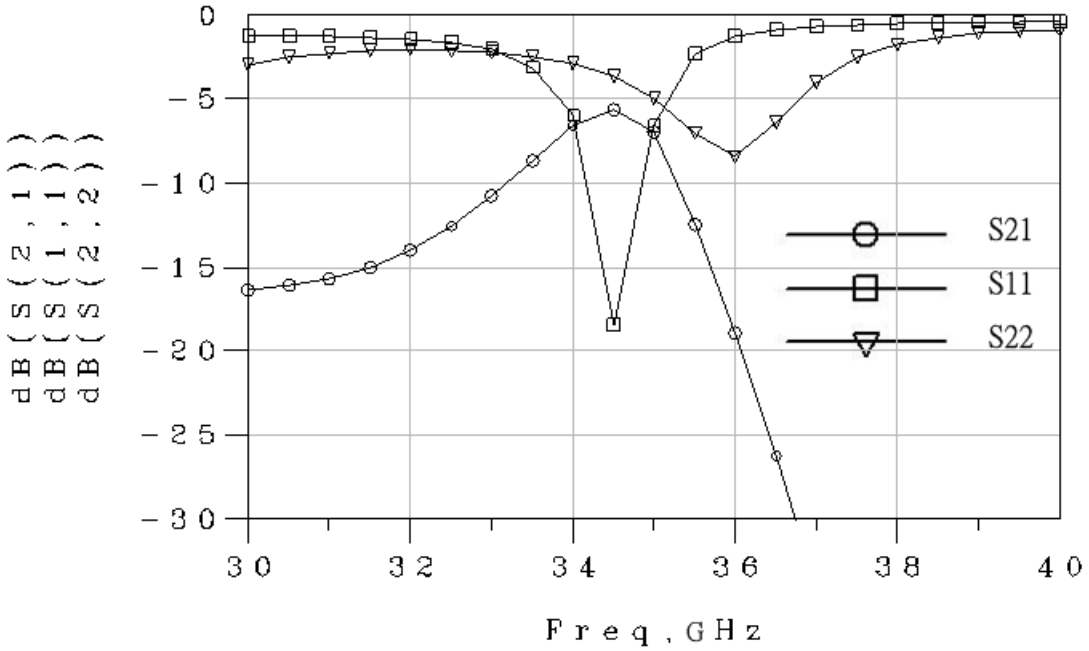


Fig. 3.7 The simulated large-signal S-parameters of the 35-to-70 GHz frequency doubler from 30 to 40 GHz for S11, S21 and S22.

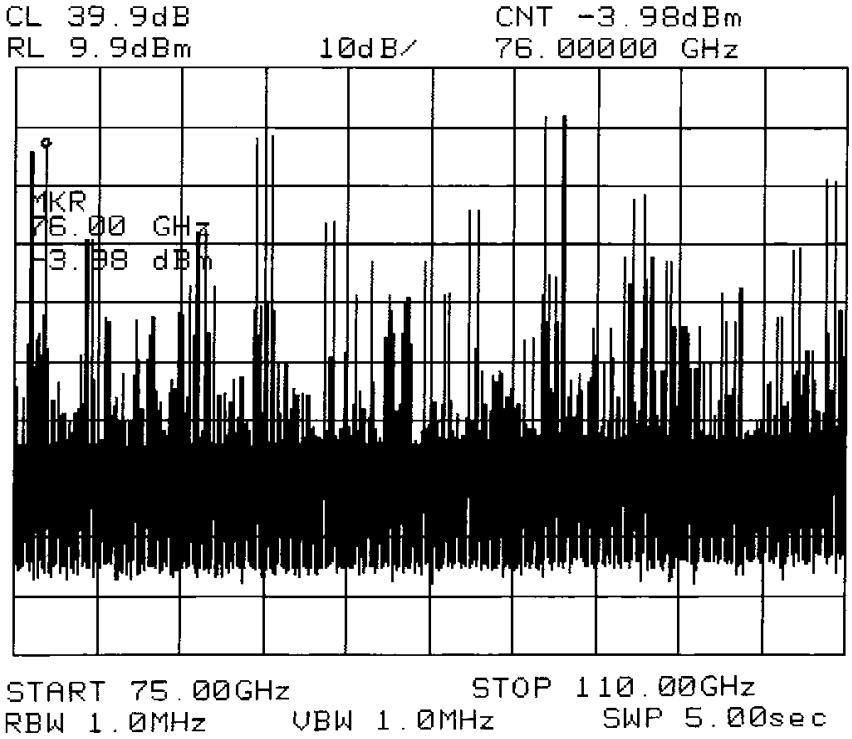
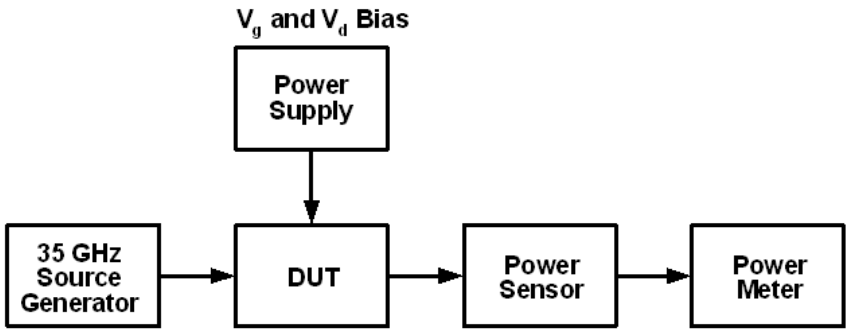
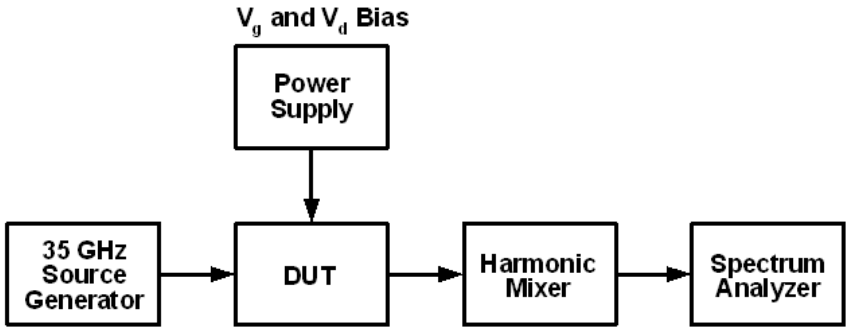


Fig. 3.8 Signal responses produced by a 76 GHz signal in W-band.



(a)



(b)

Fig. 3.9 The test setups for the 35-to-70 GHz frequency doubler characterization. (a) Power measurement, (b) stability assurance.

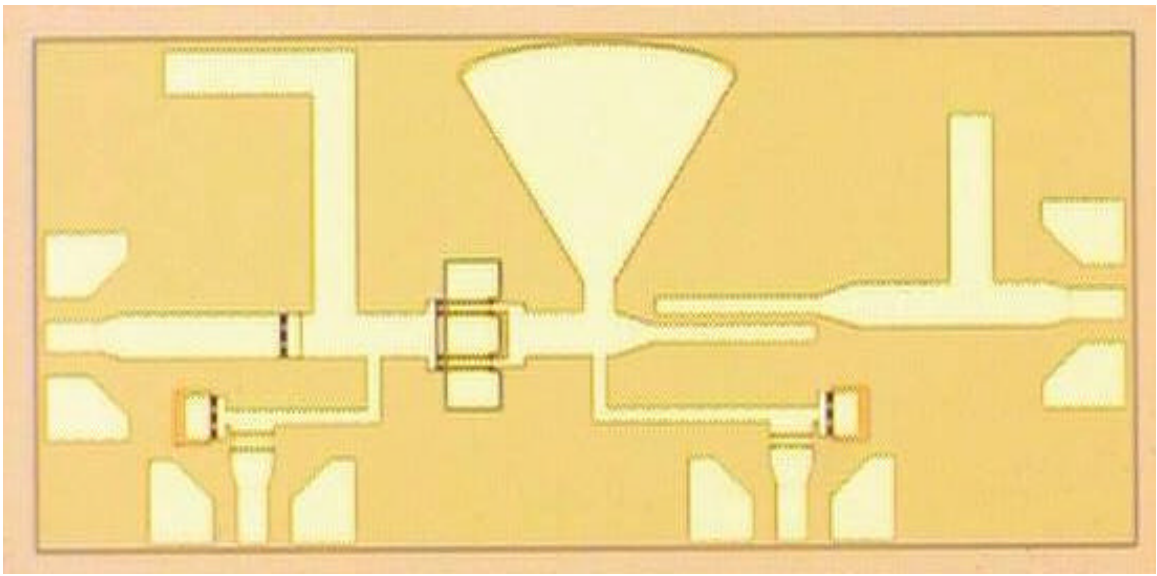


Fig. 3.10 The microphotograph of the 35-to-70 GHz frequency doubler.

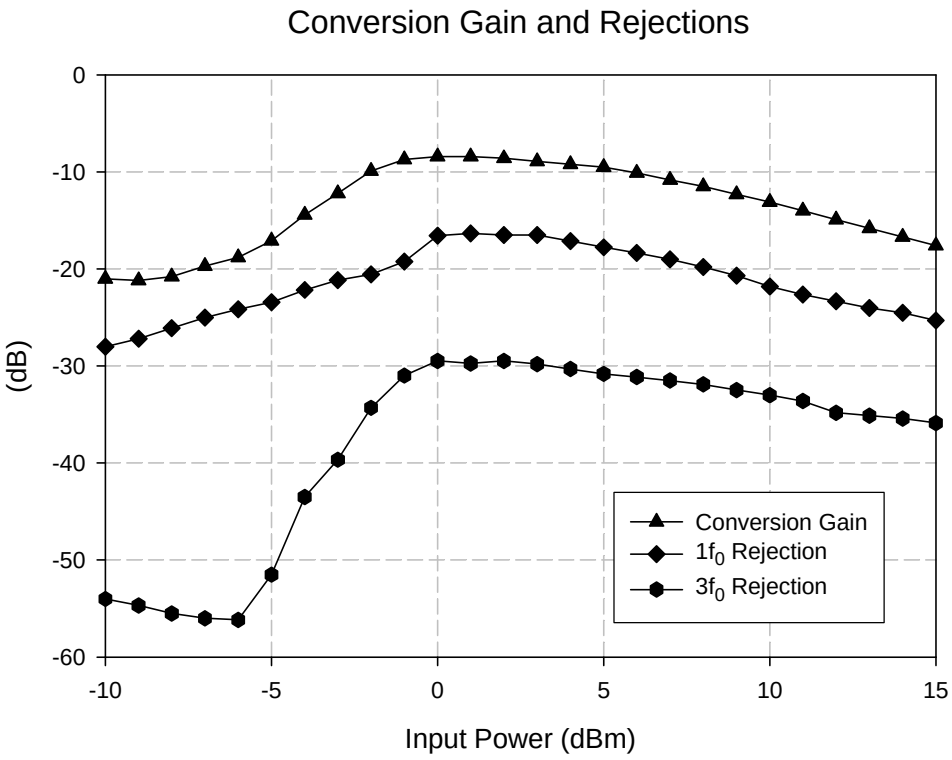


Fig. 3.11 The measured conversion gain, $1f_0$ and $3f_0$ rejection versus input power of the 35-to-70 GHz frequency doubler.

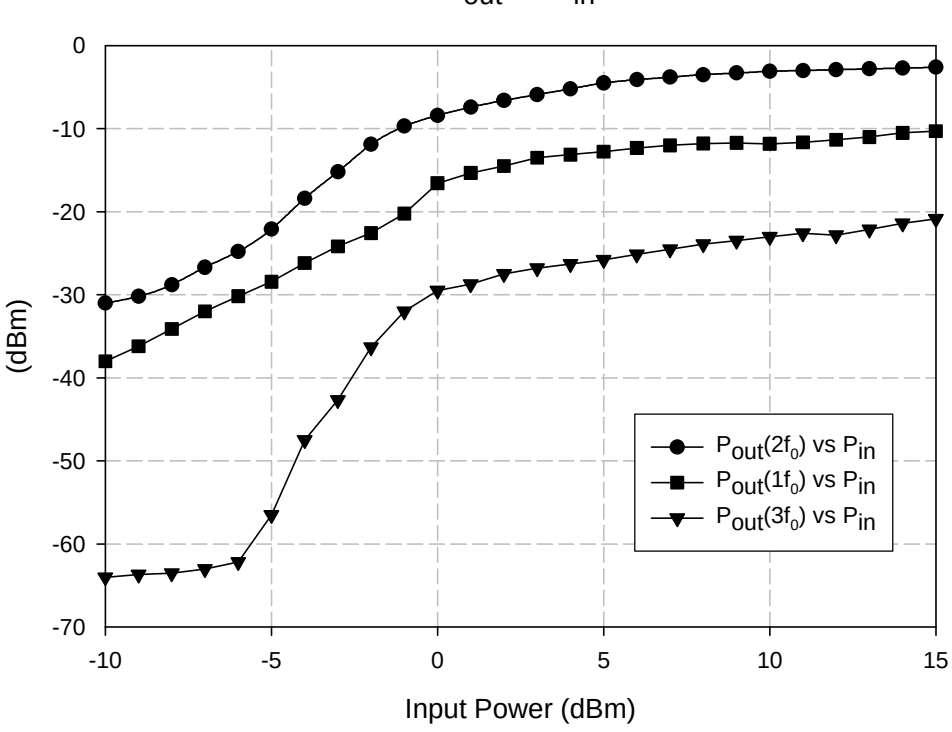
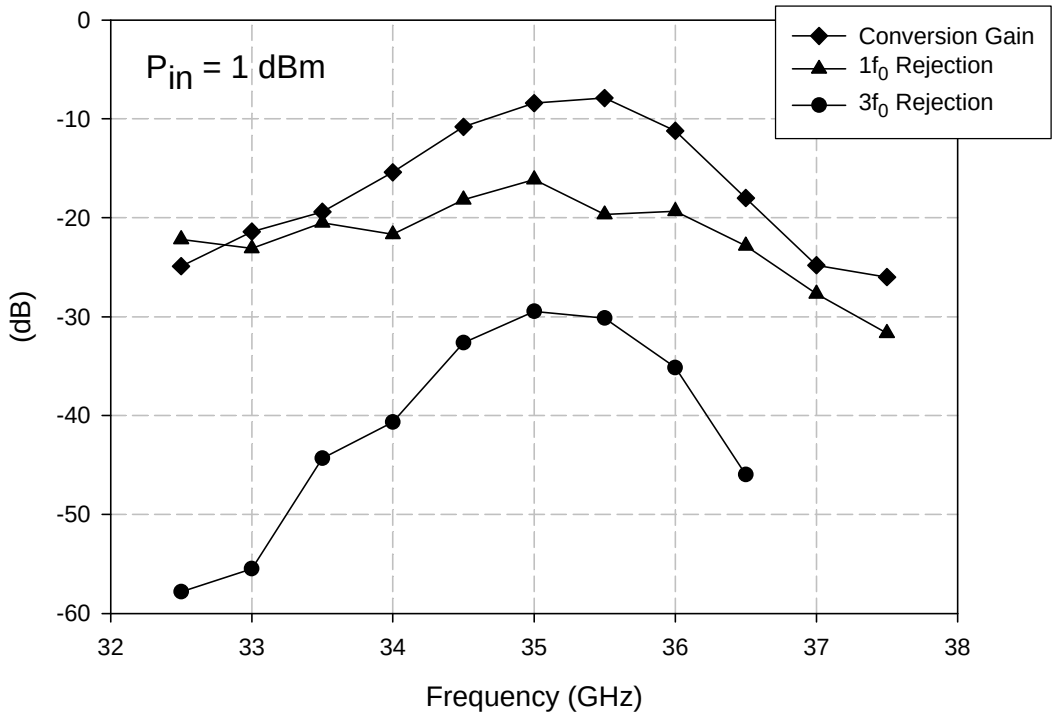
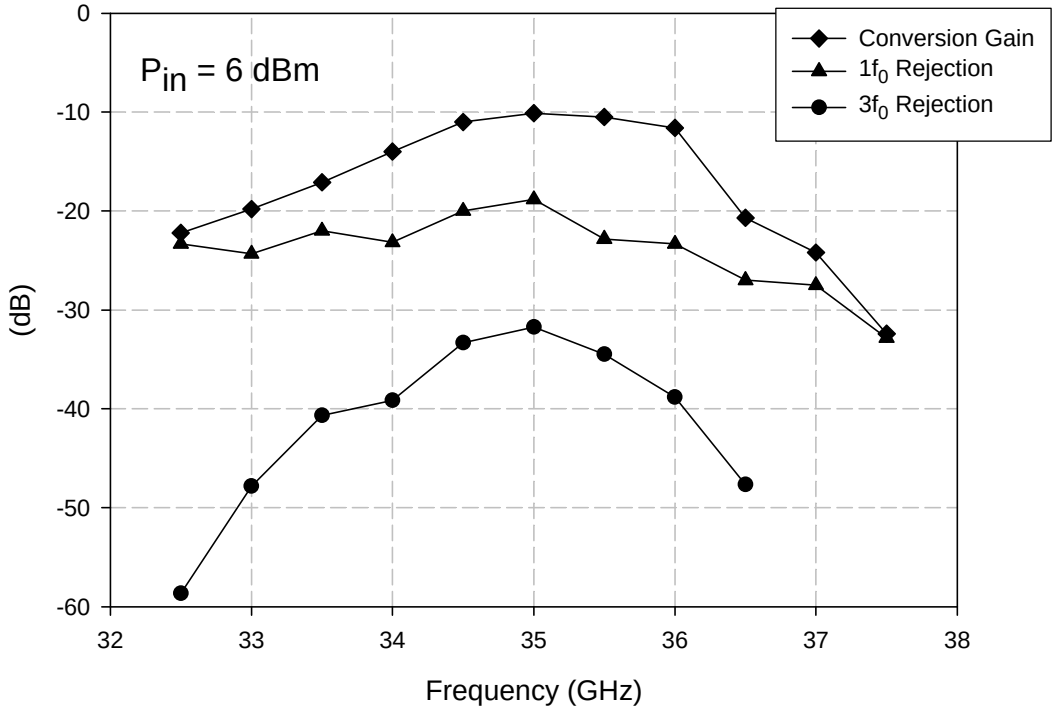


Fig. 3.12 The measured output power versus input power of the 35-to-70 GHz frequency doubler.

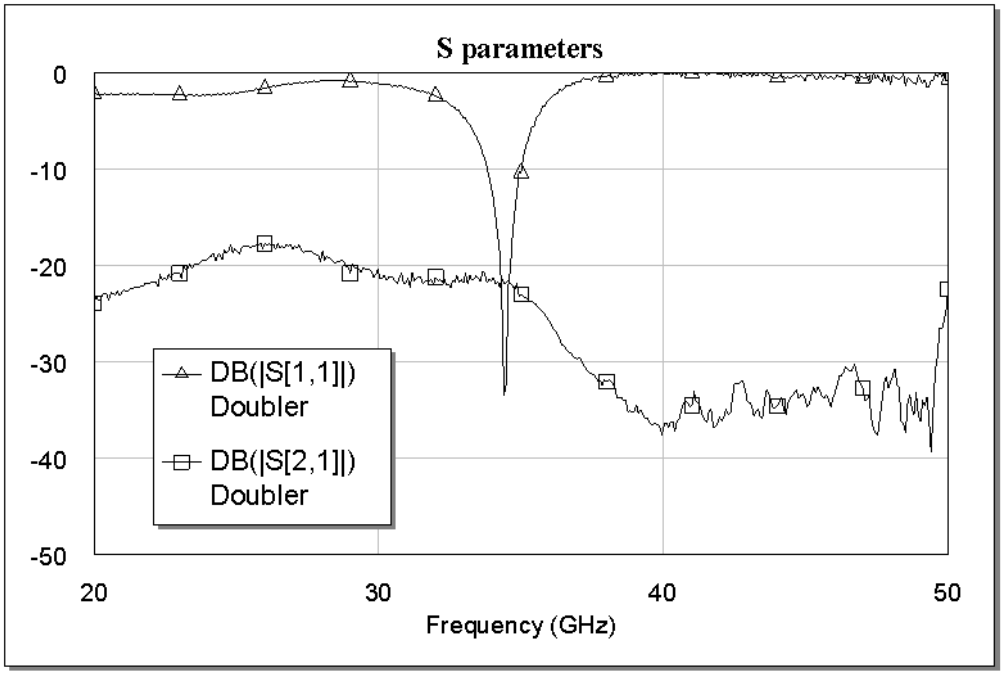


(a)

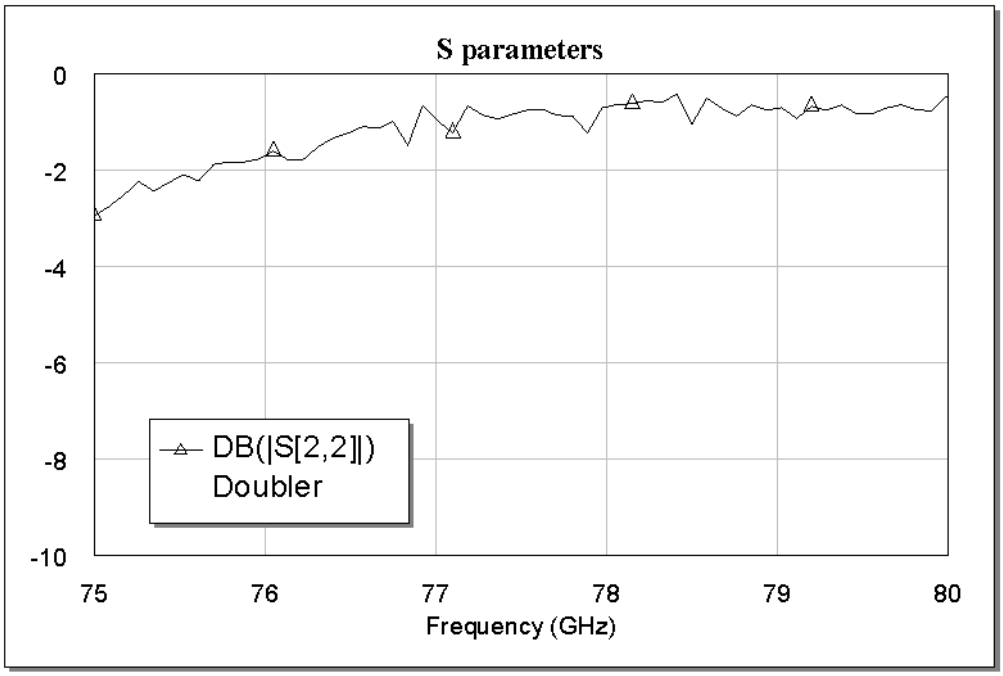


(b)

Fig. 3.13 The simulated conversion gain, $1f_0$ and $3f_0$ rejection versus frequency of the 35-to-70 GHz frequency doubler at (a) P_{in} = 1dBm, (b) P_{in} = 6dBm.



(a)



(b)

Fig. 3.14 The measured small-signal S-parameters of the 35-to-70 GHz frequency doubler. (a) From 20 to 50 GHz for S11 and S21, (b) from 75 to 80 GHz for S22.

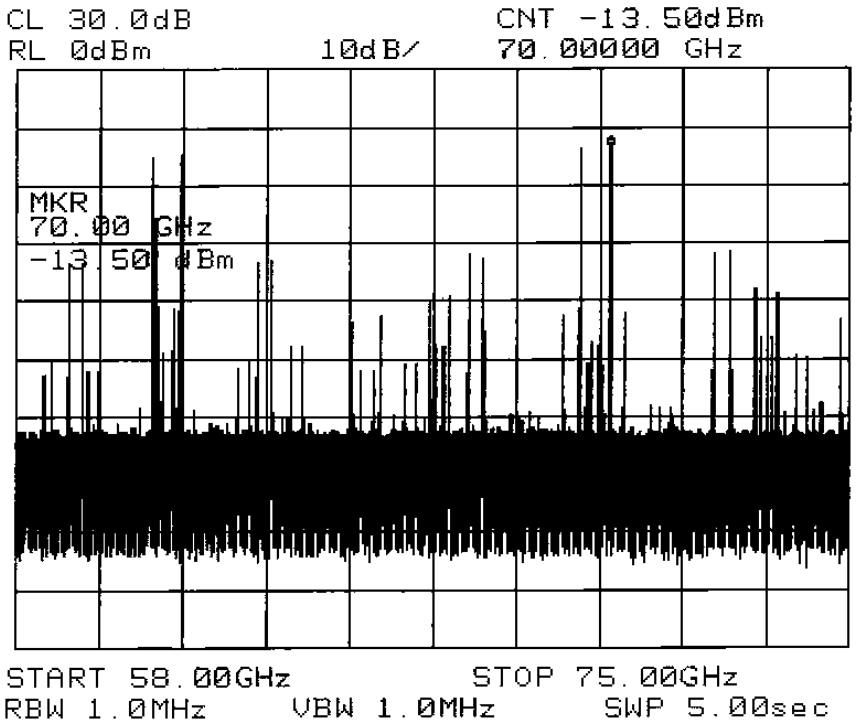


Fig. 3.15 Frequency spectrum from 58 to 75 GHz produced by a 70 GHz signal.

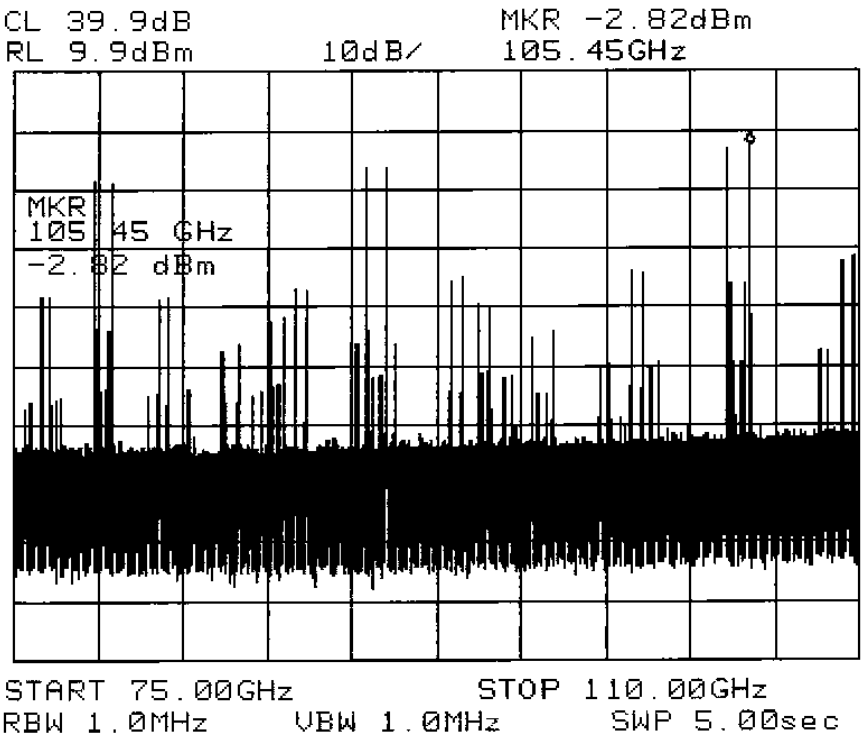
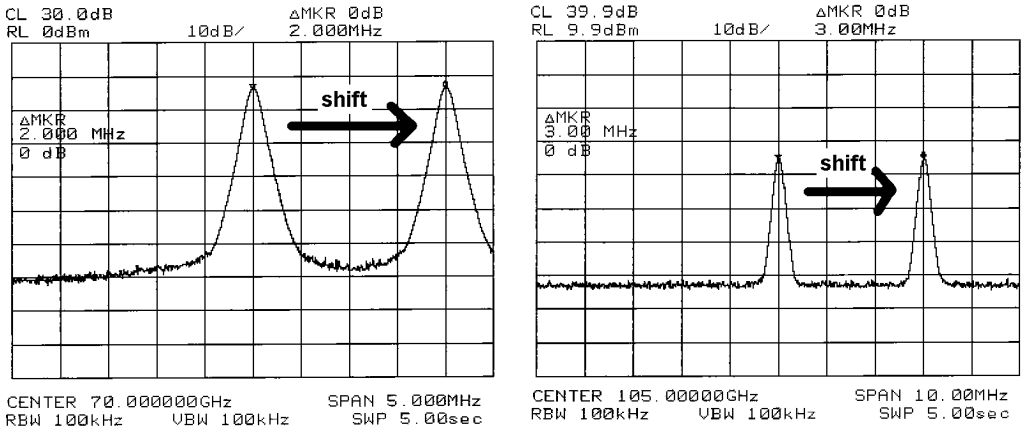
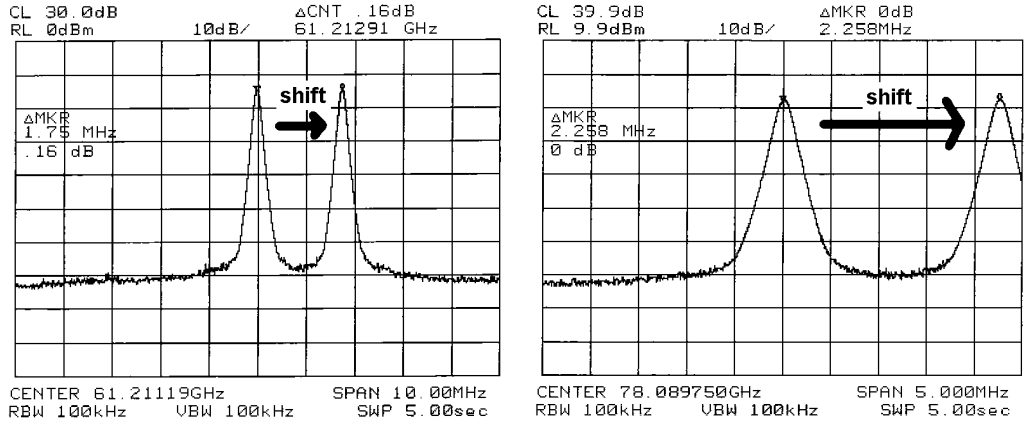


Fig. 3.16 Frequency spectrum from 75 to 110 GHz produced by a 105 GHz signal.

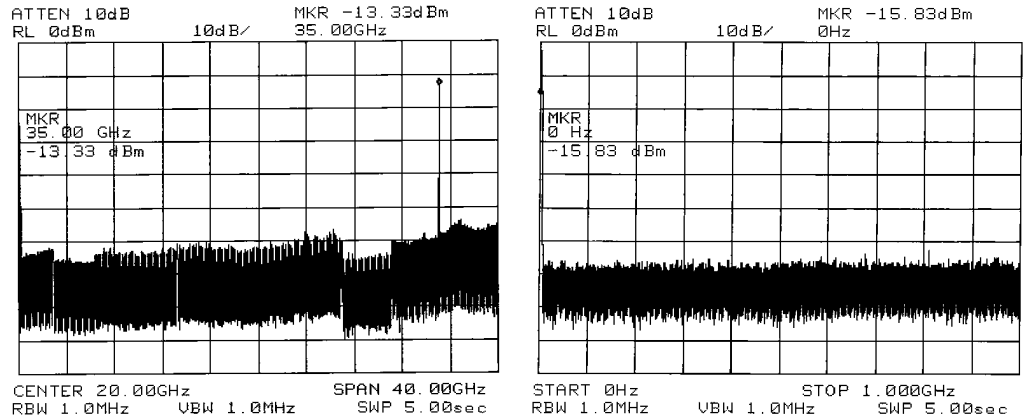


(a) (b)



(c) (d)

Fig. 3.17 (a) A 70 GHz real signal, (b) a 105 GHz real signal,
(c) a 61.2 GHz spurious signal, (d) a 78.09 GHz spurious signal.



(a) (b)

Fig. 3.18 Frequency spectrum produced by a 35 GHz leakage signal,
(a) from 0 to 40 GHz, (b) from 0 to 1 GHz.

Chapter 4

DESIGN METHODOLOGY OF BROADBAND SWITCHES

4.1 Overview

A switch can be applied to perform the multiple accesses, which is widely used and considered as a major choice in communications. It also reduces the duplicate of the circuits with identical functions. In the low frequency below several GHz, the design of switches merely concerns the parasitics and transmission-line effects. On the contrary, these effects appear significantly in the millimeter-wave frequency range and must be taken into account in the switch design. This chapter has a full discussion on the design methodology of broadband switches and presents the Fisher's equivalence [11] in order to broaden the bandwidth of switches.

4.2 Switching Devices

Two types of devices used commonly in the control circuits are PIN diodes and FETs. Before looking at the circuit design methods, we briefly review the significant properties of these devices.

PIN Diodes A PIN diode is a pn junction device that has a very minimally doped or intrinsic region located between the p-type and n-type contact regions as illustrated in Fig. 4.1(a). The addition of the intrinsic or i-region results in characteristics that is very superior for certain device applications. In reverse bias the intrinsic region results in very high values for the diode breakdown voltage, whereas the device capacitance is reduced by the increased separation between the p- and n-region. In forward bias the conductivity of the intrinsic region is controlled or modulated by the injection of charge from the end regions. A practical PIN diode

consists of a lightly doped p- or n-region between the highly doped p-type and n-type contact regions, as shown in Fig. 4.1(b) and Fig. 4.1(c). To identify very lightly doped p and n material, the Greek letters are used; consequently, lightly doped p material is called *p*-type and lightly doped n material is called ?-type. The diode is a bias-current-controlled resistor with preferable linearity and low distortion. PIN diodes can provide faster switching speed and can handle medium to large RF power levels. They also make excellent RF switches, phase shifters and limiters. Sometimes the Schottky barrier diode (SBD) is applied for faster switching speed.

FETs In recent years PIN diode switches have been increasingly replaced by FETs based monolithic switches, especially for low to medium power applications. The FET switches are three-terminal devices, in which the gate bias voltage V_g controls the states of the switch. The FET acts as a voltage-controlled resistor, in which the gate bias controls the drain-to-source resistance in the channel. The intrinsic gate-to-source and gate-to-drain capacitances and device parasitics limit the performance of the FET switches at higher frequencies. In switching applications, a low-impedance (nearly short) state is obtained by making the gate voltage equal to zero. When the negative gate-source bias is larger than the pinch-off voltage in magnitude, the FET is in a high-impedance (nearly open) state. Fig. 4.2 shows these two linear operational regions of the FET graphically [12]. Fig. 4.3 indicates the configuration of a switching FET [13]. A low-impedance state can be adequately modeled by a DC “on” resistance (R_{on}) which is series connection to a parasitic inductor (L_{on}) between the source and the drain as depicted in Fig. 4.4(a). Additional parasitic elements exist, but have no influential RF effects, particularly if the gate bias circuitry is isolated with a large value resistor (R_{iso}), as is indicated in Fig. 4.3. A complete equivalent circuit in a high-impedance state is illustrated in Fig. 4.4(b). This equivalent circuit is based on the device geometry and has been

described previously in [12], [14]. The off-state drain-to-source leakage resistance (R_{ds}) is generally large enough to be neglected in circuit modeling. The drain and the source are directly capacitive-coupled (C_{ds}) and also through the gate (C_{gs} and C_{gd}). All of these capacitances have series parasitic resistive elements (R_{gs} and R_{gd} for C_{gs} and C_{gd}; R_s and R_d for C_{ds}). A simplified FET model can be used without sacrificing accuracy as shown in Fig. 4.5(a) and Fig. 4.5(b). The parasitic inductor was neglected for the on-state equivalent circuit. The off-state equivalent circuit has been reduced to a simple series resistor (R_{off}) and capacitor (C_{off}). For the simplification, it is assumed that the magnitudes of the reactances of the various capacitances are much greater than the various parasitic resistances. This assumption yields the following relationships:

$$R_{off} \approx \frac{R_{gs}+R_{gd}}{[1+\frac{C_{ds}}{(C_{gs}+C_{gd})}]^2} + \frac{R_s+R_d}{[1+\frac{(C_{gs}+C_{gd})}{C_{ds}}]^2} \tag{4.1}$$

$$1/C_{off} \approx \frac{1/(C_{gs}+C_{gd})}{[1+\frac{C_{ds}}{(C_{gs}+C_{gd})}]^2} + \frac{1/C_{ds}}{[1+\frac{(C_{gs}+C_{gd})}{C_{ds}}]^2} \quad . \tag{4.2}$$

Note that these relationships for R_{off} and C_{off} are frequency independent. The additional terms that have been ignored are frequency dependent. It is important to note that virtually no DC power is required by the FET switches in either state. The other advantage of FET switches is that additional biasing circuits are unnecessary because of the natural DC isolation between gate and drain (or source). The negligible DC power consumption and DC biasing isolation of the FET switches are superior to the PIN diode switches.

4.3 Broadband Switch Design

4.3.1 Basic Switch Configurations

There are two basic configurations [15] that may be used for a simple switch designed to control the flow of millimeter-wave signals along a transmission line. One is series-type switch and the other is shunt-type switch. The third configuration that consists of the combination of the series-type and shunt-type switches is called series-shunt switch.

Before we go into the details, two essential parameters of switches must be specified. Insertion loss (IL) is defined as the ratio of the power delivered to the load in the on-state of the ideal switch to the actual power delivered by the practical switch. It is usually expressed in decibels. Isolation is a measure of the performance for the switch when it is in the off-state. Isolation (ISO) is defined as the ratio of the power delivered to the load for an ideal switch in the on-state to the actual power delivered to the load when the switch is in the off-state.

Series-type Switches Fig. 4.6(a) illustrates the equivalent circuit of a series-type switch. The low-impedance state of the FET allows the signal to propagate, while in the high-impedance state, the incident power on the switch is mostly reflected back. Accordingly, the low- and high-impedance states of the FET are called on-state and off-state for a series-type switch. The insertion loss may be calculated by considering the equivalent circuit depicted in Fig 4.6(b). If V_L denotes the actual voltage across the load in the ideal switch, the insertion loss may be written as

$$IL = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{R_{low}}{Z_0} + \frac{1}{4}\left(\frac{R_{low}}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X_{low}}{Z_0}\right)^2 \quad , \tag{4.3}$$

where $Z_{low} = R_{low} + jX_{low}$ is the impedance of the switching device in the low-impedance state. Similarly, the isolation is given as

$$ISO = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{R_{high}}{Z_0} + \frac{1}{4}\left(\frac{R_{high}}{Z_0}\right)^2 + \frac{1}{4}\left(\frac{X_{high}}{Z_0}\right)^2 \quad , \tag{4.4}$$

where $Z_{high} = R_{high} + jX_{high}$ is the impedance of the switching device in the high-impedance state.

Shunt-type Switches Fig. 4.7(a) illustrates the equivalent circuit of a shunt-type switch. The shunt-type switch is complement to the series-type switch. The low-impedance state of the FET almost reflects the incident power back and the high-impedance state permits the signal to propagate. Therefore, the low- and high-impedance states of the FET are called off-state and on-state for a shunt-type switch. The insertion loss may also be calculated by considering the equivalent circuit depicted in Fig 4.7(b). If V_L denotes the actual voltage across the load in the ideal switch, the insertion loss may be written as

$$IL = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{G_{high}}{Y_0} + \frac{1}{4}\left(\frac{G_{high}}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B_{high}}{Y_0}\right)^2 \quad , \tag{4.5}$$

where $Y_{high} = G_{high} + jB_{high}$ is the admittance of the switching device in the high-impedance state. Furthermore, the isolation is given as

$$ISO = \left|\frac{V_L}{V_{LD}}\right|^2 = 1 + \frac{G_{low}}{Y_0} + \frac{1}{4}\left(\frac{Y_{low}}{Y_0}\right)^2 + \frac{1}{4}\left(\frac{B_{low}}{Y_0}\right)^2 \quad , \tag{4.6}$$

where $Y_{low} = G_{low} + jB_{low}$ is the admittance of the switching device in the low-impedance state.

Series-Shunt Switches The simplest series-shunt switching configuration is indicated in Fig. 4.8(a). This switching circuit may be analyzed in terms of the equivalent circuit as shown in Fig. 4.8(b). For the on-state, the device impedance Z_{se} is denoted by the low impedance Z_{low}, and the device impedance Z_{sh} is denoted by

the high impedance Z_{high}. From the simple circuit analysis, the insertion loss may be written as

$$IL = \left| \frac{1}{2} + \frac{(Z_0 + Z_{high})(Z_0 + Z_{low})}{2Z_0 Z_{high}} \right|^2 \quad . \tag{4.7}$$

Similarly, the isolation is written as

$$ISO = \left| \frac{1}{2} + \frac{(Z_0 + Z_{low})(Z_0 + Z_{high})}{2Z_0 Z_{low}} \right|^2 \quad . \tag{4.8}$$

It may be noted that if the non-identical devices are used in the series and the shunt locations, values of Z_{high} and Z_{low} in (4.7) could be different from those in (4.8).

In general, the isolation obtained by using a series-shunt configuration is much better (more than twice in decibels) than that for either the series-type or shunt-type switch. The insertion loss for the series-shunt configuration is worse than that for a shunt-type switch but better than that for a series-type switch.

4.3.2 Single-Pole Single-Throw Switch

A single-pole single-throw (SPST) switch is used to control the flow of signals along a transmission line. As mentioned above, three basic configurations can be adopted to design the SPST switch. In the millimeter-wave frequency range, the device parasitics introduce more significantly unfavorable effects either on insertion or isolation performance. Some well-known compensated techniques, like capacitive [16] or impedance-transformation methods [17], can be utilized to minimize the non-ideal open or non-ideal short effects. Even a traveling-wave concept was applied in SPST switch design [18].

In 1965, R. E. Fisher [11] has suggested that the diode capacitance and its parallel resonating stub tuner could be analyzed approximately as a simple stub. J. F.

White [19] demonstrates the feasibility of Fisher's equivalence for low frequencies from 1 to 2 GHz in 1968. In this thesis, Fisher's equivalence is also adopted except that the switching devices are replaced by FETs and the frequencies are extended to the millimeter-wave frequency range.

Fig. 4.9 illustrates the circuit model used for Fisher's equivalent circuit. The following equation gives the relationship between Y_E, Y_T , θ_T and the diode capacitance C.

$$Y_E = \frac{2}{p}\left\{w_0 C + Y_T\left[\cot^{-1}\left(\frac{w_0 C}{Y_T}\right)\right]\left[1+\left(\frac{w_0 C}{Y_T}\right)^2\right]\right\} \qquad (4.9)$$

Fig. 4.10 plots Y_T and θ_T versus $\omega_0 C/Y_E$. For a more accurate estimation, some corresponding variable values for the common steps in the evaluation of $\omega_0 C/Y_E$ are given in Table 4.1. For small normalized susceptance, $\omega_0 C/Y_E$, the required tuning stub is nearly a quarter wavelength long and its normalized admittance, Y_T/Y_E, is nearly unity. The largest allowable value for $\omega_0 C/Y_E$ is p/4. As can be seen from the curves, θ_T and Y_T/Y_E are both equal to zero at this value.

Furthermore, a maximally flat filter, consisting of the quarter-wavelength short-circuited stubs with quarter-wavelength spacing, has been summarized in tabular form by W. W. Mumford [20]. The form of the filter is shown in Fig. 4.11 and Mumford's values for filters with three, four and five elements are tabulated in Table 4.2. The filters are symmetrical and consequently only the normalized admittances for the first stub to the center are listed.

For a broadband SPST switch design, the parasitics of FETs in the low-impedance state are usually unconcerned and can simply be ignored. In the high-impedance state, the parasitic capacitances of FETs have more significant effects, but they can also be incorporated into the equivalent quarter-wavelength

short-circuited stubs, as illustrated in Fig. 4.12, to broaden the bandwidth of SPST switches. To be more specific, a wide bandwidth of the maximally flat filter can be created via the design tables or calculations by hands first. The parasitic capacitances of FETs can be equivalent to the capacitors modeled in the Fisher's equivalence and be transformed to the quarter-wavelength short-circuited stubs used in the previously wideband filter. Therefore, an arbitrarily broadband SPST switch can be formed with an appropriate design through the technique of capacitances absorption.

4.3.3 Single-Pole Double-Throw Switch

Fig. 4.13(a) and Fig. 4.13(b) show the series-type and shunt-type circuits for a single-pole double-throw (SPDT) switch; the switch demands at least two switching devices. In operation, one FET is biased in the low-impedance state, while the other FET is biased in the high-impedances state. The input signal is switched from one output to the other by reversing the FET states. The bandwidth of the SPDT switch in shunt configuration is restricted because of the quarter-wavelength transmission line, which is required between the transmission line junction and the locations of the two switching devices.

Fisher also suggested that a SPDT shunt diode tee switch can be realized using the stub filter approach; such a method is depicted in Fig. 4.14(a). The diodes are located a quarter-wavelength apart from the input in each of two output arms. The off-arm has a nearly short circuit produced by the forward biased diode, which results in a quarter-wavelength short-circuited stub shunted with the transmission path to the on-arm. As shown in Fig. 4.14(b), this stub must have the characteristic admittance, Y_0, of the through line since it represents a transmission path when it becomes an on-arm.

To be more definite, the parasitic capacitances of FETs, in the high-impedance state, can also be incorporated into the equivalent quarter-wavelength short-circuited stubs used in the previously wideband filter as described in Section 4.3.2. This design is distinct from the conventional ones, in which the bandwidth is restricted because of the quarter-wavelength transmission line which is required between the transmission line junction and the locations of the two switching devices. The extra quarter-wavelength transmission line can be incorporated into the transmission path for the on-arm as indicated in Fig 4.14(b). Consequently, an arbitrarily broadband SPDT switch can be formed with an appropriate design through the technique of capacitances absorption.

4.3.4 Single-Pole m-Throw Switch

The single-pole m-throw (SPmT) switch has a single input, a single output on-arm and (m-1) output off-arms. We proposed that a SPmT shunt-type switch can also be realized using the stub filter approach. The FETs are located a quarter-wavelength apart from the input in each of the m output arms. The (m-1) off-arms have a nearly short circuit produced by the low-impedance FETs, which result in an equivalent quarter-wavelength short-circuited stub with the characteristic admittance of $(m-1)Y_0$ shunted with the transmission path to the on-arm. Each stub must have the characteristic admittance, Y_0, of the through line since it represents a transmission path when it becomes an on-arm. The last of the quarter-wavelength short-circuited stubs for each paths must have the characteristic admittance of $(m-1)Y_0$ which is corresponding to the equivalent quarter-wavelength short-circuited stub resulted from the (m-1) shunted off-arms. Therefore, the bandwidth of this proposed SPmT switch can be almost unrestricted if an appropriate design is employed.

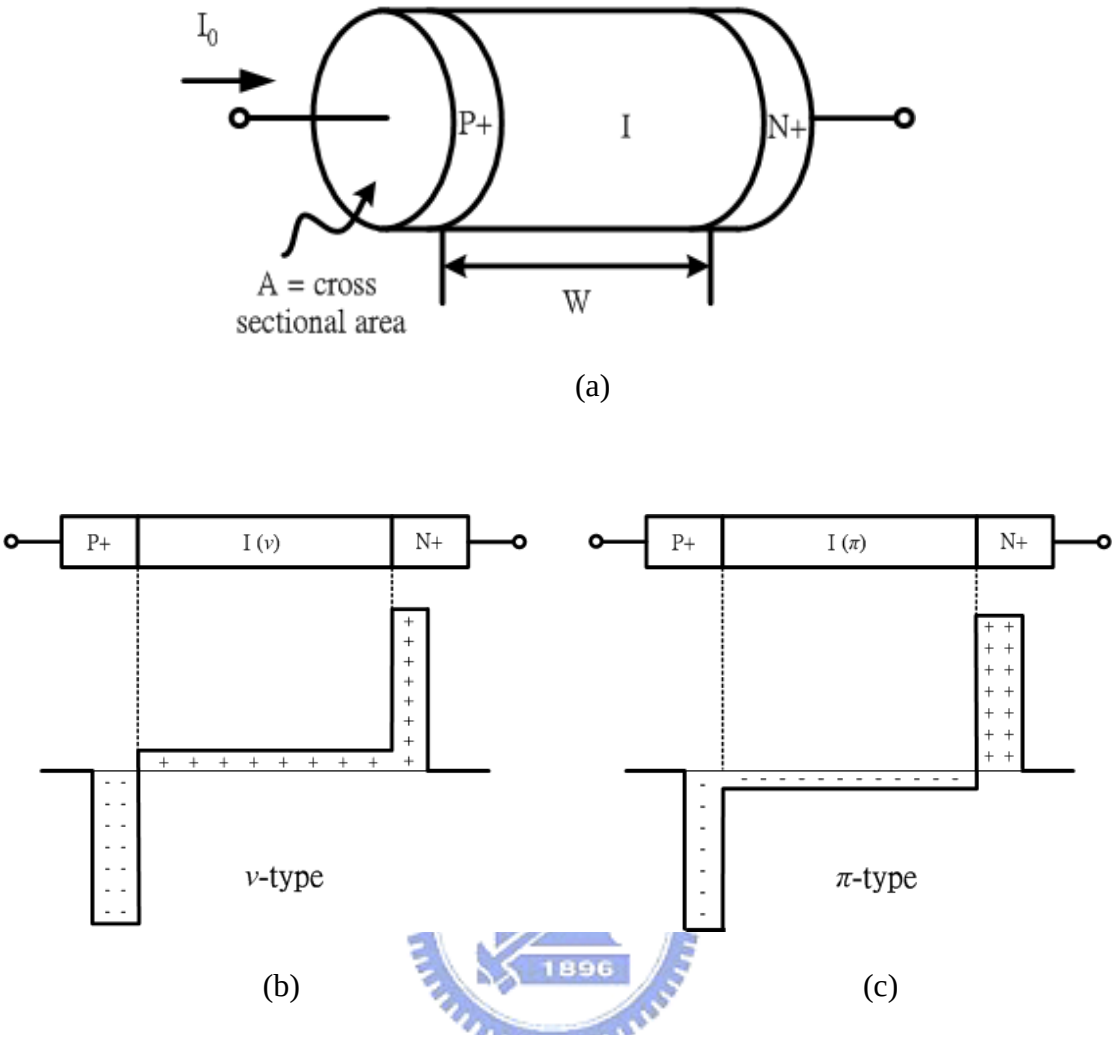


Fig. 4.1 (a) A general structure of the PIN diode, (b) ?-type, (c) *p*-type.

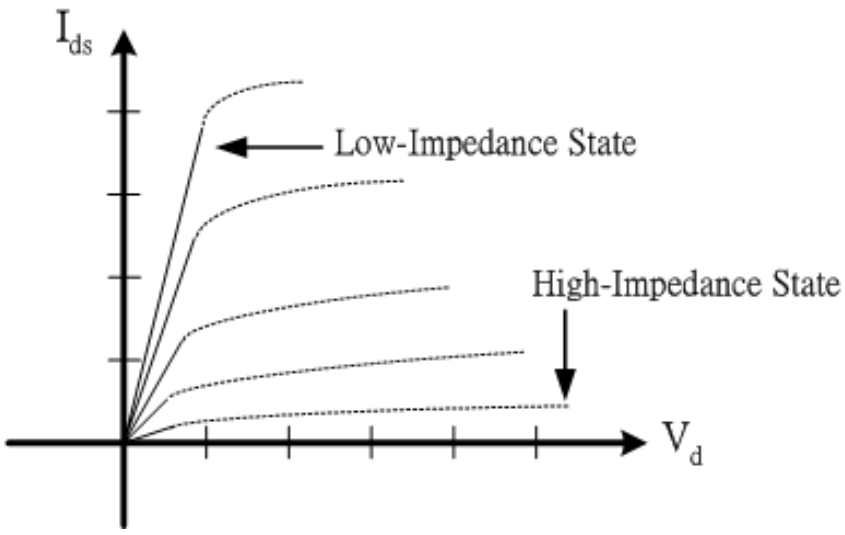


Fig. 4.2 Linear operational regions of a FET switch.

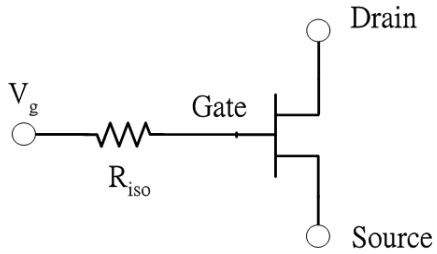


Fig. 4.3 The FET in switching configuration.

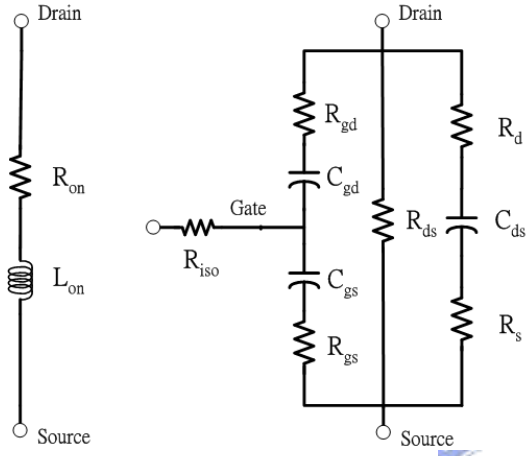


Fig. 4.4 Complete equivalent circuit for,
(a) low-impedance state,
(b) high-impedance state.

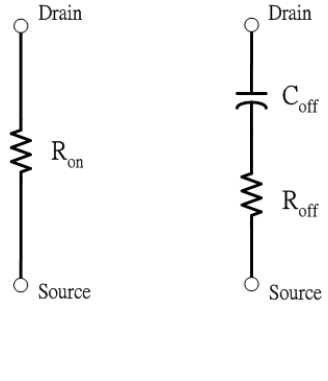
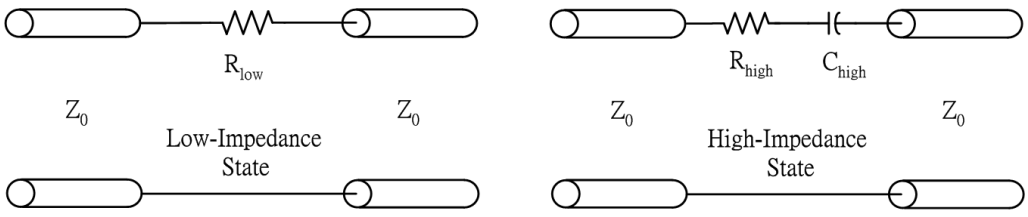
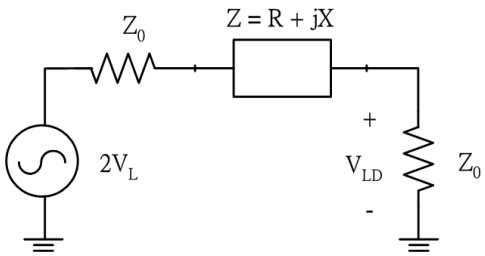


Fig. 4.5 Simplified equivalent circuit for,
(a) low-impedance state,
(b) high-impedance state.

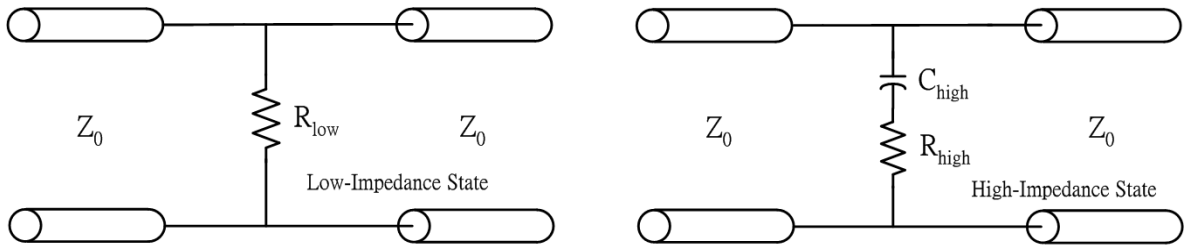


(a)

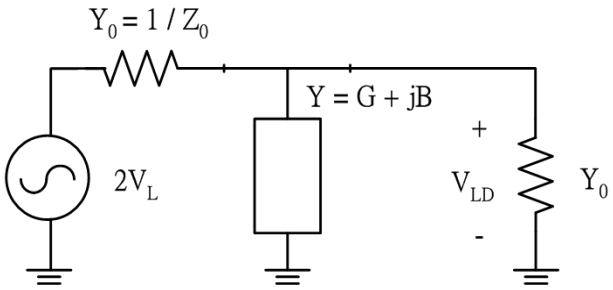


(b)

Fig. 4.6 Series-type switch configuration, (a) transmission line model,
(b) equivalent circuit model.

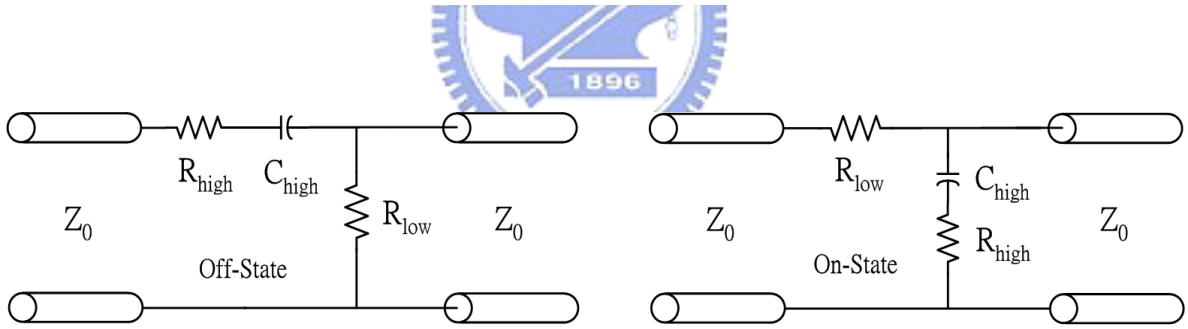


(a)

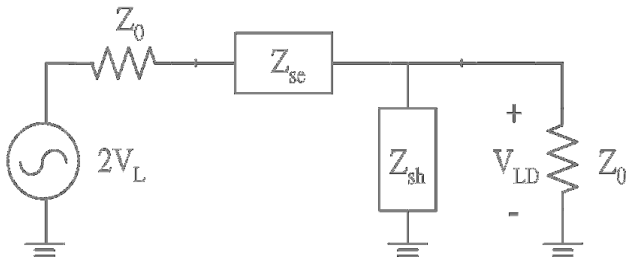


(b)

Fig. 4.7 Shunt-type switch configuration, (a) transmission line model, (b) equivalent circuit model.



(a)



(b)

Fig. 4.8 Series-shunt switch configuration, (a) transmission line model, (b) equivalent circuit model.

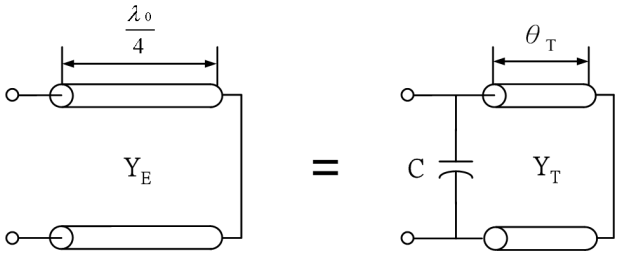


Fig. 4.9 Circuit model used for Fisher's equivalent circuit.

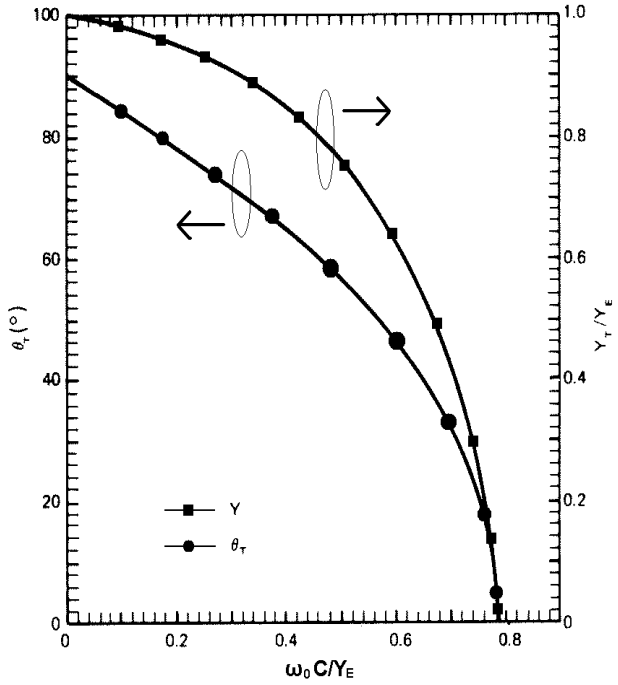


Fig. 4.10 Summary of Fisher's equivalence for simulating a quarter-wavelength stub with a capacitor and its parallel tuner.

$\omega_0 C / Y_E$	Y_T / Y_E	θ_T (degree)
0.000	1.000	90.0
0.100	0.985	84.2
0.200	0.956	78.4
0.300	0.915	71.8
0.400	0.850	64.8
0.500	0.760	56.7
0.600	0.627	46.2
0.700	0.436	31.9
0.750	0.300	21.8
0.780	0.120	8.75
0.7854(π/4)	0.000	0.00

Table 4.1 Tuned capacitor values for simulating a quarter-wavelength stub.

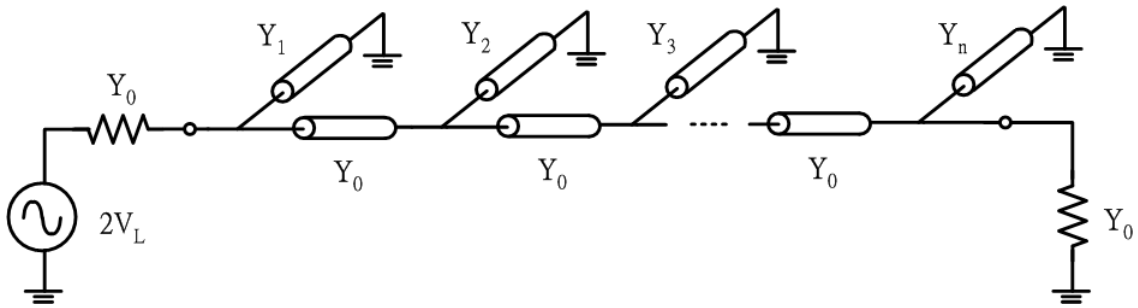


Fig. 4.11 Equivalent circuit for the maximally flat stub filter.

	Y_1 / Y_0	Y_2 / Y_0
Three Stubs	0.100	0.200
	0.300	0.600
	0.500	1.000
	0.700	1.400
	1.000	2.000
	1.400	2.800
	2.000	4.000
	2.500	5.000
	3.000	6.000
Four Stubs	0.100	0.292
	0.200	0.571
	0.400	1.109
	0.800	2.141
	1.300	3.395
	1.900	4.877
	3.000	7.568

	Y_1 / Y_0	Y_2 / Y_0	Y_3 / Y_0
Five Stubs	0.100	0.366	0.532
	0.200	0.694	0.989
	0.300	1.005	1.410
	0.400	1.304	1.808
	0.500	1.596	2.193
	0.700	2.166	2.933
	0.900	2.724	3.648
	1.300	3.819	5.038
	2.000	5.702	7.403
	2.800	7.829	10.058

Table 4.2 Mumford's design tables for the maximally flat stub filters.

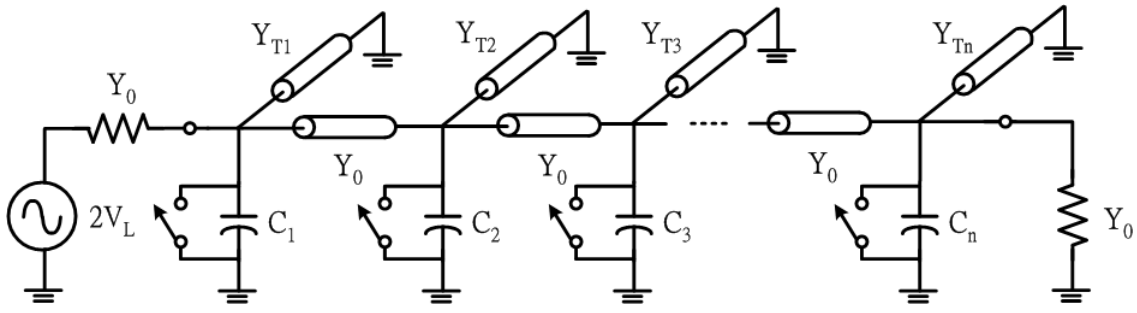


Fig. 4.12 Equivalent circuit for the transmission state of the SPST switch.

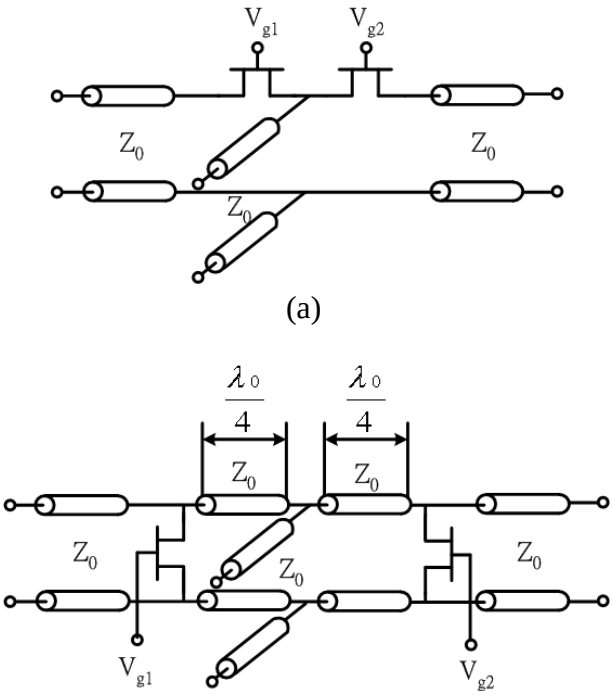


Fig. 4.13 The SPDT switch with, (a) series-type configuration, (b) shunt-type configuration.

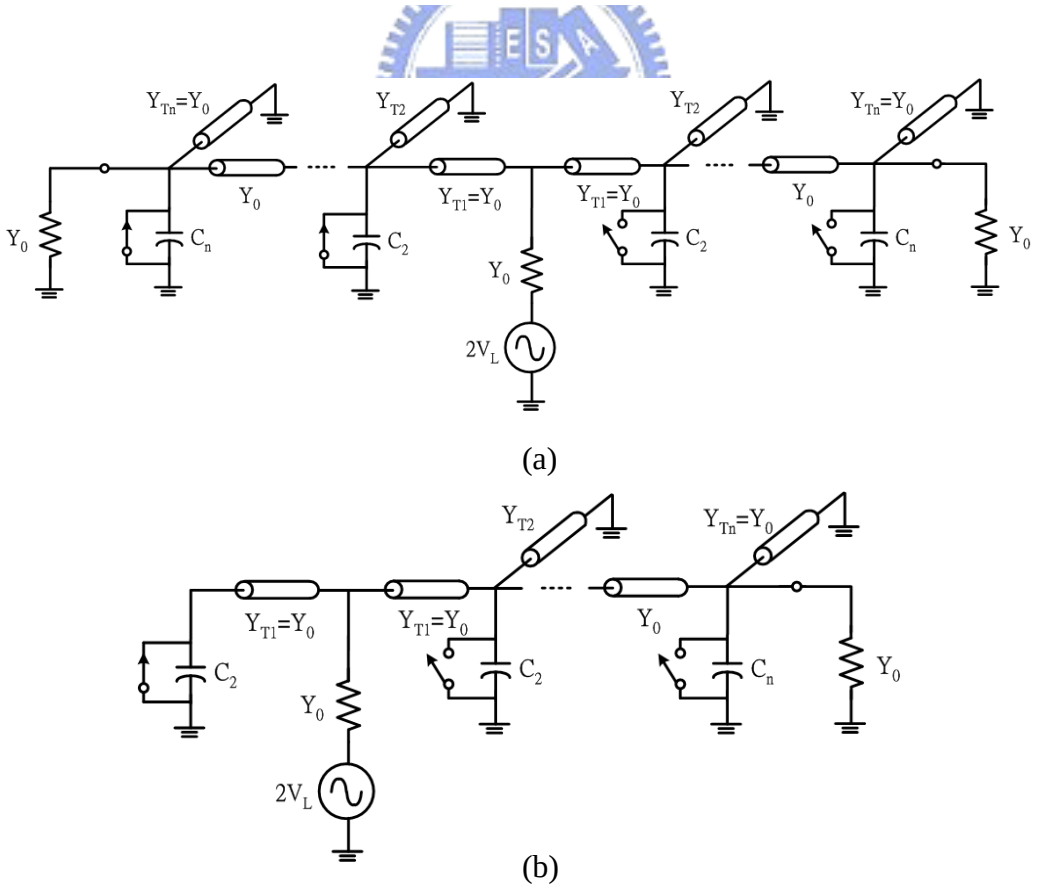


Fig. 4.14 (a) SPDT switch implemented by Fisher's equivalence,
(b) the equivalent filter circuit for the transmission state.

Chapter 5

NEW BROADBAND SWITCHES USING INGAAS PHEMT

5.1 Overview

This chapter exhibits two newly broadband millimeter-wave switches, including a 24-to-65 GHz SPST switch and a 30.5-to-64.5 GHz SPDT switch using InGaAs pHEMT. These circuits are based on the analysis and design methodology described in Chapter 4. The fabrication, design and simulations of the circuits will be presented in the following. The measurement considerations are also specified in detail; furthermore, the measured results are depicted.

5.2 MMIC Foundry Description

The pHEMT device used in this design is fabricated by WIN Semiconductor Corp. with a standard 0.15-um high-power InGaAs pHEMT MMIC process. The process employs a hybrid lithographic approach using direct-write electron beam (E-beam) lithography for sub-micron T-gate definition and optical lithography for the other process steps. The pHEMT devices are grown using molecular beam epitaxy (MBE) on 6-inch semi-insulating (SI) GaAs substrates. The pHEMT device has a typical unit current gain cutoff frequency (f_t) of 85 GHz and maximum oscillation frequency (f_{max}) of 200 GHz. The peak DC transconductance (G_m) at -0.45 V gate-source voltage is 495 mS/mm. The gate-drain breakdown voltage is 10 V, and the maximum drain current at 0.5 V gate-source voltage is 650 mA/mm. Other passive components include thin-film resistor (TFR), mesa-resistor (epitaxial layer), metal-insulator-metal (MIM) capacitors, spiral inductors, and air-bridges. The wafer is thinned to 100 um for the backside metal plating and reactive ion etching

(RIE) via-holes are used for DC grounding.

5.3 24-to-65 GHz Single-Pole-Single-Throw Switch using InGaAs pHEMT

5.3.1 Circuit Design

Fig. 5.1 indicates the schematic diagram of the 24-to-65 GHz SPST switch. In order to maximize the bandwidth of SPST switch, Fisher's method, as described in Section 4.3.2, is applied and extended to the millimeter-wave frequency range. This circuit was designed using microstrip transmission lines. The switching device is an InGaAs pHEMT with 2 x 100 um gate width. A four quarter-wavelength short-circuited stubs filter is utilized to achieve sufficient isolation. Each of the short-circuited stubs shunts with the drain port of the InGaAs pHEMT switching device. Accordingly, the drain is automatically biased at 0 V via the short-circuited stubs. The control gate bias is injected through a thin-film isolation resistor (R_{iso}) and a high-impedance transmission line to reduce the significantly coupling leakage between the drain to gate port for the millimeter-wave signals. A general rule to employ an InGaAs pHEMT as a switching device is to bias the control voltage (V_g) at -2.0 V for the high-impedance state and 0 V for the low-impedance state. A layout of the 24-to-65 GHz SPST switch with chip size of 1.2 x 2 mm^2 is accomplished by the Cadence tools and is depicted in Fig. 5.2. Nevertheless, the actually used chip area is only 1.05 x 1.3 mm^2.

5.3.2 Simulated Results

The switching InGaAs pHEMT model used in this simulation is a HP EEsof scalable nonlinear HEMT model (EE_HEMT model) provided by the foundry. The 24-to-65 GHz SPST switch performance is simulated via the S-parameters and

harmonic balance techniques implemented in the commercial CAD software Applied Wave Research (AWR) Microwave Office. All the biasing and passive circuits are simulated through an electromagnetic (EM) full-wave simulator SONNET.

The simulated insertion loss and the on-state return loss from 20 to 80 GHz are plotted in Fig. 5.3. It is observed that the insertion loss is less than 3 dB and the on-state return loss is better than 8.6 dB from 24.5 to 66 GHz. Fig. 5.4 illustrates the simulated isolation and the off-state return loss from 20 to 80 GHz with the isolation better than 34 dB and the off-state return loss less than 2 dB from 22 to 80 GHz. It has almost 41.5 GHz bandwidth centered at 45.25 GHz for a flat insertion loss. The output power versus input power simulation is also exercised at 38 GHz as shown in Fig. 5.5. As indicated from the simulated data, the 1 dB compression was observed at 38 GHz for the input power of 20.5 dBm.

5.3.3 Measurement Considerations

In the millimeter-wave frequency range, two significant concerns of the 24-to-65 GHz SPST switch should be taken into account. One is the S-parameters measurement and the other is the 1 dB compression point (P1dB).

S-Parameters To acquire the S-parameters in the millimeter-wave frequency range, the V-band and W-band test sets of the vector network analyzer (VNA) are required. The Through-Reflect-Line (TRL) or Line-Reflect-Match (LRM) calibrations must be applied to receive an accurate measurement.

1dB Compression The P1dB can be obtained by measuring the output power versus input power where the output power gain, comparing to the small-signal gain, drops by 1 dB. In general, the P1dB of SPST switches are in the order of 20 dBm or may be higher.

5.3.4 Measured Results

The 24-to-65 GHz SPST switch was measured via on-wafer probing. Fig. 5.6(a) and Fig. 5.6(b) present the test setups used for the circuit characterization. The first and second are established for the S-parameters measurement and the P1dB, respectively. A microphotograph of the 24-to-65 GHz SPST switch is depicted in Fig. 5.7.

The control voltage for each state is 0 V for the off-state and -8V for the on-state. The measured insertion loss and the on-state return loss from 20 to 80 GHz are plotted in Fig. 5.8. It is observed that the insertion loss is less than 3 dB and the on-state return loss is better than 8.2 dB from 24 to 65 GHz. Fig. 5.9 illustrates the measured isolation and the off-state return loss from 10 to 80 GHz with the isolation better than 30 dB and the off-state return loss less than 2 dB from 10 to 80 GHz. The best isolation is 60 dB around 24 GHz. It has almost 41 GHz bandwidth centered at 44.5 GHz for a flat insertion loss. The output power versus input power measurement is also exercised at 38 GHz as shown in Fig. 5.10. As indicated from the measured data, the 1 dB compression was observed at 38 GHz for the input power of 20 dBm.

5.4 30.5-to-64.5 GHz Single-Pole-Double-Throw Switch using InGaAs pHEMT

5.4.1 Circuit Design

Fig. 5.11 illustrates the schematic diagram of the 30.5-to-64.5 GHz SPDT switch. In order to maximize the bandwidth of SPDT switch, Fisher's method, as described in Section 4.3.2, is also applied and extended to the millimeter-wave frequency range. This circuit was designed using microstrip transmission lines. The

switching device is an InGaAs pHEMT with 2 x 100 um gate width. The four quarter-wavelength short-circuited stubs filter is utilized to achieve enough isolation. Each of the short-circuited stubs shunts with the drain port of the InGaAs pHEMT switching device. Accordingly, the drain is automatically biased at 0 V via the short-circuited stubs. The SPDT switch must have two identically short-circuited stub filters: one is the through-path, and the other is the isolation-path. The control gate bias is injected through a thin-film isolation resistor (R_{iso}) and a high-impedance transmission line to reduce the significantly coupling leakage between the drain to gate port for the millimeter-wave signals. A general rule to employ an InGaAs pHEMT as a switching device is to bias the control voltage (V_g) at -2.0 V for the high-impedance state and 0 V for the low-impedance state. A layout of the 30.5-to-64.5 GHz SPDT switch with chip size of 1.8 x 2 mm^2 is performed by the Cadence tools and is depicted in Fig. 5.12. Nevertheless, the common via-holes, placed on the center of this chip, can save the die size by the reduction of 5 via-holes; the actually used chip area is reduced to 1.65 x 1.5 mm^2 only.

5.4.2 Simulated Results

The switching InGaAs pHEMT model used in this simulation is a HP EEsof scalable nonlinear HEMT model (EE_HEMT model) provided by the foundry. The 30.5-to-64.5 GHz SPDT switch performance is simulated via the S-parameters and harmonic balance techniques implemented in the commercial CAD software AWR Microwave Office. All the biasing and passive circuits are simulated through an EM full-wave simulator SONNET.

The simulated on-arm insertion loss, input and output return loss from 30 to 80 GHz are plotted in Fig. 5.13. It is observed that the on-arm insertion loss is less than 6 dB with the input and output return loss is better than 5 dB and 7.2 dB from 31 to

70.5 GHz. Fig. 5.14 illustrates the simulated off-arm isolation, input and output return loss from 30 to 70 GHz with the isolation better than 34 dB and the output return loss better than 2.8 dB from 30 to 70 GHz. It has almost 30 GHz bandwidth centered at 45 GHz for a flat insertion loss. The output power versus input power simulation is also exercised at 38 GHz as shown in Fig. 5.15. As indicated from the simulated data, the 1 dB compression was observed at 38 GHz for the input power of 19.5 dBm.

5.4.3 Measurement Considerations

Similarly, two significant concerns of the 30.5-to-64.5 GHz SPDT switch should be taken into account. One is the S-parameters measurement and the other is P1dB.

S-Parameters To acquire the S-parameters in the millimeter-wave frequency range, the V-band and W-band test sets of the VNA are required. The TRL or LRM calibrations must be applied to receive an accurate measurement. The SPDT switch has three ports; therefore, the third port must be well-terminated by 50Ω standard.

1dB Compression The P1dB can be obtained by measuring the output power versus input power where the output power gain, comparing to the small-signal gain, drops by 1 dB. In general, the P1dB of SPDT switches are also in the order of 20 dBm or higher. Theoretically, the third port must be well-terminated by 50Ω standard.

5.4.4 Measured Results

The 30.5-to-64.5 GHz SPDT switch was measured via on-wafer probing. Fig. 5.16(a) and Fig. 5.16(b) present the test setups used for the circuit characterization.

The first and second ones are established for the S-parameters measurement and the P1dB respectively. A microphotograph of the 30.5-to-64.5 GHz SPDT switch is depicted in Fig. 5.17.

The control voltage for each state is 0 V for the off-state and -2V for the on-state. The measured on-arm insertion loss, input and output return loss from 30 to 70 GHz are plotted in Fig. 5.18. It is observed that the on-arm insertion loss is less than 6 dB with the input and output return loss is better than 3.3 dB and 4.7 dB from 30.5 to 64.5 GHz. Fig. 5.19 illustrates the measured off-arm isolation, input and output return loss from 30 to 70 GHz with the isolation better than 30 dB and the output return loss better than 1.8 dB from 30 to 70 GHz. The best isolation is 50 dB around 58.5 GHz It has almost 34 GHz bandwidth centered at 47 GHz for a flat insertion loss. The output power versus input power simulation is also exercised at 38 GHz as shown in Fig. 5.20. As indicated from the simulated data, the 1 dB compression was observed at 38 GHz for the input power of 20 dBm.

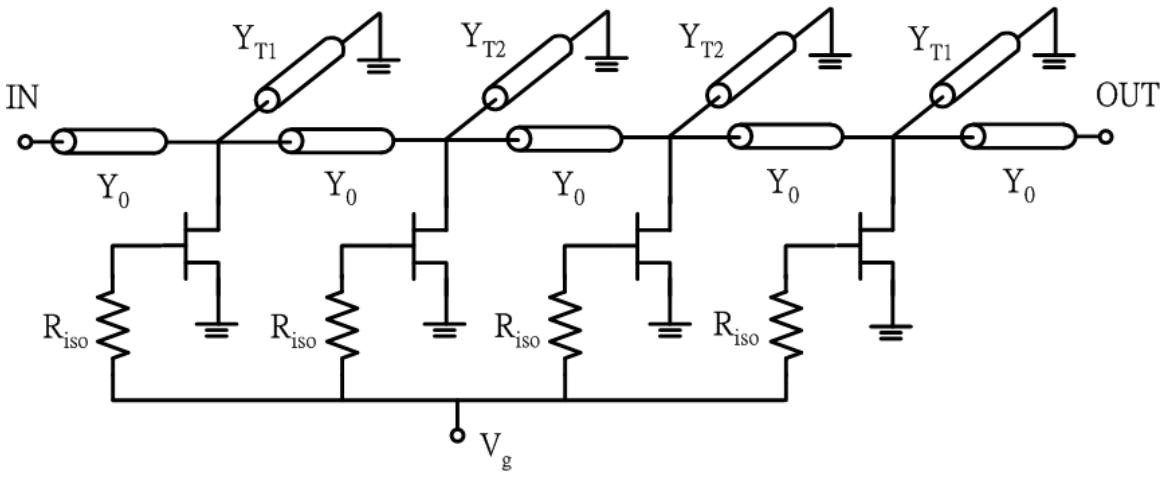


Fig. 5.1 The schematic diagram of the 24-to-65 GHz SPST switch.

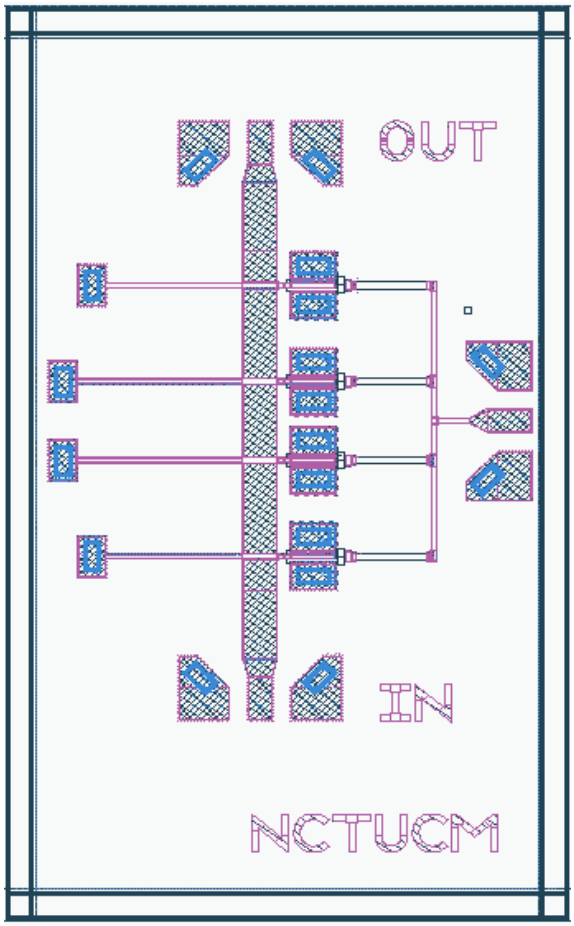


Fig. 5.2 Layout of the 24-to-65 GHz SPST switch.

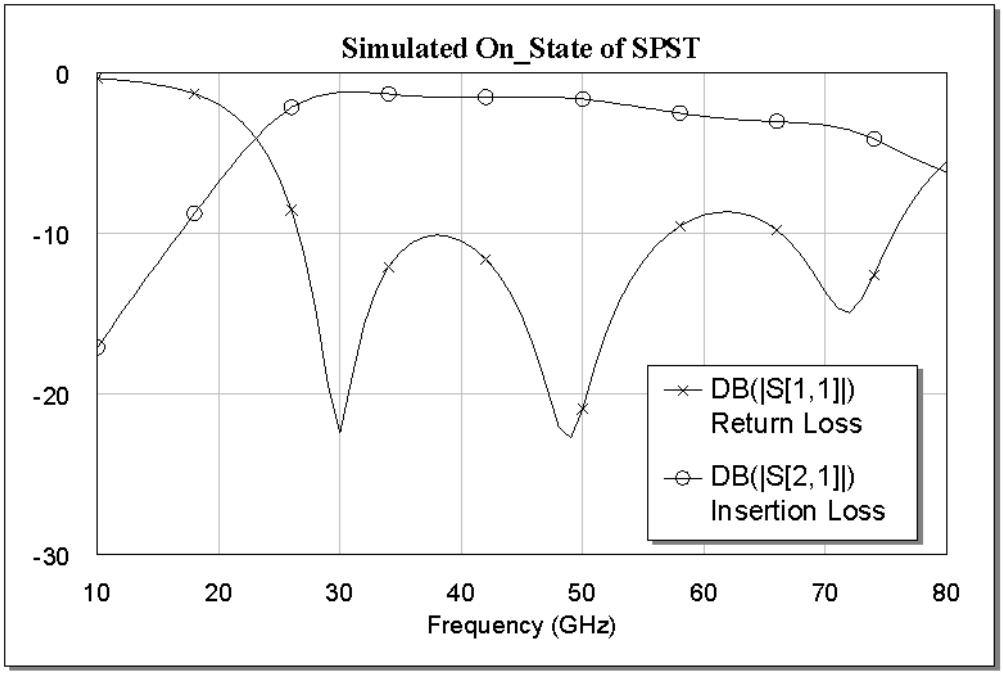


Fig. 5.3 The simulated return loss and insertion loss for the on-state of the 24-to-65 GHz SPST switch.

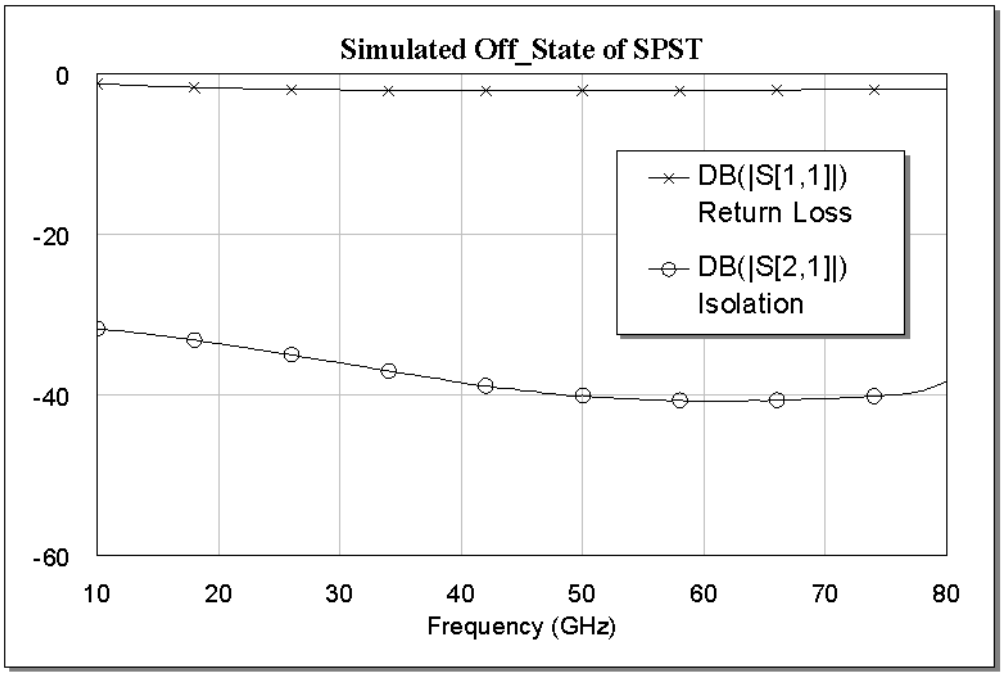


Fig. 5.4 The simulated return loss and isolation for the off-state of the 24-to-65 GHz SPST switch.

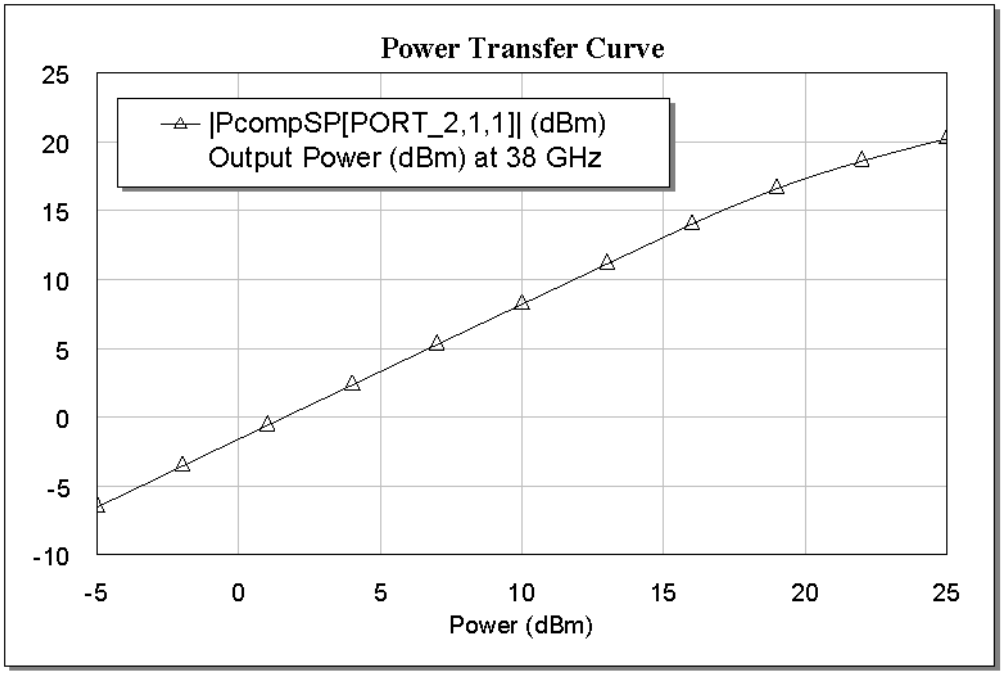
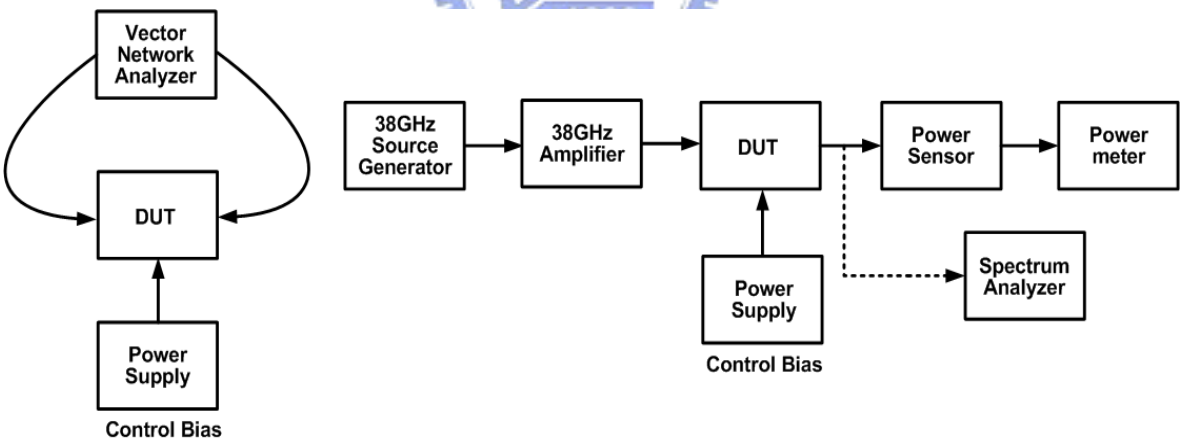


Fig. 5.5 The simulated output power versus input power of the 24-to-65 GHz SPST switch.



(a) (b)

Fig. 5.6 The test setups for the 24-to-65 GHz SPST switch characterization. (a) S parameter measurement, (b) P1dB at 38 GHz.

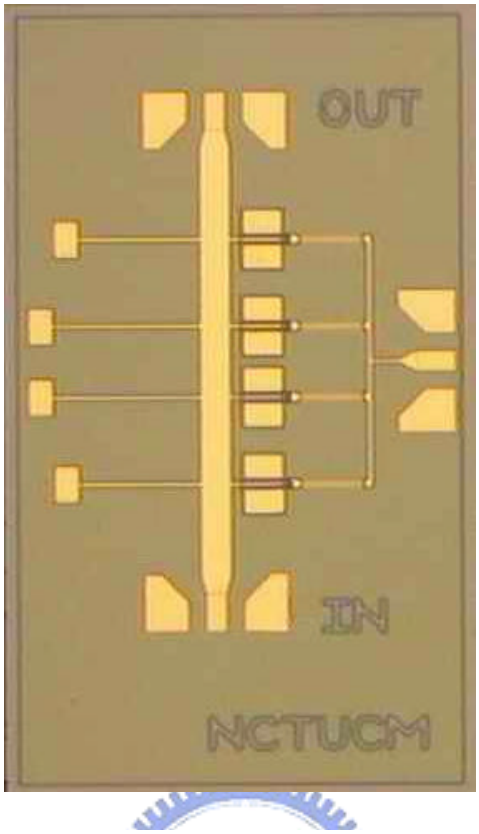


Fig. 5.7 The microphotograph of the 24-to-65 GHz SPST switch.

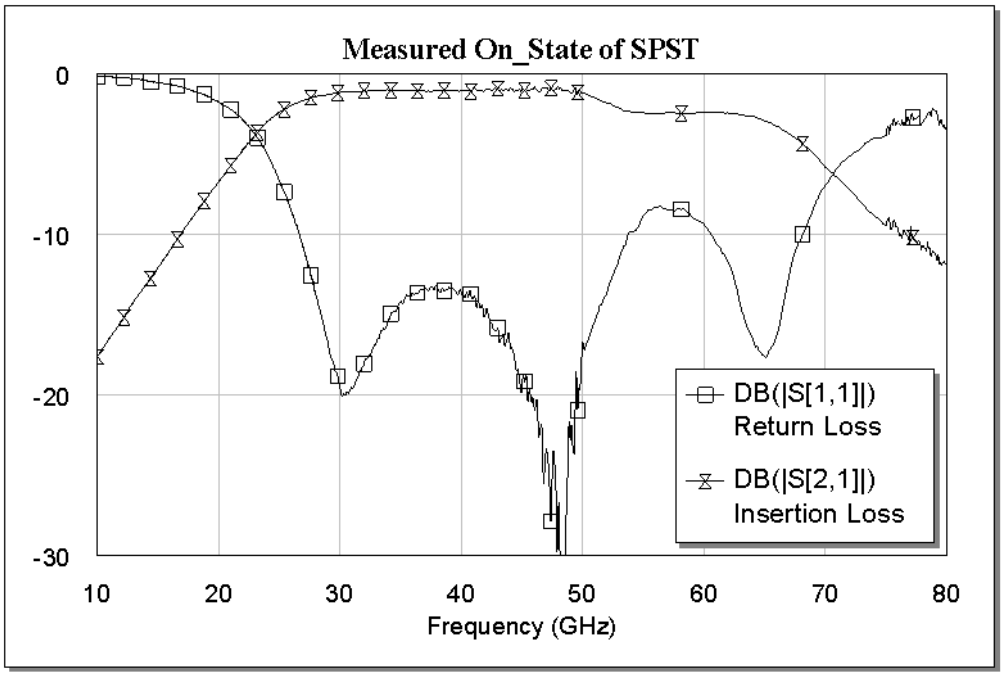


Fig. 5.8 The measured return loss and insertion loss for the on-state of the 24-to-65 GHz SPST switch.

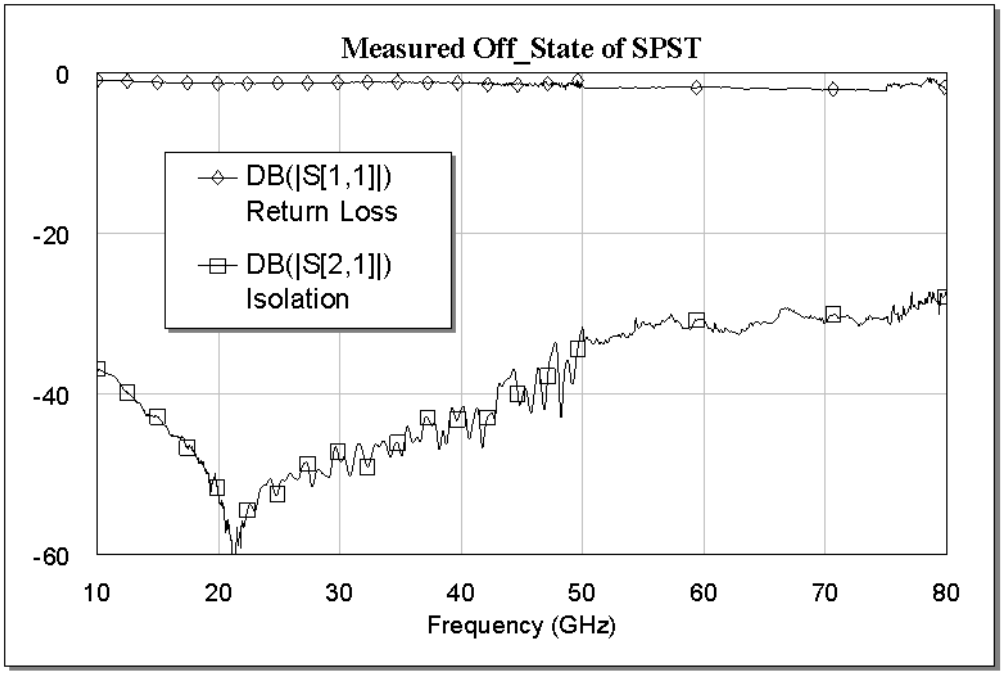


Fig. 5.9 The measured return loss and isolation for the off-state of the 24-to-65 GHz SPST switch.

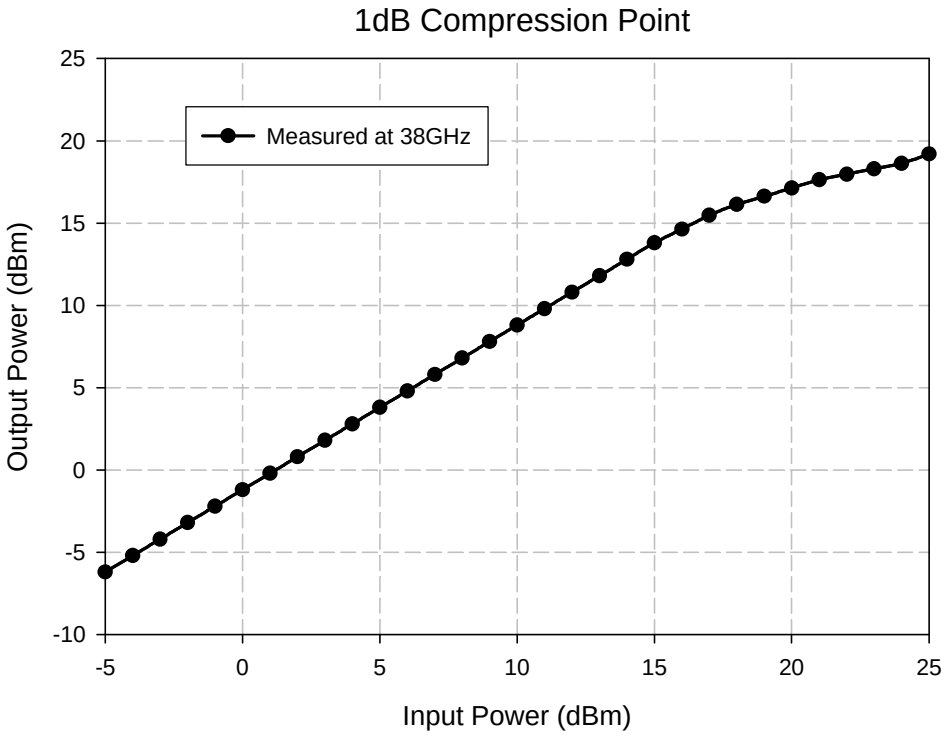


Fig. 5.10 The measured output power versus input power of the 24-to-65 GHz SPST switch.

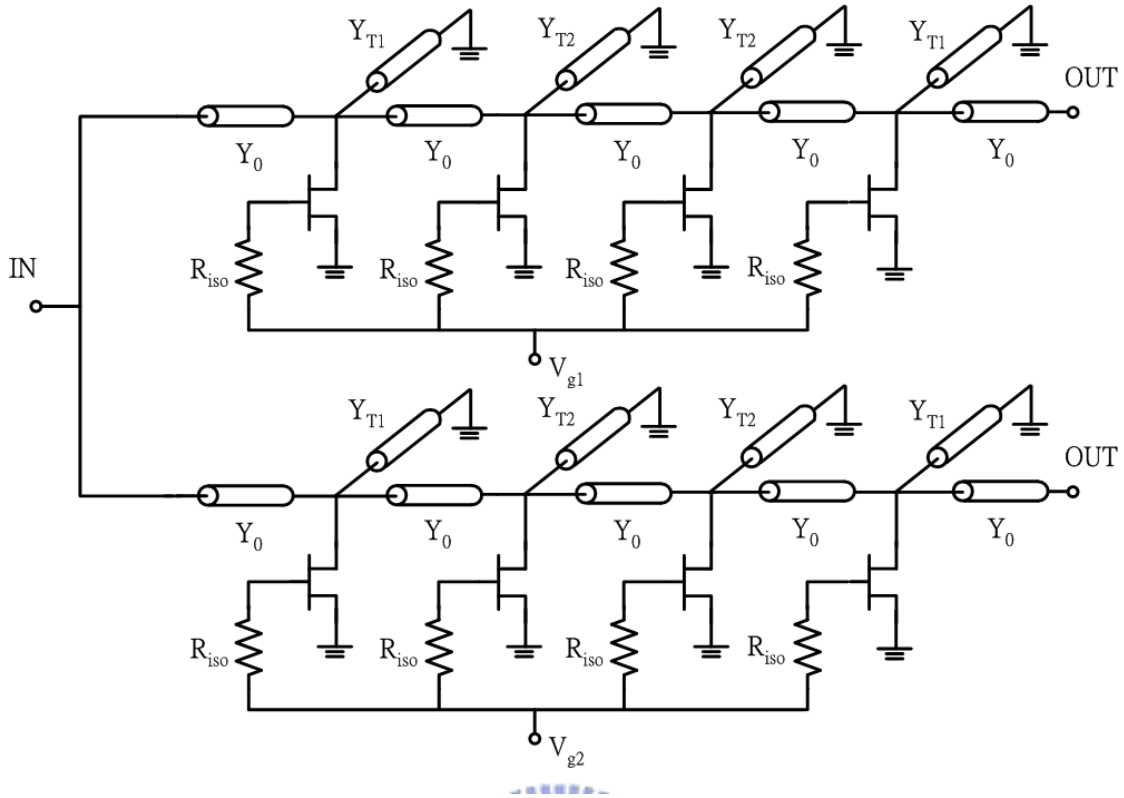


Fig. 5.11 The schematic diagram of the 30.5-to-64.5 GHz SPDT switch.

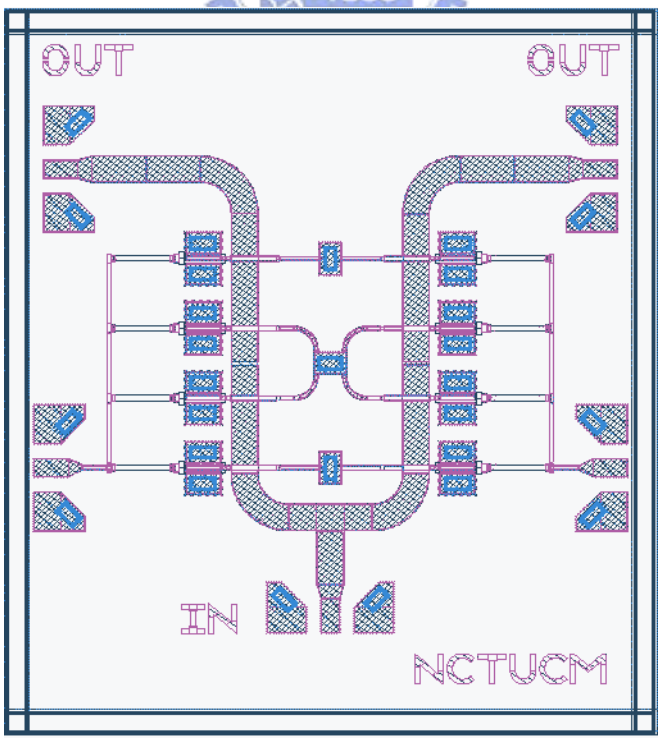


Fig. 5.12 Layout of the 30.5-to-64.5 GHz SPDT switch.

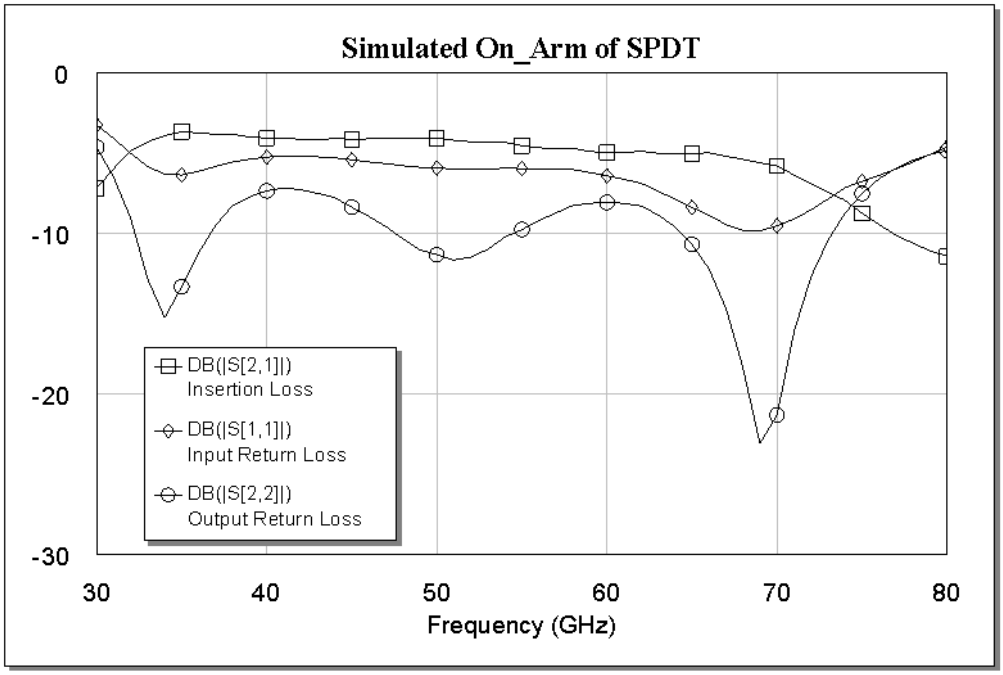


Fig. 5.13 The simulated return loss and insertion loss for the on-arm of the 30.5-to-64.5 GHz SPDT switch.

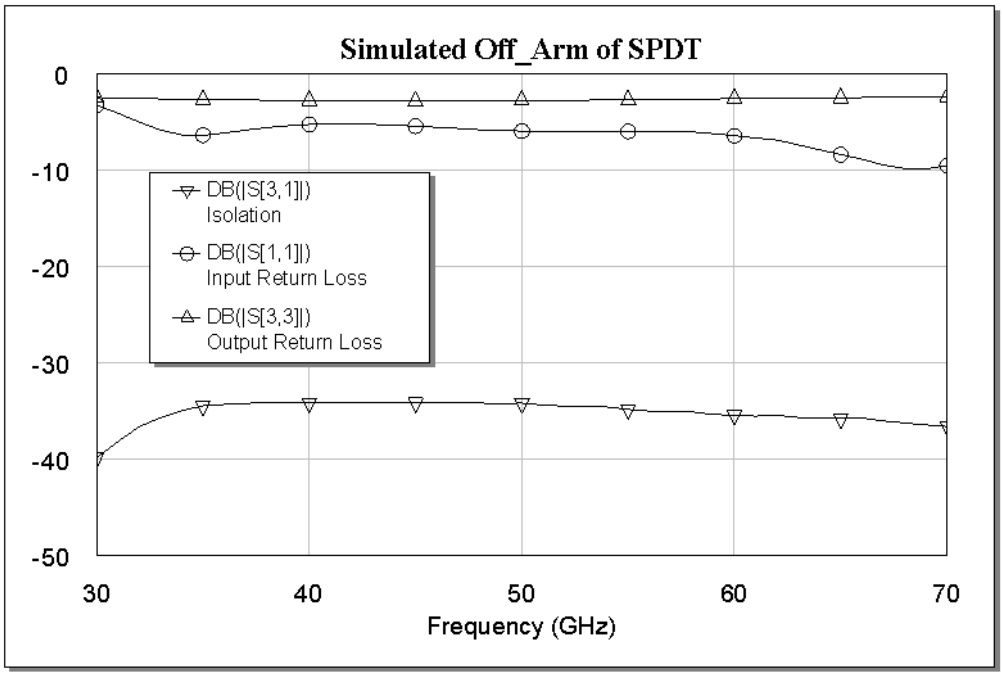


Fig. 5.14 The simulated return loss and isolation for the off-arm of the 30.5-to-64.5 GHz SPDT switch.

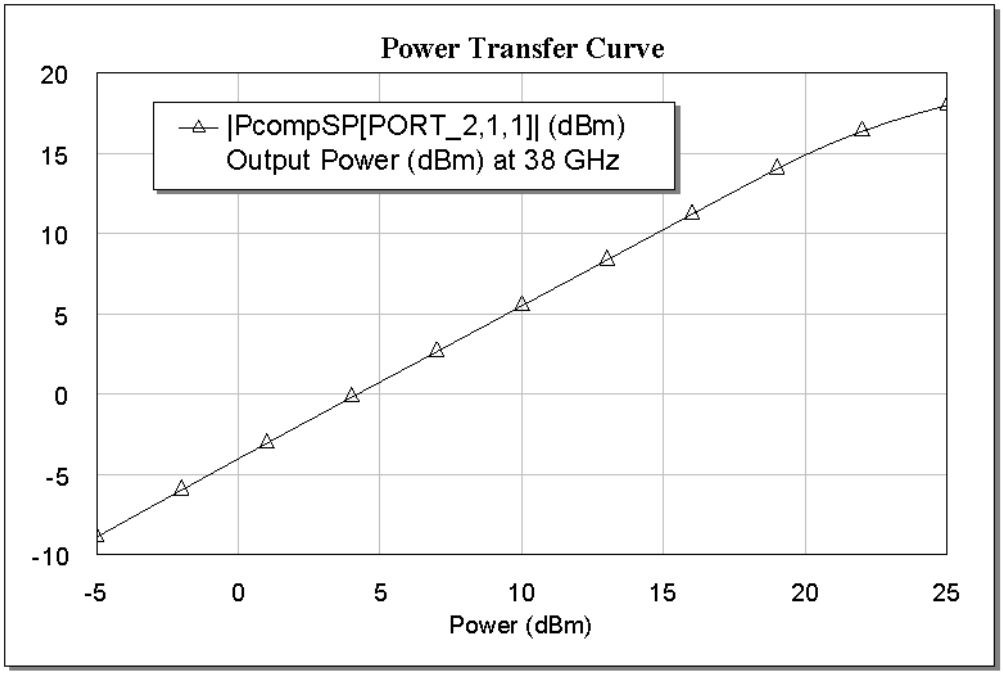
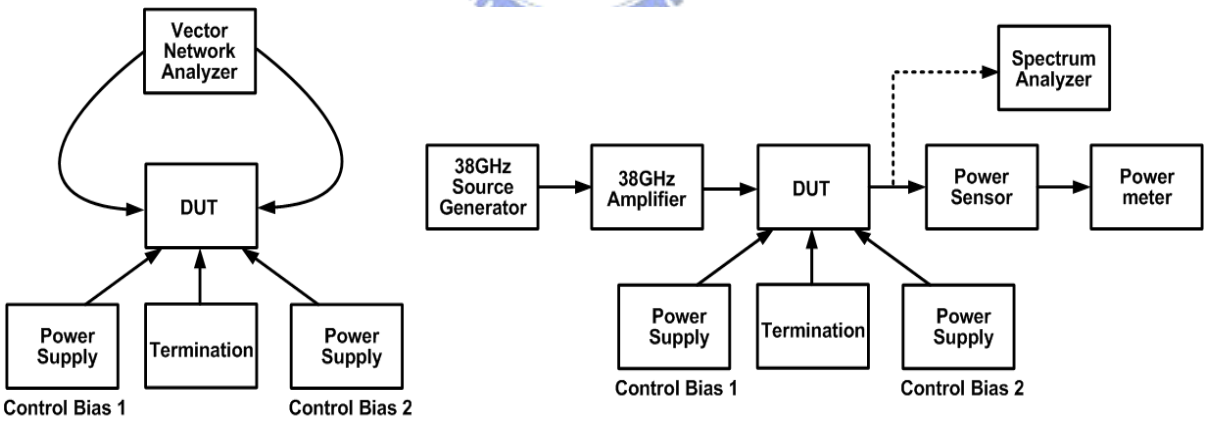


Fig. 5.15 The simulated output power versus input power of the 30.5-to-64.5 GHz SPDT switch.



(a) (b)

Fig. 5.16 The test setups for the 30.5-to-64.5 GHz SPDT switch characterization. (a) S parameter measurement, (b) P1dB at 38 GHz.

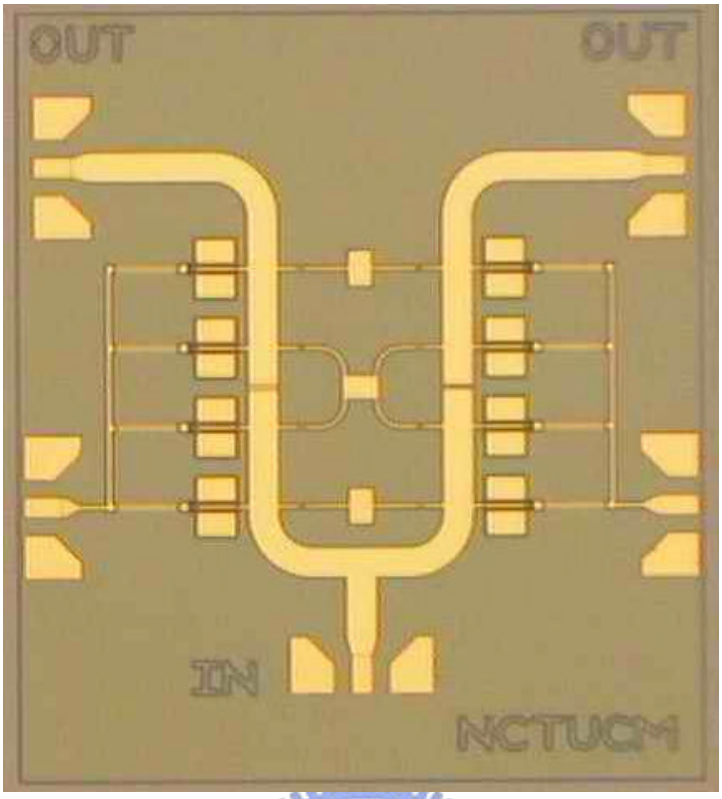


Fig. 5.17 The microphotograph of the 30.5-to-64.5 GHz SPDT switch.

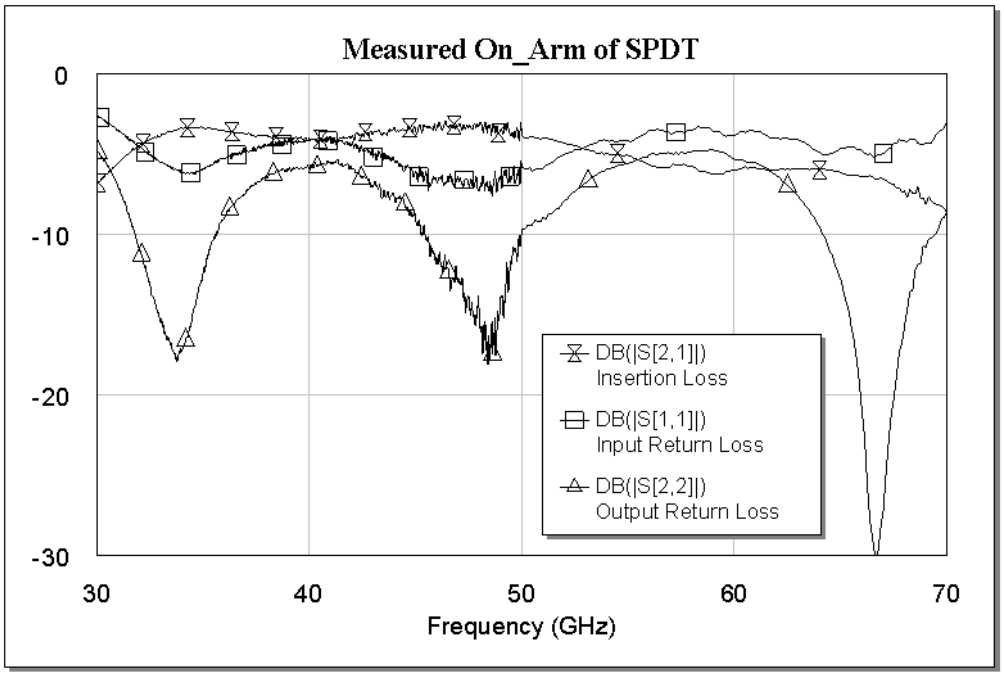


Fig. 5.18 The measured return loss and insertion loss for the on-arm of the 30.5-to-64.5 GHz SPDT switch.

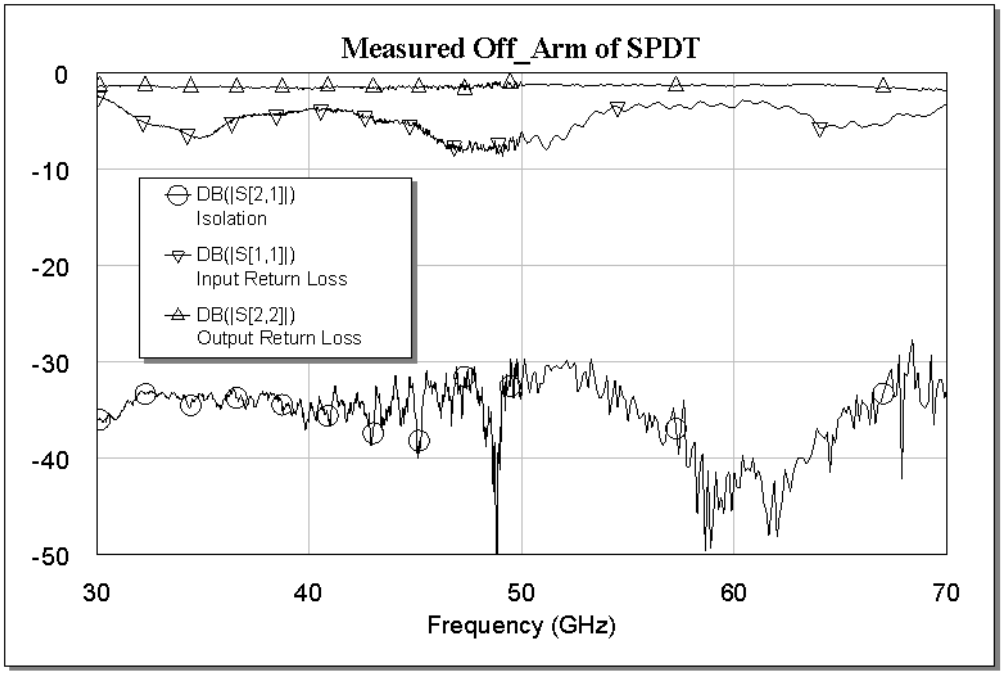


Fig. 5.19 The measured return loss and isolation for the off-arm of the 30.5-to-64.5 GHz SPDT switch.

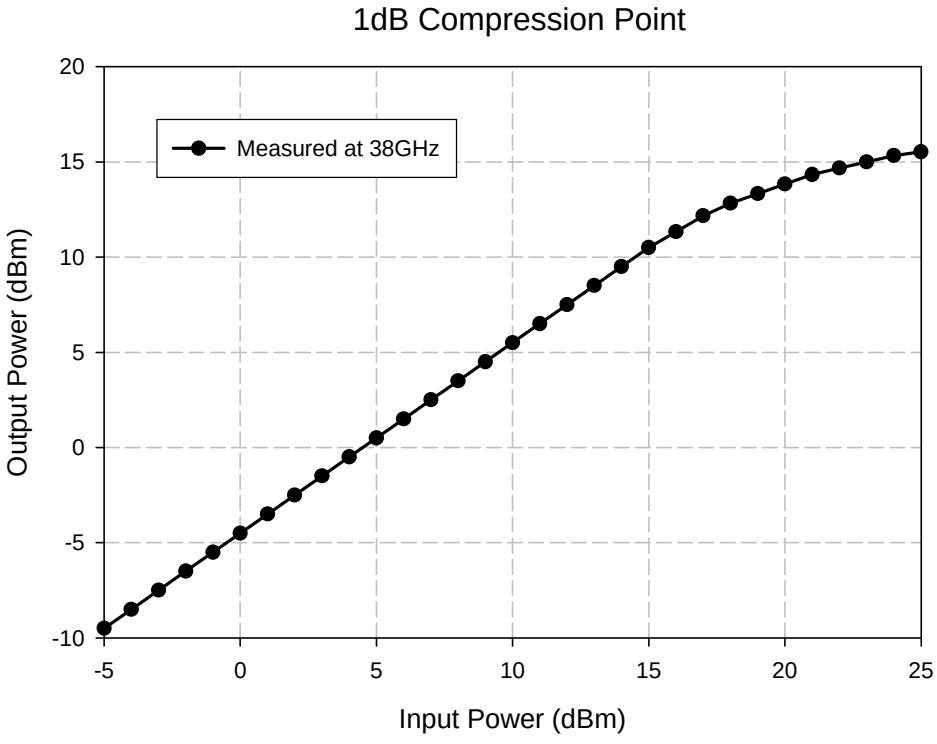


Fig. 5.20 The measured output power versus input power of the 30.5-to-64.5 GHz SPDT switch.

Chapter 6

CONCLUSIONS

In this thesis, two kinds of MMIC circuits using InGaAs pHEMT are demonstrated.

A 35-to-70 GHz frequency doubler with maximally conversion gain of -8.4 dB for 1 dBm input power has been reported in Chapter 3. The saturated output power at 70 GHz is -2.6 dBm for 15 dBm input power. It has nearly 1 GHz bandwidth centered at 35 GHz for a flat conversion gain. The measured results are slightly inconsistent with the simulations, which are caused by the inaccurate nonlinear device model.

A 24-to-65 GHz SPST switch and 30.5-to-64.5 GHz SPDT switch have been presented in Chapter 5. For the designed 24-to-65 GHz SPST switch, the insertion loss is less than 3 dB from 24 to 65 GHz and the isolation is better than 30 dB from 10 to 80 GHz. The best isolation is 60 dB around 24 GHz. It has almost 41 GHz bandwidth centered at 44.5 GHz for a flat insertion loss. The 1 dB compression at 38 GHz occurs around the input power of 20 dBm. The measured results completely correspond to the simulations below 50 GHz. Nevertheless, the simulated results are deviate from the measurements beyond 50 GHz resulting from the inexact device model, given by the foundry, for the two extremely control biases at higher millimeter-wave frequencies.

For the design of 30.5-to-64.5 GHz SPDT switch, the insertion loss is less than 6 dB from 30.5 to 64.5 GHz and the isolation is better than 30 dB from 30 to 70 GHz. The best isolation is 50 dB around 58.5 GHz. It has almost 34 GHz bandwidth centered at 47 GHz for a flat insertion loss. The 1 dB compression at 38 GHz occurs

around the input power of 20 dBm. Similarly, the measured results of the 30.5-to-64.5 GHz SPDT switch have a full correspondence to the simulations below 50 GHz. So far as we may see, the simulated results disagree with the measurements beyond 50 GHz.

The design of MMIC circuits is an art of elaboration. Six recommendations for the design of MMIC circuits are dedicated in the following:

1) Before the beginning of the circuit design, we must take notice of that either for the linear or nonlinear models, an accurate device characterization must be well-characterized through the test keys, instead of the device models provided by the foundry.
2) The EM simulations including the input/output (I/O) pads, passive and active devices should coincide with the totally physical structures to guarantee the precision for the circuit simulations.
3) In order to reduce the parasitic and coupling effects, an appropriate layout must be carefully taken into account with a possibly minimum area usage; furthermore, the width of each power line must be calculated for sufficiently power capability and moderately power consumption.
4) A suitable commercially CAD software for the circuit simulations should be applied to verify the validity of the circuit designs; in addition, the variation analyses including MMIC fabrications, temperature, parasitic and on-board bonding-wire effects are critical to certify the sensitivity and robustness of the circuits.
5) Some mature design procedures for the design of MMIC circuits, like design rule check (DRC) and layout versus schematic (LVS), should be adopted and sometimes the layout parasitic extraction (LPE) can be used for the post

layout simulations to obtain more accuracy.

6) The feasibility of measurements for the well-designed circuits must be taken into consideration, especially for the totally on-wafer probing tests.

These recommendations are extremely valuable for the design of MMIC circuits. The author suggests that the MMIC designers could follow these rules as the best regards.

References

[1] I. D. Robertson and S. Lucyszyn, *RFIC and MMIC Design and Technology 2nd ed*, Institution of Electrical Engineers, London, 2001.

[2] M. T. Faber, J. Chramiec, and M. E. Adamski, *Microwave and Millimeter-wave Diode Frequency Multipliers*, Artech House Publishers, 1995.

[3] Y. Kwon, D. Pavlidis, P. Marsh, M. Tutt, G.I. Ng, and T. Brock, "180 GHz InAlAs/InGaAs HEMT monolithic integrated frequency doubler," *Gallium Arsenide Integrated Circuit (GaAs IC) Symposium*, Technical Digest 1991, 13th Annual, 20-23 Oct. 1991 pp.165-168.

[4] C. Rauscher and H. A. Willing, "Simulation of Nonlinear Microwave FET Performance Using a Quasi-Static Model," *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-27, No. 10, pp.834-840, Oct. 1979.

[5] Guillermo Gonzalez, *Microwave Transistor Amplifiers Analysis and Design 2nd ed*, Prentice Hall, 1996.

[6] Rober C. Weast and Samuel M. Selby, *Handbook of tables for mathematics 4th ed*, Chemical Rubber Co. Publishers, 1970.

[7] Stephen A. Maas, *Microwave Mixers 2nd ed*, Artech House Publishers, 1993.

[8] Stephen A. Maas, *Nonlinear Microwave Circuits*, IEEE Press, 1996.

[9] D. G. Thomas, Jr. and G. R. Branner, "Optimization of Active Microwave Frequency Multiplier Performance utilizing Harmonic Terminating Impedances," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 44, No. 12, pp.2617-2624, Dec. 1996.

[10] C. Rauscher, "High-Frequency Doubler Operation of GaAs Field-Effect Transistors," *IEEE Trans. on Microwave Theory and Techniques*, Vol. 83, pp.462-473, Jun. 1983.

[11] R. E. Fisher, "Broadbanding Microwave Diode Switches," *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-13, No. 5, pp.706, Sept. 1965.

[12] Y. Ayasli, "Microwave Switching with GaAs FETs," *Microwave J.*, Vol. 25, pp.61-71, Nov. 1982.

[13] M. J. Schindler and A. Morris, “DC-40 GHz and 20-40 GHz MMIC SPDT switches,” *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-35, pp.1486-1493, Dec. 1987.

[14] A. Gopinath and J. Rankin, “GaAs FET RF Switches,” *IEEE Trans. on Electron Devices*, Vol. ED-32, pp.1272-1278, July 1985.

[15] I. Bahl and P. Bhartia, *Microwave Solid-State Circuit Design*, Wiley Interscience, N.Y. 1988.

[16] M. Madihian, L. Desclos, K. Maruhashi, K. Onda, and M. Kuzuhara, “A Sub-nanosecond Resonant-type Monolithic T/R Switch for Millimeter-wave Systems Applications,” *IEEE Trans. on Microwave Theory and Techniques*, Vol. 46, pp.1016-1019, July 1998.

[17] Kun-You Lin, Yu-Jiu Wang, Dow-Chih Niu, and Huei Wang, “Millimeter-wave MMIC single-pole-double-throw passive HEMT switches using impedance-transformation networks,” *IEEE Trans. on Microwave Theory and Techniques*, Vol. 51, Issue:4, pp.1076-1085, April 2003.

[18] H. Mizutani, and Y. Takayama, “DC-110-GHz MMIC traveling-wave switch,” *IEEE Trans. on Microwave Theory and Techniques*, Vol. 48 Issue:5, pp.840-845, May 2000.

[19] J. F. White and K. E. Mortenson, “Diode SPDT Switching at High Power with Octave Microwave Bandwidth,” *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-16, No. 1, pp.30-36, Jan. 1968.

[20] W. W. Mumford, “Tables of Stub Admittances for Maximally Flat Filters Using Shorted Quarter Wave Stubs,” *IEEE Trans. on Microwave Theory and Techniques*, Vol. MTT-13, No. 5, pp.695-696, Sept. 1965.