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Ka-Band單晶毫米波功率放大器

及新式可控制增益雙向放大器之分析與設計

Design and Analysis of Ka-Band MMIC Power Amplifier

And

Novel Bi-Directional Amplifier with Gain Control

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中華民國九十三年六月

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摘要

本篇論文的第一部份描述運用在汽車防撞雷達系統中的Ka頻段功率放大器電路之分析與設計。為符合防撞雷達所需的線性度及高效率，選擇採用二級的功率放大器，第一級使用 class A 架構供應足夠的功率增益，同時設計第二級為 Class AB 架構以提高 RF-to-DC 訊號比，並利用匹配電路壓制訊號經過電路所產生的二階及三階諧波以提升線性度。PHEMT 半導體材料因為擁有較高的崩潰電壓及較低的通道摻雜，適合用來設計高功率與高頻的射頻電路，故為了使電路能運用在 Ka 頻段中，選擇利用 WIN 0.15-um GaAs PHEMT 製程設計這兩個電路，量測結果上，在操作中心頻率 32.4GHz 時，功率放大器有 P-1dB 為 2dBm，Pout@P-1dB 為 12.4dBm，PAE@P-1dB 為 19.7%。

論文的第二部分實現以兩個反射式放大器及一個 90 度 branch-line 電路為架構的新式 2.4GHz 可控制增益雙向放大器，其可有效提高電路的隔離度，並降低雜訊指數，提昇訊號品質，不過因為此類放大器原理與振盪器相似，故在設計過程中必須非常小心訊號的振盪。反射式放大器為單端輸入、輸出的元件，將輸入的訊號放大並從同一端點輸出；而 Branch-Line 電路功能為將輸入端訊號分成二個相位差為 90 度、且功率相同的輸出訊號，並且在隔離埠(Isolation Port)的功率為零；藉由上述元件的特性，雙向放大器可獲得放大的輸出訊號，增益大小與一個反射式放大器相同；並加上可變電容電路，讓此電路依照需求調整增益，且能藉著此電容穩定電路的振盪情形。因為傳統 90 度 Branch-Line 電路在 2.4GHz 時

面積太大，不適合在 CMOS 裡實現，所以選擇放在 FR4 板上採用外加電容的方法將縮小其面積。反射式放大器的增益為 13.6dBm，P_{1dB} 為-5dBm，雜訊指數為 14.3dB；而雙向放大器的回損 S11 皆在-10dB 以下，增益變化從 7.5dB 到 16dB，雜訊指數變化為 4.1 到 5.4，可藉可變電容值調整，不過當增益值愈大時，則回損 S11 相對也愈大。

Design and Analysis of Ka-Band MMIC Power Amplifier

And

Novel Bi-Directional Amplifier with Gain Control

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Abstract

This thesis is divided into two parts. The first part describes the analysis and design of a Ka-Band power amplifier applied to the automotive collision avoidance radar system. In order to acquire the adequate linearity and efficiency of the system requirements, the architecture with two stages is adopted to design the power amplifier. The first stage utilizes class-A type to supply sufficient power gain. The second stage improves RF-to-DC signal ratio by class-AB type. By this way, the linearity of this circuit can also be improved. The semiconductor material of PHEMT is adequate to design the RF circuits with the characteristics of high power level and high operating frequency because it possesses the higher breakdown voltage and the lower doping channel. So as to operate the circuits at Ka-band, we select the semiconductor process of WIN 0.15-um GaAs PHEMT to design the circuits. At the central frequency of 32.4GHz, the measured results reveal that the fabricated power amplifier has the P-1dB of 2dBm、Pout of 12.4dBm, and PAE of 19.7% at P-1dB point.

The second section of this thesis proposes and demonstrates a novel architecture

of 2.4GHz bi-directional amplifier. The approach improves effectively the isolation and noise figure of the circuit to ameliorate the quality of output signal. The framework includes two reflection-type amplifiers and a 90 degree branch-line circuit. The designed process must pay attention to the oscillation condition because its principles are similar to that of an oscillator. Meanwhile, the ability of bi-direction could be realized in accordance with the characteristic of branch-line circuit. The bi-directional amplifier with this architecture can obtain the gain which is same as that of a reflection-type amplifier. Also, a variable capacitance is arranged to steady the condition of oscillation and adjust the gain according to the circuit's requires. And the conventional branch-line circuit must be realized by means of transmission lines with the quarter wavelength. This length is 16.7mm at the operating frequency of 2.4GHz. This approach is inappropriate for CMOS IC. Therefore, this 90 degree branch-line circuit is realized on a FR4 board and utilizes a new method to reduce the area. So, this IC only embraces these two critical reflection-type amplifiers. And the expected specifications of this reflection-type amplifier are as follows: power gain 13.6dBm, P_{1dB} -5dBm, the noise figure 14.3dB. Furthermore, the return loss S11 of this bi-directional amplifier is below -10dB across overall utilized bandwidth. The gain can alter from 7.5dB to 16dB and the noise figure varies from 4.1 to 5.4.

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CHAPTER 1

Introduction

1.1 Motivation

In recent year, people pay much attention to the security of driving. Meanwhile, the government and industries spare no efforts to support the study of automotive collision avoidance radar systems by investing lots of funds and manpower. The collision avoidance radar is a system with operating frequency at 77GHz. Its transmitter includes the components including VCO、PA、doubler and so on. The major of these purposed systems utilizes a voltage controlled oscillator with the operating frequency at 38GHz to supply the local signal because a lower frequency oscillator provides a system with the lower phase noise. In the millimeter wave, the signal source has better to be a signal with low phase noise. There are two common methods to produce these signal sources. The first method is the signal source produced by an oscillator directly. But this way will bring the signal source higher phase noise. The alternative method utilizes a doubler to double the operating frequency of an oscillator so as to obtain the expectable signal source. This approach can supply lower phase noise to an applied system because an oscillator with the lower operating frequency can be designed easily to provide the more excellent performance. Therefore, the architecture is applied extensively. The most expensive and significant devices of these systems are power amplifiers. Therefore, the core of the related studies concentrates on power amplifiers which are able to obtain the largest output power and the minimal chip size. The research of this thesis expects that an appropriate power amplifier applied to these systems can be accomplished.

In the other hand, Retro-directional antenna arrays are applied in many wireless communication systems extensively, such as RF identification apparatuses and intelligent transport systems. Among numerous categories of these systems, an active Van Atta retro-directive array with unilateral amplifier possesses the better corresponding field level than these of the others. The formula of the corresponding field is $E_{Bi\text{-}amp}(\theta) = C.\ N.\ G.\ F^2(\theta)$, where G is the gain of a bi-directional amplifier. Therefore, a bi-directional amplifier with high gain will play the critical role in the active retro-directive arrays systems. In common, these kinds of amplifiers are accomplished by means of switches or the approach that alters the connected direction by adjusting the gate's and drain's voltages of some transistors in the circuit. Nevertheless, these methods are not able to amplify bi-directional signals simultaneously. Therefore, a novel schematic must be utilized to ameliorate this problem.

1.2 Organization of This Thesis

This thesis is organized as follows. Chapter 2 introduces the principles and process of power amplifier's design. Meanwhile, the simulated and experimental results are appeared. Chapter 3 describes a novel bi-directional amplifier with gain control utilizing two reflection-type amplifiers. In this chapter, the designed theories and considerations are explained. The layout and simulated results are also illustrated to prove the feasibility. The conclusions are made in Chapter 4.

CHAPTER 2

Design and Analysis of a Ka-Band Power Amplifier

The RF front-end of an automotive radar operates in millimeter-wave frequencies and uses either FMCW or pulse radar principles. The forward looking automotive radar in the 76-77GHz range is one of the most promising commercial applications at W-band frequency. The majority of these modules are manufactured using hybrid assemblies of Gunn, Schottky and PIN diode circuits. Nevertheless, a major step forward is the utilization of GaAs MMIC technology which results in d reduction of assembly, test, and finally lower module costs. In addition, the use of gallium arsenide (GaAs) based dual-gate PHEMTs will lead to higher circuit performance.

2.1 Semiconductor pHEMT

The high electron mobility transistor, or HEMT, is a field-effect transistor having current carrier densely confined in a thin sheet of order 100Å thickness. The HEMT consists of epitaxial grown layers of compound semiconductors which have different bandgap energy, so the interface between them constitutes a heterojunction. For application to MMICs, the most attractive feature of the HEMT is its low noise. At millimeter frequency particularly, the HEMT promises a lower noise figure than gain. Furthermore, the HEMT also provides the better power performance due to its characteristic of high breakdown voltage.

The Fig.2.1 shows the schematic cross section of pHEMT. A planar-doped AlGaAs layer for electron supply from the bottom of the channel, an InGaAs channel, a Si planar-doped AlGaAs layer for electron supply from the top and gate isolation, and an n+ GaAs cap layer for ohmic contact enhancement. The ship is fabricated

using 0.15um AlGaAs/InGaAs/GaAs pseudomorpic T-gate power HEMT MMIC technology on a 100um GaAs substrate. The pHEMT possesses a gate-to-drain breakdown voltage of 10v typically, parameter f_T of 85GHz, and fmax of 160GHz.

2.2 Basic Theories and Design Methodology

2.2.1 Crucial Parameters

Efficiency Efficiency is a critical parameter for RF power amplifiers. It is important when the available input power is limited, such as in battery-powered mobile equipment. Efficiency is output power versus input power level in rough. The most common definitions are presented below by the different meanings of input power and output power. From a practical standpoint, a designer's goal is to minimize the total dc power required to obtain a certain RF output power level. Therefore, the **overall efficiency** is defined as

$$\eta_{overall} = \frac{Po}{Pdc + Pin} = \frac{Po}{Pdc + \frac{Po}{Gp}} \tag{2.1}$$

Power-added efficiency is an alternative definition that includes the effect of the drive power used frequently at microwave frequencies and is defined as

$$\eta_{power-added} = \frac{Po - Pin}{Pdc} = \frac{Po - \frac{Po}{Gp}}{Pdc} \tag{2.2}$$

Intermodulation The harmonic distortion is often used to describe nonlinearities of analog circuits. Common used is the intermodulation distortion in a two-tone test. When two signals with different frequencies are applied to a nonlinear system, the output in general exhibits some components that are not harmonics of the input frequencies. Of particular interest are the third-order IM products at $2W_1$-W_2 and

$2W_2$-W_1 when two signals' frequencies are W_1 and W_2 because they appear in the vicinity of W_1 and W_2, as shown in Fig.2.2. The corruption of signals due to third-order intermodulation of two nearby interferer is so critical that a performance parameter "third intercept point"(IP3) has been defined to characterize the behavior. As shown in Fig.2.3, the horizontal coordinate of this point is called the input IP3 (IIP3), and the vertical coordinate is called the output IP3 (OIP3). The value of IIP3 and OIP3 can be obtained by the formulas below.

$$P_{IIP} - Pin = P_{OIP} - Pout \tag{2.3}$$

$$P_{IIP} = Pin + \frac{1}{2}(Pout - P_{IP}) \tag{2.4}$$

Intermodulation is a troublesome effect in RF systems. The IIP3 and OIP3 can be utilized to characterize the linearity of nonlinear circuits.

Gain Compression The small-signal gain of a circuit is usually obtained with the assumption that harmonics are negligible. However, as the signal amplitude increases, the gain begins to degrade. In fact, nonlinearity can be viewed as variation of the small-signal gain with the input level. In RF circuits, this effect is quantified by the "1-dB compression point", defined as the input signal level that causes the gain to drop by 1dB.

Adjacent Channel Leakage Power Ratio (ACPR) This analysis assumes two separate carriers with fixed spacing. Such a signal is the result of the AM of a signal carrier, as shown in Fig.2.4. The two-carrier signal would be the spectrum from a double side-band suppressed carrier AM system with a single, fixed frequency modulating tone. The key point to note is that the IM bands stretch out to three times the original modulation band limits in the case of the third-order distortion

products, and five times these limits for fifth order, as shown in Fig.2.5. Therefore, the spectrum resulting from nonlinear amplification has a stepped appearance, with each step corresponding to a higher order of distortion. These steps recently have become known as growth sidebands, or the **adjacent channel power** (ACPR).

2.2.2 Class A Amplifier

Several types of RF power amplifiers will be discussed, most often called Class A, AB, B and C. The portion of the RF cycle the device spends in its active region is the **conduction angle** and is denoted by $2\theta_c$. Based in the conduction angle, the amplifiers are categorized as

- Class A amplifiers, if $2\theta_c = 360$ degree. The active device is in its active region during the entire RF cycle.
- Class AB amplifiers, if $180^\circ < 2\theta_c < 360^\circ$
- Class B amplifiers, if $2\theta_c = 180$ degree
- Class C amplifiers if $2\theta_c < 180$ degree

The numerous classic modes of operation discussed above are shown in Fig.2.6. The investigation below will focus on these operated types in detail.

The equations of the DC component is

$$Idc = \frac{1}{2\pi}\int_{-\alpha/2}^{\alpha/2} \frac{\mathrm{Im}\,ax}{1-\cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)]d\theta \qquad (2.5)$$

and the magnitude of the output nth harmonic is

$$I_n = \frac{1}{\pi}\int_{-\alpha/2}^{\alpha/2} \frac{\mathrm{Im}\,ax}{1-\cos(\alpha/2)}[\cos\theta - \cos(\alpha/2)]\cos n\theta d\theta \qquad (2.6)$$

The parameter α is the conduction angle. If a sine-wave signal of amplitude Vdc is

assumed as the RF output voltage at the transistor. Therefore, the RF fundamental output power is given by

$$Po = \frac{Vdc}{\sqrt{2}} * \frac{I1}{\sqrt{2}} \tag{2.7}$$

where I1 is the output 1st fundamental harmonic and the dc supply is given by

$$Pdc = Vdc * Idc \tag{2.8}$$

The DC power dissipation neglects the current of gate end due to the current Igs is slight extremely.

For Class A operation, the Idc current must be selected to keep the transistor in its active region during the entire RF cycle, thus assuring a 360 degree conduction angle($\alpha = 2\pi$). The operation of class A is illustrated in Fig.2.7. The input RF signal enters the device from the gate end. The drain current turns on across 0 to 2π resulting from the selection of biasing point. Utilizing the formulas of (2.5) to (2.8) and the relation of $\alpha = 2\pi$ to calculate the DC power dissipation P_{dc} and the output power Po, the efficiency of PAE could be obtained in accordance with the equation of (2.2). The operation of class A mode owns approximately 50% output PAE efficiency if the gain is high sufficiently. And the circuit possesses the higher linearity than the other types, but power dissipation is the largest drawback for this category of these circuits.

2.2.3 Class B and AB Amplifier

The power amplifier adopted class B or AB modes is a classic compromise, offering higher efficiency and cooler heat sinks than the linear and well-behaved class A mode, but incurring some increased nonlinear effects which can be tolerated. The

active device is biased to a quiescent point which is somewhere in the region between the cutoff point and the class A bias point. The Fig.2.8 shows an idealized RF device, having a linear transconductive region terminated by a defined cutoff point. Based on this figure of I_D versus V_{GS}, the biased points of class B and AB mode could be determined. Assumed that the turn-on voltage is V_t, the gate voltage of the class B mode is selected at this point V_t. But the biased point must be above V_t if the class AB mode is opted. The operation of class B and AB mode are illustrated in Fig.2.9 and Fig.2.10. The output signal without the output matching circuit is like the half-wave rectified waveform, indicated by the equation below.

$$x(t) = \sum_{k=-\infty}^{\infty} C_k e^{jkwot} \tag{2.9}$$

$$C_k = \begin{cases} C_0 = \dfrac{\chi_0}{\pi} \\ C_1 = -j\dfrac{\chi_0}{4} \\ C2 = -\dfrac{\chi_0}{4} \\ C_k = \dfrac{-\chi_0}{\pi(k^2-1)} \qquad if \quad k \neq 0 \\ C_k = 0 \qquad if \quad k \quad is \quad odd \end{cases} \tag{2.10}$$

This kind of waveform will produce the larger even harmonic terms, eliminated by means of the output matching circuit. Utilizing the formulas of calculating the PAE efficiency again, the class B mode possesses the 78.5% efficiency ideally, and the PAE efficiency of the class AB is between 50% and 78.5%.

2.2.4 Gain Match and Power Match

In general, amplifiers are realized by conjugate match in order to derive the

maximum output gain. The amplifier matched at complex conjugate is referred to gain match condition. But the output power match is necessary because power amplifiers must be devised to drive large power level. The Fig.2.11 illustrates the compression characteristics of common circuits for conjugate match and power match. The figure shows that the response for an amplifier having output power match owns lower gain at much lower drive levels. Nevertheless, amplifiers with power match could drive larger power level than that with conjugated match. It is important to note that no matter which criterion is utilized for RF power, the power match gives about 2dB improvement. Using the load pull measurement is the most efficient approach. By drawing the constant power contours, it is convenient to design the output power matching circuit. The discussion below will describe this measured system in detail.

2.2.5 Load Line Theory

The simple loadline principles could be extended to predict load-pull contours for a device kept in its linear range. The predicted output power level utilizing this method is close to the measured optimal output power P_{opt}. The start for this analysis of an RF PA is a heavily idealized device, shown in Fig.2.12. This ideal nonlinear transconductive device is represented in the figure as a voltage-controlled current source with zero output conductances and zero knee voltage. The analysis is valid up to the start of gain compression because the device is never allowed to breach the limits of linear operation. The loadline resistor is determined by drawing a straight line which connects the overdrive voltage V_{ov} to the breakdown voltage V_{DSmax}, as shown in Fig.2.12. The load-line resistor in the optimal power-matched condition has a value of

$$R_{opt} = \frac{V_{DS\max} - V_{ov}}{I_m} \tag{2.11}$$

The optimum output power P_{opt} is obtained for a load impedance with real part equal to R_{opt}. Using a simplified load-line theory, two cases have to be considered.

(1) $|Zl| \le Ropt$ when output power is current limited

$$\frac{P_o}{P_{opt}} = \frac{R_l}{R_{opt}} \quad \text{And} \quad |R_l + jX_l|^2 \le R_{opt}{}^2 \tag{2.12}$$

(2) $|Zl| \ge Ropt$ when output power is voltage limited

$$\frac{P_o}{P_{opt}} = \frac{R_l}{R_{opt}} \quad \text{And} \quad |G_l + jB_l|^2 \le G_{opt}{}^2 \tag{2.13}$$

A load resistance < R_{opt} lead to current-limited compression as evidenced by the forward gate current I_{GS} resulting from the gate end turn on. A load resistance > Ropt lead to voltage-limited compression as evidenced by the drain-gate breakdown current I_{GD}. The maximum output power occurs when $I_{GS} = I_{GD}$.

2.2.6 Load Pull Theory

The output power level is the most significant parameter for the design of power amplifiers. Power amplifiers are large-signal devices which output power is related to the output reflection parameter Γ_L generally. It is difficult to draw the constant output power contours in the Γ_L plane because they are all ellipses. In common, the load pull measurement is the most efficient approach to obtain the constant power contour, shown as the Fig.2.13. The output matching circuit could be determined according to the large-signal information of the transistor obtained by the load pull measurement. Then, assumed that the input match influences the output power slightly, the G_p circuit can be utilized to predict the overall gain. The formula of the G_p is

$$Gp = \frac{|S_{21}|^2 \left|1-|\Gamma_L|^2\right|}{\left(1-|\Gamma_{in}|^2\right)\left(|1-S_{22}\Gamma_L|\right)^2} = \frac{1-|\Gamma_L|^2}{|1-S_{22}\Gamma_L|^2 - |S_{11}-\Delta\Gamma_L|^2} * |S21|^2 = g_p * |S21|^2 \quad (2.14)$$

The center C_p and the radius R_p are

$$C_p = \frac{g_p C_2^*}{1+g_p(|s_{22}|^2 - |\Delta|^2)} \quad \text{And} \quad R_p = \frac{\left[1-2K|S_{21}S_{12}|gp+|S_{21}S_{12}2|g_p{}^2\right]^{1/2}}{\left|1+g_p(|S_{22}|^2-|\Delta|^2)\right|} \quad (2.15)$$

Observing the place of output optimal power point, the complex conjugate match is employed in the input port according to the Gp circle discussed above. The overall gain can be obtained.

The typical load-pull configuration is shown in the Fig.2.14. The load pull is a method to measure the device terminal impedance under a particular operating condition. The device is tuned with removable passive tuner until the required performance is obtained. Then, the tuner is removed and the impedance to the tuner is then measured by the network analyzer. The procedure is repeated at each frequency and power of interest. The coupled forward power P1 is measured at the fixed frequency and power level. Next, the input impedance tuner T1 is adjusted in order to receive the optimum return loss P2. Finally, the output impedance tuner T2 must be modified for the desired power performance P3. The input and output reflection coefficients are determined by a network analyzer. Therefore, power amplifiers can be realized readily base according to the information of load pull.

2.3 Ka-Band Power Amplifier

2.3.1 Selection of the Elements

The schematic of transmitted circuits applied in automotive collision avoidance radar systems connects commonly a buffer amplifier after the 38GHz oscillator in

order to boost the signal amplitude. This chip is designed to replace the buffer amplifier and remove the 77GHz power amplifier from the 77GHz output port by supporting the sufficient output power. In order to acquire the linearity and adequate efficiency of the system, the architecture with two stages is adopted to devise this power amplifier. The first stage utilizes class-A type to supply sufficient power gain. The second stage improves the RF-to-DC signal ratio by class-AB mode. The 0.15um GaInAs pHEMT transistor with gate width 300um is picked at the first stage. And the transistor with gate width 600um is utilized at the power stage to drive plentiful output power. The operating points of the two stages are shown in Fig.2.15.

2.3.2 Calculating Load Line Resistance from IV Curve

In order to estimate roughly the load line resistance, the characteristics of output conductance and variable overdrive voltages are ignored. According to the features of I-V curve shown in the Fig.2.15, the optimal load line resistance and the maximum output power are calculated in accordance with the Eq. (2.10). Assumed that Imax is equal to 300mA and Vmax is 4V, R_{opt} and P_{max} are computed in Eq. (2.16) and (2.17).

$$R_{opt} = \frac{V_{DS\max} - V_k}{I_m} = \frac{4-1}{0.3} = 10\Omega \tag{2.16}$$

$$P_{\max} = \frac{1}{8} \times V_{\max} \times I_{\max} = \frac{1}{8} \times 4 \times 0.3 = 0.15(W) = 21.8(dBm) \tag{2.17}$$

Utilizing the software of load pull measurement, the constant power contours and the constant efficiency contours are drawn as shown in Fig.2.16. The optimal output power level has to compromise with the demanded efficiency. Therefore, the adequate output matching point is selected referred to the proposed specifications.

2.3.3 Overall Schematic and Layout Considerations

The whole schematic of this 38GHz power amplifier is depicted in the Fig.2.17. The circuit is divided into five sections; they are the input matching circuit, the drive stage, the interface matching circuit, the power stage and the output matching circuit. Firstly, the biasing points of the two stages are selected in order to acquire the desired characteristics. Utilizing the software of load pull measurement, the output matching circuit could be determined by making trade-off between the output power level and the power-added-efficiency. Referred to the output optimal point of the drive stage and the input optimal point of the power stage, the best interface matching point is chosen to balance the mismatch. The input matching circuit is realized easily by conjugate match because it is assumed to influence the output power level slightly.

The layout of this power amplifier is shown in the Fig.2.18. The thin transmission lines are applied in this circuit as bias lines because a thin line is equivalent to an inductance compared to a thick one. Therefore, RF chock inductances could be neglected when the thin transmission lines are utilized. Simultaneously, a resistor is placed at gate ends in order to prevent from the low-frequency oscillation. And a bypass capacitance is put at drain ports so as to cut off DC leakage completely. In order to think over the EM characteristics of the passive circuits, the EM software of HFSS and Sonnet is adopted to simulate the interference of passive devices each other. The length of transmission lines and the gap in two lines are modified to eliminate the interference. And the active devices at the power stage are arranged in parallel so as to solve the problem of overheating. The Fig.2.19 shows the photograph of this power amplifier, marked out the input port RF_IN, the output port RF_OUT, and biasing points Vgs and Vds.

2.3.4 Simulations

The fig.2.20 shows that the PAE and Pout alter versus input power Pin. The output power is 19.4dBm and the PAE is 27.4% at the 1dB compression point. The maximum output power level is 20.5dBm at Pin=10dBm. The maximum value of PAE is 35.9% at the maximum output power point due to the equation of PAE=Pout/Pdc * (1-1/Gain) shown in Eq. (2.2). The Fig.2.21 depicts that the Pout and Gain vary versus input power Pin. The constant power gain is maintained at 16.5dB when the input power is smaller than 2dBm. The Fig.2.22 describes that the PAE and Pout vary versus frequency. Observed this diagram, the bandwidth of this circuit can be determined by the testing input power Pin=0dBm. It is about 1GHz. The Fig.2.23 shows that the fundamental and third-harmonic components vary versus input power Pin in order to examine the IIP3 and OIP3 points. The IIP3 point is about 20dBm and the OIP3 is 40dBm nearly. The result is appropriate for this design. The overall specifications are shown in the Table.2.1.

2.3.5 Measurements

The measurement of this power amplifier utilizes the on-wafer test in order to eliminate the parasitic inductances resulting from bonding wires at the RF input and output ports. The power lines are connected by gold bonding wires to supply the DC voltages. Firstly, the VNA HP8510C is adopted to determine the central frequency. Then, the source generator Agilent 83640B creates the signals of different power levels at this frequency to estimate the performance of this power amplifier. At Vds1=2.15V、Vgs1=-0.45V and Vds2=2.65V、Vgs1=-0.6V, the total drain current is 117mA. The measured maximum small-signal gain is 13.4dB at the central frequency of 32.4GHz, shown in Fig.2.24. The Fig.2.25 shows the experimental result of Pout and Gain versus input power Pin. And the experimental result of PAE versus input power Pin is depicted in Fig.2.26. The maximum power-driving ability

is 15dBm. And the largest PAE value is 23%. The experimental results are not the same as the simulated performances completely. Discussed the reasons, the S-parameter of the WIN 0.15um power device at designed frequency and biasing voltage must be confirmed by test-key devices. And the parasitic capacitances of the RF pads have to deliberate whether it's appropriate for the designed circuit or not. They are critical parameters to influence the performance crucially.

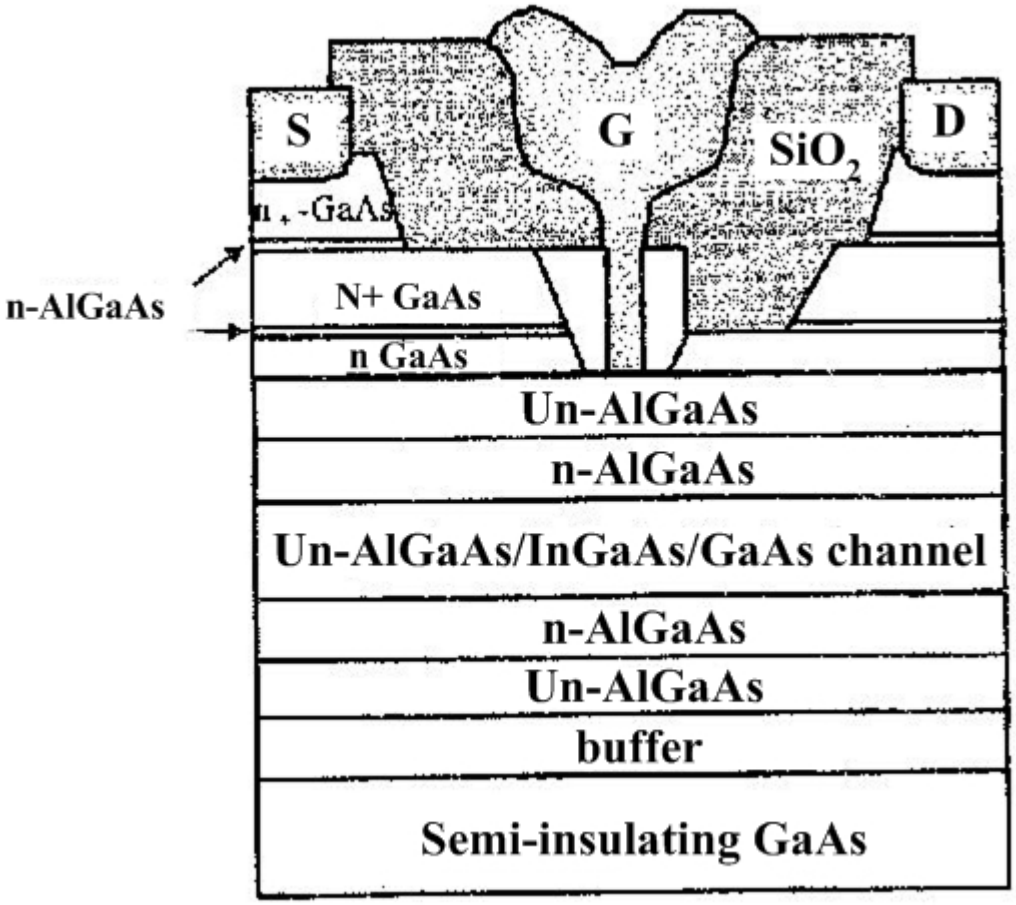

Fig.2.1 The schematic cross section of PHEMT

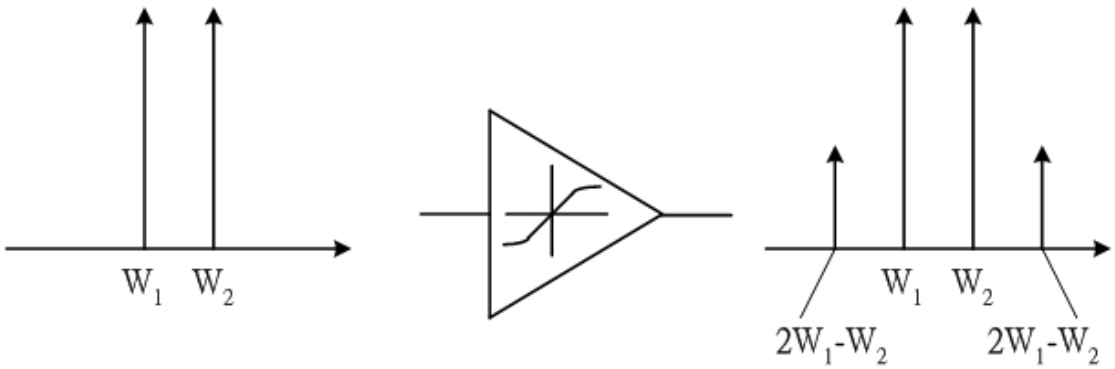

Fig.2.2 The third-order IM products resulted from the nonlinearity

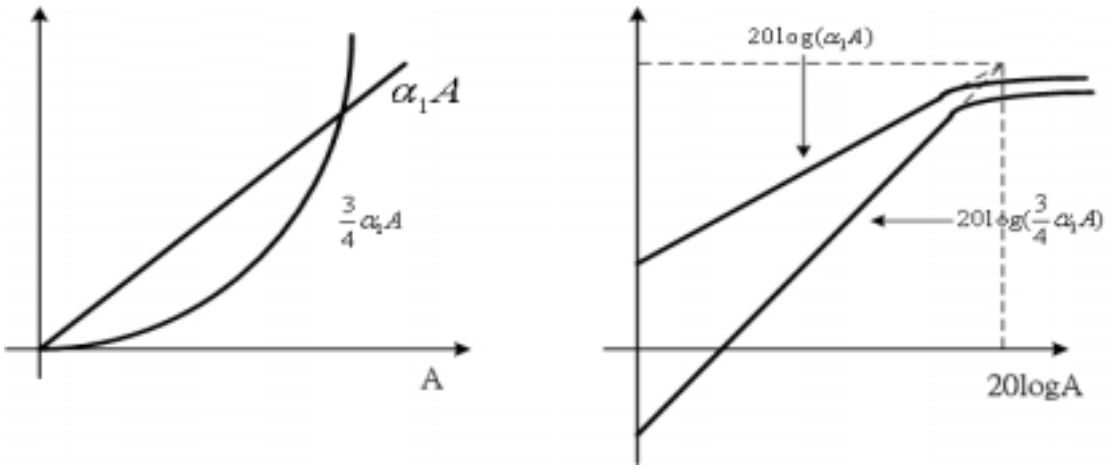

Fig.2.3 Third intercept point (IP3) has been defined to characterize the linearity

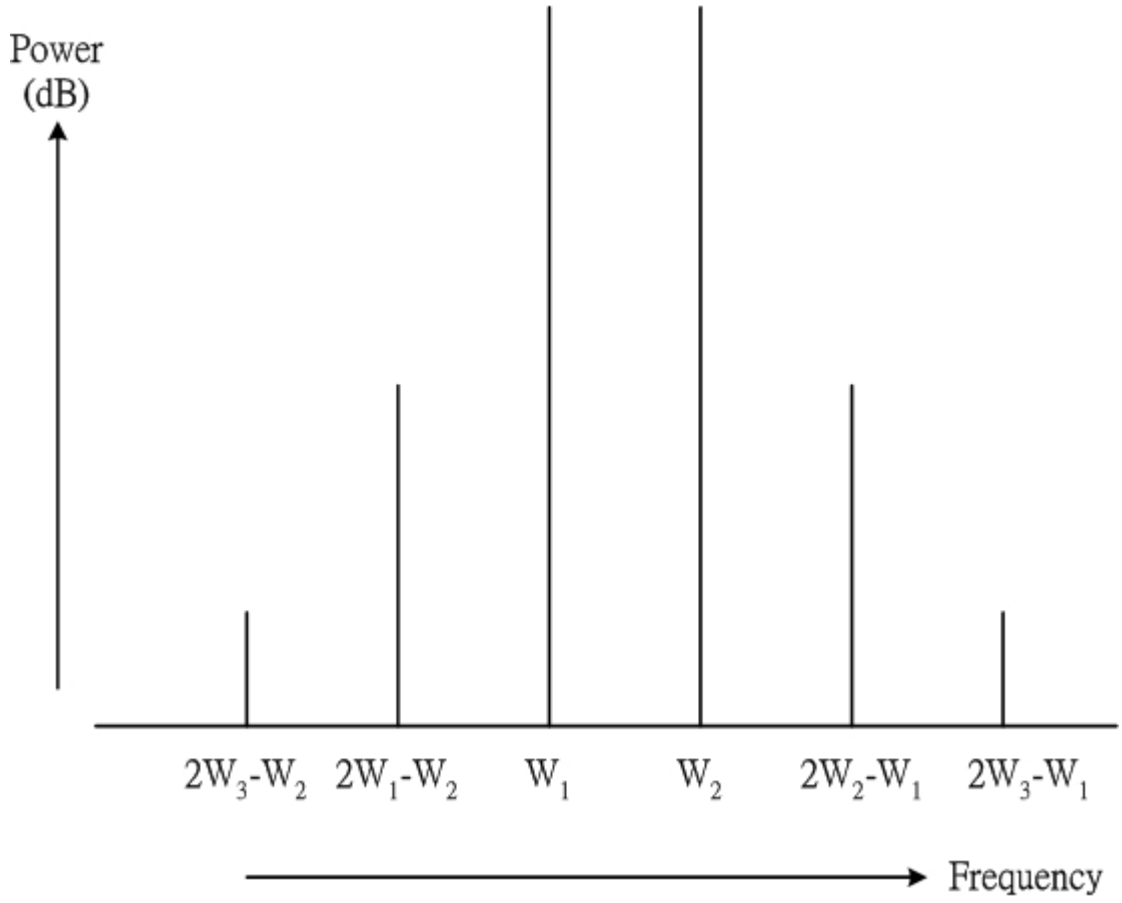

Fig.2.4 Two separate carriers with fixed spacing such as the AM of a signal carrier

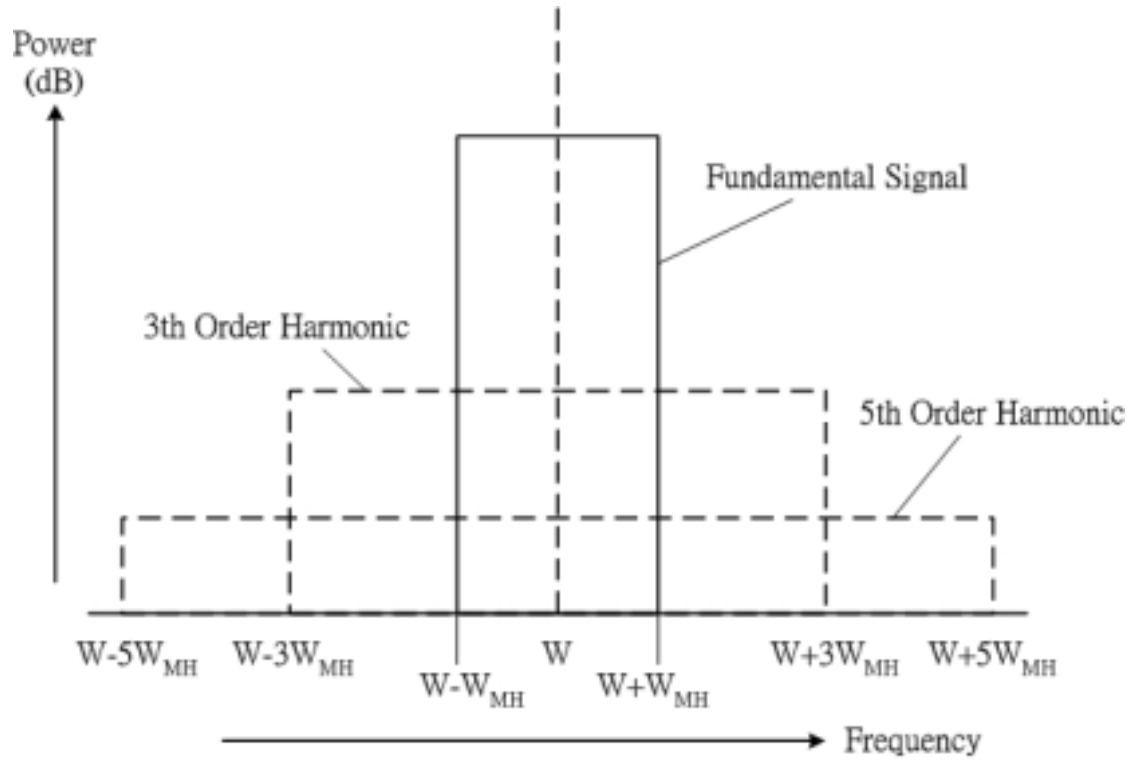

Fig.2.5 The composition of the adjacent channel leakage power is illustrated

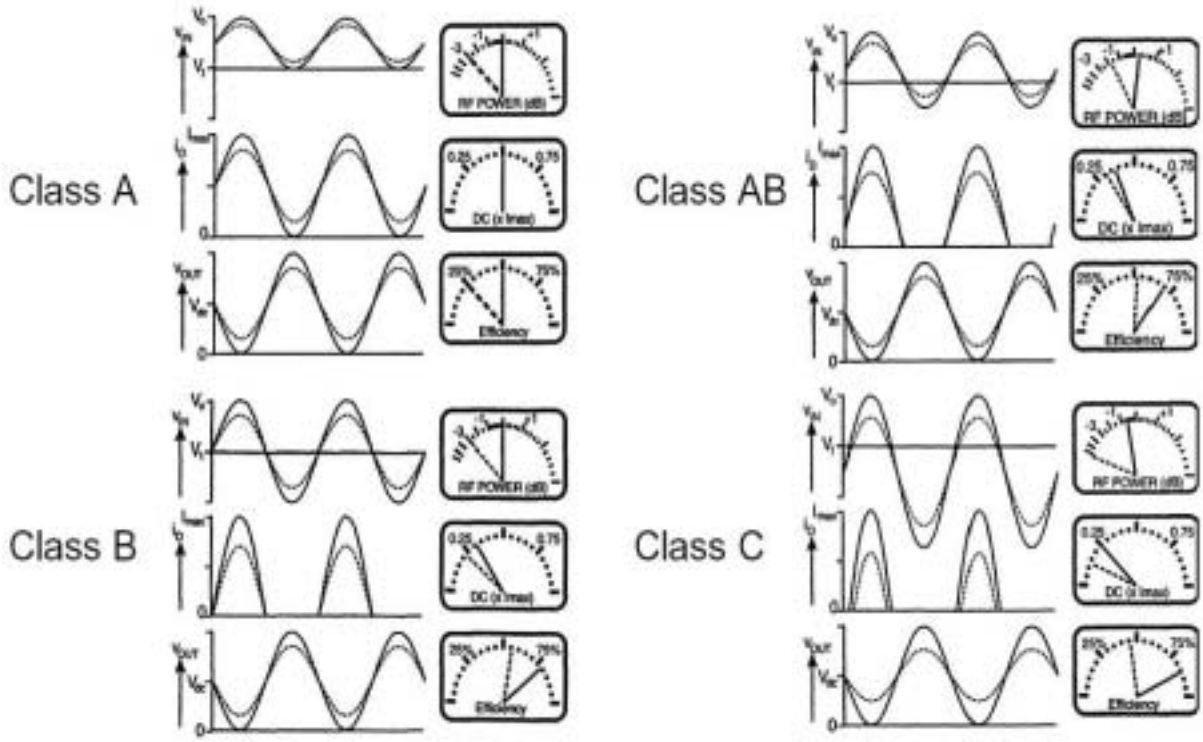

Fig.2.6 The numerous classic modes of operation are discussed

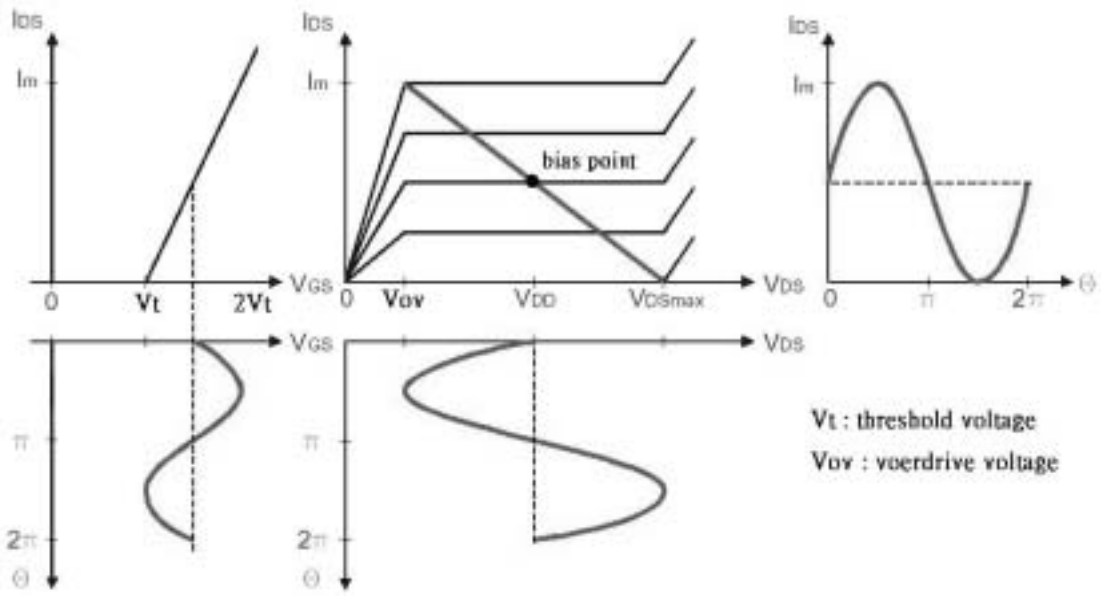

Fig.2.7 The operation of class A mode

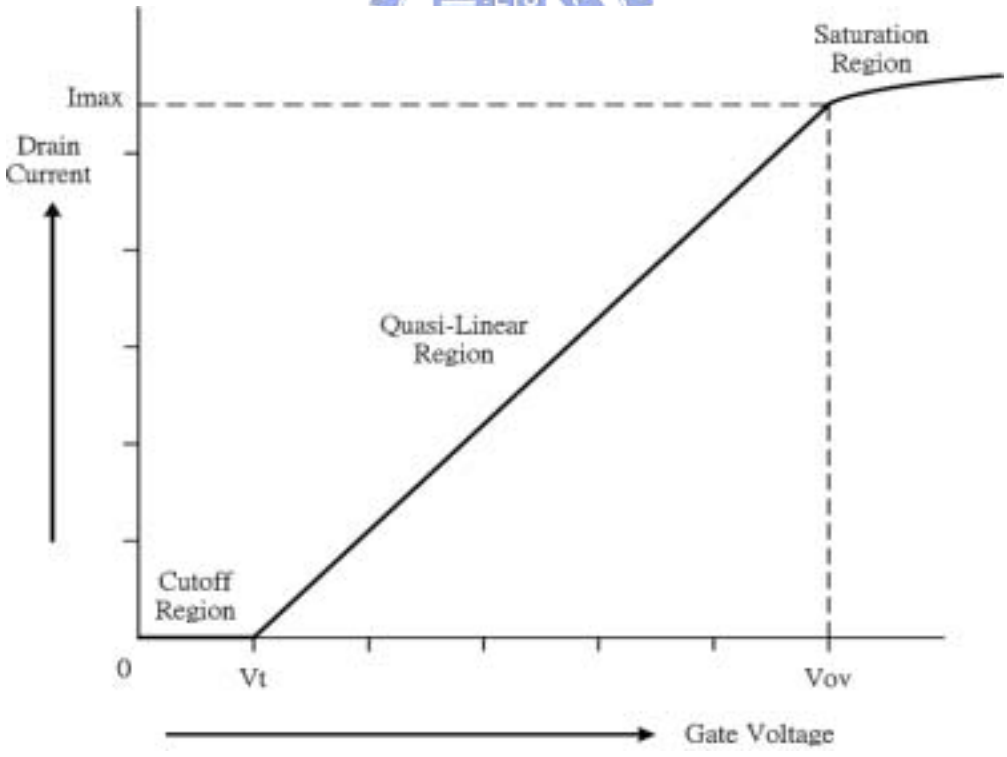

Fig.2.8 An idealized RF device, having a linear transconductive region

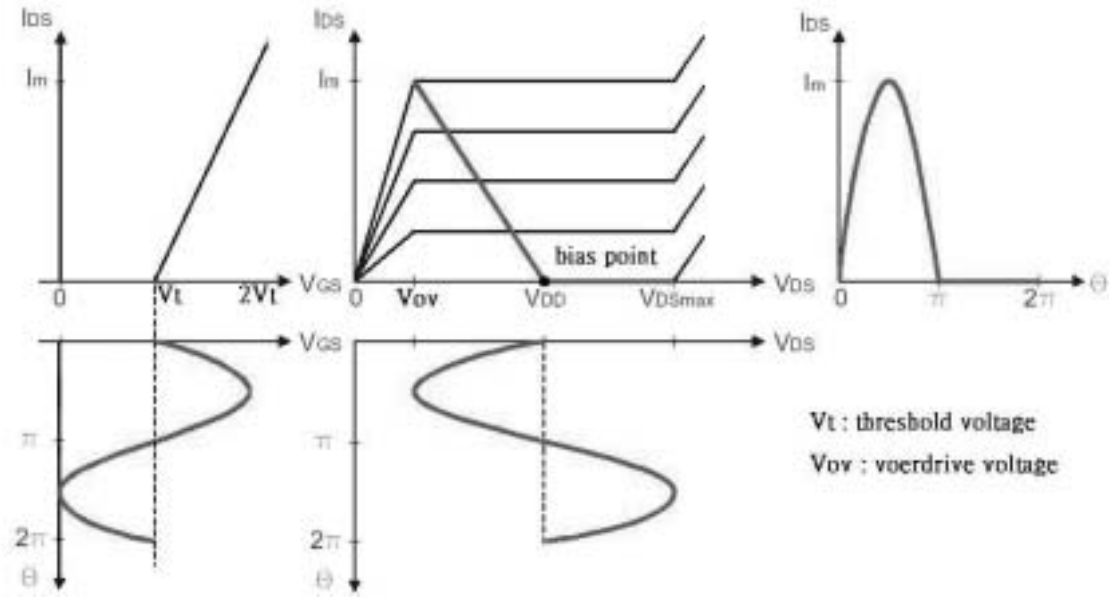

Fig.2.9 The operation of class B mode

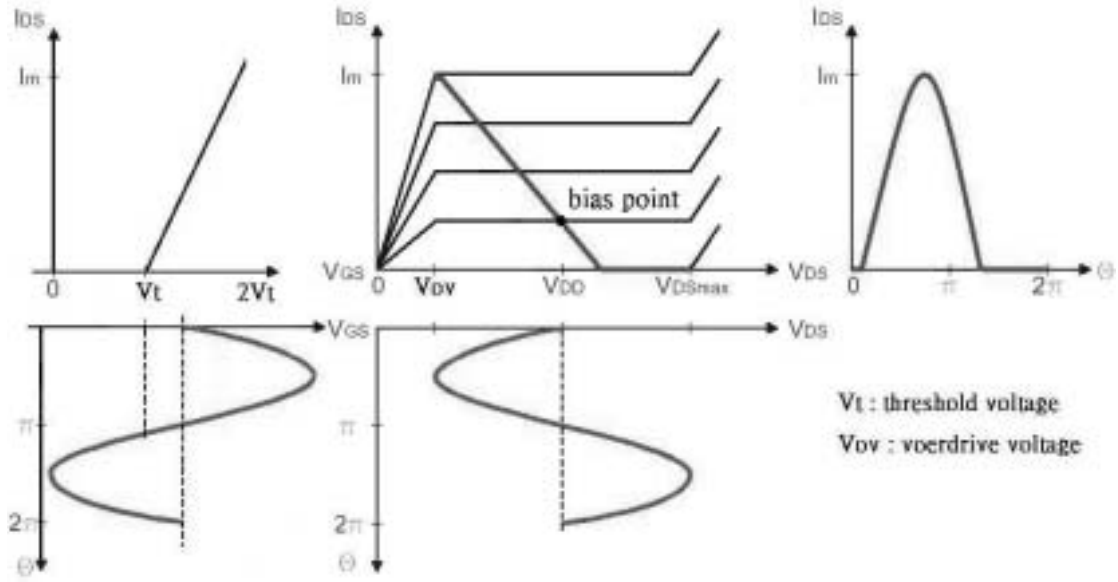

Fig.2.10 The operation of class AB mode

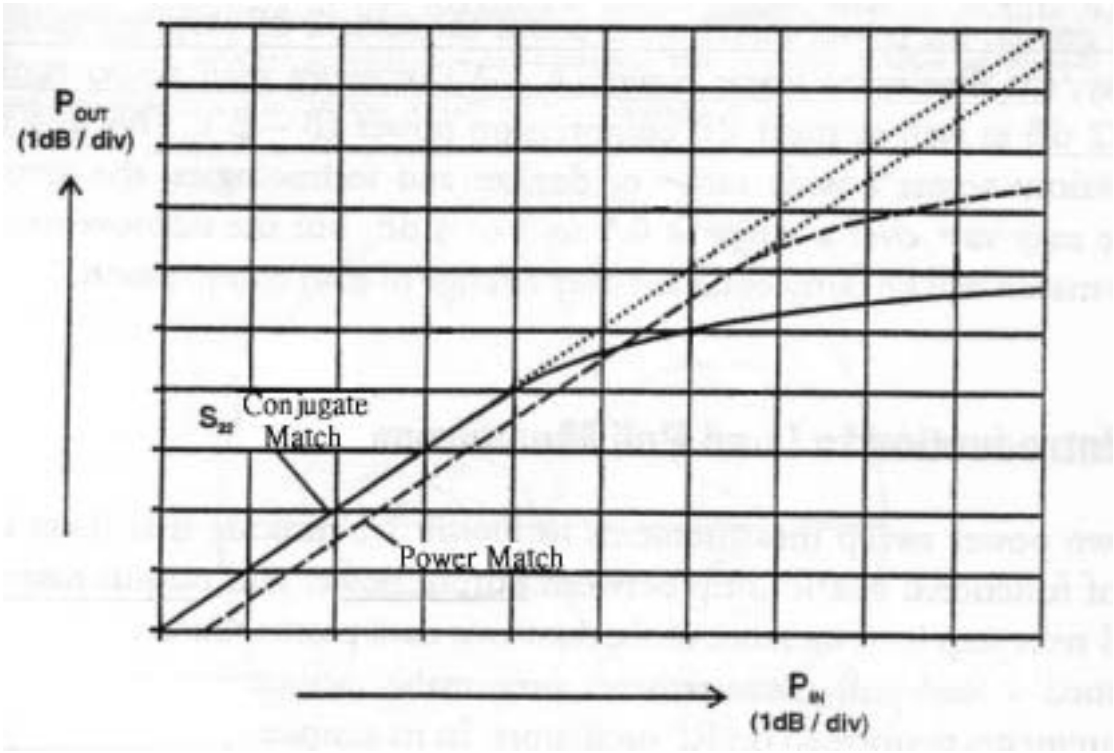

Fig.2.11 The comparison of power-driving ability between the conjugate match and the power match

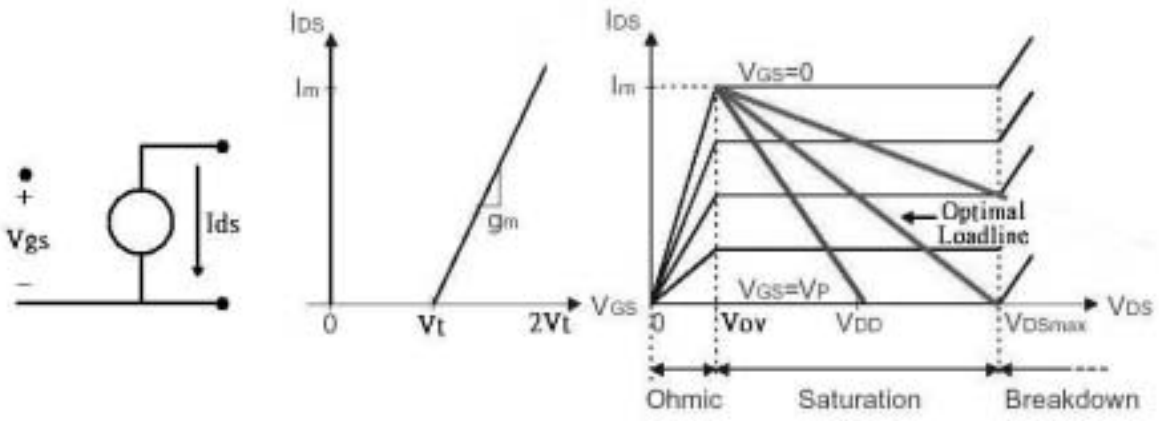

Fig.2.12 The load-line resistors are determined

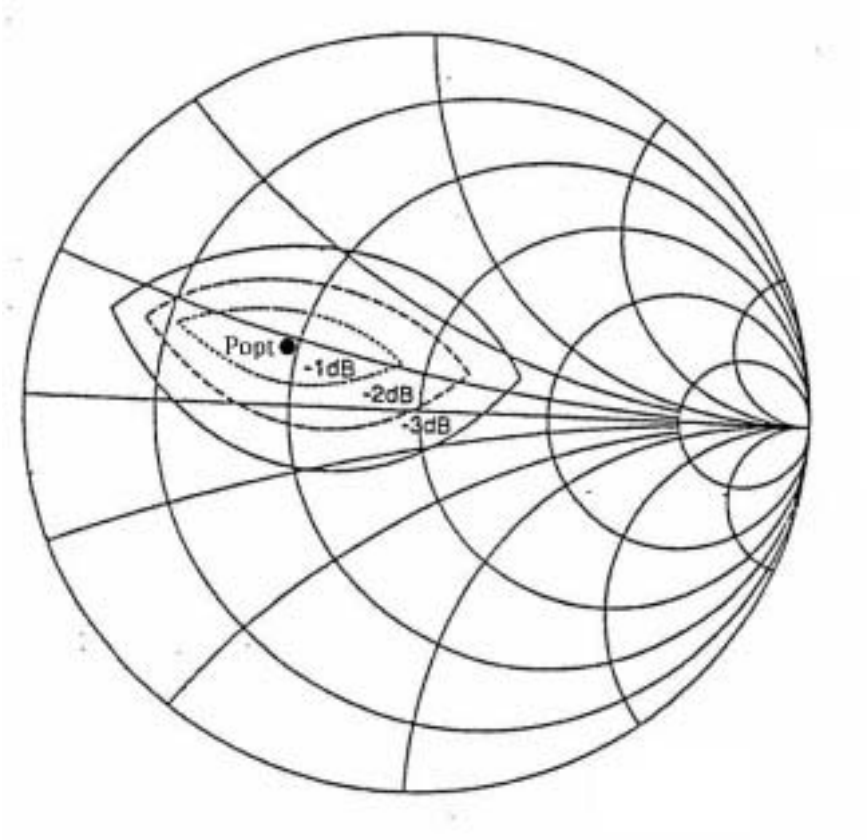

Fig.2.13 The constant power contours are illustrated

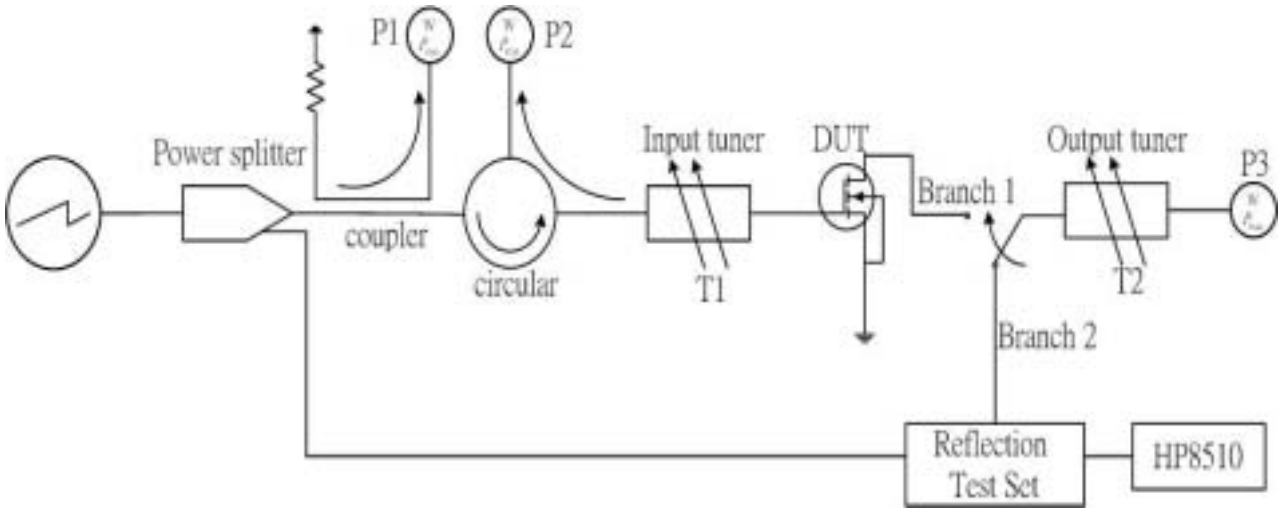

Fig.2.14 The setup of load pull measurement

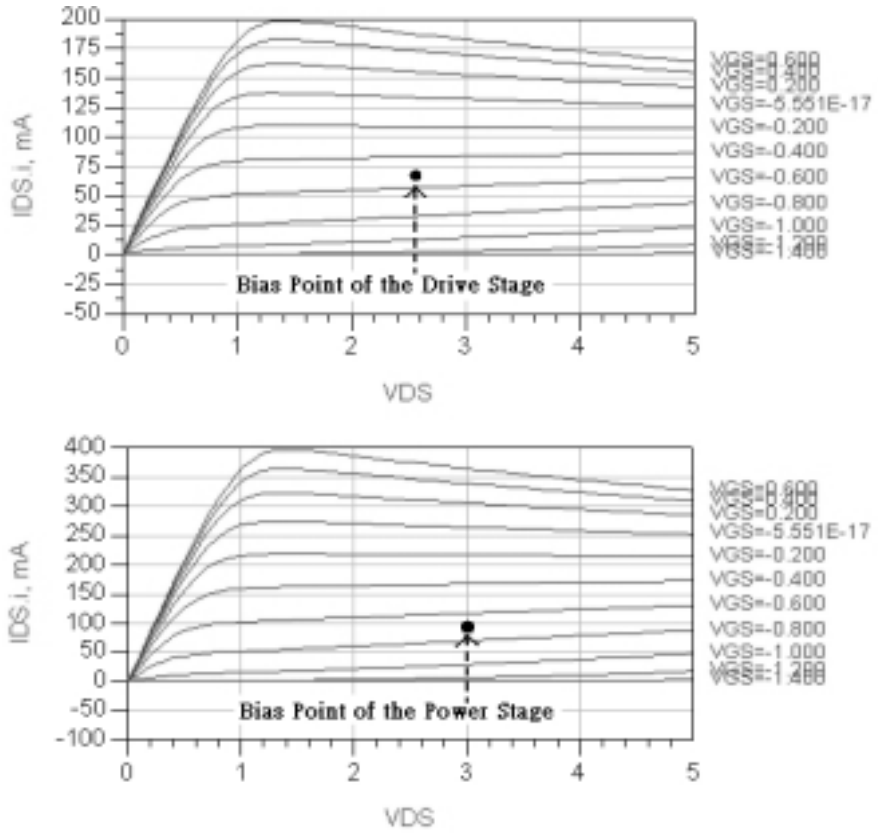

Fig.2.15 The operating points of the two stages in this power amplifier

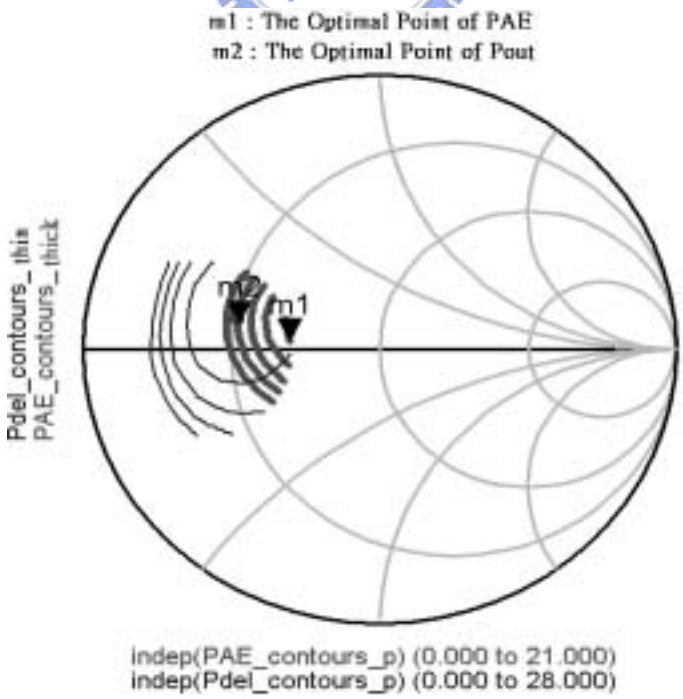

Fig.2.16 The constant power and PAE contours

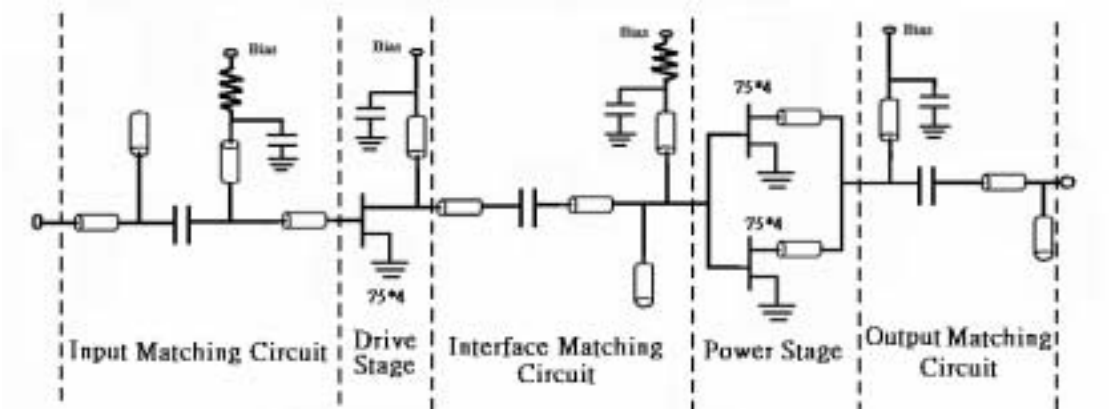

Fig.2.17 Whole schematic of this 38GHz power amplifier

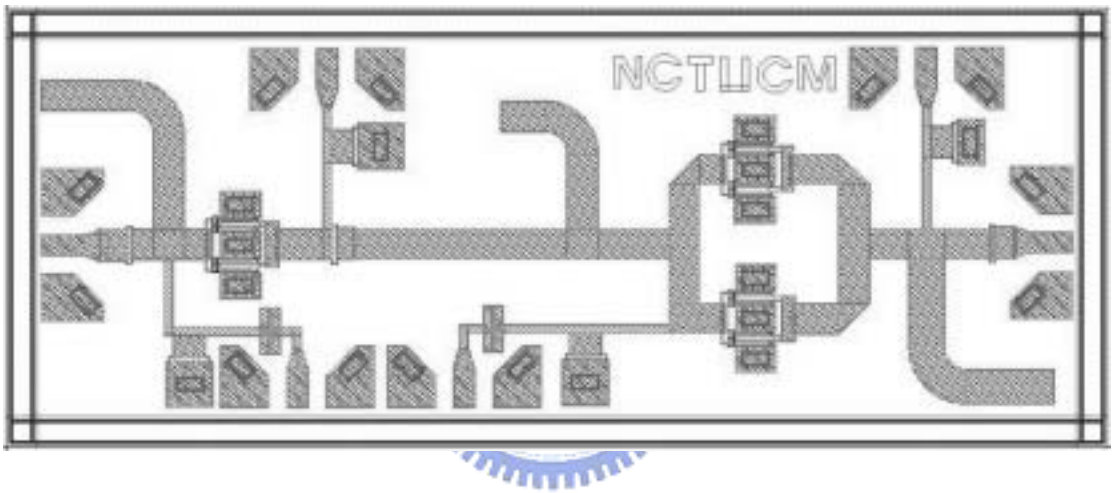

Fig.2.18 Layout of this 38GHz power amplifier

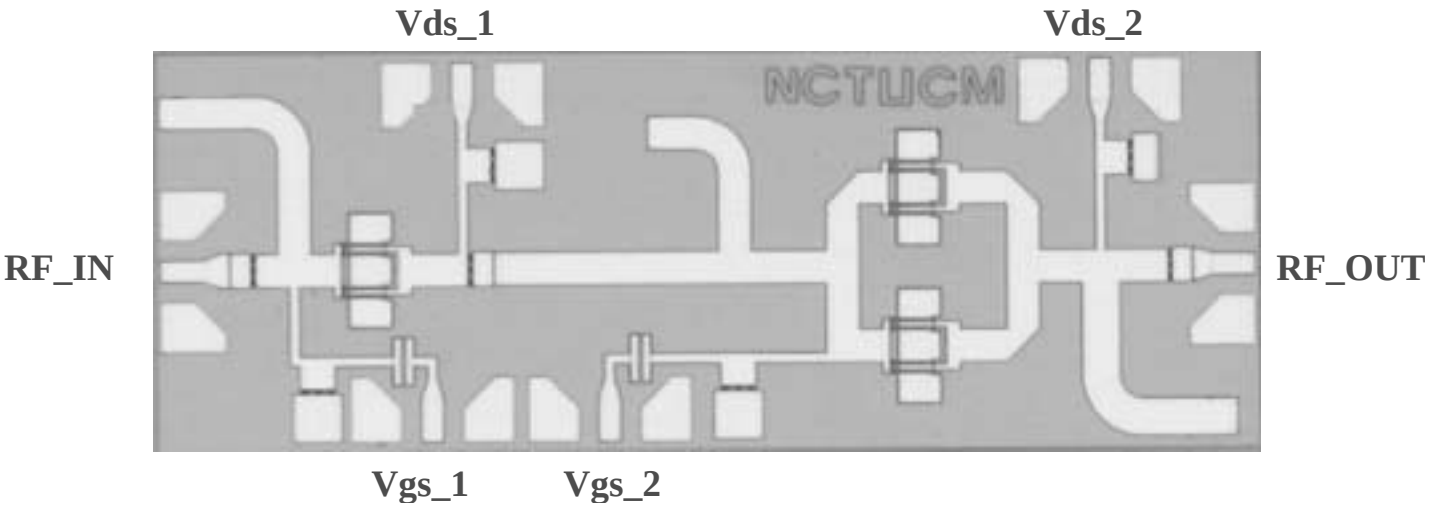

Fig.2.19 Die photograph of this 38GHz power amplifier

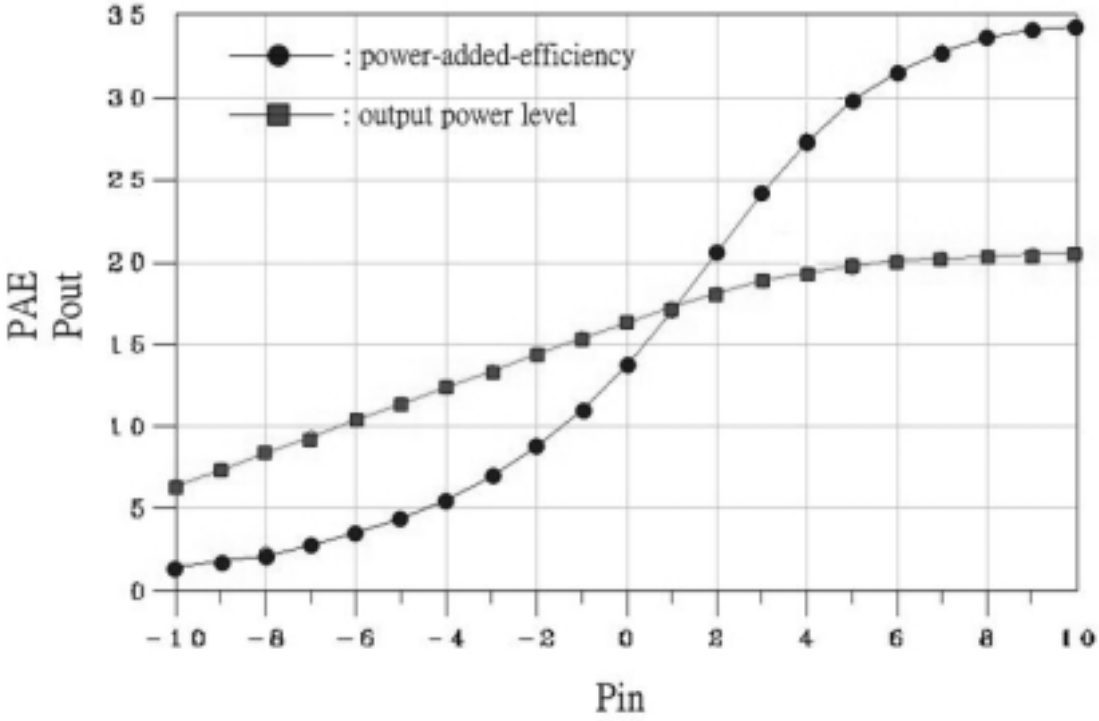

Fig.2.20 PAE and Pout versus input power Pin

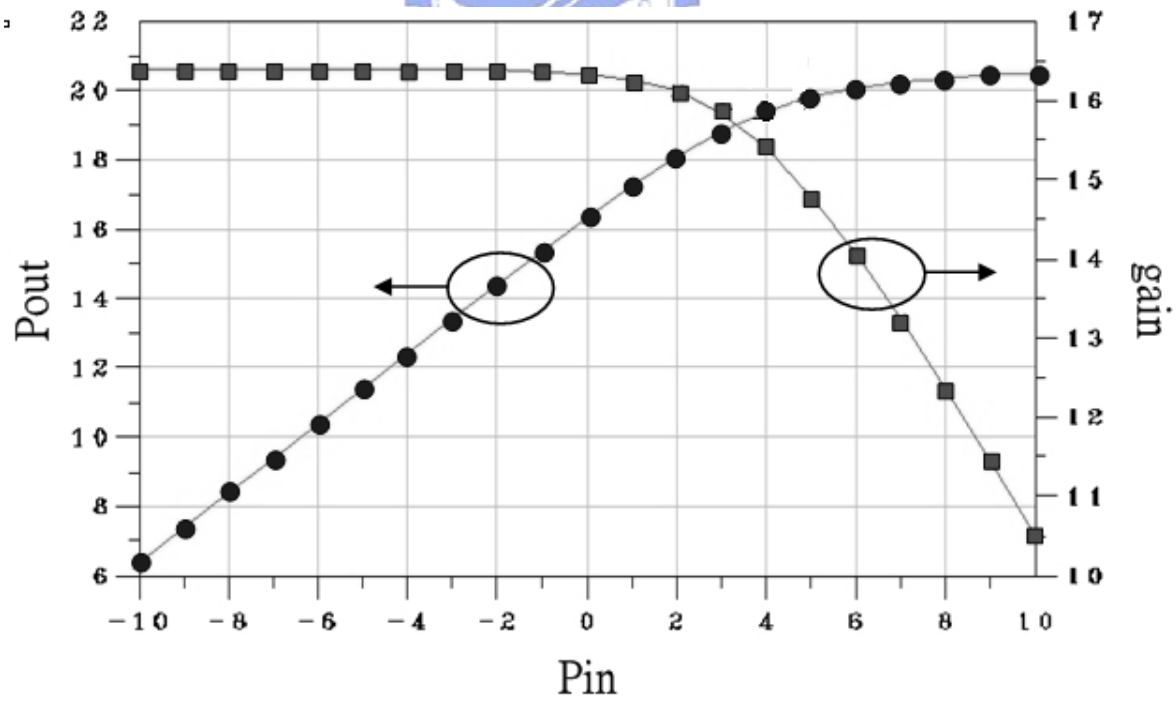

Fig.2.21 Pout and Gain versus input power Pin

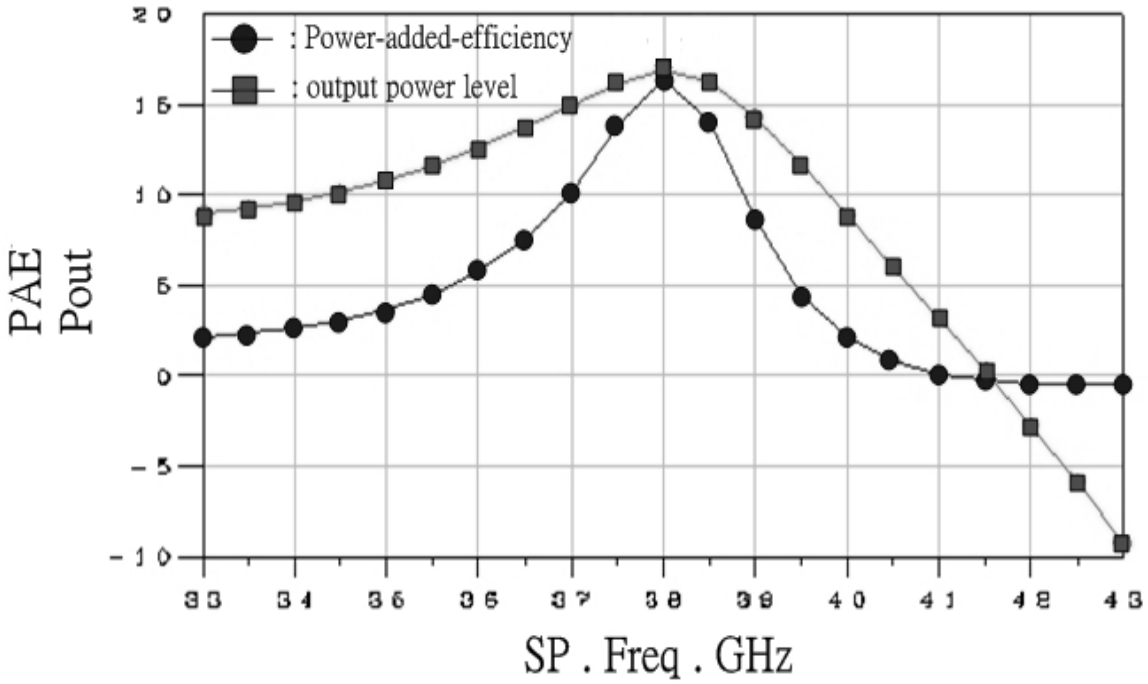

Fig.2.22 PAE and Pout versus frequency

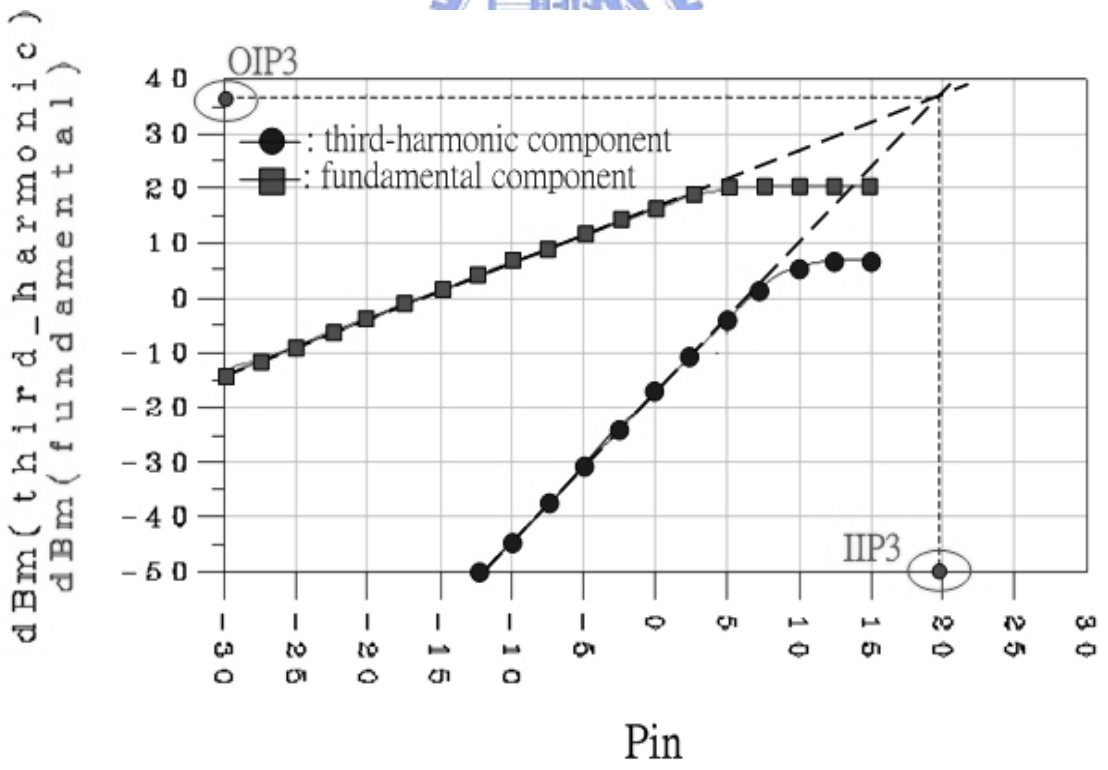

Fig.2.23 Fundamental and third-harmonic components versus input power Pin in order to examine the IIP3 and OIP3 points

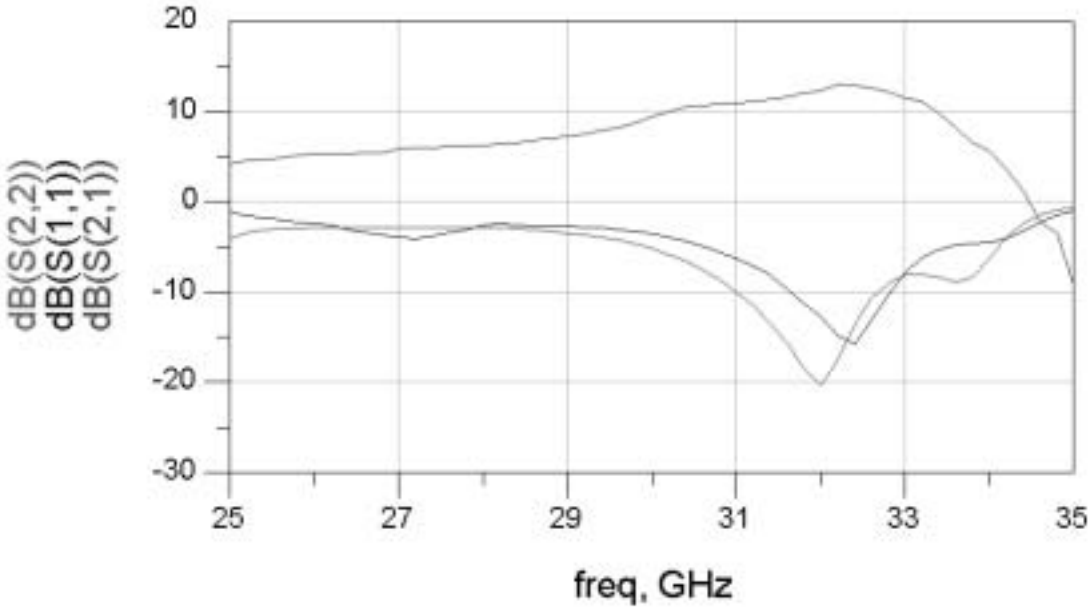

Fig.2.24 The experimental small-signal S parameter of this power amplifier

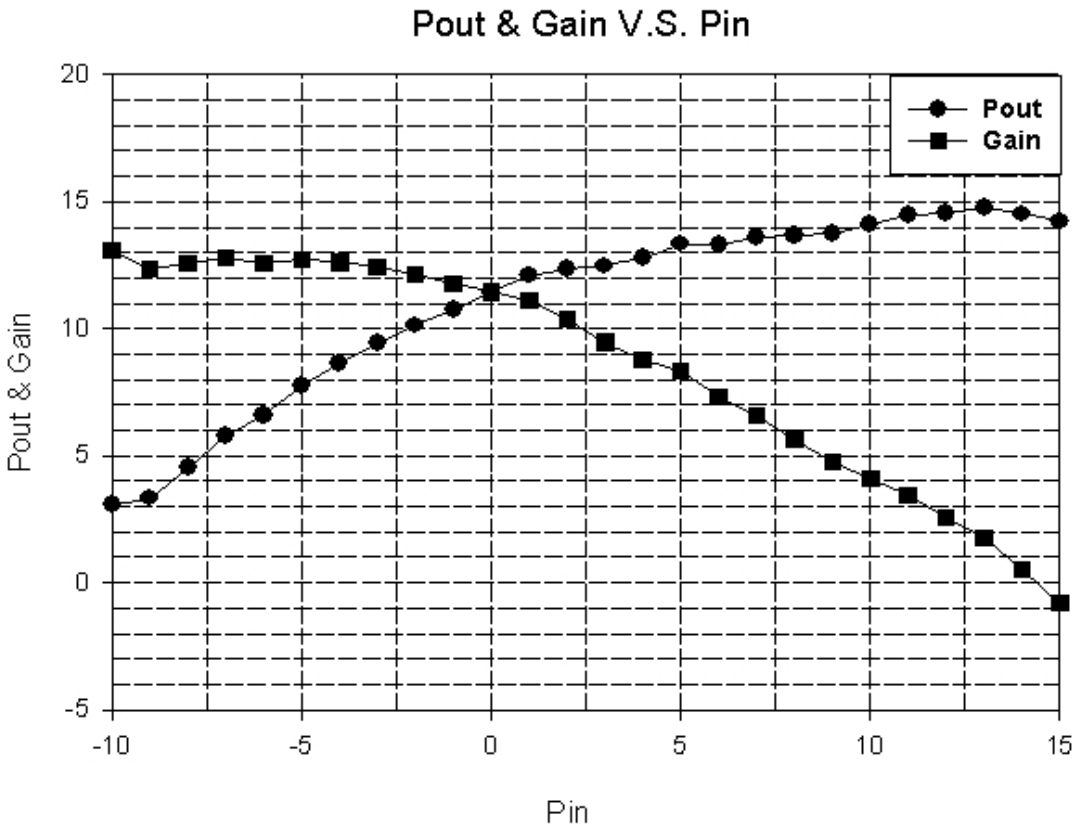

Fig.2.25 The experimental result of Pout and Gain versus input power Pin

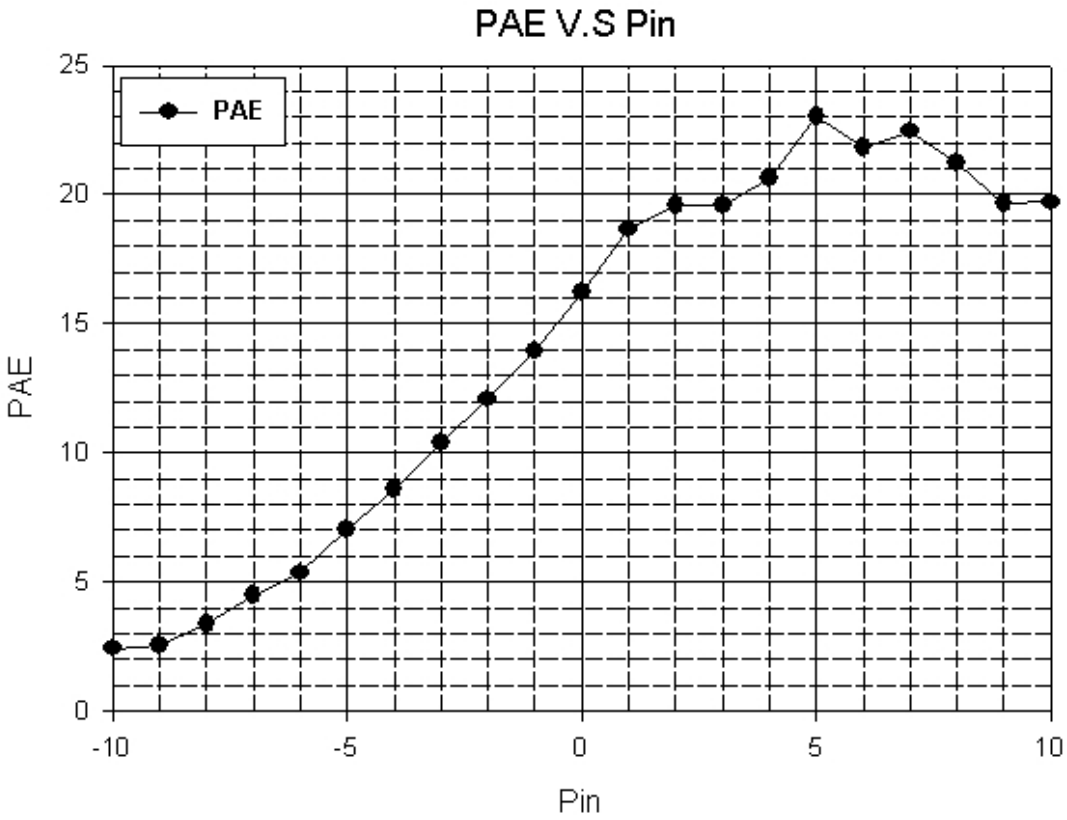

Fig.2.26 The experimental result of PAE versus input power Pin

specification	Result
Id(driver)@P1dB	64.5mA
Id(output)@P1dB	73mA
Centra1 frequency	38GHz
P-1dB	4dBm
Pout(fundamental)@P-1dB	19.59dBm
Pmax	20.5dBm
PAE(%)@P-1dB	29.9%
PAE(%)Pmax	35.9%
3-order IMD	>-30dBc@Pin=-5dBm
IIP3	20dBm
OIP3	40dBm
Input VSWR	<2
Output VSWR	<3
Bandwidth	1GHz
Chip size	2.5 x 1 mm^2

Table.2.1 The simulated specifications of this power amplifier

specification	Result
Id(driver)@P1dB	51.5mA
Id(output)@P1dB	60.7mA
Centra1 frequency	32.4GHz
P-1dB	2dBm
Pout(fundamental)@P-1dB	12.4dBm
Pmax	15dBm
PAE(%)@P-1dB	19.7%
PAE(%)Pmax	23%
Input VSWR	1.38
Output VSWR	2.61

Table.2.2 The experimental specifications of this power amplifier

CHAPTER 3

A Novel Bi-Directional Amplifier with Gain Control Utilizing Reflection-Type Amplifiers

Retro-directional antenna arrays are applied in many wireless communication systems, such as RF identification apparatuses and intelligent transport systems. These kinds of antenna systems can reflect the received signals along the incident direction without any portended signals.

There are two familiar categories of retro-directional antennas. One is the type of phase-conjugated-array elements; the other is the form of Van Atta arrangement. The former antenna has to connect an oscillator on each unit cell in order to form the conjugated phase. Therefore, the reflection-type waveform transports along the incident way by this approach. The advantages of this antenna are that the distance between random unit cells can be the same. And it is able to modulate readily the reflected signals by modifying the operating frequency of oscillators. Nevertheless, the frequent difference between the RF and LO signals of each oscillator must be large extremely. This shortcoming will make the antenna system much complex and expensive. The antennas of Van Atta arrangement have to let each unit cell symmetrize to the central point. And two unit cells are connected by simple microwave transmission line. The framework of the antenna of Van Atta arrangement is shown in Fig.3.1 (a). The corresponding electric field in the incident direction is $E_{Passive}(\theta) = C.\ N.\ F^2(\theta)$, where C is the constant value which has relations with the distance of a signal source and the strength of an incident waveform, N is the amount of antennas in the array and $F(\theta)$ is the pattern of each unit cell. For the sake of improving the strength of the radiating field, the transmission line can be replaced by an active amplifier, as shown in Fig.3.1 (b) and Fig.3.1 (c). The

architecture in Fig.3.1 (b) only has a half of antennas in the array to receive the incident waveform due to utilizing a unilateral amplifier. This kind of antennas possesses the corresponding field $E_{Uni\text{-}amp}(\theta) = C.\ N/2.G.\ F^2(\theta)$, where G is the gain of a unilateral amplifier. If the architecture adopts a bi-directional amplifier, each unit antenna can be used to receive and transmit a signal, which field is $E_{Bi\text{-}amp}(\theta) = C.\ N.\ G.\ F^2(\theta)$. Compared with two architectures, we can acquire a conclusion that the reflected power level of a system which adopts a bi-directional amplifier has 6dB much than the one with a unilateral amplifier. Similarly, when two antennas are designed to have the same reflected power level, the system which utilizes a bi-directional amplifier can reduce the half amount of unit antenna cells.

Based on the above-mentioned discussions, a bi-directional amplifier plays a significant role in the Retro-directional antenna system of active Van Atta arrangement. When a bi- directional is designed to possess the high gain, the circuit must be watched out for the isolation of signal in the input port so as to prevent the reflected signal from affecting the circuit performance of the input port. The circuit of a bi-directional amplifier also has to be devised to have the lower noise figure as far as possible. So, the noises of this circuit itself will not interference the output signal. And the system will own the better performance.

3.1 Architecture of the Bi-Directional Amplifier

This research proposes and demonstrates a novel architecture of 2.4GHz bi-directional amplifier. This approach can improve effectively the isolation and noise figure of the circuit to ameliorate the quality of output signal. This framework includes two reflection-type amplifiers and a 90 degree branch-line hybrid. The designed process must pay attention to the oscillation condition of this circuit because its principles are similar to them of an oscillator. The contents of this paper below

will introduce the complete framework of this bi-directional amplifier in detail and discuss the principles and considerations of each section.

The figure Fig.3.2 is the whole framework of a bi-directional amplifier, which embraces two reflection-type amplifiers and a 90 degree branch-line hybrid. The PortI and PortII is the input and output ports of this amplifier. The role of two ports can be exchanged due to its bi-directional amplified capability.

A reflection-type amplifier is the device of only one end as the input and output ports. The branch-line circuit can separate the input signal into two output signals with the phase difference of 90 degree and the same power level, and eliminate the signal at isolation port. In accordance with the principles of this circuit above, two signals produced by the branch-line circuit will be amplified by the reflection-type amplifiers and flash back to the hybrid circuit. If one signal is imported into the PortI now, the output signal at the PortII will acquire an amplified signal which gain is the same as that of a reflection-type amplifier. In the meanwhile, the reflected signals at PortI form the destroyed interference to improve the isolation of this circuit. On the contrary, the similar result will be obtained if the signal is imported into the PortII.

The conventional branch-line circuit must be realized by means of transmission lines with the quarter wavelength. This length is about 17mm at the operating frequency of 2.4GHz. If this circuit is completed by adopting lump devices, the overall architecture has to include four capacitances and four inductances. Therefore, these two approaches both are inappropriate for CMOS IC. This 90 degree branch-line circuit is realized on a FR4 board for these reasons and utilizes a new method to reduce the area to 6.5 square millimeters. So, this IC only embraces these two imperative reflection-type amplifiers. The content below will focus on the designed techniques of this reflection-type amplifier and branch-line circuit in detail.

3.2 Design Considerations and Results

3.2.1 Theories of the Reflection-type Amplifier with Gain Control

The principles of a reflection-type amplifier are similar to them of an oscillator. The circuit must be designed to produce negative impedance at the input port at the operating frequency. The Fig.3.3 is the general diagram of a negative resistance reflection-type amplifier. The schematic embraces a negative resistance device, a stabilization matching network, a transformer network and a circulator circuit. A negative resistance device is accomplished by a triple-well NMOS in this case. And a stabilization network is responsible to decrease the mismatch in the input port and prevent from oscillation. The transformer network adjusts the input impedance to the regulation impedance 50Ω. Furthermore, a circulator circuit is applied to separate the reflected signal from the incident signal. The total power gain G (f) is

$$G(f) \cong \left|S''\right|^4 \cdot \left|\rho_A(jw)\right|^2 \tag{3.1}$$

The circulator is characterized by its cyclically symmetric forward and reverse transmission and input reflection scattering matrix elements S'', S''', and S'. An ideal circulator possesses the relations of S'=S'''=0 and S''=1. And the reflection coefficient ρ_A at interface of the stabilization matching network and the transformer network is

$$\rho_A = \frac{Yb^* - Ya}{Yb + Ya} \tag{3.2}$$

The parameter Ya is the input admittance of the stabilization network and Yb is the input admittance of the transformer circuit. The relation of $|\rho_A|$>>1 must be obeyed in this case because a negative resistance causes the equation of $\mathrm{Re}(Ya)$<0.

The total circulator forward transmission $|S''|^4 \leq 1$ is relatively constant over the circulator's pass band so that the amplifier is accomplished by the synthesis of the stabilization network for a particular $|\rho_A|^2$. Therefore, the parameter ρ_A has to be devised carefully to fit the relations discussed above in order to provide the sufficient gain of this amplifier.

The real and imaginary parts of this impedance have to conform the function Re(Zin+Zs)≈0 and Im(Zin+Zs)≠0, where Zin is the input impedance of the amplifier and Zs is the impedance of the signal source. In order to make the circuit possess high gain, the real part of this input impedance must be devised to approach 50Ω at the central frequency because the impedances of microwave signal sources are almost 50Ω. But the imaginary part of this impedance must be insured that its value isn't identical to zero so as to prevent from the oscillation. In figure Fig.3.4, the real and imaginary parts of this impedance are 67Ω and 7.5Ω. This condition is in accordance with the designed principles. Therefore, this amplifier owns the sufficient gain and maintains the stable condition.

The detail circuit framework of this reflection-type amplifier is shown in Fig.3.5. The overall architecture embraces a variable capacitance C_{cont}, a parallel circuit of C_s and L_s to control the central frequency, the loaded impedance R_{load} and L_{load} in the drain end and a capacitance Cgs' to modify the real part of the input impedance. In the aspect of the transistor, the TSMC 2.5v RF triple-well NMOS is assigned. This transistor is made up of 32 figures and biased at Vg is 1v and Vd is 2.5v in order to acquire the appropriate S parameter.

The input impedance R_{in} of this circuit is able to estimate roughly by means of the simple MOS model shown in Fig.3.6. The resistance r_o is large and Zs is exchanged by a LC parallel circuit. Assumed that the resonated frequency of this

LC circuit is $w_0 = 1/\sqrt{LC}$, the R_{in} can be obtained roughly by

$$Rin = Z_2 - j\frac{(1+gm)}{wCgs} * Z_2 = \frac{(1+gm)L}{Cgs(1-(\frac{w}{w_o})^2)} + j\frac{wL}{1-(\frac{w}{w_o})^2} \qquad (3.3)$$

Relied on the function above, the frequency of arising negative impedance is proved that it is related with the resonated frequency of LC circuit. Therefore, the central frequency can be altered by modifying the value of L and C. And the magnitude of negative impedance can be controlled by the capacitance Cgs.

The architecture of this reflection-type amplifier adopts the gate end as the input and output port. The thermal noise is lower because the current of gate end is smaller than that of drain and source end. Furthermore, a circuit produces the flicker noise when the drain current flows through the channel of the transistor. Therefore, as the drain or source end is selected as the input port of this reflection-type amplifier, the noise figure will not be eliminated efficiently. But when the capacitance Cgs is altered to control the negative impedance, the noise will increase as the capacitance Cgs raises because the noise current source varies. So, this is a key point of selecting the magnitude of Cgs. The formula of the noise current source Ii^2 is shown below. And the MOS noise model is shown in Fig.3.7.

$$\frac{\overline{Ii^2}}{\Delta f} = 2qI_G + \frac{w^2 Cgs^2}{gm^2}(4kT\frac{2}{3}gm + K\frac{I_D{}^a}{f}) \qquad (3.4)$$

In order to settle the matching circuit of the drain end, the stable circle should be drawn primarily. The area including the center of unit circle is the unstable region due to the S parameter S22 is greater than one. When the matching circuit is devised to modify the S parameter into the unstable region, this amplifier can acquire negative

impedance surely. And by means of adjusting the reflection coefficient of the matching circuit, this method will ensure this amplifier the highest gain. The stable circle of the drain end is shown in Fig.3.8.

3.2.2 Results of Reflection-type Amplifier with Gain Control

The gain of this reflection-type amplifier is shown in Fig.3.9. This figure proves that this amplifier is not an oscillator because the output power level is linearly related with the input power level before the point P_{1dB}. The largest power gain is not opted because the linearity will degrade as the gain increases. Therefore, the figure Fig.8 reveals that the gain is 13.6dBm and P_{1dB} is -5dBm. Nevertheless, the gain and linearity can be modified by adjusting the value of the varied capacitance Ccont**.** And the received power level of this antenna system is very small generally. This amplifier should demand for a flat gain ranged among the smaller input power level. Therefore, the parameter P_{1dB} which equals -5dBm conform to the demand of this system.

The noise figure of this reflection-type amplifier is shown in Fig.3.10. When the noise figure is measured, the input port has to connect a circulator to separate from the input and output signal because this amplifier is the one port element. The noise figure of this circuit is 4.1 which changes with the external capacitance Cgs' and the varied capacitance Ccont**.**

The figures Fig.3.11 and Fig.3.12 reveal that the gain and input impedance of this reflection-type amplifier changes with the varied capacitance Ccont. The circuit adopts the MOS-type varied capacitance which connects the source and drain end of a MOS and alters the value of capacitance by means of adjusting the external voltage to modulate the interval between gate end and P+ substrate. The gain and noise figure of this reflection-type amplifier which varies with the control voltage Vcont are shown

in Fig.3.13. This figure reveals that the real part of the input impedance reduces and the gain degrades as the controlled voltage ranges from 2v to 0v. And the noise figure elevates when the gain lowers. The noise figure of this amplifier is between 4 and 5 approximately. The Table 3.1 shows that the parameters of this reflection-type amplifier vary in all kinds of process at the controlled voltage Vcont=1.3v.

3.3 Theories of the Branch-Line Circuit Utilizing Impedance Transformation

The transmission line's model of impedance transformation is shown in Fig.3.14. In accordance with the ABCD of the circuit, the impedance Z and phase θ can be obtained by the impedance transformation. The two equations can be obtained below.

$$Z = \frac{Zc}{\sin\theta} \quad \text{And} \quad wC = \frac{\cos\theta}{Zc} \tag{3.5}$$

Utilizing these two formulas, the scale of this reduced-size branch-line circuit is about 85% smaller than those of conventional hybrids by means of employing the open stubs and the external capacitances. The size of this reduced-size hybrid is about 7 millimeter square at 2.4GHz. The architecture of this hybrid is shown in Fig.3.15. The capacitances of 2pF are connected at Port5~8 to adjust the length of quarter-wave-long transmission line.

3.4 Experimental Results of the Branch-Line Circuit Utilizing Impedance Transformation

This hybrid possesses that S21、S31 are about -3.3dB and S11、S41 are about

-30dB. The phase difference between S21 and S31 is equal to the 180 degree approximately. And the magnitude of the input impedance is about 50Ω at the central frequency of 2.4GHz. All parameters of this hybrid are shown in Fig.3.16. This hybrid is simulated by the software **Sonnet**. These simulated consequences conform to the demands for this bi-directional amplifier. The photograph of the fabricated branch-line circuit is shown in Fig.3.17. And the experimental results are displayed in Fig.3.18. The results reveal that this proposed method is feasible to reduce the area of branch line circuits..

3.5 Complete Consequence of Bi-Directional Amplifier

This bi-directional amplifier is composed of the two reflection-type amplifiers and the 90 degree branch-line hybrid based on the architecture in Fig.2. The gain S21 and return loss S11 which vary with the control voltage $\mathbf{V_{cont}}$ from 0v to 2v are shown in Fig.3.19. The return loss is below -10dB which conforms the demand of common amplifiers. And the return loss becomes large as the gain S21 degrades.

The chip has to join a FR4 board with the hybrid circuit by means of bond wires. Therefore, the parasitical inductances are taken into consideration as this bi-directional amplifier is simulated. Otherwise, the circuit will oscillate due to the input un-matching circuit. The values of the parasitical inductances owing to bond wires are set as 1.5nH. The spectrum across DC to 5GHz is shown in Fig.3.20. This figure reveals that the return loss S11 is below zero whole spectrum range. This consequence means that the circuit is operated in the stable condition. But the varied capacitance can be adjusted to ameliorate unstable states which result from the parasitical inductances of bond wires. Therefore, the other capability of the varied capacitance is to improve the stability of this bi-directional amplifier.

The figure Fig.3.21 reveals that the worst case of noise figure is 5.4dB at

Vcont=0.4v. The gain is only 6.5dB in this condition. The specifications of this amplifier which compare with these of the others are shown in Table 3.2. The amplifier owns better performances than the others. And the expected specifications of this bi-directional amplifier are exhibited in Table 3.3. It also presents the variations of standards due to the variable capacitance. The layout is shown in Fig.3.23.

3.6 Measurement Considerations

The reflection-type amplifier is a device with only one port to play the roles of the input and output ends. Therefore, a 2.4GHz circulator circuit has to be placed on the input port when the reflection-type amplifiers are measured alone. Otherwise, the gain and noise figure are unable to be measured because the reflected signal mixes with the incident signal. The measured methods of the reflection-type amplifier are similar to these of the bi-directional amplifier described below. The architecture is exhibited in Fig.3.22.

The reflection-type amplifiers connect with the branch-line circuit on FR4 board by means of bond wires so as to form the bi-directional amplifier. Utilizing the vector network analyzer HP8510C, the gain S21 and the return loss S11 can be measured. Also, the oscillatory situation will be estimated by observing the spectrum across the overall operating scope. In relation to the noise figure, the noise figure meter of Agilent HP8970B is adopted to measure this parameter. In regard to the 1-dB compression point, the different power levels will be inputted into the tested devices. Observing the output power levels, this point can be obtained. The diagram of testing procedure is presented in Fig.3.22.

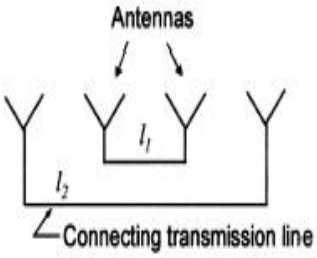

Fig.3.1 (a) Passive Van Atta retro directive directive array

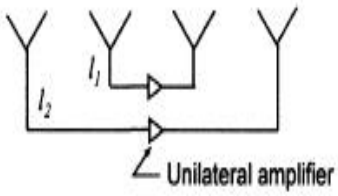

Fig.3.1 (b) Active Van Atta retro Array with unilateral amplifier

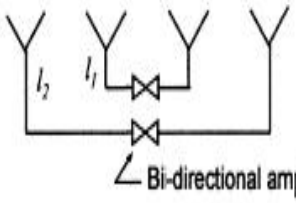

Fig.3.1(c) Active Van Atta retro directive Array with bi-directional amplifier

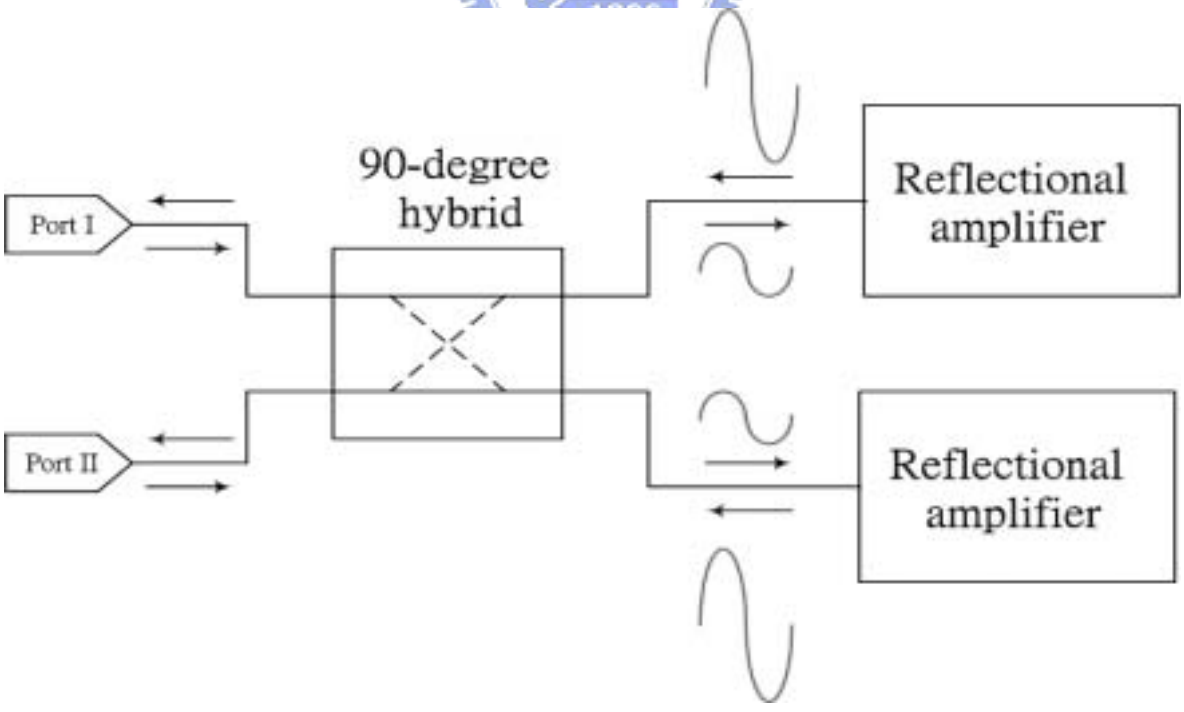

Fig.3.2 The framework of a novel bi-directional amplifier

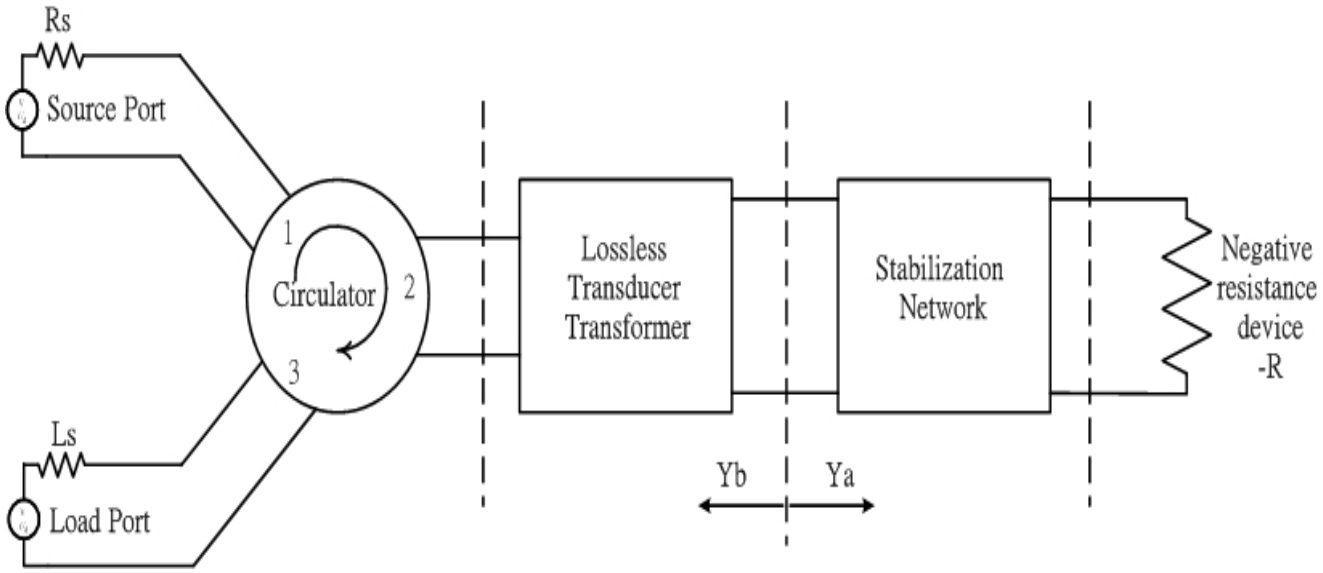

Fig.3.3 The configuration of negative resistance reflection-type amplifier

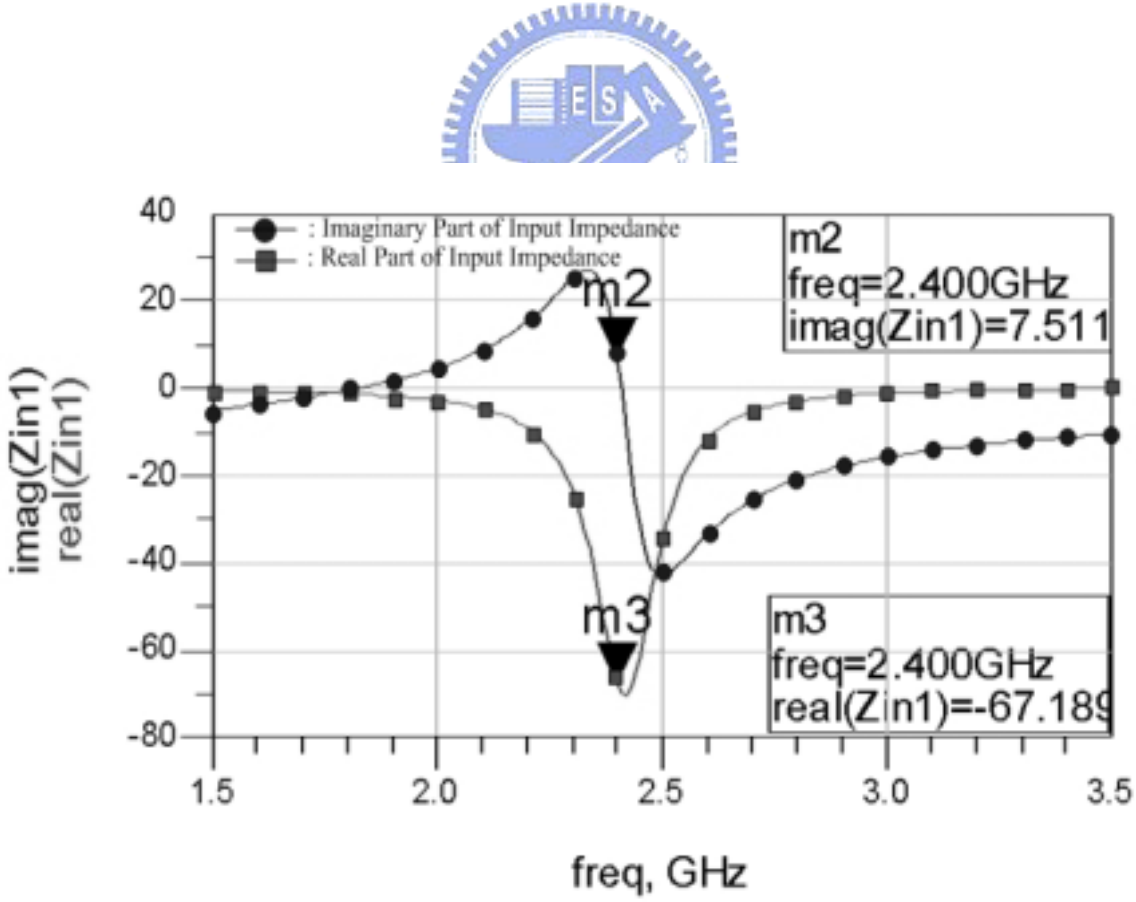

Fig.3.4 The input impedance of this amplifier

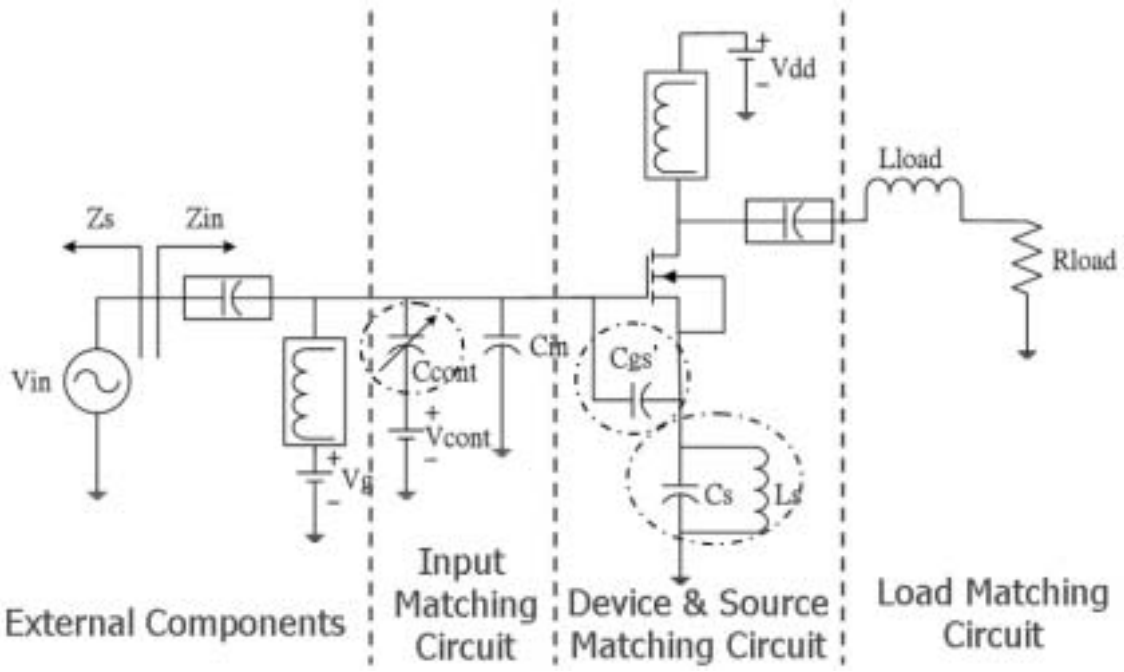

Fig.3.5 The framework of this reflection-type amplifier with gain control

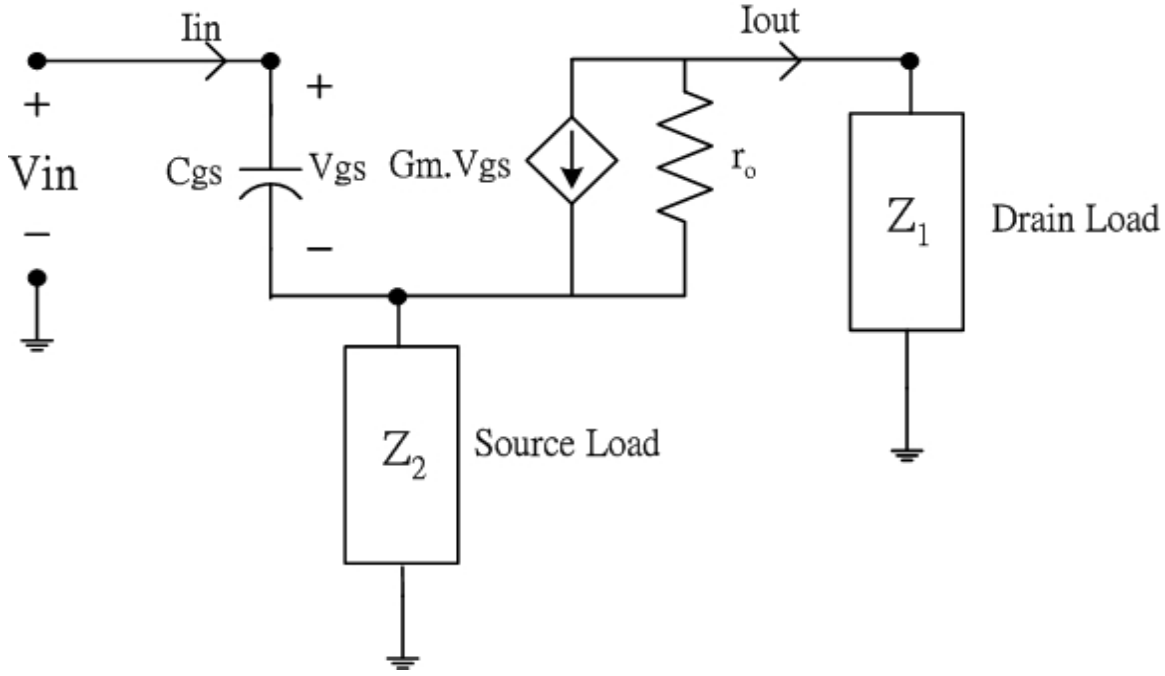

Fig.3.6 The MOS model with source and drain load

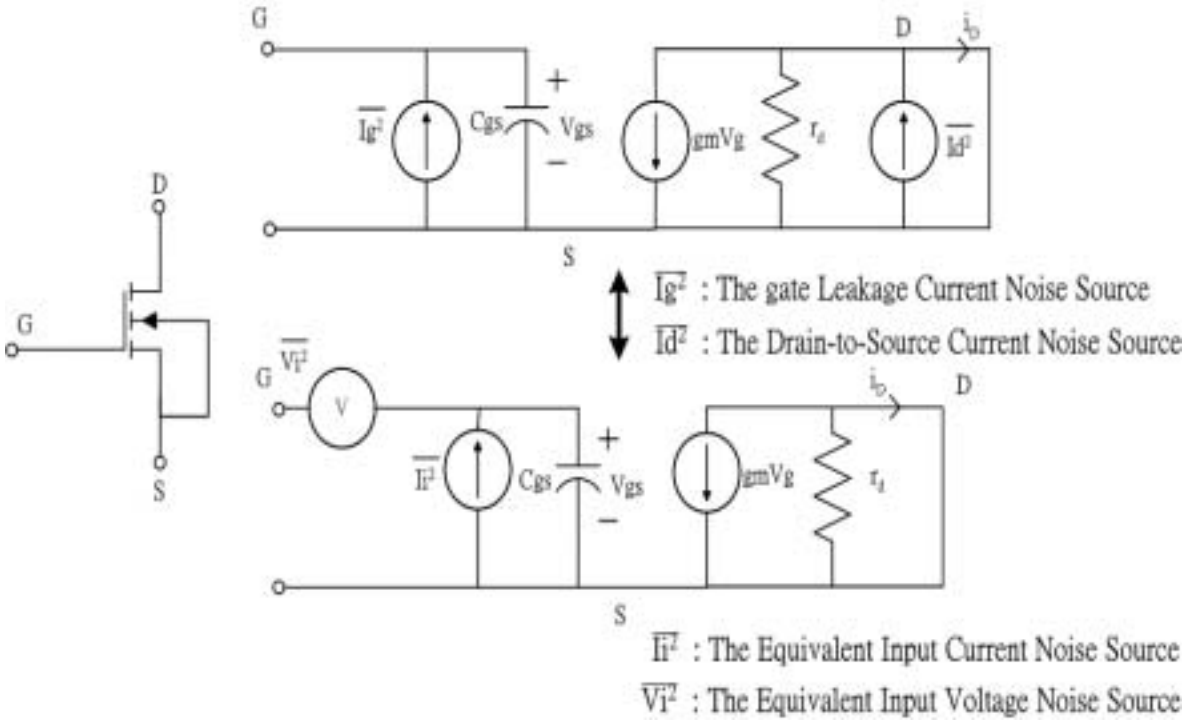

Fig.3.7 The MOS noise model

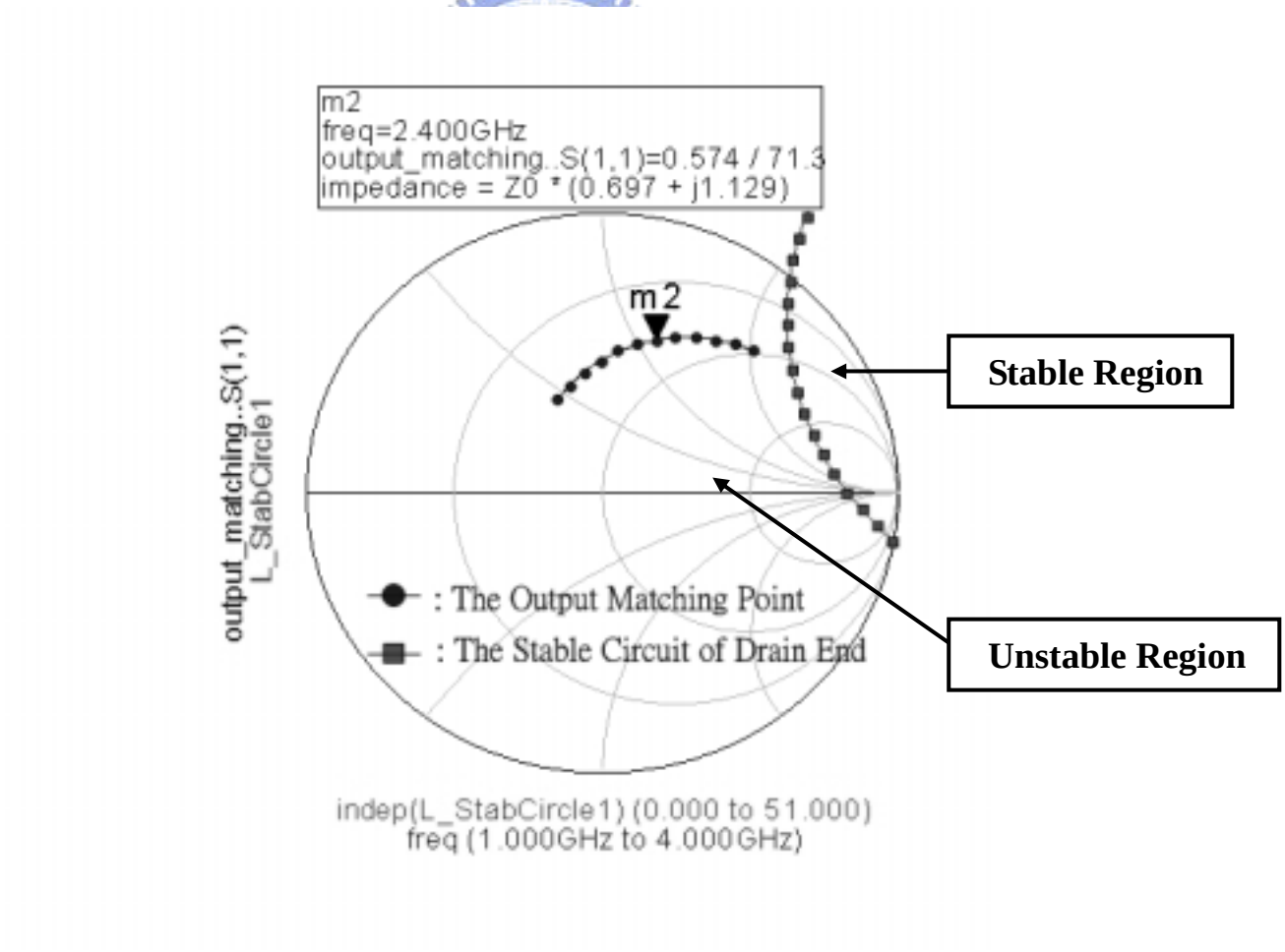

Fig.3.8 The stable circle of the drain end

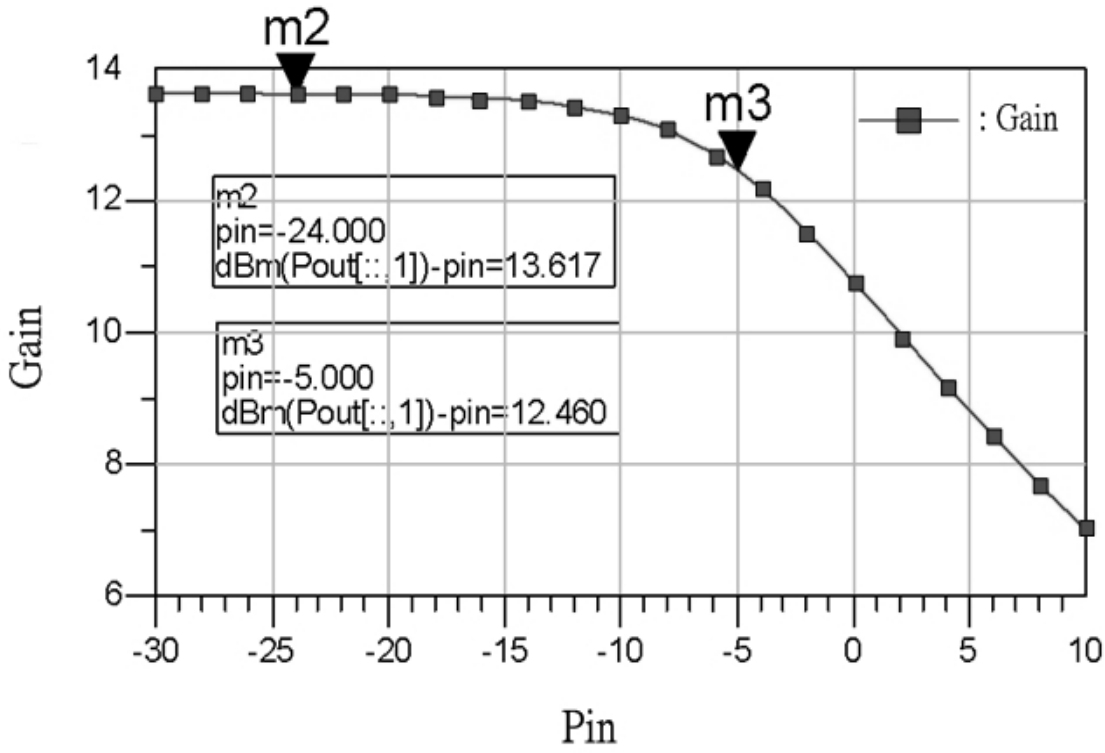

Fig.3.9 The gain of this reflection-type amplifier

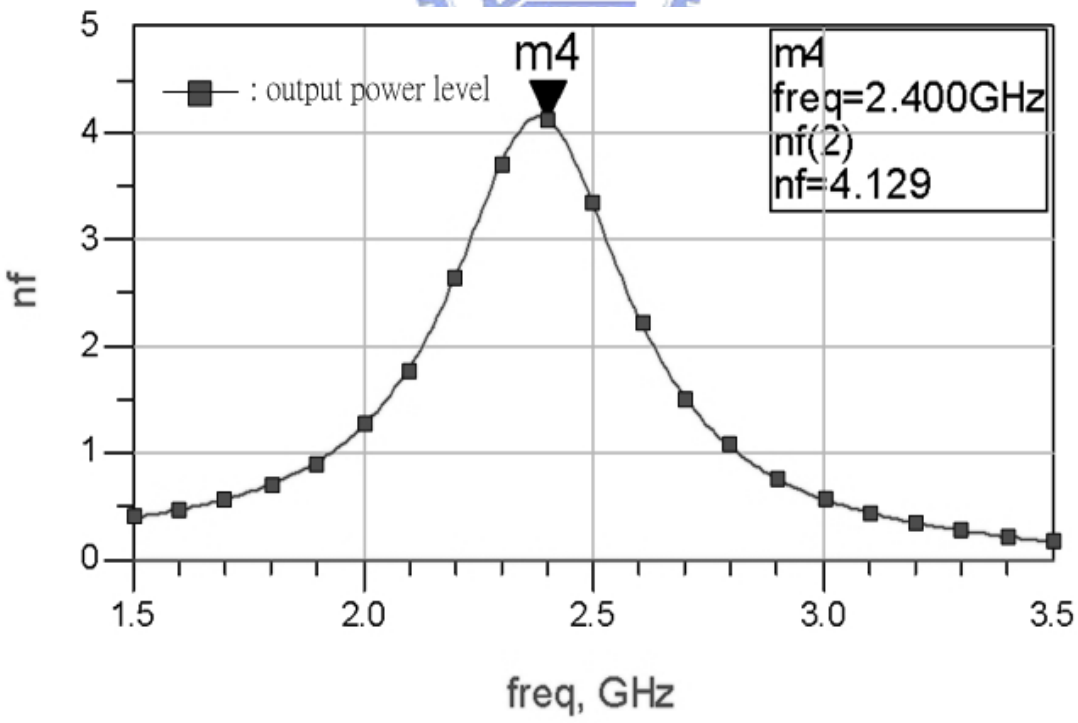

Fig.3.10 The noise figure of this reflection-type amplifier

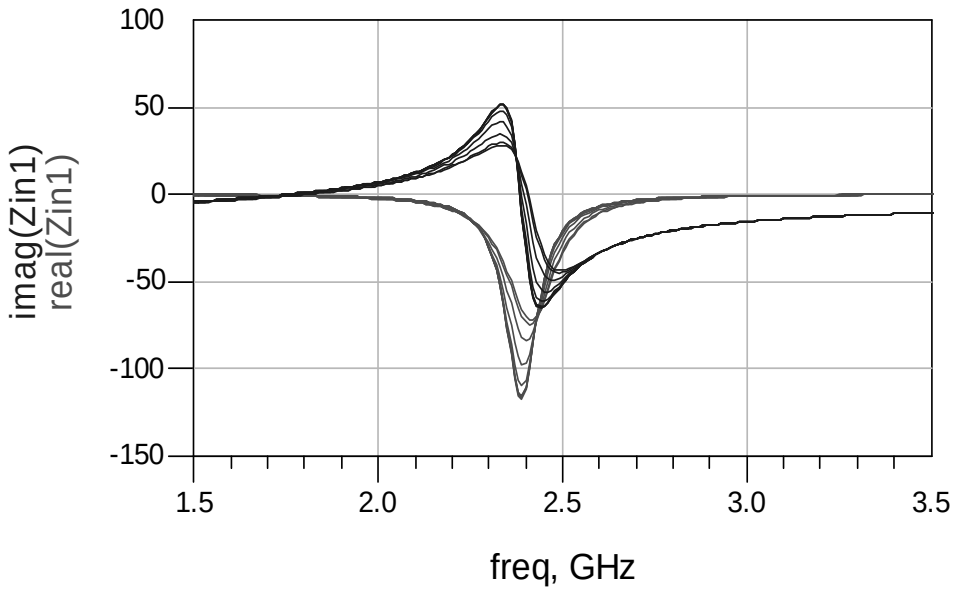

Fig.3.11 The input impedance changes as the value of the varied capacitance

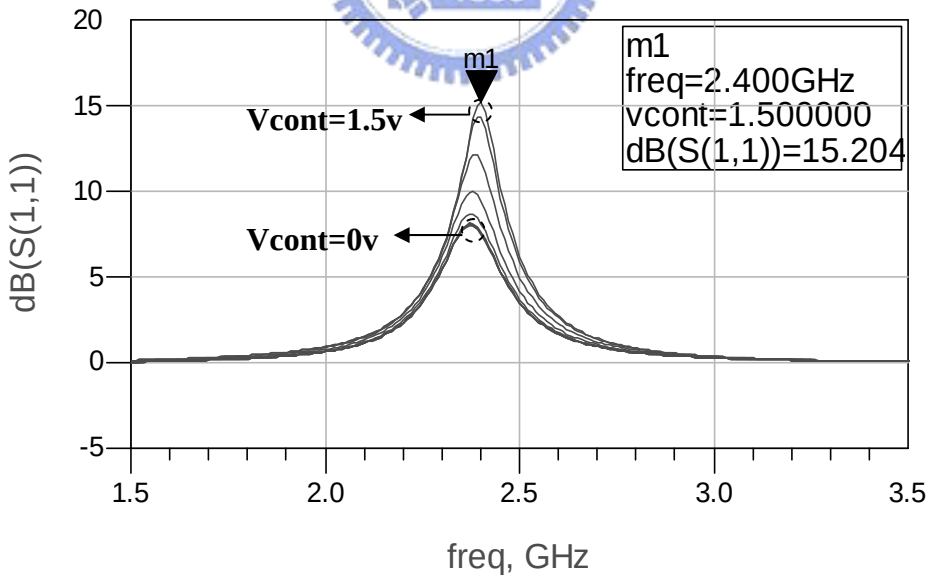

Fig.3.12 The gain of this reflection-type amplifier changes with the value of the varied capacitance

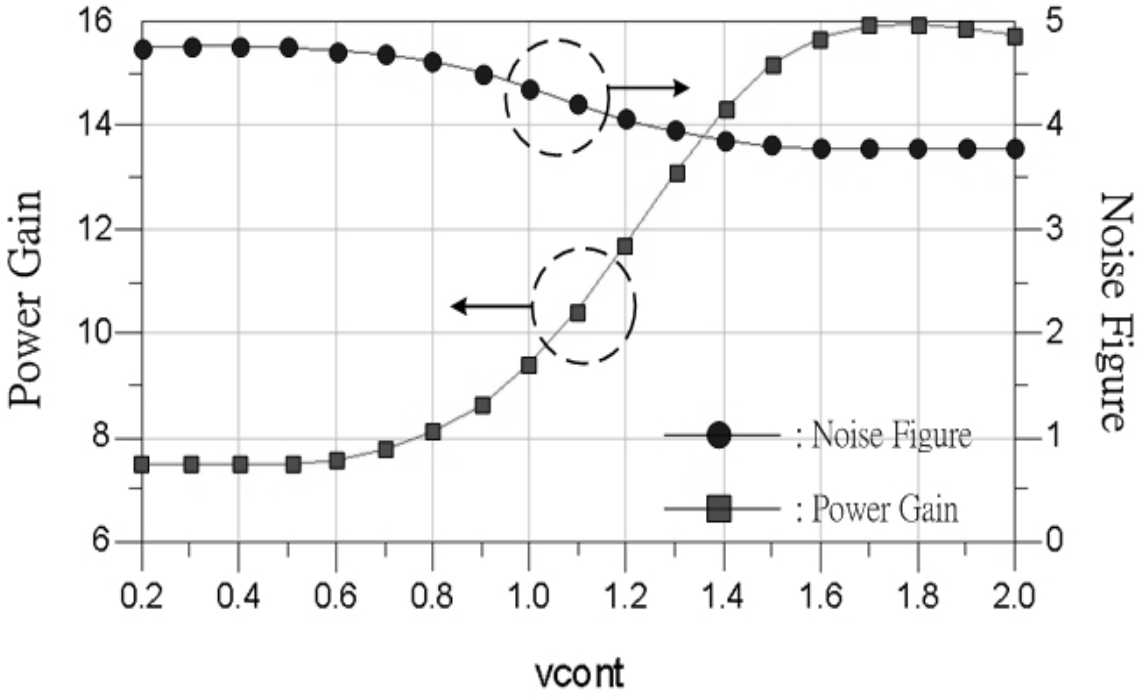

Fig.3.13 The gain and noise figure of this reflection-type amplifier varies with the control voltage V_{cont}

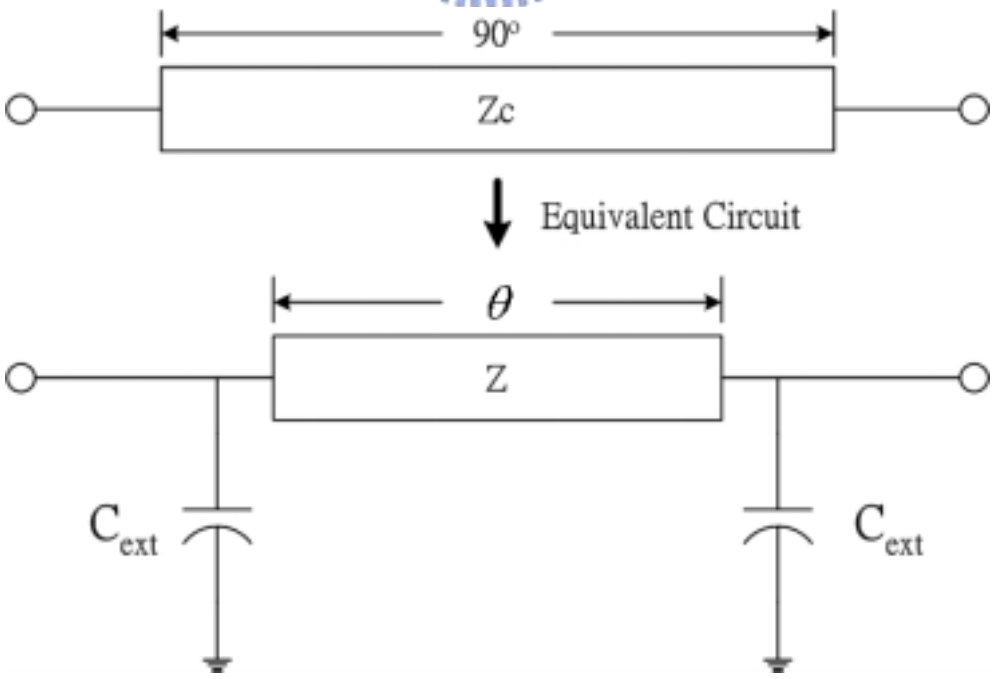

Fig.3.14 The transmission line's model of impedance transformation

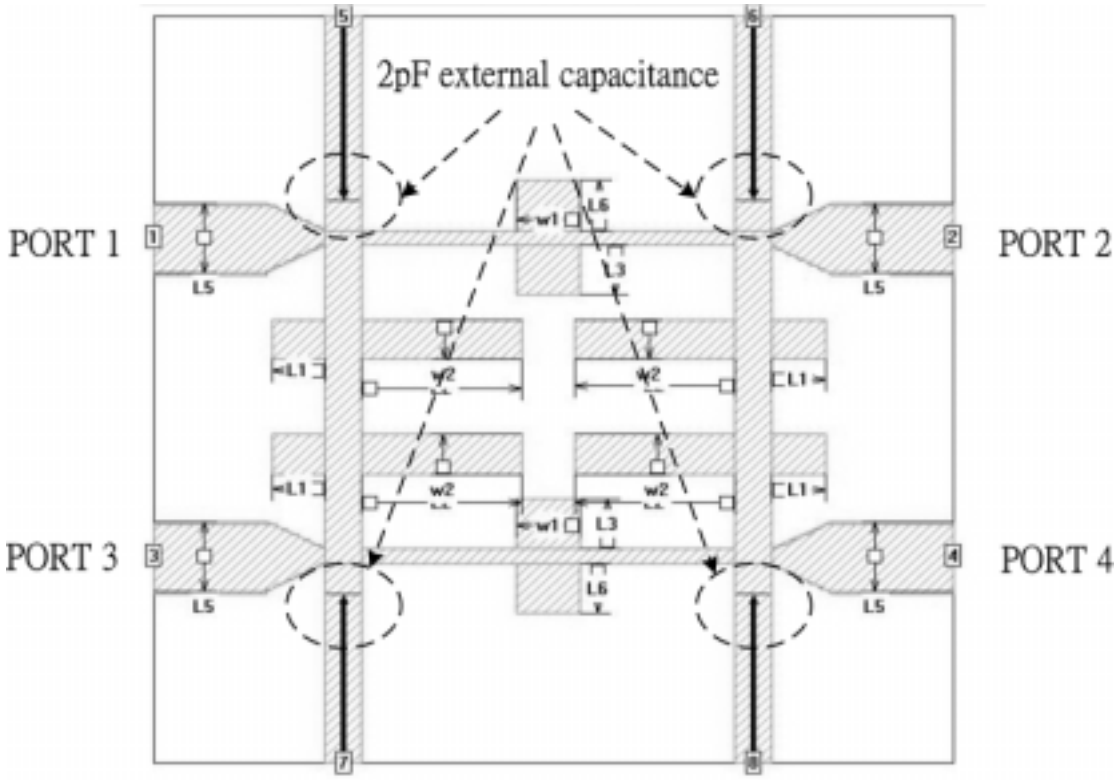

Fig.3.15 The architecture of this hybrid

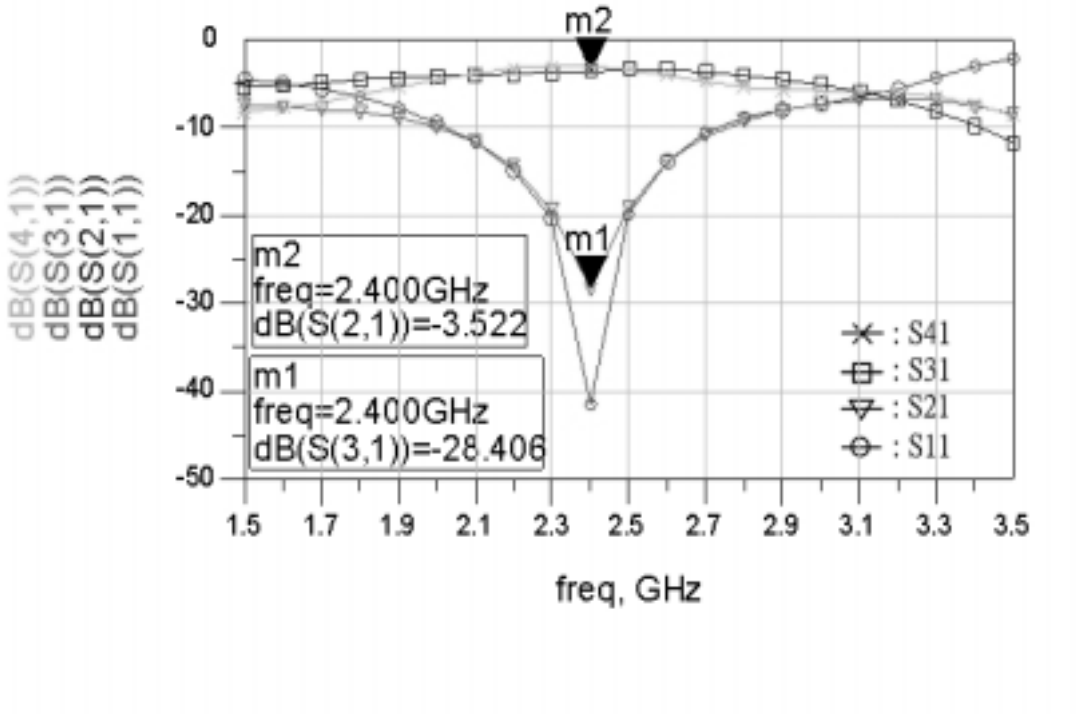

Fig.3.16 (a) The S parameters of this Branch-Line circuit

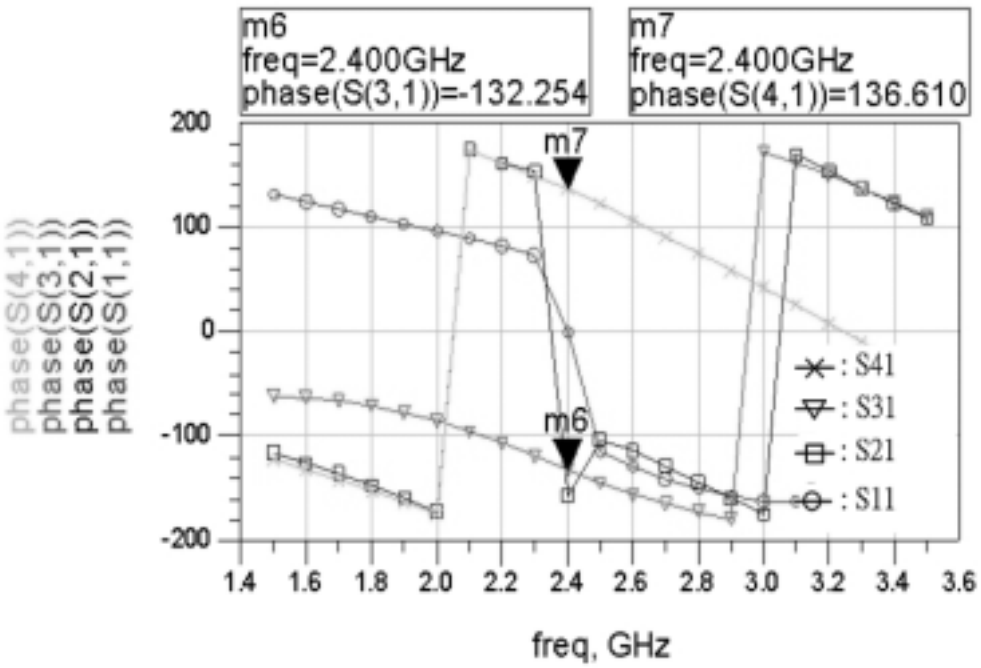

Fig.3.16 (b) The phase of this Branch-Line circuit

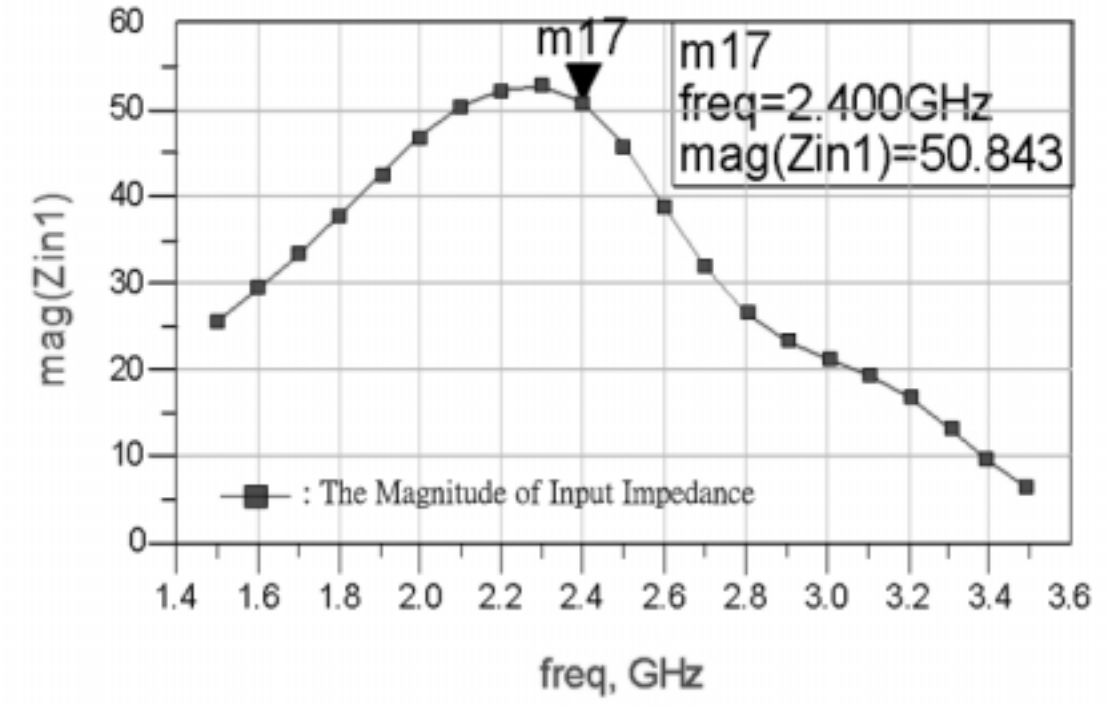

Fig.3.16 (c) The input impedance of this Branch-Line circuit

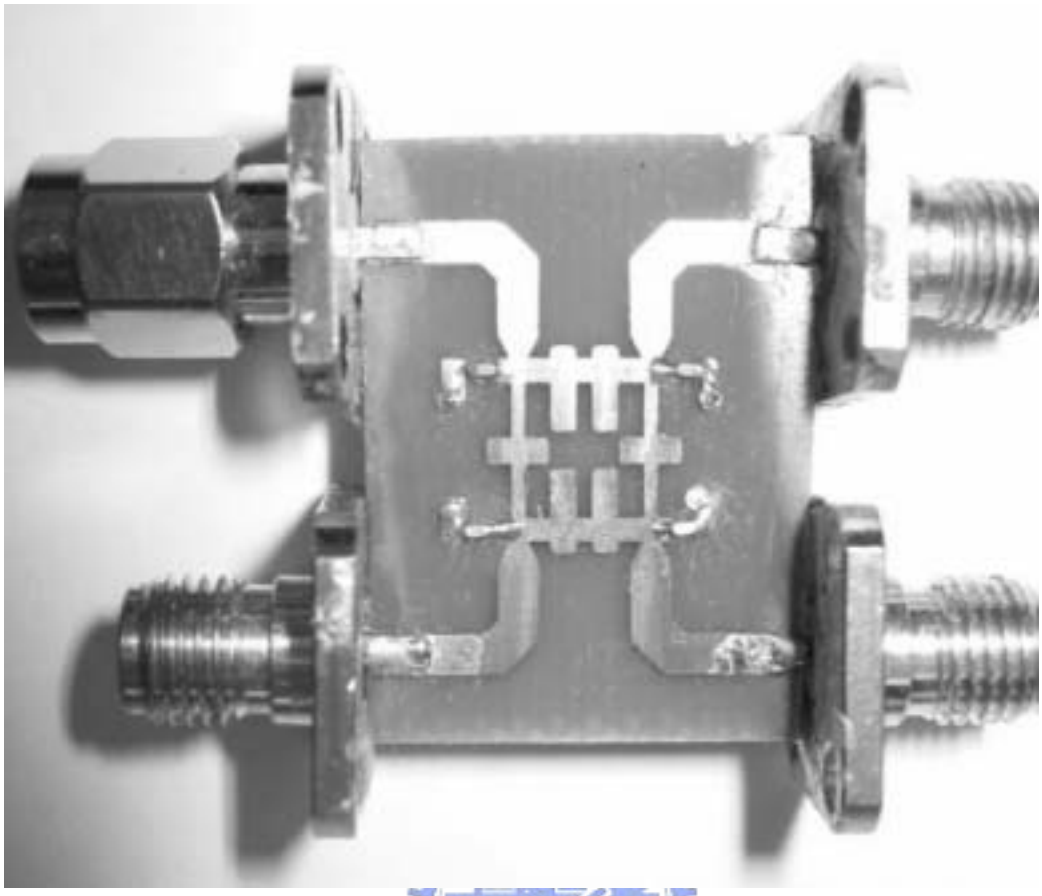

Fig.3.17 Photograph of the fabricated branch-line circuit

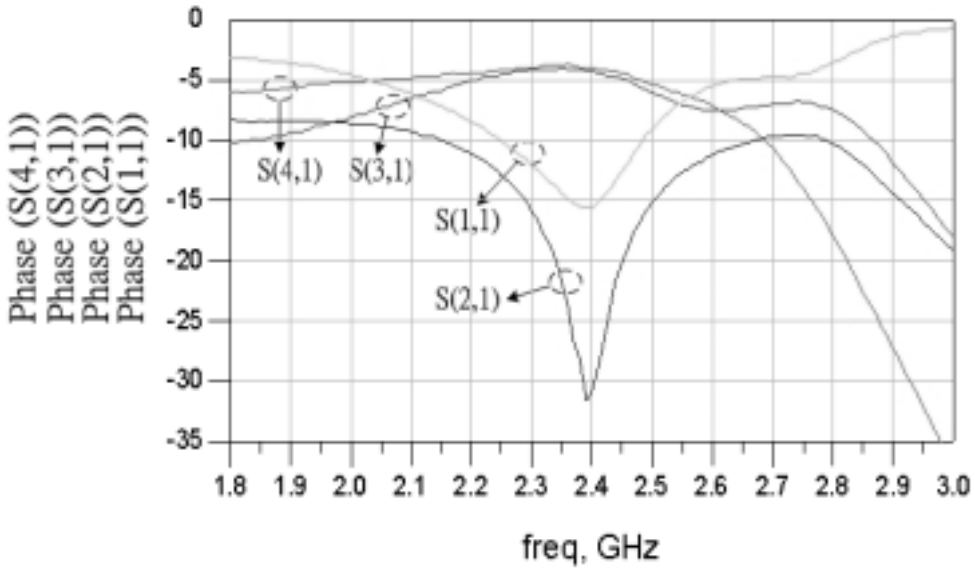

Fig.3.18 (a) The experimental S-parameter of Branch-Line circuit

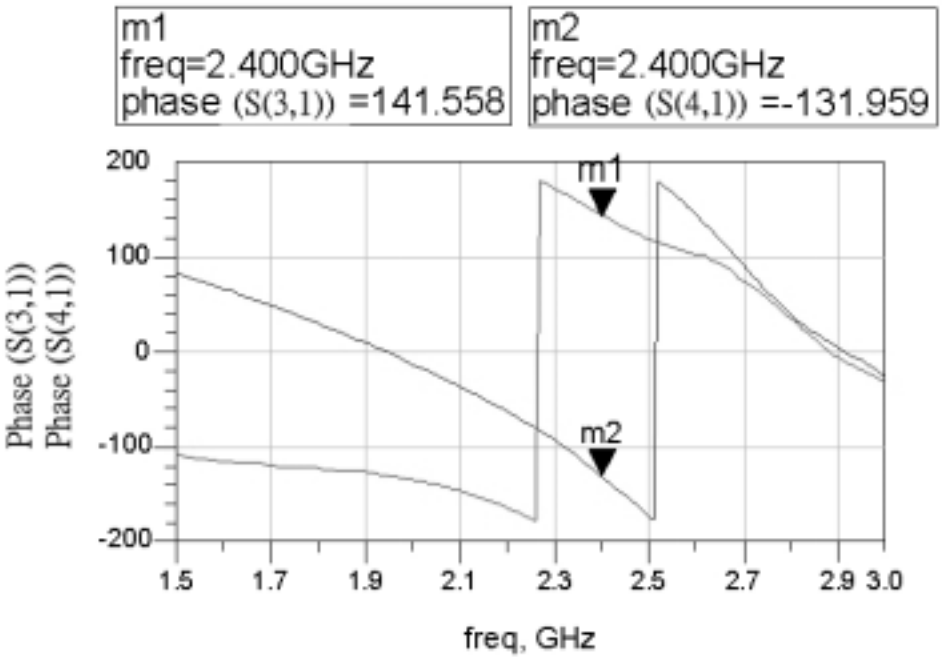

Fig.3.18 (b) The experimental phase response of this Branch-Line circuit

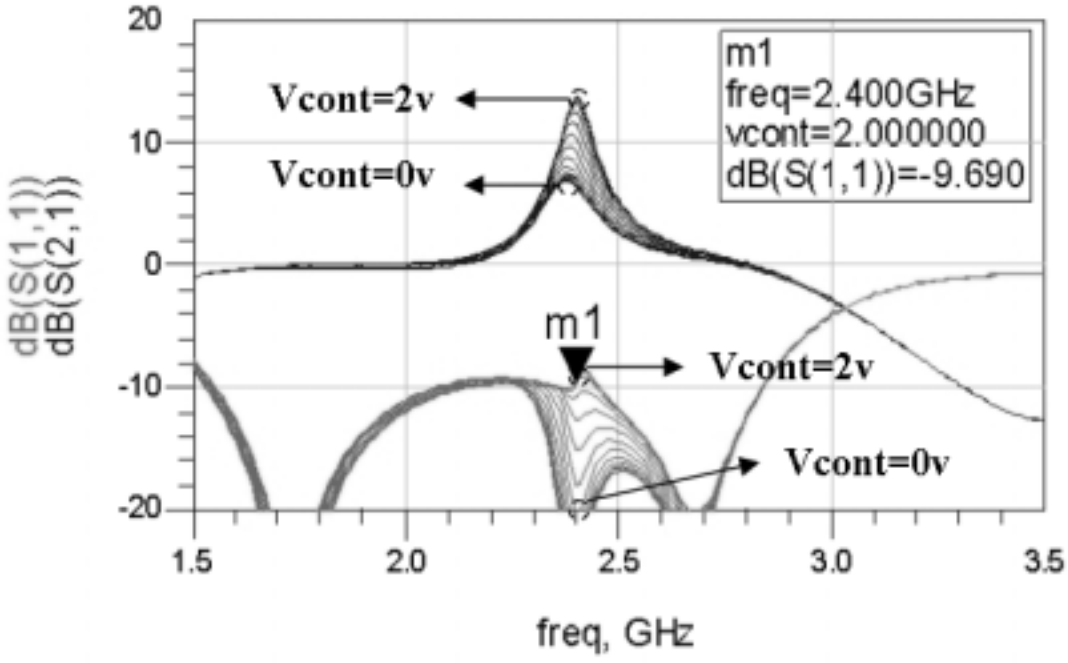

Fig.3.19 The gain and return loss of this bi-directional amplifier vary with the control voltage

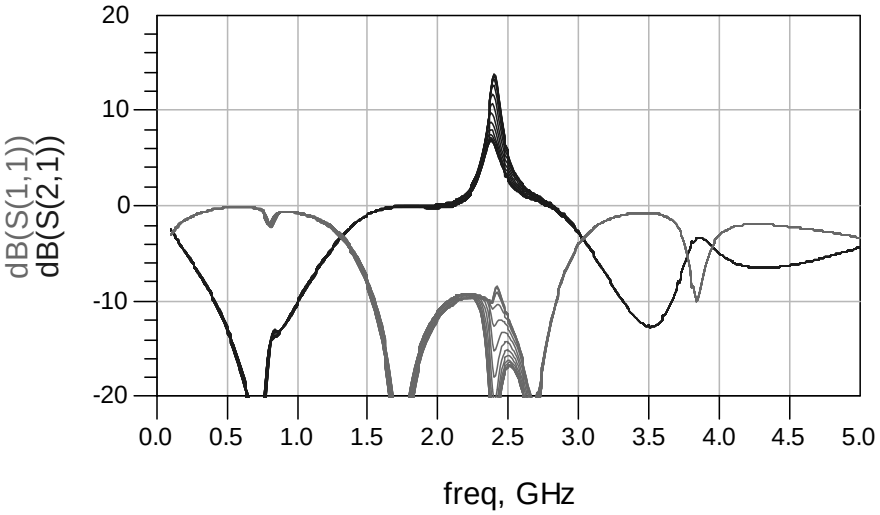

Fig.3.20 The spectrum across DC to 5 GHz

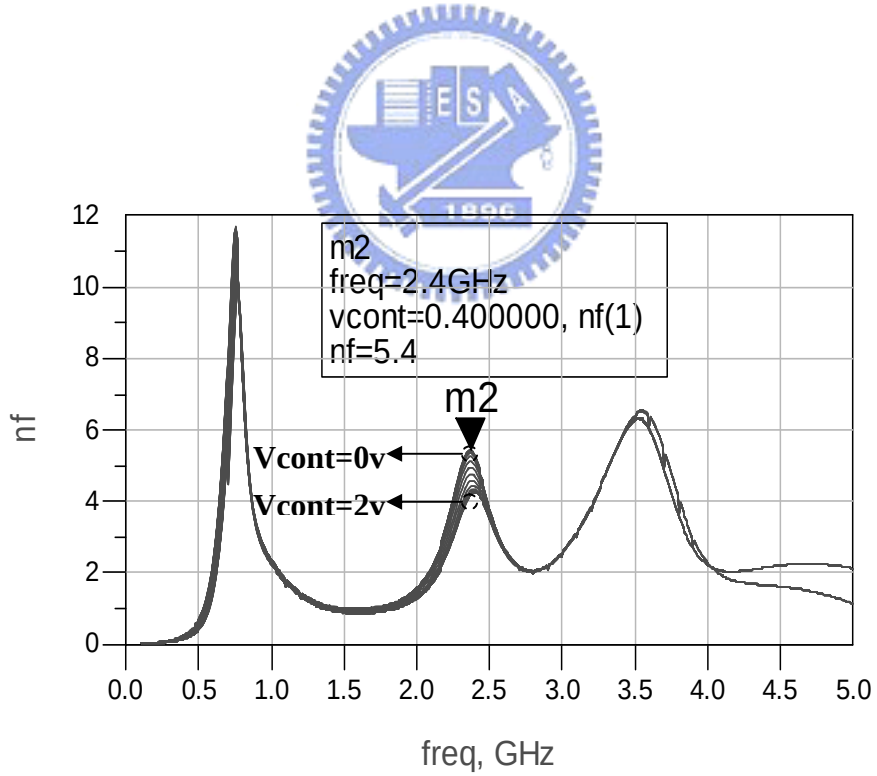

Fig.3.21 The noise figure of this amplifier varies with the controlled voltage

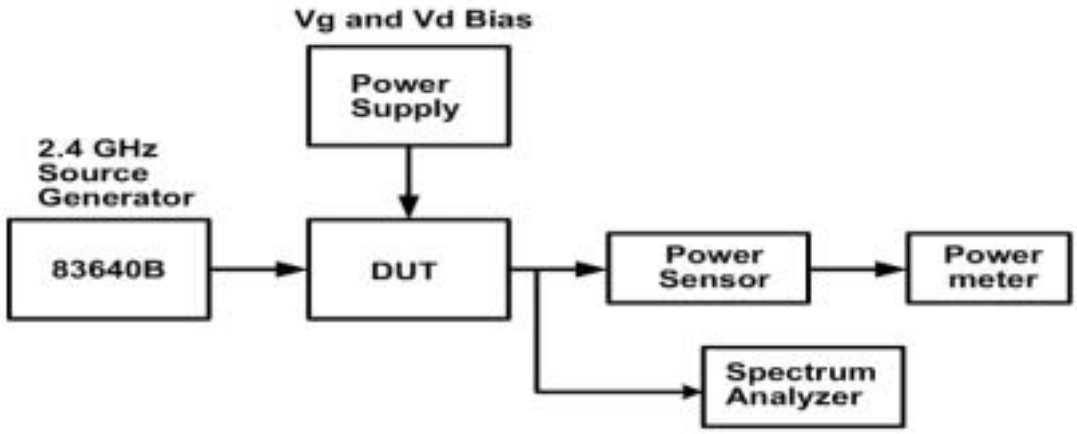

Fig.3.22 The diagram of testing procedure

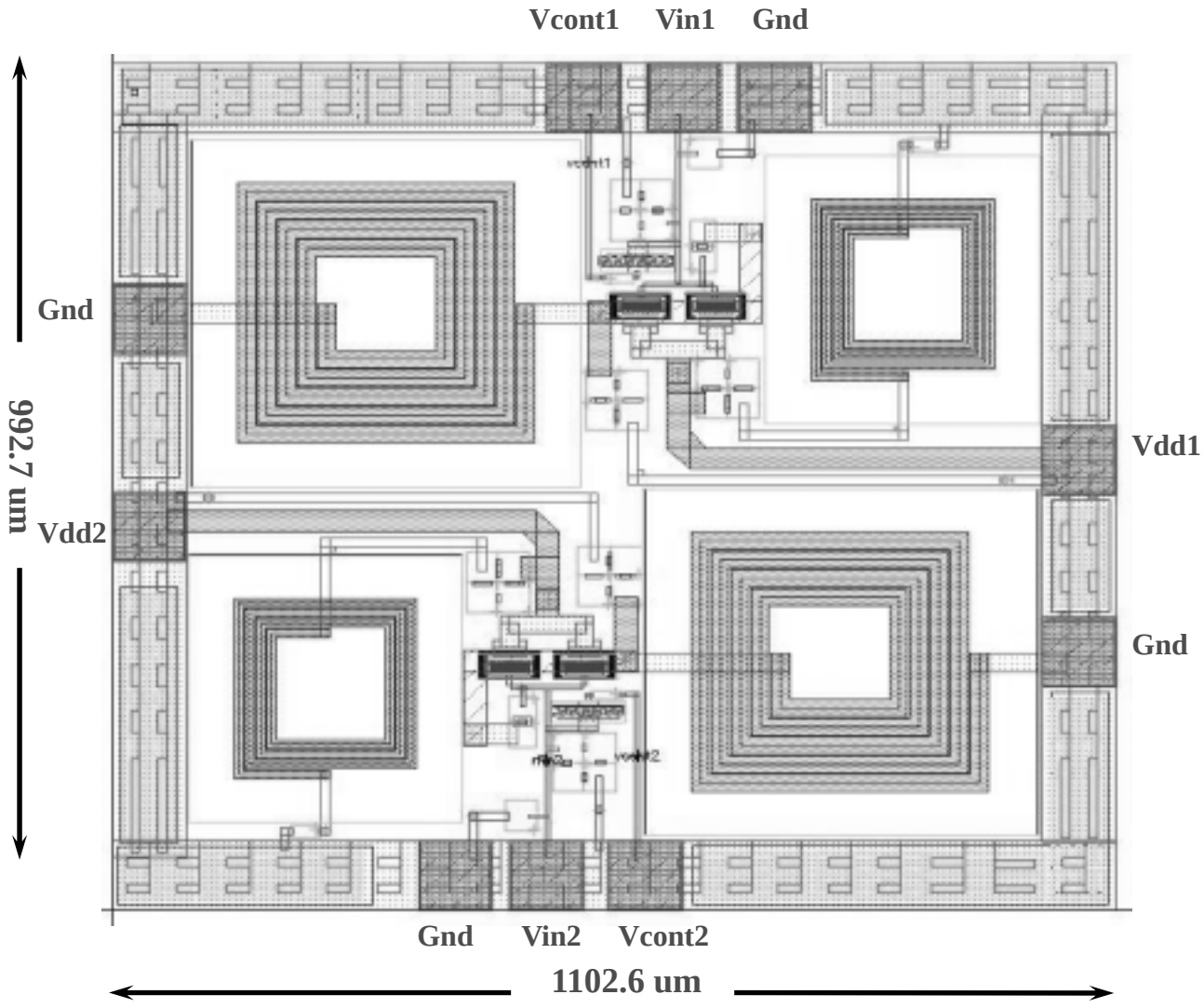

Fig.3.23 The layout of the two reflection-type amplifier

	TT	FF	SS	F/S
Gain(dB)	13.6	13.9	12.5	13.6
P-1dB(dBm)	-5.6	-4.4	-4.8	-5.6
NF	4.1	4.0	4.1	4.0

Table3.1 The parameters of this reflection-type amplifier vary in all kinds of the TSMC process

Design characteristic	Freq-Range (GHz)	Gain S21 (dB)	Return Loss S11 (dB)
accomplish amplifiers by SPDT switches **[21]**	2 ~ 18	0 ~ 4.5	12 ~ 30
	6 ~ 18	0 ~ 12	12 ~ 30
Common-gate type by Modifying bias **[20]**	42	6	10
	40	10	8
Novel bi-directional amplifier **[18]**	6	9	6
This work	**2.4**	**7.5 ~ 16**	**9.7 ~ 24**

Table3.2 The specifications of this bi-directional amplifier compare with these of others

specification	whole result	result(1)	result(2)
Id(mA)	21		
Centra1 frequency (GHz)	2.4		
P-1dB(dBm)	-5~3	3	-5
Gain S21(dB)	7.5~16	7.5	16
Return Loss S11(dB)	9.7~24	24	9.7
Noise figure	4.1~5.4	5.4	4.1
Bandwidth(MHz)	150~220	220	150
Control voltage (V)	**0~2 V**	**0 V**	**2 V**
Power dissipation(mA)	52*2		
Chip size(um^2)	1102.6 x 992.7		

Table3.3 The expected specifications of the bi-directional amplifier

CHAPTER 4

CONCLUSIONS

In the first section of this thesis, A Ka-Band Power Amplifier for Automotive Radar System is analyzed and designed. This circuit utilizes the semiconductor process of 0.15um GaInAs pHEMT power device to accomplish. In order to acquire the adequate linearity and efficiency of the system requirements, the architecture with two stages is adopted to design the power amplifier. The first stage utilizes class-A type to supply sufficient power gain. The second stage improves RF-to-DC signal ratio by class-AB type. Firstly, the biasing points of the two stages are selected in order to acquire the desired characteristics. Utilizing the software of load pull measurement, the output matching circuit could be determined by making trade-off between the output power level and the power-added-efficiency. Referred to the output optimal point of the drive stage and the input optimal point of the power stage, the best interface matching point is chosen to balance the mismatch. The input matching circuit is realized easily by conjugate match because it is assumed to influence the output power level slightly. The simulated result of output power is 19.4dBm and the PAE is 27.4% at the 1dB compression point. The maximum output power level is 20.5dBm at Pin=10dBm. The maximum value of PAE is 35.9% at the maximum output power point. The IIP3 point is about 20dBm and the OIP3 is 40dBm nearly. Nevertheless, the experimental outcome of maximum small-signal gain is 13.4dB at the central frequency of 32.4GHz. The maximum power-driving ability is 15dBm at Pin=12dBm. And the largest PAE value is 23%. This consequence is not similar completely with the simulated performances. The central frequency shifts from 38GHz to 32.4GHz. And the power-driving ability and gain

degrade compared with the original results. Discussed the reasons, the S-parameter of the WIN 0.15um power device at designed frequency and biasing voltage must be confirmed by test-key devices. And the parasitic capacitances of the RF pads have to deliberate whether it's appropriate for the designed circuit or not. They are critical parameters to influence the performance crucially. The prospect of this categorical MMIC design is to extract carefully the transistors' models. And any possible parasitic components are taken into account in order to obtain the efficient simulations. Therefore, the simulated sequence will relatively approach the experimental results.

The second part of this thesis describes a novel 2.4GHz bi-directional amplifier with gain control. This architecture includes two reflection-type amplifiers and a 90 degree branch-line hybrid. This approach can improve effectively the isolation and noise figure of the circuit to ameliorate the quality of output signal. This 90 degree branch-line circuit is realized on a FR4 board for these reasons and utilizes a new method to reduce the area to 7 square millimeters. So, this IC only includes these two imperative reflection-type amplifiers. The overall architecture of the reflection-type amplifier embraces a variable capacitance C_{cont} to control the gain and eliminate the influence of bonding wires, a parallel circuit of C_s and L_s to control the central frequency, the loaded impedance R_{load} and L_{load} in the drain end and a capacitance Cgs' to modify the real part of the input impedance. The noise figure of this amplifier is between 4dB and 5dB approximately and the gain varies between 7.5dB and 16dB as the controlled voltage ranges from 2v to 0v. The specifications of this bi-directional amplifier are the same as them of the reflection-type amplifier described above. The future work must watch out the balance of the two reflection-type amplifiers and prevent the oscillation resulting from mismatch of the connection between the reflection-type amplifiers and the branch-line couple circuit.

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