Chapter 1

Introduction

1.1 General background and motivations

Si material has been developed in semiconductor industry for over 30 years. Although other semiconductor materials may have better characteristics included higher mobility, larger band gap or higher saturation velocity, but silicon devices still account for over 96 % of all microelectronic applications. The reason why silicon so popular is that Si is the most of elements about 26% in addition to oxygen on the surface of earth and the manufacturing technology for Si material is also mature and Si substrate has potential for wafer-size expansion. So Si substrate would significantly reduce manufacturing costs compared to InP or GaAs substrates. Moreover, high thermal conductivity and mechanical hardness are also advantages of Si material.

According to Moore's law, the number of transistor on a chip approximately doubles every two years. But when the device is scaling down below 100 nm, the performance of Si device is reaching its limitation. In the same time, the outstanding features of III-V material have attracted a lot of attention. In Table 1-1, III-V materials have significantly higher electron mobility than Si and can potentially play a major role along with Si in future high speed and low power consumptions devices. In order to reduce manufacturing costs and realize the ultimate vision of high switching activity factor low-voltage and high-speed III/V based logic circuit blocks coupled with the functional density advantages provided by the Si CMOS platform. A heterogeneous integration of III/V compound materials with Si platform is necessary. But III-V materials (ex:

GaAs) epitaxy on Si substrate has many problems need to be solved including lattice mismatch, thermal expansion coefficient difference and anti-phase boundary. So many epitaxial methods are utilized to solve these problems. One of them is GaAs/Ge/Si buffer layer. The reason of using Ge as buffer layer is that the lattice constants and thermal expansion between Ge and GaAs are almost the same, as shown in Figure 1-1. So that Ge layer grown on Si substrate also can be utilized as virtual substrate for the growth of high electron mobility structure and for the integration of the III-V devices on Si substrate.

1.2 The methods of Ge grown on Si

The major problems of growing Ge layer on Si substrate are the high threading dislocation density and high surface roughness arising from the 4.2% lattice mismatch between Ge and Si. There are many growth methods and techniques to solve these problems. It has been reported that the compositionally graded buffer (CGB) layers [1], low temperature Si buffer layers [2], compliant silicon-on-insulator (SOI) substrate [3], and selective area growth combined with thermal cycle annealing [4] can be used to grow high quality and strain relaxed Ge layers on Si substrate. Among these methods, the CGB layer is widely used today. However, the method still has two major issues needed to be solved. The first, the thickness of these CGB layers is approximately 10 µm for the variation of Ge composition of SiGe buffer layer from 0 to 1.0, which increases the manufacture cost of the template substrate crucially. The second, the CGB layers often exhibit a cross hatch pattern, which would increase the roughness of Ge surface and hinder their integration with conventional Si based circuits.

In this study, the method of two-step Si_xGe_{1-x} buffer layers would be

discussed in detail. The method discussed here can not only obtain the high quality of Ge layer but also reduce the thickness of buffer layers effectively.

1.3 Outline of the thesis

The thesis of the high quality Ge epitaxial film grown on Si substrate by two-step Si_xGe_{1-x} buffer layers is discussed here. In chapter 2, the principles and characteristics of Ge and SiGe layer grown on Si substrate and the mechanism of the two-step Si_xGe_{1-x} buffer layers structure are introduced detailly. Chapter 3 is the experiment flow of the SiGe and Ge epitaxial growth by UHV/CVD, and analytic instruments are briefly presented here. The experiment results and discussion is presented in chapter 4. Finally, in chapter 5, it is the conclusion.

	Si	GaAs	$In_{0.53}Ga_{0.47}As$	InAs
Energy gap(eV)	1.12	1.42	0.72	0.36
Electron Mobility, μ_n $(cm^2/V\text{-}s)$	1350	8500	12000	40000

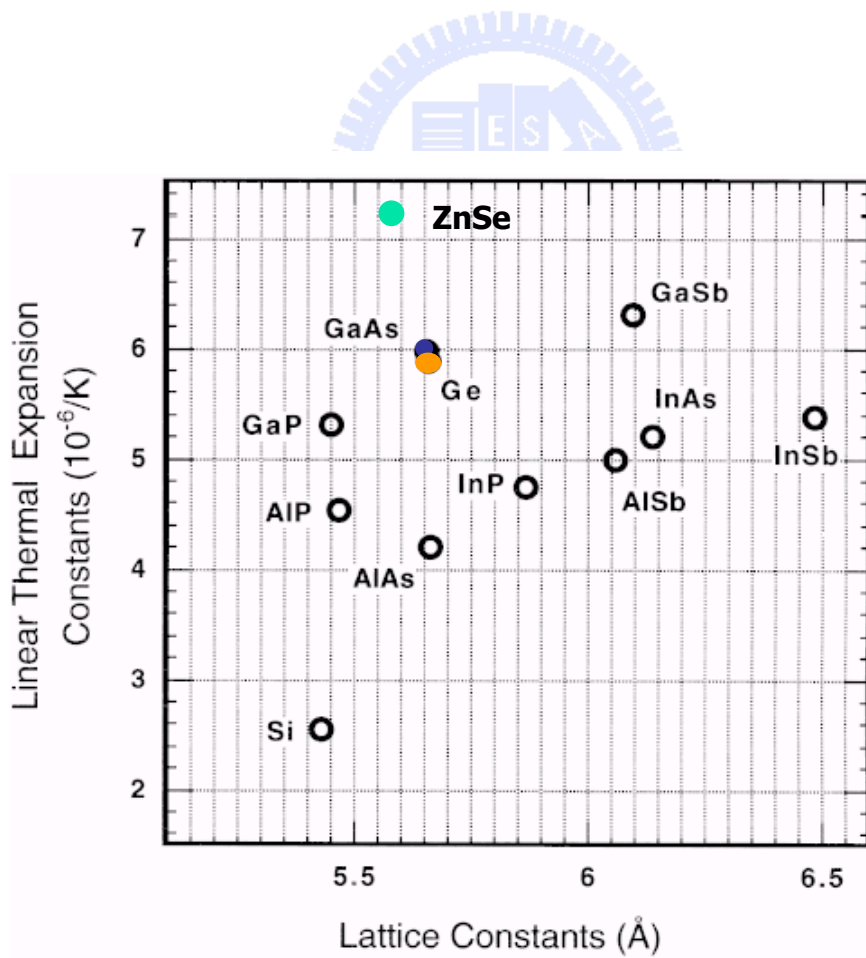Table 1-1: Energy band gap and carrier mobility of Si and III-V materials

Figure 1-1: Lattice constants and linear thermal expansion of materials

Chapter 2

Literature Review

2-1 Principle of SiGe/Ge epitaxy on Si substrate

There are many epitaxial methods today, but the most widely used one in industry is the chemical vapor deposition (CVD) techniques. These techniques use the chemical reactions between different source gases to deposit desired material on a substrate. The deposition of one material on top of the same material is called homoepitaxy, on the other way, the deposition onto different material is called heteroepitaxy. The growth of Ge film on Si substrate is heteroepitaxial growth and would be discussed here. The key issue of Ge heteroepitaxy grown on Si is large lattice mismatch (4.2%), so high dislocation density and undulation surface are two major problems needed to be solved during the growth of Ge epitaxial layer. In the thesis, the structure of two-step $Si_{1-x}Ge_x$ layers will be introduced as buffer layers to solve the problem. Before introducing the mechanism of the two step $Si_{1-x}Ge_x$ buffer layer, some principles or problems of SiGe/Ge epitaxy on Si substrate will be discussed.

2-2 Material characteristics of Si and Ge

Si and Ge are crystallized in the form of diamond lattice structure. This structure belongs to the cubic-crystal family and can be seen as two interpenetrating FCC sublattices with one sublattice displaced from the other by one quarter of the distance along the diagonal of the cube as shown in Figure 2-1. All atoms are identical in a diamond lattice, and each atom is surrounded by four equidistant nearest neighbors that lie on the corners of a tetrahedron structure. In Table2-1, selected physical properties about the Si and Ge are shown. The

outstanding performance of Ge in many applications comes from its advantageous properties, such as its high carrier mobility (1900 cm^2/Vs and 3600 cm^2/Vs for holes and electrons, respectively). The value of hole mobility of 3600 cm^2/Vs is one of the highest value of all the commonly used semiconductors. Ge has exceptional characteristics for high frequency operation and permits the design of faster devices compared to Si. Its low band gap (0.66 eV) allows the operation at lower voltage, even if the thermal noise must be correctly handled and minimized.

2-2-1 Lattice mismatch

In general, the epitaxial process may involve in different materials, it is necessary to define the lattice mismatch, d, between the substrate with lattice parameter A_{sub} and the film with lattice parameter a_{epi} as

$$d = \frac{A_{sub} - a_{epi}}{A_{sub}} \qquad (2-1)$$

From Table 2-1, the lattice constant of Ge and Si is 5.65 $\overset{\circ}{A}$ and 5.43 $\overset{\circ}{A}$. According to equation 2-1, there is a 4.2 % lattice mismatch between Ge epitaxial film and Si substrate. The lattice constant of relaxed or bulk Si_{1-x} Ge_x films ($0 \leq x \leq 1$) is almost linear as predicted by Vergard's Law although small variations to this have been measured [5].

$$a_{Si_xGe_{1-x}} = 0.5431 + 0.01992x^2 + 0.0002733x^3 \quad (nm) \qquad (2-2)$$

The epitaxial layer shows compressive strain either for Ge epitaxial film grown on Si or a thin Si_xGe_{1-x} film grown on another Si_yGe_{1-y} film (in which x < y) as shown in Figure 2-2(b). The strain of x and y axis present in the plane of the layer ($\varepsilon_x = \varepsilon_y = \varepsilon_{\parallel}$) and produces a perpendicular strain, $\varepsilon_{\perp}$, resulting in a

tetragonal distortion to the lattice as shown in Figure 2-2(b). In isotropic elasticity theory the strains are related by Poisson ratio, ν through

$$\varepsilon_\perp = \frac{-2\nu}{1-\nu}\varepsilon_\parallel \qquad (2-3)$$

If the unstrained lattice parameters of the two layers are defined as a_A and a_B respectively with the thicknesses h_A and h_B and assuming $a_A < a_B$ as shown in Figure 2-2(a), the tetragonal distortion produces a parallel lattice constant [6], $a_\parallel$, as shown in Figure 2-2(b)

$$a_\parallel = a_A\left[1 + \frac{d}{\left(1 + \frac{G_A h_A}{G_b h_B}\right)}\right] \qquad (2-4)$$

where G_i are the shear moduli of each layer and h_i are the thickness. The in-plane strain in layer A is given by the term $\frac{d}{\left(1 + \frac{G_A h_A}{G_b h_B}\right)}$ and in equilibrium the in-plane strain of layer A, $\varepsilon_\parallel{}^A$, is related to the strain layer B, $\varepsilon_\parallel{}^B$, through

$$\varepsilon_\parallel{}^A = -\left(\frac{G_B h_B}{G_A h_a}\right)\varepsilon_\parallel{}^B \qquad (2-5)$$

If the two layers are free and in equilibrium, the equation 2-5 implies that the average strain of the two layers is zero.

2-2-2 Critical thickness and dislocations

A coherent or pseudomorphic hetero-interface will be formed where the strained layer is forced to have the substrates extra in-plane lattice constant and again the epitaxial layer becomes tetragonally distorted. As the thickness of the epitaxial layer is increased, there exists a maximum thickness, called the critical thickness, h_c, above which it accumulates too much energy to elastically strain additional heterolayers into coherence with the substrate. In this case, the misfit dislocations appear to relieve the strain in the epitaxial film as shown in Figure

2-3. For every misfit dislocation there will always be two threading dislocations at the ends of the misfit which must thread to a surface or form a loop as shown in Figure 2-4. The threading dislocations are a/2 <110> 60°type for the SiGe system.

A number of models have been developed to predict the critical thickness of the strained epitaxial layer. Van der Merwe [7] produced a thermodynamic equilibrium model by minimising the total energy of a system with the generation of a periodic array of dislocations. This produced a critical thickness defined as

$$h_c \cong \frac{19}{16\pi^2}\left(\frac{1+\nu}{1-\nu}\right)\left(\frac{b}{d}\right) \qquad (2-6)$$

where b is the slip distance which is called Burger's vector. For a bulk Si substrate, b is 0.4 nm and more generally present like $a_A /\sqrt{2}$ where a_A is the lattice constant of the relaxed substrate.

Matthews and Blakeslee used an equivalent approach of balancing the forces for a propagating and threading dislocation [8]. By balancing the force of the threading dislocation arm in an uncapped epilayer with the restoring line tension force from the self energy of the extra interfacial dislocation created during relaxation and solving produces a critical thickness of

$$h_c \cong \frac{b}{2\pi d}\frac{(1-\nu \cos^2\theta)}{(1+\nu)\cos\lambda}\left[\ln\left(\frac{h_c}{b}+1\right)\right] \qquad (2-7)$$

where θ is the angle between the dislocation line and λ is the angle between the Burgers vector and the direction of the interface normal to the dislocation line. In the case of the misfit between pure Si and Ge, d= 0.0418, cos λ = cos θ = 0.5 for 60° mixed a/2 <110> dislocations, equation 2-7 reduces to

$$h_c \cong \frac{0.55}{x}\ln(10h_c) \qquad (h_c \cong 1.7793x^{-1.2371} \quad nm) \qquad (2-8)$$

This critical thickness is plotted in Figure 2-5 and corresponds to the boundary between the stable and metastable regions. A stable situation requires the Gibb's free energy of a system to be at a minimum value. As the thickness of an epilayer increases, it is going further away from a stable state. Such a system will sooner or later find a way to decrease its Gibb's free energy, which will happen either by the formation of misfit dislocations or by roughening the surface. The layer thickness at which it is no longer thermodynamically favorable to have a pseudomorphic layer is called the critical thickness and the critical thickness is defined as an upper limit for stable epitaxial layers in heteroepitaxy. A metastable region is the relaxation of an epitaxial layer including the rearrangement of atoms. Either dislocation will form, meaning that many atoms will shift their position to the lattice. These processes require the broken bonds between atoms and the movement of the atoms. Certain activation energy, E_A, must be available to make this possible. Without the energy, the relaxation cannot take place even though it would lead to a more energetically favorable situation for the system.

2-2-3 Thermal expansion mismatch

When a cubic semiconductor lattice is heated, it expands triaxially according to its thermal expansion coefficient $\alpha(T)$. In general, this thermal expansion coefficient is a function of temperature, but for small ΔT, it can be assumed to be a constant. The thermal expansion coefficient of bulk Ge and Si have shown in Table 2-1. When a thin heteroepitaxial film is deposited on a semiconductor substrate with a different thermal expansion coefficient, the thick substrate will dominate the thermal expansion behavior of the thin coherent film above it. As the deposited film is cooled from its growth temperature, it will

therefore incorporate an addition biaxial strain due to the different thermal expansion coefficients. Assuming no additional sources of plastic relaxation during cooling down, the total developed strain in such a system due to this thermal expansion mismatch, ε, could be estimated as

$$\varepsilon = \Delta\alpha\Delta T \qquad (2-9)$$

The growth of a thin Ge ($\alpha=5.5\times10^{-6}K^{-1}$) film on a Si ($\alpha=2.6\times10^{-6}K^{-1}$) substrate could be expected to introduce a tensile thermal expansion strain of approximately 0.18% assuming a Ge/Si growth temperature of 550 °C. The strain estimation is close to the calculated more rigorously by Roos and Ernst [9] using complete expressions for thermal expansion coefficients as a function of temperature, and useful for understanding the order of magnitude of the strain expected to be introduced by thermal expansion mismatch.

2-2-4 Growth mode and undulation surface

In the Figure 2-6, the classical picture distinguishes three different kinds of epitaxial film growth mechanisms [9] including Volmer- Weber (VW) mechanism (island growth), alone with Frank-van der Merwe (FM) mechanism (layer by layer growth) and the Stranski-Krastanov (SK) mechanism (an initially continuous film becomes islanded but with a thin continuous 'wetting' layer left). In the equation 2-10 and 2-11, the FM and VW mechanisms can be distinguished as being based on how the surface energies of the substrate (γ_s), the film (γ_f), and their interface (γ_i) interrelate with each other. If the substrate surface energy (γ_s) is large enough to exceed the sum of the two others, the wetting regime occurs and it is FM mechanism.

$$\gamma_s > \gamma_f + \gamma_i \qquad (2-10)$$

Whereas the reverse situation implies the lack of wetting layer, and it is defined as the VM mechanism.

$$\gamma_s < \gamma_f + \gamma_i \qquad (2-11)$$

SiGe alloys are miscible over all germanium contents for the growth temperatures used in epitaxy and the surface energy of SiGe is lower than that of Si. Therefore if the strain in a growth layer is small then two dimensional growth, the Frank-van der Merwe mode is produced in a similar function to Si homoepitaxy. This is the main growth regime required for all of the heterostructure devices.

Since Ge has a 4.2 % larger lattice constant than Si. In the equation 2-12, the stored energy in SiGe epitaxial layer will increase when the Ge content of SiGe layer, x, is increased. The ε and d represent the biaxial strain and the thickness of the SiGe layer.

$$\varepsilon^2 d = 0.0176 x^2 d \qquad (2-12)$$

When the excess strain energy equals the activation energy of island nucleation E_A, the islands will start to nucleate and grow to reduce the compressive strain energy as shown in Figure 2-7[11]. And then growth undulations and surface roughening can be developed. Stranski-Krastanov (SK) growth is where islands have formed after an initial two dimensional wetting layer driven by the heterolayer system trying to reduce the compressive strain energy.

2-3 Motivation

It has been reported that the strained isoelectronically In-doped GaAs layer grown on the GaAs wafer would reduce the dislocation density of In-doped GaAs layer drastically, and authors found that the stress formed between the In-doped GaAs layer and GaAs substrate interface could bend the dislocations

effectuality [12]. In the Figure 2-8, the similar mechanism can be easily used to grow two step Si_xGe_{1-x} buffer layers to reduce dislocation density in the top Ge epitaxial layer on Si (100) substrate. The structure contains two Si_xGe_{1-x} buffer layers which include the 1st $Si_{0.1}Ge_{0.9}$ and 2nd $Si_{0.05}Ge_{0.95}$ buffer layers and then the pure Ge layer has grown on the top of the two buffer layers. These two Si_xGe_{1-x} buffer layers create the interface with stress to prevent the penetration of dislocations. The structure can be used to attain the low dislocation density and high quality Ge layer and it also can be used as a high quality epitaxy template for GaAs growth and enables the integration between Si substrate and III-V electric devices.
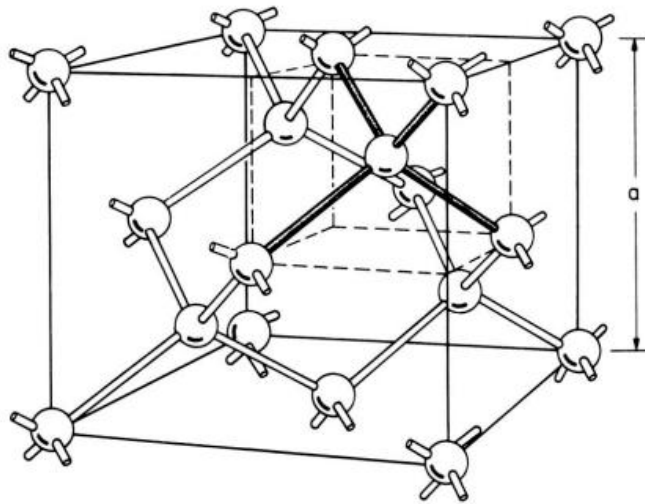
Figure 2-1: Diamond lattice structure of Si and Ge
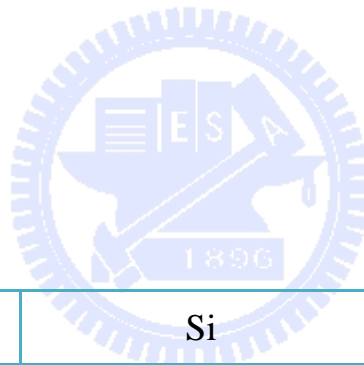
	Si	Ge
Crystal structure	Diamond	Diamond
Band gap energy (eV)	1.12	0.66
Lattice constant (Å)	5.43095	5.6579
Electron mobility (cm^2/Vs)	1500	3900
Hole mobility (cm^2/Vs)	450	1900
Linear coefficient of thermal expansion (10^{-6}/K)	2.6	5.9

Table 2-1: Basic properties of Si and Ge
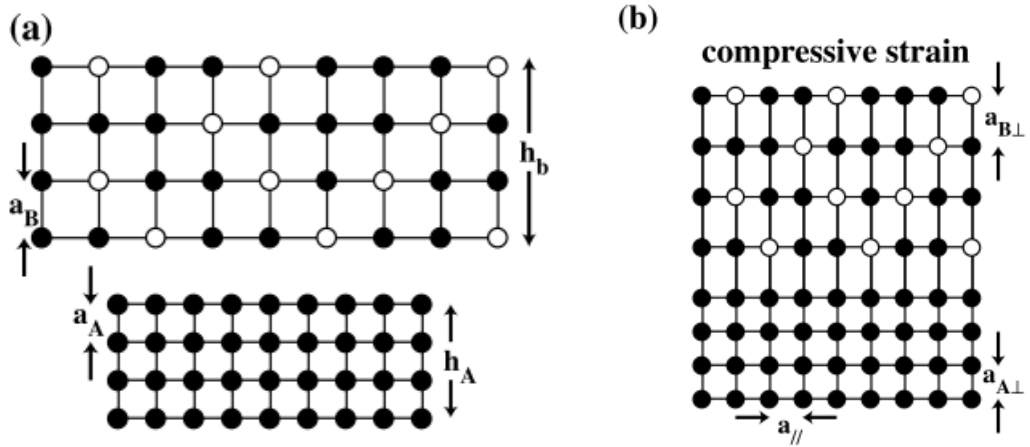
○: Ge   ●:Si

Figure 2-2: (a) A thin $Si_{1-x}Ge_x$ film with original lattice constant grown on top of a Si substrate (b) The top $Si_{1-x}Ge_x$ film will be compressive strain when the $Si_{1-x}Ge_x$ film grown on Si layer [6]
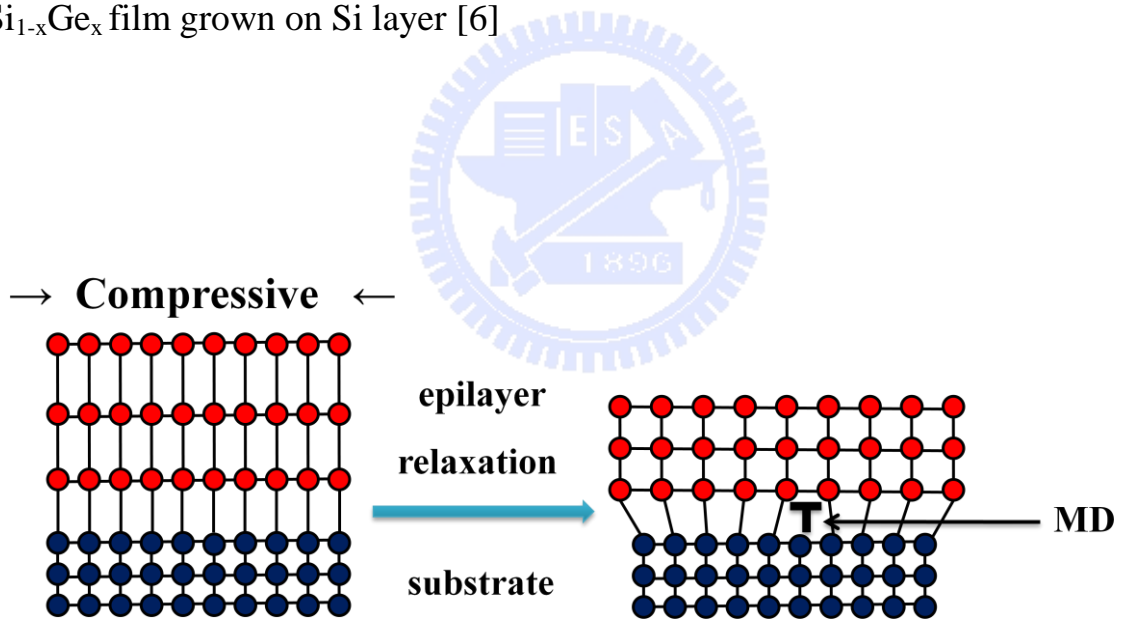
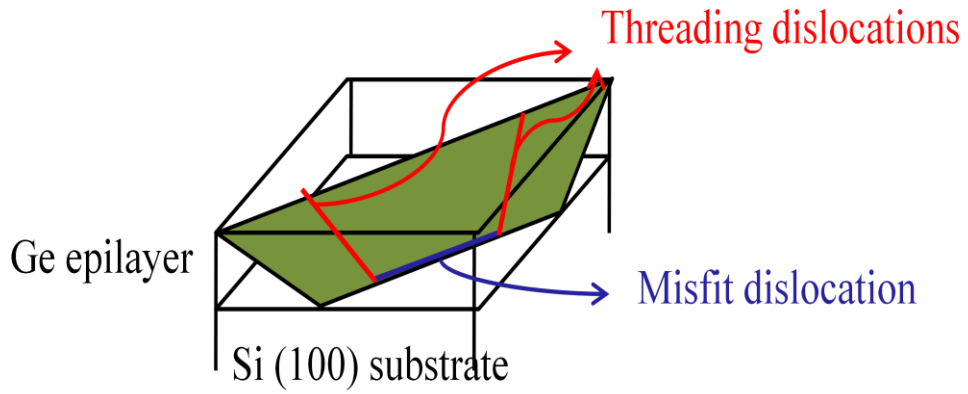Figure 2-3: The right relaxed epilayer introduced misfit dislocations

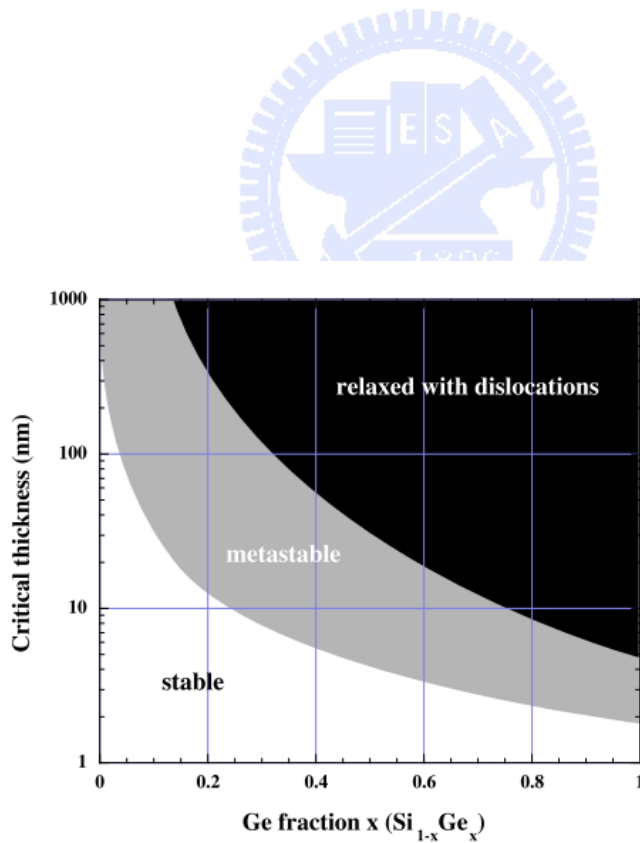Figure 2-4: The illustration of misfit and threading dislocations in Ge layer

Figure 2-5: The Matthews and Blakeslee critical thickness plotted against Ge fraction for $Si_{1-x}Ge_x$ layers grown in Si (100) substrate [8]
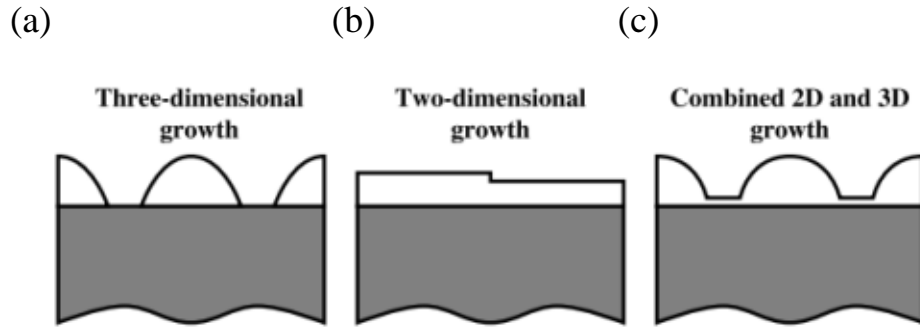
Figure 2-6: The three main growth modes for epitaxial growth of semiconductor. (a) three-dimension growth through Volmer-Weber mode, (b) two-dimension growth through Frank-van der Merwe mode and (c) combined two- and three-dimension growth through Stranski-Krastanov mode [9]
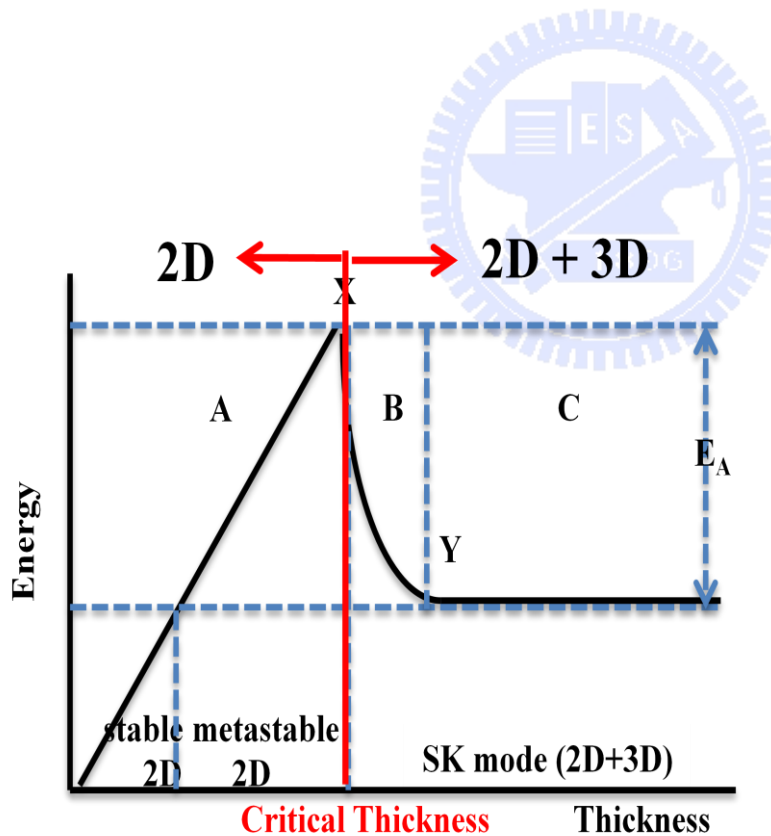

Figure 2-7: The nucleation and growth of SK islands. In region A the material grows layer by layer. The islands start to nucleate and grow in region B, and in region C the islands grows constantly.
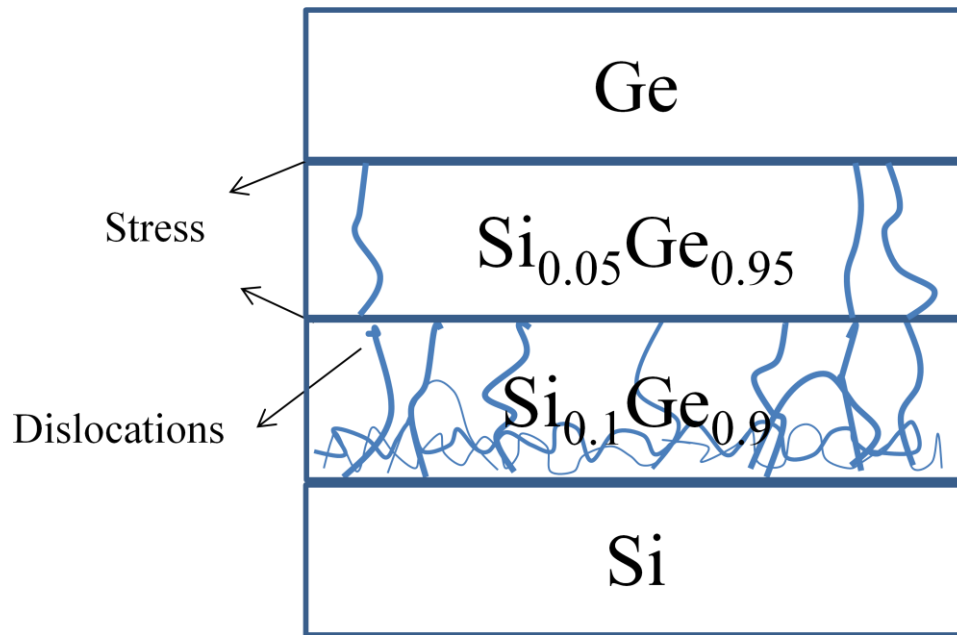
Figure 2-8: The structure of two-step Si_xGe_{1-x} buffer layers

Chapter 3

Experimental process

3.1 Chemical vapor deposition (CVD) system

A typical scheme of a CVD reactor is presented in Figure 3-1. A mixture of the precursor gases is diluted in a carrier gas (usually H_2) and injected into a chamber, heated by a radio-frequency, infrared lamp or a resistance heater. The substrate is placed over a graphite susceptor in the hot zone of the reactor. The precursor gases decompose after reaching a high temperature region and start to deposite on the substrate. The conditions of the flow dynamics, the chamber geometry, the precursor partial pressure and the operating pressure must be carefully chosen in order to promote an ordered deposition onto the substrate. Parasitic deposition on the reactor walls and heterogeneous reaction in the gas phase may hinder the crystal quality of the epilayer. Several commercial deposition systems are available on the market, but home-made reactors are also common in research institutes.

Today the most common technique to achieve Ge epitaxy is a CVD related process, with some variants such as metal-organic vacuum phase epitaxy (MOVPE), ultra high vacuum CVD (UHV/CVD) or plasma enhanced CVD (PECVD). In conventional CVD, epitaxial growth is performed with partial pressures of water vapor and oxygen greater than 10^{-4} torr. The majority of this water vapor and oxygen is due to outgassing from the walls of the chamber [13]. Contaminants such as oxygen and H_2O lead to precipitates that can result in extended lattice defects such as stacking faults and microtwins. At growth temperatures below 1000 ℃ there is high incorporation of these contaminants. These defects can cause polycrystalline inclusions in the film or result in polycrystalline growth, leading to increased surface roughness [14]. UHV/CVD utilizes very low base pressures in the growth chamber to reduce the amount of

H_2O, O_2, and other contaminants to which the wafer is exposed before and during the growth of epitaxial films. Because of this, lower temperatures that are required for the growth of strained $Si_{1-x}Ge_x$, $Si_{1-x-y}Ge_xC_y$ and $Si_{1-y}C_y$ films can be used. Moreover, the lower temperatures could reduce the atoms of epitaxial layers diffusing into Si dramatically [15], allowing sharp Ge, C, and dopant transitions.

3.1.1 Ultra high vacuum CVD (UHV/CVD) system

The machine used in this thesis is a multiple wafer UHVCVD reactor system. The growth system shown in Figure 3-2 consists of two chambers, a load lock chamber and a growth chamber where base pressure are under 10^{-7} torr and 10^{-9} torr respectively. The purpose of the load lock is to serve as an intermediary between the atmosphere and the deposition chamber, providing the isolation that ensures vacuum quality and integrity of the deposition chamber.

(a) Chamber system

The UHV/CVD growth chamber is made of quartz which is inserted into a furnace. One side of the growth chamber connects with two pumps which including a dry pump and a turbo pump. The other side of the quartz tube links load lock chamber which is constructed of stainless steel. The load lock chamber is also connected with the other turbo pump and a mechanical pump and has quick access door that enables loading the wafers. And the wafers can be put into the 4" quartz boat which is placed in the load lock. The growth chamber is resistance heated and is continuously pumped to keep UHV pressures all the time. The base pressure is as low as 10^{-9} torr, keeping the chamber practically free from contaminants.

(b) Transport system

The transport system has the transfer rod assembly consisting of a magnetically coupled and linear motion feedthrough. The linear motion feedthrough is used to locate the transfer rod precisely during the transferring and loading of the quartz boat.

(c) Gas system

Gases are introduced from the start of the chamber controlled by mass flow controllers (MFC) and vented at the end by the vacuum system consisted by mechanical and turbo pump. The source gases used in UHV/CVD to grow Si_xGe_{1-x} structure are silane (SiH_4) and germane (GeH_4).

3.1.2 Epitaxy in UHV/CVD

UHV/CVD operates at a very low pressure (base pressure of 10^{-9} torr) and a low temperature (~400℃). The effect of auto-doping, where dopants from the substrate diffuses into the epilayer and into the gas to be re-adsorbed later downstream, will be reduced. The system operated at low temperature also makes it possible to grow epitaxial films with very abrupt interfaces and doping profiles, which is useful for many device applications.

The low growth pressure means that growth rate is quite slow (~ 1-10 Å/min). But it also implies that the gas flow is molecular, with a molecule mean free path much longer than the reactor length. As mentioned above, turbulence effects are minimal and an even distribution of molecules over the samples can be assumed [16]. The throughput of UHV/CVD is high despite of the low growth rates, since simultaneous growth of multiple wafers is possible.

In many epitaxial systems, many problems would occur by impurity such as water vapor, oxygen and hydrocarbons. Due to the extremely low pressure in the UHV/CVD growth chamber and the nature of the turbo pumps the partial pressures of the impurities are insignificant [17]. The only impurities which came from the source gases silane and germane may not be completely pure. But due to the fact that the pressure during the growth is only about 10^{-3} torr, an impurity concentration of 1 ppm would only give a partial pressure on the order of 10^{-9} torr and should not be a big issue for the growth of epitaxial film.

3.1.3 Chemical reaction in UHV/CVD

In CVD growth three different regimes are recognized, that depend mainly on the growth temperature including thermodynamically limited growth, mass

transport limited growth and surface kinetics limited growth. In the thermodynamically limited growth regime, which occurs at high temperatures above 800 ℃, the deposition is mainly affected by the desorption of atoms from the growth surface. Mass transport limited growth is referred to as conventional growth regime and occurs roughly between 550-800 ℃. In this regime, the growth rate and composition of the forming epitaxial layer is determined by the input partial pressure such as the flux of precursors. The growth temperatures in surface kinetics limited growth regime are lower than in the mass transport limited growth regime starting from about 600 ℃ and reaching as low as 400 ℃. The surface adsorption rate of reaction source is lower than the diffusion rate of reactant source in the boundary layer. Therefore, in this region, the growth rate depends on the surface reaction rate and increases with increasing temperature. Si_xGe_{1-x} or Ge layers are often grown at low growth temperature in UHV/CVD and that means the growth regime is the surface kinetics limited mode. Epitaxial growth will be discussed by the adsorption and decomposition of the hydride on the surface. The initial reaction for deposition of a species X is

$$XH_4 + 2^* \rightarrow XH_3{}^* + H^* \qquad (3-1)$$

where XH_4 is the hydride of the species X (Si or Ge), 2* represents two free surface sites and H* indicates a species bonded to a surface site. The following reaction is a series of reactions that further reduce the hydride. The final reaction is

$$XH^* \rightarrow X^* + \frac{1}{2}H_2 \qquad (3-2)$$

which results in the deposition of a film of species X on the surface. What is clear from these reactions is that the rate of deposition is limited by the amount of vacant surface sites. Most of these are being occupied by hydrogen from the initial reactions and thus it is the hydrogen desorption rate that ultimately decides the rate of film growth [18].

The activation energy for hydrogen desorption from Si (100) surface has been determined to be around 2.13 eV. At low temperature this energy is not readily available, and thus hydrogen desorption will be inefficient and the growth is very slow. At higher temperature, hydrogen will be desorbed more efficiently and the regime enters the diffusion limited regime, where it is the supply of the hydrides that determine the growth rate. This regime transition is evident from the kink in the growth rate diagrams of Figure 3-3.

The activation energy for hydrogen desorption from a Ge(100) surface is 1.69 eV. This value is lower than that for the Si (100) surface because of the weak Ge-H bond. This means that Ge growth should be possible at a lower temperature compared with Si growth, and it is verified by comparing Figure 3-3(b) to (a).

3.1.4 Growth rate of SiGe

During SiGe growth, when both SiH_4 and GeH_4 are present, the growth rate is accelerated. This cooperative growth phenomenon has been studied [19], and one explanation is that the Ge atoms presenting on the growth interface acts as desorption centers for hydrogen. The activation energy for hydrogen desorption is lowered by as much as 0.22 eV, and for 20 % Ge layers grown at 550 ℃, the growth rate is enhanced by a factor of 25.

The growth rate enhancement is very important for layers with a low Ge percentage. During growth of Si_xGe_{1-x} layers with high Ge percentage, the GeH_4 partial pressure will be larger, and much of the surface will be covered by the intermediate product of the GeH_4 dissociation. The hydrogen desorption will therefore no longer be as efficient and the growth rate drops [20].

Between 570 ℃ and 700 ℃ there is a peak in the growth rate at some low x-value. Below 570 ℃ the grow rate will steadily increase and it will steadily decrease above 700 ℃, this phenomena is shown in Figure 3-4 [21]. At high x-values the growth rate is independent of x [22], and should therefore be approximately equal to the growth rate of pure Ge.

3.2 Experimental flow

The epitaxial SiGe and Ge layers were grown on Si by UHVCVD equipment using silane (SiH_4) and germane (GeH_4) as the Si and Ge sources.

The 4" Si substrates were cleaned by immersing in deionized water (DI water) for 3 mins and dipping in 10% hydrofluoric acid (HF) for 5 sec to remove silicon oxide away. After dipping HF, Si substrates were quickly loaded into load lock chamber on a quartz boat to prevent exposing under the atmosphere. The oxide-free surface and surface passivated by the dangling bonds terminated with hydrogen are obtained by the HF dipping process.

In the growth of 1st SiGe buffer layer, the composition of Si and Ge are 0.1 and 0.9. The composition of buffer layers is adjusted by SiH_4/GeH_4 flux ratio. Then the 2nd SiGe buffer layer where the composition of Si and Ge are 0.05 and 0.95 has grown on the top of the 1st SiGe buffer layer and finally the pure Ge layer has grown on this structure. Between the processes of each epitaxial layer, annealing step is introduced for 10 minutes at 600 ℃ to improve the crystal quality of the epitaxial layers. Finally, annealing was performed again at 600 ℃ for 10 min in order to remove defects that are possibly generated in the growth of Ge layer.

3.3 Fundamental of characterization techniques

The epitaxial layers are analyzed by several parameters, including thickness, surface morphology, uniformity, dislocation density, and film quality. Each parameter can be characterized by one or more measurement techniques. Several

common characterization techniques are used in this study, including X-ray diffraction (XRD), scanning electron microscopy (SEM), transmission electron microscopy (TEM), and atomic force microscopy (AFM). All the results will be briefly introduced and discussed.

3.3.1 X-ray diffraction (XRD)

Atoms or molecules that compose a substance are generally arranged at a distance of 0.1 nm to 0.5 nm from one another. When such a substance is irradiated with X-ray having a wavelength roughly equivalent to the inter-atomic or intermolecular distance, X-ray diffraction will take place. X-ray diffraction (XRD) is widely used in the field of semiconductor research because it is a nondestructive technique and yields crystal structure information in an atmospheric environment.

X-rays are electromagnetic radiation with typical photon energies in the range of 100 eV - 100 keV. For diffraction applications, only short wavelength X-rays in the range of a few angstroms to 0.1 angstrom (1 keV - 120 keV) are used. Because these wavelengths of X-rays are comparable to the size of atoms, they are ideally suited for probing the structural arrangement of atoms and molecules in a wide range of materials. The energetic X-rays can penetrate deep into the materials and provide information about the bulk structure. X-rays are produced generally by either X-ray tubes or synchrotron radiation. In an X-ray tube, which is the primary X-ray source used in laboratory X-ray instruments; the X-rays are generated when a focused electron beam accelerated by a high voltage field bombards a stationary or rotating solid target. As electrons collide with atoms in the target and slow down, a continuous spectrum of X-rays are emitted, which are termed Bremsstrahlung radiation. The high-energy electrons

also eject inner shell electrons in atoms through the ionization process. When a free electron fills the shell, an X-ray photon with energy characteristic of the target material is emitted. Common targets used in X-ray tubes include Cu and Mo, which emit 8 keV and 14 keV X-rays with corresponding wavelengths of 1.54 Å and 0.8 Å, respectively. When X-ray photons collide with electrons, photons from the incident beam will be deflected away from the direction where they original travel. If the wavelength of these scattered x-rays is not changed (meaning that X-ray photons did not lose any energy), the process is called elastic scattering (Thompson scattering) in that only momentum has been transferred in the scattering process. These are the X-rays measured in diffraction experiments, as the scattered X-rays carry information about the electron distribution in materials. On the other hand, in the inelastic scattering process (Compton scattering), X-rays transfer some of their energy to the electrons resulting in scattered X-rays with different wavelengths than the incident X-rays. Diffracted waves from different atoms can interfere with each other and the resultant intensity distribution is strongly modulated by this interaction. If the atoms are arranged in a periodic fashion, as in crystals, the diffracted waves will consist of sharp interference peaks with same symmetry corresponding to the distribution of atoms. Measuring the diffraction pattern therefore allows us to deduce the distribution of atoms in a material. For a given set of lattice plane with an inter-plane distance of d, the condition for a diffraction peak to occur can be simply written as

$$2d \sin \theta = n\lambda \qquad (3-1)$$

which is known as Bragg's law. In the equation, λ is the wavelength of the X-ray, θ the scattering angle, and n an integer representing the order of the diffraction peak. The schematic of Bragg's law is shown in Figure 3-5.

This XRD analysis is especially important for characterizing thin films epitaxially grown on substrates because these epitaxial films have vital technological applications in microelectronic and optoelectronic devices, where high quality epitaxial films are critical for device performance. There are several special considerations for using XRD to characterize thin film samples. First, reflection geometry is used for these measurements, as the substrates are generally too thick for transmission. Second, high angular resolution is required because the peaks from semiconductor materials are sharp due to very low defect densities in the material. Consequently, multiple bounce crystal monochromators are used to provide a highly collimated x-ray beam for these measurements. Typically, the configuration of double-crystal diffraction is used to provide high accuracy because the produced beam is highly collimated than the beam produced by single-crystal diffraction. Double crystal diffraction consists of two successive Bragg reflections including reference and sample crystals and the reflection from the first reference crystal produces a monochromatic and highly parallel beam to probe the sample. This double crystal diffraction configuration is mainly used for extracting a rocking curve, which is the most important tool by providing data on lattice mismatch, layer thickness, and the epitaxial layer quality, and wafer curvature for epitaxial layers. To record a rocking curve, the sample is slowly rotated or rocked with respect to an axis normal to the diffraction plane and the scattered intensity is recorded as a function of the scanning angle. The width of the rocking curve directly reflects the perfection of materials; for example, the narrower the curve, the higher crystalline quality are the materials.

Here is a summary that basic XRD measurements made on thin film samples; lattice constant - measurements derived from 2θ - θ scans, which

provide information about lattice mismatch between the film and the substrate and are therefore indicative of strain and stress. Rocking curve - measurements made by doing a θ scan at a fixed 2θ angle, the width of which is inversely proportionally to the dislocation density in the film and is therefore used as a gauge of the quality of the film. Superlattice - measurements in multilayer heteroepitaxial structures, which manifest as satellite peaks surrounding the main diffraction peak from the film. Film thickness and quality can be deduced from the experimental data. Glancing incidence X-ray reflectivity measurements can determine the thickness, roughness, and density of the film. This technique does not require crystalline film and works even with amorphous materials.

3.3.2 Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) is similar to optical microscopy with exception that electrons are used instead of photons and the image is formed in a different manner, which will be described next. An SEM consists of an electron gun, a lens system, scanning coils, an electron collector, and cathode ray display tube (CRT). Electrons emitted from an electron gun pass through a series of lenses to be focused and scanned across the sample. The most common electron gun is a tungsten hairpin filament emitting electrons thermionically with an energy spread of around 2 eV. Tungsten sources have been largely replaced by lanthanum hexaboride (LaB 6) sources with higher brightness, lower energy spread (~ 1 eV) and longer life. Field emission guns are about 100× brighter than LaB 6 sources and 1000× brighter than tungsten sources, respectively and energy spread of about 0.2 to 0.3 eV can be achieved with even longer lifetime than the other sources. The emitted electrons are accelerated through a voltage up to ~30 kV, and the resulting beam is finely focused by a series of magnetic

coils to form a spot on the specimen. A scan generator moves this spot across the specimen via two sets of scan coils. The electrons that escape from the sample comprise the signal and can be collected by various electron detectors depending on the applications to monitor some emission (or property of) the specimen. The resultant signal is amplified and transferred to the display device.

The electron energy used in SEM is in the range of 10 - 30 keV for most samples, but for insulating samples the energy can be as low as several hundreds eV. The use of electrons has two main advantages over optical microscopy such as the higher magnification possible using electron wavelengths and the greater depth of field. The electron wavelength, λ_e, depends on the electron velocity, v, and the accelerating voltage, V, can be written as

$$\lambda_e = \frac{h}{mv} = \frac{h}{\sqrt{2qmV}} = \frac{1.22}{\sqrt{V}} \qquad (3-2)$$

As an example, a voltage of 10 kV results in the wavelength of 0.012 nm. This wavelength, significantly below the 400 - 700 nm wavelength of visible light, allows for making a resolution of SEM much greater than that of optical microscopy. The focused beam of electrons is either scanned across the surface of the specimen to form an image or stopped on a fixed location to perform one of a variety of spectrographic or analytical functions. The interaction of the beam with the specimen results in the generation of secondary electrons, backscattered electrons, Auger electrons, characteristic x-rays, and photons of various energies. Electrons and photons are emitted at each beam location and subsequently detected. Secondary electrons from the conventional SEM image, backscattered electrons can also form an image; X-rays are used in the electron microprobe, emitted light is known as cathode luminescence, and absorbed electrons are measured as electron beam induced current. Figure 3-6 shows the

various signals that are emitted by the electron beam, along with the spatial region of the sample from which each signal is emitted [28]. Pertinent analysis modes used in this research are secondary electrons and electron beam induced current.

Secondary electrons – Secondary electrons are used in imaging and provide surface topographic information. The high energy incident beam electrons interact with loosely bound conduction band electrons in the specimen giving up some of their energy. The amount of energy given to these secondary electrons is small, so they have a very limited range (a few nm) in the sample. Moreover, only those secondary electrons excited near the surface have sufficient energy to be emitted from the surface and detected. Therefore, the imaging via secondary electrons is the "standard" SEM mode of imaging since it provides better resolution versus plotting backscattered electron concentrations or the x-ray signal as the secondary electrons are largely emitted from a region relatively near the surface. Primarily, secondary electrons provided topographical information for studies on large scale defects that included etch pits counting for EPD measurements as well as surface morphology information. As a secondary tool, it was used in conjunction with the other SEM modes for sample orientation and identification of topographic artifacts.

Electron Beam Induced Current – Materials characteristic can also be obtained as a result of the beam injecting charge carriers into the specimen. By making electrical connections to the sample, the induced current from these carriers can be collected, amplified, and, via the SEM scan circuitry, displayed on a CRT. The sample can be inspected in both planar and cross-section geometries providing both surface and depth information. By combining this technique with other SEM viewing modes, the position of crystalline defects,

p/n junctions, and other electrically active characteristics can be correlated to the surface topography. EBIC images are a plot of the current flowing through a p-n junction or Schottky barrier due to the electron beam-induced electron-hole pairs (ehp's) vs. lateral position. These carriers are resultant from the incident beam and are confined to a finite volume of the material, referred to as the carrier generation volume. Effectively, the image displayed is the ehp collection efficiency that is extremely sensitive to electrically active defects such as dislocations, grain boundaries, inclusions, and anti-phase domains. One application is to use EBIC as a complementary tool to etch pit density (EPD) measurements. In fact, EBIC can be a superior method to EPD in that it is a non-destructive technique. In addition, it can complement TEM with respect to threading dislocation density measurements, since EBIC performs well below 10^6 cm^{-2} density levels where TEM is inapplicable.

3.3.3 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) is, in principle, similar to optical microscopy; both contain a series of lenses to magnify the sample. The main strength of TEM lies in its use of electrons instead of using optical light sources to attain extremely high resolution, approaching 0.15 nm. The high resolution of TEM can be explained by the following equation

$$s = \frac{0.61\lambda}{NA} \qquad\qquad (3-3)$$

where s is the resolution (the minimum distance between points or parts of an object) that satisfies Raleigh's criterion. NA means a numerical aperture, a number that expresses the resolving power of the lens and the brightness of the image it forms. In optical microscopy, NA ~ 1 and λ ~ 500 nm, give s ~ 300 nm. In electron microscopy, the NA is approximately 0.01 due to larger electron lens

imperfections, but the wavelength is much shorter. As an example, if $\lambda_e \sim 0.004$ nm for V = 100 kV is used, the resolution s ~ 0.25 nm and magnifications of several hundred thousand can be obtained.

A schematic of a TEM is shown in Figure 3-7. Electrons from an electron gun are accelerated by high voltages typically 100 - 400 kV, and focused on the sample by condenser lenses. The sample is placed on a small copper grid a few mm in diameter. The static beam has a diameter of a few microns. The sample must be sufficiently thin (a few tens to a few hundred nm) to be transparent to electrons, in which the thickness restriction is critical to avoid the resolution problem caused by the beam spreading after the electrons scatter into thick film. The transmitted and forward scattered electrons form a different pattern in the back focal plane and a magnified image in the image plane. With additional lenses, either the image or the diffraction pattern is projected onto a fluorescent screen for viewing or for electronic or photographic recording. The ability to form a diffraction pattern allows structural information to be obtained.

There are a number of TEM imaging modes available. TEM micro structural imaging in diffraction contrast provides information on large structures and crystallographic features. Bright and dark field imaging can be performed and is useful or identifying crystal defects and mapping diffracting domains. Electron diffraction analysis can be used in a variety of modes and provides crystal phase identification, specimen preferred orientation information, and the determination of crystal lattice constants. Electron diffraction is also an important tool employed in crystal defect identification. Finally, EDS in spectrum and mapping modes is as described in the SEM section. Again, higher voltages, thin specimens, and better resolving power distinguish the method as practiced in TEM.

TEM imaging may be done in either cross-sectional or plan-view modes, dependent upon sample preparation. The electron beam transparency requirement demands a sample thickness on the order of 200 nm or less, requiring a complex sample preparation process involving polishing, grinding, dimpling, and ultimately ion milling to produce the final thinned sample. Cross-sectional TEM further requires gluing together a stack of wafers with the desired interface at the center. This stack is then processed similarly to plan-view samples. For cross-sectional samples it is essential to dimple and ion mill centered upon the target interface in order to image it. Dislocations, anti-phase domains, stacking faults, interface roughness, and other crystallographic defects can be imaged to provide extensive information about each, including dislocation Burgers vectors, domain orientations, etc. TEM can provide statistically accurate threading dislocation densities for values above 1×10^7 cm^{-2}, where etch pit density measurements become inaccurate. Below this level, however, TEM becomes statistically inaccurate due to the excessive number of imaging areas required to assess these low densities, for which typically less than one dislocation per field of view is observed. TEM can also distinguish individual layers in a multi-layer structure if there is sufficient electron beam scattering contrast. Practically, this means that compositional differences are observable, but not doping differences.

3.3.4 Atomic force microscopy (AFM)

Atomic Force Microscopy (AFM) is a further development on the basis of scanning probe microscopy (SPM) implemented in the mid 1980's. The AFM is an imaging tool with a vast dynamic range, spanning the realms of optical and electron microscopes, and is operated as a surface profiler with unprecedented

3D-resolution. In atomic force microscopy the surface of a sample is scanned with a sharp tip that is several micrometers long and has a smallest diameter of typically 10 nm. It is located on the free end of a cantilever (100–200 µm) as shown in Figure 3-8. Forces between the sample and the tip cause the cantilever to bend or deflect. As the tip scans across the surface, these deflections are measured with a detector and allow a computer to generate topographic maps.

The force most commonly associated with cantilever deflection in atomic force microscopy is the interatomic van der Waals force. The dependence of this van der Waals force upon the distance between the tip and the sample surface is depicted in Figure 3-9. Three distance regimes are labeled in Figure 3-9 including contact regime, non-contact regime, and intermittent-contact regime. In the so-called contact mode the tip is held less than a few Angstroms above the sample surface, and the van der Waals force between tip and sample is repulsive. In non-contact mode the tip is held tens or hundreds of Angstroms from the surface, and therefore the intermittent force is attractive due to long-range van der Waals interactions.

(a) Contact mode

In this repulsive mode the AFM tip makes soft " physical contact" with the sample. The tip is attached to the cantilever with a low spring constant, and therefore the contact force causes the cantilever to bend and accommodate the changes in topography, as the scanner traces the tip across the sample.Usually, the position of the cantilever (degree of deflection) is detected with optical techniques. A laser beam is reflected from the back of the cantilever onto a position-sensitive photodetector. A change in the bending of the cantilever results in a shift of the laser beam on the detector. This system is suited to resolve the vertical movement of the cantilever tip with sub-Angstrom resolution.

The AFM can be operated either in constant-height or constant-force mode. In constant height mode the height of the tip is fixed, and the spatial change in cantilever deflection is used to generate the topographic data. In constant force mode a feed-back loop moves the scanner up and down in z-direction, responding to the local topography, and thereby keeping the force and thus the deflection of the cantilever constant. In this case the topographic map can be directly drawn using the z-motion of the scanner as height information. Due to the "hard contact" between tip and sample, soft surfaces may be deformed, tips may collect dirt or are rubbed of and become blunt.

(b) Non-contact mode

In non-contact mode, the system vibrates a stiff cantilever with amplitude of a few tens to hundreds of Angstroms near its resonant frequency (several 100 kHz). Using a sensitive AC detection scheme, the changes in resonant frequency of the cantilever are measured. Since the resonant frequency is a measure of the force gradient, the force gradient reflects the tip-to-sample spacing. Comparable with the constant-force mode in contact regime, a feed-back system moves the scanner up and down in order to keep the resonant frequency or amplitude constant. Again this corresponds to a fixed tip-to-sample distance, and the motion of the scanner is used to generate the topographic data set. This mode does not suffer from tip or sample degradation effects and is suited to scan even soft samples and to keep the tips sharp.

(C) Intermittent-contact mode

Intermittent-contact AFM is similar to non-contact AFM, except that in this mode the vibrating cantilever tip is brought closer to the sample, so that it barely hits or taps the surface. The changes in cantilever oscillation amplitude responding to the tip-to-sample separation are monitored to obtain the surface

topography. This mode is usually preferred as it combines the high resolution of contact mode, and the low wear and tear of the tip in non-contact mode.
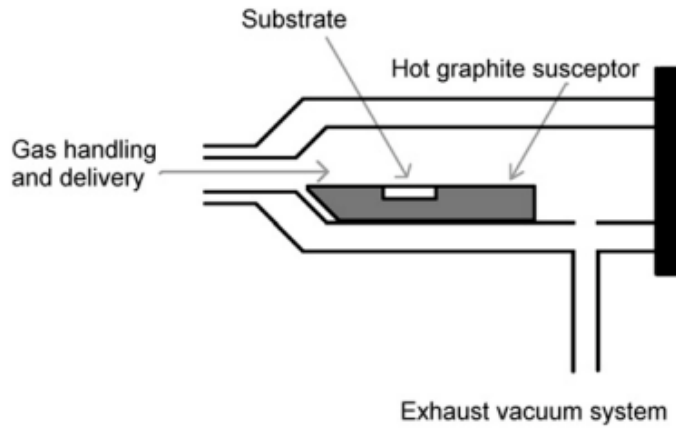
Figure 3-1: The scheme of standard CVD reactor
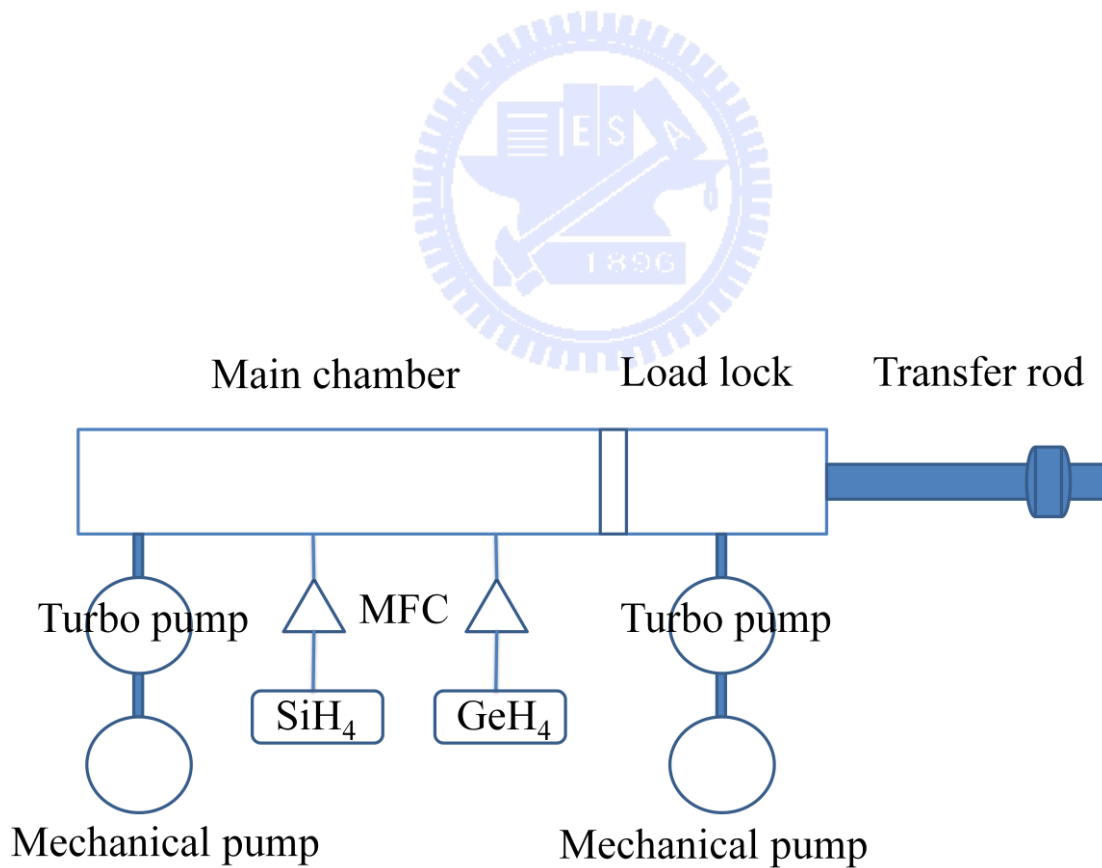
Figure 3-2: The scheme of UHV/CVD system
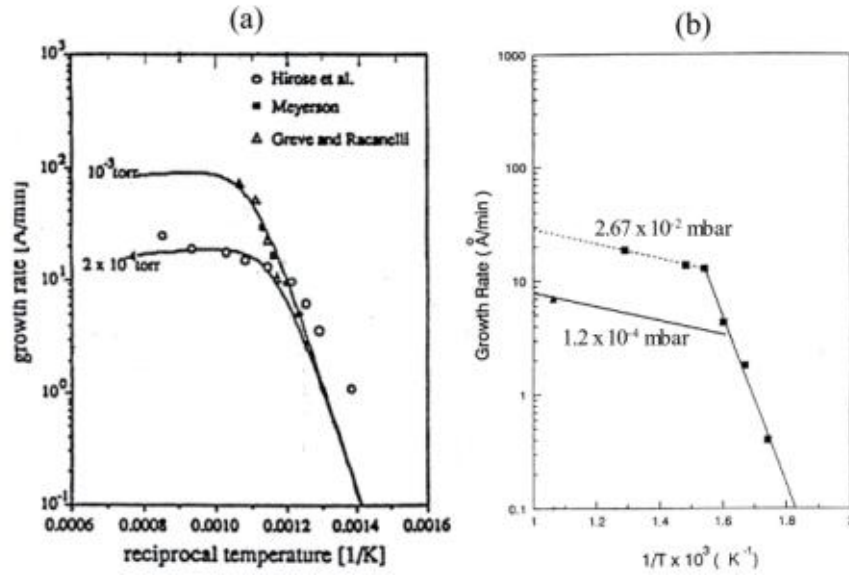
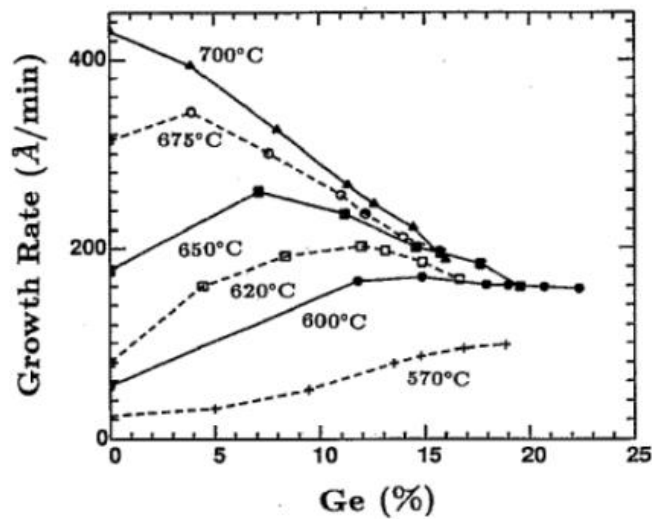Figure 3-3: (a) Growth rate of silicon at different silane pressure and(b) germanium at different german pressure [18]

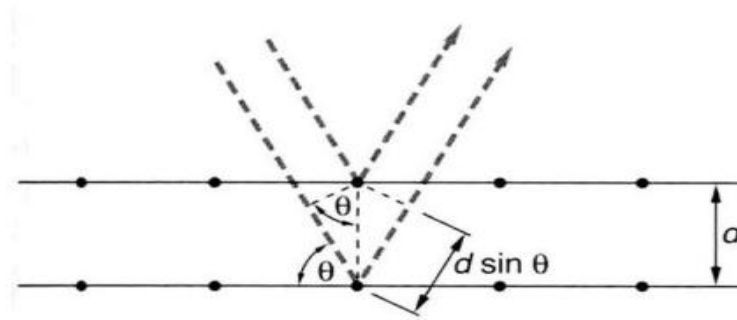Figure 3-4: Behavior of SiGe growth rate at different temperatures [19]

Figure 3-5: A schematic of Bragg's law. The optical path difference is 2dsinθ.
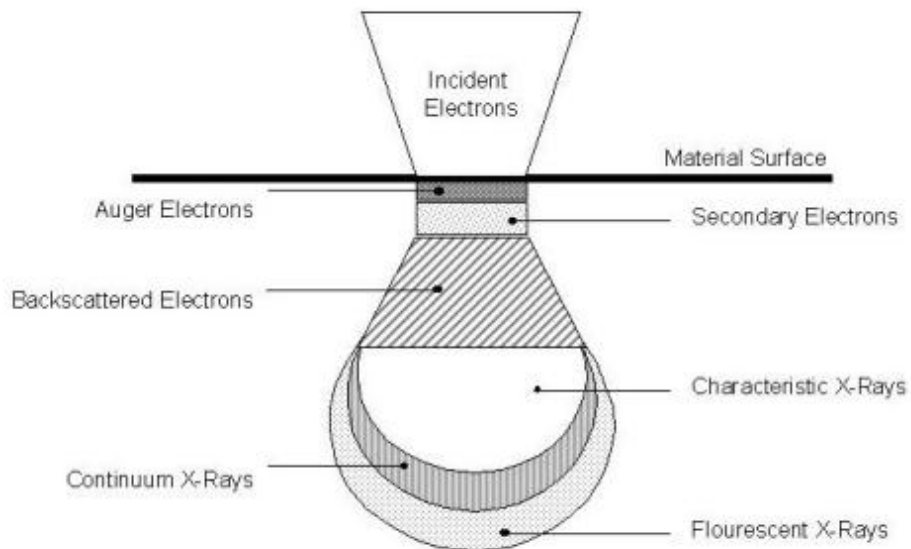
Figure 3-6: Plot of the excitation volume generated by the SEM electron beam
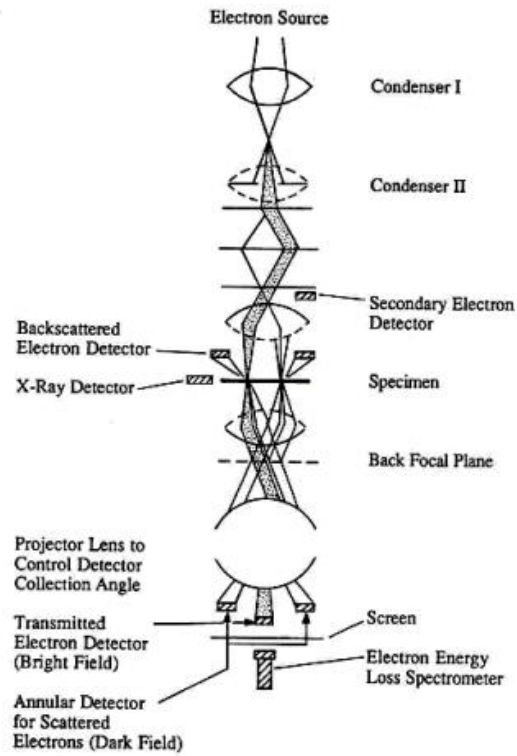
Figure 3-7: A schematic of transmission electron microscope
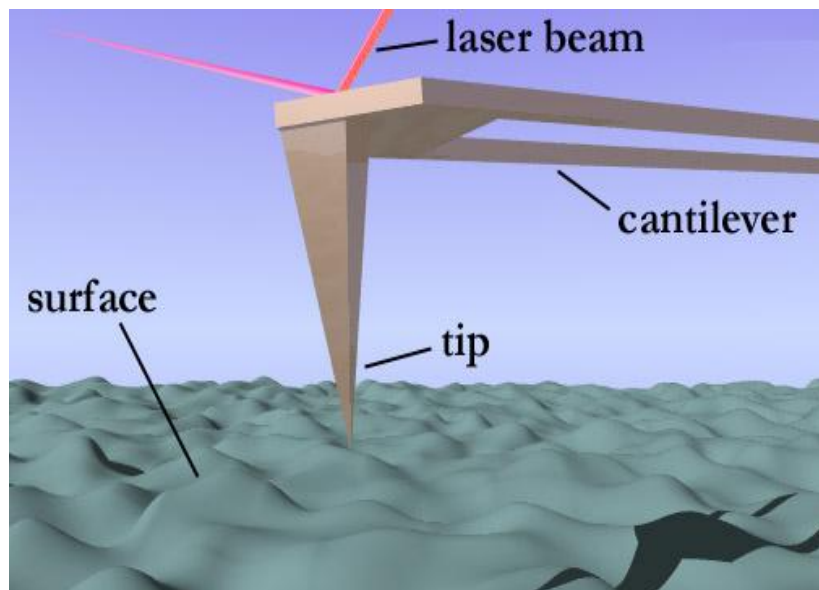
Figure 3-8: A schematic of atomic force microscopy
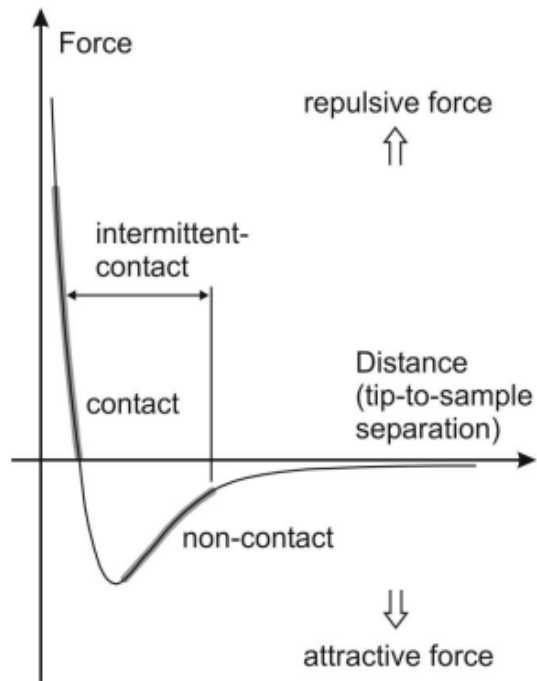
Figure 3-9: Dependence of interatomic force on tip-sample separation

Chapter 4
Results and discussion

In this chapter, the effect of growth temperature and annealing process on the $Ge/Si_{0.05}Ge_{0.95}/Si_{0.1}Ge_{0.9}/Si$ heterostructure are discussed. The result of 1st $Si_{0.1}Ge_{0.9}$ buffer layer, 2nd $Si_{0.05}Ge_{0.95}$ buffer layer and Ge epitaxial layer will be discussed respectively. On the other way, multi-annealing treatment for 1st $Si_{0.1}Ge_{0.9}$ buffer layer will also be introduced in the following.

4-1 Effect of SiH_4/GeH_4 flow ratio on composition of Si_xGe_{1-x} buffer layer

The epitaxial Si_xGe_{1-x} and Ge layers were grown on Si by UHVCVD using silane (SiH_4) and germane (GeH_4) as the Si and Ge sources. The Si/Ge ratio in Si_xGe_{1-x} buffer layer is a proportional to flow ratio of SiH_4/GeH_4 as shown

$$\frac{x}{1-x} = m \frac{P_{SiH_4}}{P_{GeH_4}} \qquad (4-1)$$

where x is Si content, 1-x is Ge content, m is a constant which is about 3.5 ~ 4 . P_{SiH_4} and P_{GeH_4} are partial pressures of SiH_4 and GeH_4 respectively [21].

At first, the 1st $Si_{0.1}Ge_{0.9}$ buffer layer can be grown by adjusting different SiH_4/GeH_4 ratio. In Table 4-1, the samples A, B and C show the different SiH_4/GeH_4 flow ratio corresponding to different composition of Si and Ge which are analyzed by XRD. The XRD peak of 1st $Si_{0.1}Ge_{0.9}$ buffer layer shows 5050 arcsec from peak of Si substrate. In the experiment the relationship between the Si/Ge ratio and SiH_4/GeH_4 flow ratio is following the equation 4-1 where m is about 3.5~3.8. According to this relation, the composition of 2nd $Si_{0.05}Ge_{0.95}$ can easily find out in sample D. The XRD peak 2nd $Si_{0.05}Ge_{0.95}$ buffer layer shows 5350 arcsec from peak of Si substrate. Finally the flow ratio 0.4 and 0.2 of

SiH$_4$/GeH$_4$ will be used to grow 1st Si$_{0.1}$Ge$_{0.9}$ and 2nd Si$_{0.05}$Ge$_{0.95}$ buffer layer respectively.

4-2 Effect of growth temperature on 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer

Because the 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer also contains very high Ge content, the buffer layer has the large lattice mismatch to Si substrate. The problem of large lattice mismatch causes island growth mode (SK mode) and makes the surface rough [10].Usually, low growth temperature (~420 ℃) was used to grow high Ge content of Si$_x$Ge$_{1-x}$ layers with 1-x > 0.8 [23] because the low growth temperature reduces the atom diffusion length which suppresses roughness as shown in Figure 4-1.

In this experiment, the low growth temperatures are used in the 1st Si$_{0.1}$Ge$_{0.9}$ buffer layers with SiH$_4$/GeH$_4$ flow ratio of 0.4 to smooth the surface and benefit the following grown. In the Table 4-2, the growth temperature of 410, 390, 370 and 350 ℃ will be used in 1st Si$_{0.1}$Ge$_{0.9}$ buffer layers sample C1, C2, C3 and C4 respectively. AFM topographical images of sample C1, C2, C3 and C4 show in Figure 4-2(a)-(d). The samples clearly exhibit the undulation surface, in which the root mean square (RMS) roughness values decreases with growth temperature decreases. The RMS values are 45.4, 18.8, 11.8, 11.5 nm for samples C1, C2, C3 and C4 respectively. In both literature and experiment result, 1st Si$_{0.1}$Ge$_{0.9}$ buffer layers grown at lower temperature shows more smooth surface. Compared to the other research groups [24], the surface roughness of high Ge content of Si$_x$Ge$_{1-x}$ buffer layer is about 20 to 50 nm and the surface of 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer with low growth temperature (< 370 ℃) is smoother than others.

Figure 4-3 shows the XRD diffraction curves of 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer grown at 350 and 370 ℃ on Si substrate. In a comparison of the XRD measurement results of samples C3 and C4, the peak intensity value of C4

appears too low at 350 ℃. This indicates that growing a 1st $Si_{0.1}Ge_{0.9}$ buffer layer on a Si substrate at a growth temperature of 370 ℃ may be the ideal choice for a Ge/$Si_{0.05}Ge_{0.95}$/$Si_{0.1}Ge_{0.9}$/Si heterostructure.

The thickness of 1st $Si_{0.1}Ge_{0.9}$ buffer layer is 150nm which above critical thickness [8] ensures the fully strain relaxation in the layer. It can be proved by reciprocal space maps (RSM) of XRD measured. Figure 4-4 shows symmetrical (004) and asymmetrical (224) reciprocal space maps of the sample C3. The reflections from 1st $Si_{0.1}Ge_{0.9}$ buffer layer and Si substrate are clearly shown. The nearly circle-shaped iso-intensity contour from the Si substrate (see Figure 4-4 (a)) indicates that the curvature of the epitaxial layer is insignificant. In both maps, there is a broadening along the ω-scan direction, which implies that there is mosaicity in the epitaxial layer. In Figure 4-4(b), the peak of $Si_{0.1}Ge_{0.9}$ buffer layer slightly deviates from [224] direction through Si substrate peak, which indicates that the 1st $Si_{0.1}Ge_{0.9}$ buffer layer has weak strain which could be induced by thermal expansion mismatch between Si substrate [9] .

4-3 Effect of growth temperature on 2nd $Si_{0.05}Ge_{0.95}$ buffer layer

In this experiment, all 2nd $Si_{0.05}Ge_{0.95}$ buffer layer will grow on 1st $Si_{0.1}Ge_{0.9}$ buffer layer at a growth temperature of 370 ℃ (C3 sample). Low growth temperatures are also used in grown 100nm~150nm 2nd $Si_{0.05}Ge_{0.95}$ buffer layer with SiH_4/GeH_4 flow ratio of 0.2 to decrease surface roughness. In the Table 4-3, the growth temperature of 370, 350 and 330 ℃ will be used in sample D1, D2 and D3 respectively. AFM topographical images of sample D1, D2 and D3 show the RMS roughness of surface decrease with growth temperature decrease as shown in Figure 4-5(a)-(c). If grown the 2nd $Si_{0.05}Ge_{0.95}$ buffer layers at 350 and 370 ℃, the RMS roughness of surfaces will increase to 17.2 and 22.5 nm respectively. Because the 1st $Si_{0.1}Ge_{0.9}$ buffer layers already exhibit the

undulation surface, the surface of following 2nd $Si_{0.05}Ge_{0.95}$ buffer layers grown could be rougher at growth temperatures of 350 and 370 ℃. The 2nd $Si_{0.05}Ge_{0.95}$ buffer layer grown at 330 ℃ shows the RMS roughness of surface is about 13.9 nm which is slightly increase from that of 1st $Si_{0.1}Ge_{0.9}$ buffer layer. It is also proved the low growth temperature reduces the atom diffusion length which suppresses roughness.

Figure 4-6 shows the XRD diffraction curves of 2nd $Si_{0.05}Ge_{0.95}$ buffer layer grown at 330 and 370 ℃ on 1st $Si_{0.1}Ge_{0.9}$ buffer layer. Because the peak of the 1st and 2nd SiGe buffer layer is too close and still lots of dislocations in these two buffer layer, the curve of 1st $Si_{0.1}Ge_{0.9}$ buffer layer will be covered with 2nd $Si_{0.05}Ge_{0.95}$ buffer layer. In a comparison of the XRD measurement results of samples D1 and D3, the peak intensity value of D3 appears too low at 330 ℃. In grown the 1st and 2nd SiGe buffer layer, the poor crystal quality is observed in growth temperature less than 350 ℃ but these samples of low growth temperature show smoother surface roughness.

Before grown 3rd Ge layer, two growth temperatures of 2nd SiGe buffer layer (D3 and D4 samples) will be used. In D3 sample, 330 ℃ low growth temperature of 2nd $Si_{0.05}Ge_{0.95}$ buffer layer which is smoother surface roughness will be prepared to grow 3rd Ge layer. In other side, 370 ℃ high growth temperature of 2nd $Si_{0.05}Ge_{0.95}$ buffer layer which is higher crystal quality will also be prepared to grow 3rd Ge layer. In this high growth temperature sample, the crystal quality is enhanced again by growing thicker 1st and 2nd SiGe buffer layer in D4 sample.

4-4 Effect of growth temperature on 3rd Ge epitaxial layer

In this part, low and high growth temperature (330 and 450 ℃) will be used in grown 3rd Ge epitaxial layer. In Table 4-4, the structure of sample E contains Ge epilayer of 330 ℃ growth temperature grown on low growth temperature

SiGe buffer layers which prefers smoother surface and the structure of sample F contains Ge epilayer of 450 ℃ growth temperature with Ge seed layer (370 ℃) grown on high growth temperature SiGe buffer layers which favors better crystal quality.

In Figure 4-7, AFM topographical images of sample E and F show the RMS roughness of surface will drastically increase when top Ge layers are grown on SiGe buffer layers. Not only high growth temperature of Ge epilayer shows 175.2 nm RMS roughness of surface but also low growth temperature of Ge epilayer shows 45.4 nm RMS roughness of surface. The thickness of Ge top grown layers is about 500nm ～ 700nm and large RMS roughness of surface is observed even in low growth temperature (sample E). Among the methods of Ge grown on Si, compositionally graded buffer (CGB) layers is widely used today and comparison of its RMS roughness of top Ge surface is about 200nm [1]. No matter the high or low growth temperature of Ge grown layer, the rough surface of top Ge epilayer can be noted and it can be solved by chemical mechanical polishing (CMP) [25] which is popular used in graded or step SiGe and Ge layer.

In Figure 4-8, the XRD diffraction curves of 3rd Ge epilayer grown at 330 and 450 ℃ on 1st and 2nd Si_xGe_{1-x} buffer layer shows high growth temperature of Ge grown layer (450 ℃) has a strong and obvious Ge peak compared the low growth temperature of Ge grown layer (330 ℃). The Ge peak of high growth temperature (450 ℃) is separated from Si_xGe_{1-x} buffer layers and has 5650 arcsec from peak of Si substrate. The Ge peak of low growth temperature (sample E) is too low and shows poor Ge crystal quality, so it is hard to separate from Si_xGe_{1-x} buffer layers. The full width at half maximum (FWHM) of the XRD diffraction curves in sample F is 253.7 arcsec. The dislocation density (D)

in the top Ge layer can be estimated from the FWHM of the X-ray Bragg peak by using the equation [26]

$$D = \frac{\Delta\varphi^2}{9b^2} \qquad\qquad (4-2)$$

where b is the length of the Burger vector of the dislocations and $\Delta\varphi$ is the FWHM. Assuming the dislocations contained in Ge layer are the $60°$ dislocations, then the value b = $\sqrt{2}$a, where a is the lattice parameter. From Figure 4-8, $\Delta\varphi$ = 253.7 arcsec can be obtained. With these values, the dislocation density in the Ge epilayer grown on Si substrate is calculated to be D = 1.1×10^8 cm^{-2}.

Figure 4-9 shows the bright-field, cross-sectional TEM and SEM images of the 3rd Ge epitaxial layer grown at 450 ℃. The thickness of Ge epilayer is about 0.7μm and that of Si$_x$Ge$_{1-x}$ buffer layers is 0.6μm. The top Ge epilayer and the Si$_x$Ge$_{1-x}$ buffer layers are clearly shown and the threading dislocations can be blocked at the interface between Ge epilayer and Si$_x$Ge$_{1-x}$ buffer layers. It is proved that dislocations can be effectively blocked by the structure of two-step Si$_x$Ge$_{1-x}$ buffer layers and Ge grown layer of high growth temperature also has the better crystal quality.

4-5 Effect of multi-annealing on 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer

In chapter 4-2, the normal 1st Si$_{0.1}$Ge$_{0.9}$ buffer layers are grown 150 nm thickness and finally 600 ℃ annealing is used on this layers. In this part, effect of multi-annealing treatment on 1st Si$_{0.1}$Ge$_{0.9}$ buffer layers will be discussed. The original 150 nm of 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer is divided in to two stages. At first stage only 50 nm 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer will be grown at 370 ℃ and 600 ℃ annealing is used on this layer. Then keep growing 100 nm 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer at 340 ℃ growth temperature and 600 ℃ annealing is used again on this

layer at second stage. In Table 4-5, the structure of normal 1st $Si_{0.1}Ge_{0.9}$ buffer layer and multi-annealing 1st $Si_{0.1}Ge_{0.9}$ buffer layer will be presented in sample C3 and C4 to compare.

AFM topographical images of sample C3 and C5 show the RMS roughness of surface is 11.4 and 7.2 nm respectively as shown in Figure 4-10(a)(b). In comparison of these samples, the RMS roughness of surface will also decreases with growth temperature decreases but the XRD diffraction curves of low growth temperature (sample C5) shows the same intensity like the curves of high growth temperature (sample C3) as shown in Figure 4-11. It is improve that multi-annealing process could enhance crystal quality for Si_xGe_{1-x} buffer layer of low growth temperature and smooth surface also can be obtained.

Sample	SiH$_4$/GeH$_4$	Temperature(℃)	Si$_x$	Ge$_{1-x}$	Pressure(mtorr)
A	0.24	410	0.055	0.945	20
B	0.32	410	0.085	0.915	20
C	0.4	410	0.1	0.9	20
D	0.2	410	0.05	0.95	20

Table 4-1: The different SiH$_4$/GeH$_4$ flow ratio parameter of sample A, B, C and D

(a)   (b)
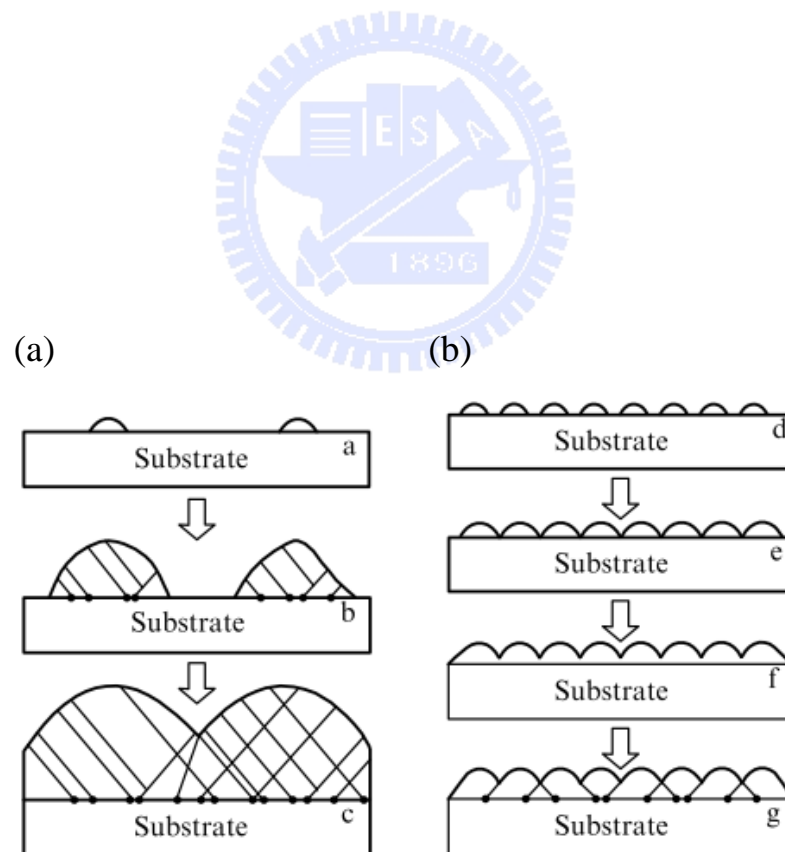
Figure 4-1: (a) high and (b) low growth temperature effect the undulation surface of SK growth mode

Sample	SiH_4/GeH_4	Si_xGe_{1-x} buffer	Temperature($^\circ$C)	Pressure(mtorr)
C1	0.4	1st $Si_{0.1}Ge_{0.9}$	410	20
C2	0.4	1st $Si_{0.1}Ge_{0.9}$	390	20
C3	0.4	1st $Si_{0.1}Ge_{0.9}$	370	20
C4	0.4	1st $Si_{0.1}Ge_{0.9}$	350	20

Table 4-2: The different growth temperature parameter of sample C1, C2, C3 and C4

(a) T = 410 $^\circ$C   (b) T = 390 $^\circ$C

RMS= 45.4 nm   RMS= 18.8 nm

(c) T = 370 ℃   (d) T = 350 ℃
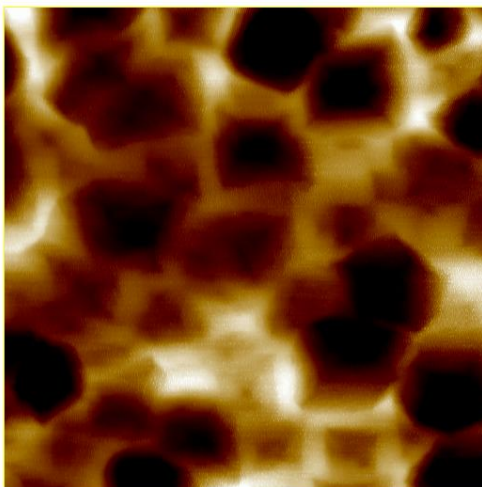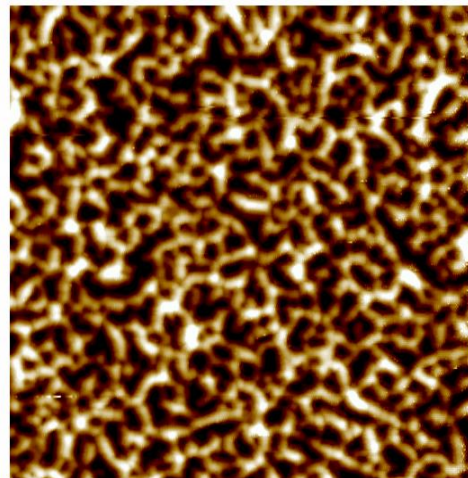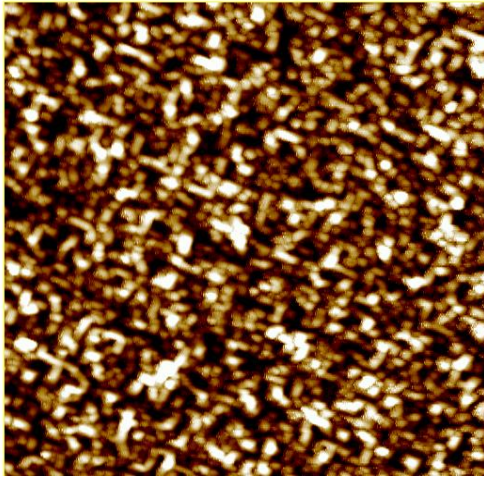
    RMS = 11.8 nm   RMS = 11.5 nm
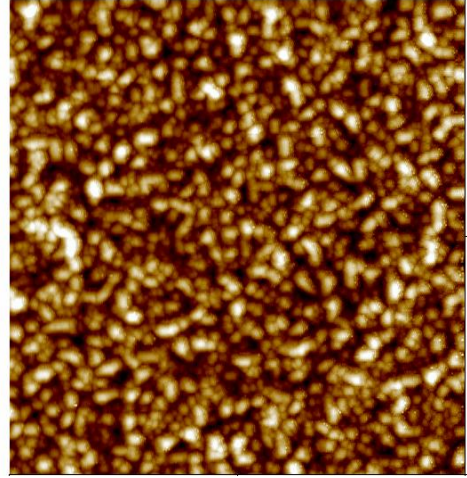
Figure 4-2: AFM images of sample (a) C1,(b) C2,(c) C3 and (d) C4
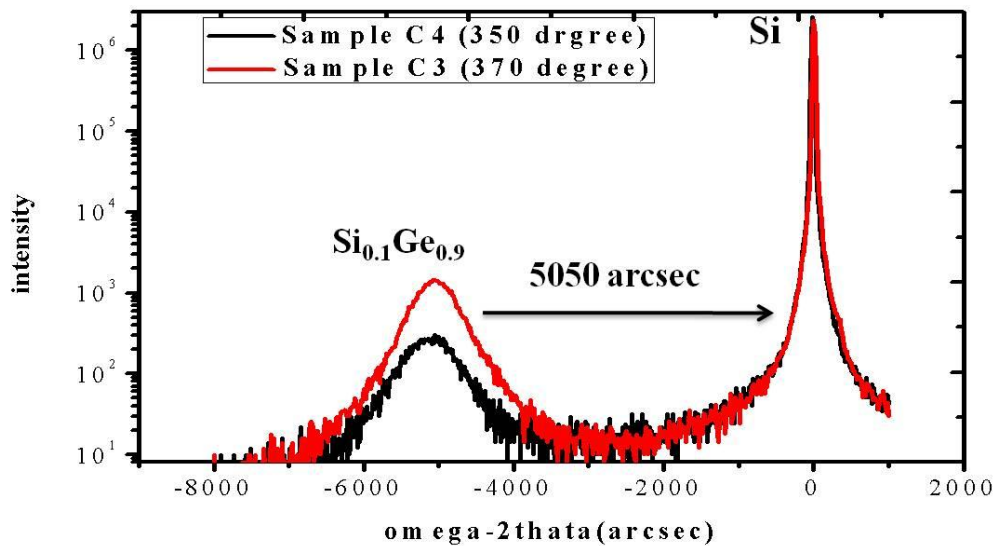
Figure 4-3: XRD diffraction curve of 1st Si$_{0.1}$Ge$_{0.9}$ buffer layer grown at 350 and

370 ℃

(a)
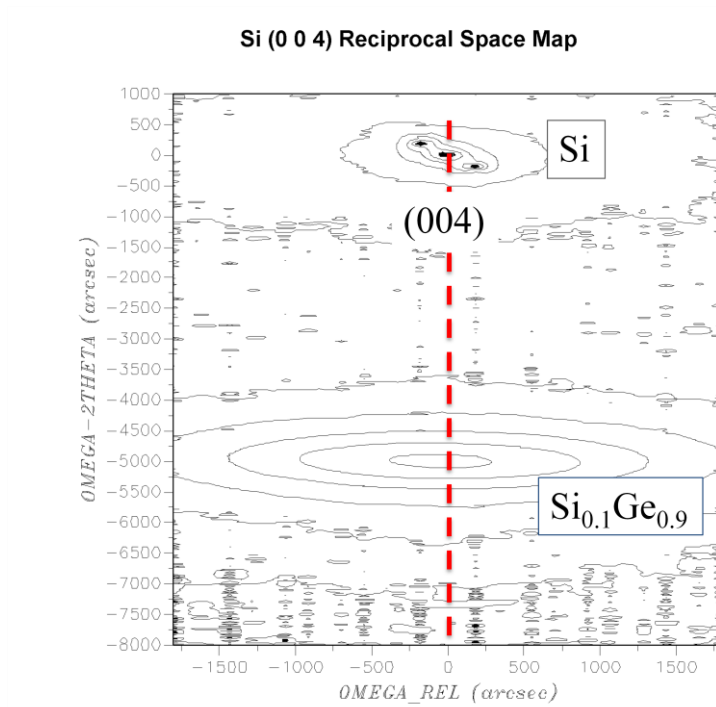
(b)
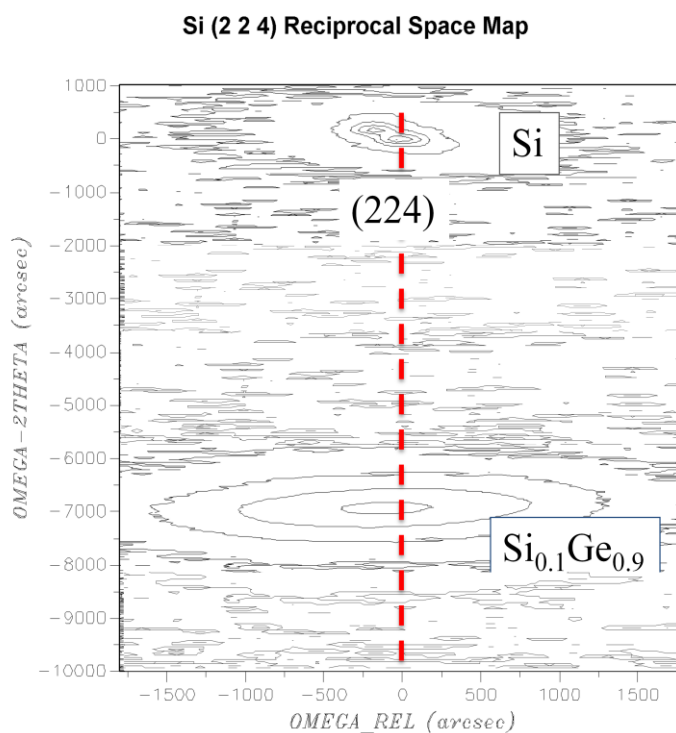
Figure 4-4: (a) Reciprocal space map data of [004] and (b) [224] orientation of 1st $Si_{0.1}Ge_{0.9}$ buffer layer on Si substrate.

Sample	SiH_4/GeH_4	Si_xGe_{1-x} buffer	Temperature($^\circ$C)	Pressure(mtorr)
D1	0.2	2nd $Si_{0.05}Ge_{0.95}$	370	20
D2	0.2	2nd $Si_{0.05}Ge_{0.95}$	350	20
D3	0.2	2nd $Si_{0.05}Ge_{0.95}$	350	20

Table 4-3: The different growth temperature parameter of sample D1, D2 and D3
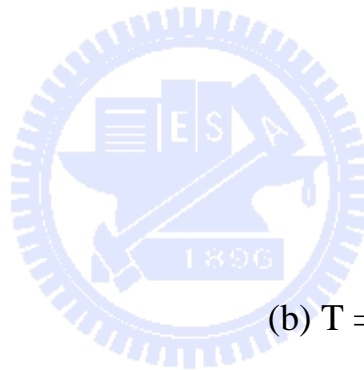
(a) T = 370 $^\circ$C

   RMS = 22.5 nm
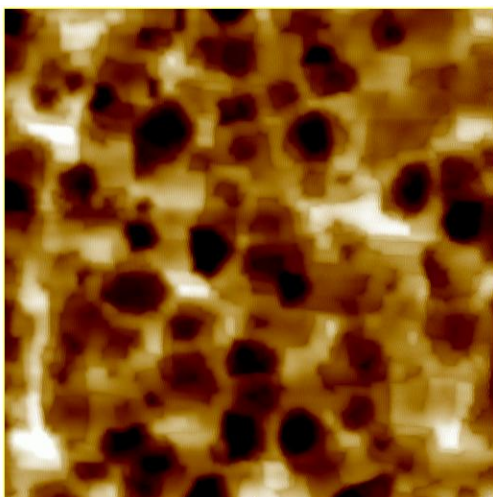
(b) T = 350 $^\circ$C

   RMS = 17.2 nm
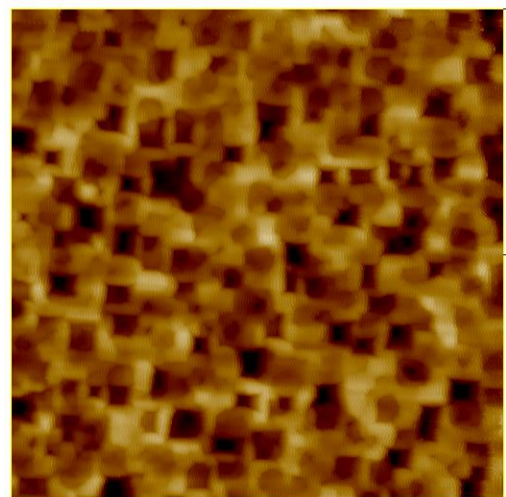
(c)T = 330 °C

RMS = 13.9 nm
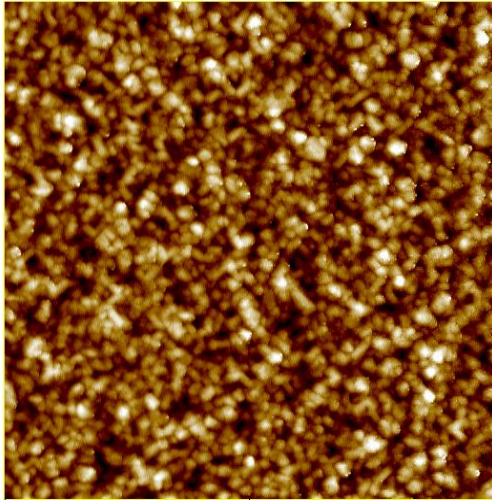
Figure 4-5: AFM images of sample (a) D1,(b) D2 and (c) D3
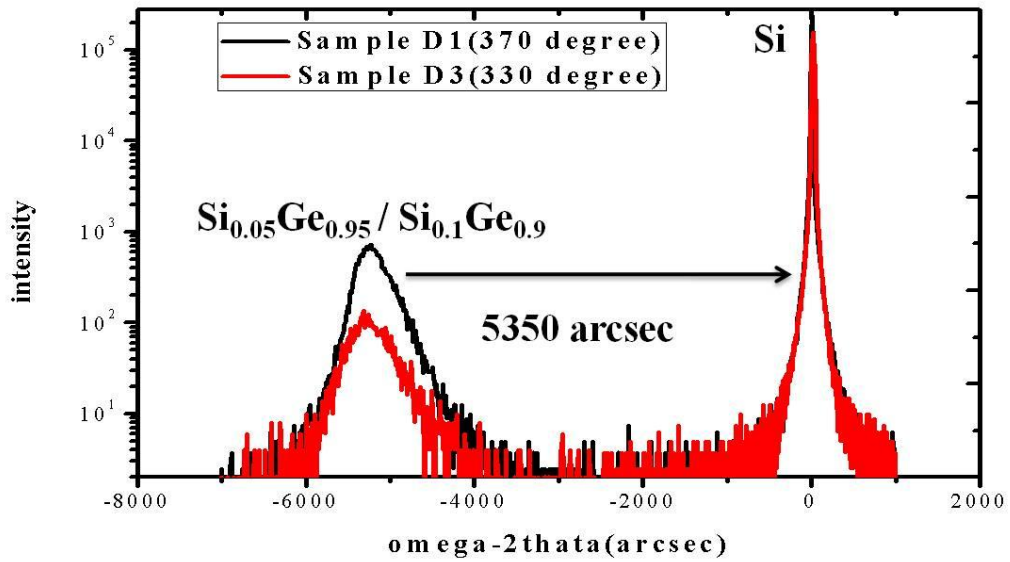
Figure 4-6: XRD diffraction curve of 2nd Si$_{0.05}$Ge$_{0.95}$ buffer layer grown at 330 °C and 370 °C

Sample	Si_xGe_{1-x} buffer	Temperature(℃)	Thickness(nm)
E	Ge	330	500
	2nd SiGe	330	120
	1st SiGe	370	150
F	Ge	450	600
	Ge seed layer	370	80
	2nd SiGe	370	300
	1st SiGe	370	300

Table 4-4: The different growth temperature parameter of sample E and F

(a) T = 330 ℃   (b) T = 450 ℃
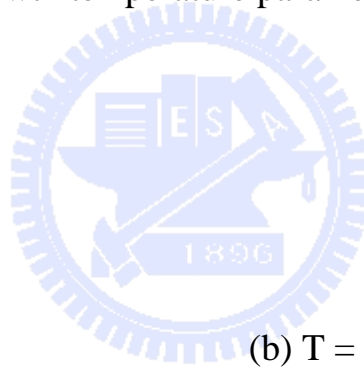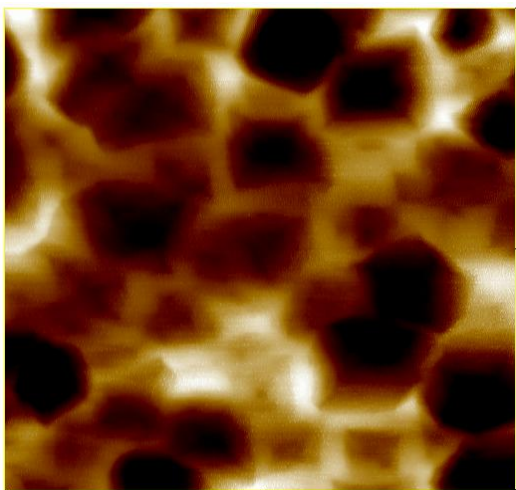
RMS = 45.4 nm   RMS = 175.2 nm
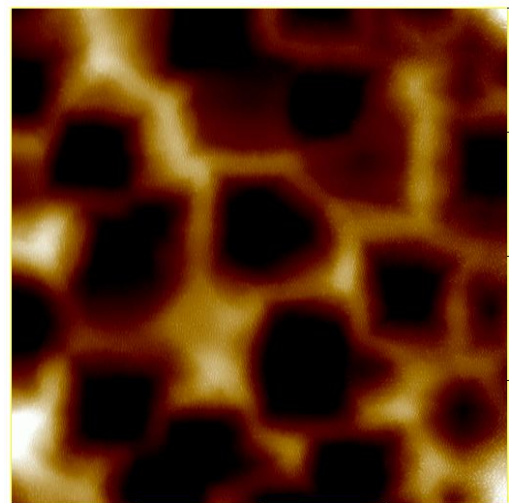
Figure 4-7: AFM images of sample (a) E and (b) F
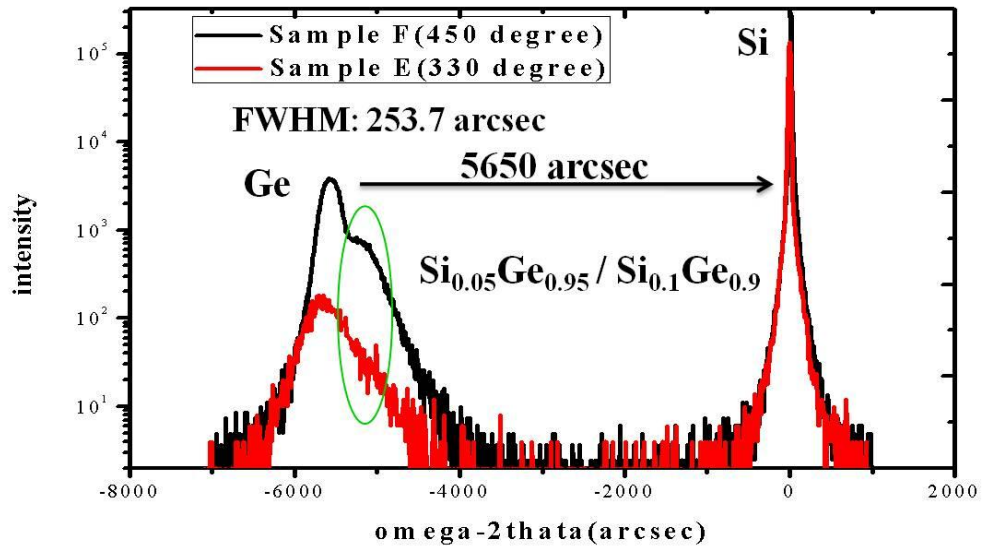
Figure 4-8: XRD diffraction curve of 3rd Ge epitaxial layer grown at 330 ℃ and 450 ℃
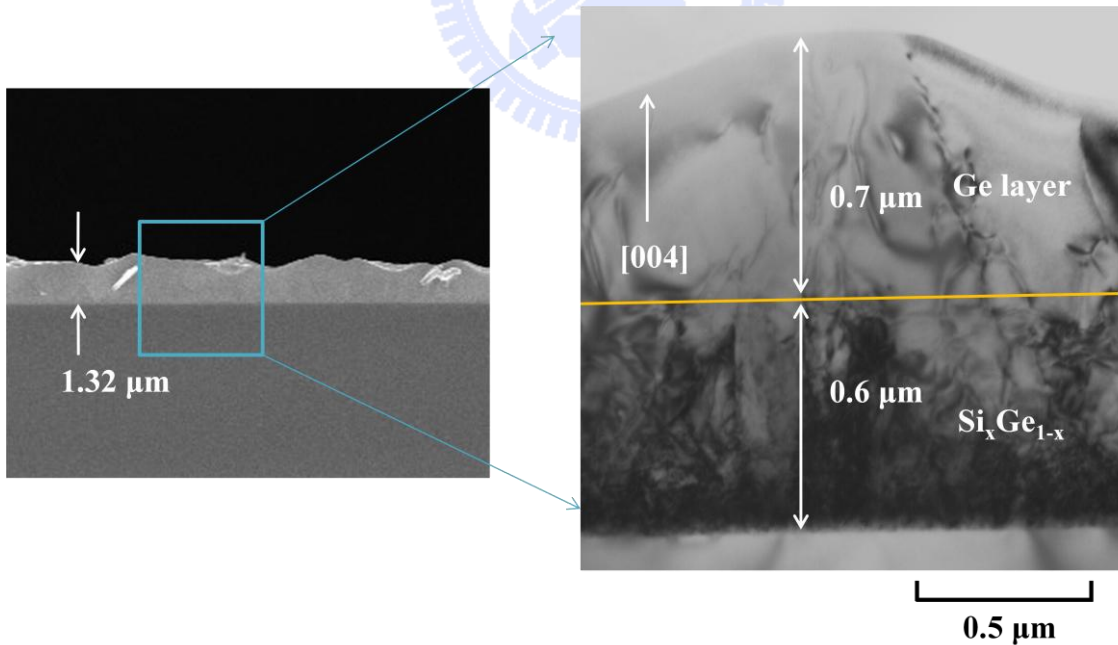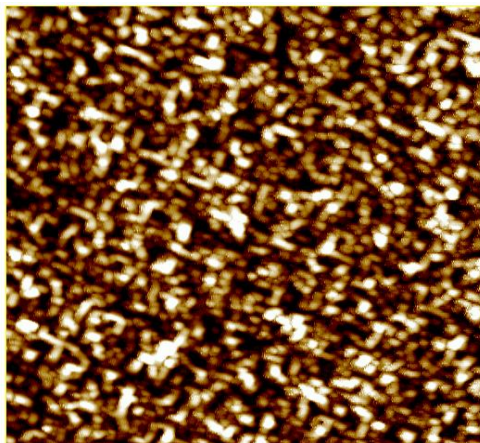

Figure 4-9: SEM and Cross-sectional TEM images of 3rd Ge epitaxial layer grown at 450 ℃

Sample	Stage	Si_xGe_{1-x} buffer	Temperature(℃)	Thickness (nm)
C3	1st	1st $Si_{0.1}Ge_{0.9}$	370	150
	2nd	1st $Si_{0.1}Ge_{0.9}$	340	100
C5	600 ℃ annealing, 10mins			
	1st	1st $Si_{0.1}Ge_{0.9}$	370	50

Table 4-5: The different growth temperature parameter of sample C3 and C5

(a) Normal $Si_{0.1}Ge_{0.9}$ buffer layer   (b) Multi-annealing $Si_{0.1}Ge_{0.9}$ buffer layer

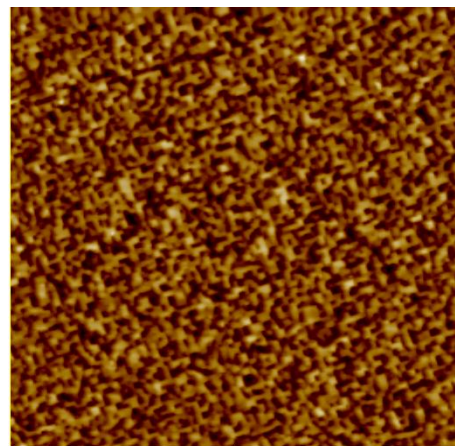   RMS = 11.8 nm   RMS = 7.2 nm
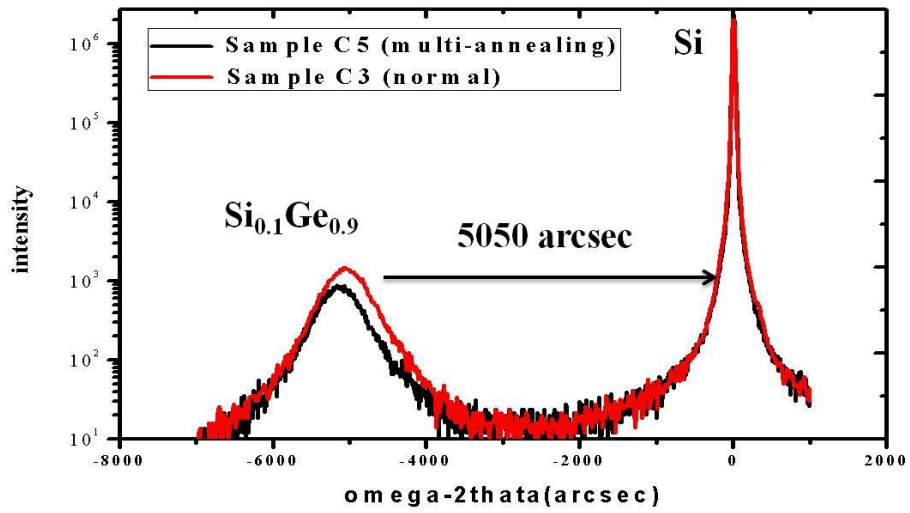

Figure 4-10: AFM images of sample (a) C3 and (b) C5

Figure 4-11: XRD diffraction curve of 1st $Si_{0.1}Ge_{0.9}$ buffer layer grown with and without multi-annealing

Chapter 5
Conclusions

In this thesis, two-step Si_xGe_{1-x} buffer layers for the growth of a high quality Ge epitaxial layer on Si substrate have been researched. In order to suppress the undulation surface of Si_xGe_{1-x} buffer layers which is introduced by large lattice mismatch with Si substrate , low growth temperatures (< 370 ℃) are used to grow 1st $Si_{0.1}Ge_{0.9}$ buffer layer and 2nd $Si_{0.05}Ge_{0.95}$ buffer layer. The low growth temperature of Si_xGe_{1-x} buffer layers (1st 370 ℃ / 2nd 330 ℃) show the smoother surface but poor crystal quality. On the other hand, the high growth temperature of Si_xGe_{1-x} buffer layers (1st 370 ℃ / 2nd 370 ℃) show better crystal quality but the RMS of surface roughness increases to 22.5 nm. Finally, low growth temperature (330 ℃) of Ge grown on low growth temperature of Si_xGe_{1-x} buffer layers compares with high growth temperature (450 ℃) of Ge grown on high growth temperature of Si_xGe_{1-x} buffer layers. The result of high growth temperature of Ge epilayer shows a strong and obvious Ge peak (FWHM: 253.7 arcsec) compared the low growth temperature of Ge grown layer. The surface of Ge grown layer becomes rough in both high and low growth temperature and it can be solved by chemical mechanical polishing (CMP) which is generally used.

Beside, crystal quality of lower growth temperature (340 ℃) in 1st $Si_{0.1}Ge_{0.9}$ buffer layer can be enhanced by multi-annealing process and smoother surface can be obtained (RMS: 7.2 nm) at this growth temperature. It is proved that poor crystal quality can effectively be solved by multi-annealing process.

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