The Analysis and Design of CMOS Multidrain Logic and Stacked Multidrain Logic

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Abstract—A new CMOS logic called the CMOS multidrain logic (MDL) is analyzed and investigated. Its basic structure consists of one MOS current injector which is connected to the input node, and one multidrain MOS driver with its drains as outputs and its gate as input. There are four available configurations in the static CMOS MDL. Each configuration can conveniently form a WIRE-AND or WIRE-OR function by tying the output drain nodes together. Both multidrain and wire-logic capabilities lead to a smaller average area per gate than that of the conventional CMOS logic. From transient analysis results, it is seen that the speed of the static CMOS MDL is comparable to that of I^2L or even ECL and is about 20–70 percent better than that of the conventional CMOS logic, whereas the power–delay product is smaller than that of I^2L and ECL and is nearly the same as CMOS under 300-MHz operation. Therefore, by using the static CMOS MDL, the speed performance can be promoted without any degradation in power–delay product or packing density. In dynamic circuits, a new structure called the dynamic CMOS stacked MDL (SMDL) is formed by stacking the MDL circuits. Due to the inherent multidrain connections, various Boolean terms are realizable within a highly merged dynamic SMDL gate. Therefore the dynamic CMOS SMDL has the features of high packing density and low interconnection complexity which make it a potential technique in CMOS VLSI design.

NOMENCLATURE

$C_{on(p)}$	Gate oxide capacitance per unit area of an NMOS (PMOS).
C_L	Fixed capacitive load at the output of a logic gate.
$I_{dn(p)}$	Drain current of an NMOS (PMOS).
I_{on}	DC current when the output of a CMOS PN MDL inverter is in the logic ZERO state.
$L_{(\text{mask})}$	Effective (mask) channel length.
$T_{PHL(LH)}$	Delay time of a fall (rise) waveform.
$V_{Tn(p)}$	Zero-bias threshold voltage of an NMOS (PMOS).
W	Effective channel width.
$\mu_{n(p)}$	Surface mobility of an NMOS (PMOS) device.

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I. INTRODUCTION

THE advantageous features of low dc power, high noise immunity, and high circuit design versatility have made CMOS a dominant VLSI technology over NMOS. However, the circuit speed of CMOS, although comparable to that of NMOS [1], is lower than that of bipolar [2]. Meanwhile, the chip area of static CMOS logic gates like AND-OR-INV (AOI) or OR-AND-INV (OAI) is rather large so that the circuit density of CMOS IC's is considerably degraded. To improve both speed and density, two effective approaches have been adopted. One is to develop advanced technologies with scaled-down feature size [1], [3]–[6]. The other is to develop new logic circuits [7]–[11].

The second approach is valuable and attractive for the following reasons.

1) In a complex VLSI chip, different parts of circuits may have distinct needs. For example, the arithmetic section or the control section needs accurate timing and tight signal delay whereas the register section needs high packing density because of complex circuitry. It is beneficial, therefore, to use different types of logic circuits to achieve various performance requirements. Such a design methodology has been used in the design of CMOS VLSI memory management chip [12], bipolar digital telecommunication IC [13], CMOS DRAM design (e.g., [14]), and CMOS SRAM design (e.g., [15]).

2) By using the new logic circuits, circuit power may be sacrificed to obtain higher speed performance and/or higher circuit density. Thus the application fields of CMOS can be extended to those of bipolar.

Recently, three CMOS dynamic logic circuits [7]–[10] and two CMOS static logic circuits [10], [11] have been proposed and shown to be able to improve speed performance and circuit density. In addition, two NMOS static logic circuits were also proposed and analyzed [16], [17].

In this study, a new CMOS logic circuit called the CMOS multidrain logic (MDL) is proposed, analyzed, and experimentally observed. The basic circuit structure, which is derived from I^2L, consists of an enhancement-mode MOSFET as a current injector and a multidrain MOSFET with drain terminals as output nodes and the gate terminal as input node. As compared with the multidrain NMOS logic [16], the difference is that an enhancement MOS

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instead of a depletion NMOS is used as a current injector. Since the enhancement MOS current injector has a higher charging efficiency [11], the switching speed of CMOS MDL is higher than that of multidrain NMOS logic. Moreover, because both PMOS and NMOS are available in CMOS, the static CMOS MDL has four different configurations and the dynamic CMOS MDL is also available. Thus the logic design flexibility of CMOS MDL is higher than that of multidrain NMOS logic.

For static CMOS MDL gates, the signal delay is 60–85 percent smaller than that of CMOS logic, even in cases of device or power supply scaled down. The packing density is also higher. Although the static power of CMOS MDL is larger, the overall power–speed performance is quite comparable to that of the conventional CMOS [1], I^2L [6], and ECL [6]. Therefore a good compromise among power, speed, and density can be achieved.

The static power dissipation can be greatly reduced in dynamic CMOS MDL circuits. Two configurations are suitable to form the dynamic logic without any internal signal glitches. The resultant dynamic circuits are similar to NORA-CMOS [8] except that the dynamic CMOS MDL has the multidrain structure. Such a new circuit structure is called the dynamic stacked MDL (SMDL) circuit. Through the use of the SMDL, various Boolean terms can be implemented and efficiently merged into one single gate structure. This drastically reduces interconnection complexity and increases packing density especially in a multiple-output or multiple-function IC. The improvement becomes more significant when the circuit complexity is increased.

In the following sections, basic analyses on CMOS MDL circuits are performed. Then the performance comparisons of the static CMOS MDL to other logic are presented and the advantageous features of the dynamic CMOS MDL are discussed. Finally, experimental results are described to verify part of the theoretical predictions.

II. Basic Analysis

Four different configurations of CMOS MDL inverters are shown in Fig. 1(a)–(d) where the names PN, NN, PP, and NP MDL are given to the corresponding configurations, respectively. As an illustrative example, only the PN MDL is analyzed in detail. Other configurations can be analyzed by using the same method.

In the PN MDL shown in Fig. 2, the transistor M_N is a multidrain NMOS with its drain terminals connected as output nodes and its gate as the input node. The transistor M_P is a PMOS which serves as a pull-up current source for the input node of transistor M_N and the output node of transistor M_{NP}. Since the gate of transistor M_P is grounded and the substrate is connected to the source, the available charging current is large without any degradation due to body effect.

If the NMOS M_{NP} in the preceding stage is OFF, V_{in} is pulled up by the PMOS M_P and the NMOS M_N is turned on. Thus the output voltage V_o is pulled down. On the other hand, if the NMOS M_{NP} is ON, V_{in} is pulled down. This turns off the NMOS M_N and V_o is pulled up by the PMOS M_{PL} in the load stage. This is the inverter operation.

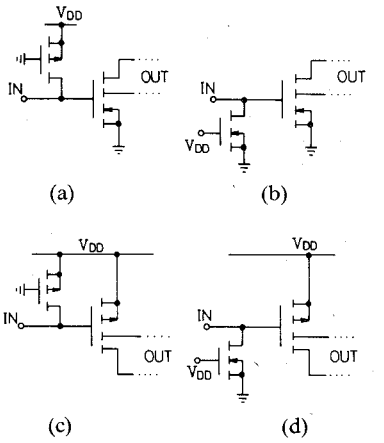


Fig. 1. Four different configurations of the static CMOS MDL inverters. (a) PN MDL. (b) NN MDL. (c) PP MDL. (d) NP MDL.

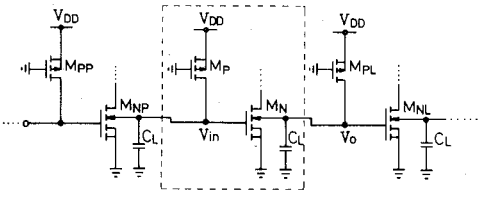


Fig. 2. The basic structure of CMOS PN MDL inverters.

Typical transfer characteristics of the CMOS MDL are shown in Fig. 3 for different values of $R' \equiv (W/L_{\text{mask}})_N/(W/L_{\text{mask}})P$. According to different operating regions of the MOSFET's M_N and M_{PL}, the whole characteristic can be divided into four regions and can be approximately modeled by using the first-order current equations. The detailed calculation is described in the Appendix. The voltages V_H and V_L in the logic ONE and ZERO states, respectively, can be written as

$$V_H = V_{DD} \tag{1}$$

$$V_L = \Big\{ R(V_{DD} - V_{Tn}) - |V_{Tp}| - \Big[\big(RV_{DD} - RV_{Tn} - |V_{Tp}|\big)^2 - (R-1)\big(V_{DD}^2 - 2V_{DD}|V_{Tp}|\big) \Big]^{1/2} \Big\} / (R-1), \quad \text{for } V_L > |V_{Tp}| \tag{2a}$$

$$= V_{DD} - V_{Tn} - \Big[(V_{DD} - V_{Tn})^2 - (V_{DD} - |V_{Tp}|)^2 / R \Big]^{1/2}, \quad \text{for } V_L < |V_{Tp}| \tag{2b}$$

where $R \equiv \mu_n (W/L)_N C_{on} / [\mu_p (W/L)_p C_{op}]$. Generally, the value of R must be designed such that V_L is smaller than V_{Tn}. In this case, the NMOS in the next stage can be turned off when $V_o = V_L$. According to this design rule, the

TABLE I
SIMULATED DC CHARACTERISTICS OF CMOS PN MDL INVERTERS

$(W_{mask}/L_{mask})_N$ ($\mu m/\mu m$)	$(W_{mask}/L_{mask})_P$ ($\mu m/\mu m$)	R'	R	V_H (V)	V_L (V)	I_{on} (μA)	V_{iul} (V)	V_{iuh} (V)	V_{oul} (V)	V_{ouh} (V)	VNM_1 (V)	VNM_0 (V)
$\frac{7.0}{3.5}$	$\frac{7.0}{3.5}$	1	3.04	5.00	0.61	190.60	1.95	3.50	1.10	4.35	1.50	1.34
$\frac{30}{3.5}$	$\frac{30}{3.5}$	1	3.04	5.00	0.60	817.30	1.90	3.50	1.10	4.35	1.50	1.30
$\frac{70}{3.5}$	$\frac{70}{3.5}$	1	3.04	5.00	0.60	1907.00	1.70	3.40	1.20	4.50	1.60	1.10
$\frac{14}{3.5}$	$\frac{7.0}{3.5}$	2	6.08	5.00	0.29	194.20	1.30	2.60	0.85	4.65	2.40	1.01
$\frac{14}{3.5}$	$\frac{3.5}{3.5}$	4	12.15	5.00	0.14	97.92	1.00	2.10	0.50	4.80	2.90	0.86
$\frac{5.0}{2.5}$	$\frac{2.5}{2.5}$	2	6.08	5.00	0.30	110.60	1.20	2.60	0.80	4.70	2.40	0.90
$\frac{10.0}{2.5}$	$\frac{2.5}{2.5}$	4	12.15	5.00	0.15	112.40	0.90	2.00	0.55	4.80	3.00	0.75

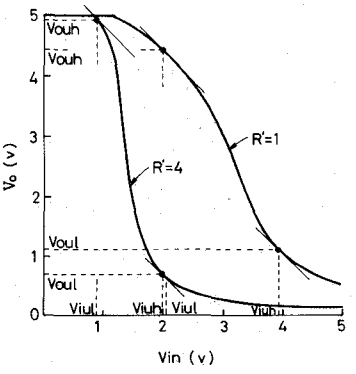


Fig. 3. Transfer characteristics of PN MDL inverters with different values of R'.

minimum required $R_{\min}$ is approximately determined by

$$R_{\min} = \Big\{ -\big(V_{DD}^2/2 - 2V_{Tn}^2 + V_{DD}V_{Tn} - V_{DD}|V_{Tp}| + V_{Tn}|V_{Tp}|\big) + \Big[\big(V_{DD}^2/2 - 2V_{Tn}^2 + V_{DD}V_{Tn} - V_{DD}|V_{Tp}| + V_{Tn}|V_{Tp}|\big)^2 - V_{Tn}(2V_{DD} - 3V_{Tn})\big(V_{DD}^2 - V_{Tn}^2 + 2V_{Tn}|V_{Tp}| - 2V_{DD}|V_{Tp}|\big)\Big]^{1/2} \Big\} / \big[V_{Tn}(2V_{DD} - 3V_{Tn})\big], \quad \text{for } V_{Tn} > |V_{Tp}| \tag{3a}$$

$$R_{\min} = \big(V_{DD} - |V_{Tp}|\big)^2 / \big[V_{Tn}(2V_{DD} - 3V_{Tn})\big], \quad \text{for } V_{Tn} \leq |V_{Tp}|. \tag{3b}$$

As may be calculated from (3), the corresponding value of the geometric ratio R' is about 0.9 for a typical CMOS process.

The voltages V_{iul}, V_{iuh}, V_{oul}, and V_{ouh} at unity-gain points indicated in Fig. 3 can be characterized by finding the slope of the transfer characteristic. Detailed calculations are given in the Appendix. From (10) and (12), the voltage noise margin VNM at logic ONE and ZERO can be expressed as

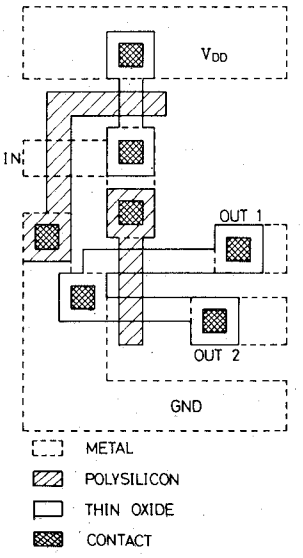
$$VNM_0 \equiv V_{iul} - V_L = V_{Tn} + \big(V_{DD} - |V_{Tp}|\big) / \big(R^2 + R\big)^{1/2} - V_L \tag{4}$$

$$VNM_1 \equiv V_H - V_{iuh} = V_{DD} - V_{Tn} - |V_{Tp}|/R - (2R - 1) \cdot \big(V_{DD}^2 - 2V_{DD}|V_{Tp}|\big)^{1/2} / \big[R(3R - 1)^{1/2}\big]. \tag{5}$$

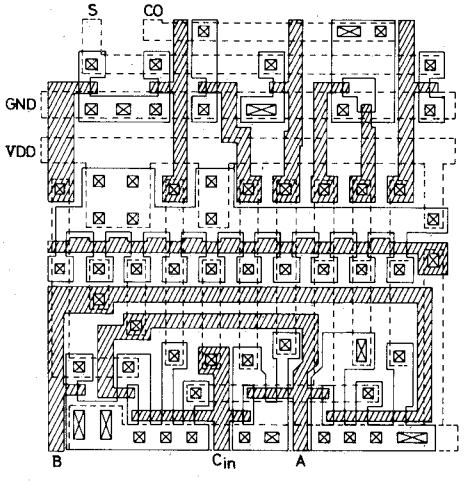
Note that the MDL circuits are ratioed. Hence, the noise margin is not as good as that of the conventional CMOS logic. Its value depends on the ratio R and the voltage V_L in the logic ZERO state.

Table I lists the SPICE simulated dc characteristics of CMOS PN MDL inverters with different R'. For $R' = 1$, $V_L < V_{Tn}$ and $VNM_0 \simeq VNM_1$. This means the logic state is stable and the transfer curve is nearly symmetric when $R' = 1$. As compared with SPICE simulations, hand calculations using the above derived equations have an error less than 20 percent if the mobility degradation is considered. Thus these equations can be used as good design guidelines.

As to the connections among the four MDL configurations, the output node from an NMOS (PMOS) driver cannot be connected to the input node with an NMOS (PMOS) current injector because there will be no charging (discharging) path to the node. The PN MDL therefore cannot be connected to the NP MDL and so on. For those nodes where an NMOS driver and a PMOS current injector are connected together, the ratio R' may be as small as 1 according to (3). On the other hand the ratio R' must be about 0.1 to obtain an output voltage higher than $V_{DD} - |V_{Tp}|$ at the node where an NMOS current injector and a PMOS driver are connected. This leads to a larger PMOS channel width and thus a larger total chip area in both NP and PP configurations.



(a)



(b)

Fig. 4. Typical layout of (a) a two-output MDL inverter, and (b) a static MDL full adder.

III. Performance Evaluation for Static MDL

A. Logic Function and Chip Area

A typical layout diagram of a PN MDL inverter with two drain nodes is shown in Fig. 4(a) where the separation region between two drains is the field oxide region. Although a multidrain transistor is formed by connecting the sources of several MOSFET's together, it is not too area consuming due to the compactly merged structure. Moreover, it can be conveniently implemented in gate-array design. Generally, the chip area A_{rea} of a multidrain PN MDL is empirically determined by

$$A_{rea} = (1+0.38N)F^2 \tag{6}$$

where N is the fan-out (drain) number and F is the minimum feature size. Based on 2-μm CMOS rules, the layout of a static PN MDL full adder is drawn in Fig. 4(b)

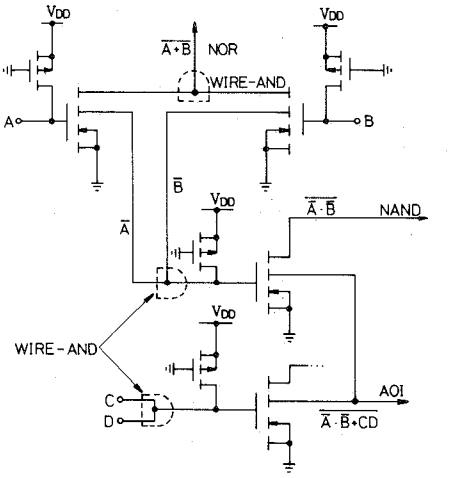


Fig. 5. Circuit structures of CMOS PN MDL NOR, NAND, and AOI gates.

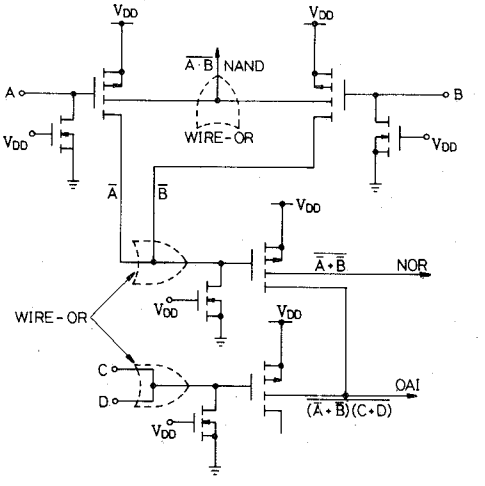


Fig. 6. Circuit structures of CMOS NP MDL NOR, NAND, and OAI gates.

where four-drain MOSFET's are used for inputs A, B, and C_{in}.

Since the WIRE-AND or DOT-AND function can be implemented by tying the output nodes together, complex logic functions can be realized by PN MDL as shown in Fig. 5 where NAND, NOR, and AOI circuits are drawn. Due to the multidrain structure, all the WIRE-AND functions can be efficiently formed without any interference among them. Similarly, the NP MDL can be used to implement NAND, NOR, and OAI gates, as illustrated in Fig. 6, through the WIRE-OR connections.

Without the multidrain structure, the transistors M_N and M_{PL} in Fig. 2 form a NMOS-like or pseudo-NMOS inverter. Similarly, the PN MDL NOR gate in Fig. 5 is the same as a NMOS-like NOR gate. However, due to the inherent multidrain and WIRE-AND capability, the MDL in general is different from the NMOS-like logic, and complex gates like NAND and AOI can be more efficiently realized with higher density and speed in PN MDL than in NMOS-like logic. Similar features exist between NP MDL and PMOS-like logic. In the following analysis, comparisons among these logic circuits will be given.

TABLE II
NORMALIZED CHIP AREAS OF VARIOUS LOGIC GATES REALIZED BY CMOS, MDL, NMOS-LIKE AND PMOS-LIKE LOGIC

GATES / NORMALIZED AREA / LOGIC	INV.	2-INPUT NAND	2-INPUT NOR	2-INPUT XOR	$\overline{AB+CD}$ AOI	$\overline{(A+B)(C+D)}$ OAI
CMOS	1	1	1	1	1	1
PN MDL	1.42	0.62	0.84	0.57	0.49	0.81
NP MDL	1.85	1.21	0.73	0.91	2.80	0.52
NMOS-LIKE	1.42	0.85	0.84	0.60	0.63	0.69
PMOS-LIKE	1.85	1.21	1.14	0.96	1.30	1.13

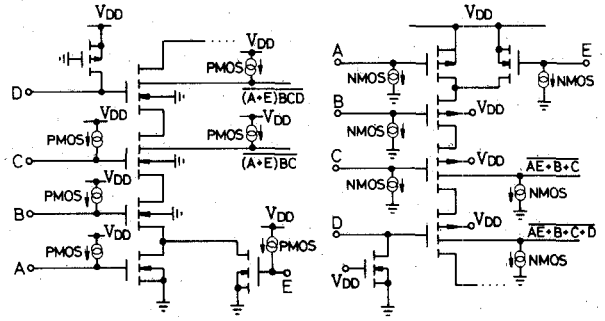


Fig. 7. Circuit structures of a static CMOS: (a) PN, and (b) NP stacked MDL.

Based upon the same design rule, the layouts of various gates implemented by CMOS, PN MDL, NP MDL, NMOS-like and PMOS-like logic were generated. Their chip areas are compared in Table II where the area of each standard CMOS gate is normalized to unity. From this table it is seen that NAND and AOI gates can be efficiently implemented by PN MDL with less chip area and NOR and OAI gates by NP MDL.

Since the voltage levels of MDL are compatible with those of CMOS, a MDL gate without current injector can be driven directly by a CMOS gate. Similarly, by adding a current injector to the output node, a MDL gate can directly drive a CMOS gate. In these cases, no interfacial buffer is needed. However, a PP or NN MDL gate is needed between PN MDL and NP MDL gates.

Both PN MDL and NP MDL can be stacked to form NAND and NOR gates, respectively, as shown in Fig. 7. To keep the same ON resistance, the channel width of each stacked MOS must be enlarged. Due to the multidrain capability of the SMDL, the output can be taken from the drain of the intermediate MOS to form another logic function. As may be seen from the illustrative circuits shown in Fig. 7, two functions can be formed in "one" gate structure. By using such highly merged structures, the interconnection complexity can be reduced and the packing density can be drastically increased. These lead to reductions in both interconnection delay and chip area, respectively. Such advantageous features are more significant in dynamic circuits, as will be seen later.

As compared to NMOS-like or PMOS-like logic, SMDL generally has higher design versatility as well as the above mentioned advantages, all due to its inherent multidrain capability.

TABLE III
NORMALIZED AVERAGE DELAY TIMES OF CMOS AND PN MDL INVERTERS UNDER DIFFERENT CONDITIONS

CONDITIONS / NORMALIZED DELAY / LOGIC	VDD = 5V C_L = 0PF L_{mask} = 3.5μm	VDD = 5V C_L=0.5PF L_{mask} = 3.5μm	VDD = 5V C_L= 2PF L_{mask} = 3.5μm	VDD = 3V C_L = 0PF L_{mask} = 3.5μm	VDD = 5V C_L = 0PF L_{mask} = 2.5μm	VDD = 5V C_L = 0PF L_{mask} = 2 μm
CMOS	1	1	1	1	1	1
PN MDL	0.63	0.82	0.83	0.56	0.83	0.59

B. Speed and Power

Since the characteristic waveform is the actual internal voltage waveform within an IC chip, it is better to evaluate the speed performance of various logic gates by characteristic waveform timing. To obtain the characteristic waveforms and their signal timing, a string of identical gates is excited and the output nodes of the intermediate stages are observed. In the following comparisons, the average delay time of a gate is defined as half of the pair delay in the characteristic waveform case.

The average delay times of various PN MDL inverters with different geometric ratio R' were simulated by using the conventional CMOS device parameters. It is found that for the same current injector, the inverters with $R'=1$ have smaller delay than those with $R'>1$, because of the smaller size of the NMOS which leads to a smaller load capacitance. In the following comparisons, only $R'=1$ is considered.

By using the same p-well CMOS device parameters, the SPICE simulated average delay times of PN MDL and standard CMOS inverters with different capacitive loads, power supply voltages, and channel lengths are compared in Table III where all the delay times are normalized. In this comparison, the CMOS inverters are optimally designed such that the rise time is nearly equal to the fall time and the delay time is minimum. Furthermore, the total channel area of the PN MDL inverter is set to be equal to that of the CMOS inverter. In this case, the delay time of the PN MDL inverter is found to be 0.56–0.83 times as small as that of the CMOS inverter, even when the capacitive load is large, the channel length is scaled down to 2 μm, or the power supply is scaled down to 3 V. If the n-well or double-well CMOS technology is adopted, the delay time of the PN MDL inverter is expected to be smaller because the p-n junction capacitance is decreased.

The simulated average delay times of inverters and three-input NOR gates implemented by CMOS, PN MDL, NP MDL, enhancement/depletion NMOS, NMOS-, and PMOS-like logic are compared in Table IV where the 3.5-μm device parameters are used. It is seen that even for complex gates, the PN MDL is still faster than other logic families, especially the CMOS logic. For the NP MDL, the speed is two times as slow as that of the PN MDL because of the large size of the PMOS driver.

To investigate the speed change due to the multidrain structure and the WIRE-AND connections, the average delay times of PN MDL inverters as a function of the number of drain nodes N and the number of WIRE-AND

TABLE IV
NORMALIZED AVERAGE DELAY TIMES OF INVERTERS AND THREE-INPUT NOR GATES REALIZED BY CMOS, MDL, E/D NMOS, NMOS- AND PMOS-LIKE LOGIC

LOGIC / NORMALIZED DELAY / GATES	CMOS	PN MDL	NP MDL	E/D NMOS	NMOS -LIKE	PMOS -LIKE
INVERTER	1.59	1	2.56	1.40	1.00	2.56
3-INPUT NOR	3.47	1	2.05	1.35	0.97	7.86
3-INPUT NAND	2.44	1	2.05	1.43	2.35	2.04

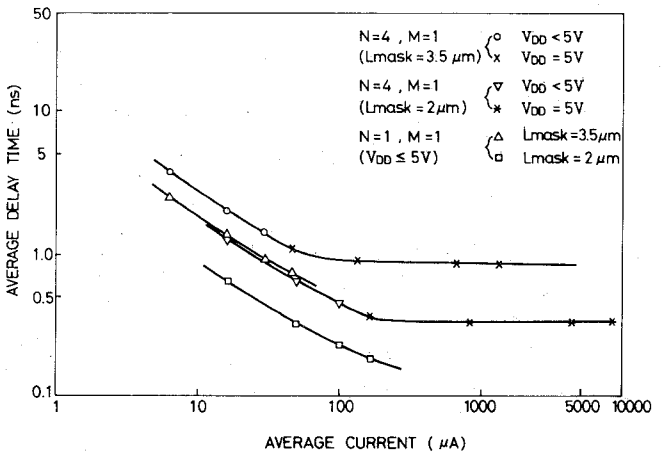


Fig. 8. The average delay times as a function of the average injector current for MDL inverters with different channel lengths and power supplies.

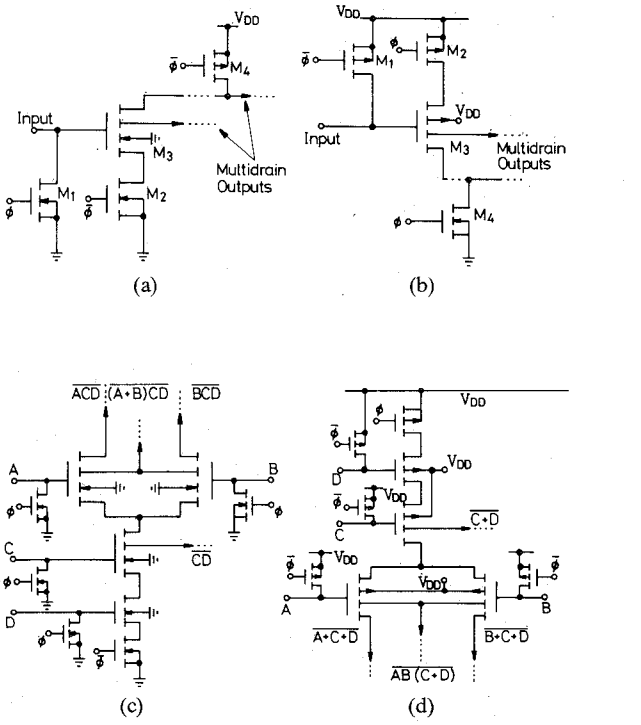


Fig. 9. Circuit structures of (a) a dynamic NN MDL inverter, (b) a dynamic PP MDL inverter, (c) a dynamic SMDL gate based on the NN configuration, and (d) a dynamic SMDL gate based on the PP configuration.

inputs M were found by simulation. The normalized average delay times are

$$\tau_N = 1 + 0.23\,N$$
$$\tau_M = 1 + 0.57\,M.$$

Note that the increase in the delay time due to an extra output drain node is very small.

The average delay time of PN MDL inverters with $N = 4$ as a function of the average injector current is shown in Fig. 8 where the average current is equal to half of the maximum injector current in the logic ZERO state because no current flows in the logic ONE state. Also shown in Fig. 8 is the average time of PN MDL inverters with $N = 1$, $R' = 1$, and scaled-down power supply. From this figure it is seen that the speed of MDL is quite comparable with that of I^2L [2] or even ECL [6]. Moreover, the minimum power–delay product of the MDL is in the range of 0.02–0.1 pJ for 2-μm CMOS process. This value is smaller than the typical values of 0.5–1.8 pJ in ECL [6] and 0.02–0.6 pJ in I^2L [6] and is nearly the same as that of 1-μm standard CMOS logic [1] under 300-MHz operations. However, unlike the standard CMOS logic, the CMOS MDL has dc power dissipation.

From the above analysis, it is realized that the incorporation of MDL in a CMOS chip can promote the speed performance to the bipolar level while keeping the same power–delay product and the same process complexity of CMOS. It is expected, therefore, that the application field of CMOS can be extended to that of bipolar.

IV. DYNAMIC MDL AND SMDL

The NN and PP MDL configurations can be used to construct the dynamic circuits to reduce the dc power dissipation. The basic dynamic MDL structures are drawn in Fig. 9(a) and (b) where $\phi = 1$ is the precharging phase and $\phi = 0$ is the evaluation phase. The precharging device M_4 is used to pull up or pull down the output voltage. It also serves as the input precharging device of the next stage. Similarly, the MOS M_1 is the input precharging device of this stage and is the output precharging device of the preceding stage. In the circuit of Fig. 9(b), the geometric ratio R' of the PMOS M_3 to the NMOS M_4 may be unity.

The SMDL structures of Fig. 7 can also be converted into dynamic circuits as shown in Fig. 9(c) and (d). In this diagram, the output precharging devices are not shown. According to the analysis in Section II, these dynamic NN and PP configurations in Fig. 9 must be alternatively connected. Therefore both dynamic MDL and dynamic SMDL circuits have no internal race (glitch) problems, like the DOMINO [7] or the NORA-CMOS [8] techniques. Basically, the dynamic MDL and SMDL circuits are similar in structure to the other two dynamic circuits except that the dynamic MDL and SMDL have multidrain capability. Due to such inherent multidrain connections, many Boolean terms among various logic functions can be realized and merged together in a dynamic SMDL gate as shown in Fig. 9(c) and (d). In these illustrative circuits, three extra Boolean terms can be implemented by adding three extra drain nodes to the original dynamic AOI/OAI

TABLE V
SPEED COMPARISONS BETWEEN THE DYNAMIC SMDL GATES AND THE CONVENTIONAL DYNAMIC GATES

CIRCUITS / CHARACTERISTICS					
OUTPUT	A	A	A	B	B
TOTAL CHANNEL AREA	×16	×16	×15.5	×9.5	×9
T_{PHL} (ns)	1.140	1.164	1.097	0.911	0.893

gates and suitably enlarging the channel widths of the related MOS's. There is no need to separately construct three extra gates. Therefore the interconnection complexity for input signals is reduced. Meanwhile, the packing density is improved due to the highly merged structure.

To investigate signal speed and channel-width design in a dynamic SMDL gate, SPICE simulations on the fall delay time T_{PHL} of various PN dynamic SMDL gates excited by an evaluation clock ϕ with 1.6-ns rise time were performed. Some of the results are listed in Table V where the delay times of the corresponding conventional dynamic gates are also given for comparison. It is seen that if the multidrain structure is formed in the output NMOS, the channel widths of the other three NMOS's must be doubled as shown in the second circuit of Table V. As compared with the corresponding conventional dynamic gate, the total channel area is the same and the delay time is also the same. If the multidrain structure is formed in the second upper NMOS as shown in the third circuit, suitable width design still leads to the same total channel area and nearly the same speed. Generally, the gate speed characteristics of the dynamic SMDL are similar to those of conventional dynamic circuits.

To illustrate more clearly the advantageous features of the dynamic SMDL, a dynamic lookahead carry generator for a dynamic 4-bit full adder is designed and shown in Fig. 10(a) where the circuits used to generate $\overline{P}_i$ and $\overline{G}_i$ are not drawn out. As compared with the conventional design which implements C_2, C_3, and C_4 separately using dynamic AOI/OAI gates as shown in Fig. 10(b), the design in Fig. 10(a) is much more compact due to the multidrain capability which merges many devices together.

The layout of both circuits was generated according to 2-μm CMOS design rules. The layout of the dynamic SMDL lookahead carry generator in Fig. 10(a) is shown in Fig. 10(c). As compared with the layout of the conventional CMOS design, the chip area of the SMDL design is only 58 percent that of the CMOS design. This is due to the highly merged structure and the simple interconnection, as can be seen from Fig. 10(c). Generally, less interconnection complexity also leads to smaller delay. Such advantageous features become more significant in VLSI design where interconnections dominate both packing density and signal delay.

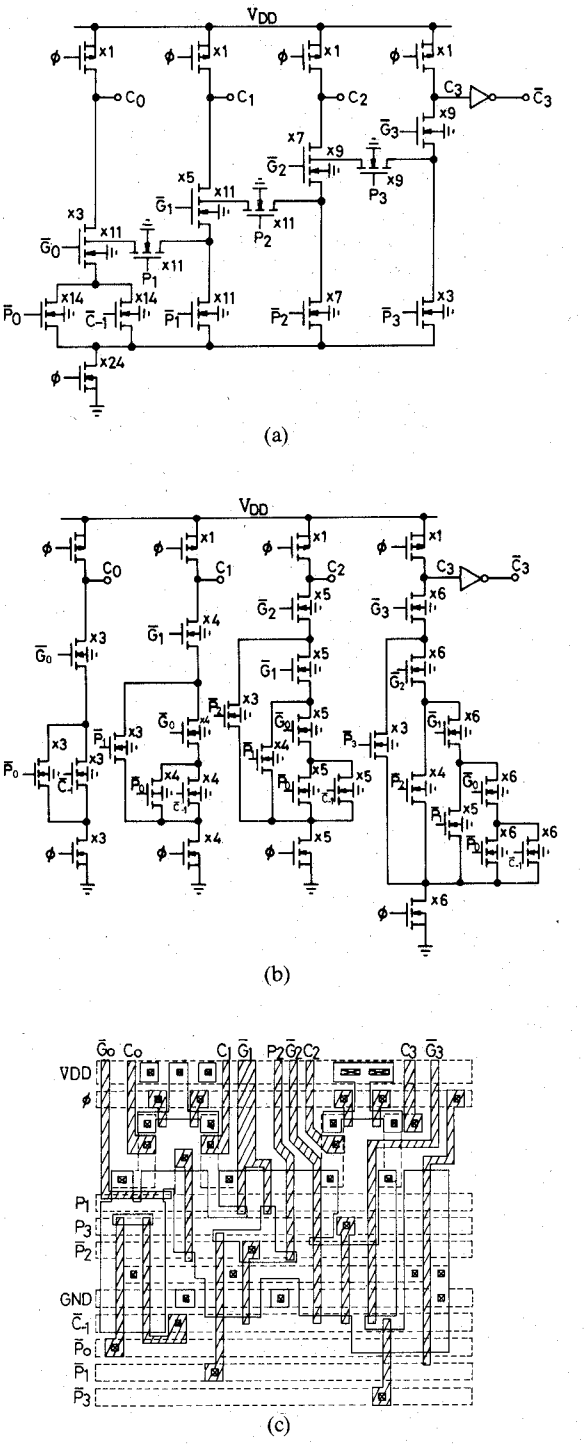
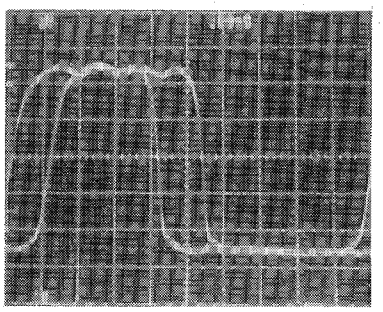


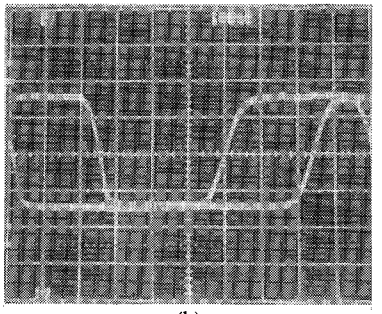
Fig. 10. (a) Circuit structure of a dynamic SMDL lookahead carry generator. (b) Circuit structure of a dynamic CMOS lookahead carry generator. (c) Layout of the dynamic SMDL lookahead carry generator based on 2-μm CMOS design rules.

V. EXPERIMENTAL RESULTS

One string of ten identical static PN MDL inverters and one string of ten identical standard CMOS inverters were designed, fabricated, and measured. The output node of



(a)



(b)

Fig. 11. Measured characteristic waveforms of the fabricated PN MDL inverters with (a) $V_{DD} = 5$ V, and (b) $V_{DD} = 3$ V.

TABLE VI
EXPERIMENTALLY MEASURED AVERAGE DELAY TIMES OF PN MDL AND CMOS INVERTERS

VDD	GATE	T_{PF} (ns)	T_{PR} (ns)	$(T_{PF}+T_{PR})/2$ (ns)	MDL/CMOS
5V	PN MDL	103.5-121.5	111.3-125.0	107.6-120.1	0.82 - 0.78
	CMOS	129.3-149.6	132.4-159.4	130.9-154.5	
3V	PN MDL	236.3-265.6	233.4-245.1	240.7-250.0	0.72 - 0.77
	CMOS	325.2-338.9	324.2-335.9	324.7-337.4	

each inverter is connected to a bonding pad through a CMOS buffer. Due to the buffer action, the output load capacitance in each inverter is nearly the same even when the output bonding pads of the fifth and seventh inverters are connected respectively to two FET probes with 2-pF input capacitance. By using such an arrangement, therefore, the characteristic waveform timing can be measured through the FET probes.

Typical measured characteristic waveforms of the PN MDL inverters which were designed and fabricated by using 5-μm p-well CMOS technology are shown in Fig. 11(a) and (b) with $V_{DD} = 5$ and 3 V, respectively. The two waveforms in each figure are identical because they are measured from the outputs of the fifth and seventh stages. The pair delay T_{PF} (T_{PR}) between two fall (rise) waveforms thus can be measured directly. The results are listed in Table VI where the corresponding data of standard CMOS inverters are also given. It is seen that the measured delay times of static PN MDL inverters are about 0.72–0.82 times as small as those of standard CMOS inverters. These experimental observations, therefore, are consistent with the theoretical predictions described in Section III.

VI. DISCUSSION AND CONCLUSION

A novel logic in CMOS technology called the CMOS multidrain logic (MDL) is proposed, analyzed, and experimentally observed in this study. In the static CMOS MDL, four different configurations are available in logic design and complex logic gates are formed through the use of WIRE-AND and WIRE-OR capabilities in PN and NP configurations, respectively. Due to the wire logic and the multidrain capabilities, the average area per gate is smaller in the MDL than in the conventional CMOS. Furthermore, the minimum delay of a PN MDL inverter with single fan-in and fan-out is about 200 ps in 2-μm CMOS technology. This speed performance is comparable to that of I^2L or even ECL and is about 20–70 percent better than that of the conventional CMOS. The power–delay product is nearly the same as that of the conventional CMOS under 300-MHz operations but is smaller than that of I^2L and ECL. Therefore the static CMOS MDL can be used to increase the signal speed while keeping the same power–delay product as the conventional CMOS. Meanwhile, it is expected that the static CMOS MDL can be designed to achieve the bipolar speed level with smaller power–delay product and smaller dc power dissipation.

The static CMOS MDL can be stacked to form the stacked MDL (SMDL). Both PP and NN configurations in the MDL and the SMDL can be converted into dynamic circuits. They have no glitch problems. Moreover, due to the inherent multidrain structure which can be used to realize many Boolean terms within a highly merged dynamic SMDL gate, the resultant circuits have higher packing density and lower interconnection complexity than other CMOS dynamic circuits. These advantageous features make the dynamic CMOS SMDL a potential technique in CMOS VLSI design.

Based upon the results in this study, it is felt that the bipolar-competitive MOS VLSI can be designed by using the bipolar-like CMOS logic circuits. Further research in this direction will be done.

APPENDIX

According to different operating regions of the consistent MOSFET's in the PN MDL inverter shown in Fig. 2, the transfer characteristic of Fig. 3 can be divided into four regions. In Region I, $V_{in} = V_L < V_{Tn}$ and the NMOS M_N is OFF. We have

$$I_{dn} \simeq 0$$
$$V_0 = V_H = V_{DD}.$$

In Region II, $0 < V_{in} - V_{Tn} < V_o$. In this region, M_N is in the saturation region whereas the PMOS M_{PL} is in the linear region. Thus we have

$$I_{dn} = \mu_n C_{on}(W/L)_N (V_{in} - V_{Tn})^2/2$$
$$= I_{dp} = \mu_p C_{op}(W/L)_p \left[2(V_{DD} - |V_{Tp}|) \cdot (V_{DD} - V_0) - (V_{DD} - V_0)^2\right]/2.$$

The output voltage V_o can be solved from the above equation as

$$V_o = -|V_{Tp}| + \sqrt{(|V_{Tp}| - V_{DD})^2 - R(V_{in} - V_{Tn})^2}. \quad (7)$$

In Region III where $V_{in} - V_{Tn} > V_o > |V_{Tp}|$, both MOSFET's are operated in the linear region. The current can be written as

$$I_{dn} = \mu_n C_{on}(W/L)_N \left[2(V_{in} - V_{Tn})V_o - V_o^2\right]/2$$
$$= I_{dp} = \mu_p C_{op}(W/L)_p \left[2(V_{DD} - |V_{Tp}|) \cdot (V_{DD} - V_o) - (V_{DD} - V_o)^2\right]/2.$$

Solving the above equation, we have

$$V_o = \left\{ R(V_{in} - V_{Tn}) - |V_{Tp}| - \left\{ \left[|V_{Tp}| - R(V_{in} - V_{Tn})\right]^2 - (R-1)\left(V_{DD}^2 - 2V_{DD}|V_{Tp}|\right)\right\}^{1/2} \right\}/(R-1). \quad (8)$$

In Region IV, $V_o < |V_{Tp}|$ and $V_o < V_{in} - V_{Tn}$. Thus M_N is in the linear region and M_{PL} is in the saturation region. From the current relation which can be similarly written out, V_o can be solved as

$$V_o = V_{in} - V_{Tn} - \left[(V_{in} - V_{Tn})^2 - (V_{DD} - |V_{Tp}|)^2/R\right]^{1/2}. \quad (9)$$

It may be seen from (9) that Region IV exists only when $V_{Tn} \leq V_{DD} - (V_{DD} - |V_{Tp}|)/R^{1/2}$.

To find V_L, V_{in} in (8) and (9) must be replaced by V_{DD} $(= V_H)$. The resultant expression is shown in (2).

One of the unity-gain points defined at the point of V_{iul} and V_{oul} is located in Region II. By taking the first derivative of (7) and setting it to unity, V_{iul} and V_{ouh} can be expressed as

$$V_{iul} = V_{Tn} + (V_{DD} - |V_{Tp}|)/(R^2 + R)^{1/2} \quad (10)$$

$$V_{ouh} = -|V_{Tp}| + (V_{DD} - |V_{Tp}|)\left[R/(R+1)\right]^{1/2}. \quad (11)$$

The other unity-gain point denoted by V_{iuh} and V_{oul} is located in Region III. By using the similar method, V_{iuh} and V_{oul} can be written as

$$V_{iuh} = V_{Tn} + |V_{Tp}|/R + (2R-1) \cdot \left[\left(V_{DD}^2 - 2V_{DD}|V_{Tp}|\right)/(3R-1)\right]^{1/2}/R \quad (12)$$

$$V_{oul} = \left\{ R(V_{iuh} - V_{Tn}) - |V_{Tp}| - \left\{ \left[|V_{Tp}| - R(V_{iuh} - V_{Tn})\right]^2 - (R-1)\left(V_{DD}^2 - 2V_{DD}|V_{Tp}|\right)\right\}^{1/2} \right\}/(R-1). \quad (13)$$

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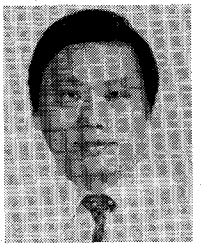

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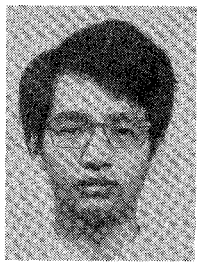

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