國立交通大學

電子工程學系 電子研究所碩士班

碩 士 論 文

交絡奈米碳管網路薄膜電晶體特性之研究

A Study on Thin Film Transistor Performance Based on Percolating Carbon Nanotube Networks

研究生：陳定業

指導教授：崔秉鉞 教授

中華民國一ＯＯ年九月

交絡奈米碳管網路薄膜電晶體特性之研究

A Study on Thin Film Transistor Performance Based on Percolating Carbon Nanotube Networks

研究生：陳定業　　Student : Ting-Yeh Chen

指導教授：崔秉鉞　　Advisor : Bing-Yue Tsui

國立交通大學

電子工程學系 電子研究所

碩士論文

A thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical Engineering and Computer Science

National Chiao Tung University

in Partial Fulfillment of the Requirement

for the Degree of Master

in

Electronic Engineering

2011

Hsinchu, Taiwan, Republic of China

中華民國一 OO 年九月

交絡奈米碳管網路薄膜電晶體特性之研究

研究生：陳定業　　指導教授：崔秉鉞

國立交通大學電子工程系 電子研究所碩士班

摘要

本論文利用旋塗法製作交絡碳管網路於區域性背閘極薄膜電晶體，因金屬性與半導體性碳管同時存在於碳管網路中，元件特性必須在導通電流和電流開關比之間取得平衡。在此元件特性有兩種極端情形，一為元件有大導通電流10^{-5}安培但低電流開關比小於10，另一類元件特性為低導通電流10^{-8}安培與高電流開關比大於10^{3}。

為求最佳化之元件特性，本次研究應用交絡理論於隨機分布之碳管網路，系統性的分析各項參數包含碳管密度、碳管長度、元件通道長度與寬度、不同介電層材料與厚度對元件導通電流、電流開關比與載子遷移率之影響。

研究發現增加碳管密度能增加通道中導通路徑之數目，因而提高導通電流。但當金屬性碳管之密度高於滲濾閾值(percolation threshold)時，元件開關比會大幅衰退。隨著通道長度增加，導通電流呈非線性下降，此因區域性背閘極與基板間之高低差造成碳管在通道上分布不均。同時增加通道長度能降低金屬性導通路徑的形成而改善元件開關比。為使元件有高導通電流之特性下同時保有良好的元件開關比，在通道寬度50微米、通道長度分別為1.4、4、7微米之元件尺寸下，最佳化之碳管溶液旋塗次數分別為30、40、60次。

減少通道寬度同樣造成導通電流非線性減少與電流開關比之改善。在此可發現當通道長度大於4微米時，電流開關比將維持在固定範圍，不隨通道寬度而改變。氧化鋁介電層之厚度由10奈米降至5奈米能有效降低元件操作電壓，但對導通電流與元件開關比之影響甚小。增加碳管之平均長度能減少導通路徑所需之碳

管數目與碳管間接觸阻抗，使得導通電流大幅提升。然而使用長碳管同時也增加金屬性導通路徑形成之機率，須將碳管旋塗次數降至20次以下，元件才有可能形成半導體特性。比較分別利用氧化鋁與二氧化鉿介電層製作之元件，可發現因二氧化鉿對碳管之浸潤性較差，造成碳管不易分布在二氧化鉿表面而使導通電流較低，因此氧化鋁較適合製作區域性背閘極元件。

除了元件電性分析外，論文中同時模擬二維交絡碳管網路在通道長度1.4到7微米時所需的滲濾閾值，發現增加元件長度會使得滲濾閾值提升。模擬得出之滲濾閾值略高於利用掃描式電子顯微鏡下觀測之滲濾閾值，此因肉眼觀察碳管數目產生之誤差。

利用電性量測轉換之載子遷移率介於0.01至2.7 cm^2/Vs之間，此值優於有機化合物之載子遷移率。當考慮碳管分布只佔通道之1%，歸一化之載子遷移率介於1至270 cm^2/Vs之間，其載子遷移率低於單根碳管元件，乃是因為碳管網路中串聯之蕭基位障所限制，減少通道長度與寬度可提高載子遷移率。論文最後利用電壓崩潰法，使元件操作在合適的崩潰電壓區間內，對通道長度小於4微米之元件，電流開關比能提升超過兩個數量級。通道長度大於4微米之元件，不需此法元件即可擁有半導體操作特性。

A Study on Thin Film Transistor Performance Based on Percolating Carbon Nanotube Networks

Student: Ting-Yeh Chen Advisor: Bing-Yue Tsui

Department of Electronics Engineering

Institute of Electronics

National Chiao Tung University

Abstract

In this work, percolating carbon nanotube (CNT) network fabricated by spin-coating method was applied to local bottom gate thin film transistor. Since the percolating CNT networks consist of mixture of both metallic and semiconducting CNTs, there is a trade off of device performance between high on-state current and high on/off ratio. One extreme case is devices with high on-state current of 10^{-5} A at low on/off ratio < 10, and another case is devices with low on-state current of 10^{-8} A at high on/off ratio > 10^{3}.

A systematical analysis based on percolation theory was applied to determine various effects including CNT density, CNT length, devices dimension, gate dielectric thickness, and different coating surfaces on on-state current, on/off ratio, and field-effect mobility for optimized device performance in this thesis.

Increasing CNT density results in the increase of on-state current due to increase of the number of CNT conducting paths in channel. On the other hand, if metallic CNT density exceeds percolation threshold for high CNT coating density, the on/off ratio would dramatically degrade. Increasing channel length decreases on-state current

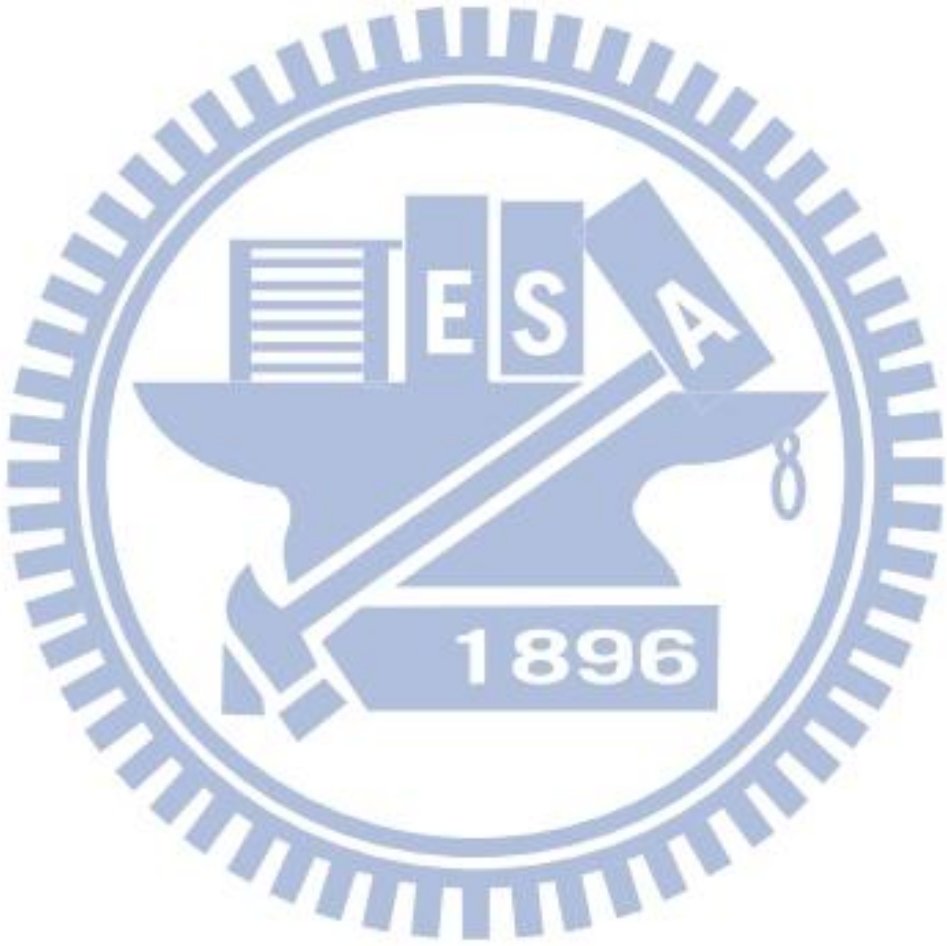
nonlinearly due to non-uniform CNT coverage resulted from geometric rise of bottom gate. In addition, the increase of channel length also improves on/off ratio since metallic conducting paths are hard to form. The optimized CNT coating density for devices with high on-state current at acceptable on/off ratio > 100 is CNT coating density of 30, 40, and 60 cycles for channel length of 1.4, 4, and 7 μm and channel width of 50 μm, respectively.

Decreasing channel width decreases on-state current nonlinearly and enhances on/off ratio. It is observed that on/off ratio > 100 remains and is not varied with increasing channel length of L> 4 μm for high CNT coating density. Decreasing Al_2O_3 gate dielectric from 10 nm to 5 nm further reduces the operate voltage. But the dependence of on-state current and on/off ratio is weak. Increasing CNT length reduces the number of CNT intersections and then increases on-state current significantly. However, the CNT coating density needs to be below 20 cycles to exhibit semiconducting behavior. For different dielectric layers of Al_2O_3 and HfO_2, since poor wet ability of HfO_2 film determined by SEM images attributes low on-state current, Al_2O_3 film is proper for local bottom gate CNTTFTs.

Monte Carlo simulations of two-dimensional percolating CNT networks were performed to obtain percolation threshold for channel length varying from 1.4 to 7 μm. Increasing channel length results in the increase of percolation threshold. The simulation results of percolation threshold are lower than CNT density determined by SEM images since counting error and resolution of SEM contribute to the deviation of percolation threshold between simulation and experimental results.

The effective field-effect mobility ranging from 0.01 to 2.7 cm^2/Vs is superior to mobility of organics. Since CNT network coverage is lower than 1% in SEM images, the normalized field-effective mobility is in a range of 1-270 cm^2/Vs, which is limited by the series of Schottky barriers between CNTs. Besides, decreasing channel length

and width would increase field-effective mobility. Finally, we also performed adapted electrical breakdown method to enhance on/off ratio. It is noticed that on/off ratio could be improved by larger than two orders of magnitude for devices with channel length L< 4 μm. For L> 4 μm, all devices exhibit semiconducting behavior without the help of this method.



致謝

在這兩年的研究所生活中，無論是在課業知識、製程技巧或是研究方法都習學到許多，過程中雖遭遇些許瓶頸，也靠著大家的幫助度過難關，在此獻上由衷感謝。

首先最感謝的便是指導教授 崔秉鉞老師，從大學專題便在老師指導下研究，在老師悉心指導與討論下，不只是如何有系統條理的分析實驗上的數據，在作學問的態度方面，正直卻不失圓融的處事方法更是學生學習的目標。

實驗方面則感謝交大奈米中心與國家奈米元件實驗室所提供的製程機台，其中特別感謝 NDL 負責曝光機台的庭瑋姊，在庭瑋姊的幫助下，讓我的製程速度提升許多，而其開朗風趣的談吐也讓無塵室的生活增添不少樂趣。

感謝實驗室的大家，振銘學長不論是在實驗製程、結果討論、訓練機台、甚至日常生活與休閒上都惠我良多，互相勉勵一同畢業的畫面仍記憶猶新。元件物理上與實驗的問題則感謝元宏學長與嶸健的討論與幫助，也很感謝瑄美學姊在我力不從心時候的幫忙。碳管研究方面則感謝孝瑜學姊與振欽學長的幫助，讓我能很快進入狀況進行碳管的研究。

在此也要感謝室友兼六年同學罩哥培宇的幫忙，不管是研究討論或是平常的生活起居，沒有罩哥的出現學校生活的回憶便會出現空缺。同時也要感謝炫滋帶給實驗室歡笑與新想法還有食物、子瑜、克勤、茂元、高銘鴻、孫銘鴻，在生活與實驗上的幫忙以及崇德、哲儒、雪君、翰奇、泰源與國丞帶給實驗室年輕活力。

最後要感謝我的父母與弟弟對我的支持，讓我能無後顧之憂的進行研究，並朝自己的目標前進，謝謝你們。

Contents

List of Tables

Chapter 1

Chapter 3

List of Figures

Chapter 1

Chapter 2

Chapter 3

Chapter 1

Introduction

1-1 Fundamental Properties and Fabrication of Carbon Nanotubes

In 1985, R. Smalley, H. Kroto, and R. Curl found C_{60} molecule formed by performing laser irradiation to vaporize graphite [1]. This carbonaceous product has a truncated icosahedrons structure, which is commonly considered as the football called buckyball. This C_{60} molecule has a stable structure which all sites are satisfied with one double bond and two single bonds. The discovery of C_{60} caught researcher's eyes and made significant study of carbonaceous product.

In 1991, S. Iijima, a researcher of NEC corporation, first found multi-walled nanotubes (MWNTs) in fullerene synthesis [2]. MWNTs have hollow cylinder structure consisting of multiple concentric shells of graphite. Soon after the discovery of MWNTs, in 1993, Iijima discovered single-walled nanotubes (SWNTs) grown by using transition metals as catalysts [3].

Carbon nanotubes (CNTs) are hollow cylinder structures with diameter verying from 1 to several nm and length up to tens of μm. We can imagine that CNTs are made by wrapping graphene sheets to tube structures. There are two types of CNTs including single-walled nanotubes (SWNTs) and multi-walled nanotubes (MWNTs) shown in Fig. 1-1 [2,4]. The diameter of a SWNT is usually 1-2 nm whereas the diameter of a MWNT is ranging from 1 nm to hundreds of nm depending on the number of graphite shells with the spacing of 0.34 nm between each interlayer [5]. The characteristics of MWNTs are hard to analyze due to the complex interaction of

multiple shells. In addition, CNT bundles could be formed owing to van der Waals force between successive graphene layers.

The diameter and the way graphite layer wrapped of SWNT are defined uniquely by the chiral vector $c= na_1+ ma_2$, which denoted as (n,m) indices on two-dimensional graphene layer, where a_1 and a_2 are lattice vectors and (n,m) are integers shown in Fig. 1-2 [6-7]. SWNTs exhibit metallic or semiconducting behavior which are affected by (n,m) indices. There are three types of SWNTs including zigzag, chiral and armchair SWNTs. Zigzag (n,0) SWNTs which the index of m= 0 could exhibit metallic behavior as n/3 is an integer, otherwise zigzag SWNTs exhibit semiconducting behavior. Chiral (n,m) SWNTs also can have metallic or semiconducting behavior, when (2n+m)/3 is an integer, SWNTs exhibit metallic behavior and in other cases of (n,m) semiconducting SWNTs exist. Armchair (n,n) SWNTs which the index of m= n only exhibit metallic behavior. The calculation results derived from electronic band structure also confirmed that about l/3 SWNTs are metallic and 2/3 SWNTs are semiconducting [8-9]. The diameter of SWNTs is defined as $d = \frac{|c|}{\pi} = \frac{a}{\pi}\sqrt{n_1^2 + n_1 n_2 + n_2^2}$, where a= 0.246 nm, which is the unit vector of graphene lattice [8]. In addition, the band gap is inversely linear proportion to the diameter of SWNTs [4,10].

CNTs could be synthesized by various methods such as arc discharge [11], laser ablation [12-13], and chemical vapor deposition (CVD) [14-16].

The arc discharge method was performed to form the fullerenes in the beginning and is a simple way to produce CNTs. The reaction chamber is filled with inert gas at low pressure. The high temperature discharge occurs between two carbon electrodes by applying high potential difference. The discharge would vaporize and consume the positive carbon electrode. On the other hand, the carbonaceous products containing

CNTs are produced in the negative electrode. The product formed in this method is a complex mixture containing both SWNTs and MWNTs with some defects and catalysts. Thus, the purification is needed. The yield is low and depends on the gas pressure in the reaction chamber and the temperature of discharge.

The laser ablation method is conducted by using a laser pulse to vaporize the target which is a mixture of graphite and metal catalyst particles such as cobalt or nickel in the chamber filled with inert gas. As the carbonaceous vaporization condenses, SWNTs are formed on the cool surface. This method is with high yield of 70% and synthesizes SWNTs with controllable diameter and better quality. The diameter of SWNTs could be defined by tuning the growth temperature and catalyst composition. However, it is much expensive than arc discharge and CVD method.

The principle of chemical vapor deposition (CVD) method is that by feeding process gas such as hydrogen and carbonaceous gas such as methane or ethylene into reaction chamber, CNTs would grow at the location of metal catalysts on the substrate at high temperature. The diameter of CNTs depends on the size of metal catalysts [17]. In addition, the alignment of CNTs can be realized by applying electric field on silicon substrate with patterned metal catalysts [18] or on single crystal quartz substrate [19]. The CVD method is suitable for large scale production for commercial industry to decrease the cost of SWNT production.

1-2. Potential Applications of CNTs

CNTs have various potential properties such as one-dimensional transport , extraordinary electrical, thermal, mechanical, optical, and chemical property, which are attractive and studied in many applications including TFTs [20-21], diodes [21], logic circuits [22], optical modulators [23], strain-sensing devices [24], chemical

[25-26] and biological [27-28] sensors.

The metallic CNTs could carry electric current density of 4×10^9 A/cm^2, which is 1000 times larger than copper [29]. CNTs exhibit high thermal conductivity of 3500 $Wm^{-1}K^{-1}$ along the tube direction, comparing to thermal conductivity of copper of 385 $Wm^{-1}K^{-1}$[30-31]. In addition, it is also an insulator with thermal conductivity of 1.52 $Wm^{-1}K^{-1}$ across the tube direction. CNTs have tensile strength of 63 GPa and are remarkably flexible with high elastic modulus due to formation of sp^2 bond [32-33].

1-3. Electrical Characteristics of CNTFET with Single SWNT

In 1998, the first carbon nanotube field-effect transistor (CNTFET) consisting of one semiconducting SWNT as channel connected to metal S/D was fabricated [34-35]. The fabrication of this single molecule device realizes the potential for next generation of molecular electronics. Nowadays, CNTFETs exhibit high mobility of 100000 cm^2/Vs [36], current carrying capacity > 10^9 A/cm^2 [37], on/off ratio > 10^6 [38], and subthreshold swing < 80 mV/decade [39].

In an ambient environment, the semiconducting CNTs usually exhibit p-type behavior [37] since the adsorbed oxygen on CNT surface results in the modification of the Schottky barriers between metal contacts and CNT [40]. The location of Fermi level pinning is close to the valence band. Studies also showed that the conversion from p-type to n-type CNTTFT could be done by doping CNTs with alkali metals [41-42] or polyethylene (PEI) [21,43] to change barrier thickness and shift the threshold voltage, or anneal CNTTFTs [40] to remove adsorbed oxygen. It is noticed that oxygen modifies the barrier at contact rather than dopes the bulk of tube. The oxygen would oxidize the metal contact and then changes the charge transfer from metals. In addition, by lining up the valence or conduction band of CNTs to Fermi

level of metal contact, for instance, palladium (Pd) for p-type and scandium (Sc) for n-type CNTTFT were demonstrated [37,44].

The electrical characteristics of CNTTFT would be affected by various factors such as chirality and diameter of CNTs [45], types of metal contacts [46], environmental conditions. The band gap of CNT is inversely proportion to the diameter of CNTs and different chirality of CNTs contributes to metallic or semiconducting behavior. Choosing proper metals which have strong interaction with carbon results in good contact between S/D and CNTs. CNTTFTs are also sensitive to environmental conditions such as gas type, vapor, and vacuity. Charge transfer occurs from adsorbed gas molecules to CNTs [47-49] and water vapors contribute the hysteresis of CNTTFT due to charge trapping by water molecules around the CNTs [50-52]. In addition, the irradiation of electrical beam would damage CNT structure and decrease the conductivity of CNTs [53-54]. Although CNTTFTs with individual SWNT exhibit superior performance, the large variation of electrical characteristics between each device hurdles the development of CNTTFTs which are not suitable for large scale production.

1-4. Percolating CNT network TFT

In order to minimize the variation between each SWNT, TFTs based on SWNT networks consisting of large number of SWNTs rather than individual SWNT are fabricated to average individual SWNT deviation by SWNT networks. In 2003, Duan et al. proposed TFTs fabricated with aligned CNTs as channel by using flow-directed alignment method [55]. This work offered a new direction for high performance TFTs. Since then, many studies of CNT network TFT are published.

CNT network TFTs could be divided to two groups by the way CNT networks

orient. Y. Huang showed that parallel CNT array could be formed by using fluidic alignment and flow direction control with surface-patterning of PDMS mold [56]. CNT orientation also could be controlled by the direction of gas flow with a tilt angle [57-58]. M. Engel used evaporation self-assembly method to orient CNT arrays [59]. The CNT array also could be fabricated on a designed array of catalysts by using PECVD [60]. A.D. Franklin proposed aligned CNT array FETs with current density > 40 uA/μm at on/off ratio $>10^5$ [61], however, the CNT array needed to transfer from quartz to silicon wafers. This CNT transfer process preserved CNT density and alignment by using thermal release adhesive tape, but the process was complex and unsuitable for large scale manufacture [62]. The drawback of aligned CNT network is that the assembling process is complex and lack of precise control of CNT alignment. Although CNT arrays would align along specific direction, intersections between CNTs still exist. Papers listed above about aligned CNT network as device channel are shown in Table 1-1.

Due to the simplicity for the formation of CNT network, random CNT network TFTs which CNTs orient with no preferential directions are suitable for large scale fabrication. A large number of CNTs average deviation of individual CNT. E.S. Snow reported a random SWNT networks TFTs with field-effect mobility of 10 cm^2/Vs at on/off ratio > 10^5 for low CNT density and field-effect mobility > 100 cm^2/Vs at on/off ratio < 10 for high CNT density [63-64]. CNT powder dissolved in SDS [65] or EAQ/DMF [66] solution with gradient ultracentrifugation were used to separate CNT bundles and improved the uniformity of CNT networks formed by spin-coating method. In addition, aminosilane such as aminopropyltriethoxy silane (APTES) was used to functionalize the SiO2 [67] and HfOx [68] surface to achieve high density and uniform CNT network due to its well-known affinity to the CNTs.

The simple way to fabricate random CNT network is performing spin-casting

method. However, about 1/3 metallic and 2/3 semiconducting CNTs both exist in network. Once metallic CNT conducting paths bridge channel, the on/off ratio would significantly degrades. Recently some works studied percolation theory [69-71] which was studied in the formation of CNT conducting paths in the network. J. N. Coleman reported an organic composite consisted of mixture of organic polymer and CNTs [72]. The CNT concentration increased with the significant increase of conductivity of organic composite which was in agreement of percolating behavior. L. Hu studied the sheet conductance and transparency of CNT network as a function of CNT density [73]. When the CNT density is above the percolation threshold, conductivity of CNT network increases obviously. This means the CNT conducting paths are formed. On the other hand, the percolation theory is not suitable for study of optical transparency of CNT network since transparency is determined by CNT excitation rather than CNT conductance. H. E. Unalan found that device performance of CNT TFT is limited by metallic CNTs as percolation density of metallic CNTs is much below percolation threshold of conducting paths [74]. S. Kumar studied a computational model containing ballistic and diffusive transport limit to analysis the conductance of CNT network [75]. A. Behnam performed Monte Carlo simulations to study the geometry-dependant resistivity of CNT films and found that the lowest resistivity occured in the partially aligned CNTs rather than perfectly aligned CNTs [76]. J. Hicks reported the CNT length distribution dependent on the resistivity for junction-resistance-dominant and intrinsic-resistance-dominant CNT networks, respectively [77]. S. Seppälä computed percolating network of CNT bundles due to van der Waals interaction for varying bundle length and bundle density. This work discovered semiconducting CNT bundle paths were more frequently formed for low density comparing with ordinary SWNT networks [78]. V. K. Sangwan performed experiments and simulations to determine that the percolating CNTTFT with mobility

of 5~50 cm^2/Vs at on/off ratio > 10^3 at L > 70 μm and W= 50 μm for CNT density of 0.54~0.81 CNTs/μm^2 [79]. Table 1-2 shows papers discussing random CNT networks as device channel.

1-5. Motivation

Recently, most percolation issues were emphasized on the conductance of CNT network rather than device performance of CNT network TFTs. Although some studies showed experimental electrical characteristics of devices fabricated with CNT percolating networks, a few works focused on the analytical study of properties of CNT networks TFT. This thesis systematically studied the effects of CNT property and device geometry on device performance based on CNT networks for both experiments and simulations. By studying the percolating CNT network with proper fabrication condition and device structure, the suitable device design and control could be obtained.

This thesis studies the carbon nanotube network thin film transistor (CNTN TFT) structure consisting of an extra poly-Si gate as local bottom gate instead of using heavily-doped Si substrate as a back gate. The merit of back gate structure is easy to fabricate. However, the back gate structure would not control each device on whole wafer respectively at single operation. Besides, devices with back gate structure need thicker gate dielectric layer to prevent gate leakage since that source/drain is totally overlapped by back gate. But increasing gate dielectric thickness would degrade the gate-to-channel control ability.

To improve the drawback of back gate structure, some papers proposed the idea of top-gated CNT TFT [39]. Though top gate structure would control each device respectively, the surface coverage of top gate dielectric layer and gate leakage are

severe issues. First, the gate dielectric would not be formed by thermal oxide since the CNT network which belongs to back-end process is formed prior to gate dielectric. Other methods to form gate dielectric layer would be sputter, plasma enhanced chemical vapor deposition (PECVD), E-gun evaporation, atomic layer deposition (ALD), and so on. But note that for some process such as PECVD would strongly damage CNTs by plasma bombardment. G. Zhang presented a plasma hydrocarbonation reaction to selectively etch metallic CNTs and remain semiconducting CNTs [80]. The key process to selective etch metallic CNTs was to use methane plasma instead of hydrogen plasma due to its moderate reactivity.

Recently ALD is a popular process to form the gate dielectric to cover on CNT network. However, ALD process is still difficult to grow high quality of thin film on CNT network since the chemical inert exterior surface of CNTs would retard the precursor to absorb on. Therefore, to form perfect ALD gate dielectric layer on CNT network needs another CNT functionalization to improve the surface coverage of top gate dielectric layer and prevent gate leakage. B Damon made NO_2 functional group attach to nanotube surface to improve the ALD Al_2O_3 layer uniformity due to the reactivity of precursors enhencement [81-82].

The second issue of top gate structure is gate leakage. In order to avoid damaging CNTs, the source/drain fabrication also needs to prevent CNTs exposing in the plasma atmosphere. Therefore, the metal source/drain definition process is performed by lift-off method rather than metal dry etching. The disadvantage of lift-off method is the sharp edge of source/drain affects the conformal ALD gate dielectric and makes gate dielectric locally thinner near sharp edge of source/drain. This locally sharp region further enhances the electric field and then increases the probability of gate leakage.

In this work, the CNTN TFT with poly-Si bottom gate which is compatible to

horizontal furnace of front-end process is studied. Bottom gate structure would eliminate the gate dielectric coverage issue since the gate dielectric formation is prior to CNT network fabrication. There is no need to employ other functionalization to CNTs. The reduction of overlap between bottom gate and source/drain could decrease the parasitic capacitance and scale the gate dielectric thickness to operate device at low operation voltage. Besides, devices with bottom gate structure would control single device at single operation.

1-6. Thesis Organization

The first chapter is the introduction including fundamental properties of CNTs, the CNT fabrication methods, and various applications using CNTs. Then, the review of individual CNT TFT and percolating random CNT network TFT are discussed. The second chapter shows the device structure of CNTN TFT, experimental settings and process flow.

Experiment results are discussed in the third chapter. Firstly, the CNT network distribution and various CNT densities corresponding to spin-coating cycles were determined by scanning electron microscopy (SEM) images. Electrical characteristics such as on-state current, on/off ratio, and field-effect mobility were conducted to study the following effects of CNT density and length, channel length and width dependence, gate dielectric thickness, and coating surface consisted of Al_2O_3 and HfO_2 on the device performance. The Monte Carlo simulation of percolating CNT network was also performed to determine percolation threshold with varying CNT density and device channel length. Finally, the adapted electrical breakdown is introduced to improve on/off ratio. The last chapter is the summary and future works of this thesis.

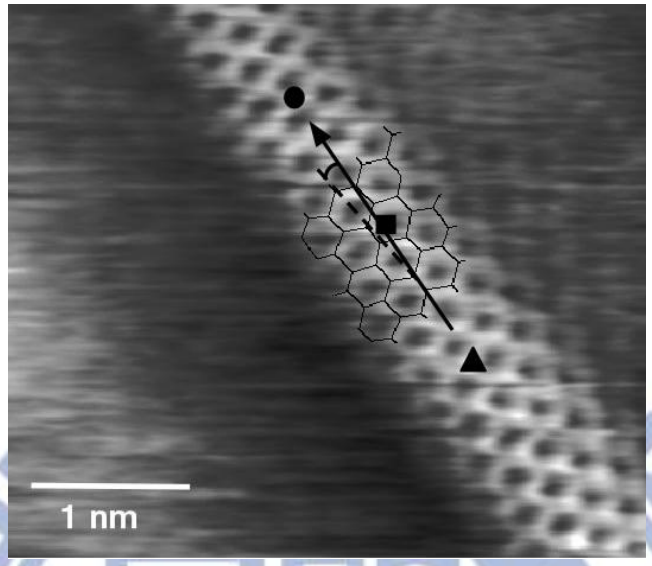
Table 1-1 Papers about using aligned CNT network as device channel.

Aligned CNT network as device channel	Current density (A/μm)	On/off ratio	Methods for aligned CNT network formation
X. Duan, et al. [55]	**1.94×10^{-6}**	**10^{8}**	Fuidic alignment (V_d=-1 V)
H. Kuo, et al. [58]	5.88×10^{-6}	<10	Tilted-drop casting (V_d=-0.5 V)
M. Engel, et al. [59]	2×10^{-7}	10^{4}	Self-assembly CNTs from solution (V_d= -0.1 V)
W.J. Yu, et al. [60]	2.5×10^{-9}	10^{6}	A designed array of catalysts by PECND (V_d= -0.1 V)
A.D. Franklin, et al. [61]	**4×10^{-5}**	**10^{5}**	CNT arrays are transferred from quartz to silicon wafers (V_d= -0.5 V)
S.J. Kang, et al.	1.9×10^{-6}	10^{4}	

Table 1-2 Papers about using random CNT network as device channel.

Random CNT network as device channel	Current density (A/μm)	On/off ratio	Methods for random CNT network formation
E.S. Snow, et al. [63]	2.86×10^{-6}	< 10	Random CNT network by using CVD method (V_d= -0.1 V)
	5.71×10^{-9}	**> 10^{5}**	
E.S. Snow, et al. [64]	5.38×10^{-7}	~ 100	The wafer was soaked in CNT solution and then blown dry (V_d= -0.01 V)
Z. Dai, et al. [66]	1.67×10^{-8}	~ 10^{4}	Spin-coating method with the help of EAQ to attack metallic CNTs (V_d= -2 V)
C. Wang, et al. [67]	1.85×10^{-7}	>10^{4}	The wafer was soaked in CNT solution and aminosilane was used to functionalize the SiO_2 [67] and HfO_2 [68] surface (V_d= -1 V)
K.C.Narasimhamurthy, et al. [68]	**1.3×10^{-5}**	>10^{4}	
V. K. Sangwan, et al. [79]	Mobility~50 cm^2 /Vs	~ 10^{3}	Random CNT network by using CVD method

(a)



(b)

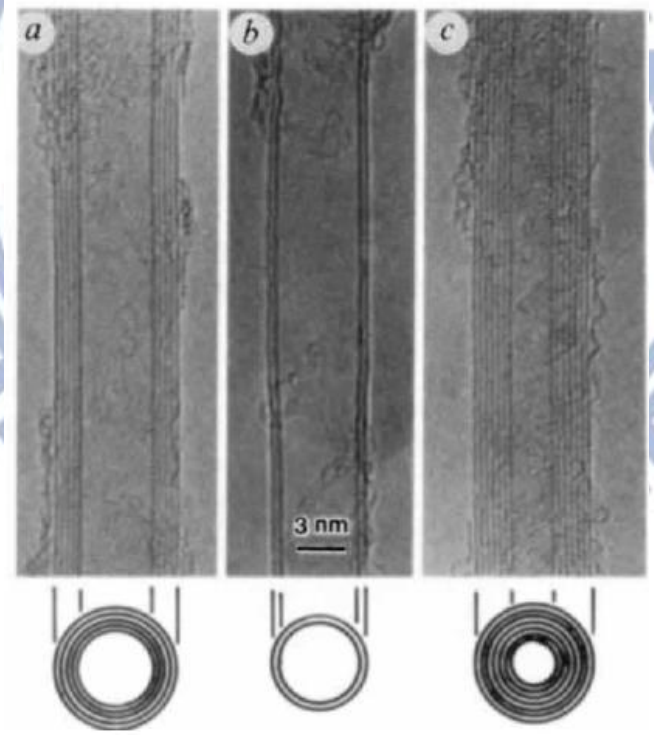


Fig. 1-1 (a) Scanning tunneling microscope (STM) image of a SWNT [4]. (b) Cross-section TEM images of MWNT with different sheets [2].

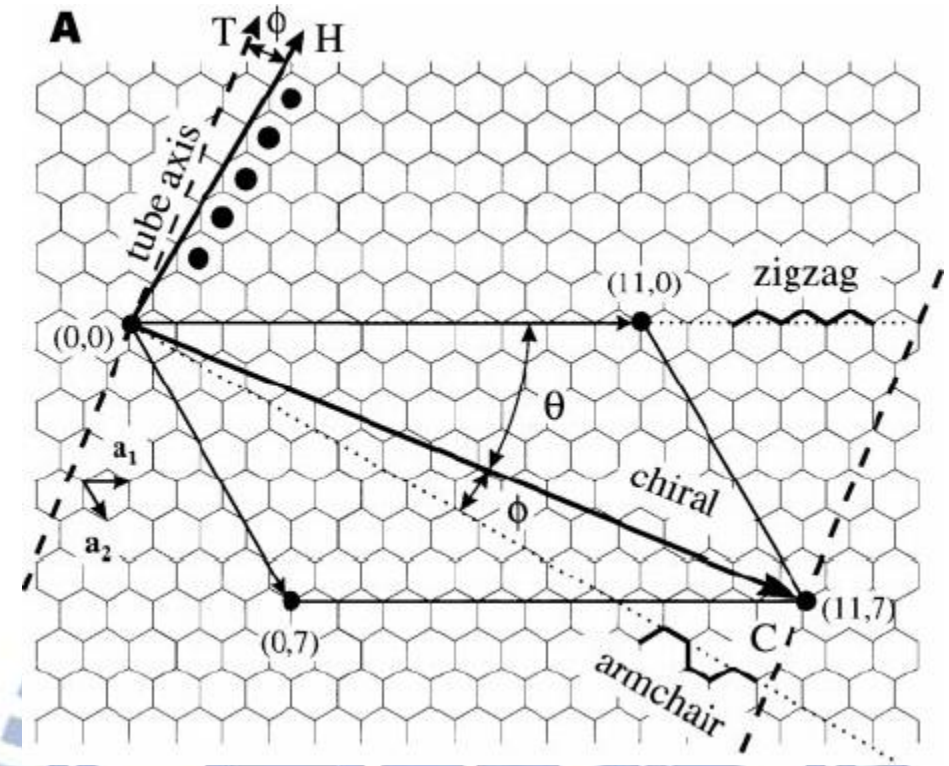


Fig. 1-2 Schematic description of the three types of SWNTs on the two-dimensional graphene layer: zigzag, chiral, and armchair SWNTs [6].

Chapter 2

Experimental Settings and Device Fabrication

2-1 Device Structure of CNTN TFT

Fig. 2-1 shows the CNTN network with bottom gate structure. First, a SiO_2 isolation layer was formed. Then, the in-situ doped N^+ poly-Si bottom gate was defined and a 900 ℃, 20 seconds RTA was performed to activate dopant of poly-Si. Atomic layer deposition (ALD) was performed to deposit Al_2O_3 and HfO_2 layer as gate dielectric respectively and then a 700℃, 30 minutes N_2 annealing was performed for Al_2O_3 layer densification. After the contact hole etching by dipping wafers in BOE solution, CNT network was formed by spin-coating method and defined by O_2 plasma. The CNT powder was dissolved in dimethylformamide (DMF) solution with 24-hours-socication for preparation. Finally, the palladium (Pd) source/drain was formed by lift-off process. Palladium had good interaction with CNTs and due to its high work function, the ohmic contact was formed between palladium and CNTs to reduce the barrier of hole transport [105]. Source/drain deposition after CNT network formation would reduce the gate leakage due to locally sharp edge of source/drain caused by metal source/drain lift-off method. The details of process flow would be described in section 2-4.

2-2 Experimental Settings

This thesis studies CNTN TFT with bottom gate structure. Devices are listed as following for electrical characterization:

1. CNT network with short length of CNTs (average length of CNT is 1.4 μm)

Sample a-d. CNTN TFT with 10 nm Al_2O_3 gate dielectric

Sample a. CNT coating density of 20 cycles

Sample b. CNT coating density of 30 cycles

Sample c. CNT coating density of 40 cycles

Sample d. CNT coating density of 60 cycles

Sample e-g. CNTN TFT with 5 nm Al_2O_3 gate dielectric

Sample e. CNT coating density of 30 cycles

Sample f. CNT coating density of 40 cycles

Sample g. CNT coating density of 60 cycles

Sample h,i. CNTN TFT with 10 nm HfO_2 gate dielectric

Sample h. CNT coating density of 40 cycles and sample i. 60cycles

2. CNT network with long length of CNTs (average length of CNT is 15 μm)

Sample j,k. CNTN TFT with 10 nm Al_2O_3 gate dielectric

Sample j. CNT coating density of 30 cycles and sample k. 60cycles

Fig. 2-2 is the top view of CNTN TFT device. The dumbbell-shaped black pattern is the active region of CNT network. The CNT network was covered underneath the light gray region of palladium as source/drain. The dark gray region is the poly-Si bottom gate. The black squares are the contact hole for performing electrical probing.

In this thesis, there are 8 sizes of channel length for mask layout: ranging from 0.4, 1.4, 4, 7, 9, 14, 29 to 49 μm. The channel widths of 5 μm, 20 μm, 50 μm are defined. For channel length of 0.4 μm and 1.4 μm, the source/drain to gate overlap is 0.3 μm. For other dimensions of channel length, the source/drain to gate overlap is 0.5 μm. Therefore, the gate lengths of devices are 1, 2, 5, 8, 10, 15, 30 and 50 μm respectively.

2-3 Carbon Nanotube Solution Makeup

The AP-Grade carbon nanotube powder was commercially obtained from CarboLex Inc. The carbon nanotbes were made by arc discharge method which produced both single and multi-walled nanotubes (MWNT). Since the AP-Grade carbon nanotube powder was not performed by any chemical treatment, the quality of CNTs is high and the purity of CNTs is between 50 to 70 vol%. The residual catalyst impurities are nickel (Ni) and yttrium (Y). There are 66.7% semiconducting SWNT and 33.3% metallic SWNT with diameter 1.4 nm and length about 1.4 μm. The diameter of CNT bundle is 20 nm. Fig. 2-3 shows the SEM image of AP-grade carbon nanotube provided by CarboLex Inc.

The carbon nanotube powder of 1 mg was dissolved in 40 ml dimethylformamide (DMF) solution which is very effective on separating and suspending CNTs. Note that if the concentration of CNT powder > 0.025 mg/ml, the concentration of CNT solution would exceed the saturation concentration and then deposit CNT residues. These residues of CNT bundles would make the CNT network non-uniform after employing spin-coating and then affect device electrical characterization. After dissolving the CNT powder in DMF solution, a 24-hours of sonication was performed to separate the tangled CNT bundles. The duration of sonication would not be longer than 24 hours to avoid the length reduction of CNT and the CNT quality degradation.

2-4 Process Flow

The details of process are showed in Fig. 2.4:

1. Laser marking of 6-inch Si wafer

The 6-inch p-type silicon wafers were commercially obtained from Wafer Works

Corp. Then laser marker NEC SL473D2 was used to mark the wafers for label. To remove the particles produced by laser marking, an standard clean 1 (SC-1) which is the cleaning process of soaking wafers into solution containing $NH_4OH : H_2O_2 : H_2O = 1 : 4 : 20$ for 600 seconds at 75 ℃ was performed after laser marking.

2. Pre-furnace standard (STD) clean and wet oxide 150nm

   Before the wet oxidation, the wafers were performed the STD clean. The STD clean contains SC-1 and SC-2. The DI water rinse was performed before and after each clean. SC-2 is the cleaning process of soaking wafers into solution containing $HCl : H_2O_2 : H_2O = 1 : 1 : 6$ for 600 seconds at 75 ℃. After the STD clean, the wet oxidation of 150 nm SiO_2 isolation layer was grown at 980 ℃ by horizontal furnace.

3. Pre-furnace STD clean and in-situ doped N^+ poly Si 50 nm

   If this deposition process was subsequent to previous process, the STD clean could be skipped. Otherwise, after the pre-furnace STD clean, in-situ doped N^+ poly Si layer of 50-nm-thickness was formed by vertical furnace and used for bottom gate.

4. RTA process for dopant activation of in-situ doped N^+ poly Si bottom gate

   After in-situ doped N^+ poly Si formation, the HEATPAULSE AG-610i system was used for 900 ℃ rapid thermal annealing (RTA) process for 20 seconds. The RTA process was performed to activate PH_3 dopant of in-situ doped N^+ poly Si layer and made the grain size grow to reduce the gate resistance.

5. Bottom gate patterning

   The lithography process was performed by TEL CLEAN TRACK MK-8 for photo resist (PR) coating and development. The Canon FPA-3000i5+ Stepper was used for exposure. After the lithography process, the 50 nm poly-Si bottom gate was patterned by TCP 9400SE poly etcher. The Mattson AspenII Asher was used to remove the PR residue by O_2 plasma when patterning process was completed.

6. RCA clean and ALD 10 nm Al_2O_3 and HfO_2 gate dielectric layer respectively

Before gate dielectric layer was formed, the RCA clean was performed to remove contaminants and native oxide from wafer surface. Cambridge NanoTech Fiji-202 DC system was used to atomic layer deposition (ALD) process. There were two split conditions for gate dielectric layer: one was Al_2O_3 and another was HfO_2 layer. Trimethylaluminium (TMA) and H_2O were the ALD precursors for Al_2O_3 layer. Tetrakis(ethylmethylamino)hafnium (TEMAH) and H_2O were precursors for HfO_2 layer. Then each wafer put in a 8-inch chuck at 250 ℃. The deposition cycle was composed of one H_2O pulse and one TMA/TEMAH precursor pulse. The 10-seconds-wait and pumping were performed after each pulse to remove reaction byproducts and residual precursors. The ALD deposition rate were 0.99 Å per cycle for Al_2O_3 layer and 0.85 Å per cycle for HfO_2 layer respectively.

7. Horizontal furnace annealing for ALD Al_2O_3 layer

After ALD Al_2O_3 deposition, a 30 minutes, 700 ℃, N_2 annealing was performed to densify Al_2O_3 layer and decrease the gate leakage by horizontal furnace. The HfO_2 layer was not performed annealing process since high-temperature-annealing might cause HfO_2 agglomeration to increase gate leakage.

8. Bottom gate contact hole etching

After the I-line lithography process, the wafers were soaking in buffered oxide etchant (BOE) solution containing NH_4F : Hf = 6 : 1 for 10 seconds to etch the 10 nm Al_2O_3 layer. Then wafers were sonicated in acetone for 5 minutes to remove the residual photo resists.

9. CNT network formation by spin-coating method

The details of CNT solution preparation is described in section 2-3. The 1 mg CNT powder was dissolved in 40 ml DMF solution with 24-hours-socication. Then, using a burette to drop about 0.1 ml CNT solution and a 2-step spin-coating was

performed by Synrex 1-PM101D-R790 photo resist spinner. The first step was with rotation speed of 500 rpm for 10 seconds to make CNT solution spread on the wafer uniformly. The second step was with 2500 rpm rotation speed for 20 seconds to remove residual solution on the wafer. After the spin-coating, wafers were baked on the hot-plate for 120℃, 180 seconds to evaporate DMF residues which would affect device electrical characteristics.

The high rotation speed of second step would affect the number of CNTs on the device channel. The higher the rotation speed was, the less the number of CNTs were on the channel. Fig. 2-5 shows the SEM image of CNT coating 40 cycles on Al_2O_3 film. The CNT network was spread on the wafer without any aggregation. From the SEM image we can derive the coverage rate of CNT network is about 1% since the coverage area of single CNT is equal to 1.4 nm CNT diameter times CNT length. Fig. 2-5 also shows that the CNT length is ranged from 0.3 μm to 1.4 μm due to some broken CNTs caused by sonication.

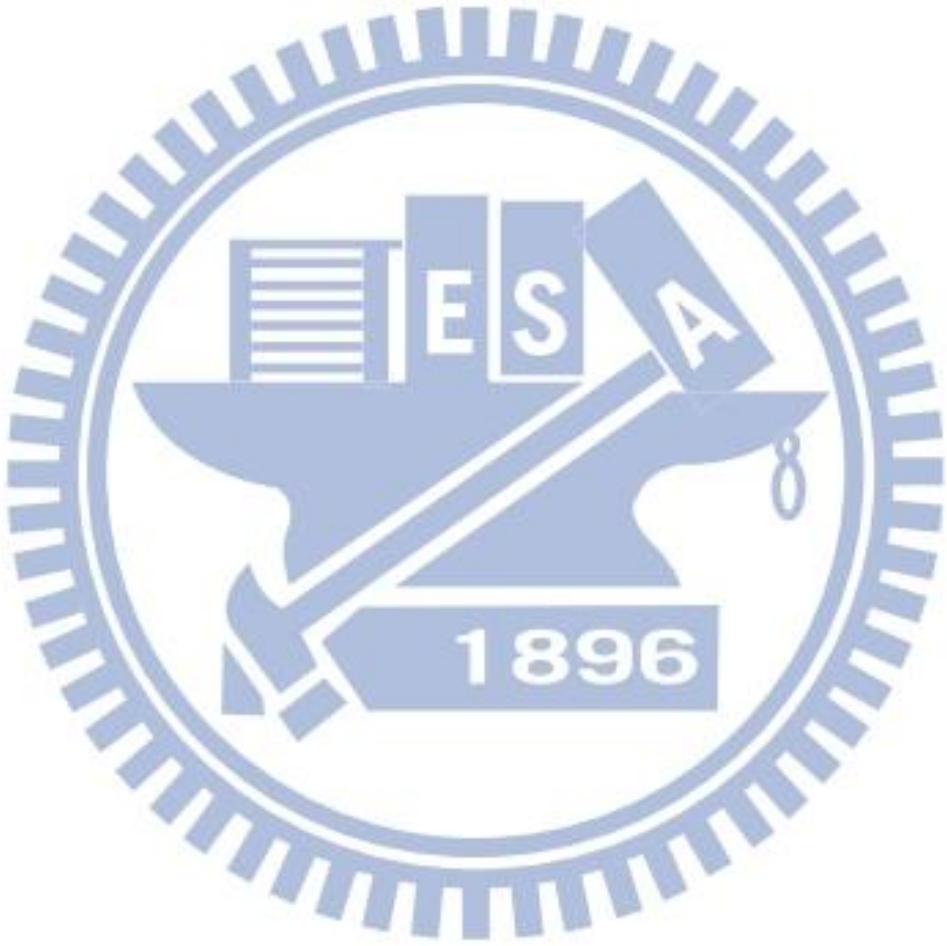
10. CNT stripe definition by O_2 plasma

The lithography process of CNT network was performed by I-line lithography system. The Anelva ILD-4100 Metal etcher was used to define the CNT stripes by O_2 plasma. The photoresists were covered on the device active region and then the O_2 plasma was used to remove CNTs which were not protected by photoresists. The CNT network patterned to CNT stripes would further define the channel region precisely. After the patterning process, the wafers were sonicated in acetone for 2 minutes to remove the residual photo resist.

11. 60 nm Pd source/drain patterning by sputter deposition and lift-off method

After the lithography process using I-line lithography system, the 60 nm palladium (Pd) source/drain were deposited by Ion Tech Microvac 450CB sputter system. The DC sputter process under Ar gas of 24.4 sccm was performed with

pressure 7.6 mbar. The deposition rate is 0.78 nm per minute with DC power of 17 W. The residual photo-resist and metal were sonicated in acetone for 10 seconds by lifted-off method. Then the whole process was finished.



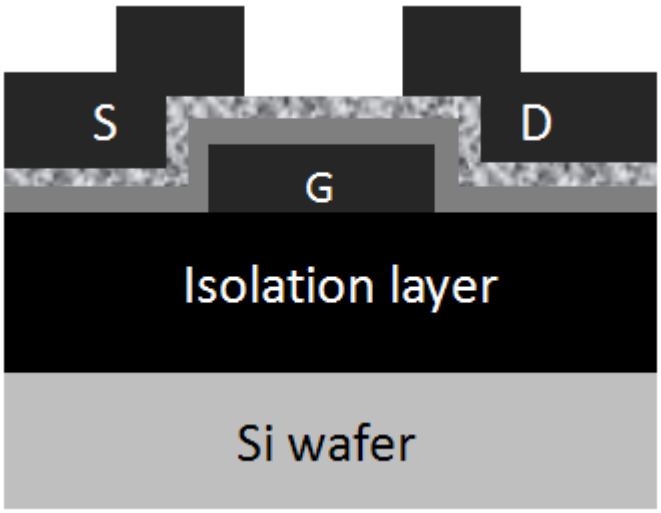


Fig. 2-1 Schematic cross-sectional view of the CNTN TFT along channel direction.

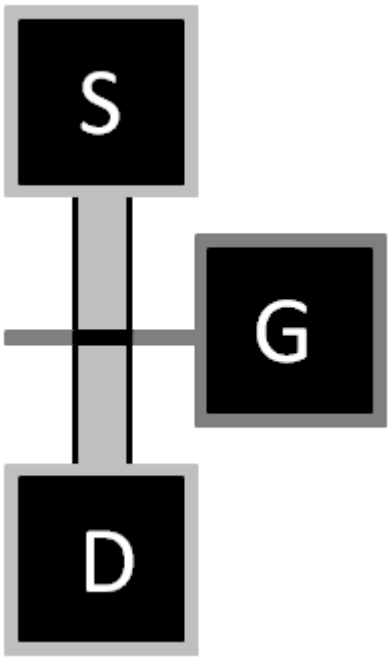


Fig. 2-2 Schematic top-view of the CNTN TFT.

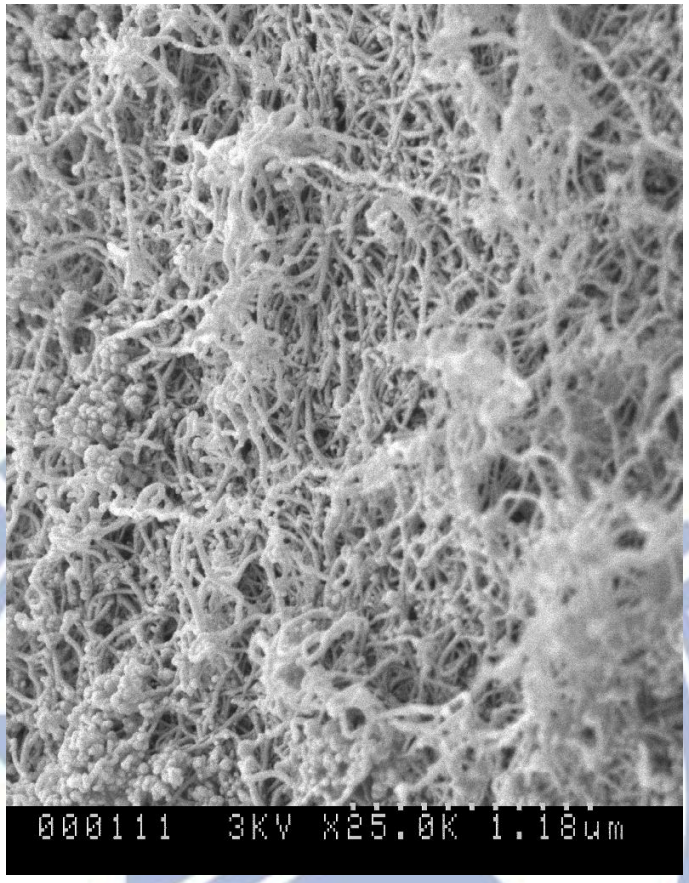


Fig. 2-3 SEM image of the AP-grade carbon nanotube provided by CarboLex Inc.

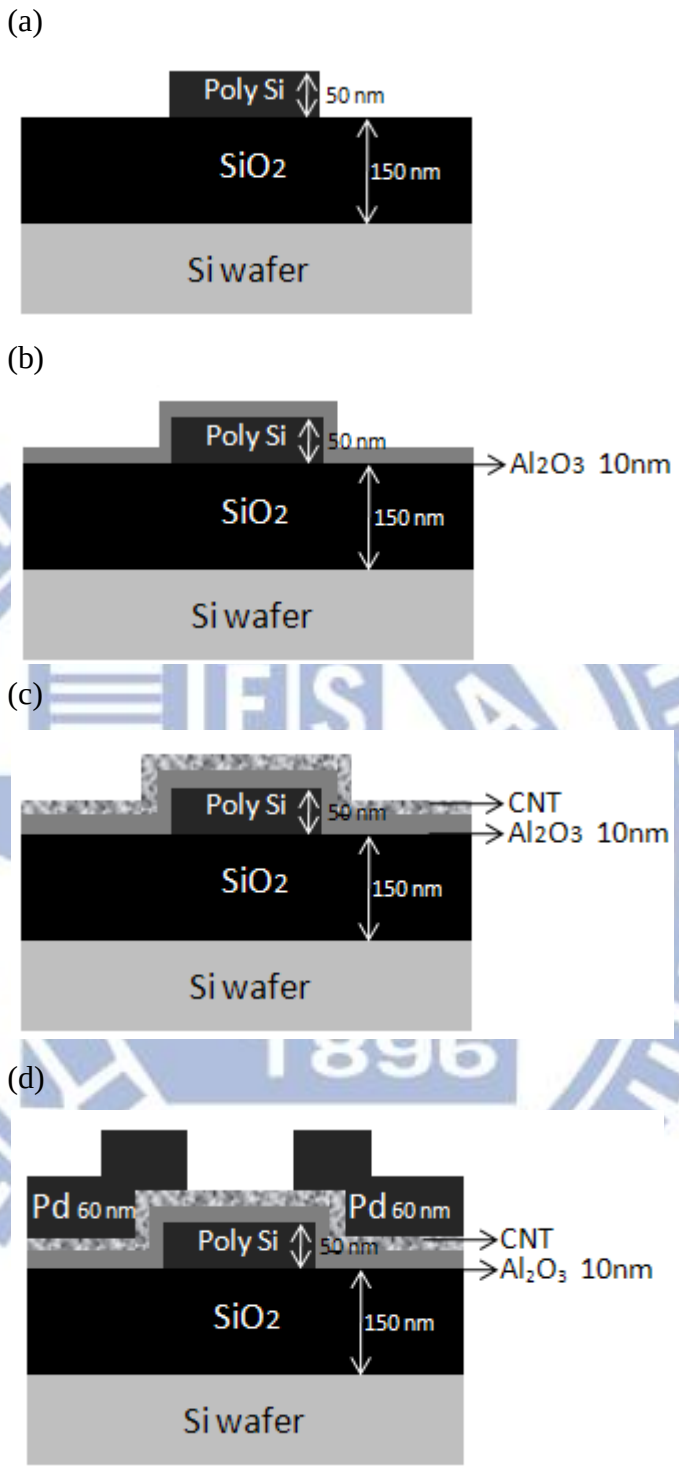
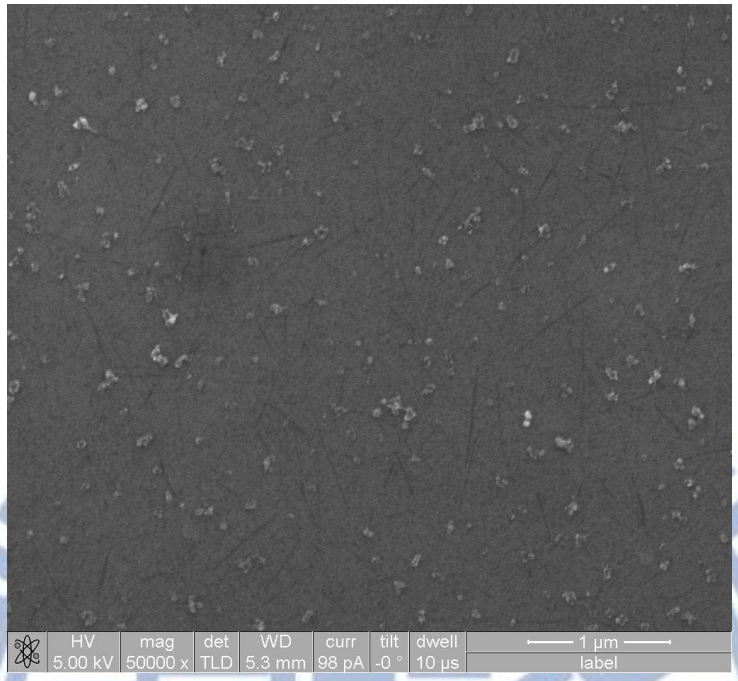


Fig. 2-4 Process flows of the CNTN TFT. (a) SiO_2 isolation layer and in-situ doped poly Si gate definition (b) ALD Al_2O_3 gate dielectric layer and furnace annealing for Al_2O_3 layer densification (c) Bottom gate contact hole etching and spin-coating CNT network (d) Pd source/drain formation by sputter deposition and lift-off method.

(a)



(b)

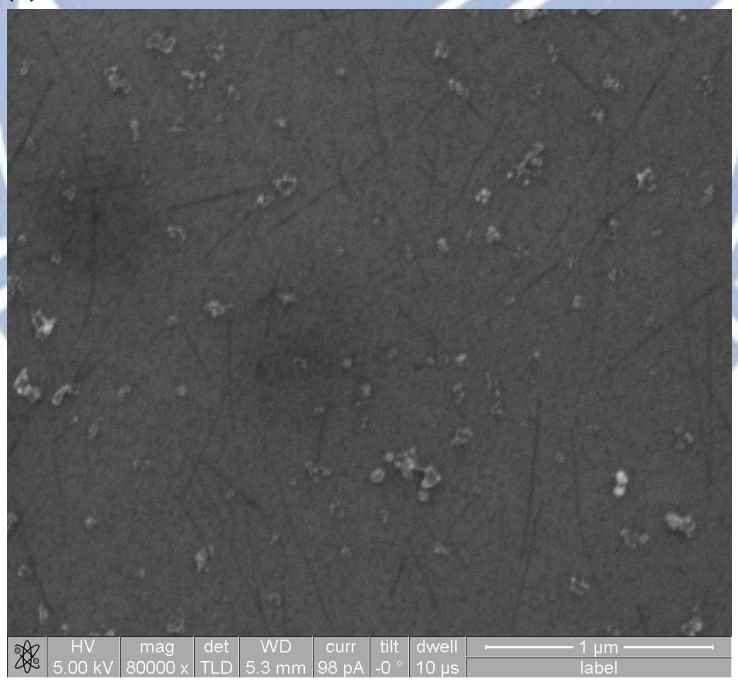


Fig. 2-5 SEM images of CNT coating 40 cycles on Al_2O_3 layer (a) 50k x magnification (b) 80k x magnification.

Chapter 3

Results and Discussion

3-1 Scanning Electron Microscopy (SEM) Analysis of CNT Networks

FEI Nova 200 Dual beam (focused ion beam and electron beam) System (FIB/SEM) was performed to observe the dispersion and coating density of CNT networks. The accelerate voltage is 5 kV. The dual beam FIB/SEM system is with high solution since pure metal would occur field emission in high electric field to enhance resolution limit.

The SEM images were used to analyze the effect of CNT coating density, average CNT length and coating surface types on CNT network coverage. In addition, the number of CNTs on device channel was also shown in SEM images.

Fig. 3-1a to 3-1d show the CNT networks on the active channel region with Al_2O_3 surface for 1-μm-long CNT coating density ranging from 20 to 60 cycles. The CNTs were dispersed without aggregation on Al_2O_3 film. By approximately counting the number of CNTs in the 3.2 μm × 2.5 μm channel area in Fig. 3-1a to 3-1c, the CNT density were 2.13, 3.75, and 6.5 CNTs/μm^2, respectively. Note that lighter CNTs (white CNTs) occur in the dense network for CNT coating density of 60 cycles in Fig 3-1d rather than dark CNTs shown in Fig 3-1a to 3-1c. For SEM analysis, the lighter images exhibit the higher conductivity. This suggests that increasing CNT density increases the electrical conduction in the CNT network.

For the SEM images of Fig. 3-1a to 3-1d, increasing CNT coating cycle would increase the number of CNTs and CNT conducting paths in the channel. In addition,

the catalyst particles and carbon residues increase with the increase of CNT coating density.

Besides the CNT density, the coating surface property is also a crucial factor to affect the CNT network dispersion. For the same concentration of CNT solution and spin condition, the CNT density is much lower on the HfO_2 surface (~ 0.63 CNT/μm^2) shown in Fig. 3-2a. The sparse network is due to the poor wet ability of HfO_2 film which also affects the electrical characterization discussed in section 3-3.

In Fig 3-2b and 3-2c, the long CNT networks with average CNT length of 15 μm were formed instead of short CNTs of 1 μm shown in Fig 3-1. The CNT conducting paths were formed up to tens of μm. Thus, the lower CNT coating density of 30 cycles was able to bridge source and drain in channel length L= 50 μm. However, the bundled CNTs rather than single CNTs occurred in Fig. 3-2(c) to affect the device electrical properties for long length CNTs.

Fig. 3-2d shows that there were a large number of CNTs on the substrate rather than on the bottom gate since the height of 50 nm between bottom gate and substrate would hinder CNTs on the channel during spin-coating method. The geometrical rise of bottom gate would decrease the CNT network density in the channel region and cause non-uniform CNT dispersion for devices with channel length L > 4 μm.

3-2 Effects of CNT Properties and Device Parameters - Al_2O_3 Gate Dielectric

The electrical characterization of CNTN TFTs was conducted in ambient condition using the probe station of Cascade Microtech Inc and Agilent 4156C semiconductor parameter analyzer. Device characteristics were measured and used to analyze device on-state current, off-state current, on/off ratio and effective field-effect

mobility in linear region.

This thesis studies the following effects on CNTN TFT device performance:

1. CNT density
2. Channel length dependence ranging from 0.4 to 14 μm
3. Channel width dependence ranging from 5 to 50 μm
4. Gate dielectric thickness
5. CNT length
6. Coating surface types including Al_2O_3 and HfO_2 gate dielectric layer

We measured 12 devices with same device dimension for each factor mentioned above to average the individual deviation of CNTN TFTs and then the statistical diagrams were performed to analyze each effect which affects device performance.

The gate voltage (V_g) swept from -4 V to 4 V for devices with 10 nm Al_2O_3 layer to obtain the I_d-V_g transfer characteristics at V_d= -0.1 V since the CNTN TFTs proposed in this thesis exhibit p-type behavior.

Fig. 3-3 to 3-6 show the Id-Vg characteristics of CNTN TFTs with various channel length L= 0.4 – 14 μm and fixed channel width W= 50 μm for CNT coating density varying from 20 to 60 cycles. The CNT density increases by increasing the number of spin-coating cycles of CNT solution.

The transfer characteristics are divided roughly into two cases, one extreme case is shown in Fig 3.3 with high on-state current of 10^{-5} A and low on/off ratio < 10, and another extreme case shown in Fig 3.6 with low on-state current of 10^{-8} A and high on/off ratio > 10^3. In between these two extreme cases, other transfer characteristics shown in Fig. 3-4 and 3-5 depend on the interaction between CNT coating density and channel length. CNTN TFTs with the same CNT coating density and device dimension could exhibit either metallic or semiconducting behavior since CNT conducting paths in channel were mixed with both metallic and semiconducting CNTs.

Once the conducting path contains one semiconducting CNT at least, the conducting path exhibits the semiconducting behavior with high on/off ratio.

3-2.1 Effect of CNT Density

In order to further analyze the effect of CNT density on on-state current and on/off ratio, the transfer characteristics measured in Fig. 3-3 to 3-6 were also performed to statistical diagrams of on-state current and on/off ratio against various CNT coating density at channel length L= 0.4-7 μm shown in Fig. 3-7 and 3-8. Fig. 3-7(a)-(d) show that increasing CNT coating density results in the increase of on-state current for all channel length.

For channel length L= 0.4 μm, Fig. 3-7(a) and 3-8(a) show the on-state current and on/off ratio are plotted against various CNT coating density. The on-state current increases with CNT coating density increasing from 20 to 60 cycles. Larger variation of on-state current was found for CNT coating density of 20 cycles due to sparse CNT conducting paths. The device on/off ratio is not affected by CNT coating density since channel length of L= 0.4 μm < average CNT length of 1 μm, a single CNT could bridge the channel. Once a metallic CNT connects the channel, the device would exhibit metallic behavior at on/off ratio < 10 no matter other conducting paths are semiconducting or not. Although metallic conducting paths could contribute to high on-state current, metallic CNTs also increase off-state current to cause low on/off ratio.

For channel length L= 1.4 μm, Figs. 3-7(b) shows the on-state current vs. CNT coating density. Channel length L= 1.4 μm is larger than average CNT length of 1 μm. Therefore, the conducting paths in channel need more than one CNT to form. Increasing CNT coating density from 20 to 60 cycles results in the increase of on-state

current. Increasing CNT density achieves high on-state current by increasing the number of CNT conducting paths in the channel. Note that the on-state current for CNT coating density of 30 cycles exhibits large deviation since devices exhibit either metallic behavior with high on-state current or semiconducting behavior with low on-state current shown in Fig 3-4(b). In addition, increasing the CNT coating density reduces the on-state current variation.

In Fig. 3-8(b), for L= 1.4 μm, the device on/off ratio is in the range from 10 to 10^3 with CNT coating density of 20-30 cycles. Since the channel length > average CNT length, each conducting path contains more than one CNT. For lower CNT coating density, if there is at least one semiconducting CNT in each conducting path, the device would exhibit the semiconducting behavior to enhance the on/off ratio to 10^3. In contrast, the on/off ratio suddenly drops to 10 for CNT density > 30 cycles. This means that at least one conducting path in the channel contains all metallic CNTs to decrease the on/off ratio.

Fig. 3-9(a) plots the on-state current vs. on/off ratio for L= 1.4 μm to determine which CNT coating density is appropriate for device with high on-state current and good on/off ratio which on/off ratio > 100 is acceptable in this thesis. The blue line shown in Fig. 3-9(a) indicates that on/off ratio = 100. The on/off ratio < 10 could be improved by 2 orders of magnitude by using adapted electrical breakdown method discussed later in section 3-6. Thus, CNT coating density in the range of 20 and 30 cycles is the proper one.

For channel length L= 4 μm, Figs. 3-7(c) and 3-8(c) show the on-state current and on/off ratio vs. various CNT coating density. The on-state current also increases with CNT coating density increasing from 30 to 60 cycles. The conducting paths were not formed for CNT coating density of 20 cycles. Increasing CNT coating density first results in increase of on/off ratio, whereas on/off ratio drops when CNT density > 40

cycles. This suggests the metallic CNT density exceeds percolation threshold to let device exhibit metallic behavior for CNT coating density of 60 cycles.

Fig 3-9(b) shows the on-state current and on/off ratio as a function of CNT density for channel length L= 4 μm. It is noticed that the electrical breakdown method is not suitable for devices with L> 4 μm since that devices with long channel length require higher stress bias approaching breakdown voltage to burn out metallic conducting paths. High stress voltage reduces the yield of devices applied electrical breakdown method. Although devices for CNT density of 60 cycles achieve high on-state current, some devices at on/off ratio < 100 exist. Thus, the appropriate CNT density for L= 4 μm is 40 cycles with high on-state current and acceptable on/off ratio.

For channel length L= 7 μm, Fig. 3-7(d) shows that the on-state current increases with CNT coating density increasing from 40 to 60 cycles. The conducting paths were not formed for CNT density of 20 and 30 cycles. Fig. 3-8(d) shows that although the device on/off ratio decreases slightly with increasing CNT density for L= 7 μm, note that the on/off ratio still remains > 10^3. This suggests that the metallic CNT conducting paths are not able to connect the channel even for CNT density up to 60 cycles. Fig 3-9(c) shows the on-state current and on/off ratio as a function of CNT density. The appropriate CNT coating density for L= 7 μm is 60 cycles with higher on-state current and on/off ratio > 100.

For CNT coating density of 20 cycles, the maximum conducting channel length is only L= 1.4 μm. In this case, the CNT network is too sparse to form the CNT conducting paths and then reduce the conducting channel length. At higher CNT coating density, more conducting paths are formed which result in increase of conducting channel length. For CNT coating density of 30, 40, and 60 cycles, the maximum CNT conducting path in the channel are 4, 7, and 14 μm, respectively.

3-2.2 Effect of Channel Length

For CNT coating density of 30 cycles, Fig. 3-10(a) and 3-10(b) show on-state current and on/off ratio plotted against channel length. For the short channel length (L< 1.4 μm) which is comparable to average CNT length, a single metallic CNT can directly connect the channel to achieve high on-state current and low on/off ratio. The high on-state current is achieved at the cost of high off-state current since metallic CNTs could not be fully depleted by gate bias and then increase off-state current.

On-state current decreases with channel length increasing shown in Fig. 3-10(a). If device channel length is longer than the average CNT length (L> 1.4 μm), the current flow from source to drain would be through the series of CNTs and junctions between CNTs to decrease on-state current. The electrical behavior of CNT conducting paths is a combination of three effects: the field dependence of CNT itself, the ohmic contact at CNT/S/D junction, and the intersection between two cross CNTs. The electrical conductance of intersection between two semiconducting CNTs or two metallic CNTs is only $0.1e^2/h$. However, the intersections of semiconducting CNT and metallic CNT form the Schottky barriers to further reduce the on-state current due to the increase of barrier for hole transport.

Note the on-state current decreases nonlinearly with channel length increasing. Fig. 3-10(a) shows that the channel length of 0.4 μm increases 10 times to 4 μm, but on-state current decreases more than 100 times from 10^{-6} to 10^{-8} A. The nonlinear decreasing behavior supposed to be due to the series of Schottky junctions and non-uniform coverage of CNT network on long channel length. The geometry rise of bottom gate would hinder the CNTs coated on device channel than planar back gate structure. Most of CNTs are coated on substrate rather than active region on bottom

gate. Thus, the longer channel length would need more CNTs to bridge the channel and then further reduce the number of CNT conducting paths in channel and on-state current.

Increasing channel length results in on/off ratio improvement in Fig. 3-10(b). The devices exhibit an on/off ratio > 100 for channel length > 1.4 μm. This means metallic CNT conducting paths are not able to connect the long channel. Note that the small variation of on/off ratio occurs at L= 0.4 μm since that increasing channel length increases the mixture of semiconducting and metallic CNTs in the conducting paths and then increases the complexity of CNT conducting path.

On-state current is plotted against off-state current as log-log plot in Fig. 3-10(c) to determine the channel length dependence on device performance. The diagonal presents the on/off ratio= 1 which on-state current is equal to off-state current. Increasing channel length makes the difference between on-state current and off-state current more obvious. On-state current vs. on/off ratio at various channel length is shown in Fig. 3-10(d). There are two kinds of electrical characteristics. One is devices with high on-state current but low on/off ratio, and another is devices with lower on-state current but high on/off ratio.

For CNT coating density of 40 and 60 cycles, devices are shown in Fig. 3-11 and 3-12, respectively. Increasing channel length also results in the decrease of on-state current. However, on/off ratio enhancement is achieved by increasing channel length. In contrast to lower CNT density (30 cycles), increasing CNT coating density increases the maximum conducting paths. Fig. 3-11(a) shows the conducting channel length is up to 7 μm for CNT coating density of 40 cycles. On the other hand, the cconducting channel length is up to 14 μm for CNT density of 60 cycles in Fig. 3-12(a), but note that the variation of on-state current for L= 14 μm is larger than other dimension due to non-uniform coverage of CNT network. Fig. 3-11(b) shows

that devices with channel length L> 4 μm are at on/off ratio > 100 for CNT density of 40 cycles, whereas Fig. 3-12(b) shows devices with L> 7 μm are at on/off ratio > 100 for CNT density of 60 cycles. That means increasing CNT coating density would increase the channel length at acceptable on/off ratio to avoid metallic CNT conducting paths connecting the channel.

Fig. 3-13 shows the brief summary of percolation threshold and metallic percolation threshold against channel length ranging from 0.4 to 14 μm. Percolation threshold is the critical CNT density for the beginning of formation of conducting path in the channel no matter it is semiconducting or metallic. Metallic percolation threshold is the CNT density for the metallic conducting path formation. As CNT density is above metallic percolation threshold, the devices exhibit metallic behavior. In addition, if devices exhibit semiconducting behavior, the yield is lower than 100%. Yield is defined as devices which channels conduct are divided by all devices measured. Since CNT density is not high enough to let all measured devices conduct, the yield is lower than 100%. It is the trade-off of random CNT network TFTs between 100% yield and metallic path formation.

Fig. 3-14 shows the 3D diagram of on-state current- CNT density- channel length and on/off ratio- CNT density- channel length to summarize the interaction between channel length and on/off ratio.

3-2.3 Effect of Channel Width

For devices with channel length L= 0.4 μm shown in Fig. 3-15(a), the on-state current decreases approximately in proportion to the channel width varying from 5 to 50 μm. Decreasing channel width results in reduction of the number of conducting paths in the channel, which decreases the on-state current. The on-state current scaling

ratio is defined as a quotient of on-state current for two different channel widths. In idea case, the decreasing on-state current is in proportion to channel width. There is only a small deviation (~4%) of on-state current scaling ratio for devices with L= 0.4 μm due to non-uniform CNT network coverage. Since one CNT could bridge the channel for channel length L= 0.4 μm, the non-uniform CNT coverage has weak effect on the error of on-state current scaling ratio.

Fig. 3-15(b) shows that for CNT coating density of 20 cycles, decreasing channel width to 5 μm strongly enhances on/off ratio up to 10^4. Although decreasing channel width decreases on-state current, it also decreases the number of metallic conducting paths to improve the on/off ratio for low CNT density < 30 cycles. But note that the effect of channel width becomes weak for short channel length L= 0.4 μm and high CNT coating density > 40 cycles since metallic conducting paths dominant device behavior.

For the devices with channel length L= 1.4 μm shown in Fig. 3-16(a), devices with channel width W= 5 μm could not form conducting paths for CNT density of 20 cycles. Increasing channel length affects strongly the deviation of on-state current scaling ratio ~16%. This suggests the effect of non-uniform coverage becomes more serious with the increase of channel length. On the other hand, when channel width reduces to W= 5 μm, obvious on/off ratio improvement is shown in Fig. 3-16(b) for CNT coating density varying from 30 to 60 cycles.

For the devices with channel length L= 4 and 7 μm shown in Fig. 3-17(a) and 3-16(a), respectively. Decreasing on-state current is not proportion to the decrease of channel width. The effect of channel width on on-state current becomes weaker with the increase of channel length since long channel length would make CNT conducting paths hard to form in the channel. It is noticed that for channel length L> 4 μm, on/off ratio remains a certain value in Fig. 3-17(b) and 3-16(b).

Fig. 3-19 shows on-state current is plotted against on/off ratio for various CNT coating density at varying channel length and fixed channel width W= 20 μm. Compare to Fig. 3-9 for devices with channel width W= 50 μm, the appropriate CNT coating density with high on-state current and on/off ratio > 100 comes to the same conclusion when channel width decreases from 50 to 20 μm. However, when channel width further decreases to W= 5 μm, the appropriate CNT coating density is varied to 40 cycles for L= 1.4 μm shown in Fig. 3-20(a) rather than 30 cycles shown in Fig. 3-19(a). This means channel width also affects the appropriate CNT density.

Table 3-1 shows the summary of optimized CNT coating density for channel length ranging from 1.4 to 7 μm and channel width varying from 5 to 50 μm.

3-2.4 Effect of Gate Dielectric Thickness

In this thesis, the gate voltage (V_g) swept from -2.5 V to 2.5 V for devices with 5 nm Al_2O_3 gate dielectric in contrast to operate voltage between -4 V and 4 V for devices with 10 nm Al_2O_3 gate dielectric. Reducing gate dielectric thickness results in lower operate voltage which contributes to low power consumption.

Fig. 3-21 and 3-21 show on-state current and on/off ratio vs. CNT coating density with various channel length to determined the gate dielectric layer thickness dependence of device performance. The CNT density and channel length dependence of on-state current and on/off ratio of 5-nm-gate dielectric thickness devices are the same with 10-nm-gate dielectric thickness devices. However, the effect of reducing gate dielectric thickness is not obvious on on-state current for devices with 5-nm-gate dielectric thickness. Fig. 3-21 shows decreasing gate dielectric thickness from 10 to 5 nm would not increase on-state current monotonously due to non-uniform CNT networks coverage and variation of CNT solution concentration. The geometric rise of

bottom gate would hinder CNTs coated on the channel and then cause non-uniform CNT coverage. In addition, since the 24-hours long-period sonication performed to separate the tangled CNT bundles might damage and shorten CNTs, new CNT solution was fabricated for devices with 10 nm and 5 nm gate dielectric, respectively. The inaccuracy of electronic scale contributes to variation of CNT solution concentration.

Although the effect of reducing gate dielectric thickness is not obvious, Fig. 3-23(a)-(c) shows that the appropriate CNT coating density with higher on-state current and acceptable on/off ratio is CNT coating density of 30, 40, and 60 cycles for device with L= 1.4, 4, and 7 μm, respectively, which leads to the same conclusions of devices with Al_2O_3 film of 10 nm. This suggests that devices with Al_2O_3 gate dielectric of 5 and 10 nm both have the same CNT density and channel length dependence of device performance.

3-2.5 Effect of CNT Length

For devices fabricated with CNT network consisting of average CNT length of 15 μm shown in Fig. 3-24, the maximum conducting channel length is up to 50 μm. Increasing CNT coating density from 30 to 60 cycles results in 10 times increase of on-state current. In contrast to the same size of devices coated with 1-μm-long CNTs, on-state current of devices coated with 15-μm-long CNT is 2~3 order of magnitude higher. Longer CNTs could reduce the number of CNT intersections and increase the contact area of each CNT to increase on-state current significantly. It is much easier to form dense conducting paths in the channel with less number of long CNTs. However, since a few of CNTs can bridge the channel, the network exhibits metallic behavior even at low CNT coating density of 30 cycles. In order to achieve semiconducting

behavior, CNT coating density needs to be lower than 20 cycles.

3-3 Effects of CNT Properties and Device Parameters - HfO_2 Gate Dielectric

The device performance of CNTN TFT with HfO_2 gate dielectric of 10 nm was shown in Fig. 3-25 and 3-25. To determine coating surface dependence of on-state current and on/off ratio between HfO_2 and Al_2O_3 gate dielectric, Fig. 3-25(a) shows that on-state current of devices with HfO_2 film is 7 times lower than devices with the same dimension and Al_2O_3 film. In addition, the maximum conducting channel length is only 1.4 μm even for CNT coating density up to 60 cycles showed in Fig. 3-26. This suggests the poor wet ability of HfO_2 surface attributes to decrease the coverage area of CNT networks and the number of CNT conducting paths, which are also determined by SEM image shown in Fig. 3-2(a). In contrast, due to the poor wet ability of HfO_2 surface, in Fig. 3-2(b) the devices exhibit semiconducting behavior at channel length L= 0.4 μm, which are not shown for devices with same dimension and Al_2O_3 film. It is noticed that high performance of devices with on-state current of 10^{-6} A and on/off ratio of 10^8 are obtained at L= 0.4 μm, W= 50 μm and 10 nm thickness HfO_2 layer for CNT coating density of 40 cycles.

For channel length L= 1.4 μm, Fig. 3-26(a) shows that the variation of on-state current is larger than devices with Al_2O_3 gate dielectric due to low coverage of CNT network. The lower on-state current is also obtained for devices with L= 1.4 μm and 10 nm thickness HfO_2 layer. In Fig. 3-26(b), on/off ratio is improved significantly for devices with HfO_2 layer rather than devices with Al_2O_3 layer since a single CNT would not form conducting path and low CNT coverage results in the decrease of metallic conducting paths. Table 3-2 shows the summary of following effects

including CNT density, CNT length, channel length, channel width, gate dielectric thickness and different coating surface on device performance.

3-4 Simulation of Percolating CNT Networks

We performed Monte Carlo simulation to compute the percolation threshold of random CNT networks with various CNT density and device dimension. Here we performed the 1-μm-long "sticks" to approach to CNTs. A two-dimensional random CNT network was generated by using random number generators. This random number generator would generate a set of random numbers between 0 and 1 according to uniform probability. The generation result of random numbers was different each time. There were three array sets of random numbers to consist of CNT network: random parameter sets x, y, and θ to present x-axis, y-axis position and rotation angle of CNTs, respectively. Each array size was equal to the number of CNTs. The starting point of a CNT stick could be defined from a random set of (x, y) position and then this point would extend 1-μm-long along a random rotation angle to generate a CNT "stick". Repeating the calculation described above would generate a random percolation CNT network.

The percolation threshold was the specific CNT density defined as the connection probability is equal to 99%. The connection probability was the ratio of devices with connected source/drain to total devices. The CNT density was defined as the number of CNTs divided by channel area and each CNT density increased with a step of 25 CNTs. In order to determine the percolation threshold for channel length ranging from 1.4 to 4 μm, 100 devices were simulated for each channel length and CNT density.

The simulation results are shown in Fig. 3-27. Fig. 3-27(a) shows that when the

number of CNTs is equal to 125, the connection probability exceeds 99% for device dimension of L= 1.4 μm and W= 50 μm. This means the percolation threshold is 125 (CNTs) divided by 70 μm^2 (channel area) = 1.79 CNTs/μm^2.

In the same way, Fig. 3-27(b) and 3-26(c) show that the percolation threshold are 550 (CNTs)/ 200 μm^2 = 2.75 CNTs/μm^2 and 1050 (CNTs)/ 350 μm^2 = 3 CNTs/μm^2 for devices of fixed W= 50 μm, L= 4 μm and 7 μm, respectively. Increasing channel length results in the increase of percolation threshold.

Note that SEM images in Fig. 3-1 shows the CNT density are 2.13, 3.75, and 6.5 CNTs/μm^2 for CNT coating 20, 30 and 40 cycles, respectively. In addition, section 3-2.1 shows the maximum CNT conducting channel length are 1.4, 4, and 7 μm for CNT coating density of 20, 30, and 40 cycles by electrical characterization, respectively. Combine these two results above and then we can obtain that the minimal CNT density are 2.13, 3.75, and 6.5 CNTs/μm^2 for conducting path formation in channel length L= 1.4, 4, and 7 μm, respectively.

In contrast to the simulation results of 1.79, 2.75, and 3 CNTs/μm^2 for channel length L= 1.4, 4, and 7 μm, the simulation results of percolation threshold are lower than experimental results determined by SEM images. The variation of CNT length might affect the experimental results to deviate from simulation ones since 24-hour-sonication of CNT solution might shorten the CNTs. In this thesis, we consider CNT segments as single CNTs to determine the CNT density shown in Fig.3-1. Thus, deviation of percolation threshold exists between simulation and experimental results. Table 3-3 shows the comparison of simulation and experimental percolation threshold for channel length varying from 1.4 to 7 μm.

3-5 Channel Length and Width Dependence of Mobility

In this thesis, the effective field-effect mobility was defined as $u = \frac{g_{m,max} L}{W C_{ox} V_d}$ at V_d= -0.1 V, where L and W are the device channel length and width. $g_{m,max}$ is the maximum g_m defined as $\frac{\partial I_d}{\partial V_g}$. The parallel-plate gate capacitance $C_{ox} = \frac{\varepsilon}{d}$ was used, where ε is gate dielectric constant and d is the gate dielectric thickness. The dielectric constant of Al_2O_3 and HfO_2 were 8 and 13 [83], respectively. Devices were operated at linear region at V_d= -0.1 V.

The effective field-effect mobility is ranging from 0.01 to 2.7 cm^2/Vs shown in Fig. 3-28 and 3-28, which is much better than the mobility of organics [84-85]. The low field-effect mobility results from the geometry rise of bottom gate which makes CNT hard to coat on the channel and then decreases the number of CNT conducing paths in the channel. In addition, a large number of Shottky barriers between CNT intersections also decrease field-effect mobility.

Note that the width W calculated in field-effect mobility is the channel width rather than the sum of width of CNT conducting paths. Since the surface coverage of CNT networks is lower than 1%, the values of mobility we calculated need to multiply 100 times to compare to typical TFT device performance. The normalized field-effective mobility is in a range of 1-270 cm^2/Vs, which is much lower than mobility of devices with single CNT as channel [36]. It is due to the series Schottky barriers between CNT intersections which limit the mobility.

In order to determine the channel length dependence of field-effect mobility, in Fig. 3-28, mobility is plotted against channel length for devices with channel width W= 50 μm and Al_2O_3 film of 10 nm for CNT coating density ranging from 20 to 60 cycles. It is shown that increasing channel length decreases mobility.

The mobility of devices with channel width W= 5 μm was shown in Fig. 3-29.

Decreasing channel width results in the mobility increase. In contrast to mobility of devices with channel width W= 50 μm shown in Fig. 3-28, mobility of devices with channel width W= 5 μm is twice rather than 10 times larger since decreasing channel width decreases the number of conducting paths which attributes to the decrease of on-state current and then makes the mobility enhancement not obvious.

For mobility of devices with 10 nm HfO_2 film shown in Fig. 3-30, mobility is twice smaller than devices with 10 nm Al_2O_3 film due to the poor surface wet ability and higher Cox of HfO_2 film.

3-6 On/Off Ratio Improvement by Adapted Electrical Breakdown Method

The CNT network consists of 2/3 semiconducting CNTs and 1/3 metallic CNTs, once the density of metallic CNTs exceeds the percolation threshold of conducting path formation, the CNT network exhibits metallic behavior. In order to achieve high on-state current with good on/off ratio, the number of metallic conducting paths needs to be reduced. Therefore, we used adapted electrical breakdown method to apply a high stress voltage (V_d > 5 V) to burn out the metallic CNTs and then reduce the off-state current. In the meantime, the large positive gate bias (Vg= 5 V) is also applied to turn off the semiconducting CNTs and avoid damaging semiconducting CNTs. The maximum stress voltage was decided by 1 V below the breakdown voltage of semiconducting CNT when applying the large positive gate voltage. Note that when stress voltage is higher than breakdown voltage of semiconducting CNT, the significant degradation of on-state current occurs. Thus, the precise control of stress voltage is crucial.

Fig. 3-31 shows I_d-V_g curves before and after applying adapted electrical

breakdown method to devices with different channel length L= 0.4 and 1.4 μm, fixed channel width W= 50 μm, and Al_2O_3 film of 5 nm for CNT coating density of 60 cycles. On/off ratio was improved by 2 orders of magnitude by adapted electrical breakdown method. The decrease of on-state current (< 1 order of magnitude) is due to reduction of metallic conducting paths contributing to high on-state current. In addition, comparing Fig. 3-31(a) and 3-30(b), it is found that increasing channel length increases stress bias V_d from 6 V to 11 V to burn out the metallic conducting paths.

Fig. 3-32 shows that increasing gate dielectric thickness from 5 nm to 10 nm results in on/off ratio improvement larger than 2 orders of magnitude (up to on/off ratio ~ 10^5). Increasing gate dielectric thickness increases breakdown voltage. Then increasing stress voltage (up to 13 V) could burn out more metallic CNT conducting paths to improve the on/off ratio.

It is noticed that the electrical breakdown method only applied to devices with short channel length (L< 4 μm) which metallic conducting paths are easy to form. When channel length increases to L> 4 μm, the devices all exhibit semiconducting behavior without applying electrical breakdown method in this thesis. Channel length L= 4 μm is the critical length which is also not suitable for electrical breakdown method since high stress voltage for devices with L= 4 μm makes Vgd or Vgs high enough to cause gate leakage.

Table 3-1 Summary of optimized CNT coating density for channel length ranging from 1.4 to 7 μm and channel width varying from 5 to 50 μm.

Channel length L (μm)		1.4	4	7
Optimized CNT coating cycle	W= 20 & 50 μm	30	40	60
	W= 5 μm	40	60	X

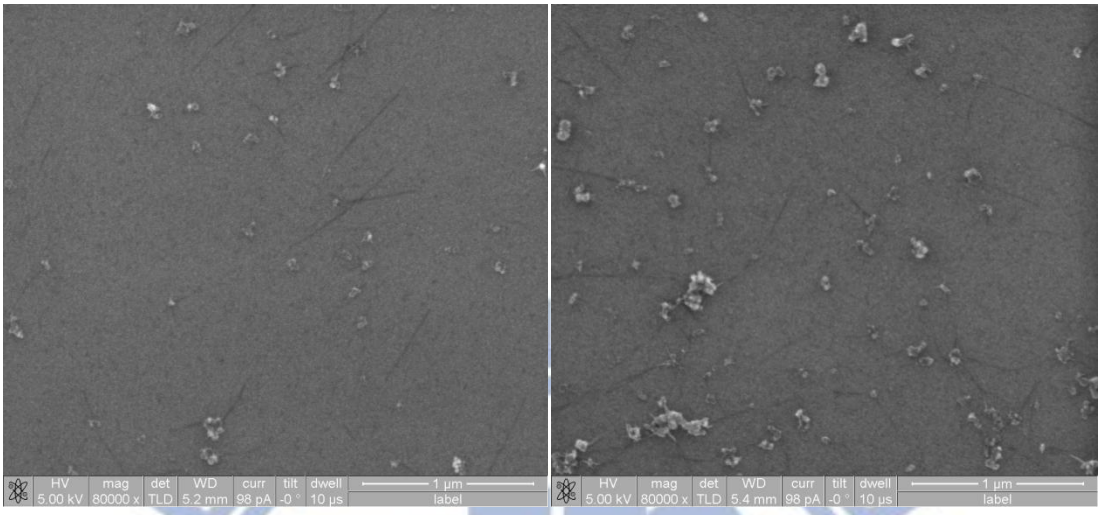
Table 3-2 Summary of effects of CNT solution properties and device parameters on on-state current and on/off ratio.

Factor	CNT density ↑	CNT length ↑	Channel length L ↑	Channel Width ↓	Gate dielectric thickness ↑	Coating surface
Ion	↑	↑↑	↓	↓	The effect is weak (for 5 nm and 10 nm Al_2O_3)	Al_2O_3 > HfO_2
On/off ratio	Metallic percolation threshold > percolation threshold → ↓		↑	↑ (effective for L~ CNT length)		HfO_2 > Al_2O_3

Table 3-3 Comparison of simulation and experimental percolation threshold for channel length varying from 1.4 to 7 μm.

Channel length L (μm)		1.4	4	7
Percolation threshold ($CNTs/\mu m^2$)	Experiment	2.13	3.75	6.5
	Simulation	1.79	2.75	3

(a) (b)



(c) (d)

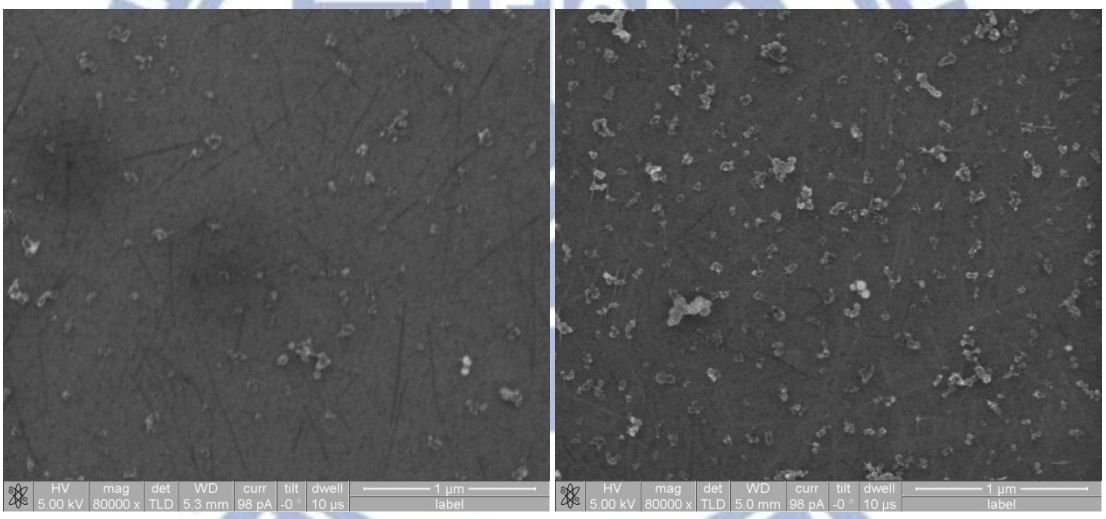
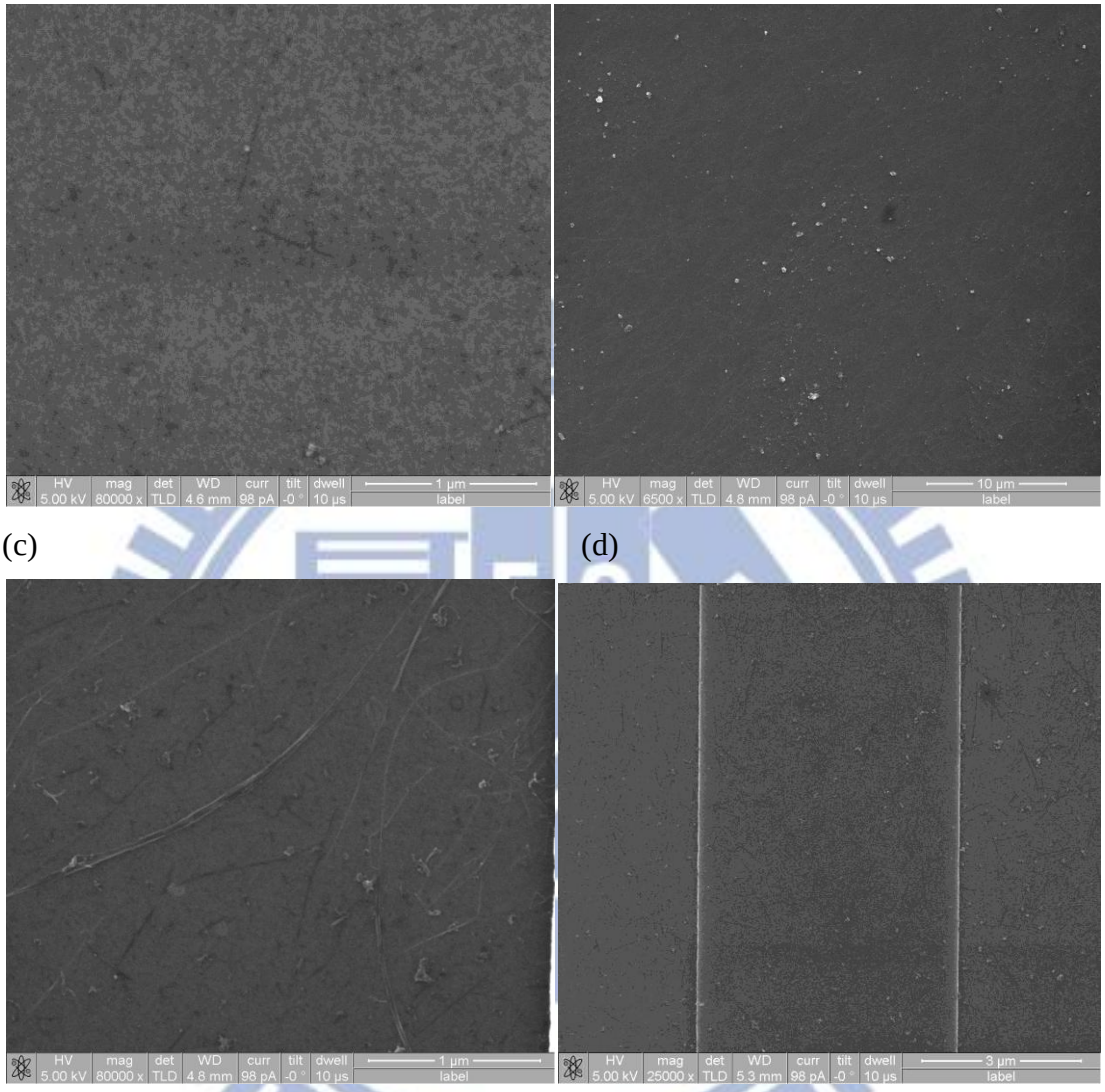


Fig. 3-1 SEM images of CNT networks with CNT coating density ranging from 20 to 60 cycles on Al_2O_3 film (a) 20 cycles (b) 30 cycles (c) 40 cycles (d) 60 cycles, increasing CNT coating cycles results in the increase of CNT density.

(a) (b)



(c) (d)

Fig. 3-2 (a) SEM image of CNT network with CNT coating 60 cycles on HfO_2 film. The poor wet ability of HfO_2 film attributes low CNT network coverage. (b)(c) SEM images of CNT network with 15-µm-long CNTs coating 30 cycles on Al_2O_3 film. It is noted that the CNT bundles are found. ((b) 6.5k x and (c) 80k x magnification) (d) A large number of CNTs were coated on the substrate rather than the bottom gate due to geometrical rise.

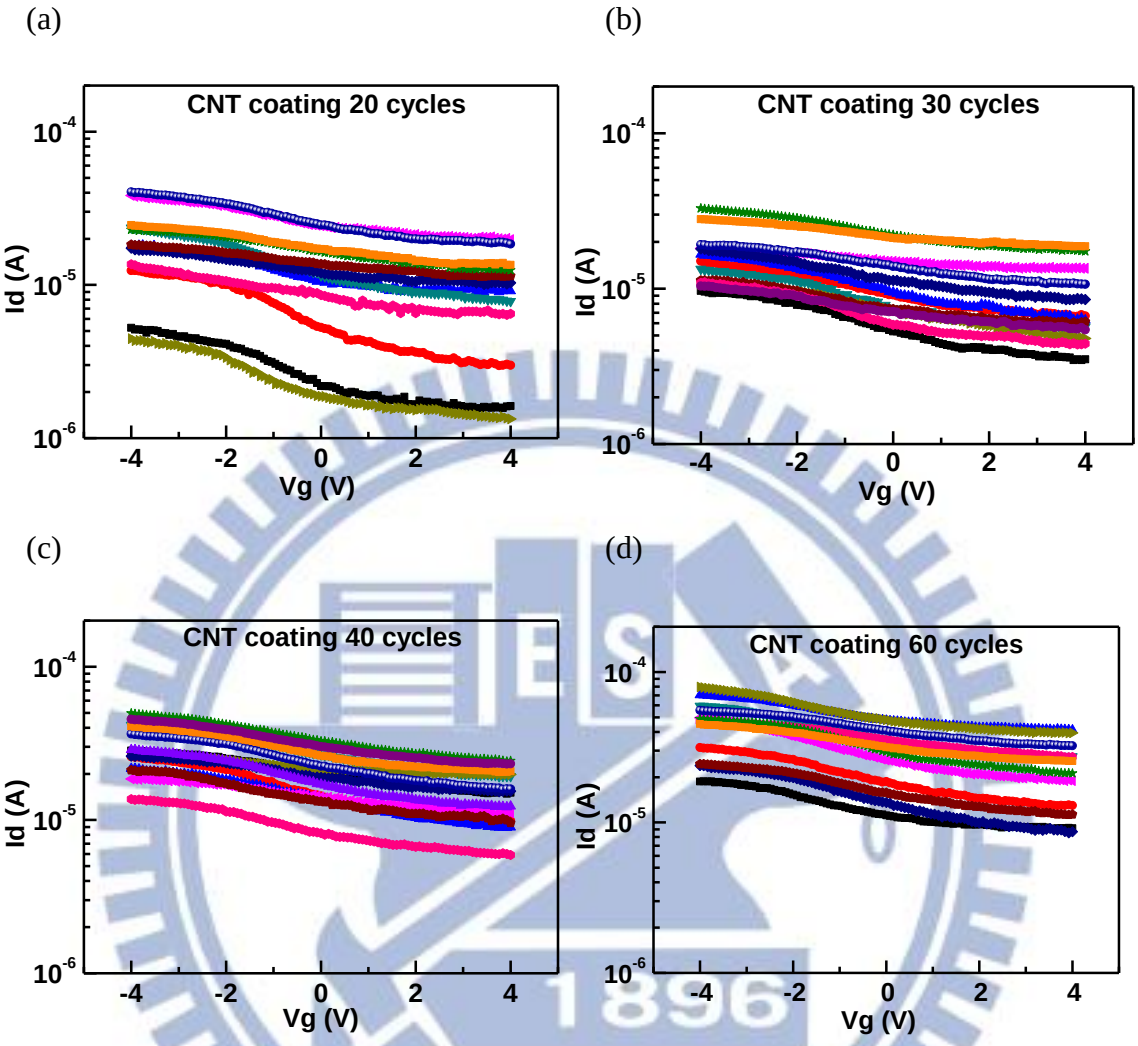


Fig. 3-3 Transfer characteristics (I_d vs. V_g) at V_d= -0.1V for devices with 10 nm Al_2O_3 gate dielectric layer (device dimension L= 0.4 μm and W= 50 μm) with CNT coating density varying from 20 to 60 cycles (a) CNT coating 20 cycles (b) CNT coating 30 cycles (c) CNT coating 40 cycles (d) CNT coating 60 cycles. All devices exhibit metallic behavior on this condition.

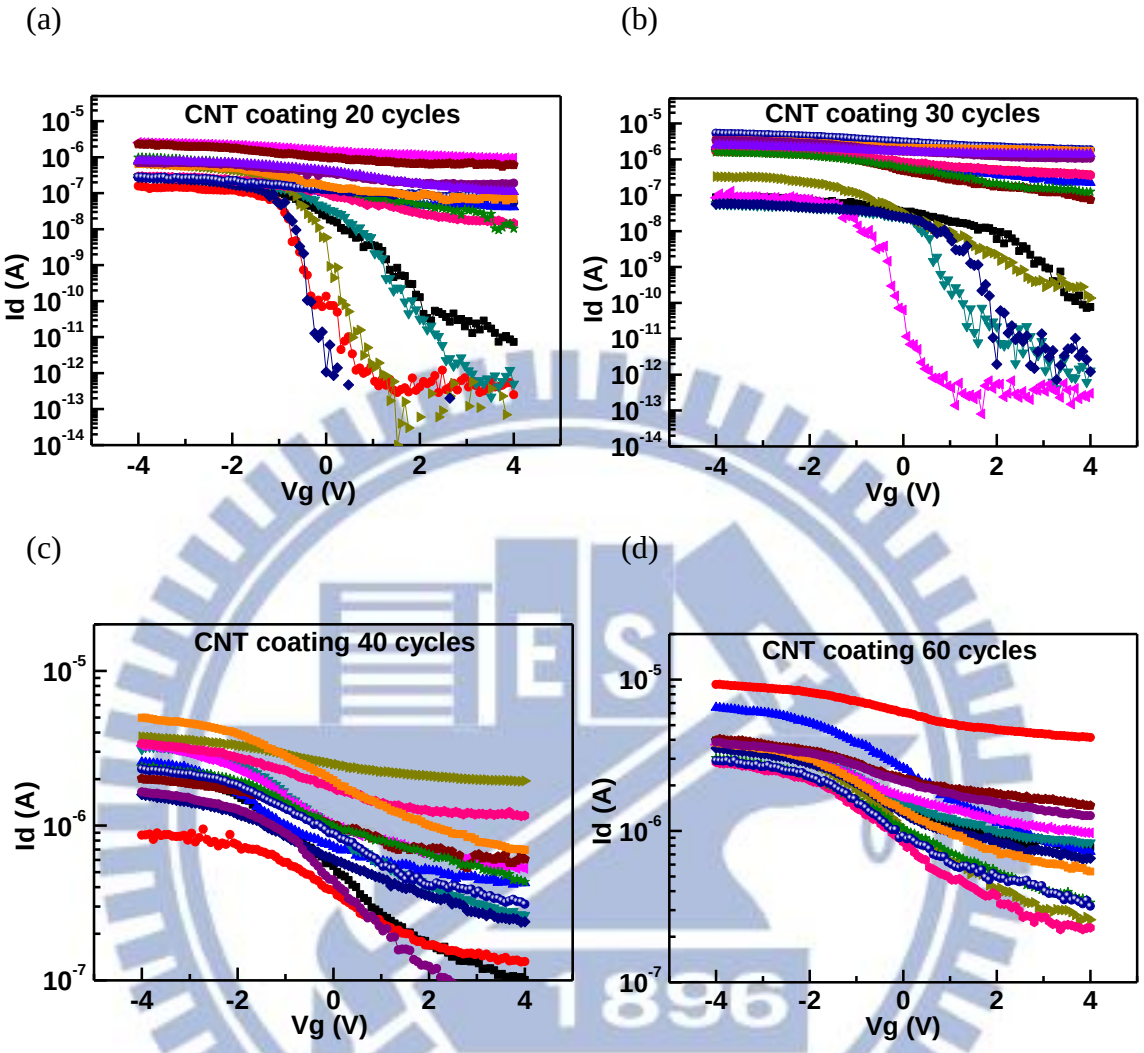
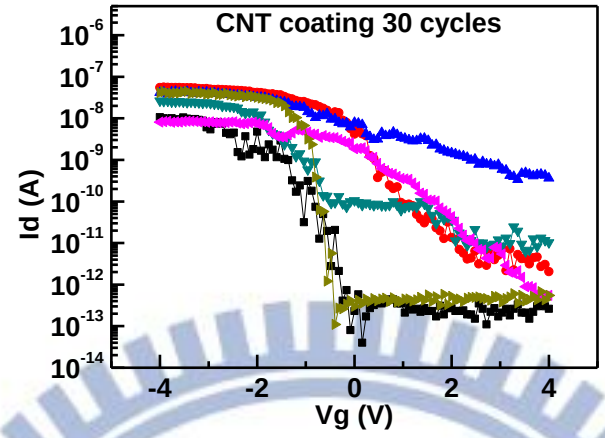
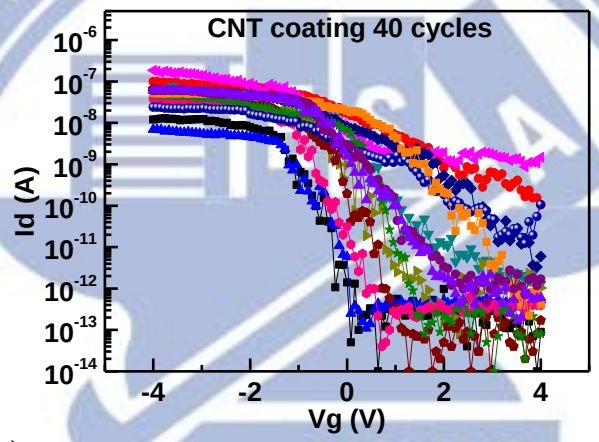


Fig. 3-4 Transfer characteristics (I_d vs. V_g) at V_d= -0.1V for devices with 10 nm Al_2O_3 gate dielectric layer (device dimension L= 1.4 μm and W= 50 μm) for CNT coating density varying from 20 to 60 cycles (a) CNT coating 20 cycles (b) CNT coating 30 cycles (c) CNT coating 40 cycles (d) CNT coating 60 cycles.

(a)



(b)



(c)

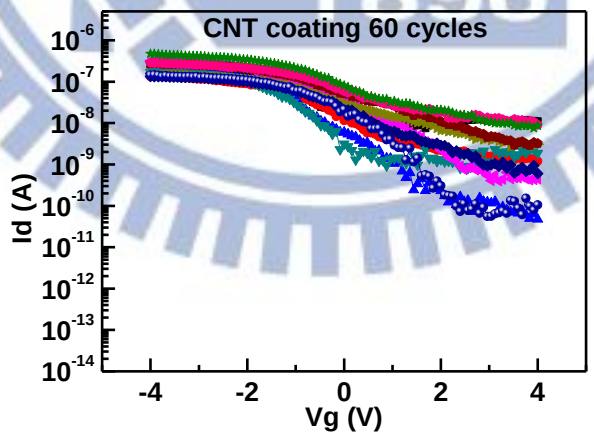
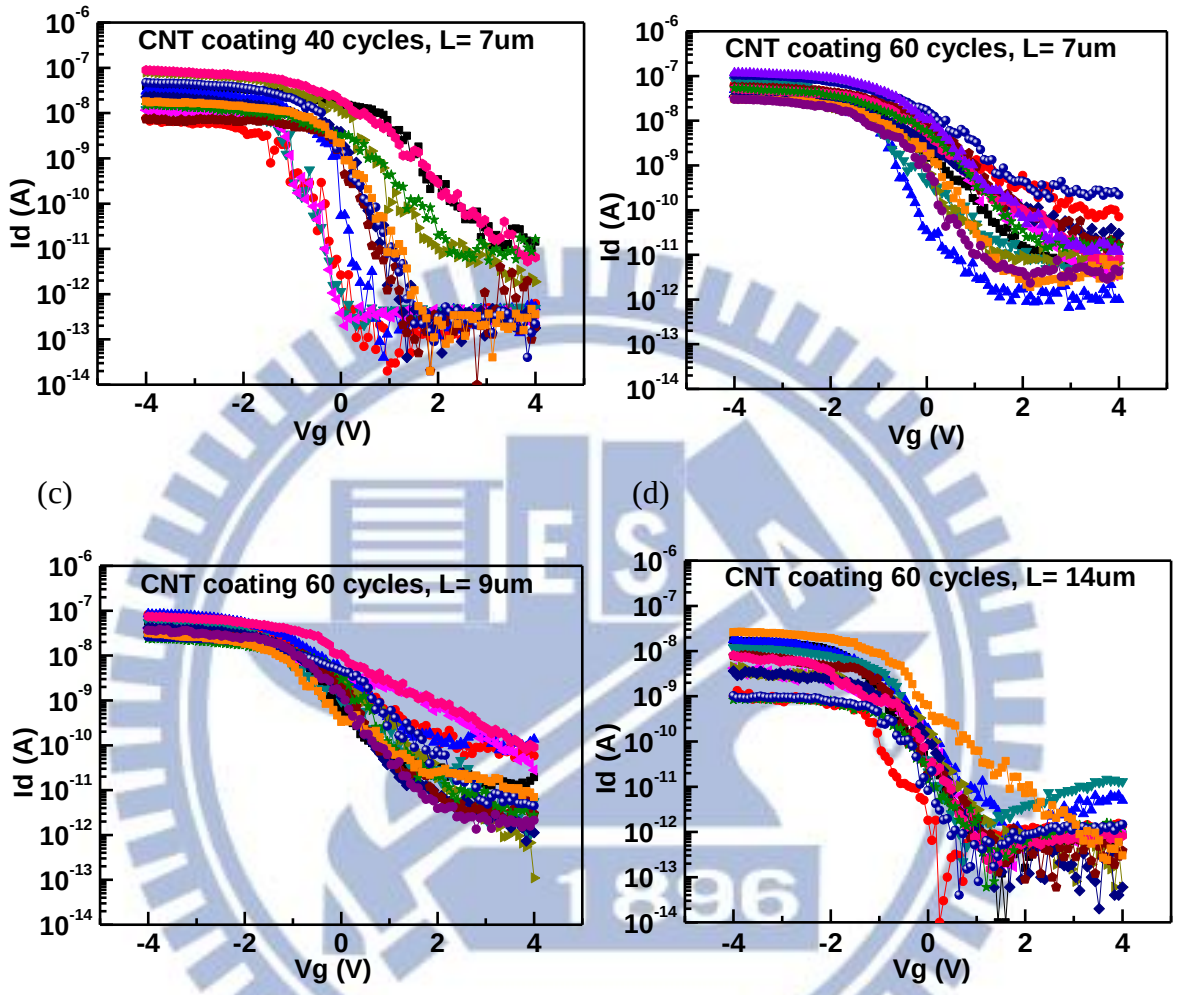


Fig. 3-5 Transfer characteristics (I_d vs. V_g) at V_d= -0.1V for devices with 10 nm Al_2O_3 gate dielectric layer (device dimension L= 4 μm and W= 50 μm) for CNT coating density varying from 30 to 60 cycles (a) CNT coating 30 cycles (b) CNT coating 40 cycles (c) CNT coating 60 cycles.

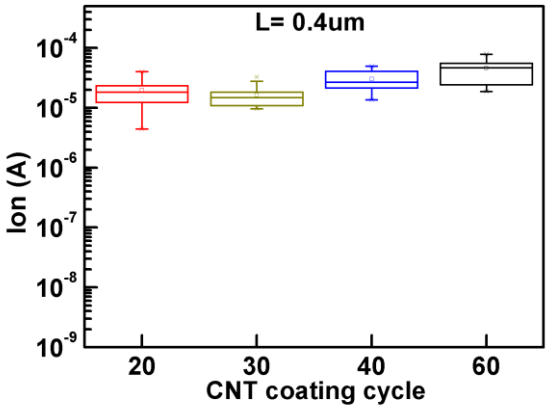
(a) (b)

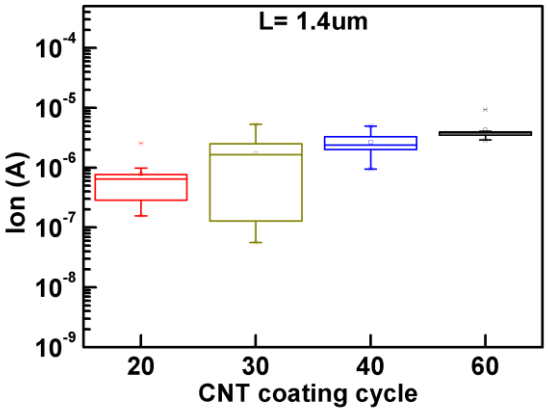


(c) (d)

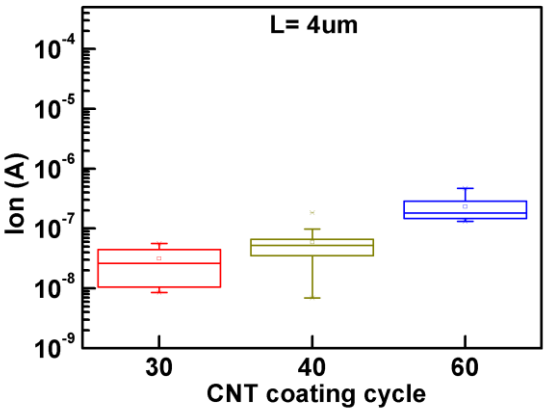
Fig. 3-6 Transfer characteristics (I_d vs. V_g) at V_d= -0.1V for devices with 10 nm Al_2O_3 gate dielectric layer (fixed channel width W= 50 μm) (a) L= 7 μm, CNT coating 40 cycles (b) L= 7 μm, CNT coating 60 cycles (c) L= 9 μm, CNT coating 60 cycles (d) L= 14 μm, CNT coating 60 cycles. All devices exhibit semiconducting behavior.

(a)





(c)



(d)

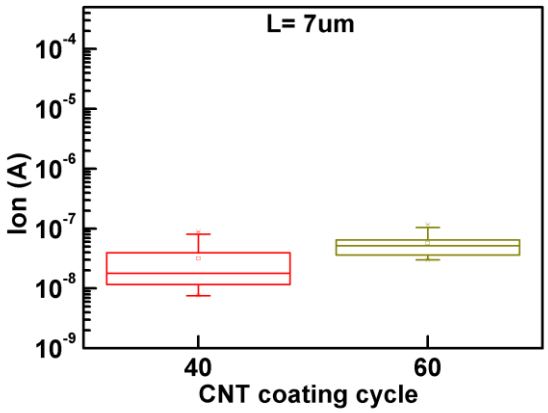


Fig. 3-7 On-state current vs. CNT coating density with various channel length L, fixed channel width W= 50 μm and Al_2O_3 gate dielectric thickness of 10 nm (a) L= 0.4 μm (b) L= 1.4 μm (c) L= 4 μm (d) L= 7 μm. Increasing CNT coating density increases on-state current.

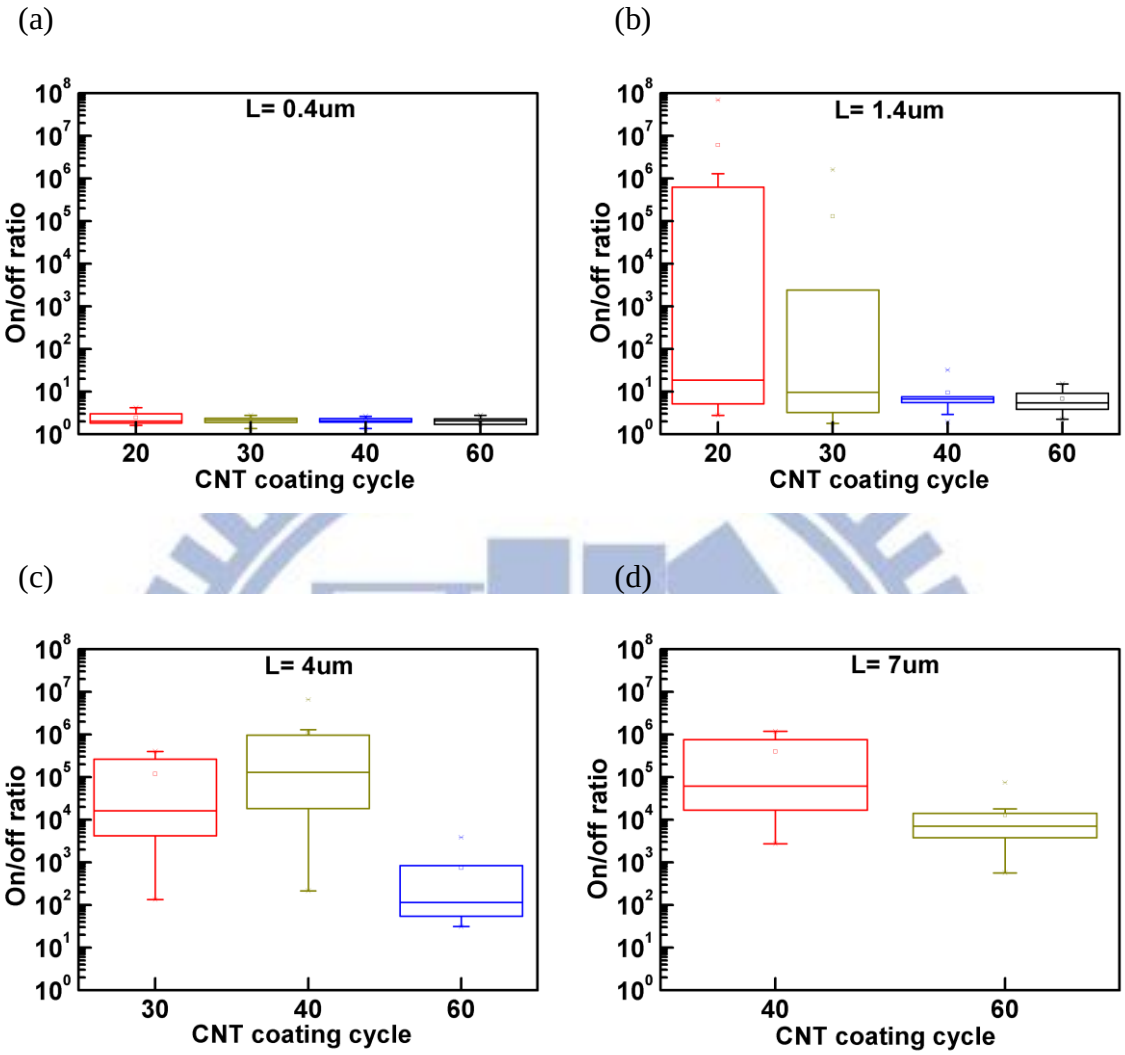


Fig. 3-8 On/off ratio vs. CNT coating density with various channel length L, fixed channel width W= 50 μm and Al_2O_3 gate dielectric thickness of 10 nm (a) L= 0.4 μm (b) L= 1.4 μm (c) L= 4 μm (d) L= 7 μm.

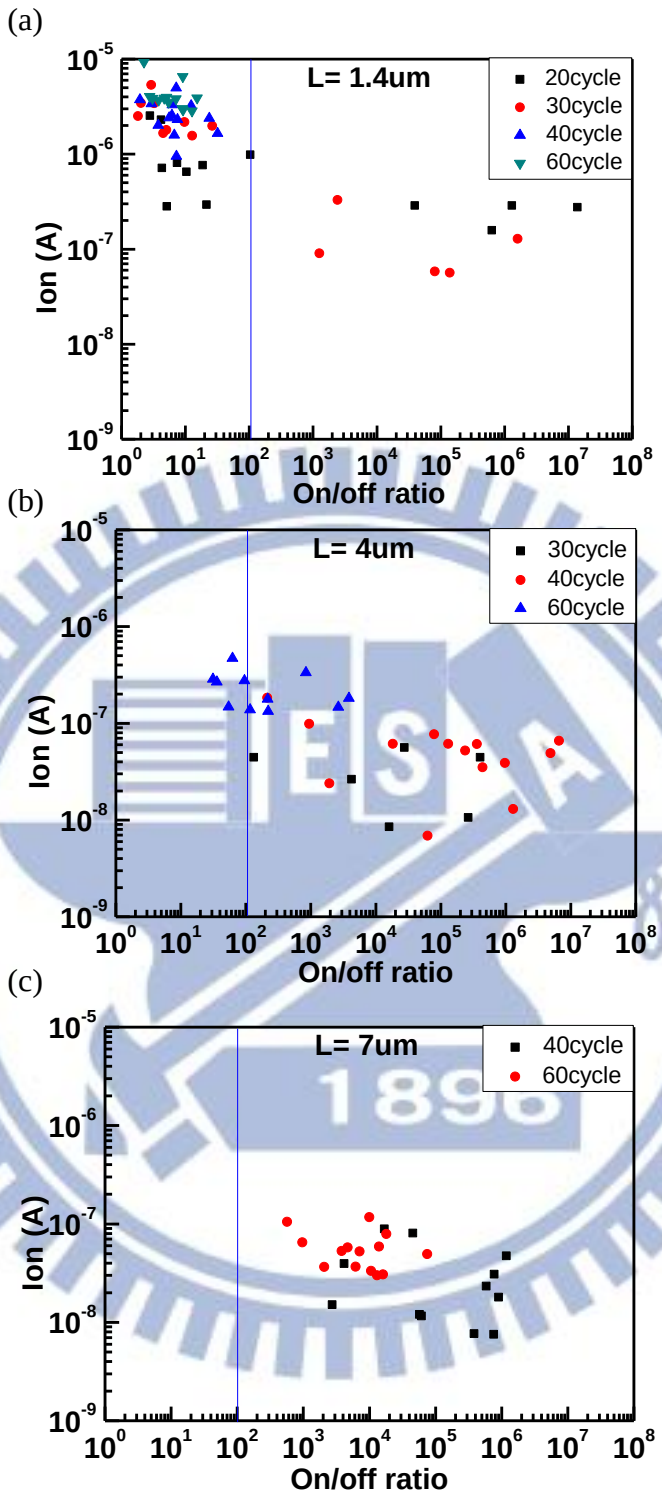


Fig. 3-9 On-state current against on/off ratio for various CNT coating density at varying channel lengths, fixed channel width W= 50 μm, and Al_2O_3 gate dielectric layer of 10 nm (a) L= 1.4 μm (b) L= 4 μm (c) L= 7 μm. The blue line indicates On/off ratio = 100. Optimized CNT density are 20, 40, and 60 coating cycles for channel length L= 1.4, 4, and 7μm, respectively.

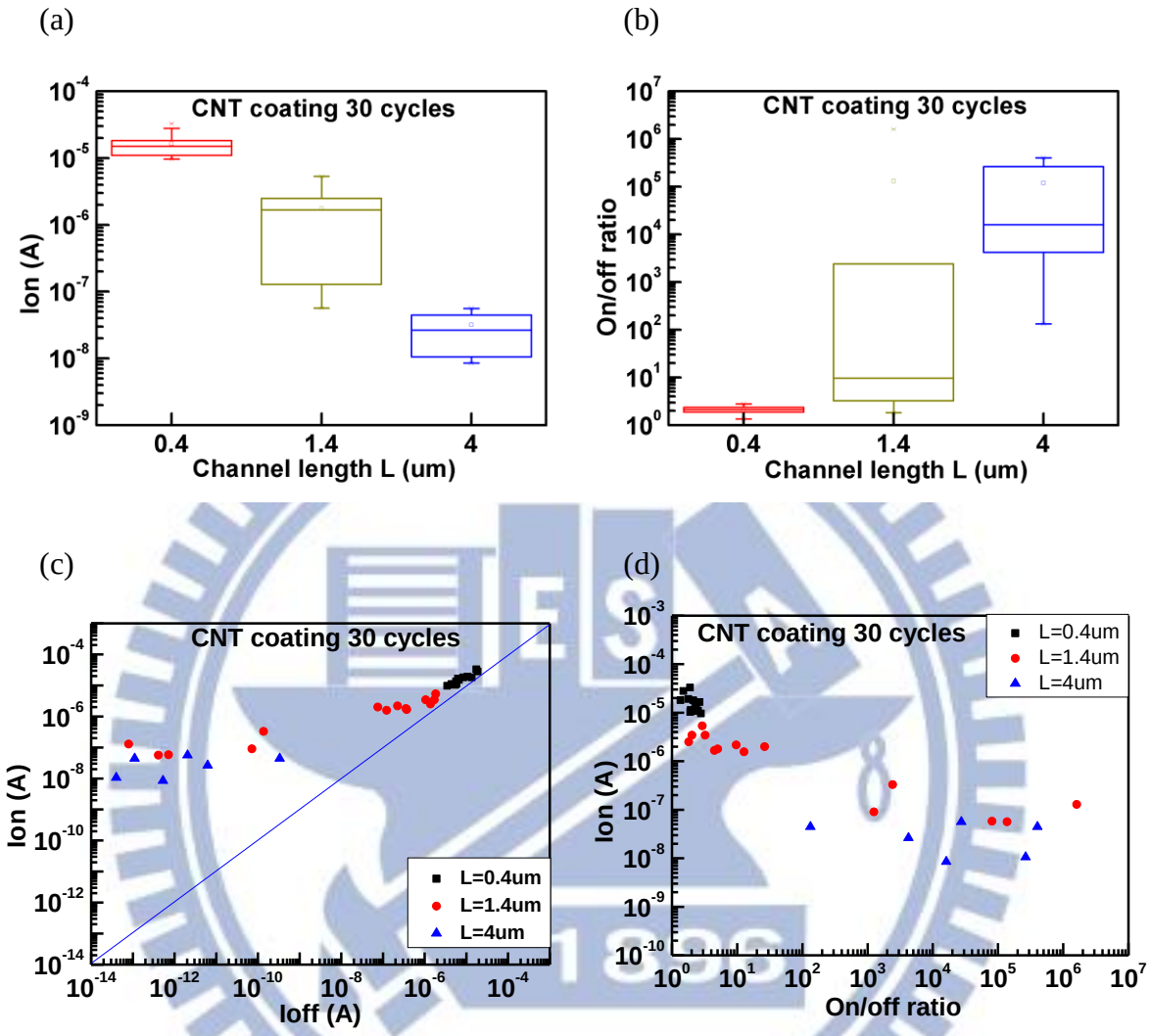


Fig. 3-10 CNT networks with CNT coating density of 30 cycles (a) on-state current vs. channel length shows increasing channel length decreases on-state current nonlinearly. (b) on/off ratio vs. channel length shows increasing channel length improves on/off ratio. (c) on-state current vs. off-state current for various channel length (d) on-state current vs. on/off ratio for various channel length.

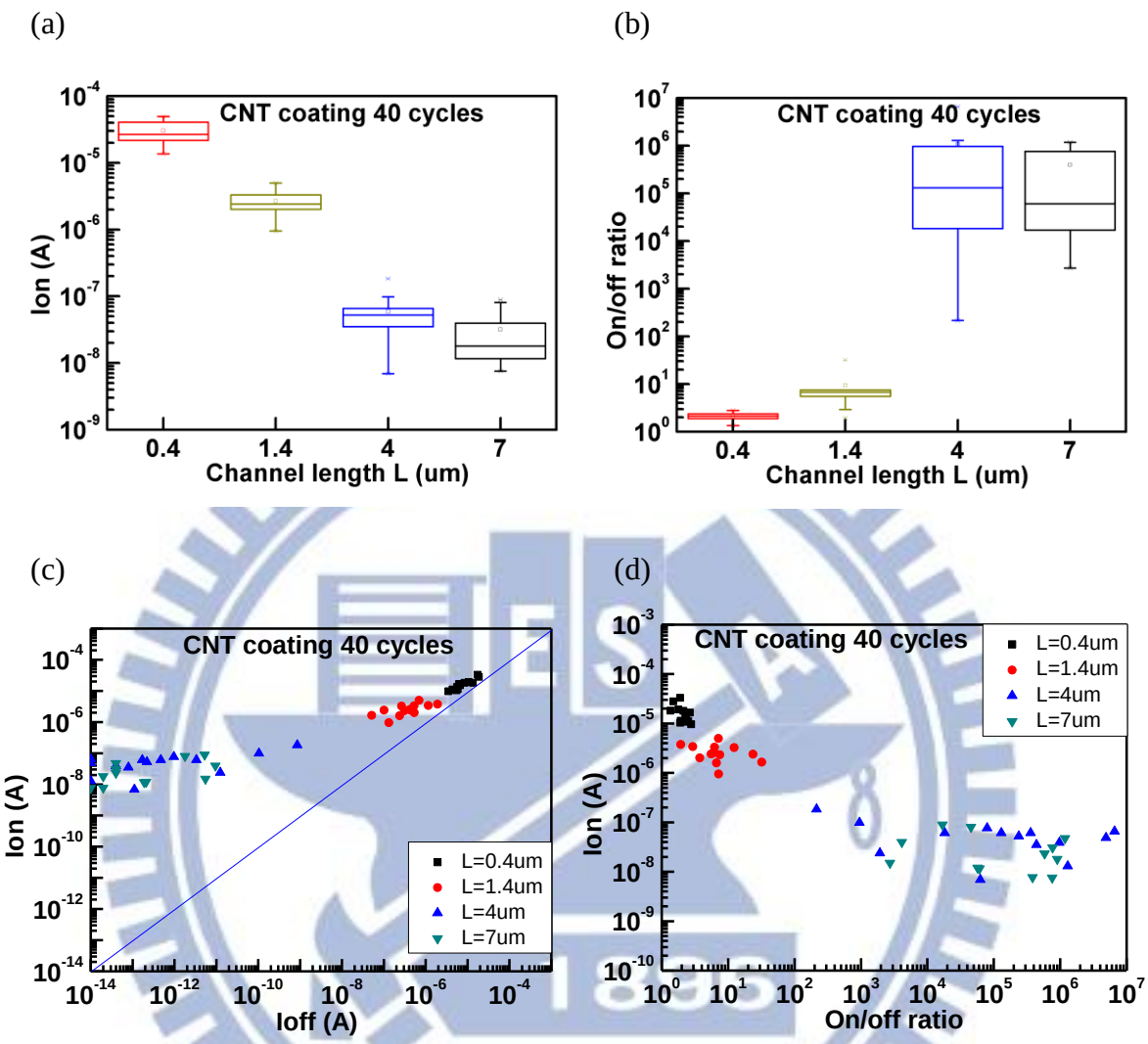


Fig. 3-11 CNT networks with CNT coating density of 40 cycles (a) on-state current vs. channel length (b) on/off ratio vs. channel length (c) on-state current vs. off-state current for various channel length (d) on-state current vs. on/off ratio for various channel length.

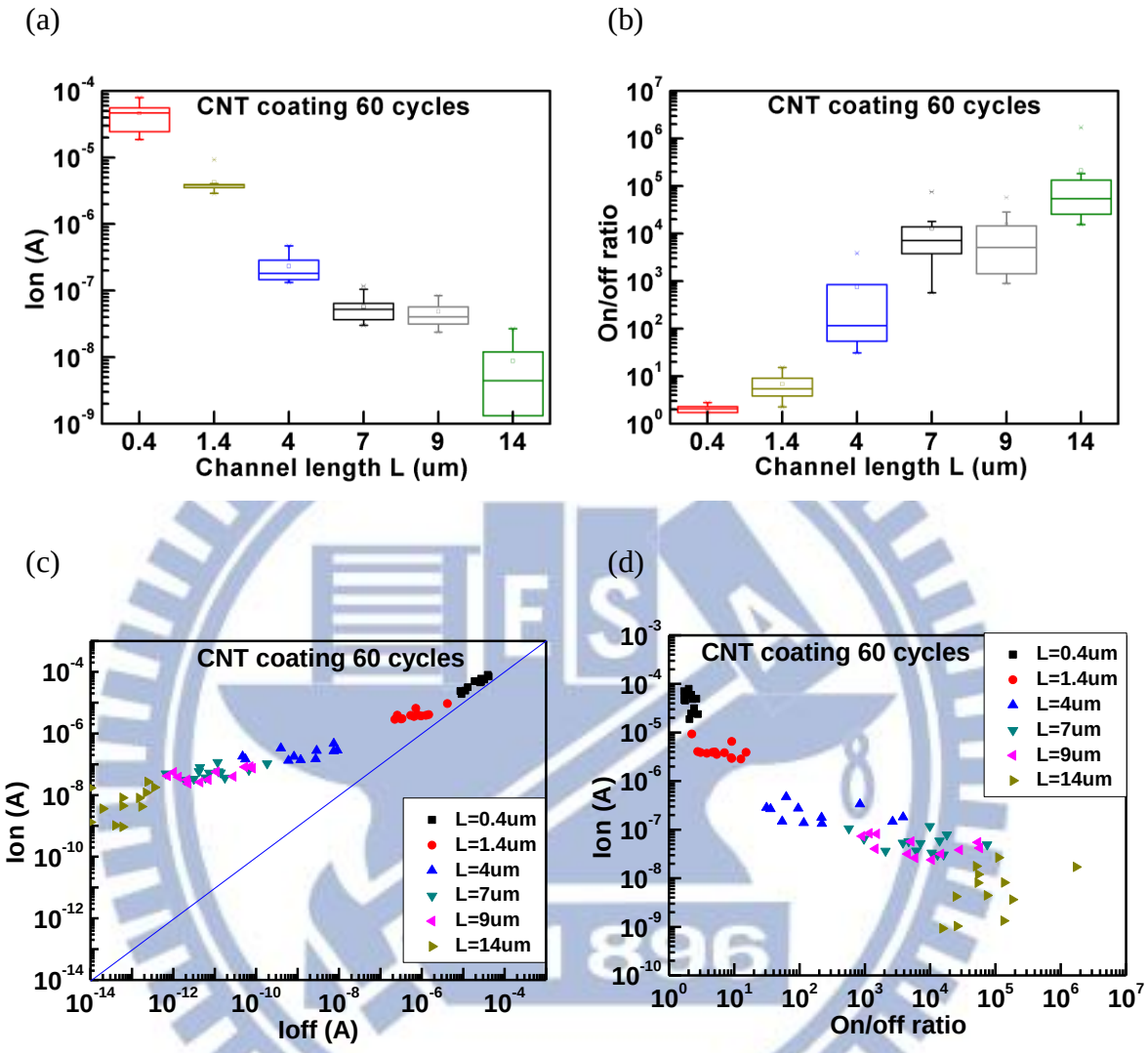


Fig. 3-12 CNT networks with CNT coating density of 60 cycles (a) on-state current vs. channel length (b) on/off ratio vs. channel length (c) on-state current vs. off-state current for various channel length (d) on-state current vs. on/off ratio for various channel length.

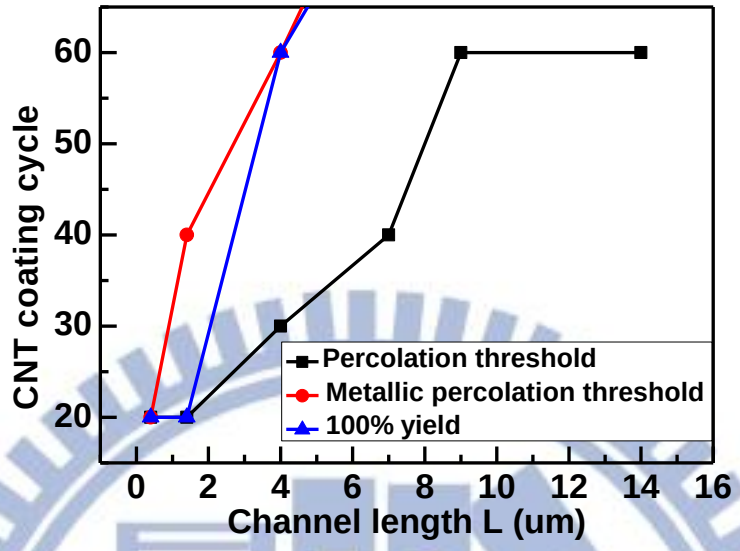
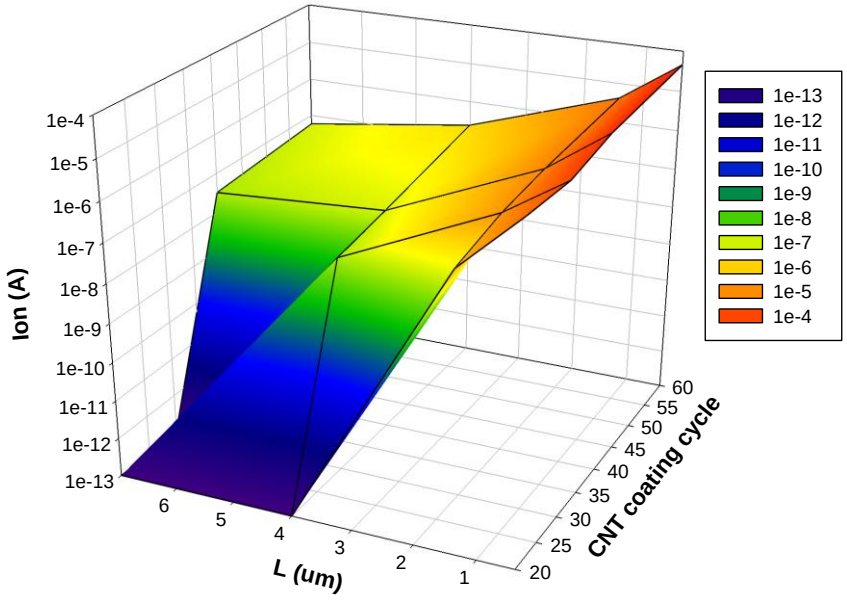


Fig. 3-13 Conducting percolation threshold (black line), metallic percolation threshold (red line), and CNT density for 100% yield vs. channel length ranging from 0.4 to 14 μm. Devices exhibit metallic behavior when CNT density is above metallic percolation threshold. Besides, if devices exhibit semiconducting behavior, the yield is lower than 100%. There is a trade-off between 100% yield and metallic behavior.

(a)



(b)

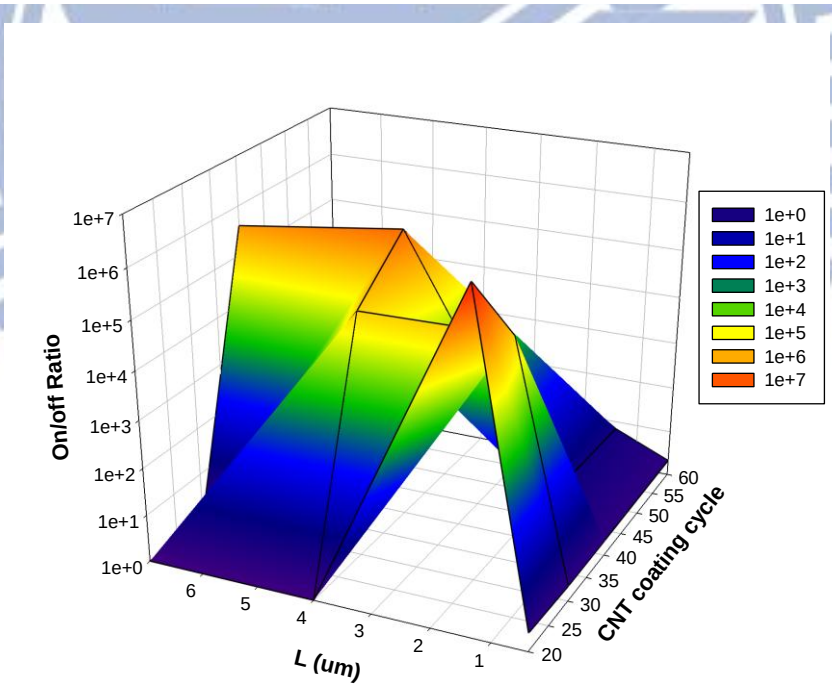
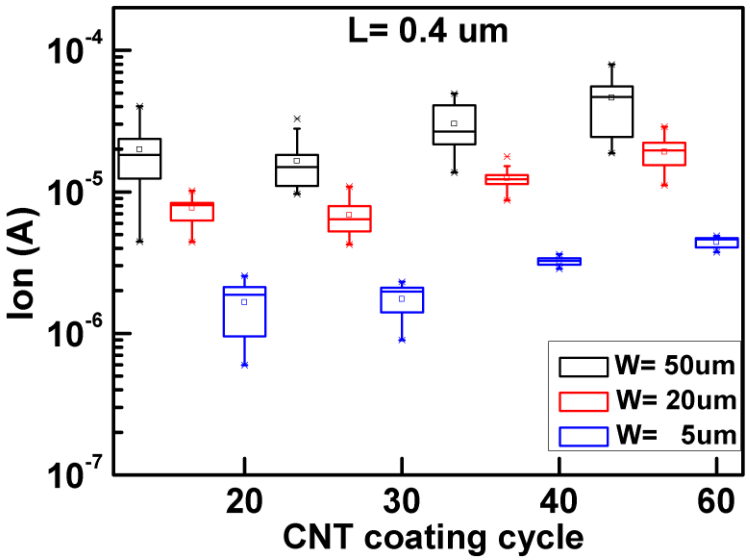


Fig. 3-14 CNT density and channel length dependence of on-state current and on/off ratio are shown in 3D diagram. (a) on-state current- CNT density- channel length (b) on/off ratio- CNT density- channel length.

(a)



(b)

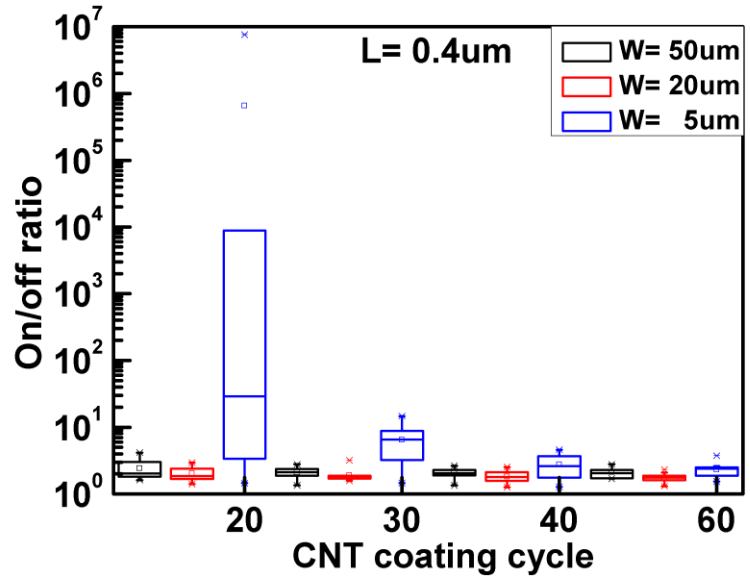
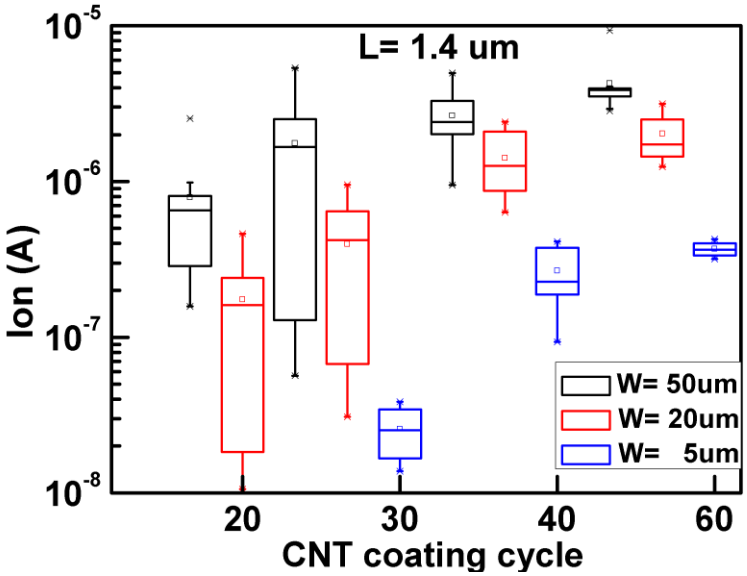


Fig. 3-15 Channel width dependence of on-state current and on/off ratio (device dimension of fixed channel length L= 0.4 μm and width varying from W= 5 to 50 μm) (a) on-state current vs. CNT coating density (b) on/off ratio vs. CNT coating density. Decreasing channel width results in the decrease of on-state current and the improvement of on/off ratio.

(a)



(b)

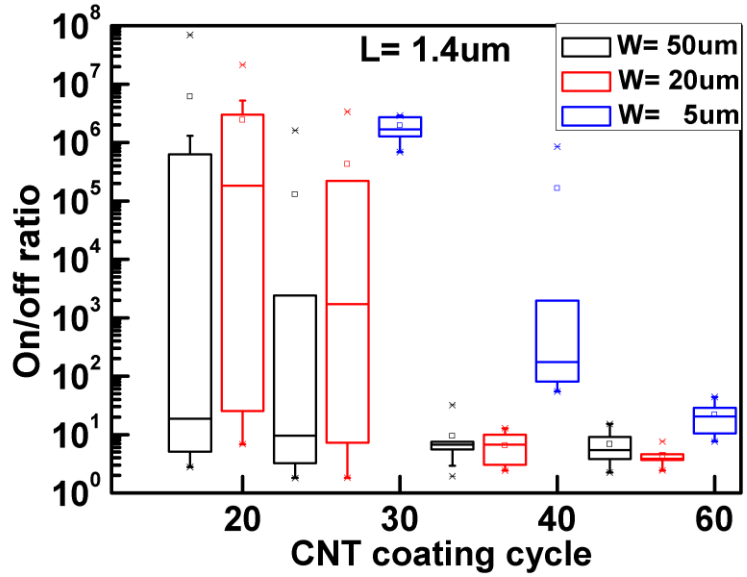
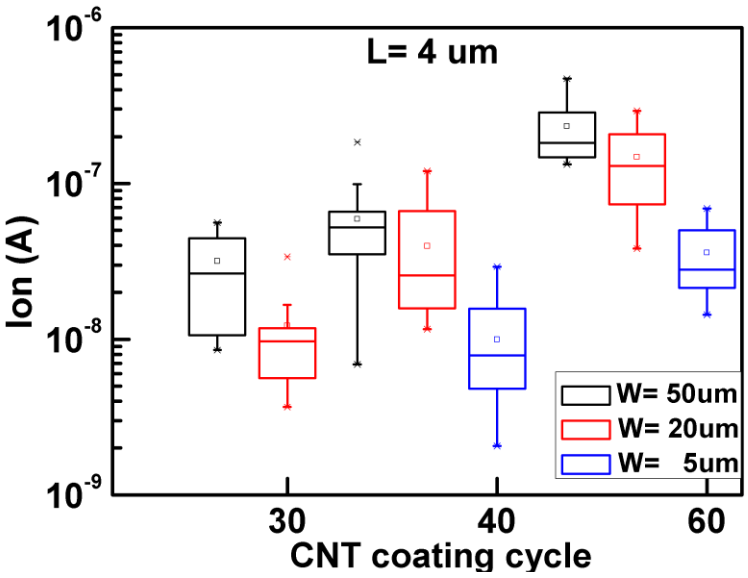


Fig. 3-16 Channel width dependence of on-state current and on/off ratio (device dimension of fixed channel length L= 1.4 μm and width varying from W= 5 to 50 μm) (a) on-state current vs. CNT coating density (b) on/off ratio vs. CNT coating density. It is noticed that increasing channel length would make on-state current decrease non-linearly due to nonuniform CNT network coverage. In addition, increasing channel length also improves on/off ratio significantly.

(a)



(b)

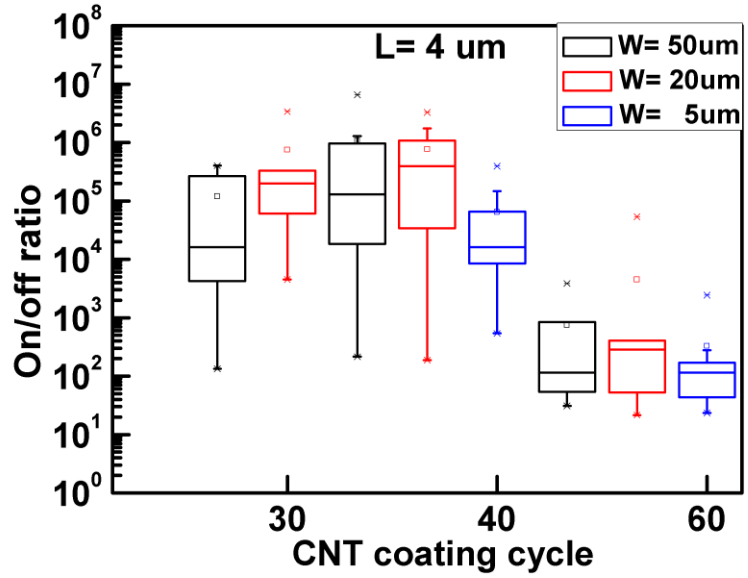
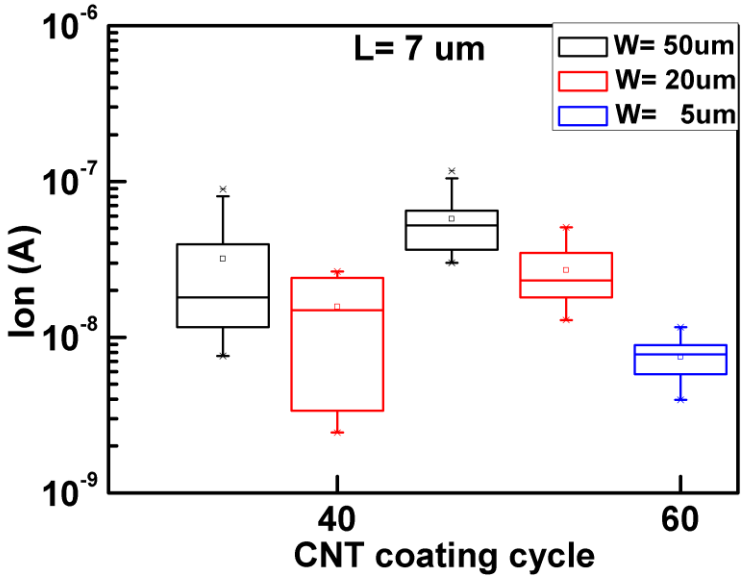


Fig. 3-17 Channel width dependence of on-state current and on/off ratio (device dimension of fixed channel length L= 4 μm and width varying from W= 5 to 50 μm) (a) on-state current vs. CNT coating density (b) on/off ratio vs. CNT coating density. The on/off ratio maintains a certain value which is not affected by channel width for devices with L= 4 μm.

(a)



(b)

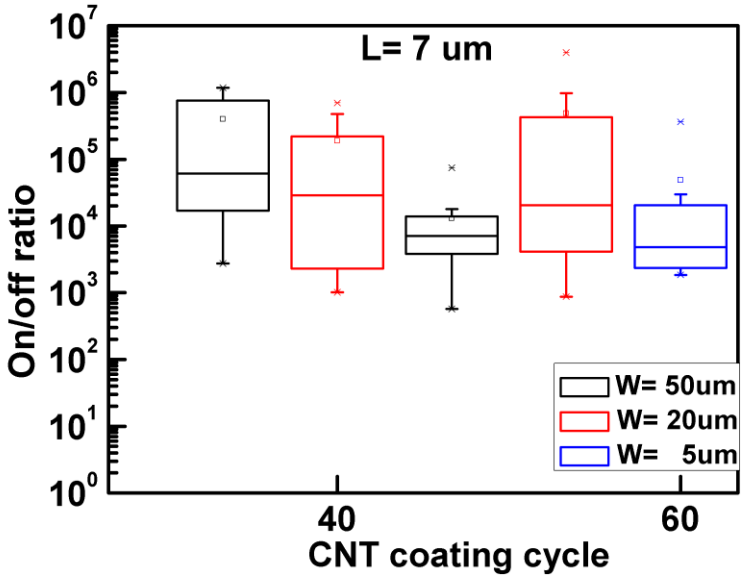


Fig. 3-18 Channel width dependence of on-state current and on/off ratio (device dimension of fixed channel length L= 7 μm and width varying from W= 5 to 50 μm) (a) on-state current vs. CNT coating density (b) on/off ratio vs. CNT coating density. The on/off ratio is not affected by channel width for devices with L= 7 μm.

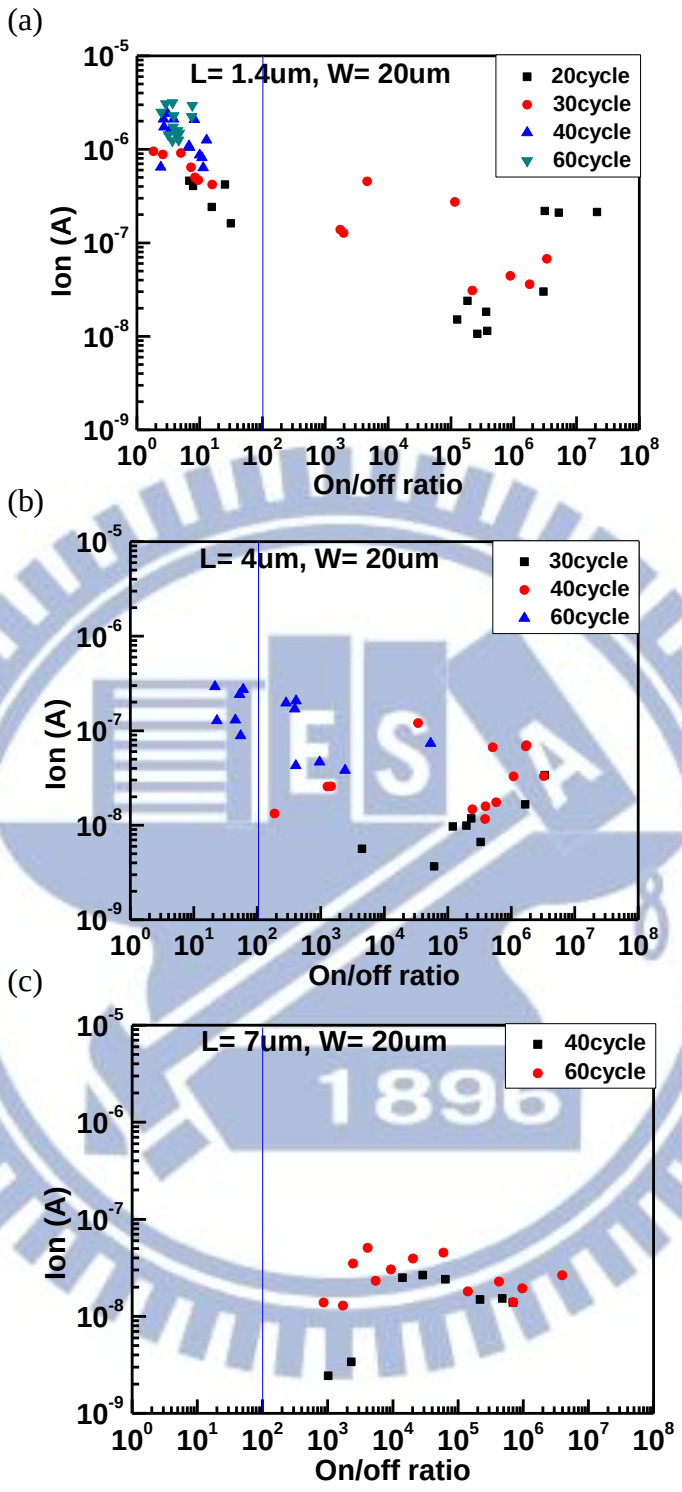


Fig. 3-19 On-state current plotted against on/off ratio for various CNT coating density at varying channel lengths and fixed channel width W= 20 μm, and 10 nm Al_2O_3 gate dielectric layer (a) L= 1.4 μm (b) L= 4 μm (c) L= 7 μm. The blue line indicates On/off ratio = 100. Optimized CNT density are 30, 40, and 60 coating cycles for channel length L= 1.4, 4, and 7μm, respectively.

(a)

(b)

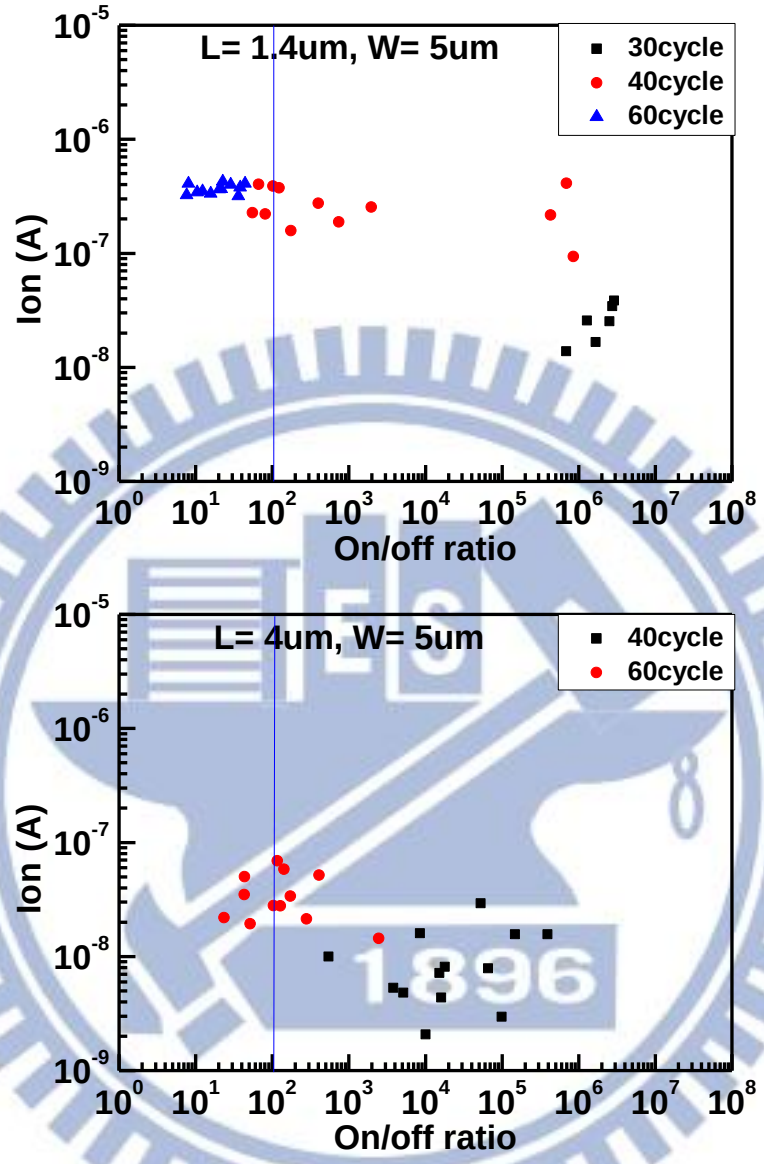


Fig. 3-20 On-state current plotted against on/off ratio for various CNT coating density at varying channel lengths and fixed channel width W= 5 μm, and 10 nm Al_2O_3 gate dielectric layer (a) L= 1.4 μm (b) L= 4 μm. Optimized CNT density are 40 and 60 coating cycles for channel length L= 1.4 and 4μm, respectively.

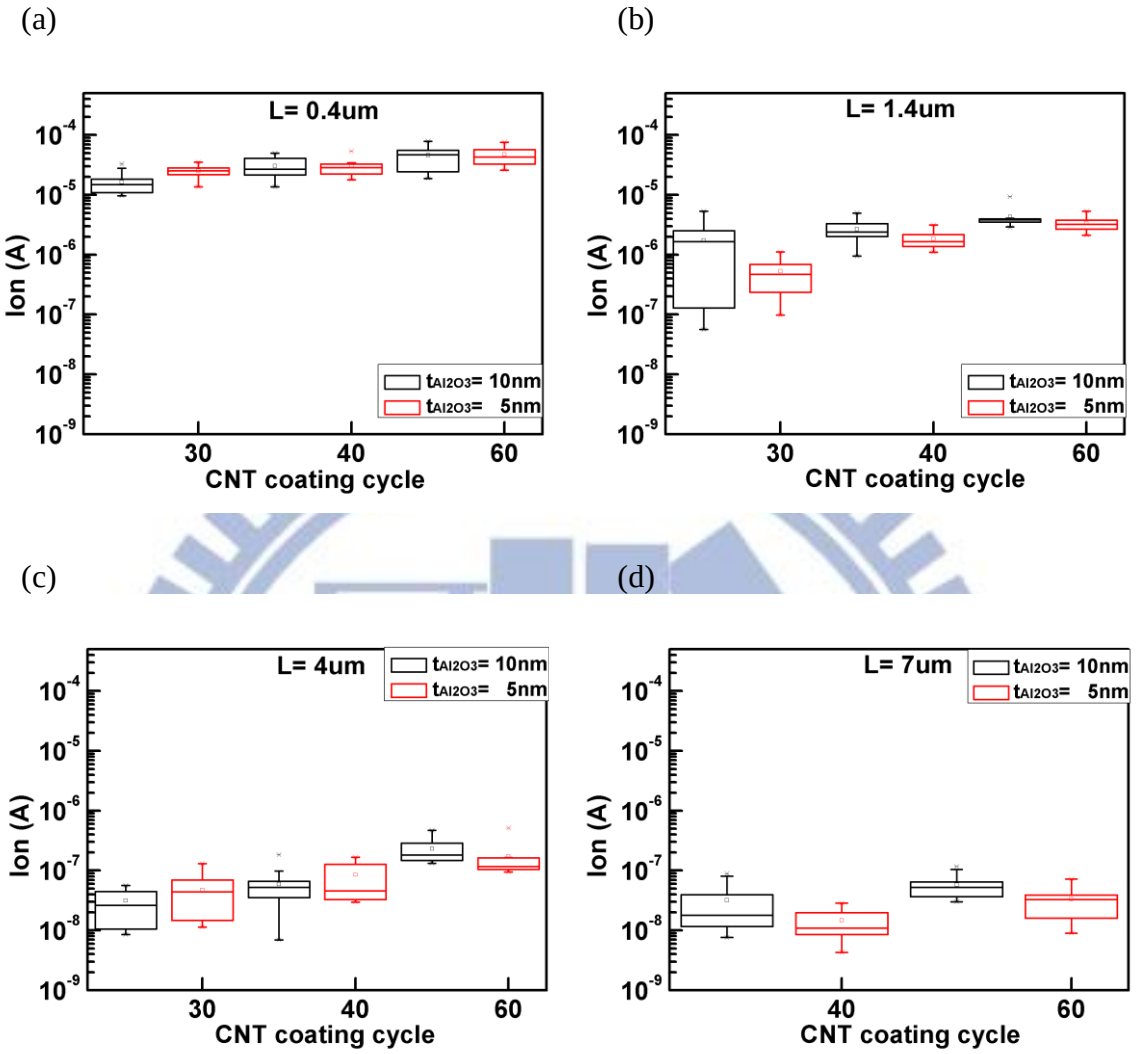


Fig. 3-21 Gate dielectric thickness dependence on on-state current plotted against CNT coating density with various channel length L (a) L= 0.4 μm (b) L= 1.4 μm (c) L= 4 μm (d) L= 7 μm. Since device variation is larger than gate dielectric thickness change, decreasing gate dielectric thickness does not increase on-state current obviously.

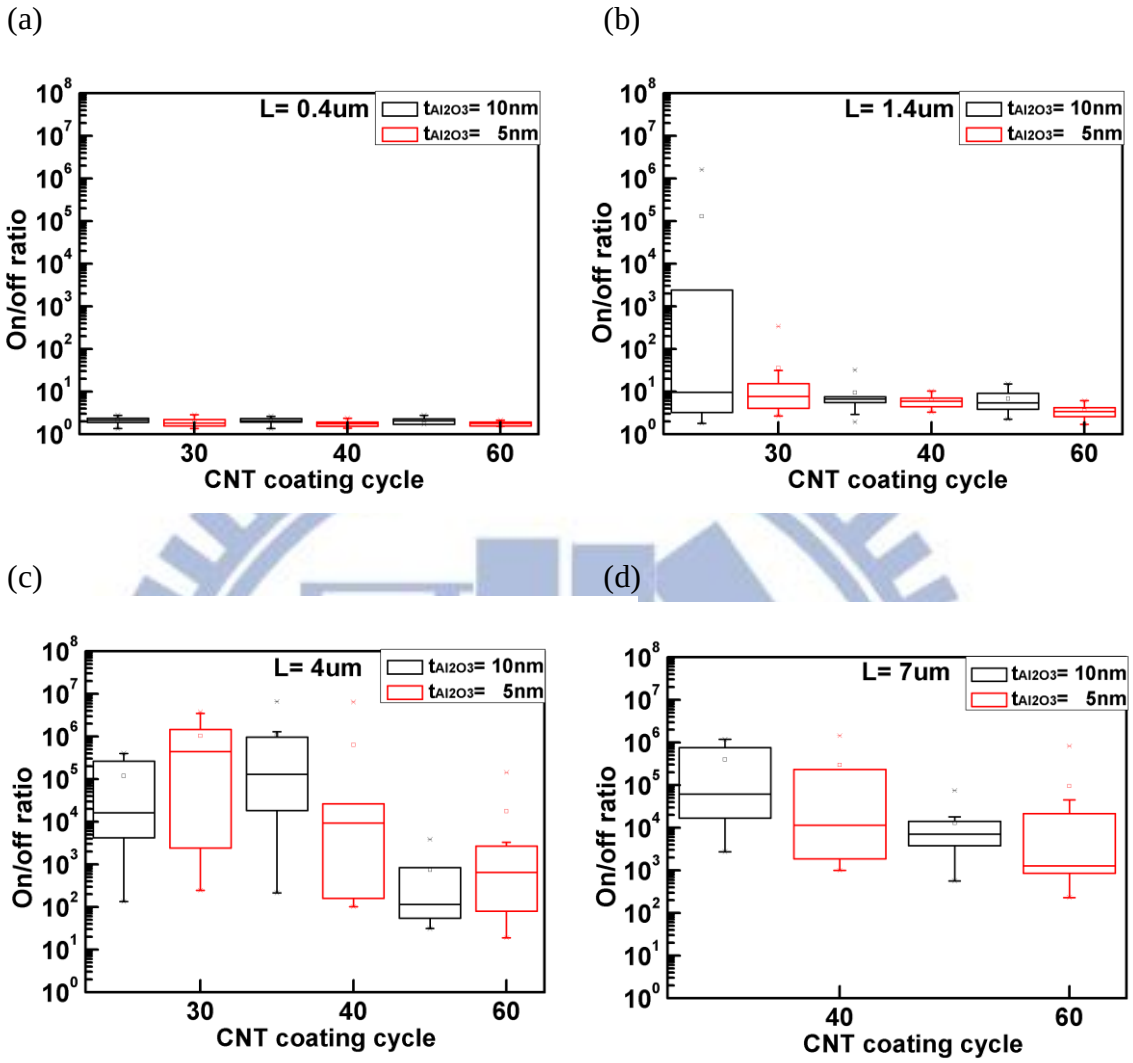


Fig. 3-22 Gate dielectric thickness dependence on on/off ratio plotted against CNT coating density with various channel length L (a) L= 0.4 μm (b) L= 1.4 μm (c) L= 4 μm (d) L= 7 μm. Since device variation is larger than gate dielectric thickness change, decreasing gate dielectric thickness does not increase on/off ratio dramatically.

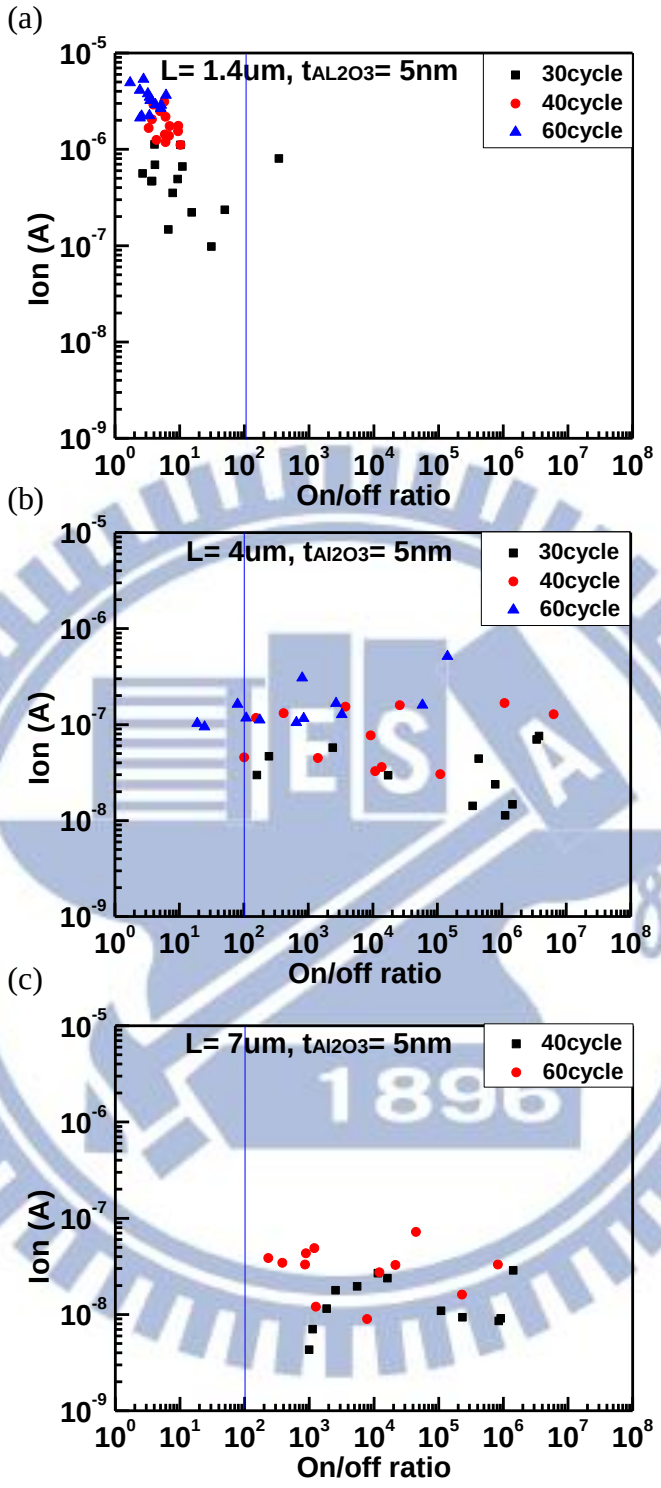
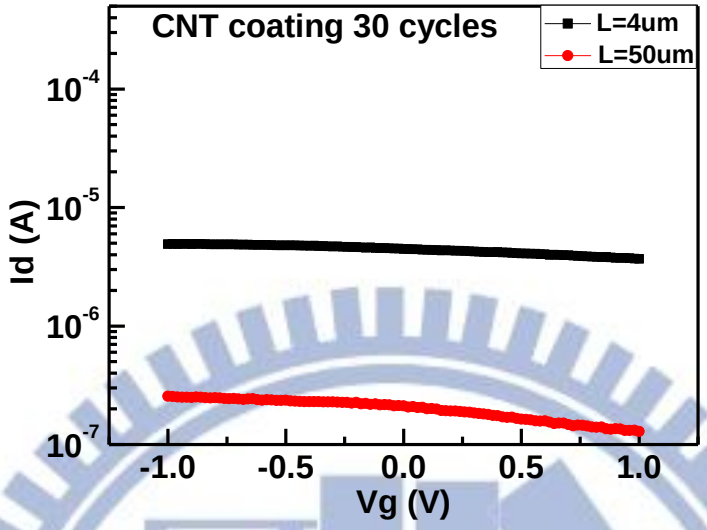


Fig. 3-23 On-state current vs. on/off ratio for various CNT coating density at varying channel lengths, fixed channel width W= 50 μm, and 5 nm Al_2O_3 gate dielectric thickness. (a) L= 1.4 μm (b) L= 4 μm (c) L= 7 μm. The blue line indicates On/off ratio = 100. Optimized CNT density are 30, 40, and 60 coating cycles for channel length L= 1.4, 4, and 7μm, respectively.

(a)



(b)

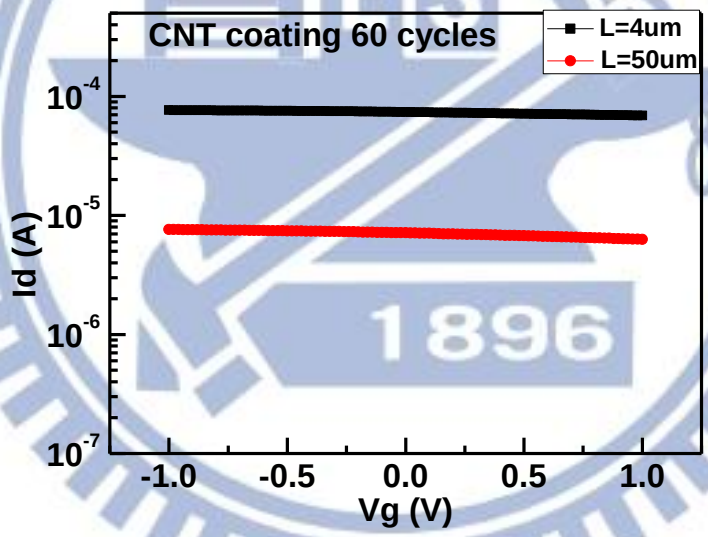
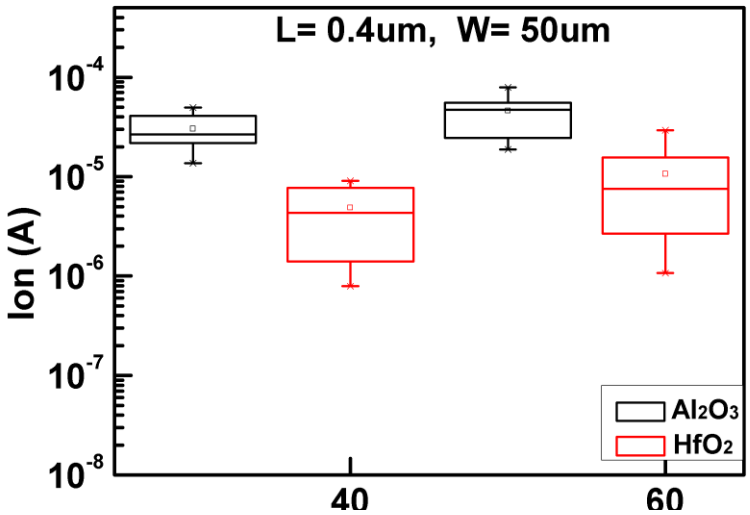


Fig. 3-24 Transfer characteristics (I_d vs. V_g) at V_d= -0.1V for devices coated with average CNT length of 15 μm. (a) CNT coating 30 cycles (b) CNT coating 60 cycles. Increasing CNT length results in the increase of on-state current significantly.

(a)



(b)

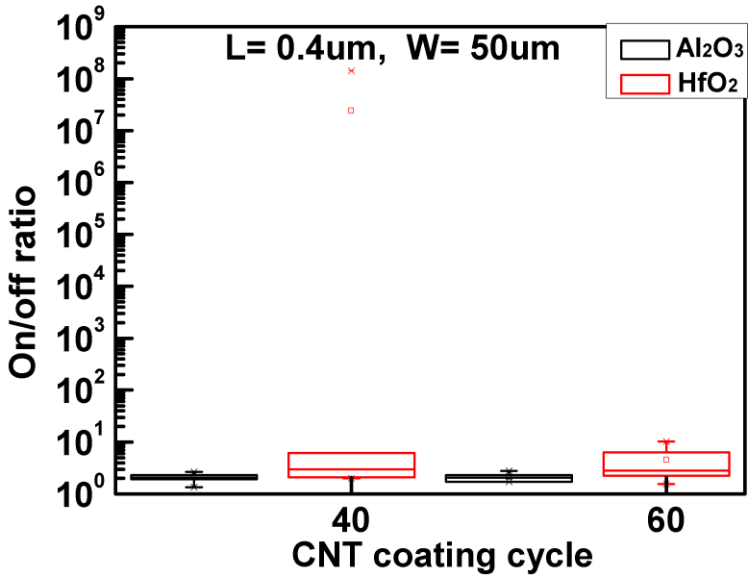
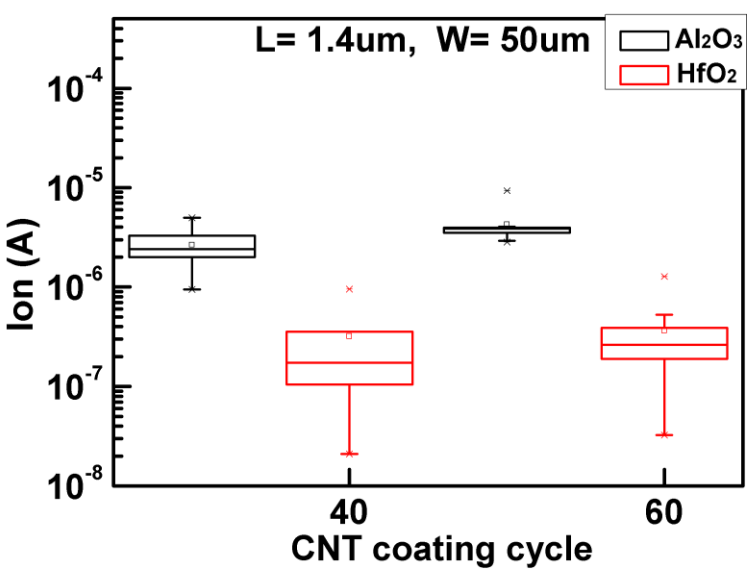


Fig. 3-25 Coating surface dependence (10-nm-thickness Al_2O_3 and HfO_2) of on-state current and on/off ratio (device dimension of L= 0.4 μm and W= 50 μm) (a) on-state current vs. CNT coating density (b) on/off ratio vs. CNT coating density. Poor wet ability of HfO_2 film attributes low on-state current.

(a)



(b)

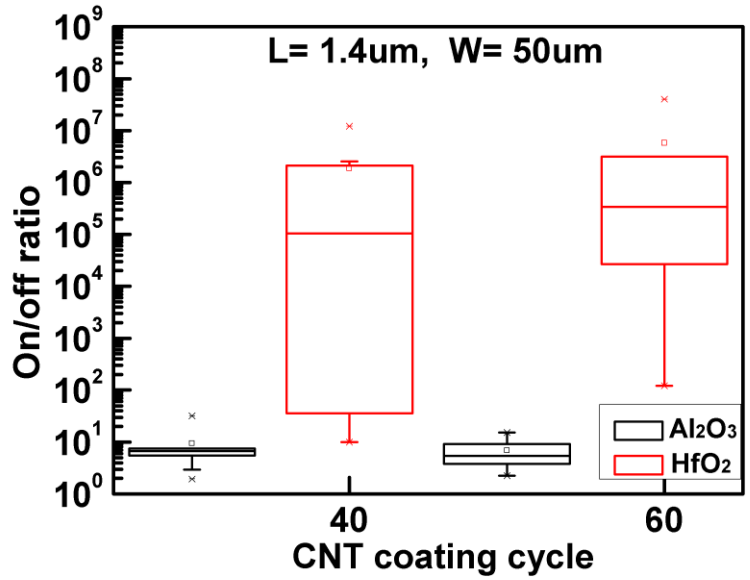


Fig. 3-26 Coating surface dependence (10-nm-thickness Al_2O_3 and HfO_2) of on-state current and on/off ratio (device dimension of L= 1.4 μm and W= 50 μm) (a) on-state current vs. CNT coating density (b) on/off ratio vs. CNT coating density. Devices with HfO_2 film improves on/off ratio with channel length L= 1.4 μm.

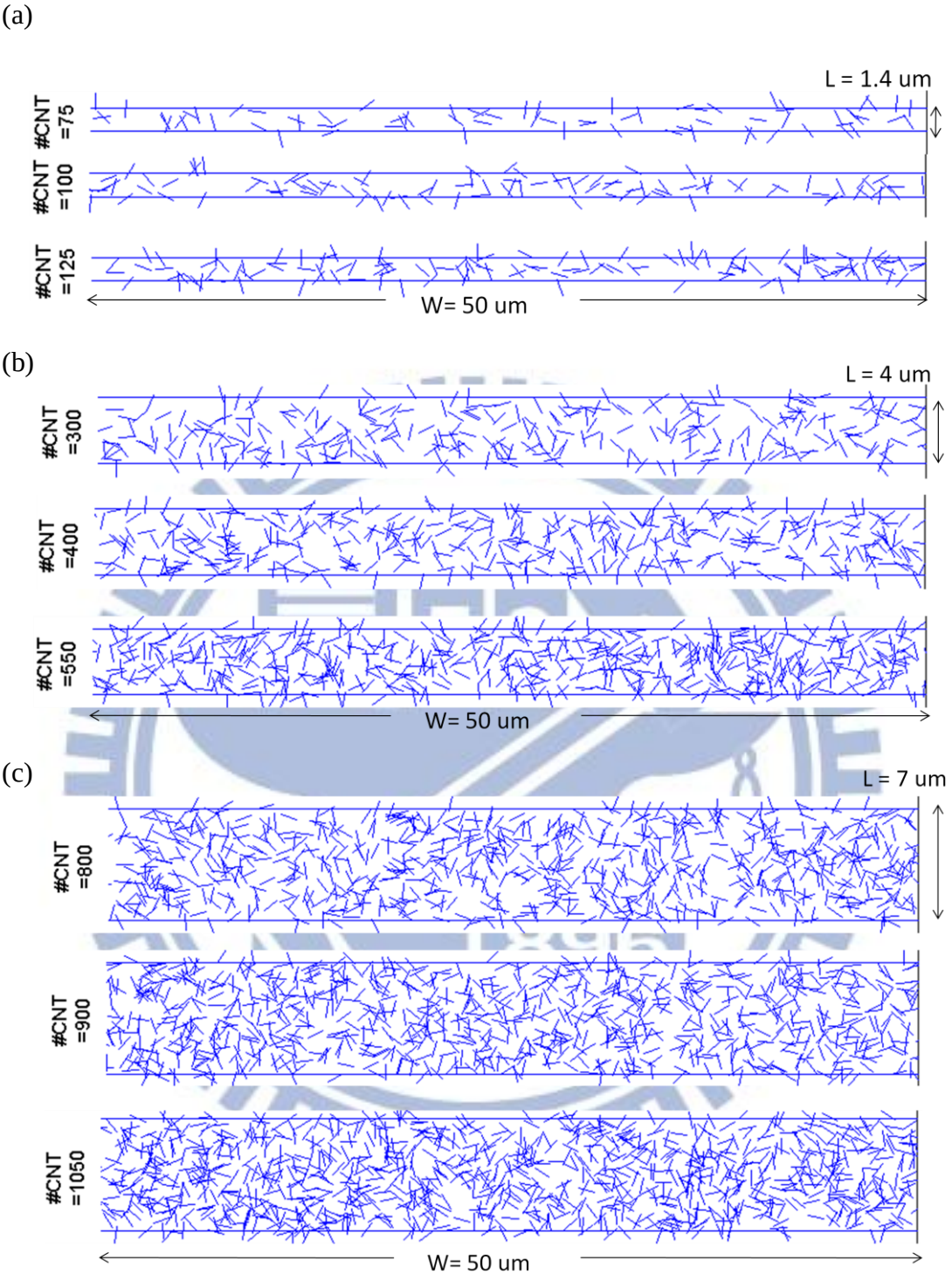


Fig. Fig. 3-27 Percolation threshold for devices with fixed W= 50 μm and channel length varying from L= 1.4, 4, to 7 μm, respectively. (a) percolation threshold is 125 (CNTs) /70 μm^2 = 1.79 CNTs/μm^2 for L= 1.4 μm (b) 550 (CNTs)/ 200 μm^2 = 2.75 CNTs/μm^2 for L= 4 μm (c) 1050 (CNTs)/ 350 μm^2 = 3 CNTs/μm^2 for L= 7 μm.

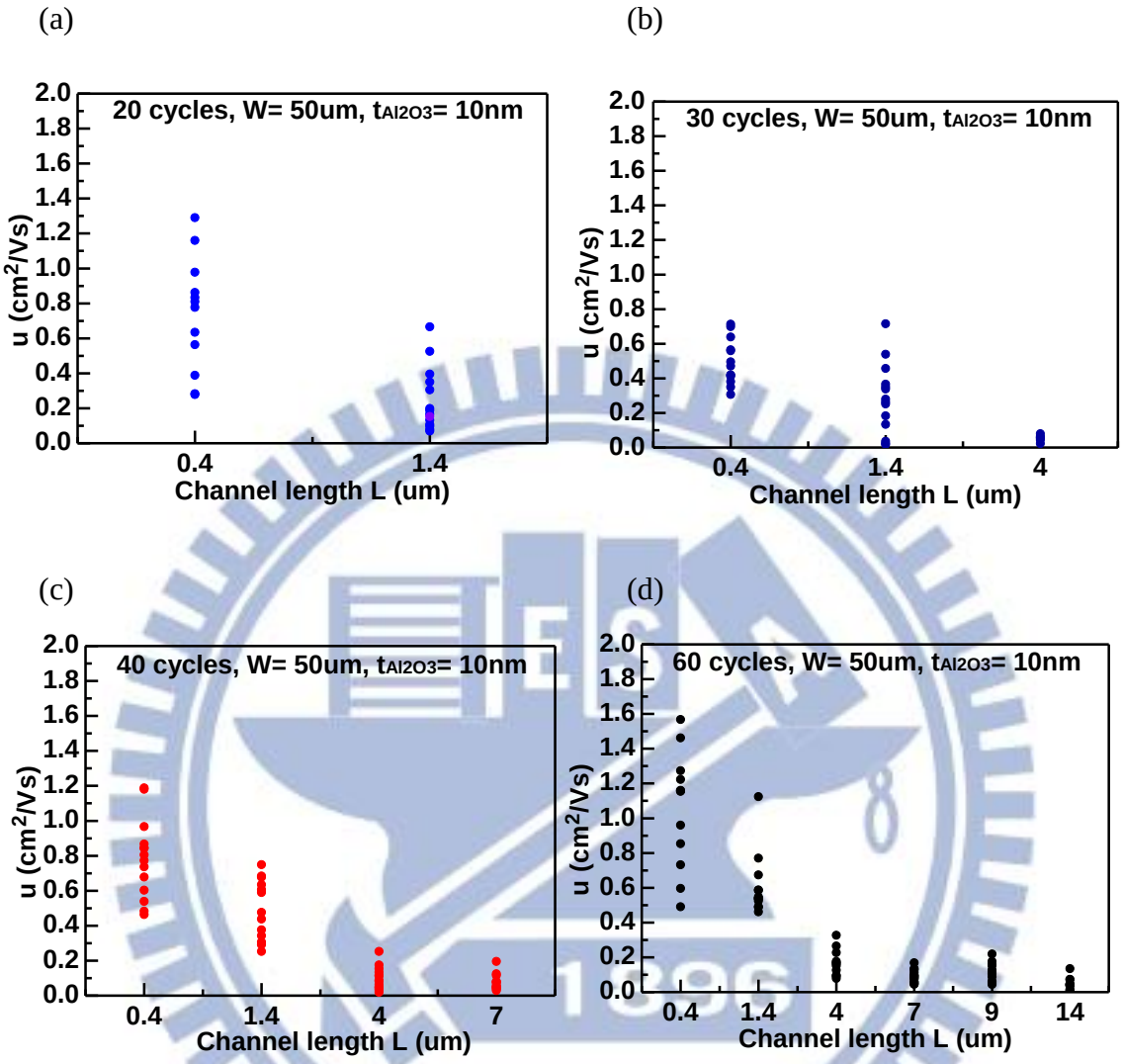


Fig. 3-28 Mobility was plotted against channel length for devices with channel width W= 50 μm and Al_2O_3 film of 10 nm for CNT coating density ranging from 20 to 60 cycles (a) CNT coating 20 cycles (b) CNT coating 30 cycles (c) CNT coating 40 cycles (d) CNT coating 60 cycles. Increasing channel length decreases mobility.

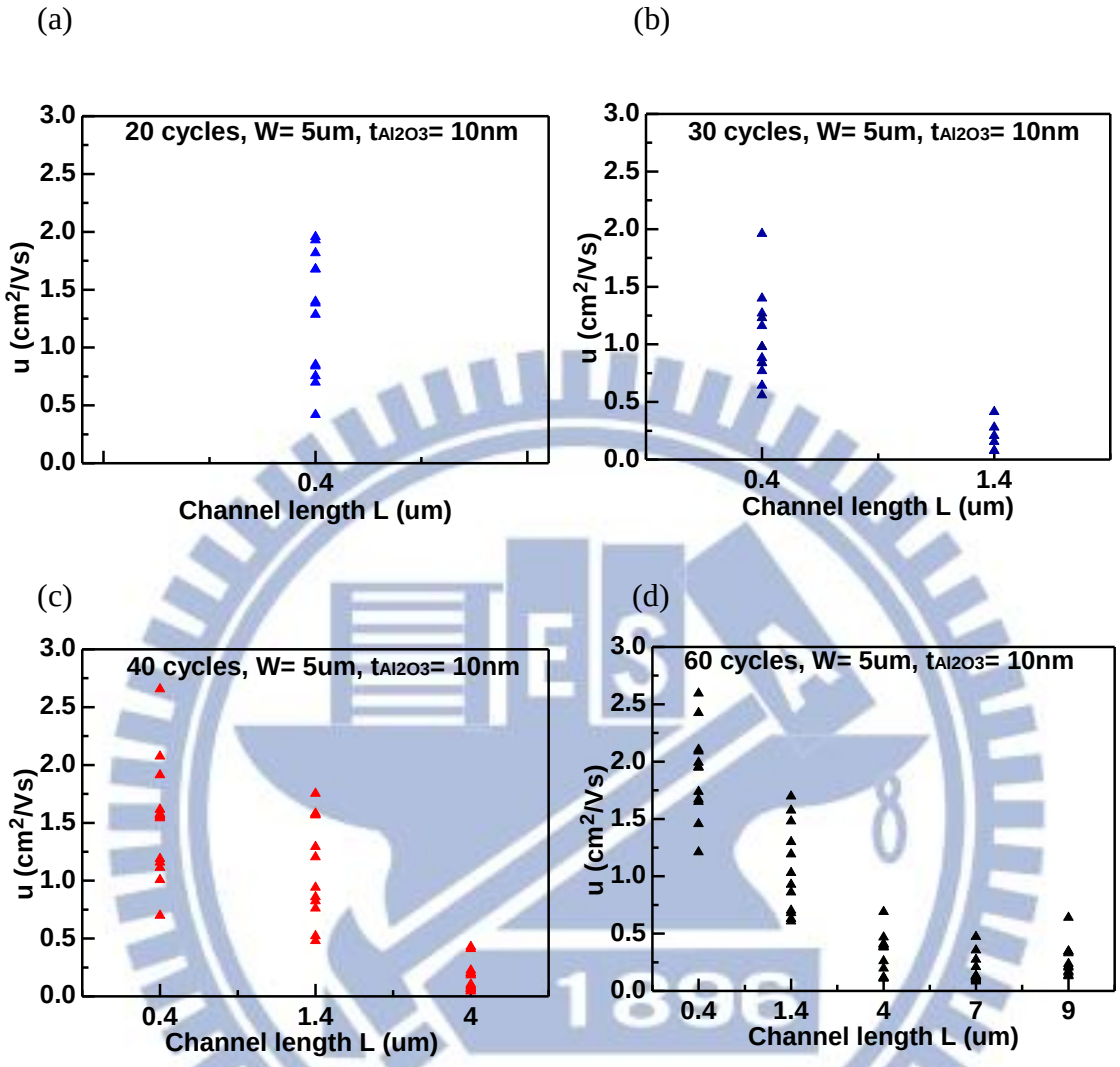


Fig. 3-29 Mobility was plotted against channel length for devices with channel width W= 50 μm and Al_2O_3 film of 5 nm for CNT coating density ranging from 20 to 60 cycles (a) CNT coating 20 cycles (b) CNT coating 30 cycles (c) CNT coating 40 cycles (d) CNT coating 60 cycles. Increasing channel length decreases mobility.

(a)

(b)

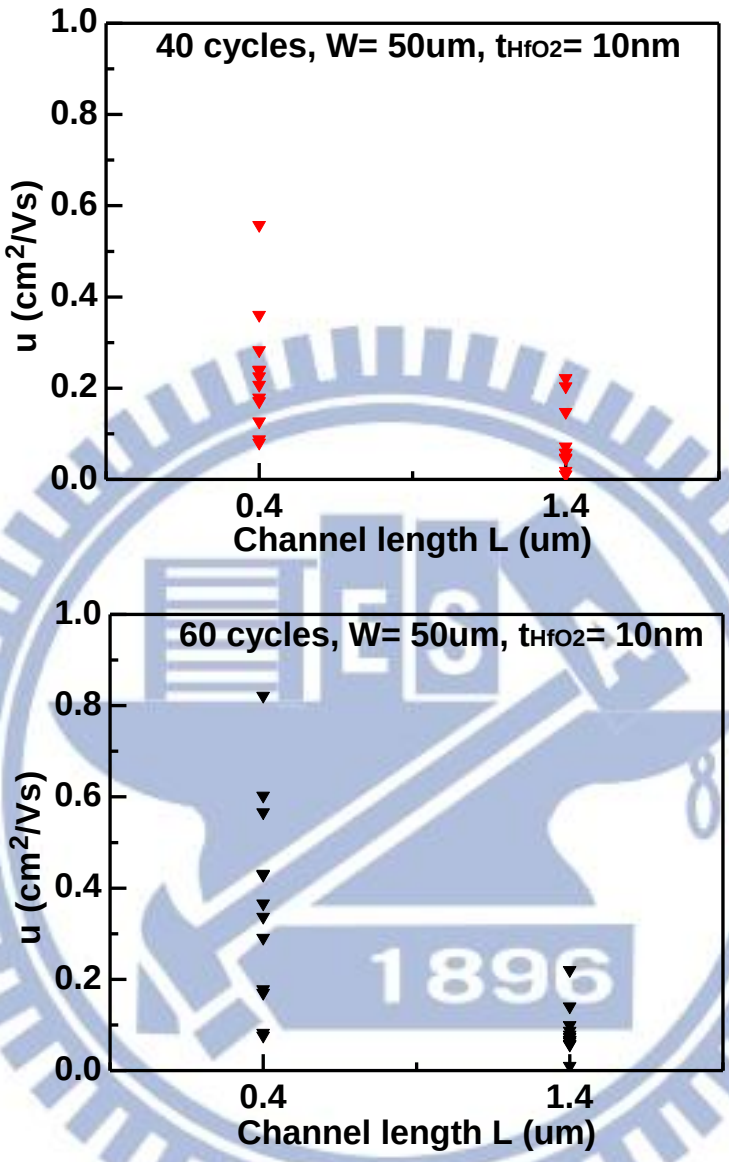
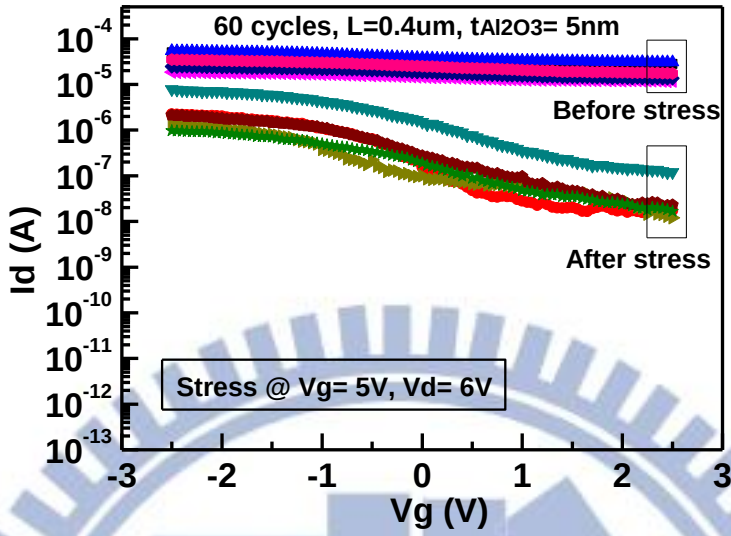


Fig. 3-30 Mobility was plotted against channel length for devices with channel width W= 50 μm and HfO_2 film of 10 nm for CNT coating density ranging from 40 to 60 cycles (a) CNT coating 40 cycles (b) CNT coating 60 cycles.

(a)



(b)

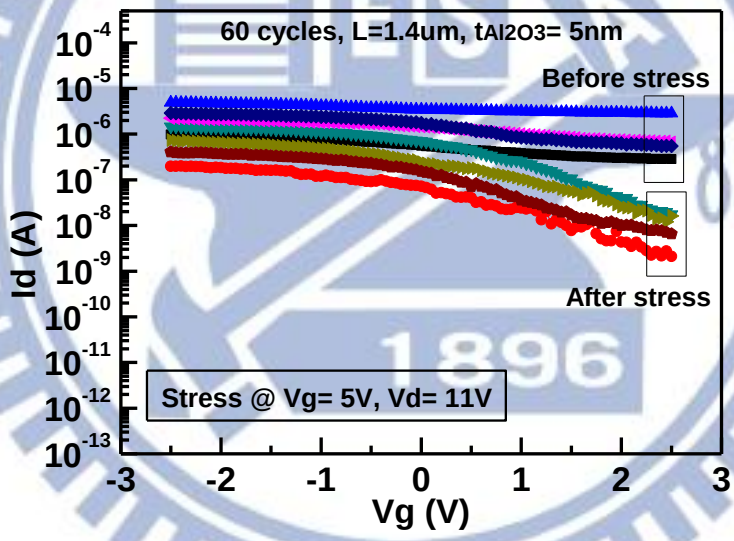
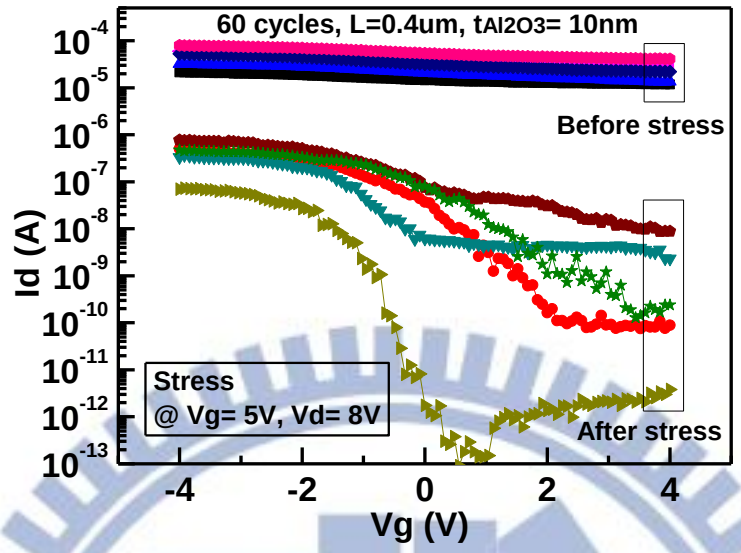


Fig. 3-31 Transfer characteristics (I_d vs. V_g) before and after applying adapted electrical breakdown method (device dimension of channel length L= 0.4 and 1.4 μm, fixed channel width W= 50 μm, and Al_2O_3 film of 5 nm) (a) L= 0.4 μm (b) L= 1.4 μm. By performing electrical breakdown method, on/off ratio improves 2 orders of magnitude.

(a)



(b)

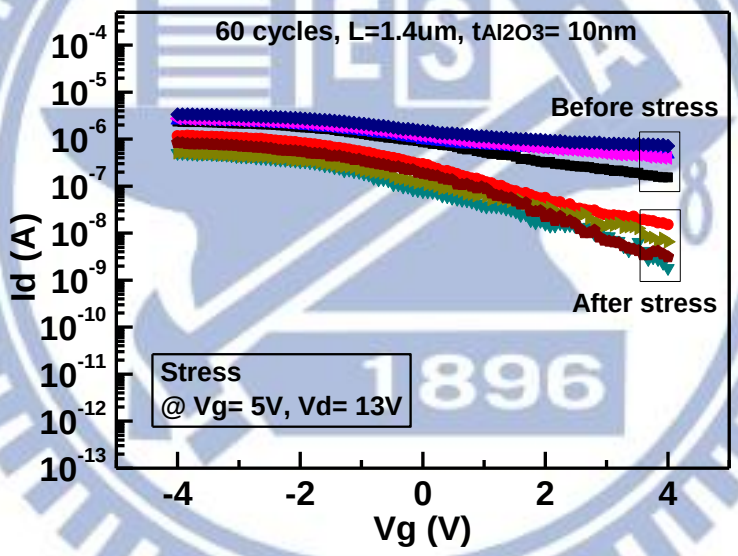


Fig. 3-32 Transfer characteristics (I_d vs. V_g) before and after applying adapted electrical breakdown method (device dimension of channel length L= 0.4 and 1.4 μm, fixed channel width W= 50 μm, and Al_2O_3 film of 10 nm) (a) L= 0.4 μm (b) L= 1.4 μm. On/off ratio improves more than 2 orders of magnitude with the increase of gate dielectric thickness.

Chapter 4

Summary and Future Works

4-1 Summary

This thesis studied the transport characteristics of percolating carbon nanotube network thin film transistor (CNTN TFT) with local bottom gate structure. We systematically analyzed the following effects including CNT density, CNT length, devices dimension, gate dielectric thickness, and different coating surfaces on device performance by applying percolation theory to CNT network. Monte Carlo simulations of percolation threshold in random CNT network were performed to compare to experimental results of CNTN TFTs.

The CNT network was fabricated by spin-coating method. The SEM images show that CNTs are dispersed without aggregation on Al_2O_3 film whereas the sparse CNT network coated on HfO_2 film is due to poor wet ability of HfO_2. Increasing CNT coating cycles by spin-coating method increases the number of CNTs and CNT conducting paths in the channel.

Since CNT network consists of semiconducting CNTs and metallic CNTs, there is a tradeoff between high on-state current and high on/off ratio. There are two extreme cases of transfer characteristics. One is devices with high on-state current of 10^{-5} A and low on/off ratio < 10, and another is devices with low on-state current of 10^{-8} A and high on/off ratio > 10^3. In between two extreme cases, devices with optimized performance could be fabricated by tuning appropriate device dimension and CNT coating density.

For the effects of CNT density and channel length on on-state current and on/off

ratio, electrical characterization of CNTN TFTs shows that increasing CNT coating density increases on-state current for all channel length ranging from 0.4 to 7 μm since the number of CNT conducting paths in the channel increases. Besides, increasing CNT coating density results in reduction of on-state current variation and increase of maximum conducting channel length. For CNT coating density of 20, 30, 40, and 60 cycles, the maximum CNT conducting path in the channel are 1.4, 4, 7, and 14 μm, respectively. Increasing channel length results in nonlinear decrease of on-state current since non-uniform coverage of CNT network in long channel length due to geometric rise of bottom gate which hinders CNTs coated on the channel. On/off ratio is also improved by increasing channel length.

For devices with short channel length L= 0.4 μm < average CNT length of 1 μm, high on-state current and low on/off ratio < 10 were obtained and not affected by CNT coating density since a single metallic CNT might connect the channel to increase both on-state and off-state current. As channel length L > average CNT length, once metallic CNT density exceeds percolation threshold for high CNT coating density of 60 cycles, device still exhibits metallic behavior, otherwise channel length is long enough (L> 7 μm) to prevent the formation of metallic conducting paths. If at least one semiconducting CNT exists in the conducting path, the device exhibits semiconducting behavior to improve on/off ratio > 10^3. The optimized CNT coating density for device with high on-state current and acceptable on/off ratio > 100 are 30, 40, and 60 cycles at channel length of 1.4, 4, and 7 μm, respectively in this thesis.

The channel width dependence of on-state current and on/off ratio shows that decreasing channel width results in decrease of on-state current and improvement of on/off ratio due to reduction of CNT conducting paths. It is noticed that decreasing on-state current is not proportion to decreasing channel width for long channel length L> 4 μm since that non-uniform CNT coverage affects conducting paths hard to form

in long channel. In addition, the effect of channel width on on/off ratio remains a certain value not varied with increasing channel length for L> 4 μm.

The gate dielectric thickness dependence of on-state current and on/off ratio is not obvious for devices with Al_2O_3 gate dielectric of 5 and 10 nm. The appropriate CNT coating density with higher on-state current and acceptable on/off ratio is the same for both devices. Note that decreasing gate dielectric thickness results in decrease of operate voltage, which is an advantage in terms of low power applications.

The CNT length dependence of on-state current and on/off ratio shows that long CNTs reduce the number of CNT intersections to decrease contact resistance in conducting paths. Therefore, on-state current increases significantly to 10^{-4} A. However, CNT coating density of 30 cycles is still too high to let devices exhibit metallic behavior. CNT coating density needs to be lower than 20 cycles to improve on/off ratio.

For the dependence of coating surface type including Al_2O_3 and HfO_2 gate dielectric layer on device performance, since poor wet ability of HfO_2 film attributes low CNT network coverage, devices with HfO_2 film achieve low on-state current, short conducting channel length, and high on/off ratio in contrast to devices with Al_2O_3 film.

Monte Carlo simulations of percolating CNT networks were also performed to obtain percolation threshold of random CNT networks for channel length ranging from 1.4 to 7 μm. Increasing channel length results in increase of percolation threshold. The simulation results of percolation threshold are 1.79, 2.75, and 3 CNTs/μm^2 for channel length L= 1.4, 4, and 7 μm, respectively, which are lower than CNT density determined by SEM images. Since we counted CNT segments as intact CNTs in SEM images, experimental results of percolation threshold deviate from

simulation results.

The effective field-effect mobility ranging from 0.01 to 2.7 cm^2/Vs is superior to mobility of organics. The normalized field-effective mobility is in a range of 1-270 cm^2/Vs since that CNT network coverage is lower than 1%. The normalized mobility is still lower than devices fabricated with single CNT due to the series Schottky barriers between CNT intersections. Reducing channel length and channel width both results in increase of field-effective mobility.

Adapted electrical breakdown method was performed to improve on/off ratio more than 2 orders of magnitude by applying high stress voltage to burn out metallic CNTs. Increasing channel length and gate dielectric thickness increases stress bias to remove metallic CNTs. This method is suitable for devices with channel length L< 4 μm.

4-2 Future Works

The CNT network is formed by spin-coating CNT solution on the substrate rather than grown on the substrate directly. That would avoid the substrate of CNTN TFT exposing to high temperature and then various substrates such as plastic substrate could be compatible with flexible and display process. The transport and flexible CNTN TFTs could be fabricated.

In order to improve on/off ratio, in addition to applying electrical breakdown method to selectively remove metallic CNTs, there are a variety of techniques including reducing the diameter of CNTs during CNT grow to increase the band gap of CNTs or separating metallic CNTs from semiconducting CNTs to suppress leakage current.

The mobility and on-state current improvement could be done by precisely

assembling an array of parallel semiconducting CNTs to enhance the drive current rather than randomly spreading CNTs. Since purity of 50% to 70% of CNT was used in thesis, using purity > 90% of CNT could also enhance mobility. In addition, decreasing the geometrical rise of bottom gate is also feasible to improve CNT coverage uniformity.

The determination of percolation threshold was done by performing Monte Carlo simulation. The random CNT networks were generated to examine the conducting path formation. Next step is assigning each CNT interaction a contact resistance and then the resistivity of CNT networks could be done by dividing the voltage drop between S/D contacts by total current flowing in conducting paths.

References

[1]. H. W. Kroto, J. R. Heath, S. C. O'Brien, R. F. Curl and R. E. Smalley, "C60: buckministerfullerene", Nature, vol. 318, pp. 162-163, 1985.

[2]. S. Iijima, "Helical microtubules of graphitic carbon", Nature, vol. 354, pp. 56-58, 1991.

[3]. S. Iijima and T. Ichihashi, "Single-shell carbon nanotubes of 1-nm diameter", Nature, vol. 363, pp. 603-605, 1993.

[4]. T. Wang Odom, J. Huang, P. Kim, and C. M. Lieber, "Atomic structure and electronic properties of single-walled carbon nanotubes", Nature, vol. 391, pp. 62-64, 1998.

[5]. R. Sen, B. C. Satishkumar, G. Raina, and C. N. R. Rao, "Structures and images of novel derivatives of carbon nanotubes, fullerenes and related new carbon forms", Taylor & Francis: Oxford, 1997.

[6]. J. W. G. Wildo, L. C. Venema, A. G. Rinzler, R. E. Smalley, and C. Dekker, "Electronic structure of atomically resolved carbon nanotubes" , Nature, vol. 391, pp. 59-62, 1998.

[7]. P. Avouris, J. Appenzeller, R. Martel, and S. J. Wind, "Carbon Nanotube Electronics", Proceedings of the IEEE, vol. 91, 2003.

[8]. R. Saito, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Electronic structure of chiral graphene tubules", Appl. Phys. Lett., vol. 60, pp. 2204–2206, 1992.

[9]. R. Saito, M. Fujita, G. Dresselhaus, and M. S. Dresselhaus, "Electronic structure of graphene tubules based on C_{60}", Phys. Rev. B, vol. 46, pp. 1804–1811, 1992.

[10]. A. Rakitin, C. Papadopoulos, and J. M. Xu, "Electronic properties of amorphous carbon nanotubes", Phys. Rev. B, vol. 61, pp. 5793-5796, 2000.

[11]. T. W. Ebbesen, and P. M. Ajayan, "Large-scale synthesis of carbon nanotubes", Nature, vol.358, pp. 220-222, 1992.

[12]. T. Guo, P. Nikolaev, A. Thess, D.T. Colbert, and R.E. Smalley, "Catalytic growth of single-walled nanotubes by laser vaporization", Chem. Phys. Lett., vol. 243, pp. 49-54, 1995

[13]. A. Thess, R. Lee, P. Nikolaev, H. Dai, P. Petit, J. Robert, C. Xu, Y.H. Lee, S.G. Kim, A.G. Rinzler, D.T. Colbert, G.T. Scuseria, D. Tomanek, J.E. Fischer, and R.E. Smalley, "Crystalline Ropes of Metallic Carbon Nanotubes", Science, vol. 273, pp. 483-487, 1996.

[14]. M. José-Yacamán, M. Yoshida, and L. Rendón, "Catalytic growth of carbon microtubules with fullerene structure", Appl. Phys. Lett., vol. 62, pp. 202-204,

1993.

[15]. N. Inami, M.A. Mohamed, E. Shikoh, and A. Fujiwara, "Synthesis-condition dependence of carbon nanotube growth by alcohol catalytic chemical vapor deposition method", Sci. Technol. Adv. Mater., vol. 8, pp. 292-295, 2007.

[16]. C. Bower, O. Zhou, W. Zhu, D.J. Werder, and S. Jin, "Nucleation and growth of carbon nanotubes by microwave plasma chemical vapor deposition", Appl. Phys. Lett., vol. 77, pp. 2767-2769, 2000.

[17]. Y. Li, D. Mann, M. Rolandi, W. Kim, A. Ural, S. Hung, A. Javey, J. Cao, D. Wang, E. Yenilmez, Q. Wang, J. F. Gibbons, Y. Nishi, and H. Dai, "Preferential growth of semiconducting single-walled carbon nanotubes by a plasma enhanced CVD method", Nano Lett., vol. 4, pp. 317-321, 2004.

[18]. A. Ural, Y. Li, and H. Dai, "Electric-field-aligned growth of single-walled carbon nanotubes on surfaces", Appl. Phys. Lett., vol. 81, pp. 3464-3466, 2002.

[19]. G. Zhang, X. Wang, X. Li, Y, Lu, A. Javey, and H. Dai, "Carbon nanotubes: from growth, placement and assembly control to 60 mV/decade and sub-60 mV/decade tunnel transistors", in *IEDM Tech. Dig.*, pp. 431-434, 2006.

[20]. M. A. Meitl, Y. Zhou, A. Gaur, S. Jeon, M. L. Usrey, M. S. Strano, and J. A. Rogers, "Solution casting and transfer printing single-walled carbon nanotube films", Nano Lett, vol. 4, pp. 1643-1647, 2004

[21]. Y. Zhou, A. Gaur, S. H. Hur, C. Kocabas, M. A. Meitl, M. Shim, and J. A. Rogers, "p-channel, n-channel thin film transistors and p-n diodes based on single wall carbon nanotube networks," Nano Lett., vol.4, pp.2031-2035, 2004.

[22]. Z. Chen, J. Appenzeller, Y.M. Lin, J. Sippel-Oakley, A. G. Rinzler, J. Tang, S. J. Wind, P. M. Solomon, and P. Avouris, "An integrated logic circuit assembled on a single carbon nanotube", Science, vol. 311, p. 1735, 2006.

[23]. Z.Wu, Z. Chen, X. Du, J. M. Logan, J. Sippel, M. Nikolou, K. Kamaras, J. R. Reynolds, D. B. Tanner, A. F. Hebard, A. G. Rinzler, "Transparent, conductive carbon nanotube films", Science, vol. 305, pp. 1273-1276, 2004.

[24]. Z. Li, P. Dharap, S. Nagarajaiah, E. V. Barrera, and J. D. Kim, "Carbon nanotube film sensors", Adv. Mater., vol. 16, pp. 640-643, 2004

[25]. J. K. Abraham, B. Philip, A. Witchurch, V. K. Varadan, and C. C. Reddy, "A compact wireless gas sensor using a carbon nanotube/PMMA thin film chemiresistor", Smart Mater. Struct., vol. 13, pp. 1045-1049, 2004.

[26]. M, E. Roberts, M, C. LeMieux, and Z, Bao, "Sorted and Aligned Single-Walled Carbon Nanotube Networks for Transistor-Based Aqueous Chemical Sensors," ACS Nano, vol. 3, pp. 3287–3293, 2009.

[27]. E. Gui, L. J. Li, K. Zhang, Y. Xu, X. Dong, X. Ho, P. S. Lee, J. Kasim, Z. X. Shen, J. A. Rogers and J. Mhaisalkar, "DNA Sensing by Field Effect Transistors

Based on Networks of Carbon Nanotubes", J. Am. Chem. Soc., vol. 129, pp. 14427-14432, 2007.

[28]. X. Tang, S. Bansaruntip, N. Nakayama, E. Yenilmez, Y. Chang and Q. Wang, "Carbon Nanotube DNA Sensor and Sensing Mechanism", Nano Lett., vol. 6, pp. 1632-1636, 2006.

[29]. S. Hong, and S. Myung, "Nanotube electronics: a flexible approach to mobility", Nature, vol. 2, pp. 207-208, 2007.

[30]. J. Hone, M. Whitney, C. Piscoti, and A. Zettl, "Thermal conductivity of single-walled carbon nanotubes", Phys. Rev. B, vol. 59, pp. R2514-R2516, 1999.

[31]. E. Pop, D. Mann, Q. Wang, K. Goodson, and H. Dai, "Thermal conductance of an individual single-wall carbon nanotube above room temperature", Nano Lett., vol. 6, pp. 96-100, 2006

[32]. M. R. Falvo, G. J. Clary, R. M. Taylor II, V. Chi, F. P. Brooks Jr, S. Washburn, and R. Superfine, "Bending and bucking of carbon nanotubes under large strain", Nature, vol. 389, pp. 582-584, 1997.

[33]. E. W. Wong, P. E. Sheehan, and C. M. Lieber, "Nanobeam mechanics: elasticity, strengthand toughness of nanorods and nanotubes", Science, vol. 227, pp. 1971-1975, 1997.

[34]. R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris, "Single-and multi wall carbon nanotube field-effect transistors", Appl. Phys. Lett., vol. 73, pp. 2447-2449, 1998.

[35]. S. J. Tans, A. R. M. Verschueren, and C. Dekker., "Room-temperature transistor based on a single carbon nanotube", Nature, vol. 393, pp. 49-52, 1998.

[36]. T. Durkop, S. A. Getty, E. Cobas, and M. S. Fuhrer, "Extraordinary Mobility in Semiconducting Carbon Nanotubes," Nano Lett., vol. 4, pp.35-38, 2004.

[37]. A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai, "Ballistic carbon nanotube field-effect transistors", Nature, vol. 424, pp. 654-657, 2003.

[38]. S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," Nature, vol. 393, pp. 49-52, 1998.

[39]. A. Javey, J. Guo, D. B. Farmer, Q. Wang, D. Wang, R. G. Gordon, M. Lundstrom, and H. Dai, "Carbon Nanotube Field-Effect Transistors with Integrated Ohmic Contacts and High-k Gate Dielectrics," Nano Lett., vol. 4, pp.447-450, 2004.

[40]. R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. Chan, J. Tersoff, and P. Avouris, "Ambipolar Electrical Transport in Semiconducting Single-Wall Carbon Nanotubes", Phys. Rev. Lett., vol. 87, pp. 256805-256808, 2001.

[41]. V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, "Carbon nanotube inter- and intramolecular logic gates", Nano Lett., vol. 1, pp. 453-456, 2001.

[42]. M. Bockrath, J. Hone, A. Zettl, P. L. McEuen, A. G. Rinzler, and R. E. Smalley, "Chemical doping of individual semiconducting carbon-nanotube ropes", Phys. Rev. B, vol. 61, pp. 10606 -10608, 2000.

[43]. M. Shim, A. Javey, N. Wong, S. Kam, and H. Dai, "Polymer functionalization for air-stable n-type carbon nanotube field-effect transistors," J. Am. Chem. Soc., vol.123, pp.11512-11513, 2001.

[44]. S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris, "Carbon Nanotubes as Schottky Barrier Transistors," Phys. Rev. Lett., vol.89, pp.106801-1-106801-4, 2002.

[45]. Z. Chen, J. Zppenzeller, J. Knoch, Y.M. Lin, and P.n Avouris,"The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors," Nano Lett., vol.5, pp.1497-1502, 2005.

[46]. Y. Zhang and H. Dai, "Formation of metal nanowires on suspended single-walled carbon nanotubes," Appl. Phys. Lett., vol.77, pp.3015-3017, 2000.

[47]. O.K. Varghese, P. D. Kichambre, D. Gong, K. G. Ong, E. C. Dickey, and C. A. Grimes, "Gas sensing characteristics of multi-wall carbon nanotubes" Sensors and Actuators B, vol.81, pp.32-41,2001.

[48]. K. Bradley, J. C. P. Gabriel, M. Briman, A. Star, and G. Gruner, "Charge Transfer from Ammonia Physisorbed on Nanotubes" Phys. Rev. Lett., vol.91, pp.218301-1-218301-4, 2003.

[49]. J. Kong, M. G. Chapline, and H. Dai, "Functionalized Carbon Nanotubes for Molecular Hydrogen Sensors,", Adv. Mater., vol.13, pp.1384-1386, 2001.

[50]. W. Kim, A. Javey, O. Vermesh, Q. Wang, Y. Li, and H. Dai,"Hysteresis caused by water molecules in carbon nanotube field-effect transistors," Nano Lett., vol.3, pp.193-198, 2003.

[51]. A. Zahab, L. Spina, and P. Poncharal "Water-vapor effect on the electrical conductivity of a single-walled carbon nanotube mat," Phys. Rev. B, vol.63, pp.10000-10003, 2000.

[52]. S.J. Han, J. Chang, A.D. Franklin, A.A. Bol, R. Loesing, D. Guo, G.S. Tulevski, W. Haensch, and Z. Chen, "Wafer Scale Fabrication of Carbon Nanotube FETs with Embedded Poly-gates," in *IEDM Tech. Dig.*, pp. 206-209, 2010.

[53]. S. Suzuki, and Y. Kobayashi, "Conductivity Decrease in Carbon Nanotubes Caused by Low-Acceleration-Voltage Electron Irradiation ", Japanese Journal of Appl. Phys., vol. 44, pp. L1498-L1501, 2005.

[54]. C. Jin, K. Suenaga, and S. Iijima, "Vacancy migrations in carbon nanotubes," Nano Lett., vol.8, pp.1127-1130, 2008.

[55]. X. Duan, C. Niu, V. Sahi, J. Chen, J. W. Parce, S. Empedocles, and J. L. Goldman,"High-performance thin-film transistors using semiconductor

nanowires and nanoribbons," Nature, vol.425, pp.274-278, 2003.

[56]. Y. Huang, X. Duan, Q. Wei, and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," Nature, vol.291, pp. 630-633, 2001.

[57]. H. Xin, and A. T. Woolley, "Directional orientation of carbon nanotubes on surfaces using a gas flow cell," Nano Lett., vol.4, pp.1481-1484, 2004.

[58]. H. Ko, and V.V. Tsukruk, "Liquid-crystalline processing of highly oriented carbon nanotube arrays for thin-film transistors," Nano Lett., vol.6, p.1443-1448, 2006.

[59]. M. Engel, J. P. Small, M. Steiner, M. Freitag, A. A. Green, M. C. Hersam, and P. Avouris, "Thin film nanotube transistors based on self-assembled, aligned, semiconducting carbon nanotube arrays", ACS Nano, vol. 2, pp. 2445–2452, 2008

[60]. W. J. Yu, U. J. Kim, B. R. Kang, H. Lee, E. H. Lee, and Y. H. Lee, "Adaptive logic circuits with doping-free ambipolar carbon nanotube transistors", Nano Lett., vol. 9, pp. 1401-1405, 2009.

[61]. A. D. Franklin, A. Lin, H.-S. Philip Wong, and Z. Chen, "Current Scaling in Aligned Carbon Nanotube Array Transistors With Local Bottom Gating," IEEE Elec. Dev. Lett., vol.31, pp.644-646, 2010.

[62]. N. Patil, A. Lin, E. R. Myers, K. Ryu, A. Badmaev, C. Zhou, H.S. P. Wong, and S. Mitra, "Wafer-scale growth and transfer of aligned single-walled carbon nanotubes," IEEE Trans. Nanotechnol., vol. 8, pp. 498–504, 2009.

[63]. E. S. Snow, J. P. Novak, P. M. Campbell, and D. Park, "Random networks of carbon nanotubes as an electronic material," Appl. Phys. Lett., vol.82, pp.2145-2147, 2003.

[64]. E. S. Snow, P. M. Campbell, M. G. Ancona, and J. P. Novak,"High-mobility carbon-nanotube thin-film transistors on a polymeric substrate", Appl. Phys. Lett., vol.86, pp. 033105-1-033105-3, 2005.

[65]. Y. Zhou, L. Hu, and G. Grüner, "A method of printing carbonnanotube thin films," Appl. Phys. Lett., vol.88, pp.123109-1-123109-3, 2006.

[66]. Z. Dai, L. Yan, S. M. Alam, J. Feng, P. R. D. Mariathomas, Y. Chen, C. M. Li, Q. Zhang, L.J. Li, K. H. Lim, and M. B. Chan-Park, "Selective Small-Diameter Metallic Single-Walled Carbon Nanotube Removal by Mere Standing with Anthraquinone and Application to a Field-Effect Transistor", J. Phys. Chem. C, vol. 114, pp. 21035-21041, 2010.

[67]. C. Wang, J. Zhang, K. Ryu, A. Badmaev, L. G. D. Arco, and C. Zhou, "Wafer-scale fabrication of separated carbon nanotube thin-film transistors for display applications", Nano Lett., vol. 9, pp. 4285-4291, 2009.

[68]. K.C. Narasimhamurthy and R. Paily, “High-performance local back gate thin-film field-effect transistors using sorted carbon nanotubes on an amino-silane treated hafnium oxide surface”, Semicond. Sci. Technol, vol. 26, pp. 075002-1-075002-11, 2011.

[69]. G. E. Pike and C. H. Seager, “Percolation and conductivity L A computer study. I,” Phys. Rev. B, vol. 10, pp. 1421-1434, 1974.

[70]. C. H. Seager and G. E. Pike, “Percolation and conductivity L A computer study. II,” Phys. Rev. B, vol. 10, pp.1435-1446, 1974.

[71]. Y.B. Yi and A. M. Sastry, “Analytical approximation of the two-dimensional percolation threshold for fields of overlapping ellipses”, Phys. Rev. E., vol. 66, pp. 066130-1-066130-8, 2002.

[72]. J. N. Coleman, S. Curran, A. B. Dalton, A. P. Davey, B. McCarthy, W. Blau, and R. C. Barklie, "Percolation-dominated conductivity in a conjugated polymer carbon nanotube composite," Phys. Rev. B., vol. 58, pp. R7492-R7495, 1998.

[73]. L. Hu, D. S. Hecht, and G. Gru1ner, “Percolation in Transparent and Conducting Carbon Nanotube Networks,” Nano Lett., vol. 4, pp.2513-2517, 2004.

[74]. H. E. Unalan, G. Fanchini, A. Kanwal, A. D. Pasquier, and M. Chhowalla, “Design Criteria for Transparent Single-Wall Carbon Nanotube Thin-Film Transistors,” Nano Lett., vol.6, pp. 677-682, 2006.

[75]. S. Kumar, J.Y. Murthy, and M. A. Alam,, “Percolating conduction in finite nanotube networks,” Phys. Rev. Lett., vol. 95, pp. 066802-1-066802-4, 2005.

[76]. A. Behnam and A. Ural, "Computational study of geometry-dependent resistivity scaling in single-walled carbon nanotube films," Phys. Rev. B, vol. 75, pp. 125432-1-125432-8, 2007.

[77]. J. Hicks, A. Behnam, and A. Ural, “Resistivity in percolation networks of one-dimensional elements with a length distribution”, Phys. Rev. E, vol. 79, pp. 012102-1-012102-4, 2009.

[78]. S. Seppälä, E. Häkkinen, M. J. Alava, V. Ermolov and E. T. Seppälä, “Electrical transport properties of percolating random networks of carbon nanotube bundles,” EPL, vol. 91, pp.47002-1-47002-6, 2010.

[79]. V. K. Sangwan, A. Behnam, V. W. Ballarotto, M. S. Fuhrer, A. Ural, and E. D. Williams, “Optimizing transistor performance of percolating carbon nanotube networks,” Appl. Phys. Lett., vol.97, pp. 043111-1-043111-3, 2010.

[80]. G. Zhang, P. Qi, X. Wang, Y. Lu, X. Li, R. Tu, S. Bangsaruntip, D. Mann, L. Zhang, H. Dai, ”Selective Etching of Metallic Carbon Nanotubes by Gas-Phase Reaction”, Science, vol. 314, pp. 974-977, 2006.

[81]. D. B. Farmer and R. G. Gorden, “ALD of high-k dielectrics on suspended Functionalized SWNTs”, Electrochemical and Solid-State Letters, vol. 8, pp.

89-91, 2005.

[82]. D. B. Farmer and R. G. Gorden, “Atomic layer deposition on suspended single-walled carbon nanotubes via gas-phase noncovalent functionalization”, Nano Lett., vol. 6, pp. 699-703, 2006.

[83]. The dielectric constant of Al_2O_3 and HfO_2 are determined by Dr. Jiun-Rung Su, nano facility center (NFC) researcher.

[84]. C. D. Dimitrakopoulos and P. R. L. Malenfant, “Organic thin film transistors for large area electronics”, Adv. Mater., vol. 14, pp. 99-117, 2002.

[85]. G.H. Gelinck, H.E.A. Huitema, E.V. Veenendaal, E. Cantatore, L.Schrijnemakers, J.B.P.H. Van Der Putten, T.C.T. Geuns, M. Beenhakkers, J.B. Giesbers, B.H. Huisman, E.J. Meijer, E.M. Benito, F.J. Touwslager, A.W. Marsman, B.J.E. Van Rens, and D.M. De Leeuw, “Flexible active-matrix displays and shift registers based on solution-processed organic transistors”, Nat. Mater., vol. 3, pp. 106-110, 2004.

Author’s Biography

姓名：陳定業

性別：男

生日：民國 76 年 2 月 20 日

學歷：

新北市立新泰國民小學 (82.9-88.6)

新北市立新莊國民中學 (88.9-91.6)

國立臺灣師範大學附屬高級中學 (91.9-94.6)

國立交通大學電子工程學系 (94.9-98.6)

國立交通大學電子研究所碩士 (98.9-100.6)

碩士論文題目：

交絡奈米碳管網路薄膜電晶體特性之研究

A Study on Thin Film Transistor Performance Based on Percolating Carbon Nanotube Networks