國 立 交 通 大 學

電子工程學系電子研究所

碩 士 論 文

銻化物高電子遷移率電晶體研究

Studies of Sb-based High Electron Mobility Transistors

研 究 生：李 孟 穎

指導教授：李 建 平

中 華 民 國 100 年 6 月

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研 究 生： 李孟穎　　　Student：Meng-Ying Li

指導教授： 李建平 老師　　　Advisor：Prof. Chien-Ping Lee

國 立 交 通 大 學

電子工程學系 電子研究所碩士班

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學生: 李孟穎　　　　　　　　　　　　指導教授: 李建平 博士

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摘要

這篇論文主要是研究銻(Sb)化物材料的高電子遷移率電晶體元件(HEMT)的開發。由於銻化物材料和砷化鎵(GaAs)基板之間的晶格差異很大，所以在使用分子束磊晶系統(MBE)的過程需要透過變晶成長的方式進行磊晶。藉由實驗我們成功成長出高電子遷移率的試片(22700cm2V-1s-1)。此外，對於閘極長度為 2um 的電晶體，傳導率(transconductance)為 730mS/mm。對於閘極長度為 50nm 的電晶體，其截止頻率(ft)和最大震盪頻率(fmax)分別為 50GHz 和 5GHz。

除此之外，由於銻化物材料本身的能帶間隙非常的小，因此元件在操作的過程很容易就產生碰撞游離，造成糾結效應(Kink effect)。本研究也展示了透過主動區的結構調整，可以加大能帶間隙，進而提高糾結效應所造成的軟性崩潰電壓(soft-breakdown voltage)。

Studies of Sb-based High Electron Mobility Transistors

Student: Meng-Ying Li   Advisor: Dr. Chien-Ping Lee

Institute of Electronics

National Chiao Tung Universty

Abstract

This thesis focuses on the development of Sb-based High Electron Mobility Transistor (HEMT). In this work, because of the large lattice mismatch, the Sb-based HEMT is grown on semi-insulating GaAs substrate by using metamorphic MBE growth. The best electron mobility we obtained is 22700$cm^2V^{-1}s^{-1}$ by experiments. In addition, the fabricated device showed the maximum transconductance is 730mS/mm at a high drain bias Vd=1.6V for a 2um gate length device. The cut-off frequency (*ft*) is 50GHz and the maximum oscillation frequency (*fmax*) is 5GHz for a 50nm gate length device.

Furthermore, due to the narrow band gap of Sb-based material, the device would generate impact ionization easily and cause the kink effect. This work also demonstrates the adjustment of the channel structure to enlarge the soft-breakdown voltage resulting from kink effect.

致謝

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最後，謹以此文獻給我摯愛的雙親，感謝你們能夠構將我扶養成人，在我的生涯中給予最適時的幫助與鼓勵。

李孟穎

於新竹交大

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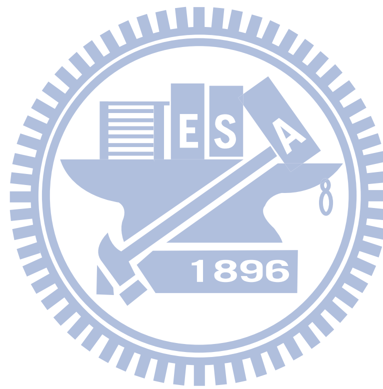

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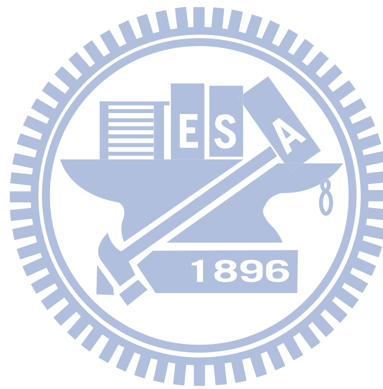


Chapter1. Introduction

1.1 InAs High electron mobility transistor

III-V compound semiconductors have been potential candidates for post-Si CMOS transistors due to their inherent high electron mobility. This characteristic also can be applied in the development of high-speed systems such as communications or data processing.

Values of the material properties often used in HEMT are listed in Table 1- 1 [1, 2, 3, 4], showing that III-V materials exhibit excellent electron mobility compared with Si. The electron mobility is 1000 cm^2/V-s in Si and 30000 cm^2/V-s in InAs, explains that III-V compound materials are available in high performance device.

Although Sb-based material (InAs, InSb) has excellent electron mobility, it's narrow band gap result in some drawbacks. From Table 1- 1, the energy band gap is 0.36eV in InAs and 0.18eV in InSb that could be easily breakdown by the impact ionization and accompany with large leakage. The channel design is important in order to improve the breakdown voltage. This work demonstrates the device by growing the InAs/InAsSb composite channel on GaAs substrates.

Because of the large lattice mismatch between Sb-based channel and the GaAs substrate, the buffer layers are necessary to reduce defect densities, which may severely degrade the qualities of the InAs/InAsSb channel. This work uses the a metamorphic buffer in order to approach the sample with high electron mobility.

	Si (100)	GaAs	InAs	InSb
Electron mobility (cm^2/Vs)	700 ($N=2x10^{17}cm^{-3}$)	7800 ($N=10^{15}cm^{-3}$)	30000 ($N=2x10^{16}cm^{-2}$)	80000 ($N=2x10^{15}cm^{-3}$)
Channel band gap (eV)	1.12	1.42	0.36	0.18
Lattice constant (Å)	5.43	5.65	6.06	6.48

Table 1- 1 Channel material properties at 300K

1.2 Outline of Thesis

The remainder of this thesis is organized as follows.

Chapter 2 demonstrates the epitaxy of InAs HEMT using the MBE system, including the substrate choice, buffer layer growing and channel layer design. Chapter 3 presents the process steps of fabricating the InAs HEMT, including the ohmic contact, mesa isolation and gate contact. In addition, the measurement methods are also presented in this chapter. Chapter 4 shows a serial of experiment results. The improvements in our research are shown and discussed. Chapter 5 is the conclusion about this thesis and the improvement in the future is shown in this chapter.

Chapter2. Epitaxy

2.1 Operation principle of InAs HEMT

Fig 2- 1 shows the band diagram of a conventional InAs High Electron Mobility Transistor (HEMT). Due to the large energy band gap and the condition of lattice-matched to InAs channel, the AlSb could be used as both the buffer and barrier layer. Due to the high mobility property, the narrow band gap InAs is used as the channel material.

With Te doping in the top AlSb barrier layer, electrons would transfer into the InAs channel due to the lower conduction band level compared with AlSb and create a two dimensional electron gas (2DEG). Due to the much reduced impurities scattering in channel, electrons can move quickly with very high mobility. The bottom AlSb is the buffer layer and could be used as the electron barrier to improve the confinement.

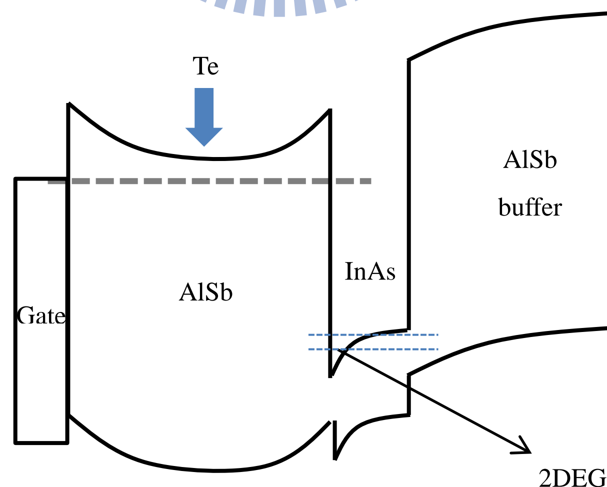


Fig 2- 1 The band diagram of the depletion-mode HEMT

Fig 2- 2 shows the operation of HEMT, the Source and Drain electrodes are ohmic contact. With a voltage applied between Source and Drain, electrons could acquire energy and flow in the active layer. The Schottky Gate electrode put between Source and Drain in order to modulate the channel. The gate bias is applied to change the conductivity of active layer. For a n-channel HEMT, applying a negative gate bias could deplete electrons in the channel and restrain the drain current, as shown in Fig 2- 3.

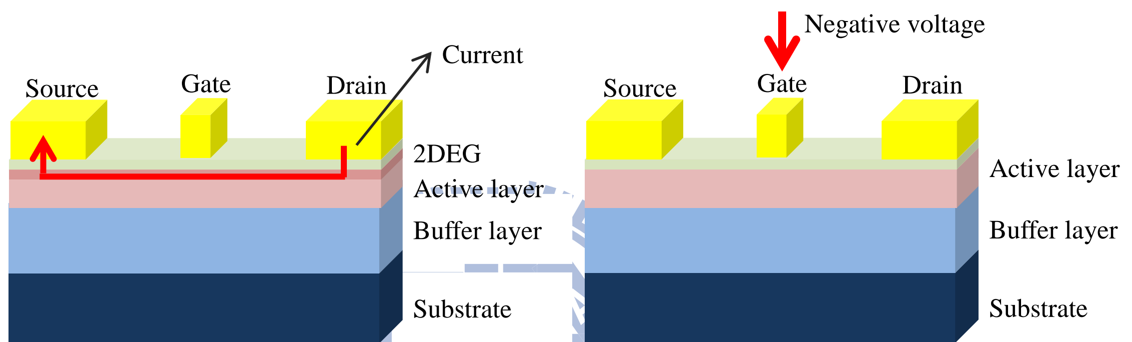


Fig 2- 2 The operating diagram of a depletion-mode HEMT

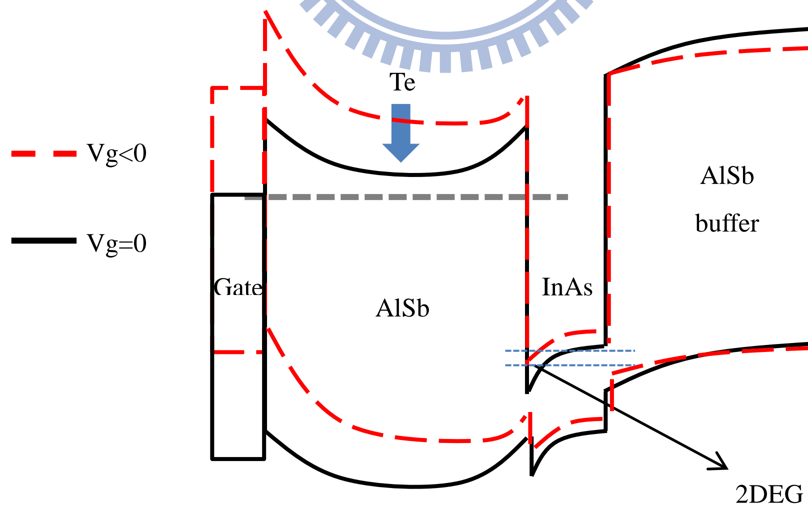


Fig 2- 3 The comparison of the band diagram with Vg=0 and Vg<0

2.2 Substrate choice

The first challenge in this research is the epitaxy. Although InAs has high electron mobility, there is no lattice-matched semi-insulating substrate available with this material. As shown in Fig 2- 4 [5], the other semiconductors with lattice constant close to InAs are GaSb and AlSb. GaSb, however, is conductive resulting from its narrow bandgap (0.73 eV). This characteristic will cause undesired leakage. AlSb, on the other hand, oxidizes easily in air and causes cracks in the device. For this reason, using lattice-mismatched semi-insulating substrate has been considered as a solution. InP (3.5% mismatch) and GaAs (7.2% mismatch) substrates are usually used.

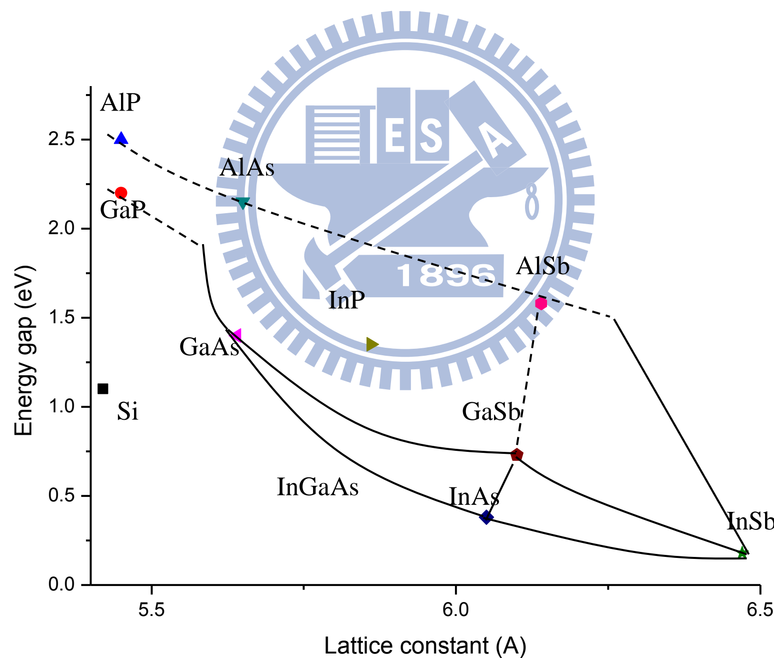


Fig 2- 4 The lattice constant and energy gap of III-V materials

In our study, we choose GaAs as the substrate due to the need of the future development. In the future post-Si generation, material integration becomes an important topic because of the limitation of Si. Integrating high electron mobility III-V material device layers to the Si substrate is one of the solutions to further

improve the n-MOSFET performance [6]. Nevertheless, there exists a very large lattice-mismatched (10.3% mismatch) between Si an InAs. Compared with InP, GaAs is closer to Si in the lattice constant and is suitable to be a research platform toward the device integration.

2.3 Buffer layer

With larger lattice constant in AlSb than in GaAs, there exist defects in the interface between these two materials. These defects could cause dislocations and thread up to the active layers. Furthermore, these dislocations also provide a path for carriers in the buffer layer and cause the buffer leakage.

However, the 7.2% mismatch between GaAs and InAs lattice constant still resulted in some problems such as dislocations and mobility degradations. The relaxed AlSb buffer layer between GaAs substrate and InAs channel can effectively suppress the dislocation densities extended to the InAs active layers and improve the channel material quality.

In this work, we approach the target with two methods: the Interfacial Misfit (IMF) and the Low Temperature buffer.

2.3.1 Interfacial Misfit (IMF) array [7]

To obstruct the thread dislocations, more than 2um of AlSb buffer is grown usually. However, the thickness of AlSb could be reduced for the efficiency.

At the compressive AlSb on GaAs interface, the IMF formation is initiated with an Sb soak. Each Sb atom forms a single bond with a bottom Ga atom and doesn't

react with the GaAs substrate to display the As atom, as shown in Fig 2- 5. A Sb-Ga bond skipped every 13 atomic sites which form the IMF array and results in the strain relief.

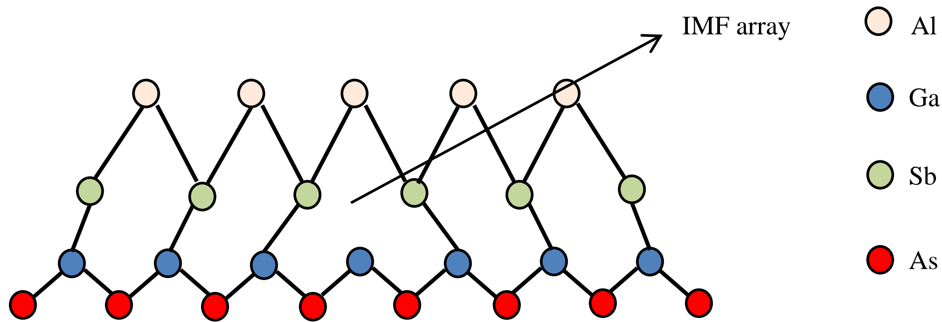


Fig 2- 5 The IMF array

The IMF relieves strain caused by the lattice-mismatched immediately at the compressive heterointerface. This advantage enables the AlSb buffer to be grown thinner than normal buffer without IMF array. Fig 2- 6 is the buffer structure by using the IMF array on the heterointerface in our work. After the As desorption and Sb soaking, the IMF array formation.

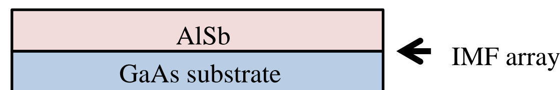


Fig 2- 6 Schematic of the buffer layer uses the IMF array

2.3.2 Low Temperature (LT) Buffer

By growing the AlSb layer in low temperature (<450 ℃), the AlSb buffer could form a 2-dimentional film similarly to the quantum dot layer to obstruct the threading dislocation. This is because the Sb atoms couldn't get enough energy on the wafer surface at the low temperature environment and vibrate weakly. As a result, these Sb

atoms are forced to cohere on the wafer and block the dislocations. But the LT AlSb buffer is very rough and may affect the active layer. So we cap a high temperature (HT) AlSb layer on the LT layer to smooth the surface, as shown in Fig 2- 7.

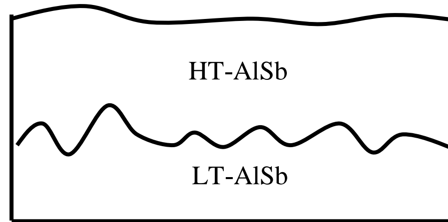


Fig 2- 7 Capping a HT-AlSb on a LT-AlSb to smooth the roughness

The structure in Fig 2- 7 could be seen as a LT-AlSb pair. Fig 2- 8 is one of the LT-Ab buffer structures in our work. We grow a number of pairs with total thickness 600nm on the IMF array.

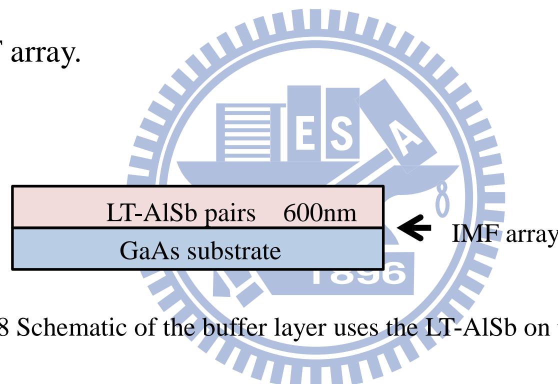


Fig 2- 8 Schematic of the buffer layer uses the LT-AlSb on the IMF array

2.4 Channel design

The InAs/AlSb HEMT with high speed performance comes from the fast electron transport properties of the InAs channel. But there consists a trade-off: device would suffer breakdown easily due to the narrow energy band gap of InAs, as mentioned in Chapter 1. In the device operation, electron gains energy from the high field region between the gate and drain. When the energy of electron is excess the band gap of the channel (0.36eV), it can generate electron-hole pair causing from impact ionization. Furthermore, due to the type II heterojunction of the InAs/AlSb, the impact-ionized holes would flow to everywhere due to the lack of holes

confinement, causing the gate leakage and kink effect.

In order to resolve the disadvantage of the type II heterojunction and improve the breakdown voltage, we design the $InAs/InAs_{0.7}Sb_{0.3}$ composite channel [8], as shown in Fig 2- 9. With the nearly lattice-matched AlSb, which has a conduction band offset of 1.35eV and a valance band offset of 0.05eV relative to $InAs_{0.7}Sb_{0.3}$, the AlSb/ $InAs_{0.7}Sb_{0.3}$/AlSb structure could be seen as a type I heterojunction. This means the confinement of hole would be better than AlSb/InAs/AlSb heterostructure.

But the energy band gap of $InAs_{0.7}Sb_{0.3}$ (0.26eV) is smaller than which of InAs (0.36eV). As a result, we insert a InAs layer into the $InAs_{0.7}Sb_{0.3}$ structure in order to enlarge the effective band gap in this structure.

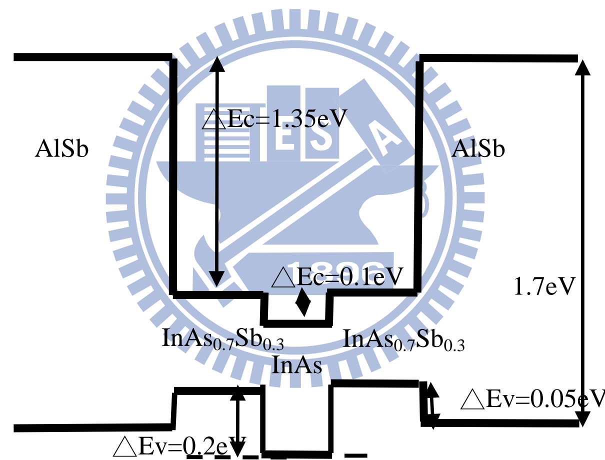


Fig 2- 9 The band alignments for the InAs/InAsSb composite channel

One of the structures in our design is shown in Fig 2- 10. The top layer of $InAs_{0.7}Sb_{0.3}$ is 3nm. The inserted InAs and bottom $InAs_{0.7}Sb_{0.3}$ layers are both 6nm.

Layer	Thickness
AlSb	15nm
$InAs_{0.7}Sb_{0.3}$	3nm
InAs	6nm
$InAs_{0.7}Sb_{0.3}$	6nm
AlSb	15nm

Fig 2- 10 Schematic of the structure of the InAs/InAsSb composite channel

2.5 Doping design

Fig 2- 11 shows the difference between ordinary doping and modulation doping. With dopants exist in the channel, electrons would transport slowly due to the scattering with the ionized dopants. In order to achieve high electron mobility in the InAs channel, we use the modulation doping to avoid the impurity scattering.

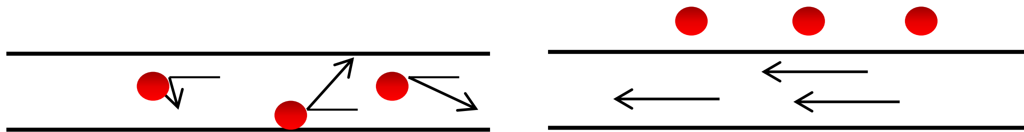


Fig 2- 11 The diagrams for normal doping and modulation doping

We have designed uniform doped structures in this work. One of the uniform doped structures in our design is shown in Fig 2- 12. A 5nm of the AlSb spacer is the InAs/$InAs_{0.7}Sb_{0.3}$ composite channel. Than a 5nm of the AlSb layer doped with Te dopant in the temperature of SnTe=300°C. Finally, a 5nm of the AlSb is capped on the doped layer as the barrier.

Layer	Thickness
AlSb	5nm
AlSb : Te	5nm
AlSb	5nm
Composite channel	15nm

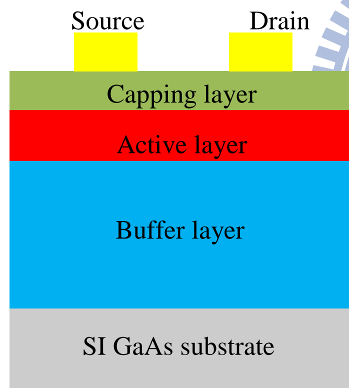
SnTe: 300°C

Fig 2- 12 Schematic of the structure of the uniform doped structure

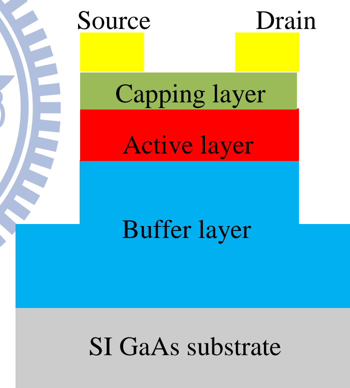
Chapter3. Device Process and measurement

The Fig 3- 1 shows the InAs HEMT process flow. The first step is the ohmic contact with mask#1. The second step is the mesa isolation with mask#2. After etching through the active layer, the SiN passivation is used to present the oxidation in the buffer layer. The third step is the gate contact by using the DUV or E-beam.

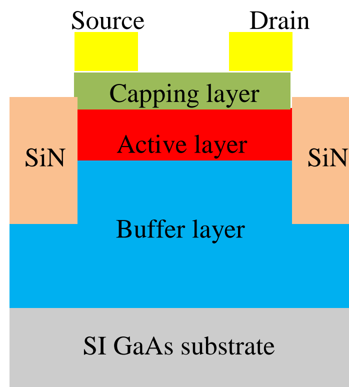
(1) Ohmic contact (mask #1)



(2) Mesa isolation (mask #2)



(3) Passivation



(4) Gate contact (mask #3)

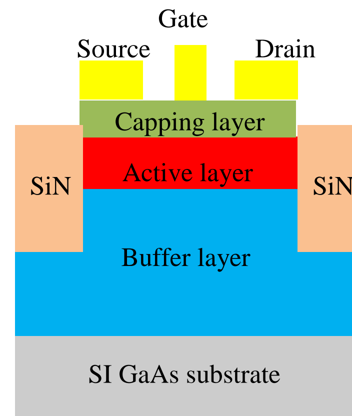


Fig 3- 1 Schematic of the fabrication process for the InAs HEMT

3.1 Photolithography: image reversal process

The photolithography is used in the large patterns: Ohmic contact, Mesa isolation and gate (2um) contact.

In our work, we use AZ5214E photoresist (PR). It's a positive PR but also can be used for the image reversal. This reversal procedure is shown in Fig 3- 2:

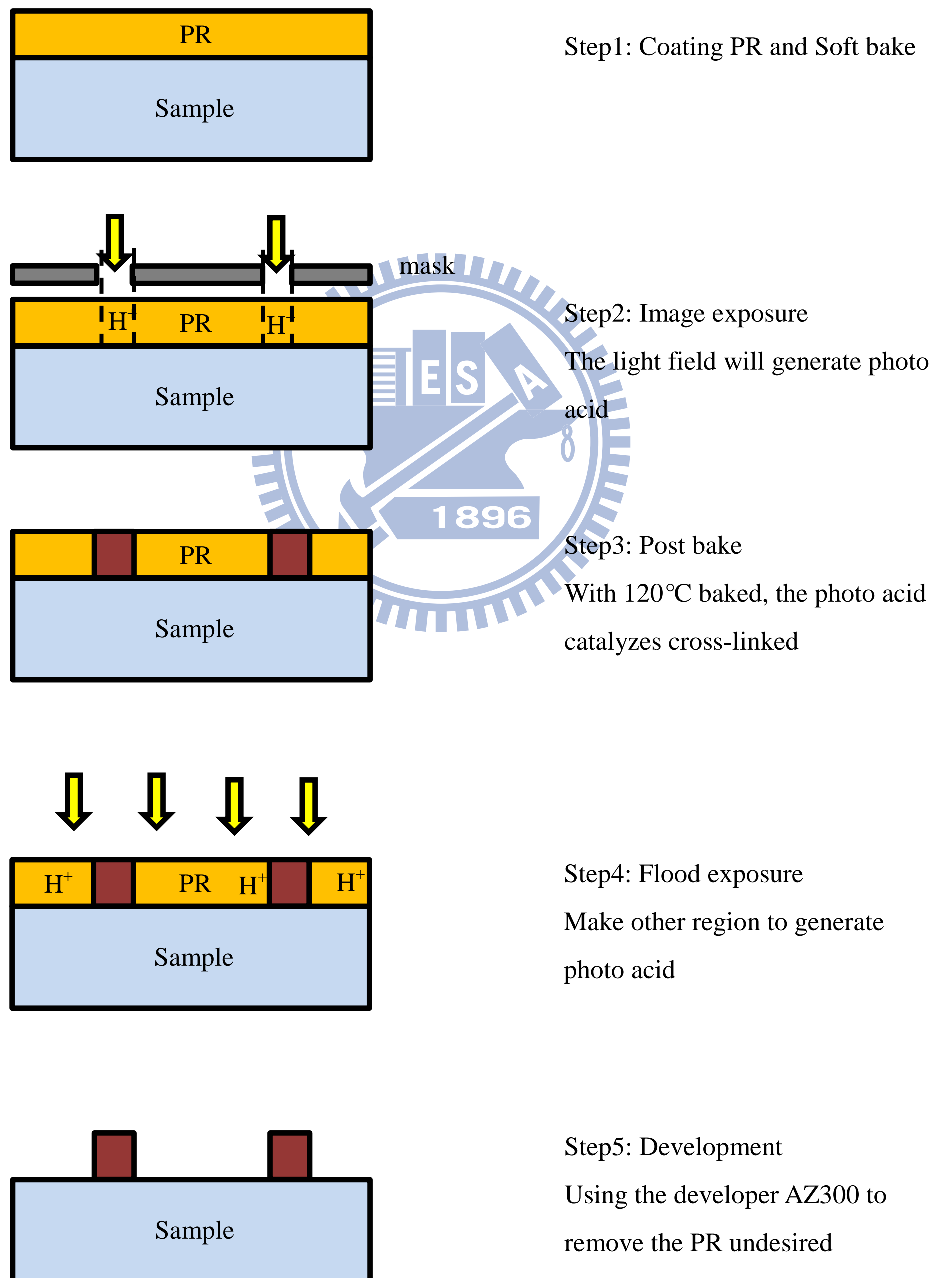


Fig 3- 2 Schematic of the lithography

3.2 Ohmic contact

The work function between the contact metal and the semiconductor plays an important role on the ohmic contacts. Compared with the low sheet resistance in the InAs channel, the contact resistance may account for a large proportion of the input resistance and affect the drain current. In order to reduce this influence, many steps are necessary:

3.2.1 UV-ozone

There may contain some residual PR on the sample surface after the photo-lithography. However, this residual PR will affect the contact condition between metal and sample, and lead to the increase of the contact resistance. As Fig 3- 3 shows, the UV-ozone PR stripper could generate through the UV light. The residual PR could be cleaned by O_3 gas environment under an elevated temperature.

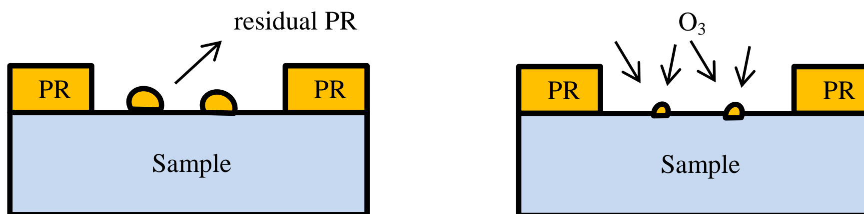


Fig 3- 3 Schematic of the effect for the UV-ozone

3.2.2 Dip

The native oxide existing on the surface could increase the contact resistance. So before the metal deposition, sample needs to be dipped in the HCl solution and remove the native oxide.

3.2.3 Metal evaporation

The ohmic contact metal is Pd/Ti/Pd/Au. With 4nm $In_{0.5}Al_{0.5}As$ cap layer on the sample surface, we choose Pd as the contact metal due to its work function is available for ohmic contact. Followed by 100 Å Pd, the Ti was deposited with 300 Å to be a binding layer. The 2000 Å Au is capped on the top layer as the contact pad.

3.2.4 Lift-off

With the photolithography, the PR on the sample formats a pattern, which we called Stencil-layer. After the metal evaporation, the whole surface is covered with the metal. Soaking samples with Acetone solution to dissolve the PR could remove the metal undesired. After the lift-off process, the contact metal of source and drain has been deposited on the surface.

Whether the lift-off is smooth or not depend on the sidewall profile of the PR. If the profile is overcut, as Fig 3- 4a shows, the metal may link together and makes the lift-off more difficult. The better profile for lift-off is undercut, like Fig 3- 4b shows. Acetone can infiltrate to the PR and dissolve it easily. In appropriate conditions, the AZ5214E can form the undercut profile after the reversal procedure.

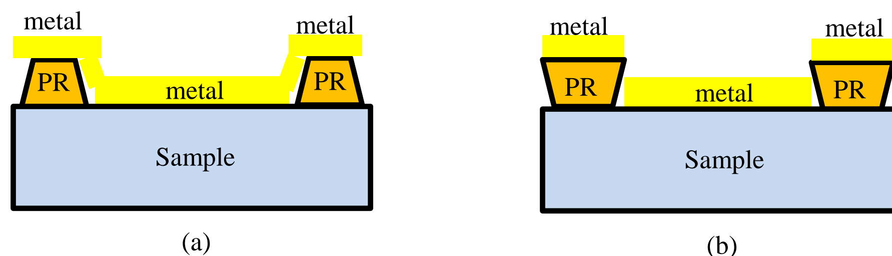


Fig 3- 4 Schematic of the metal deposition between the overcut and the undercut

In addition, the temperature of E-gun chamber is also a variable factor for the lift-off. During the metal evaporation, the high temperature would change the PR profile from undercut into overcut. Moreover, the PR may deteriorate and can't remove with Acetone. So during the E-gun evaporation, cooling is necessary to keep the PR's profile and quality.

3.2.5 Rapid thermal anneal (RTA)

The RTA process could enhance the contact condition and reduce the contact resistance. After a low temperature anneal at 180°C for 30 seconds, the Pd would be diffused into the semiconductor and be closer to the active layer, as illustrated in Fig 3- 5. Furthermore, in order to avoid surface oxidation of the contact metal, the nitrogen (N2) or Forming gas (97% N2 + 3%H2) flow is used during the RTA.

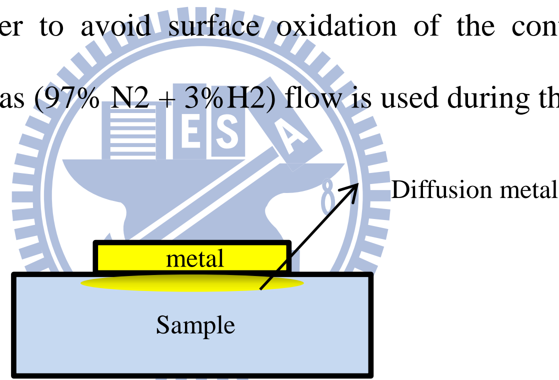


Fig 3- 5 The schematic diagram of the metal diffusion after annealing

3.3 Mesa isolation and Passivation

After the lift-off, we define the active region with the contacts of source and drain. The second step in the fabrication of the HEMT is Mesa isolation. This step is to separate devices by etching through the active layer so that all of them could work independently.

In this work, we attempt to accomplish the mesa isolation through the wet etching or dry etching.

3.3.1 Wet etching

At first, we choose wet etching by using the selective wet chemical etchants. Through the etch test the etching rate of the selective etchant (HF: H_2O_2: H_2O = 4: 1: 100) is 4nm/s. But the lateral etching is very serious, causing the sloped sidewall (Fig 3- 6). Therefore, we couldn't perform deep etch by using the wet etching to obtain a good isolation.

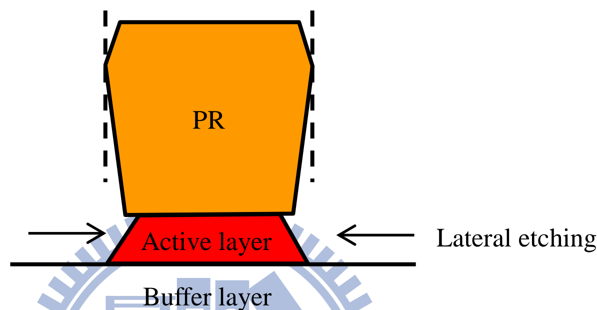


Fig 3- 6 Schematic of the lateral etching by the wet etching

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3.3.2 Inductively Couple Plasma (ICP) dry etching

The mechanism of dry etching is related to ion-bombardment. The plasma induced high-energy ions which would hit the sample, removing portions of the surface. Different from the wet etching, this physical etching is anisotropic and the sidewall profile can be very vertical.

But the ion-bombardment, however, has a low selectivity and the etching rate is slow. So the reactive ion etch (RIE) has been used for the dry etching. By adding some specific gases into the chamber, a radical would be induced from the plasma. After the ion-bombardment, the lattice of the surface is damaged and the radical reacts with the materials on the surface chemically. This reaction enhances the etching selectivity and etching rate. In this fabrication, we use $SiCl_4$ as the radical source and

Ar for ion-bombardment, as illustrated in Fig 3- 7.

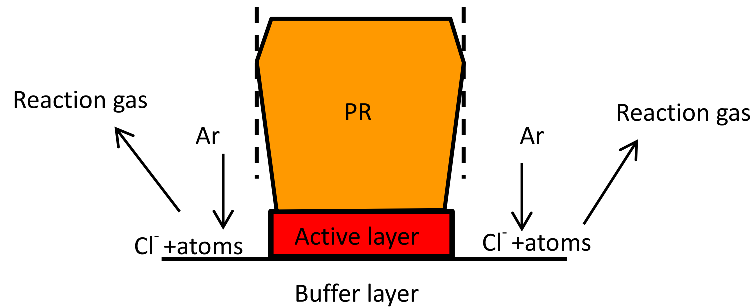

Fig 3- 7 Schematic of the vertical profile for the dry etching

3.3.3 AlSb oxidation

Because this is the first attempt in our group to fabricate InAs HEMT, we encounter lots of problems we have never seen before. The oxidation of AlSb is one of them. With extreme reactivity in air, AlSb buffer layer would oxidize immediately after the mesa etching and moreover, epitaxial layers would then crack completely. Capping an $Al_{0.7}Ga_{0.3}Sb$ layer on the AlSb buffer is a solution for this problem.

3.3.4 SiN passivation

In order to isolate AlSb from the air, we deposit a low-temperature SiN film on the surface immediately after mesa etching. Without additional lithography, the PR as the mesa etching mask also could be used as the passivation mask.

The Plasma-enhanced chemical vapor deposition (PECVD) is suitable for this fabrication because it could deposit SiN with high quality. But if the sidewall is sloped after wet etching like Fig 3- 8a shows, the SiN couldn't cover AlSb completely and oxygen would invade into the AlSb layer through this path. As a result, this is one factor that we used dry etching for better passivation.

After the deposition of SiN, using Acetone to remove the PR and the active region could be exposed for future treatments.

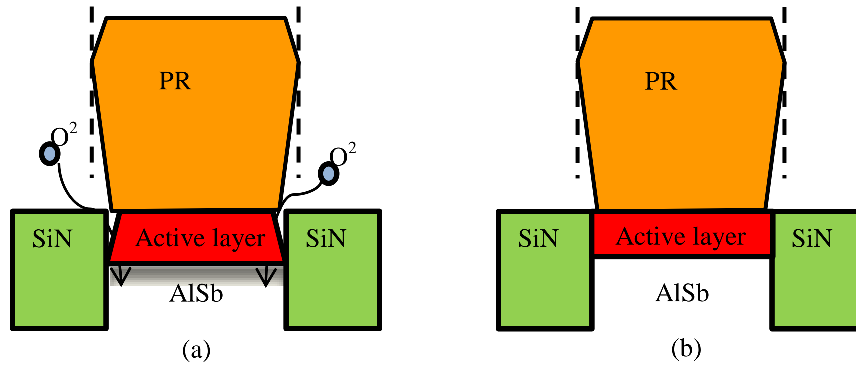

Fig 3- 8 Schematic of the SiN passivation for different etching

3.4 Gate contact

The next fabrication for HEMT is gate metal contact. Compared with the Ohmic contact of source and drain, the gate should be Schottky contact in order to modulate the drain current. In the operation of HEMT, a reverse bias for gate is applied to deplete electrons in the InAs channel and forbid the current. With Schottky contact, the voltage drop mainly on the channel region rather than on serial resistance. Furthermore, the gate leakage plays an important role on the drain current when the operation is near pinch-off. The Ti is available as the contact metal to form the Schottky barrier due to its work function.

We fabricate two kinds of gate length with different methods: the photo lithography for large gate fingers (~2 um) and the E-beam lithography for narrow gate fingers (<0.2 um).

In the photo lithography, due to the weak adhesion between the AZ5214E PR and the SiN, HMDS is used as a link layer.

The resistance of a conductor can be computed as

$$R = \rho \frac{L}{A} \tag{3-1}$$

where ρ is the electrical resistivity, L is the length and A is the cross-section area of the conductor. With the small cross-section area in the narrow gate finger, the serial resistance would be very large. As a result, the T-gate structure is a solution by increasing the cross-section area. In the E-beam lithography, Bi-layer process shows in Fig 3- 9 could form the undercut profile easily.

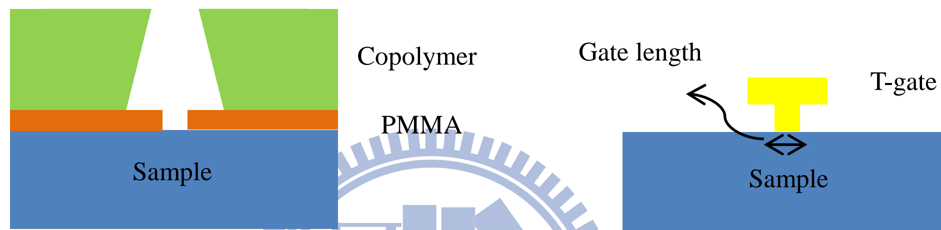

Fig 3- 9 Schematic of the T-gate PR profile for E-beam

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3.5 Measurement

3.5.1 Transfer Length Method

The transfer length method (TLM) is used to measure the contact resistance and channel sheet resistance. In Fig 3- 10, different spacing of metal contacts constitute as a TLM pattern. The total serial resistance between any neighbor contacts is

$$R_t = R_s \frac{l}{Z} + 2R_c \tag{3-2}$$

where R_s is the sheet resistance of the sample, Z is the width of the metal pad, l is the spacing between the pads and R_c is the contact resistance.

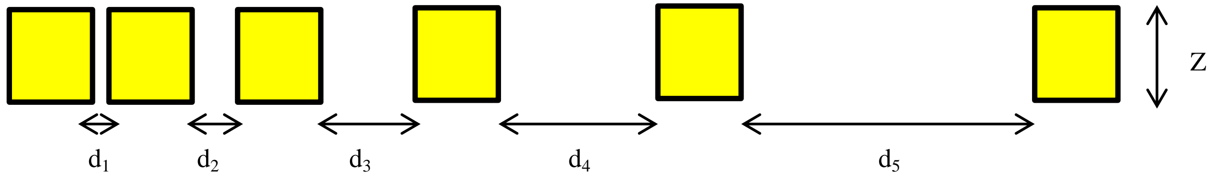


Fig 3- 10 The diagram of the TLM pattern

The TLM is to measure the total resistance in different constant spacing d_1, d_2, d_3, d_4, d_5. After that, we could get the correlation between the total serial resistance and the spacing, as Fig 3- 11 shows. The resistance increases linearly with the spacing and from (3-2), we could get sheet resistance R_s from the slope and contact resistance R_c from the intercept with Y-axis.

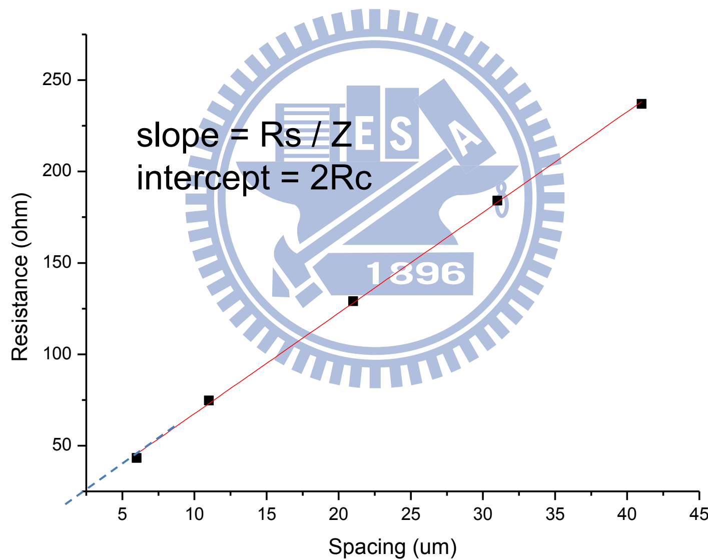


Fig 3- 11 The resistance measuring by the TLM pattern is linear to the spacing

3.5.2 Hall measurement

The carrier concentration (Ns) and electron mobility (μ) are considered as quality checks of the epitaxy. Hall measurement is the most common method to measure these two parameters.

We fabricate Hall-bar (Fig 3- 12) for Hall measurement. After ohmic contact and

mesa, the Hall-bar defines a straight path for current and vertical pins for voltage measurement.

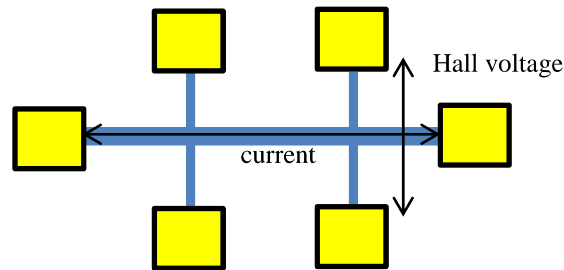


Fig 3- 12 The diagram of the Hall-bar pattern

Moving charge carriers would be affected by Lorentz force (Eq. 3-3) in a magnetic field and a Hall voltage V_H appears in a direction perpendicular to both the current and the magnetic field, shown in Fig 3- 13. From the V_H, we could obtain Hall coefficient (R_H) and estimate the carrier concentration (Eq. 3-4) and electron mobility (Eq. 3-5).

$$\vec{F} = q[\vec{\boldsymbol{E}} + (\vec{\boldsymbol{v}} \times \vec{\boldsymbol{B}})] \quad (3\text{-}3)$$

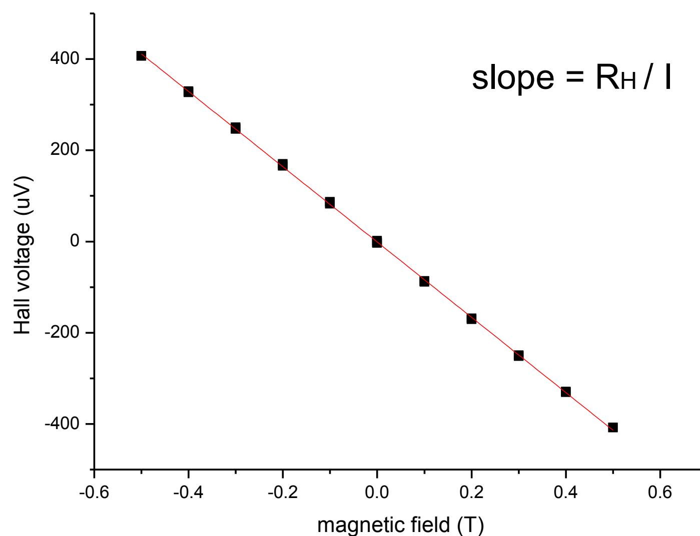


Fig 3- 13 The Hall voltage is linear to the magnetic field

$$Ns = \frac{-1}{qR_H} \tag{3-4}$$

$$\mu = \frac{1}{qR_S N_S} \tag{3-5}$$

3.5.3 Buffer leakage check

The buffer leakage responds to the quality of the buffer layer directly. With the better quality, the resistance of the buffer layer is larger and therefore, contributes to less buffer leakage in the device operation. Similar to the Hall-bar pattern, the buffer leakage check pattern is fabricated with ohmic contact and mesa. As presented in Fig 3- 14, the active layer is etched and current could only flow in the buffer layer. We could measure this buffer leakage by applying a fixed voltage.

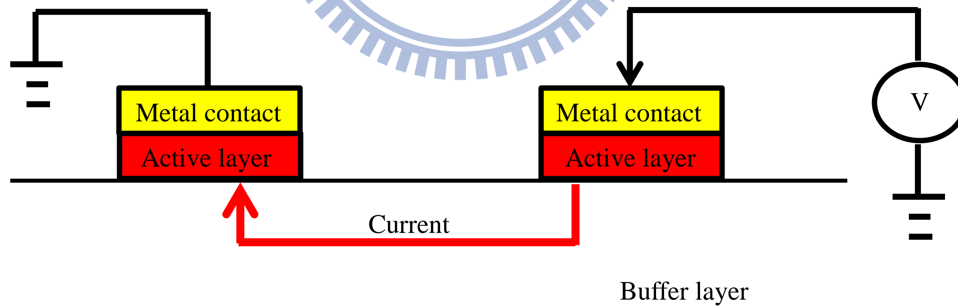


Fig 3- 14 The schematic of the measurement for the buffer leakage

3.5.4 Depletion-mode FET

As mentioned in Chapter 2, the InAs HEMT operates in the depletion mode. The drain is biased with positive voltage and the gate is biased with negative voltage, as Fig 3- 15 shows.

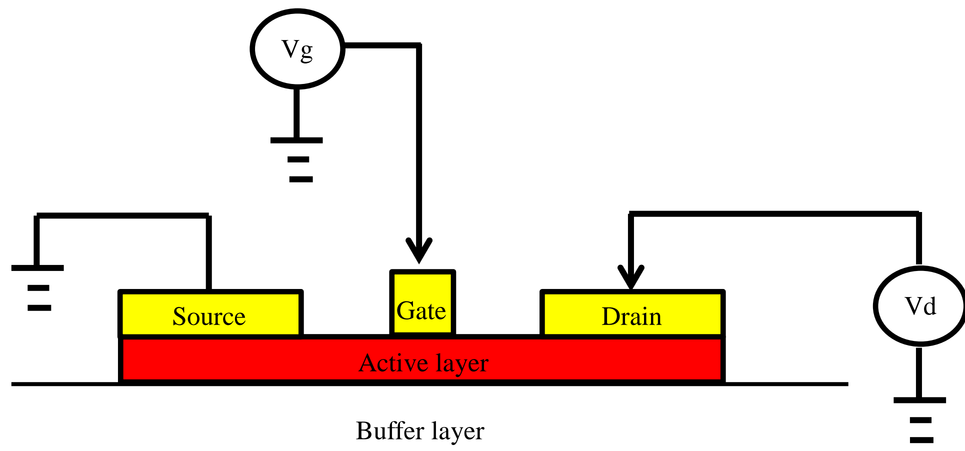
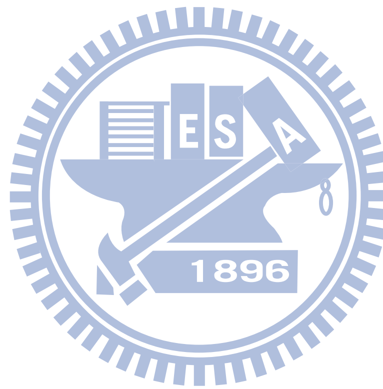


Fig 3- 15 The schematic of the measurement for the HEMT



Chapter4. Experiment result and discussion

4.1 Buffer layer and isolation improvement

4.1.1 AlSb/GaSb Supper lattice

This is the first attempt for us to fabricating InAs HEMT, so the first step is to solve the epitaxial problems of Sb-based materials. The metamorphic buffer is the first but not least problem. After many attempts trying to improve the epitaxy quality of buffer layer, we obtain a lot of experience and some preliminary results as follows.

At first, we try to apply ten pairs of AlSb/GaSb supper lattice [9] in the buffer layer to obstruct the thread dislocations causing from the lattice mismatch between GaAs substrate and Sb-based active layer. Fig 4- 1 shows the sample structure of Rn694 and the I-V curve of a device which width is 100um and gate length is 2um. As a result, no gate modulation could be observed. We attribute this to the large buffer leakage. Thus, the AlSb/GaSb Superlattice buffer cannot obstruct the dislocation resulting from the lattice mismatch between the GaAs substrate and AlSb buffer.

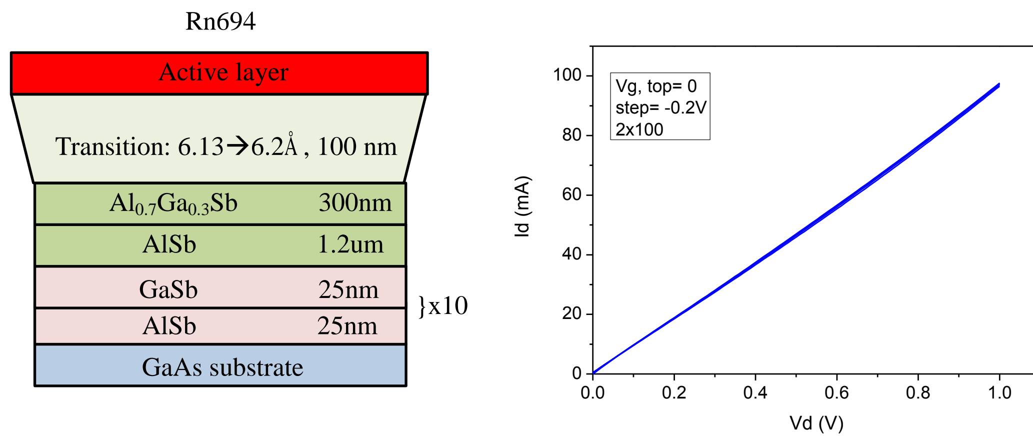


Fig 4- 1 Schematic of the supper lattice buffer grown on GaAs substrate and the device operation

We performed another experiment to further study the influence of AlSb/GaSb Superlattice, as shown in Fig 4- 2. We etch to every layer and estimate their sheet resistance with four-point probe. In Fig 4- 2 we could see that the resistance of the $Al_{0.7}Ga_{0.3}Sb$ layer is lower with the AlSb/GaSb supper lattice. Thus, from the above results, the AlSb/GaSb Superlattice isn't necessary for the buffer layer.

Rn706

Layer	Thickness	Sheet resistance
Active layer		
$Al_{0.7}Ga_{0.3}Sb$	300nm	(~350Ω/□)
AlSb (HT)	200nm	(~4.8kΩ/□)
GaSb	25nm	}x10
AlSb	25nm	
AlSb (HT)	900nm	(>40kΩ/□)
AlSb (LT)	100nm	
GaAs substrate		

Rn735

Layer	Thickness	Sheet resistance
Active layer		
$Al_{0.7}Ga_{0.3}Sb$	300nm	(~1.7kΩ/□)
AlSb (HT)	1.6um	(>40kΩ/□)
AlSb (LT)	100nm	
GaAs substrate		

Fig 4- 2 Schematic of the LT buffer grown on GaAs substrate and the sheet resistance of each layer

4.1.2 LT AlSb buffer

In order to improve the resistance of buffer layer, we tried a different approach and grown an AlSb layer at a low temperature, as shown in Fig 4- 3.

The gate modulation is appeared in the FET device with LT layer is applied. Fig 4- 3 shows the I_d-V_d curve of a device with 50um in the width and 2um in the gate length. According to the I-V curve, the drain current is 40mA/mm at V_d=0.5V and V_g=-0.4V, but a large part of which is the buffer leakage. Although the buffer leakage dominates in the negative gate bias and device can't pinch-off, this is the preliminary result for us to fabricate the InAs HEMT.

Rn735

Active layer	
$Al_{0.7}Ga_{0.3}Sb$	300nm
AlSb (530°C)	1.6um
AlSb (470°C)	100nm
GaAs substrate	

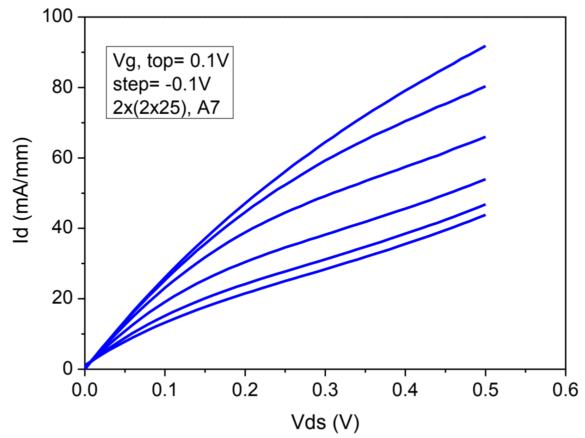


Fig 4- 3 Schematic of the LT buffer grown on GaAs substrate and the device operation

Nevertheless, as mentioned in Chapter 2, the LT layer is very rough. The roughness of the sample surface measured by Atomic Force Microscope (AFM) is shown in Fig 4- 4. Compared with the thickness of active region (15nm), the roughness (12nm) is too large, which would severely degrade the electron mobility of channel.

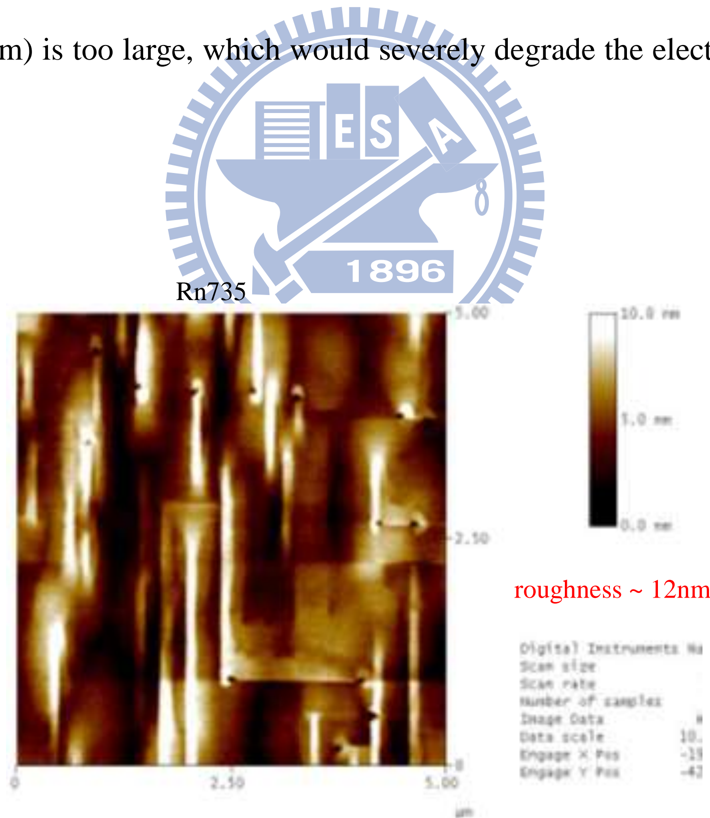


Fig 4- 4 AFM topography of the surface of the sample with using LT buffer layer

4.1.3 IMF array buffer layer

In order to reduce the surface roughness of the sample, we use the IMF quantum dot instead of the LT buffer. As shown in Fig 4- 5, the surface roughness is 7nm, which is smaller than LT buffer (12nm), so the surface is smoother with IMF method.

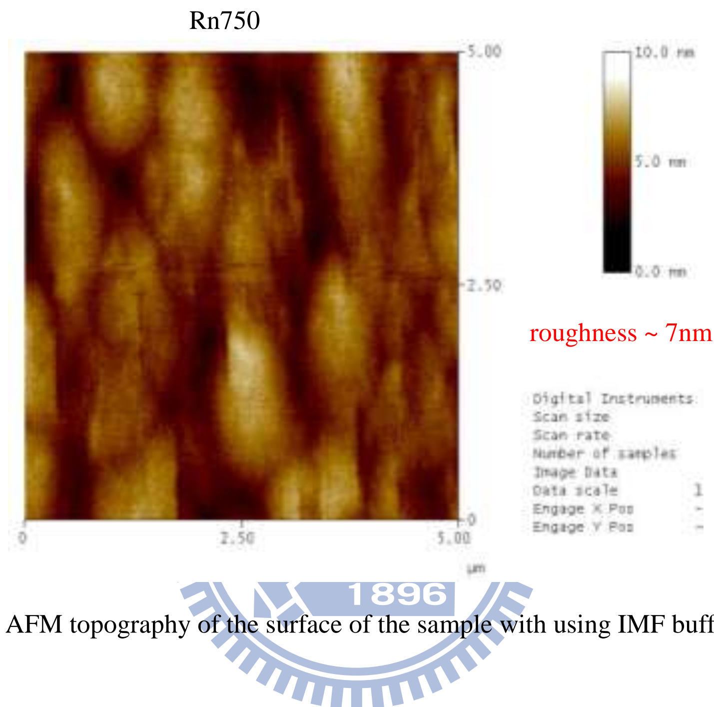


Fig 4- 5 AFM topography of the surface of the sample with using IMF buffer layer

The IMF buffer structure and I_d-V_d curve of a FET with device width 50um and gate-length 2um is shown in Fig 4- 6. The resistance of each buffer layer is higher than that grown by LT method.

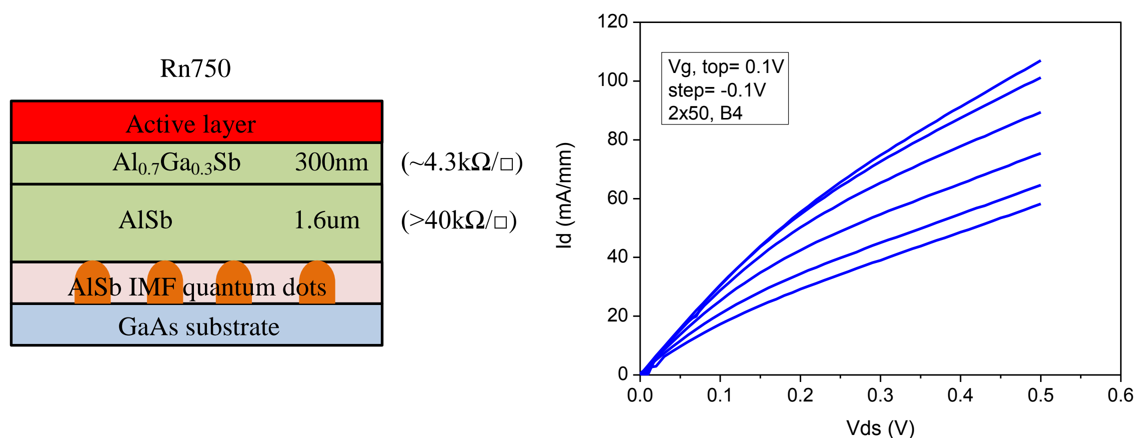


Fig 4- 6 Schematic of the IMF buffer grown on GaAs substrate and the device operation

But as Fig 4- 6 shows, a single AlSb IMF quantum dot layer can't relieve strains completely and the thread dislocation still causes the buffer leakage obviously. The I-V curve exhibits the influence of buffer leakage in a depletion mode FET. Due to the serious buffer leakage, the FET can't pinch-off with negative gate bias.

We approach our goals nearly by adding the second quantum layer (Fig 4- 7). Adding an InSb quantum dot layer 300nm above the AlSb IMF quantum dot layer helps to suppress the threading of the dislocations more effectively than previous approaches.

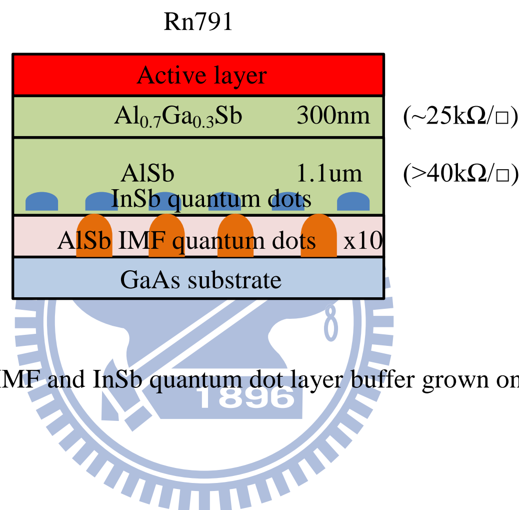


Fig 4- 7 Schematic of the IMF and InSb quantum dot layer buffer grown on GaAs substrate

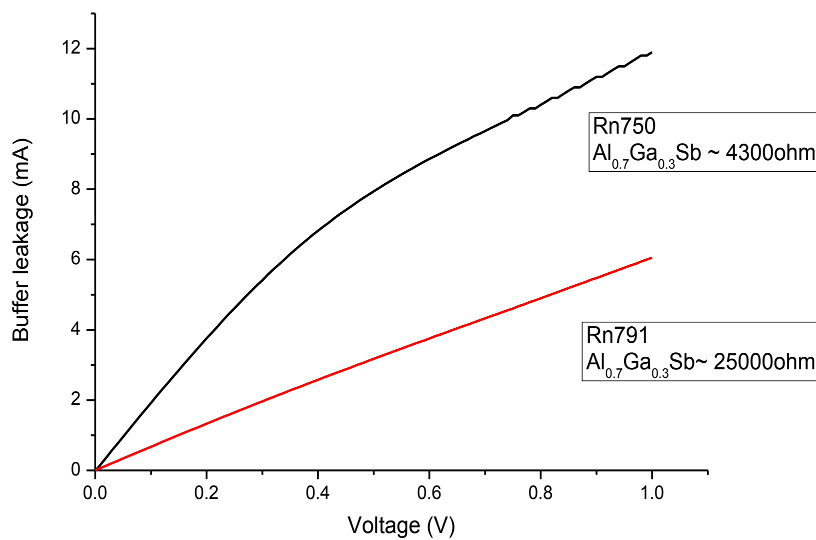


Fig 4- 8 The comparison of the buffer leakage with and without InSb quantum dot layer

The resistance of the $Al_{0.7}Ga_{0.3}Sb$ layer is larger than that grown with only a single IMF quantum dot. As Fig 4- 7 shows, the sheet resistance of the $Al_{0.7}Ga_{0.3}Sb$ layer increases to 25000Ω/□. But the buffer leakage isn't comparable to this value. The buffer leakage is reduced by half from 12mA to 6mA under bias voltage 1V.

So far we have been used wet etching for the fabric action of the mesa isolation. Due to the serious lateral etching, as mentioned in Chapter 3, we have to stop etching at the $Al_{0.7}Ga_{0.3}Sb$ layer in order to keep off the patter out of shape, as Fig 4- 9 shows. The resistance of the $Al_{0.7}Ga_{0.3}Sb$ layer is too low to provide an good device isolation and therefore the buffer leakage could flow through buffer layer easily.

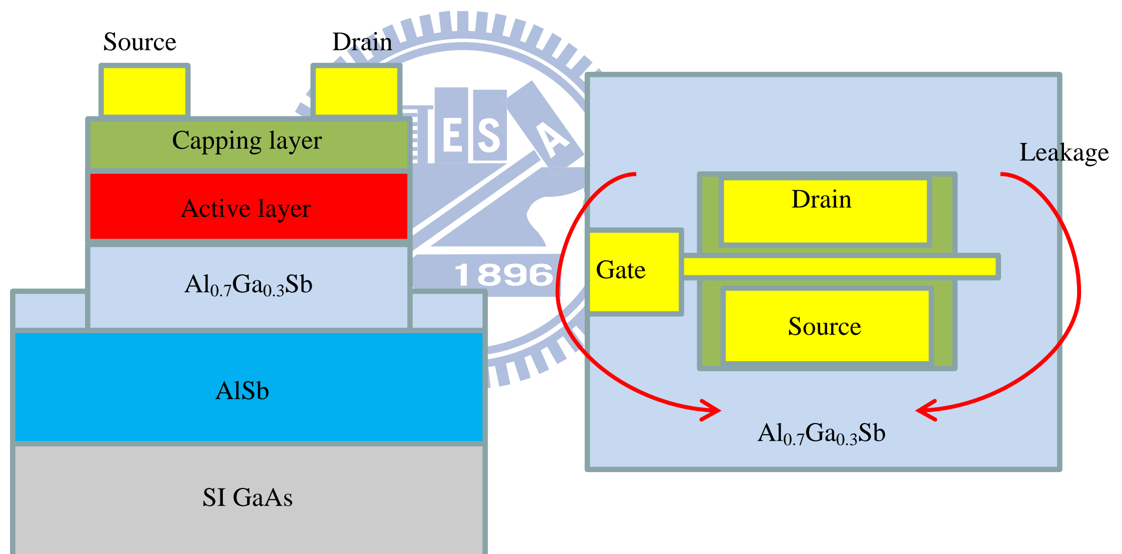


Fig 4- 9 Schematic of the poor mesa isolation due to the leakage path in $Al_{0.7}Ga_{0.3}Sb$ layer

4.1.4 ICP dry etching

The poor isolation couldn't be improved by epitaxy temporarily, so we try to block the leakage path by dry etching through the $Al_{0.7}Ga_{0.3}Sb$ layer (Fig 4- 10). The bottom AlSb layer with larger resistance (>40k Ω/□) is more suitable as the isolation

layer. But the instability of this material which presented in Chapter 3, oxidize with extreme fast rate in air. As a result, the SiN passivation is more important in this fabrication step.

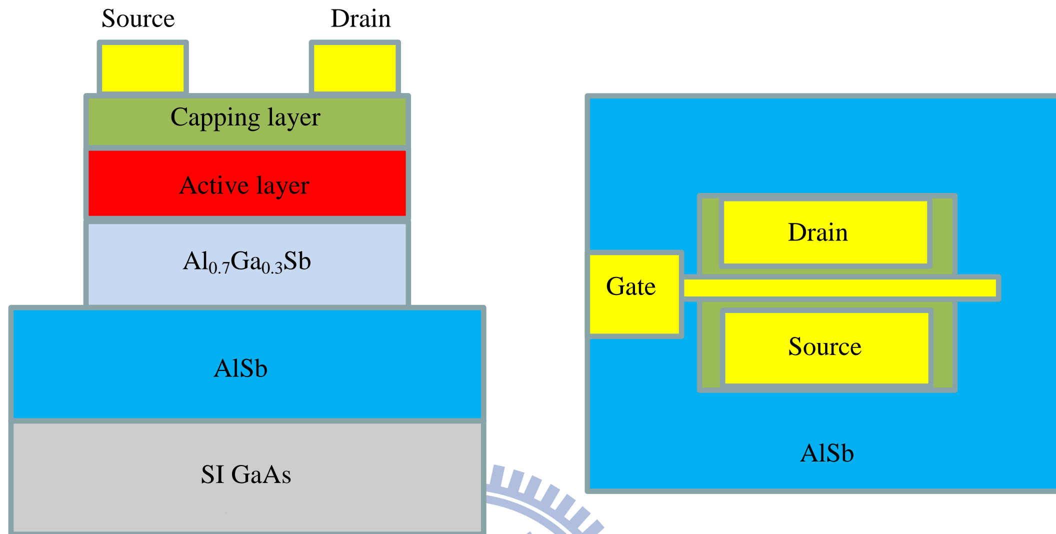


Fig 4- 10 Schematic of the mesa isolation with etching through the $Al_{0.7}Ga_{0.3}Sb$ layer

Fig 4- 11 compares the I-V curve of device FET with wet etching and dry etching respectively. The buffer leakage reduces remarkably with the dry etching fabrication from 30mA/mm to below 10mA/mm under V_{gs}=-0.5V, V_{ds}=0.5V.

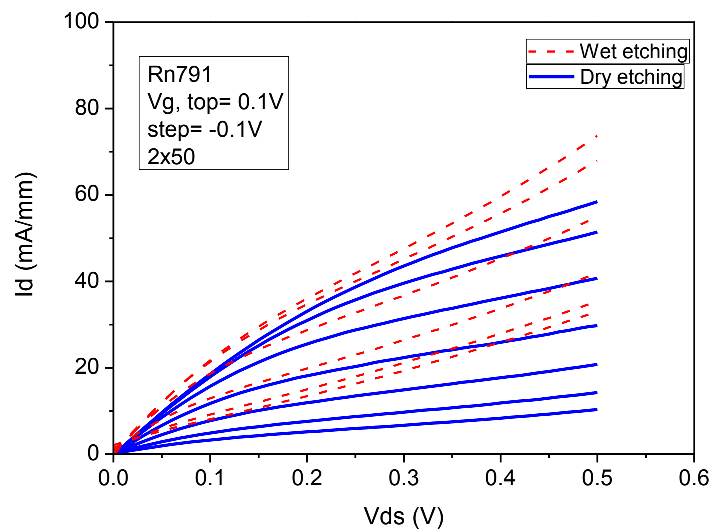


Fig 4- 11 The characteristics of the device in different mesa isolation

The accuracies of TLM and Hall measurement have also been improved with the change of mesa isolation correspondingly. Fig 4- 12 indicates that the resistance doesn't increase linearly with the extension of the spacing in the case of poor isolation. The buffer could be considered as a resistance parallel to the channel and cause the drop of sheet resistance. This influence of buffer leakage could be improved by dry etching.

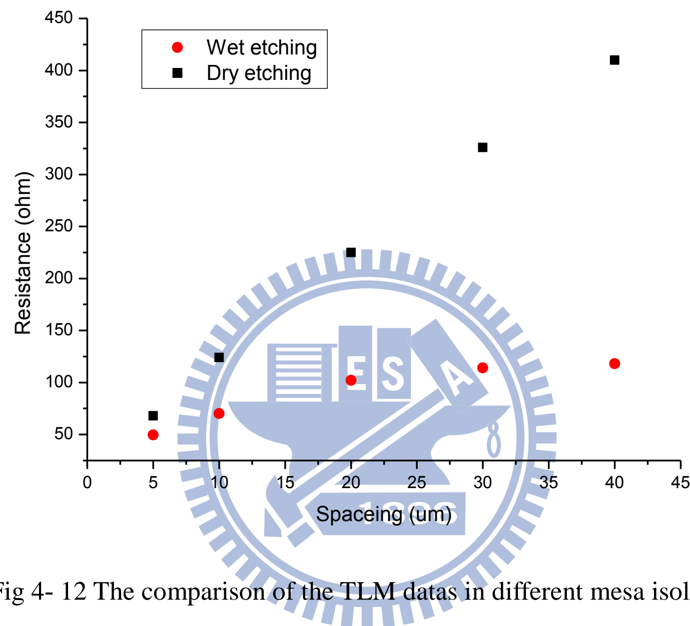


Fig 4- 12 The comparison of the TLM datas in different mesa isolation

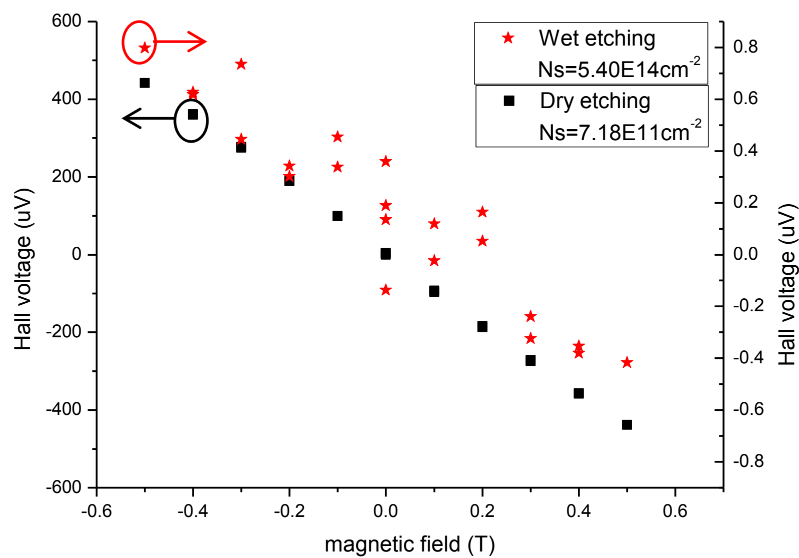


Fig 4- 13 The comparison of the Hall measurements in different mesa isolation

In addition, the buffer layer would provide a great deal of carriers undesired and also appear in the result of Hall measurement. Fig 4- 13 presents the Hall voltage with different mesa isolation. The carrier concentration decreases substantially from $5.40x10^{14}cm^{-2}$ to $7.18x10^{11}cm^{-2}$ after etching through the $Al_{0.7}Ga_{0.3}Sb$ layer by dry etching.

We are very inspired by this improvement. Compared with the energy band gap of InAs (0.36eV), the device with 2um gate length could operate normally with drain voltage up to 1.0V, as shown in Fig 4- 14. The contact resistance of this device is 0.6Ω-mm.

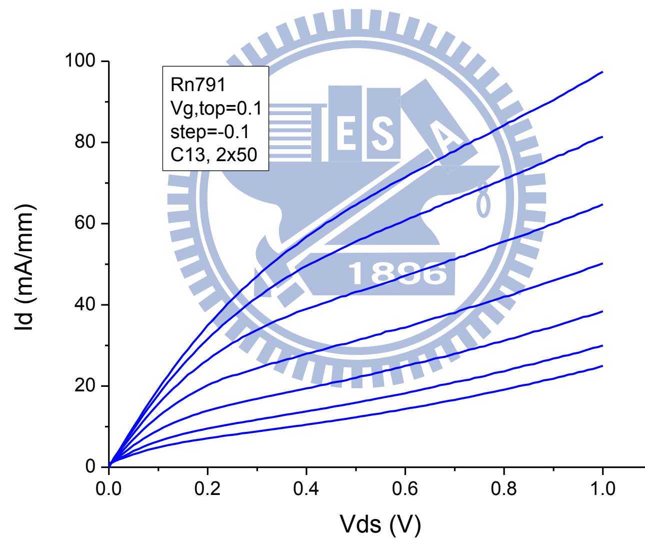


Fig 4- 14 The Id-Vd characteristic of the device operates with 2um gate length

But the maximum transconductance (Gm) of this device is 150mS/mm with 2um gate length, shown in Fig 4- 15. From the Hall measurement, the carrier density in channel is $7.19x10^{11}cm^{-2}$, which is below the typical density $1x10^{12}cm^{-2}$. As a result, the drain current is very small and transconductance is not high. This also reflects to the RF operation, as shown in Fig 4- 16. The *ft* is 1.2GHz and *fmax* is 0.2GHz with 2um gate length.

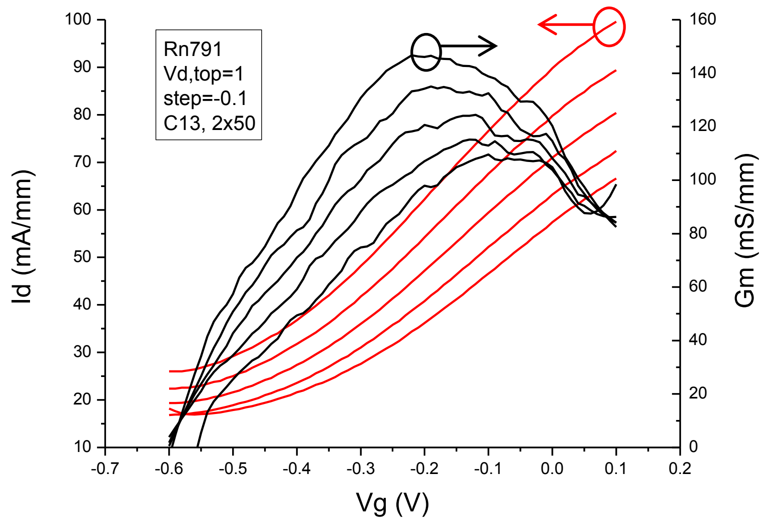


Fig 4- 15 Measured dc transconductance with 2um gate-length of Rn791

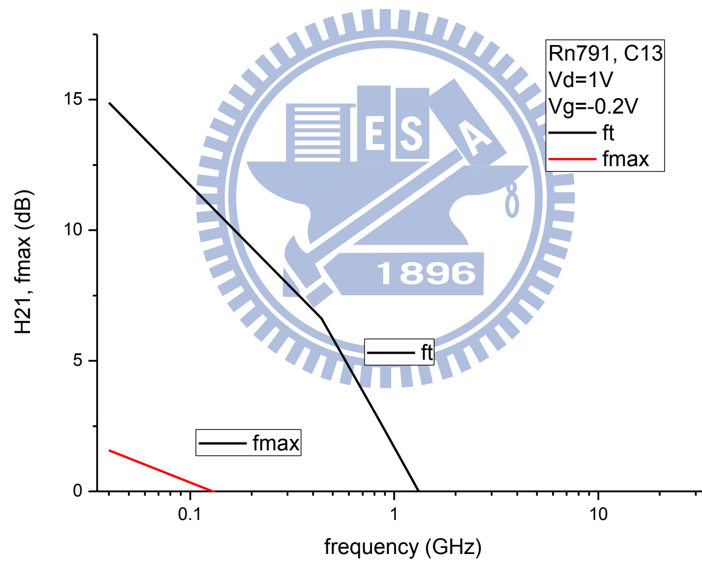


Fig 4- 16 The ft and fmax with 2um gate-length of Rn791

4.1.5 The combination with IMF and LT buffer

Due to the high sensitivity and variation in growing the quantum dot, we decide to add an AlSb LT buffer layer, which is insensitive to the chamber condition, as illustrated in Fig 4- 17.

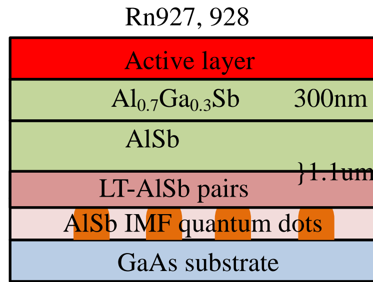


Fig 4- 17 Schematic of the buffer layer combines the IMF array and LT method

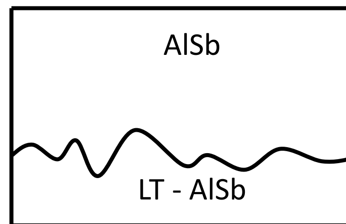


Fig 4- 18 The LT-AlSb pair

From the previous experiment, the roughness is the most drawback of LT buffer. Trying to solve this problem, we adjust the thickness of LT layer and cap a layer with normal temperature on it for smoothing, as shown in Fig 4- 18.

	Rs (Ω/□)	Ns (cm^{-2})	Mobility ($cm^2V^{-1}s^{-1}$)
Rn927	346	7.95×10^{11}	22700
Rn928	375	8.86×10^{11}	19200

Table 4- 1 The results of Hall measurement in the samples Rn927 and Rn928

After a series of work, we obtain high mobility in sample Rn927 and Rn928, as shown in Table 4- 1, which is about $20000cm^2V^{-1}s^{-1}$.

4.2 Channel design

The improvement of mobility and sheet resistances in Table 4- 2 indicates that we have approached the epitaxy of LT buffer layer. The other evidence is the buffer leakage. Fig 4- 19 shows the buffer leakage of Rn927 is less than 10nA, which is very small. So the next step is the channel design.

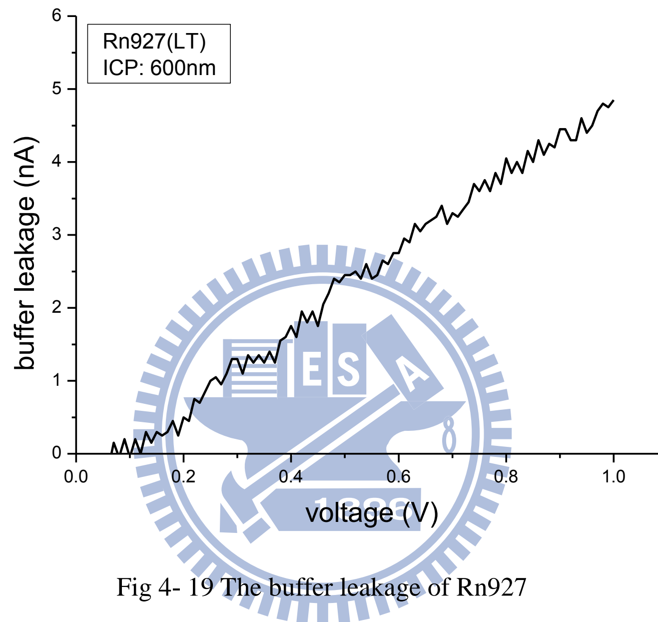


Fig 4- 19 The buffer leakage of Rn927

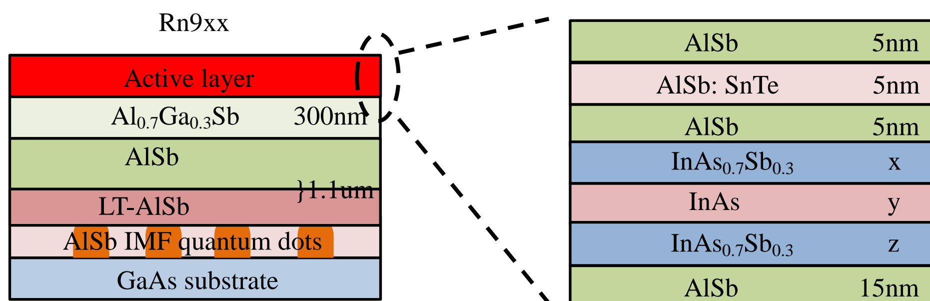


Fig 4- 20 Schematic of the structure with different active layer

Fig 4- 20 is the schematics of the device structure with different active layer. The detailed channel design and SnTe doping condition is shown in Table 4- 2. With the

thickest InAs layer in Rn927, its mobility is the highest and agrees with our expectation. Compared with Rn927, the other two samples Rn936 and Rn938 have small proportion of InAs. So their mobility is a little lower than Rn927 but still close to 15000$cm^2V^{-1}s^{-1}$.

	x/y/z thickness (nm)	**SnTe doping**	**Rs (Ω/□)**	**Ns (cm^{-2})**	**Mobility (cm^{2}V^{-1}s^{-1})**
Rn927	3/9/3	300℃	346	7.95 x 10^{11}	22700
Rn936	3/6/6	325℃	450	8.68 x 10^{11}	15000
Rn938	3/6/6	350℃	550	8.96 x 10^{11}	12700

Table 4- 2 The results of Hall measurement in the samples with different active layer

The device I-V curves of Rn927 with 2um gate length are shown in Fig 4- 22 and Fig 4- 22. According to Fig 4- 21, the device leakage is near 80mA/mm at Vd=1V, Vg=-1.2V. But Fig 4- 22 indicates that the gate leakage is only 6mA/mm at this condition. As a result, the device leakage doesn't come from the gate.

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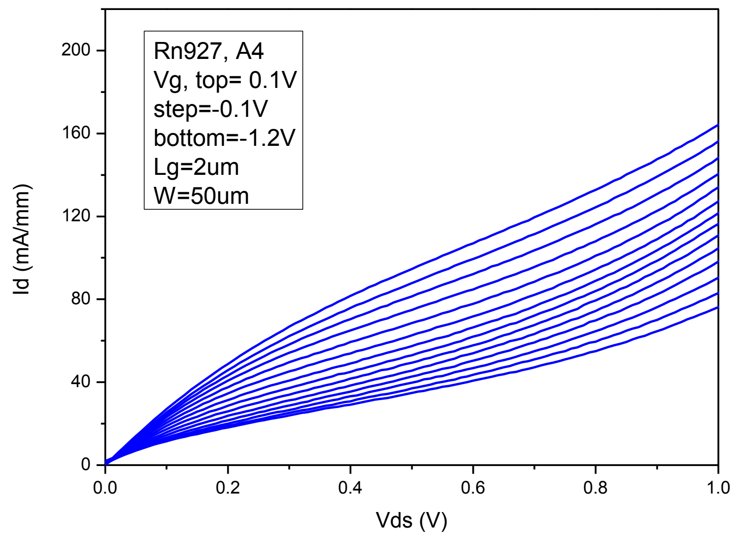

Fig 4- 21 The drain characteristics of Rn927

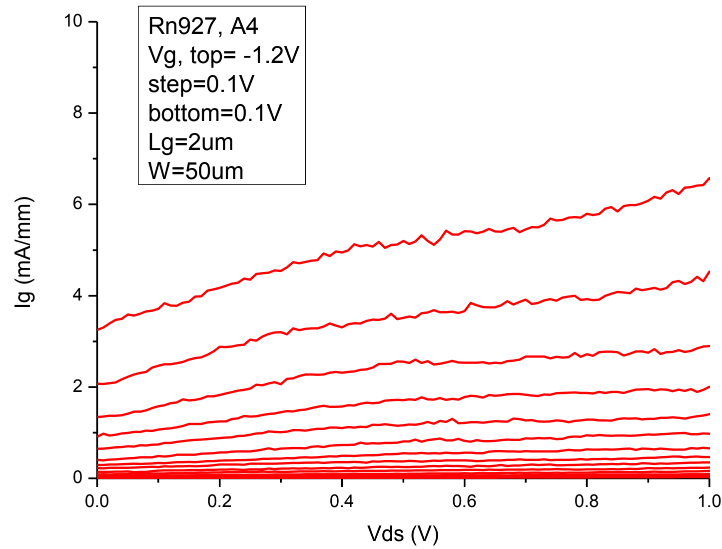

Fig 4- 22 The gate leakage of Rn927

The device I-V curves of Rn936 with 2um gate length are shown in Fig 4- 24 and Fig 4- 24. The device leakage is near 60mA/mm at Vd=1V, Vg=-0.7V. Compared with the gate leakage showing in Fig 4- 24 which is less than 5mA/mm, the device leakage is still serious.

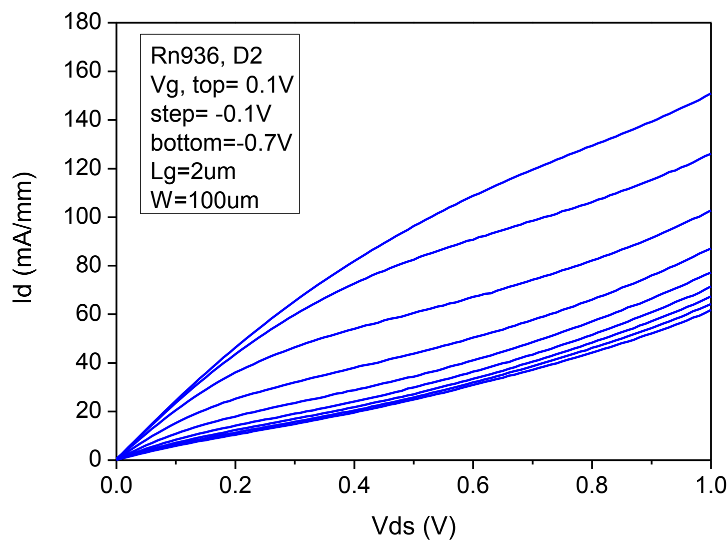

Fig 4- 23 The drain characteristics of Rn936

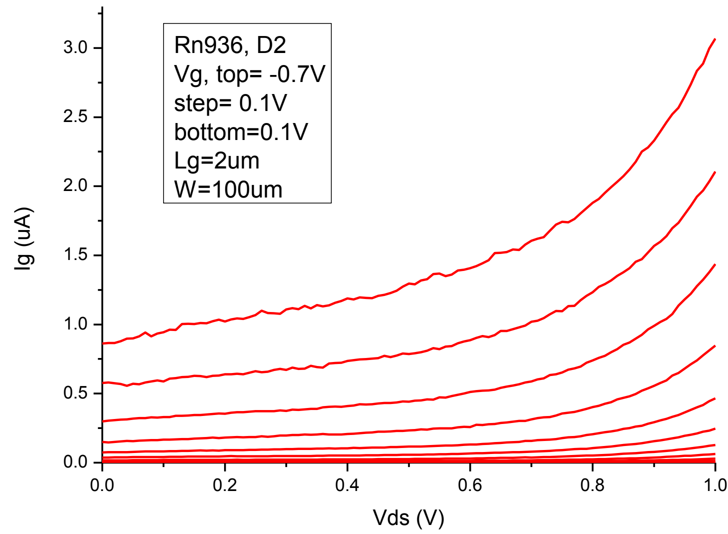

Fig 4- 24 The gate leakage of Rn936

The same situation occurs in Rn938. The device I-V curves of Rn936 with 2um gate length are shown in Fig 4- 26 and Fig 4- 26. The device leakage is near 60mA/mm at Vd=1V, Vg=-1.1V. The gate leakage showing in Fig 4- 26 is less than 15mA/mm, so the device leakage doesn't come from gate, either.

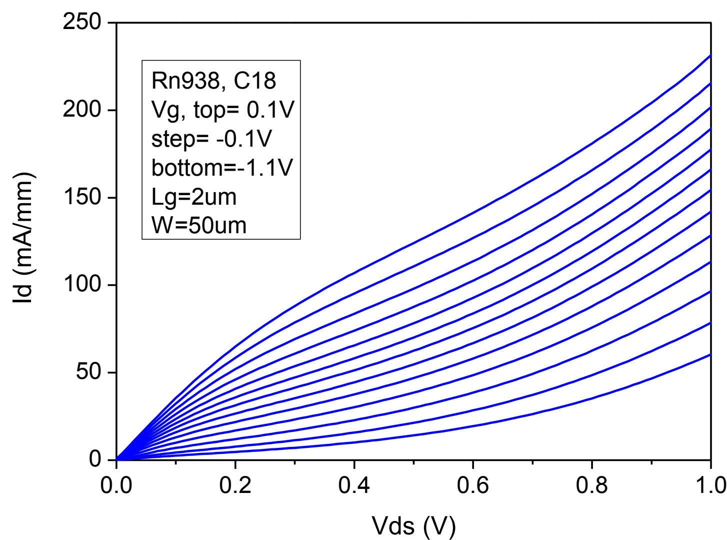

Fig 4- 25 The drain characteristics of Rn938

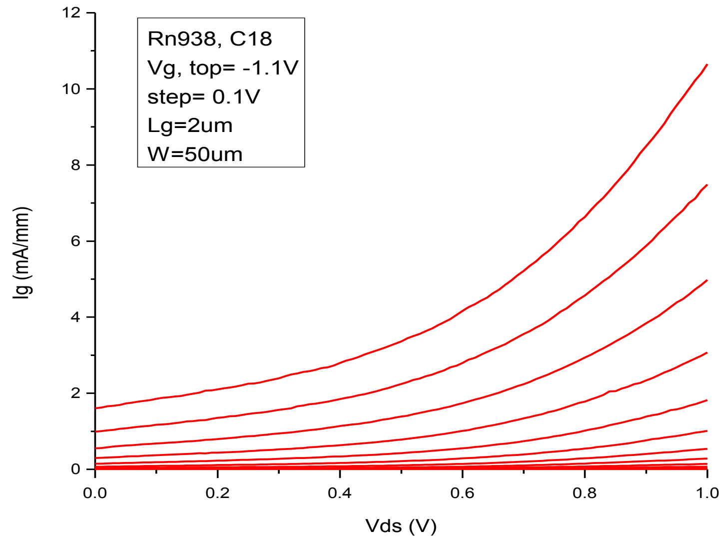

Fig 4- 26 The gate leakage of Rn938

We attributed the difference from the $Al_{0.7}Ga_{0.3}Sb$ buffer layer. This layer is used as a passivation layer for AlSb. If the resistance of this layer is lower than AlSb buffer, it may be a leakage path, as shown in Fig 4- 27.

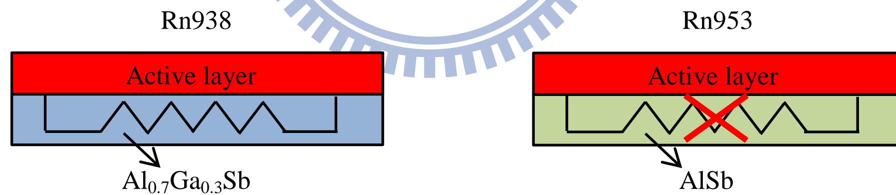

Fig 4- 27 Schematic of the parallel resistance existing in buffer

As a result, more negative gate bias is needed to pinch off the drain current. This means the threshold voltage is changed by the $Al_{0.7}Ga_{0.3}Sb$ layer. However, the threshold voltage (Vt) would become so negative that the Schottky gate couldn't afford it. As Fig 4- 26 shows, the maximum gate leakage is near 12mA/mm at Vd= 1V and Vg= -1.1V and would increase dramatically.

To improve the operation of devices, we try to remove the $Al_{0.7}Ga_{0.3}Sb$ layer. The SnTe doping temperature is 400℃ and the whole epitaxy structure is shown in Fig 4-28.

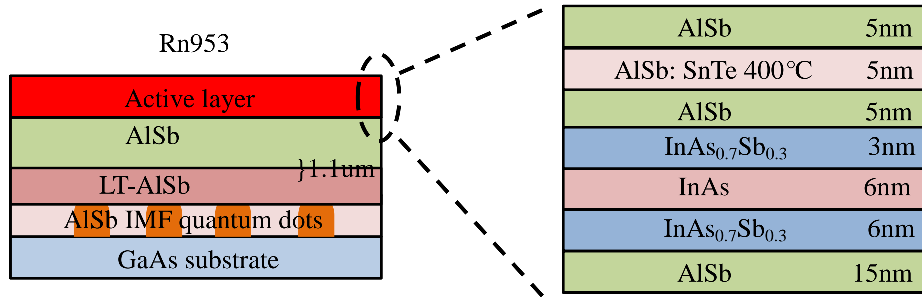

Fig 4- 28 Schematic of the structure without the $Al_{0.7}Ga_{0.3}Sb$ layer

We compare the Hall data after the $Al_{0.7}Ga_{0.3}Sb$ buffer was removed, as shown in Table 4- 3. The sheet resistance increases with the removal of the $Al_{0.7}Ga_{0.3}Sb$ layer from 550Ω/□ to 980Ω/□, indicates that this layer may help to improve the roughness in channel. The degradation of sheet resistance would also affect the mobility in channel. The mobility drops from 12700cm^{2}v^{-1}s^{-1} in Rn938 to 7640 cm^{2}v^{-1}s^{-1} in Rn953.

	$Al_{0.7}Ga_{0.3}Sb$ layer	SnTe doping	Rs (Ω/□)	Ns (cm^{-2})	Mobility (cm^{2}V^{-1}s^{-1})
Rn938	w	350℃	550	8.96×10^{11}	12700
Rn953	w/o	400℃	980	8.34×10^{11}	7640

Table 4- 3 The comparison of the basic parameters with and without the $Al_{0.7}Ga_{0.3}Sb$ layer

The results of the HEMT with 2um of gate length are presented as followings. Fig 4- 29 shows the drain current Id from Vd=0V to 1.2V in Rn953. The contact resistance of this device is 0.5Ω-mm. The gate leakage is shown in Fig 4- 30 correspondingly. According to these two figures, the devices could be nearly pinch-off

with threshold voltage = -0.9V and meanwhile, the gate leakage is about 6mA/mm, accounting for a large proportion of the drain current at this region. This is the first time for us to achieve pinch off in devices operation.

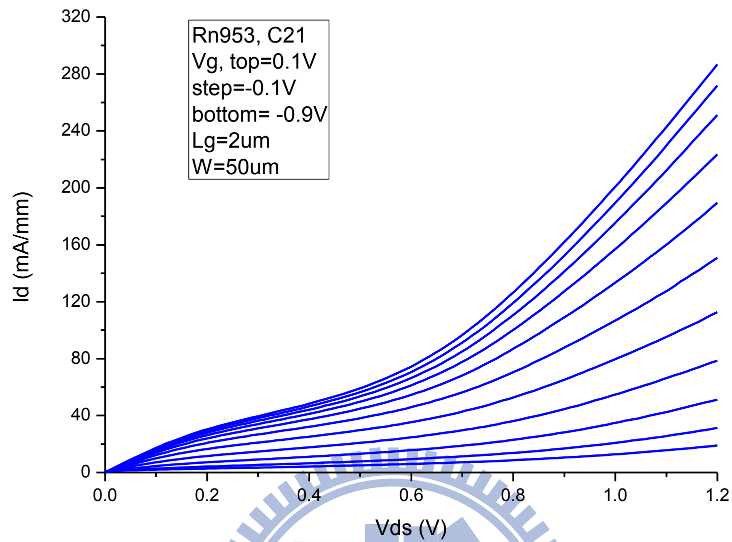

Fig 4- 29 The drain characteristics of Rn953 with 2um of gate length

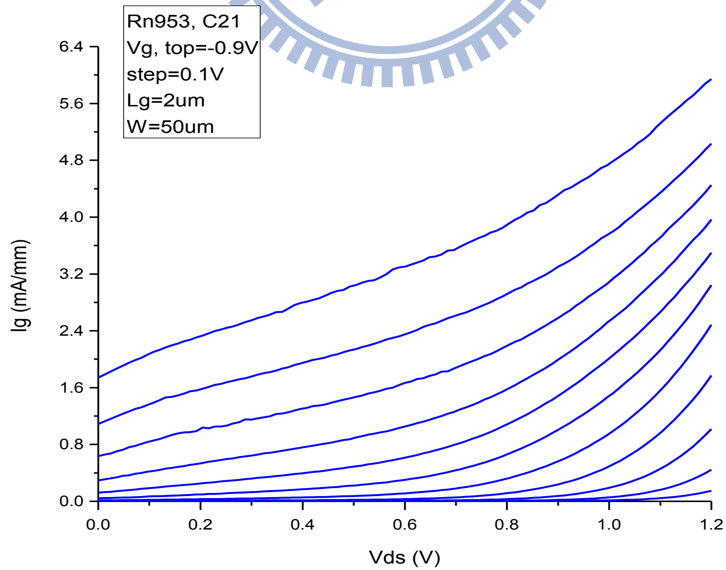

Fig 4- 30 The Schottky gate leakage of Rn953

Fig 4- 31 shows the enhancement in drain current and transconductance with the increase of drain voltage. The threshold voltage of this device is about -0.8V. The peak value of transconductance (Gm) is 730mS/mm, occurring at a very high drain voltage 1.6V, and the gate voltage -0.55V. The Schottky gate would suffer too large electric field and breakdown with the voltage above it.

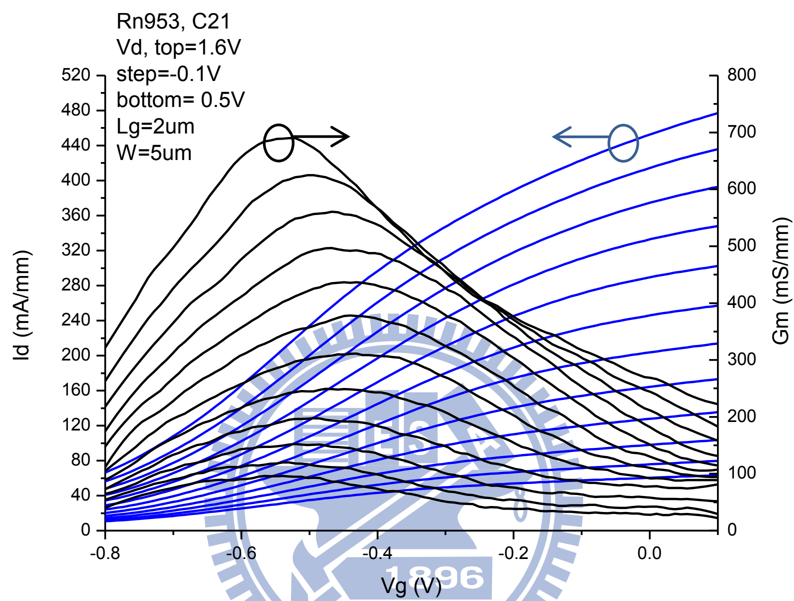

Fig 4- 31 Measured DC transconductance of Rn953

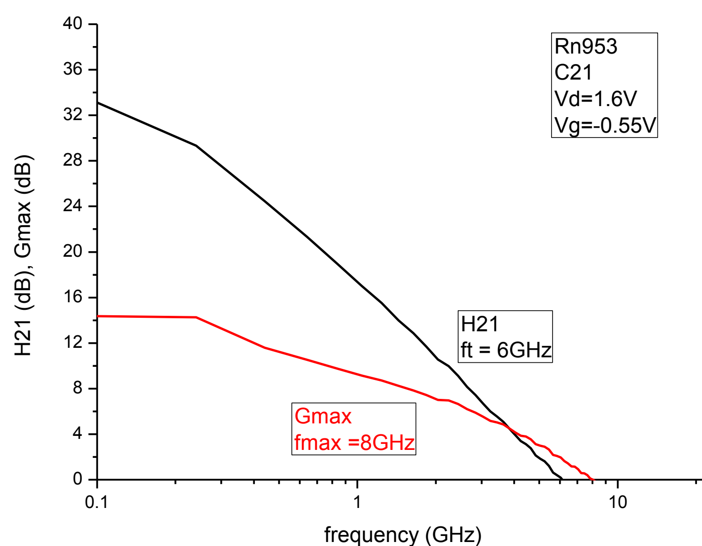

Fig 4- 32 Measured RF characteristic of Rn953

The values of *ft* and *fmax* of a device with 2um gate-length is shown in Fig 4- 32, which are 6GHz and 8GHz.

4.2.1 Kink effect

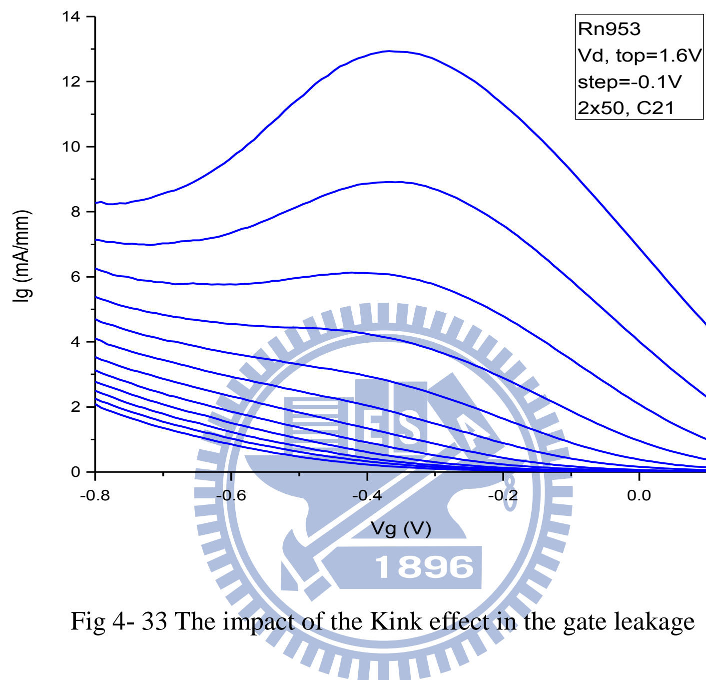

Fig 4- 33 The impact of the Kink effect in the gate leakage

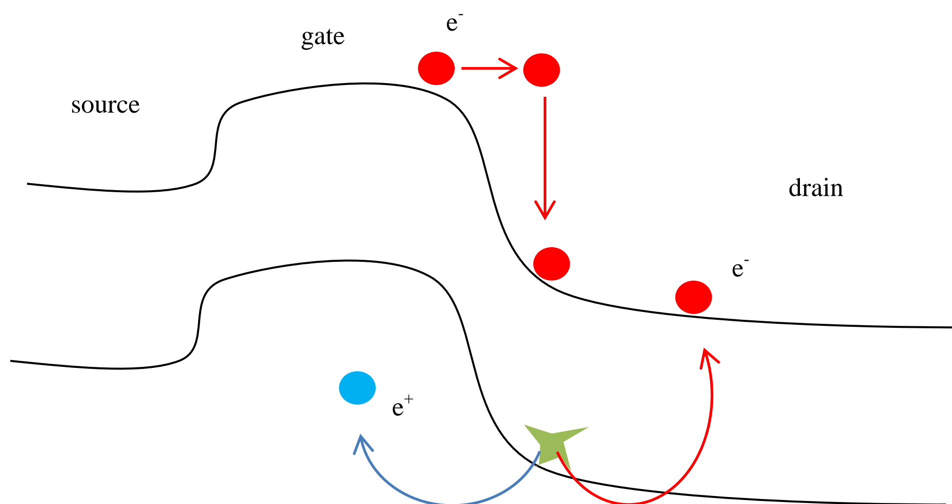

Fig 4- 34 Schematic of the impact ionization

There is a sign of impact ionization in the gate current, as shown in Fig 4- 33. A wave-shaped gate leakage current occurs with the increase of drain bias. The excess gate leakage at high drain bias attributes to the impact ionization, which also enhance the transconductance and is referred to as the "kink effect".

The mechanism of the impact ionization could be illustrated in Fig 4- 34. Moving in the channel, electrons would gain energy as they enter the high electric field region between gate and drain. When the energy exceeds the band gap of the InAs channel (0.36eV), electrons would undergo impact ionization and generate electron-hole pairs.

The impact-ionized electrons would flow to the drain and holes, on the contrary, should drift back toward the source. Nevertheless, due to the week confinement in valance band barrier as shown in Fig 4- 35, a great deal of impact-ionized holes would drift everywhere and thus cause the gate leakage and kink effect.

Fig 4- 35 illustrates that with negative gate bias, a part of holes would be swept into the gate and become the additional gate leakage, as seen in Fig 4- 33. The wave-shaped gate leakage becomes serious with the increase of drain bias, indicating that the more holes were generated due to the higher electric field.

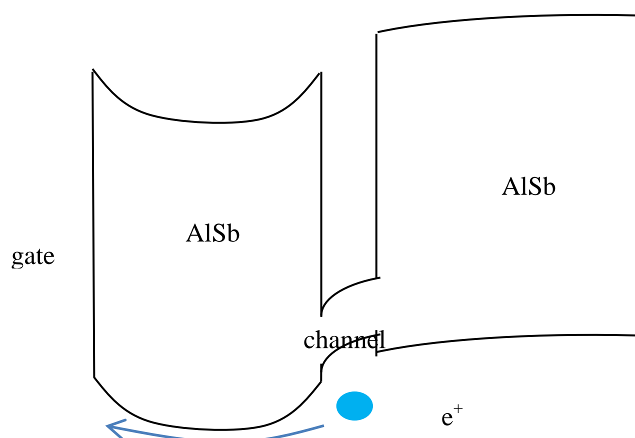

Fig 4- 35 Holes would flow to gate due to the week confinement

Besides causing the gate leakage, the impact-ionized holes could also lead to the significant increase of the drain current, as shown in Fig 4- 36. The drain current raises significantly when the drain bias exceeding 0.6V, which is called the kink effect.

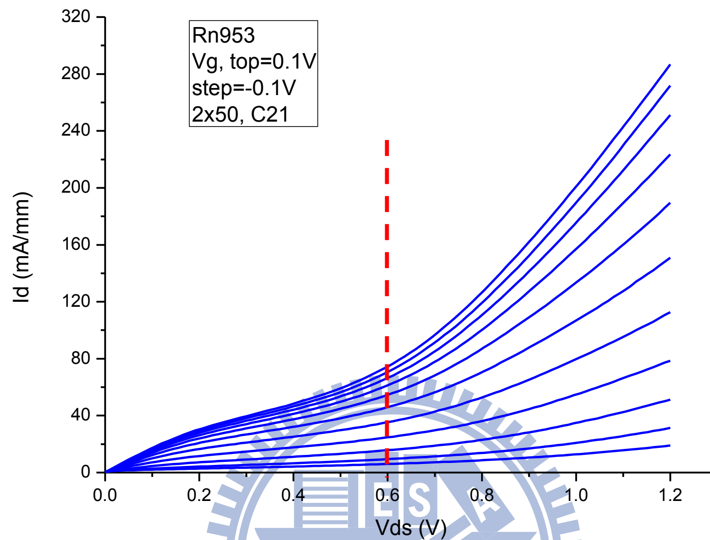

Fig 4- 36 The impact of the Kink effect in drain current is obvious at Vd > 0.6V

The impact-ionized holes could not only be attracted toward gate but also would accumulate in the substrate [10], as illustrated in Fig 4- 37. The accumulating positive charge would lower the energy band in the bottom AlSb barrier and in the channel. As a result, electrons in the channel would increase and enhance the current.

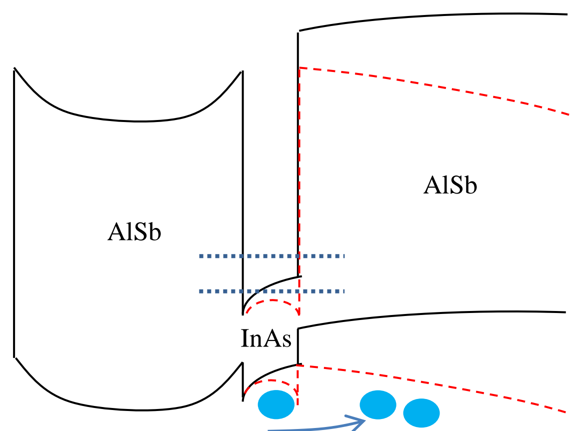

Fig 4- 37 Schematic of the Kink effect causing from the increase of 2DEG in the channel

There is another possible mechanism to cause the kink effect. After the impact ionization, holes may collect at source-gate barrier, as shown in Fig 4- 38. The additional positive charges would drag the energy band of gate region and lower the effective potential barrier for electrons in source. Therefore, more electrons could pass through the barrier and enter the high electric field region between gate and drain, causing more drain current, which further enhance the impact ionization. This is a positive feedback in the drain current but from another point of view, this also means the degradation of gate control.

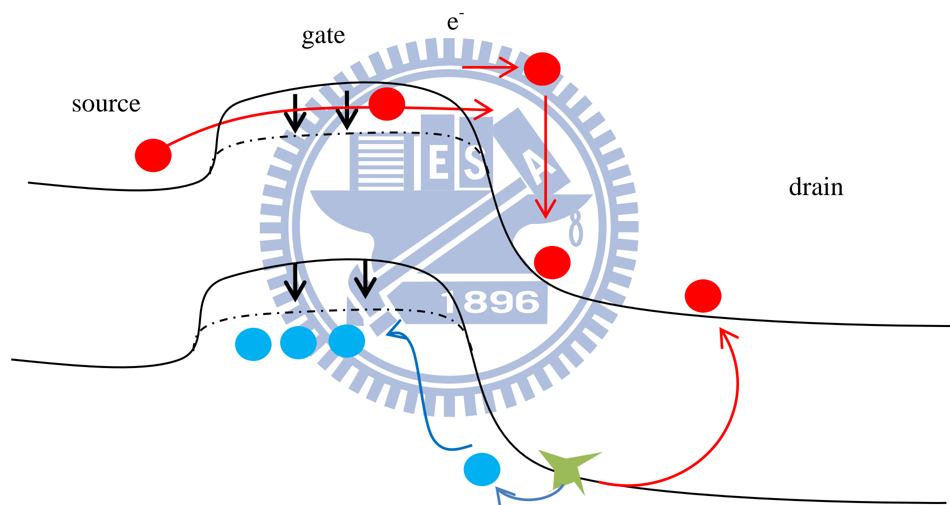

Fig 4- 38 Schematic of the Kink effect causing from the lower of the source-gate barrier

Fig 4- 39 presents the I-V curve of the e-beam device a gate length 125nm. The kink effect is more obvious than the device with a gate length 2um at about Vd=0.6V and the drain current increase significantly. But the occurrence of kink effect at Vd=0.6V is higher than the typical type-II device which is at about Vd=0.4V [11]. This means the channel structure we designed is helpful to enlarge the soft breakdown voltage of type-II device.

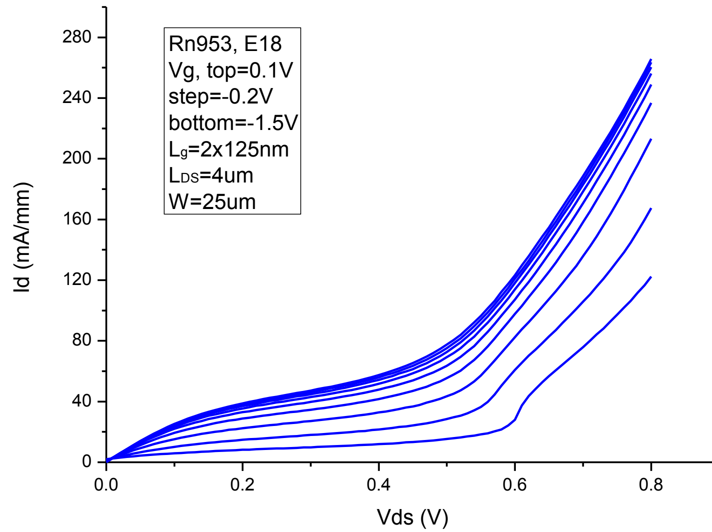

Fig 4- 39 The drain characteristics of Rn953 with 125nm of gate length

4.2.2 Modulation doping design

The kink effect is attributed to the impact ionization. The solution to reduce the influence of kink effect is to avoid the generation of impact ionization. Therefore, the channel design becomes more important to enlarge the effective energy band gap in channel.

In addition, the doping structure of the active layer is also very important. The doping structure could determine the magnitude of electron density in channel and the threshold voltage of device. The drain current we obtained in sample Rn953 is small as the bias lower than 0.6V, as shown in Fig 4- 36 and Fig 4- 39. Similar results were also obtained for our precious sample Rn791. For the device of Rn791, the electron density ($7.19 \times 10^{11} cm^{-2}$) for the doping condition of the SnTe doping temperature 300°C is also not enough. Without the kink effect, the I_{on}/I_{off} ratio and the transconductance is low at lower drain voltages.

In order to increase the drain current of the device, the carrier concentration in the channel should be raised. We try to solve this problem by raising the doping temperature from 300°C to 400°C. But the Hall measurement indicates that the carrier concentration doesn't change significantly, as shown in Fig 4- 40.

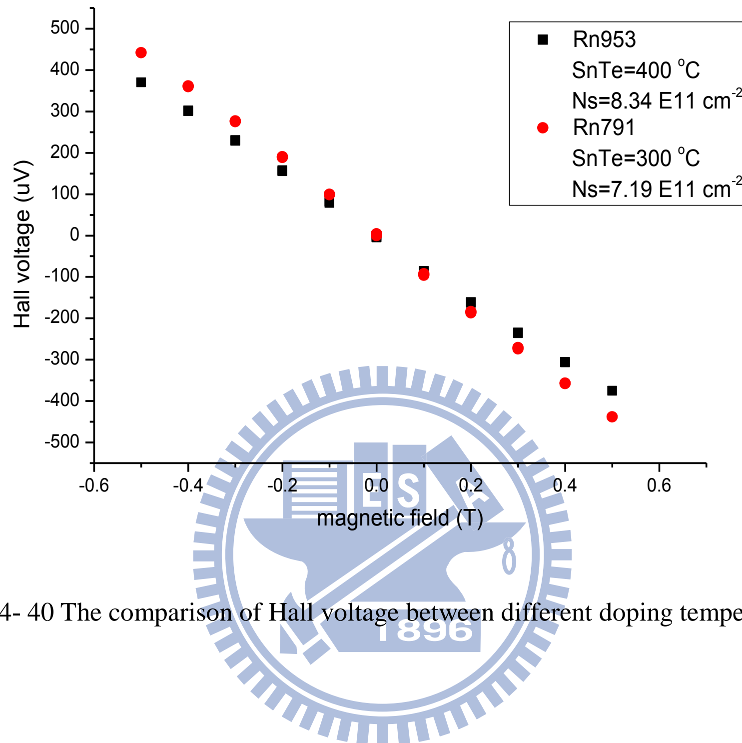

Fig 4- 40 The comparison of Hall voltage between different doping temperature

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We could see that raising the SnTe temperature is not effective to increase the carrier concentration. Another method is to reduce the thickness of the AlSb spacer layer between the uniform doping layer and the channel, as illustrated in Fig 4- 41. However, this may increase the scattering between the ionized dopants and the electrons in the channel and degrade the electron mobility.

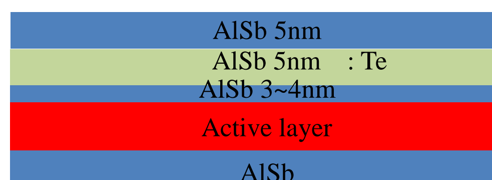


Fig 4- 41 Schematic of the modulation doping structure with the scale down of the bottom layer

The result of the Hall measurement is shown in Table 4- 4. The electron density in channel in sample Rn969 is $1.31x10^{11}cm^{-2}$, which is higher than that in Rn968 ($5.42x10^{11}cm^{-2}$). The large increment of the carrier concentration indicates that the reduction of the AlSb spacer thickness is effective to raise the carrier density in channel. But the electron mobility indeed degraded with the reduction of the thickness of the AlSb spacer. According to Table 4- 4, the electron mobility in Rn969 is $9000cm^2V^{-1}s^{-1}$, which is much lower than that in Rn968 ($18900cm^2V^{-1}s^{-1}$). Thus, the reduction of AlSb spacer thickness is a trade-off between the carrier concentration and electron mobility.

	SnTe doping	**AlSb thickness (nm)**	**Ns (cm^{-2})**	**Mobility ($cm^2V^{-1}s^{-1}$)**
Rn968	350°C	4	5.42×10^{11}	18900
Rn969	350°C	3	1.31×10^{12}	9000

Table 4- 4 The comparison of the carrier concentration and mobility between different spacing

The SnTe doping temperature is 350°C and the whole epitaxy structure in Rn968 is shown in Fig 4- 42. The buffer layer is the same as which in Rn953. The SnTe temperature is 350°C and AlSb spacer is 4nm.

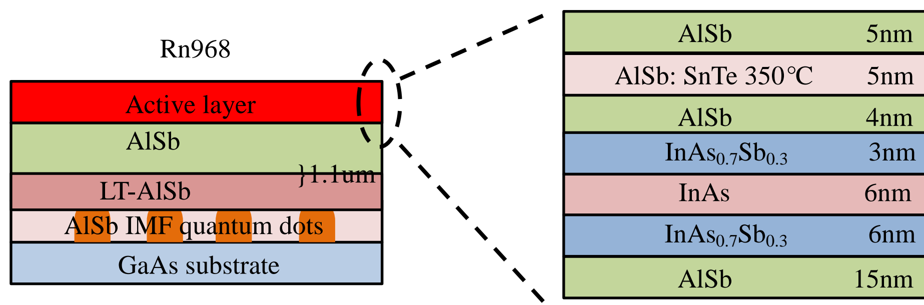


Fig 4- 42 Schematic of the structure with the AlSb spacer is 4nm

The results of the HEMT with 50nm of gate length in Rn968 are presented as followings. Fig 4- 43 shows the drain current Id from Vd=0V to 0.5V in Rn968. The contact resistance of this device is 0.5Ω-mm. The gate leakage is shown in Fig 4- 44 correspondingly. Due to the non-optimized process in E-beam lithography, the devices couldn't pinch-off. The device leakage is nearly 60mA/mm at Vd=0.5V and Vg=-1V. The gate leakage is about 20mA/mm, which is serious and account for a proportion of the drain current at this region.

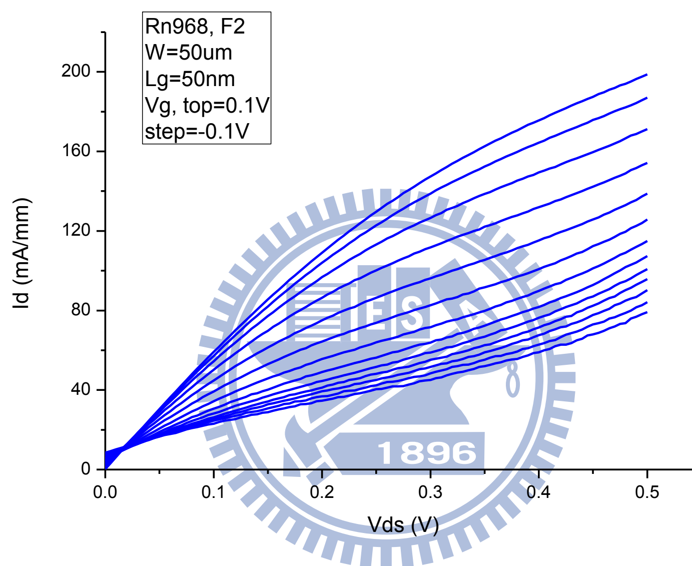


Fig 4- 43 The drain characteristics in Rn968 with 50nm of gate length

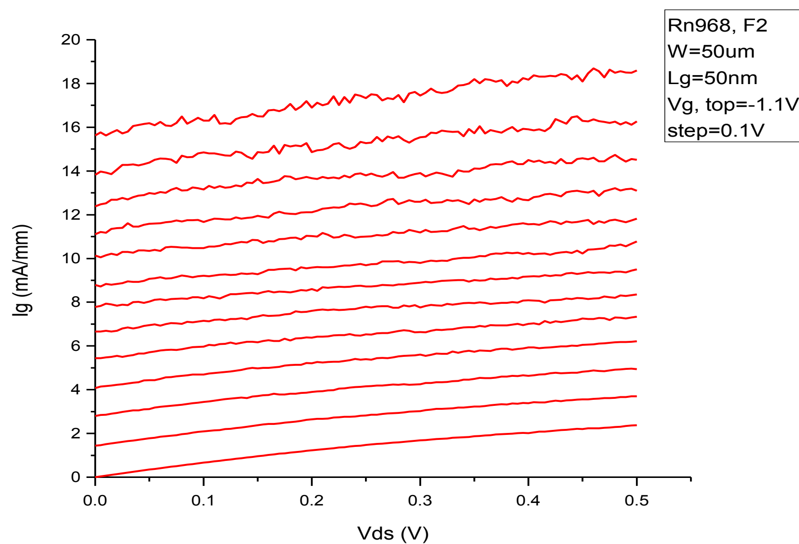


Fig 4- 44 The gate leakage in Rn968 with 50nm of gate length

Fig 4- 45 shows the enhancement in drain current and transconductance with the increase of drain voltage from Vd=0.1V to 0.5V. The threshold voltage of this device is larger than -1V, which results from the non-optimized process. The peak value of transconductance (Gm) is 110mS/mm, occurring at a drain voltage 0.5V, and the gate voltage -0.65V. The corresponding gate leakage is shown in Fig 4- 46, indicating that the gate leakage is about 13mA/mm.

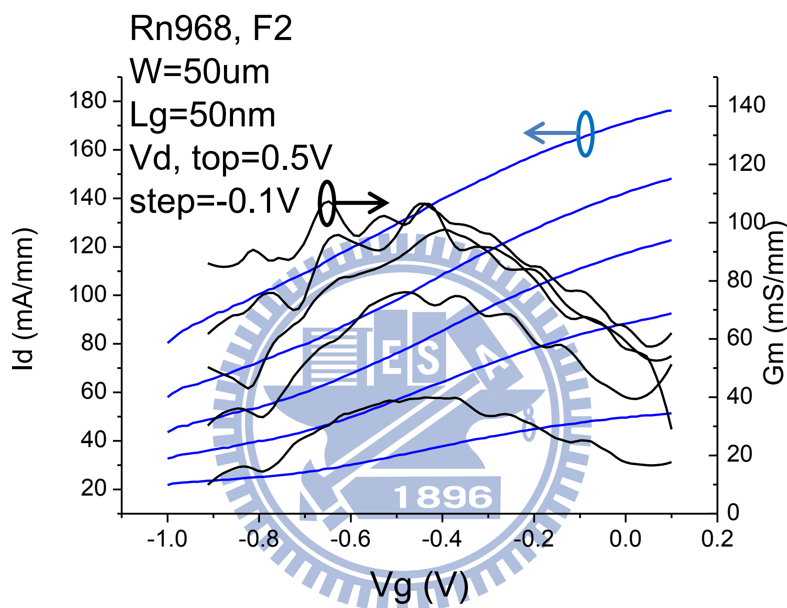


Fig 4- 45 Measured DC transconductance in Rn968 with 50nm of gate length

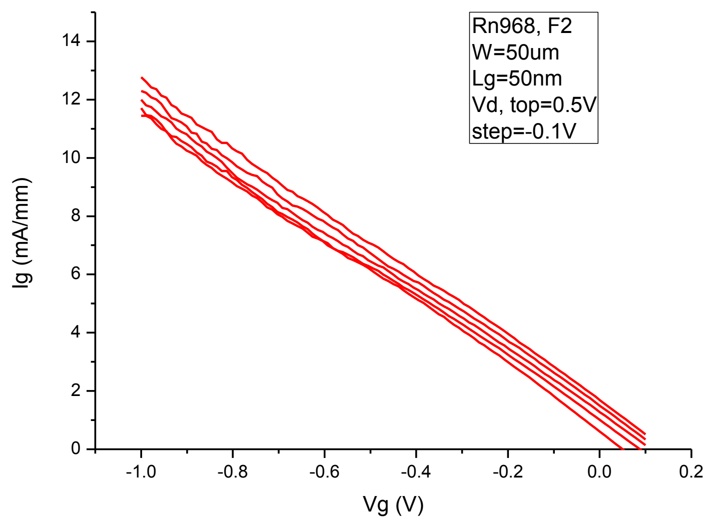


Fig 4- 46 The gate leakage in Rn968 with 50nm of gate length

In RF operation, the current-gain cut-off frequency (*ft*) is 50GHz and the maximum oscillation frequency (*fmax*) is 5 GHz, as shown in Fig 4- 47.

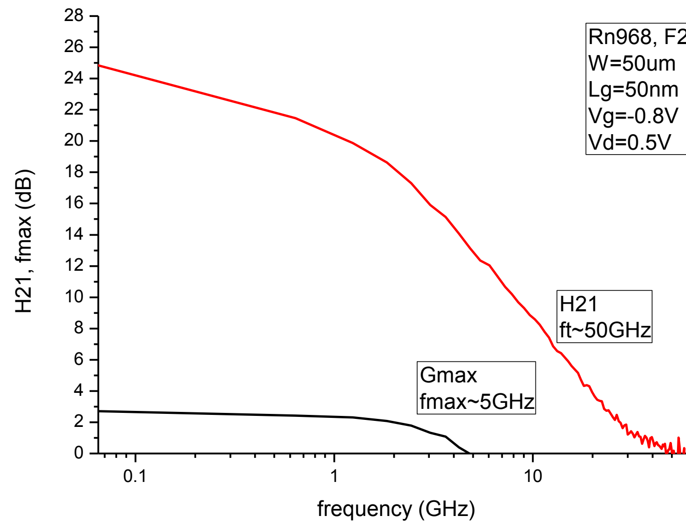
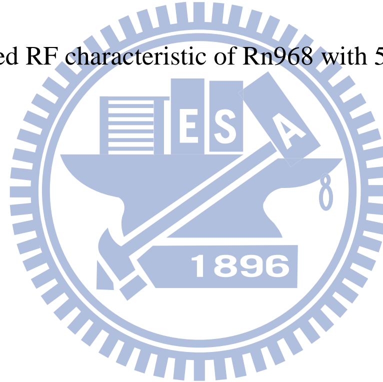


Fig 4- 47 Measured RF characteristic of Rn968 with 50nm of gate length



Chapter5. Conclusions and Future Work

In this work, we studied Sb-based HEMT on GaAs substrate. Using the IMF quantum dot layer and LT-AlSb layer, we could effectively suppress the threading dislocations, which caused from the lattice mismatch between the Sb-based channel material and the GaAs substrate. In addition, we also studied the channel design. The best Hall mobility obtained was $22700cm^2V^{-1}s^{-1}$.

The fabricated device showed excellent dc performance. The maximum transconductance is 730mS/mm at a high drain bias Vd=1.6V for a 2um gate length device. In addition, the occurrence of kink effect at Vd=0.6V was higher than the typical type-II InAs channel device, which was just about Vd=0.4V. In RF performance, the best current-gain cut-off frequency (*ft*) obtained was 50GHz for a 50nm gate length device. Thus, the design of $InAs/InAs_{0.7}Sb_{0.3}$ composite channel in our study demonstrates transport characteristics, and superior channel breakdown performance to the conventional type-II InAs channel device.

However, the epitaxy design and the process still need to be optimized to further improve device RF performance. The ultimate target for us is to fabricate an Sb-based HEMT with RF performance more than 100 GHz.

Reference

[1] S. Reggiani, M. Valdinoci, L. Colalongo, M. Rudan, G. Baccarani, and W. Fichtner, "Electron and Hole Mobility in Silicon at LargeOperating Temperatures—Part I: Bulk Mobility", IEEE Transactions on Electron devices, Vol. 49, No. 3, March 2002

[2] W. Walukiewicz, J. Lagowski, L. Jastrzebski, and H. C. Gatos, "Minority-carrier mobility in p -type GaAs", J. Appl. Phys., Vol. 50, No.7, July 1979

[3] Brian R. Bennett, Brad P. Tinkham, J. Brad Boos, Michael D. Lange and Roger Tsai, "Materials growth for InAs high electron mobility transistors and circuits", J. Vac. Sci. Technol. B 22.2., Mar/Apr 2004

[4] D. K. Gaskill, G. T. Stauf, and N. Bottka, "High-mobility InSb grown by organometallic vapor phase epitaxy", Appl. Phys. Lett. 58 (17), 29 April 1991

[5] B. R. Bennett et al., "Antimonide-based compound semiconductors for electronic devices: A review", Solid-State Electronics. 49, 1875–1895, 2005

[6] Kwang-Man Ko, Jung-Han Seo, Dong-Eun Kim1, Sang-Tae Lee, Young-Kyun Noh, Moon-Deock Kim and Jae-Eung Oh., "The growth of a low defect InAs HEMT structure on Si by using an AlGaSb buffer layer containing InSb quantum dots for dislocation termination", Nanotechnology 20, 225201, 2009

[7] S. H. Huang et al., "Epitaxial growth and formation of interfacial misfit array for tensile GaAs on GaSb", Appl. Phys. Lett. 90, 161902, 2007

[8] M. J. Yang, B. R. Bennett, M. Fatemi, P. J. Lin-Chung, and W. J. Moore., "Photoluminescence of $InAs_{1-x}Sb_x/AlSb$ single quantum wells: Transition from type-II to type-I band alignment", J. Appl. Phys., Vol. 87, No. 11, 1 June 2000

[9] P. S. Dutta, H. L. Bhat and Vikram Kumar, "The physics and technology of gallium antimonide: An emerging optoelectronic material", J. Appl. Phys., Vol. 81, No. 11, 1 May 1997

[10] B. Brar, H. Kroemer., "Influence of impact ionization on the drain conductance in InAs-AlSb quantum well heterostructure field-effect transistors", IEEE Electron Device Lett., Vol. 16, No. 12, 1995

[11] H.-K. Lin, "Design and characteristics of strained InAs/InAlAs composite-channel heterostructure field-effect transistors", J. Appl. Phys., Vol. 97, 2005