Chapter 1
Introduction

Silicon-oxide-nitride-oxide-silicon (SONOS) flash memory has been widely used in recent year. Compared with the conventional floating gate flash memory, SONOS flash memory exhibits great advantages in scaling, storage density, and better immunity to defects in the bottom oxide. Nevertheless, with advances in VLSI processing, SONOS cells become much smaller than before. Therefore, the effect of a single charge may be significant to SONOS cell.

Random Telegraph Signal (RTS) is observed in recent years. Since the signal is very sensitive to surface potential along the channel in SONOS, we can utilize it to do some experiments. Besides, channel hot electron (CHE) program is used. With RTS and CHE program, the trap position can be extracted and CHE program charge lateral profile can be inspected. What is more, program charge retention loss is observed in this thesis. Since there are different types of models for this phenomenon [1.1] [1.2], we do some further investigation. Furthermore, we build a model to simulate program charge V_t retention loss distribution.

There are five chapters in this thesis. Chapter 1 is Introduction, a brief outline is given in this chapter. In Chapter 2, RTS mechanism is reviewed, and CHE program charge lateral distribution is inspected. In Chapter 3, the phenomenon of single a charge retention loss is described. The model for V_t retention loss distribution is built in Chapter 4. At last, Chapter 5 is the conclusion of this thesis.

Chapter 2
Charge Lateral Profile

2.1 Introduction

Current fluctuations because of a single carrier charge trapping/de-trapping in defect states near the Si/gate dielectric interface will become a serious issue of scaling technique. Not only in dynamic random access memory and other digital application, but also as a source of excessive low-frequency noise in analog and mixed-mode circuits.

In a SONOS flash memory cell, random telegraph signal (RTS) in the channel current arises from electron emission and capture at a SiO_2/Si interface trap. Recently, in flash memories, RTS has been recognized as a major scaling concern since a large amplitude RTS will cause a read error in a multilevel-cell flash memory because of V_t fluctuations [2.1] [2.2]. Besides, we can use RTS as internal probe to detect a variation in a trapped charge density during program, erase and retention because it is very sensitive to a local potential change near the trap. There are two kinds of waveform that RTS may exhibit: one is a two-level waveform and the other is a multi-level switching in a current, and these two kinds of waveform depend on the number of traps in a device. Since it is difficult for us to do experiment with devices with multi-level RTS (more than one interface trap), we choose devices with two level RTS (single interface trap).In this way, we can clearly measure trap emission time and capture time.

2.2 RTS Mechanism

Recently, people pay more and more attention to nitride-based trapping storage

flash memory because of its immunity from stress-induced leakage current and the coupling of floating gates in conventional flash memory [2.3]. We can use the mechanisms channel hot electron (CHE) and band-to-band tunneling (BTBT) hot hole to program and erase a two-bits/cell NOR-type SONOS flash memory [2.4]. The major thrust to improve cell performance and scalability is the control of program/erase charge lateral distributions of each bit. A charge pumping (CP) method [2.5] and an inverse I-V modeling approach [2.6] are the two lateral profiling techniques often used. As SONOS cells become smaller and smaller in these years, CP method is not appropriate because the current of charge pumping is hardly sensed in a small area SONOS cell due to a few interface traps in a cell. On the other side, the inverse I-V modeling is an indirect method. This method is to extract a charge lateral distribution by fitting simulated subthreshold and GIDL characteristics to measurement results. There are some limitations of the inverse I-V modeling. First, a two-dimensional device doping profile must be known in device simulation [2.6]. Second, in [2.6] [2.7], the simulated width of a program-state charge distribution varies considerably. For the reasons above, we use RTS method to propose a new charge profiling technique, since it is very sensitive to injected electrons or holes in program/erase operation. Besides, RTS method does not need a 2D numerical device simulation and it is suitable for a small area cell.

A typical two-level RTS waveform is shown in Fig. 2.1. When a trap energy level is a few kT difference to the Fermi level E_f, the drain current fluctuated, where k is the Boltzmann`s constant and T is equilibrium temperature. The trap would be permanently empty when its energy level is several kT above the Fermi level. On the other hand, when the energy level of the trap is several kT below the Fermi level, it would be permanently filled. When there are more than one trap in the bottom oxide near the Fermi level E_f, the RTS waveform will be muti-level as shown in Fig. 2.2. If

RTS is transferred from time domain to frequency domain, $1/f^2$ and 1/f, the waveform is shown in Fig. 2.3(a) and (b), respectively.

There are three main parameters as shows in Fig. 2.1: τ_c, capture time, means the average time to capture an electron, i.e., the trap state is empty. τ_e, emission time, is the average time to emission an electron, i.e., the trap state is full. ΔI_d is the difference between the two level drain current. The local channel potential at the trap position can be extracted from the ratio $<\tau_c>$ to $<\tau_e>$ in RTS according to the following equation:

$$\frac{\langle \tau_c \rangle}{\langle \tau_e \rangle} = g \exp\left(\frac{E_T - E_F}{kT}\right) \propto \exp\left(\frac{-q\Delta\varphi_s}{kT}\right) \qquad \text{Eq (2.1)}$$

where g is a pre-factor, E_T is the trap energy and $\triangle\varphi_s$ is a local potential change at the trap position due to injected program/erase charge. As shown in Fig. 2.4, we can measure surface potential $\triangle\varphi_s$ by measuring $<\tau_c>$ /$<\tau_e>$ and with Eq (2.1).

2.3 Trap Position Extraction by RTS

The samples we used are SONOS flash cells with an ONO thickness of 8.5nm (top oxide), 7nm (nitride) and 5.5nm (bottom oxide). The channel width and length are W/L=0.11μm/0.1μm. V_g=8V/V_{ds} =3.7V for CHE program and V_g=-4V/V_{ds}=5V for BTBT erase. For sure that the channel electric field is uniform, RTS is measured at a small V_{ds} that the device is operated in the linear region. As we can see in Fig. 2.5, the device is programmed at three $\triangle V_t$(=0.3V, 0.9V, 1.2V). The applied voltages are fixed at Vg=3.5V/V_{ds}=0.05V and the device is in strong inversion at the measurement bias. From Eq 2.1, as $\triangle V_t$ increases, $<\tau_c>$ /$<\tau_e>$ decreases. In Fig. 2.5, we can obviously observe the phenomenon. From the result of this experiment, we can sure

that by measuring the value of $<\tau_c>$ /$<\tau_e>$, the surface potential φ_s will be known.

The way of extracting an interface trap position (L_t) is similar to [2.8]. As shown in Fig. 2.6, we can have the following equation:

$$\frac{\Delta V_{ts}}{\Delta V_{ds}} = \frac{L_{ts}}{L_{ds}} \qquad \text{Eq (2.2)}$$

where V_{ts} is the channel potential at the trap position, L_{ts} is the distance of the trap from the source edge and L_{ds} is the channel length. Besides, $<\tau_c>$ depends on the electron concentration as the following equation:

$$<\tau_c> = \frac{1}{n_e \sigma \upsilon_{th}} \qquad \text{Eq (2.3)}$$

where n_e is the electron density, σ is the capture cross-section, and v_{th} is the thermal velocity. Two different drain voltages (V_{ds}=0.05V and 0.3V) are used in RTS and $<\tau_c>$ measurement. From Eq (2.3), $<\tau_c>$ depends on the electron concentration n_e, or a voltage drop between the gate (V_{gs}) and the channel right below the trap (V_{ts}). As shown in Fig. 2.7, the difference of the voltages ($\triangle V_{ts}$) at the point of the trap (L_{ts}) is equal to the lateral shift of these two curves, raised by two drain voltages. From the above, we can extract the trap position in the channel from Eq (2.2).

In our experiment, more than 150 fresh cells with RTS are measured, but we only record devices with two-level (i.e., a single trap) RTS for simplicity. The cumulative trap position distribution along the channel is shown in Fig. 2.8, and from the figure we can conclude that more process-induced interface traps are near the source/drain junctions. To do experiments as the following sections, we choose devices with appropriate trap positions to investigate program/erase charge lateral spread.

2.4 CHE Program Charge Lateral Profile

Since RTS is very sensitive to surface potential as described in section 2.2, we can use it as a probe to investigate the charge distribution in a SONOS flash memory. In this section, we use RTS to inspect the lateral distribution of injected charge in a SONOS flash memory in program sates. The concept is to use the interface trap, which position in the channel is known (by the way in section 2.3), as internal probe to detect a local channel potential change resulting from injected charge during program. By using RTS method, the lateral width of injected charge by channel hot electron (CHE) program induced potential barrier can be know.

From now on, we define a parameter x_t which is the trap distance to the drain junction (i.e. x_t=1-L_{ts}). In order to know the lateral profile of CHE program charge, four SONOS of different trap position at x_t=0.03L_{ds}, 0.05 L_{ds}, 0.2 L_{ds} and 0.3 L_{ds} are used. As the schematic diagram shown in Fig. 2.9(a), we can predict that if the trap position is near the drain junction, more electrons are injected into the nitride layer above the trap position, then the conduction band-edge at x_t and the trap energy level (E_t) move upward with respect to the Fermi level. From eq. (2.1), $<\tau_c>/<\tau_e>$ ratio increases in this kind of situation. On the contrary, as shown in Fig. 2.9(b), if the trap position is away from the drain junction, few electrons are injected into the nitride layer above the trap position, then the conduction band-edge and the trap energy (E_t) remain almost unchanged, and so as $<\tau_c>/<\tau_e>$ ratio.

Since $<\tau_c>/<\tau_e>$ ratio increases with $\triangle V_t$ (described in section 2.2), the measurement result of $<\tau_c>/<\tau_e>$ versus $\triangle V_t$ in the four cells described above are shown in Fig. 2.10. The τ_c/τ_e ratio increases more rapidly with $\triangle V_t$ for a x_t closer to the drain junction, for example, the x_t=0.03L_{ds}. This implies that higher program charge density is at the trap position x_t=0.03L_{ds}. On the other hand, at x_t=0.3L_{ds} , the

τ_c/τ_e ratio remains almost unchanged, which means the injected program charge does not reach the trap point during program.

For further investigation of the lateral charge distribution of CHE program, the measurement result of the surface potential change along the channel versus the trap distance (x_t) for a program window of $\triangle V_t$=0.6V is presented in Fig. 2.11. We can see that the trend of the surface potential change decreases as the trap distance increases, and the surface potential remains almost unchanged when x_t is at $0.3L_{ds}$. From eq. (2.1), this concludes that the potential barrier induced by the program charge is within 30nm for $\triangle V_t$=0.6V. Our result is consistent with most of published results from Monte Carlo simulation [2.9] [2.10] and from the inverse I-V method [2.11] [2.12].

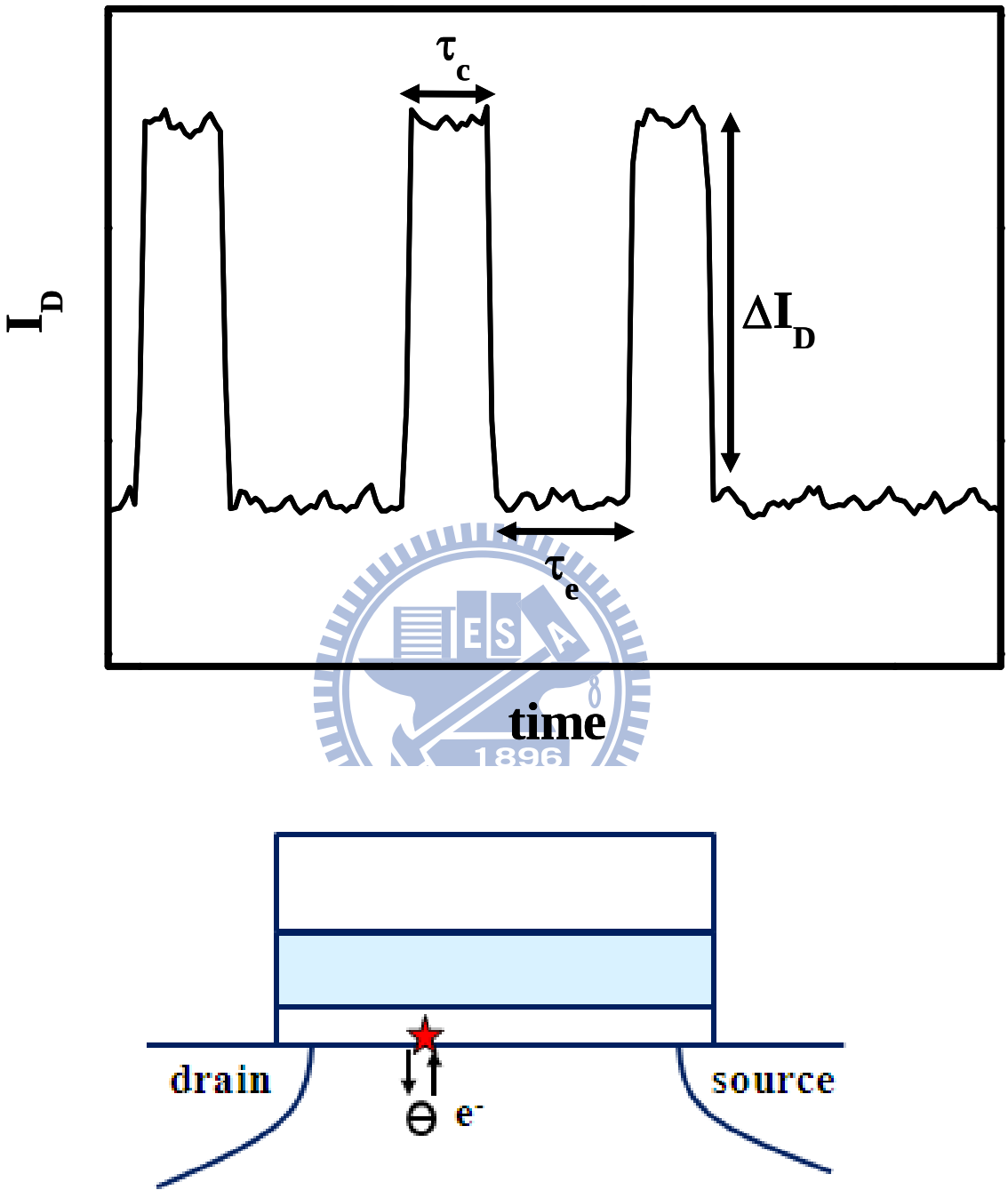


Fig. 2.1 A two-level RTS waveform resulting from electron emission and capture at an interface trap. τ_c and τ_e are electron emission time and capture time.

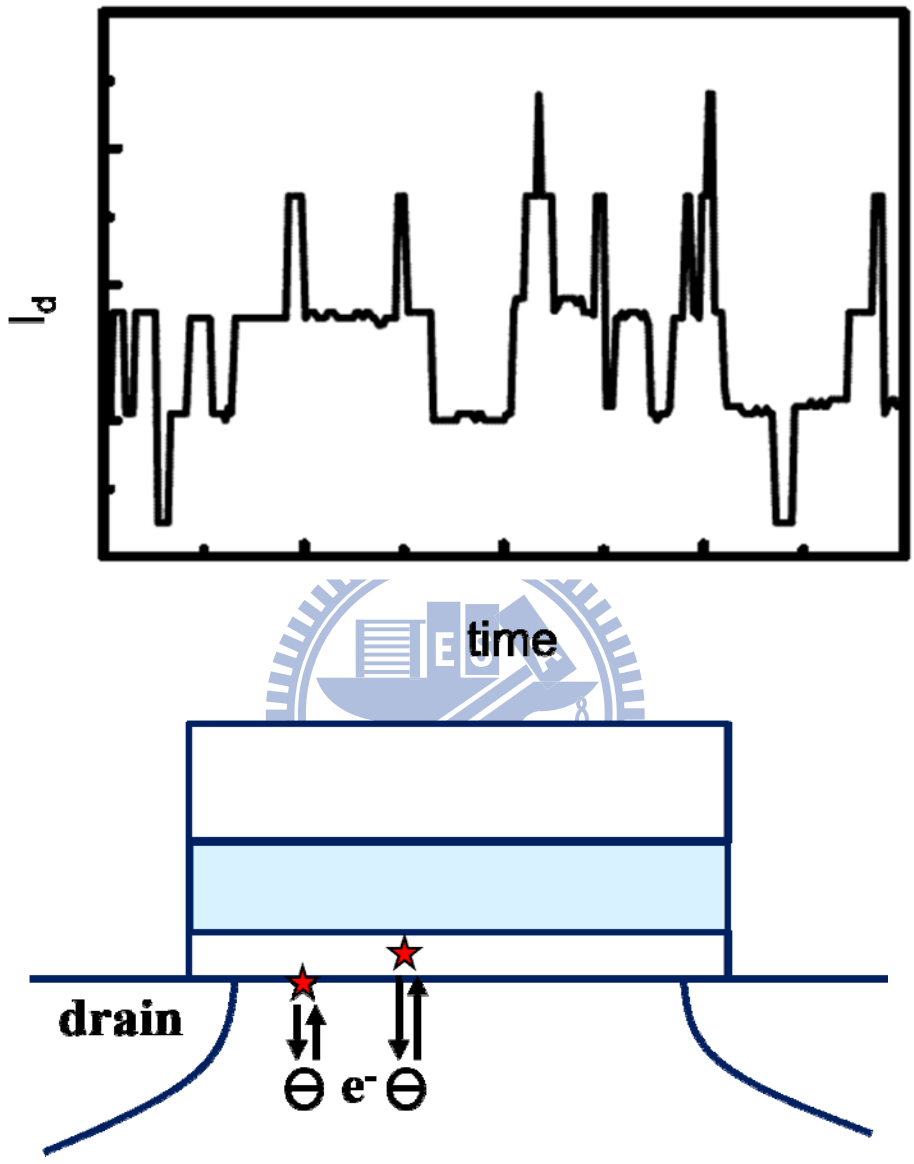


Fig. 2.2 A multi-level RTS waveform. There are more than one trap in the bottom oxide.

Fig. 2.2(a)

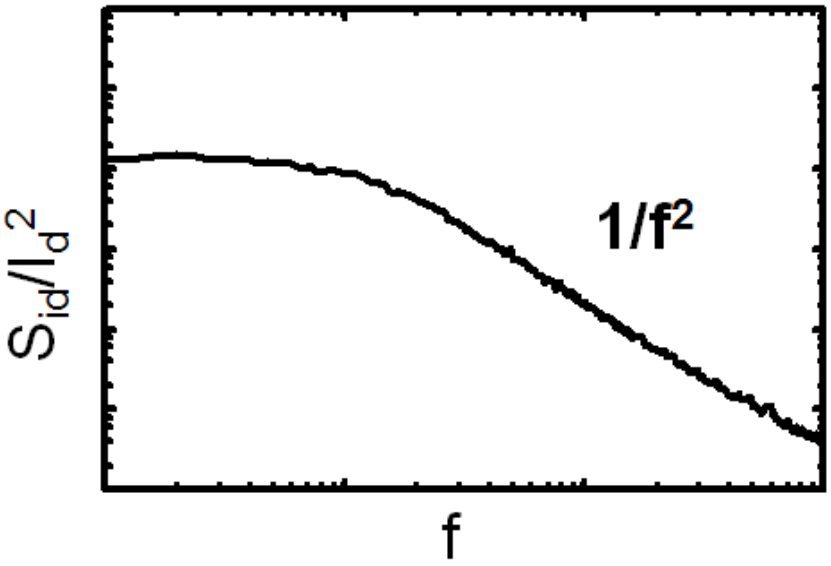


Fig. 2.2(b)

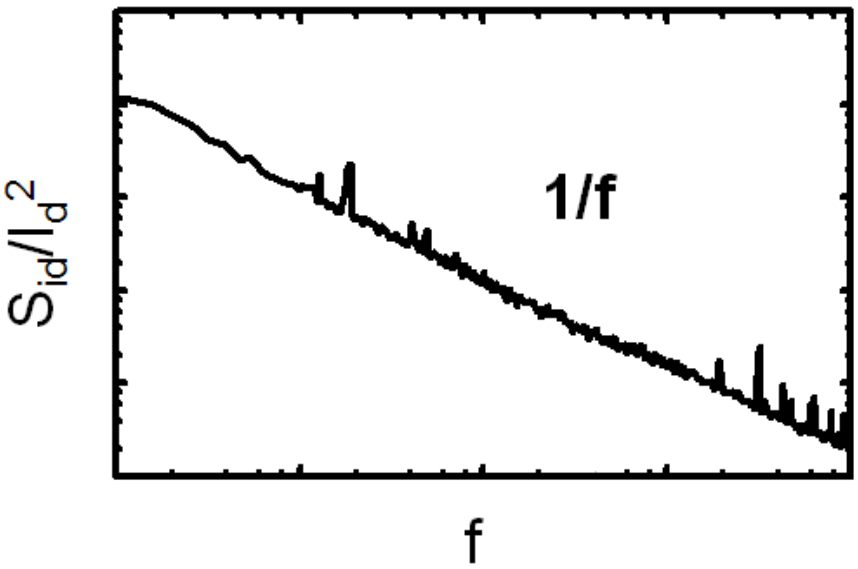


Fig. 2.3 Transfer RTS from time domain to frequency domain in (a) $1/f^2$ (b)1/f by Fourier transform.

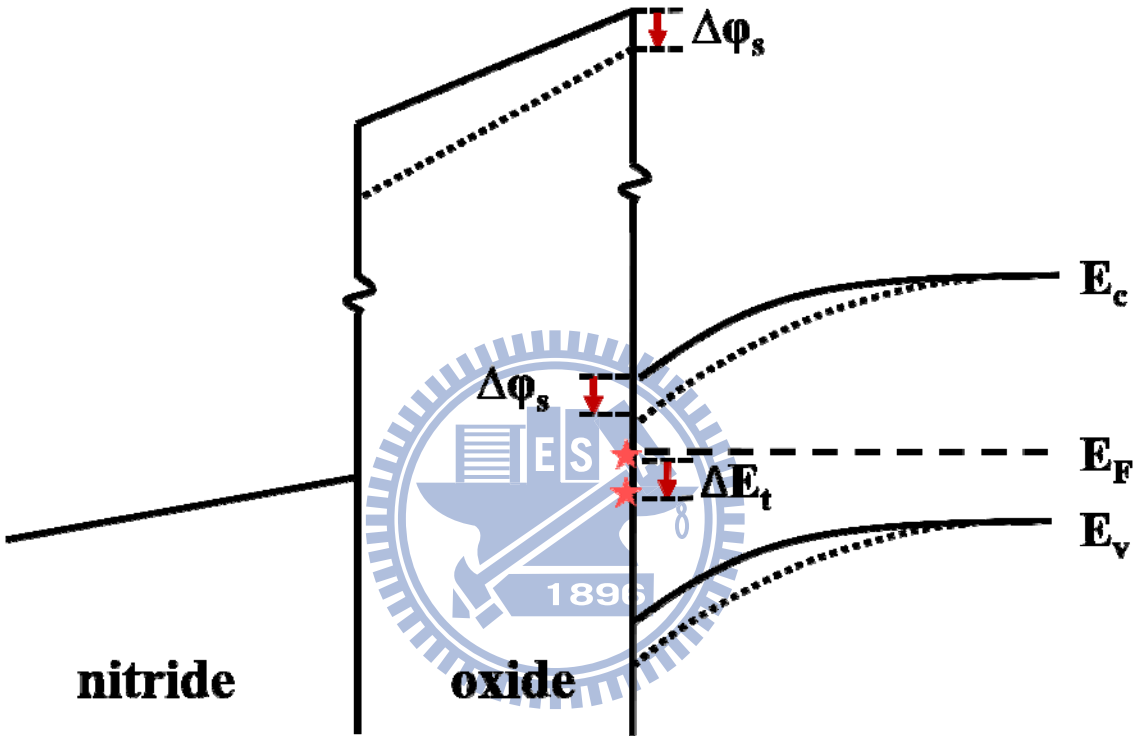


Fig. 2.4 The band diagram showing the energy change of surface potential ($\triangle\varphi_s$) and interface trap ($\triangle E_t$).

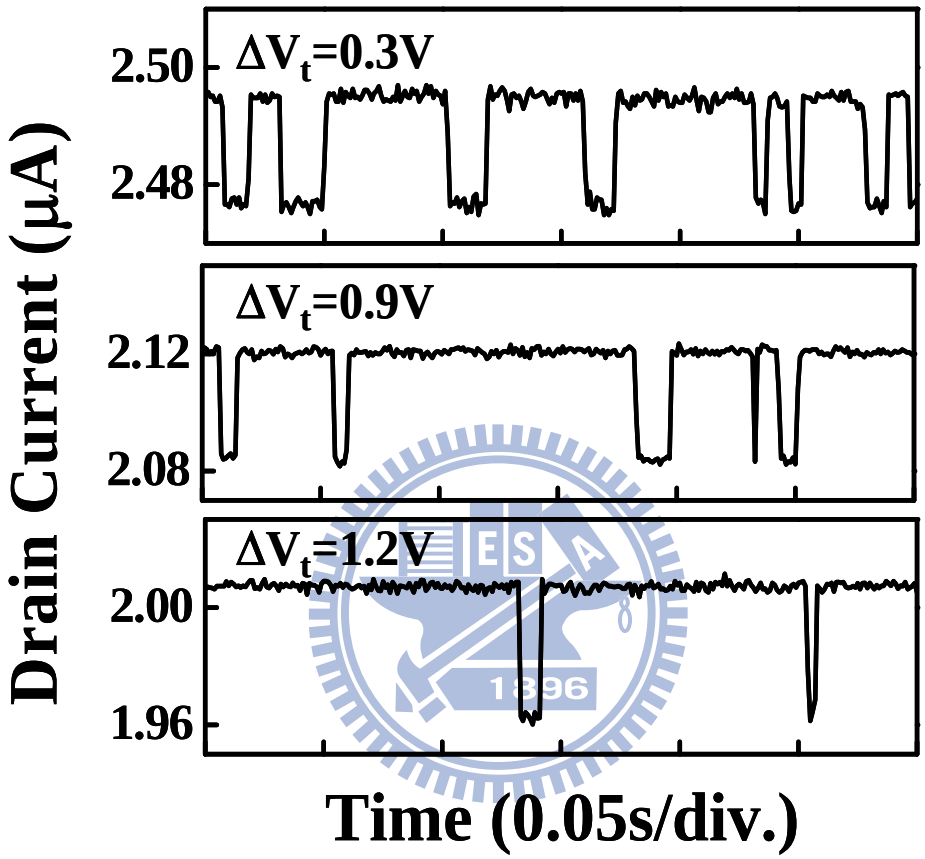


Fig. 2.5 RTS patterns as device programmed at three different $\triangle V_t$.

The applied voltages are fixed at V_{gs}=3.5V and V_{ds}=0.05V.

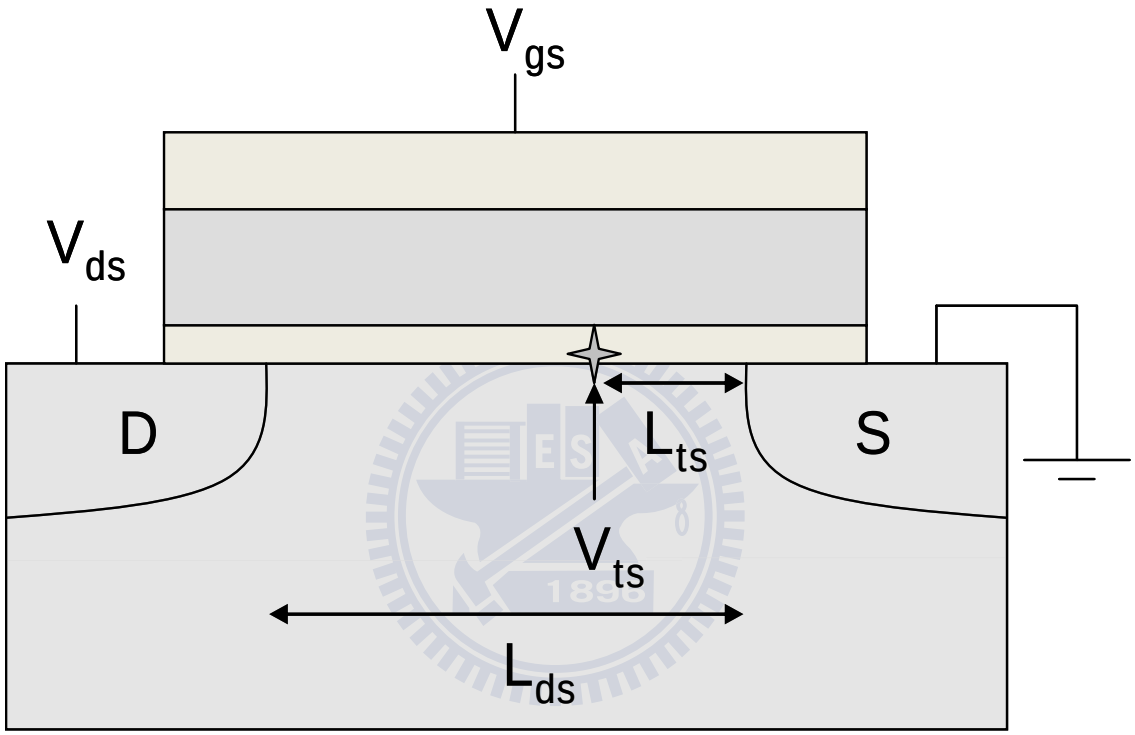


Fig. 2.6 Illustration of the extraction of the trap position

L_{ts} is the trap position from the source junction.

V_{ts} denotes the channel potential right below the trap.

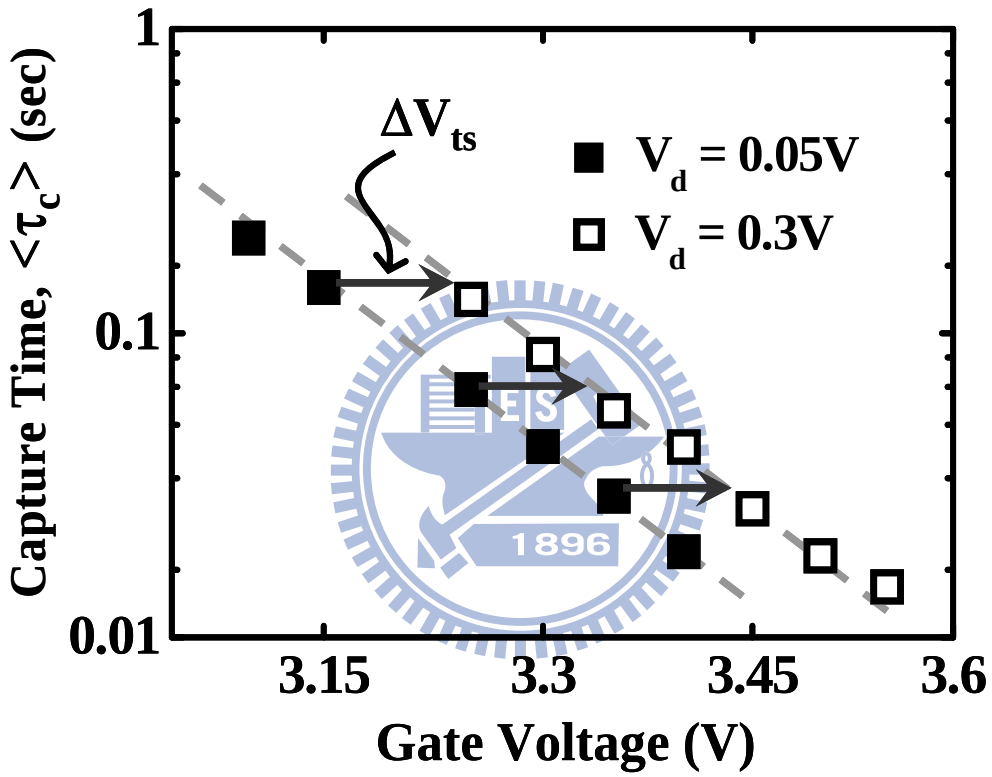


Fig. 2.7 The gate voltage dependence of $<\tau_c>$ at two different drain voltages (Vds=0.05V and 0.3V). $\triangle V_{ts}$ is equal to the lateral shift of these two curves

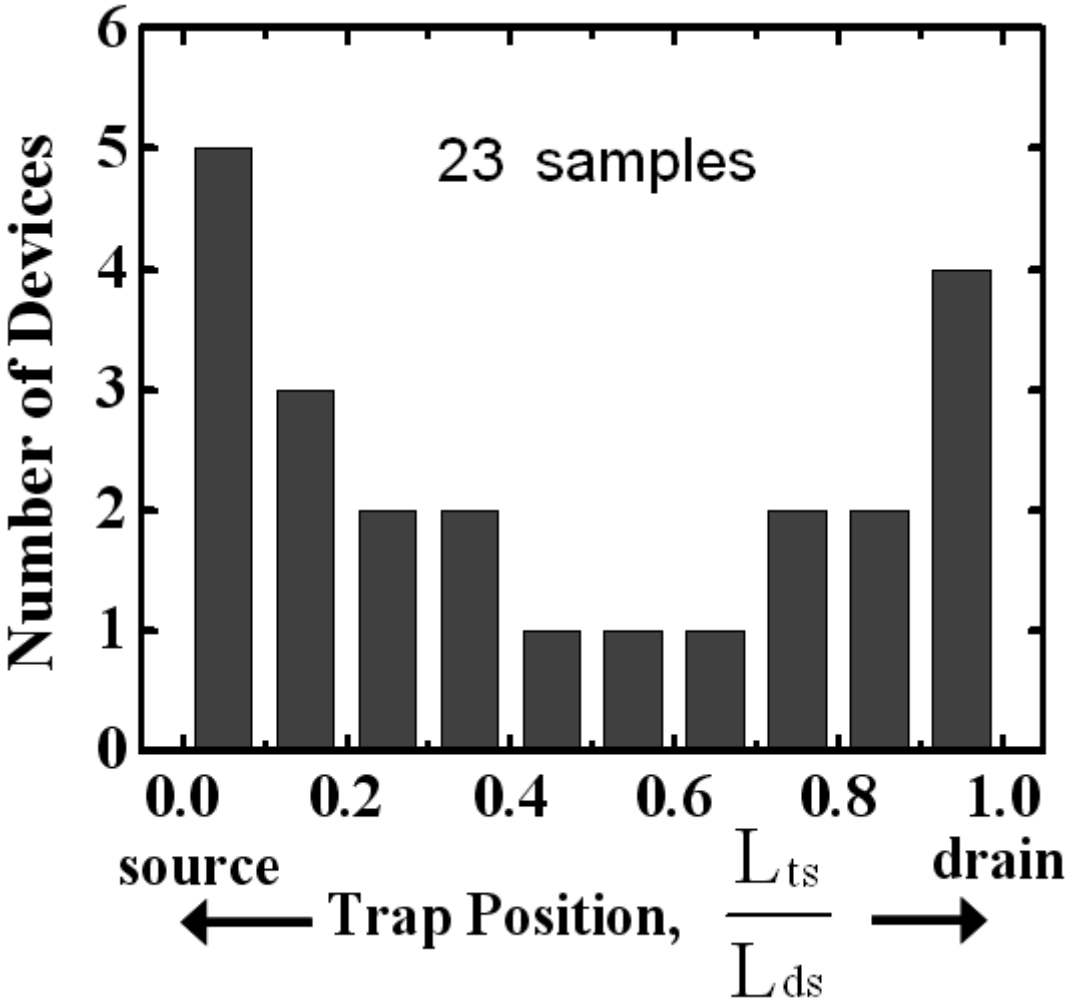


Fig. 2.8 Cumulative trap position distribution along the channel. L_{ds}=0.1μm is the channel length and L_{ts} is the distance of a trap from the source.

Fig. 2.9(a)

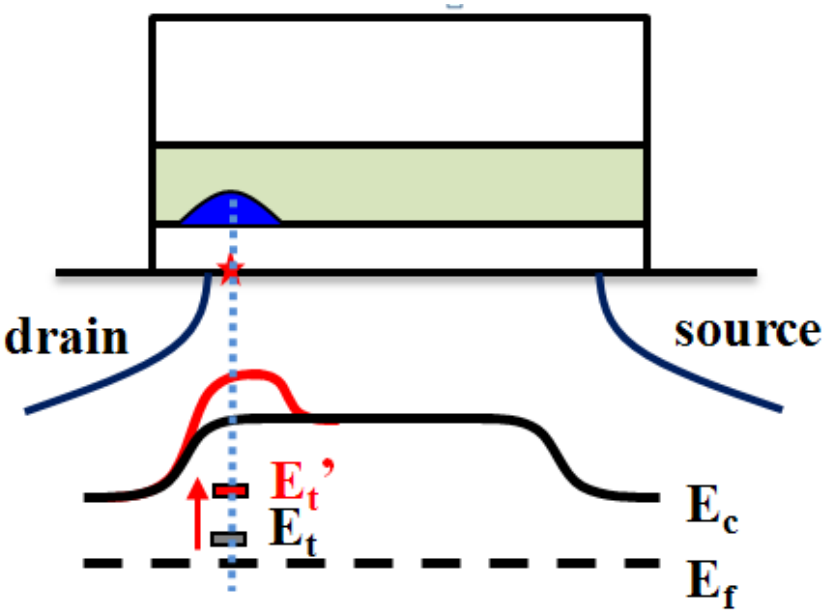


Fig. 2.9(b)

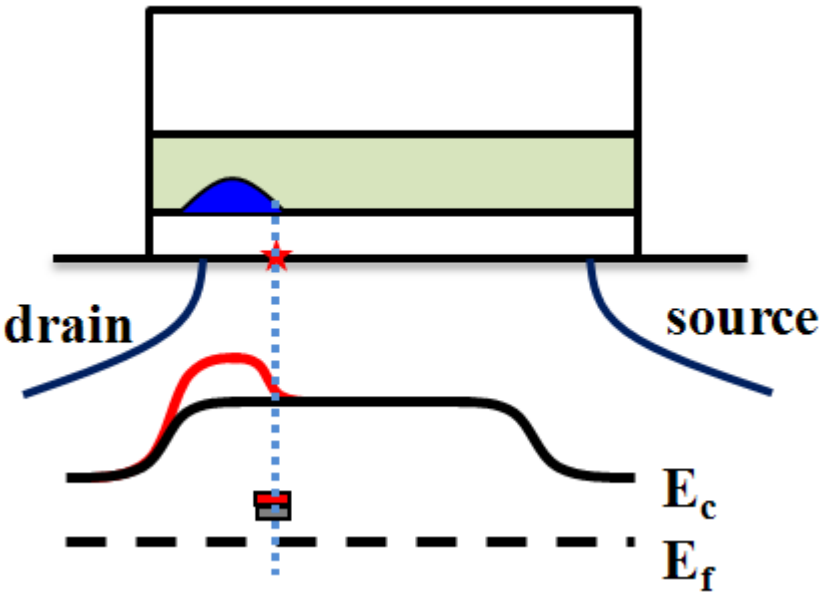


Fig. 2.9 Schematic diagrams of trap energy level (E_t) change during CHE program.

(a) The trap position is near the drain junction.

(b)The trap position is away from the drain junction

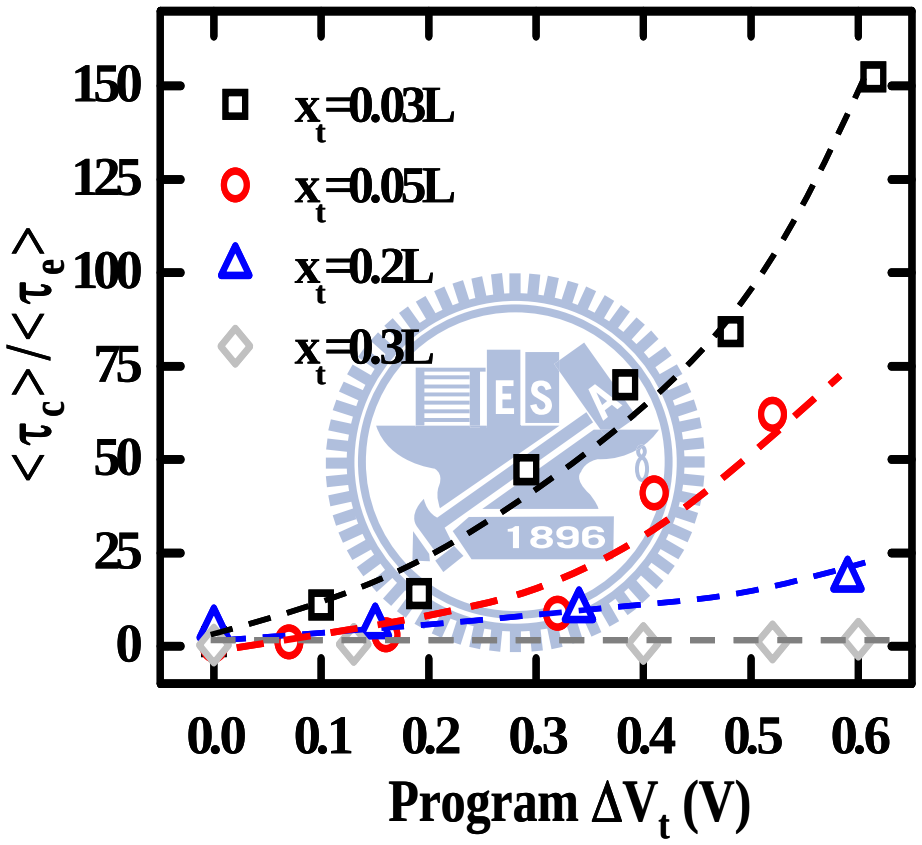


Fig. 2.10 The $<\tau_c>/<\tau_e>$ ratio versus program $\triangle V_t$ at four different trap positions x_t =0.03L_{ds}, 0.05L_{ds}, 0.2L_{ds} and 0.3L_{ds}

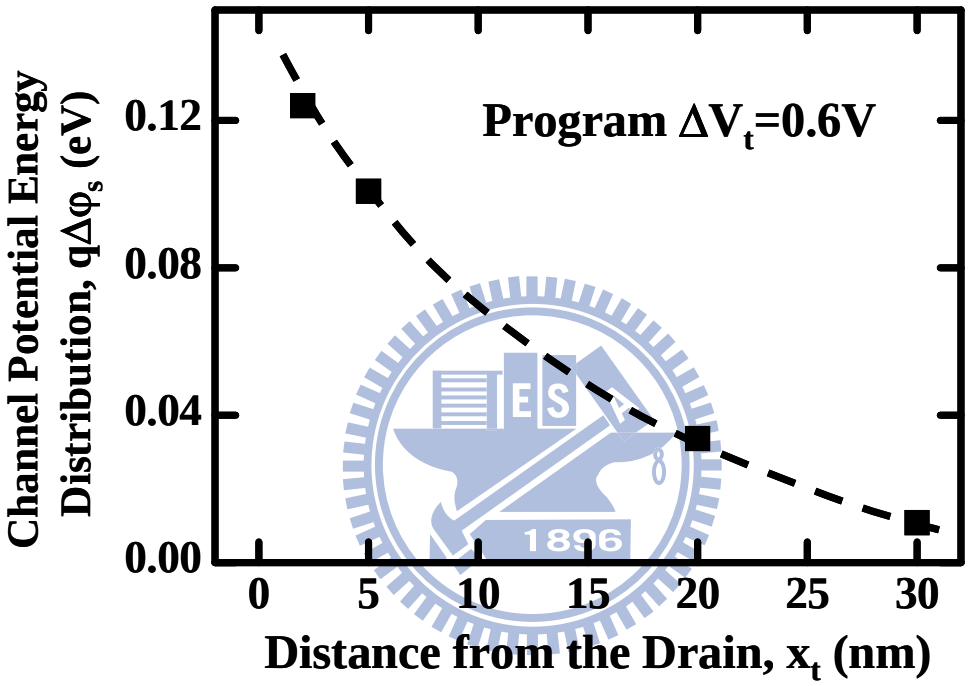


Fig. 2.11 The channel potential energy distribution extracted from RTS. The program window is $\triangle V_t$=0.6V. The potential barrier width is about 30nm.

Chapter 3

Single Charge Retention Loss

3.1 Introduction

In recent years, the SONOS flash memory scaling advances aggressively, and the size of the SONOS flash memory becomes much smaller than in the past few years. Therefore, the number of the program charge in the nitride reduces greatly. For this reason, a single charge loss may affect the read current and result in a read failure. The reasons for the program charge retention loss have been explained in many ways. In this chapter, we find some evidences to explain the reasons for program charge retention loss.

What is more, as the charge spread for CHE program is random, we can regard the single charge loss phenomenon as a percolation effect intuitively. The research of RTS induced V_t fluctuation has been done widely. For example, in [3.1], the distribution of RTS in floating gate is exponential. Therefore, we can predict that the distribution of a single charge loss is exponential, for its mechanism is familiar to RTS. At the end of this chapter, we gather statistics of 275 single charge loss samples to inspect whether the distribution is exponential or not.

3.2 Phenomenon of Program Charge Retention Loss

Two phenomena of single charge are discussed in this section: First one, as shown in Fig. 3.1(a), is RTS, which is described in CH.2. For RTS, read current fluctuated between different levels (depends on the number of traps in the device), which is due to a single electron tapping/de-trapping at a Si/SiO_2 interface trap.

Second phenomenon is program charge retention loss, as shown in Fig. 3.1(b). The staircase-like read current with retention time is due to the discrete charge loss.

In recent studies, as shown in Fig. 3.2, program-state V_t retention loss is explained by three kinds of models. Fig. 3.2(a) shows the first explanation that program-state V_t retention loss is due to the nitride charge vertical loss through the bottom oxide [3.2] [3.3]. The second explanation, presented in Fig. 3.2(b), is that lateral nitride charge redistribution in program state induces the V_t retention loss [3.4] [3.5]. The last explanation is that nitride trapped holes migration in program state, and this explanation should be assumed that a three-pole electron-hole-electron distribution is in program state [3.2] [3.3].

First of all, we do an experiment to exclude the second explanation (nitride charge lateral redistribution). We choose a SONOS cell with a trap located at $x_t=0.03L_{ds}$ form the drain. The cell is programmed only once and baked in 120℃ for about an hour. RTS method is used to explore the possibility of program electron lateral movement. The experiment result is presented in Fig. 3.3, and $<\tau_c>/<\tau_e>$ remains unchanged, which means the program electron concentration is the same during baking. From the result described above, we can conclude that there is no lateral redistribution within our measurement time.

Next, the third explanation of nitride trapped holes migration may be excluded due to the following experiment. Two cells with a trap at $x_t=0.05L_{ds}$ and $0.12L_{ds}$, respectively, are chosen. The $<\tau_c>/<\tau_e>$ is measured in program-state and erase-state at different P/E cycles for the two cells. The result of the cell with $x_t=0.05L_{ds}$ is shown in Fig. 3.4(a). Since RTS becomes unclear over 20 P/E cycles, 16 $<\tau_c>/<\tau_e>$ data are recorded in our experiment. As we can see in Fig. 3.4(a), the $<\tau_c>/<\tau_e>$ in program-state is always larger than either in a fresh cell or in erase-state. The other cell with $x_t=0.12L_{ds}$ shows the same result. This means a negative polarity is in

program-state in all the measured cells, i.e., no evidence of positive charge (hole) accumulation in program.

From the conclusion of the previous paragraphs, there is no sign of hole accumulation in 20 P/E cycles, but program charge retention loss in these cells under a gate stress V_g=-5V is still observed apparently as shown in Fig. 3.5. The $<\tau_c>/<\tau_e>$ ratio decreases with gate stress time for RTS traces immediately after program. Since nitride charge lateral movement and hole accumulation are excluded as described above, the decreases of $<\tau_c>/<\tau_e>$ is attributed to nitride charge vertical loss through the bottom oxide. For more evidence on our conclusion, we make the assumption as shown in Fig. 3.6. If there are holes accumulated and had lateral migration in the nitride in program-state, as shown in Fig. 3.6(a), the curve of I_d traces with time should increase smoothly. On the other hand, if the program charge retention loss is a vertical loss, the curve of I_d traces time should increase abruptly at sometime. To prove this assumption is true, we use the measurement setup presented in Fig. 3.7(a). An electronic switch is used to record gate stress time accurately. The sampling is 10kHz, which enable the observation of read current switching with time resolution up to 0.1ms. The experiment result is shown in Fig. 3.7(b), and the cell in under 33 P/E cycles. The result in Fig. 3.6(b) is identical to our assumption. Besides, the current level remains almost the same between two consecutive nitride charge escape. This means during the gate stress, no diffusive process is observed. Therefore, since the lateral migration is in nature a diffusion process, charge lateral transport should be ruled out according to our experiment. From the description above, we can prove that program charge retention loss is vertical loss.

3.3 Distribution of Single Charge Loss

In [3.1], we know that RTN induced Vt fluctuation in floating cells is exponential distribution. Since the purpose of statistic single charge loss distribution in this section, RTN induced Vt fluctuation must be confirmed to an exponential distribution in SONOS cells for sure that it is an percolation effect. RTN amplitude (ΔV_t) measured in program/erase state is shown in Fig. 3.8. A program-state RTN amplitude is almost independent of erase-state RTN in SONOS cells, which means the percolation effect may cause by random program charge. What is more, 3D atomistic device simulation of RTN is represented in Fig. 3.9. The simulation result shows that RTN induced Vt fluctuation in SONSO cells is an exponential distribution, similar to RTN in floating gate cells.

The importance of single charge loss has been widely emphasized described as the previous sections. In RTN, a single charge may affect the current percolation path and makes the read current fluctuated in two or more levels. It had been studied that RTN percolation effect in floating gate cells has the equation as following [3.1]:

$$f(|\Delta V_T|) = \frac{1}{\sigma}\exp(-\frac{|\Delta V_T|}{\sigma}) \qquad \text{Eq. (3.1)}$$

where σ the distribution standard variation. In eq. (3.1), ΔV_t in percolation effect of RTN is an exponential distribution, and the figure is shown in [3.1] (Fig.4). From the first paragraph of this section, we know that RTN induced Vt fluctuation shows an exponential distribution in SONOS cells. Since a single charge vertical loss is a kind of percolation effect, we predict that it may have the exponential distribution similar

to RTN. For this reason, we statistic the read current fluctuation with a single charge escaping, and investigate whether a single charge vertical loss is an exponential distribution or not.

At first, we choose SONOS cells which bottom oxide is 5.5nm thick with L/W=0.11μm/0.11μm. It is hard to observe a single charge loss since the bottom oxide is too thick for a single charge to tunnel through. In Fig. 3.10(a), we cannot see any charge loss less than 3 P/E cycles, only when the cell is P/E for 70 times, charge loss can be observed. Since the cell is P/E for many times, some traps are generated in the bottom oxide and RTN may be observed as the inset of Fig. 3.10(a). Although RTN is observed, we can clearly distinguish a single charge loss and RTN as shown in Fig. 3.10(a). The staircase-like current jump can be concluded to a single charge loss. In this way, a single charge loss can be observed, but the cell needs to be P/E for more than 50 times. Another way we use is a negative voltage applied in retention phase to accelerate nitride charge loss. In Fig. 3.10(b), V_g=-5V is applied, and charge loss can be observed. Besides, no charge loss is found without applied voltage on gate (i.e., V_g=0V). As description above, the result we want can be measured by these two methods, but it takes a lot of time. Therefore, we choose cells which bottom oxide is 2nm thick as the following experiment.

The cell with 2nm bottom oxide is programmed in different window (ΔV_t). More charges escape when ΔV_t is larger, as presented in Fig. 3.11, which is due to more stored charges in nitride with larger program window. Therefore, the cells is programmed with ΔV_t=4V. Since ΔI_d is similar to ΔV_t in physical meaning, we measure $\Delta I_d/I_d$ in convenience and statistic $\Delta I_d/I_d$ for 275smaples. The experiment result is presented in Fig. 3.12. As we can see the distribution of a single charge loss shows an exponential distribution, and this result is the same as our prediction.

Fig. 3.1(a)

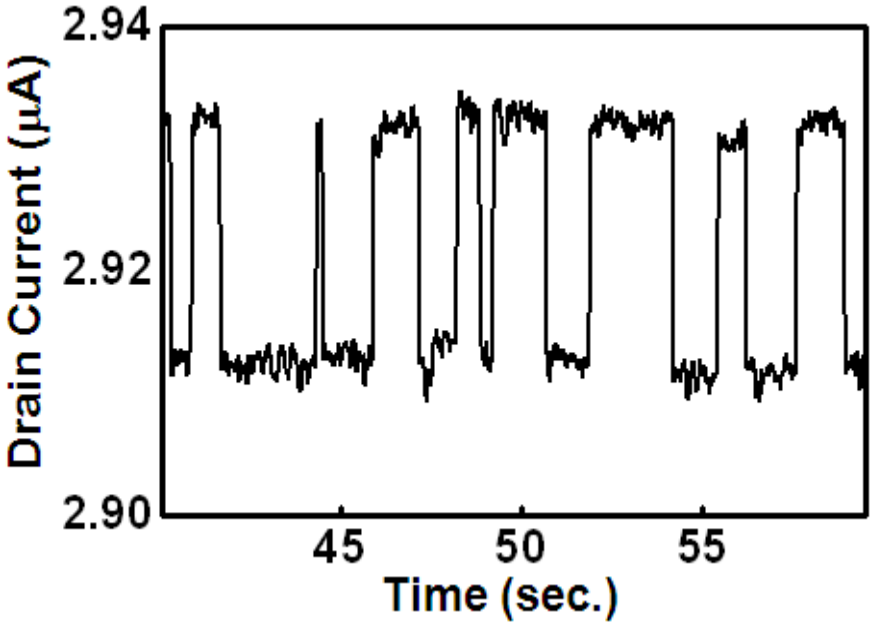


Fig. 3.1(b)

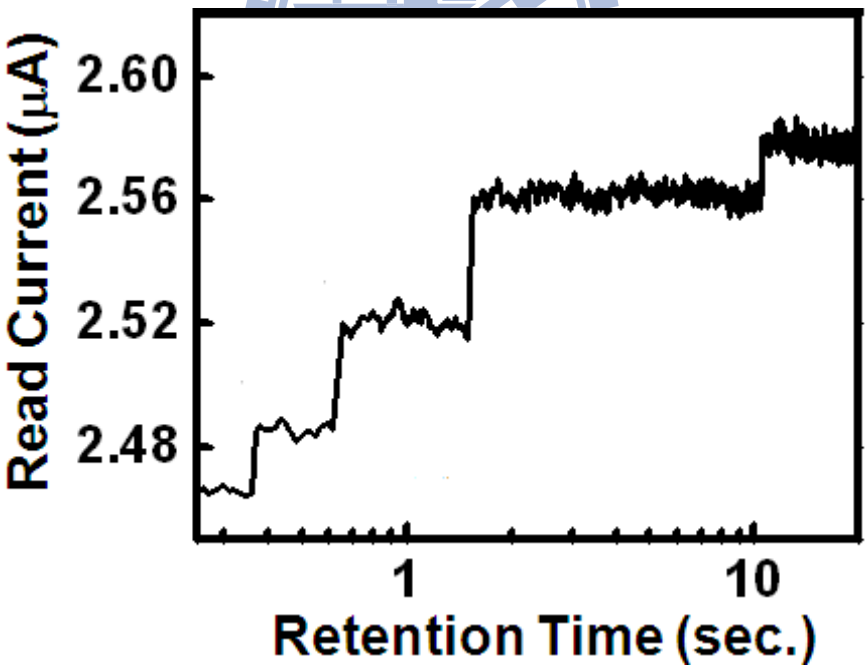


Fig. 3.1 (a) A typical two-level RTN waveform.

(b) Phenomenon of program charge loss, with staircase-like read current.

Fig. 3.2(a)

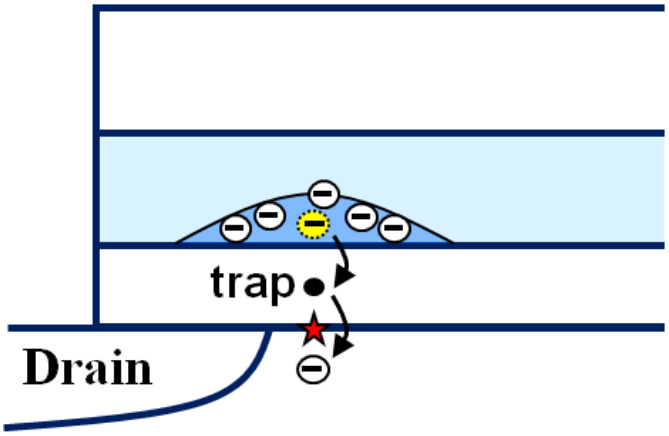


Fig. 3.2(b)

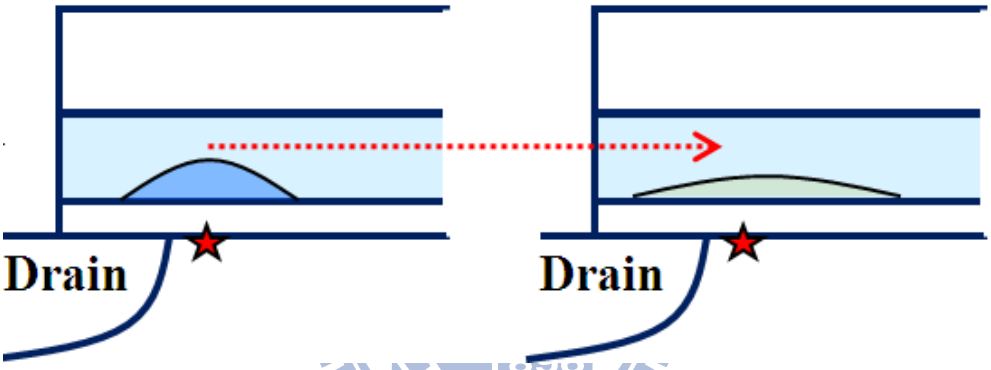


Fig. 3.2(c)

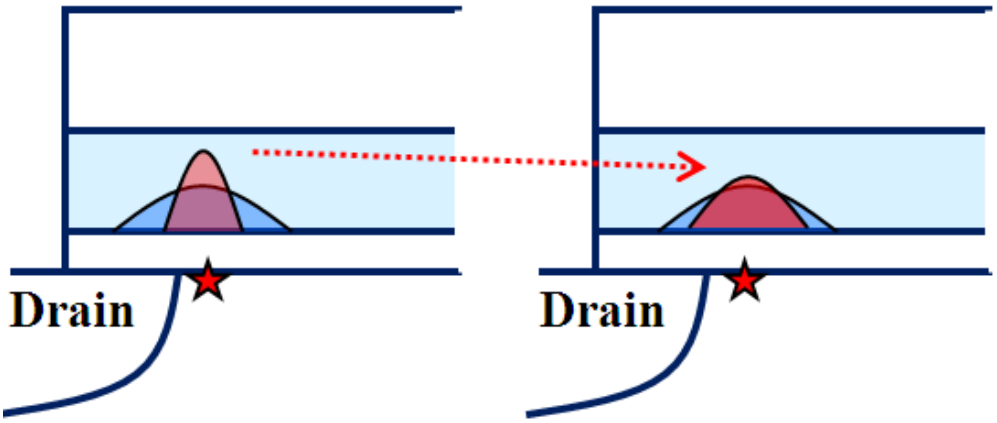


Fig. 3.2 Three types of model for program charge retention loss.

(a) Chare vertical loss (b) Electron lateral redistribution

(c) Hole migration in program-state

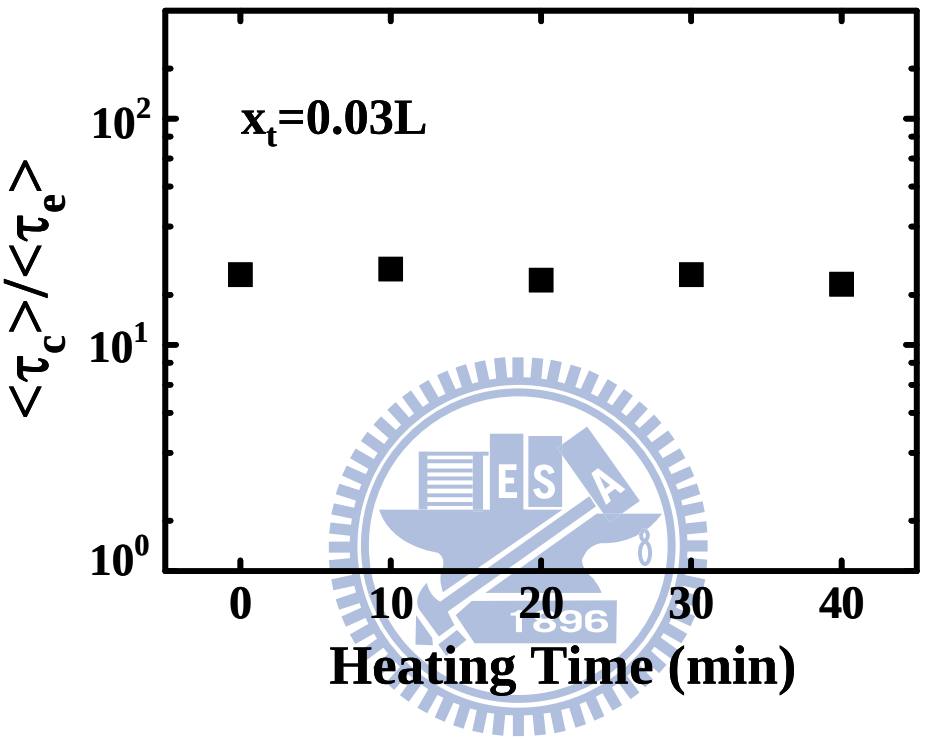


Fig. 3.3 $<\tau_c>/<\tau_e>$ versus heating time for a cell with trap position is located at $0.03L_{ds}$ from drain.

Fig. 3.4(a)

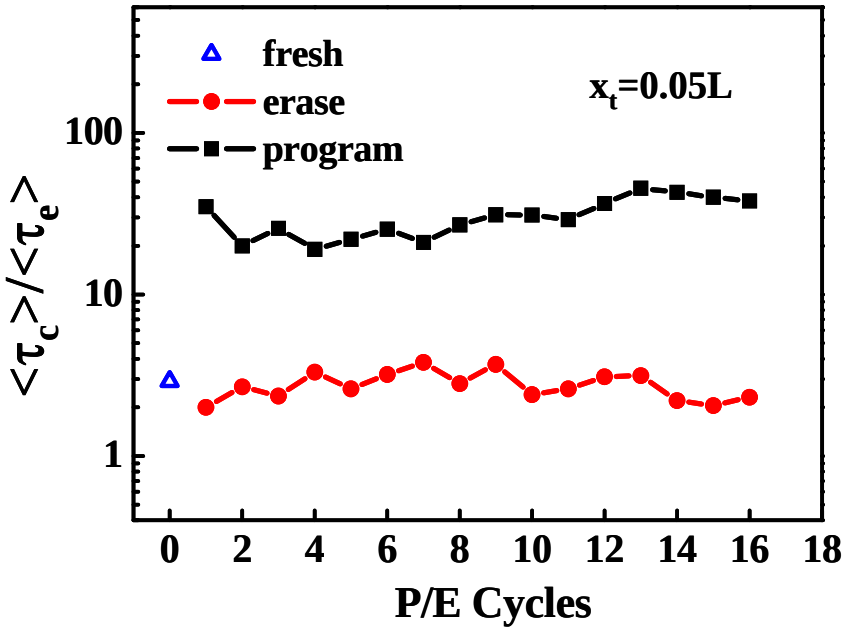


Fig. 3.4(b)

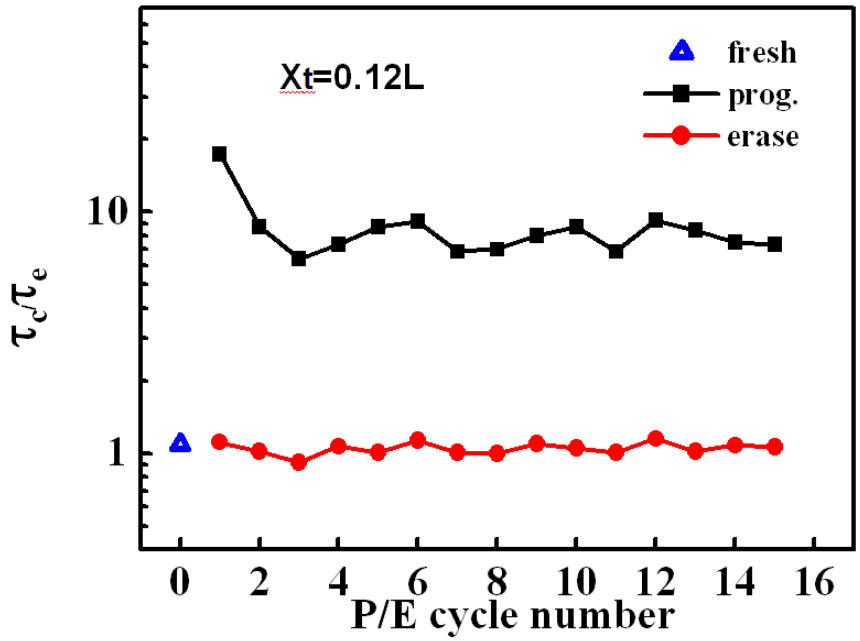


Fig. 3.4 $<\tau_c>/<\tau_e>$ in program-state and in erase-state at different P/E cycles, with the trap position located at (a) $0.05L_{ds}$ and (b) $0.12L_{ds}$ from drain.

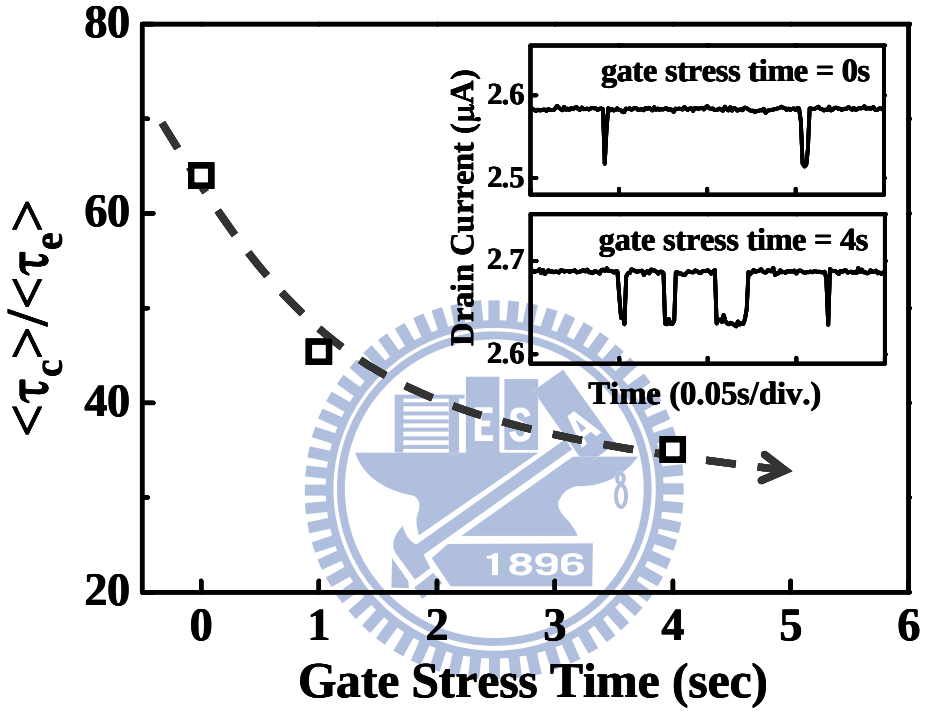


Fig. 3.5 $<\tau_c>/<\tau_e>$ is plotted against gate stress time. ΔVt=1V and gate stress voltage is V_g=-5V. The trap position is at $x_t=0.05L_{ds}$.

Fig. 3.6(a)

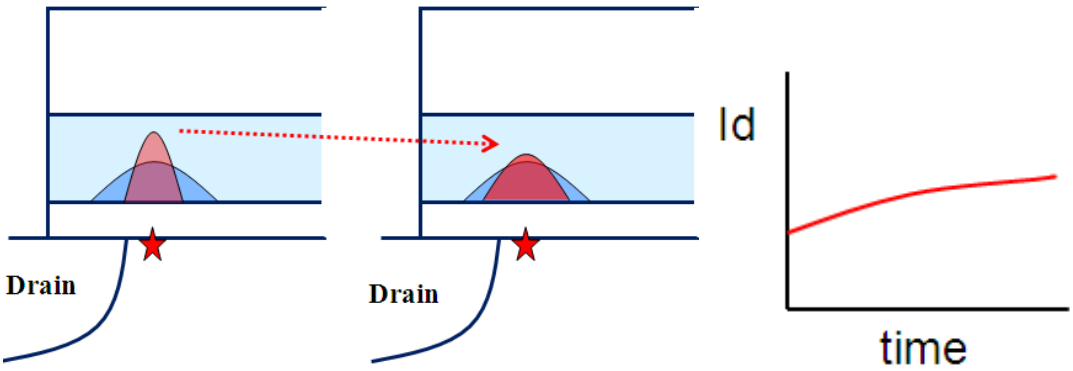


Fig. 3.6(b)

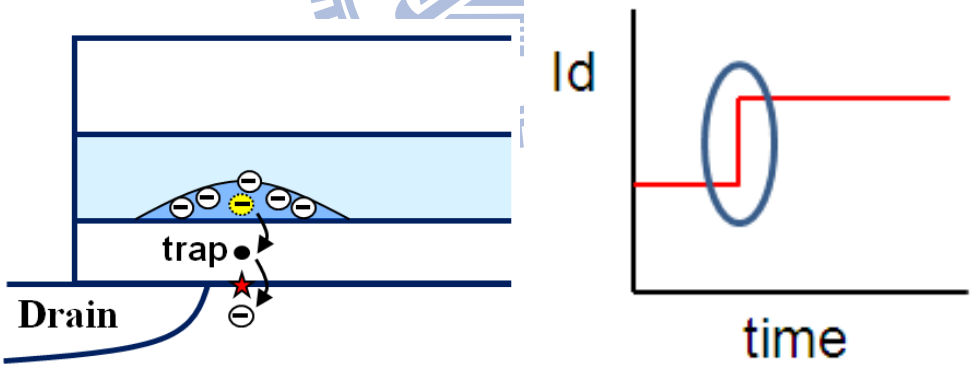


Fig. 3.6 Prediction of I_d versus time for two different charge loss modes.

(a) Holes migration in program-state. I_d should increase smoothly.

(b) Charge vertical loss. I_d should increase abruptly.

Fig. 3.7(a)

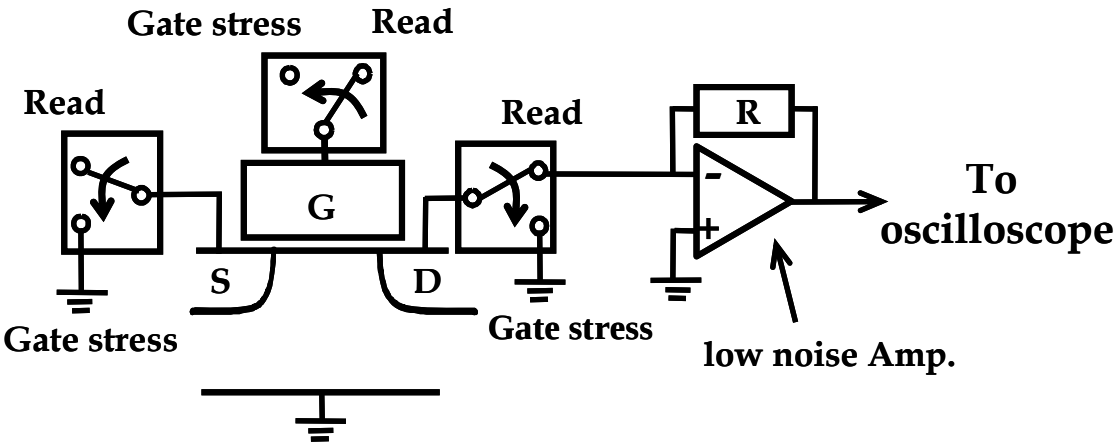


Fig. 3.7(b)

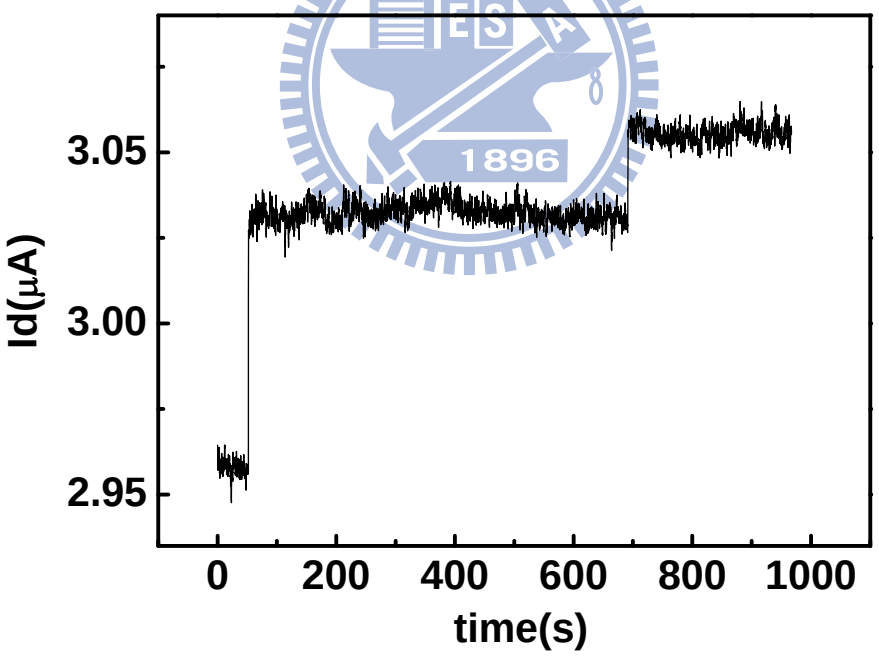


Fig. 3.7 (a) Measurement setup.

(b) Experiment result for charge vertical loss.

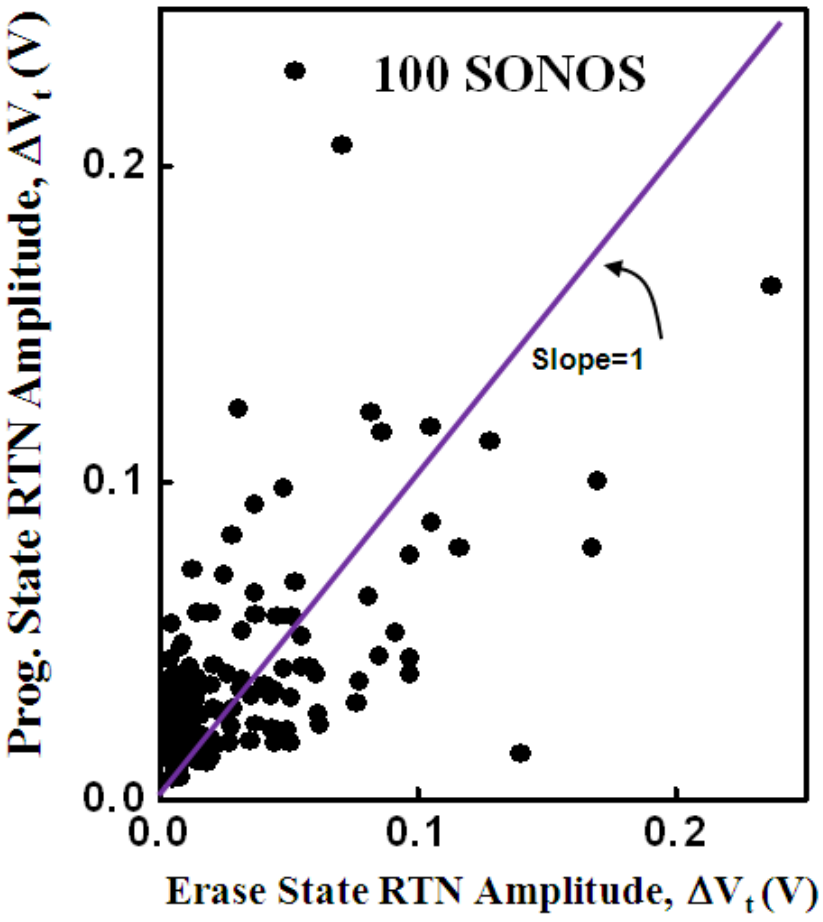


Fig. 3.8 Measured RTN amplitude in program/erase state in 100 SONOS cells.

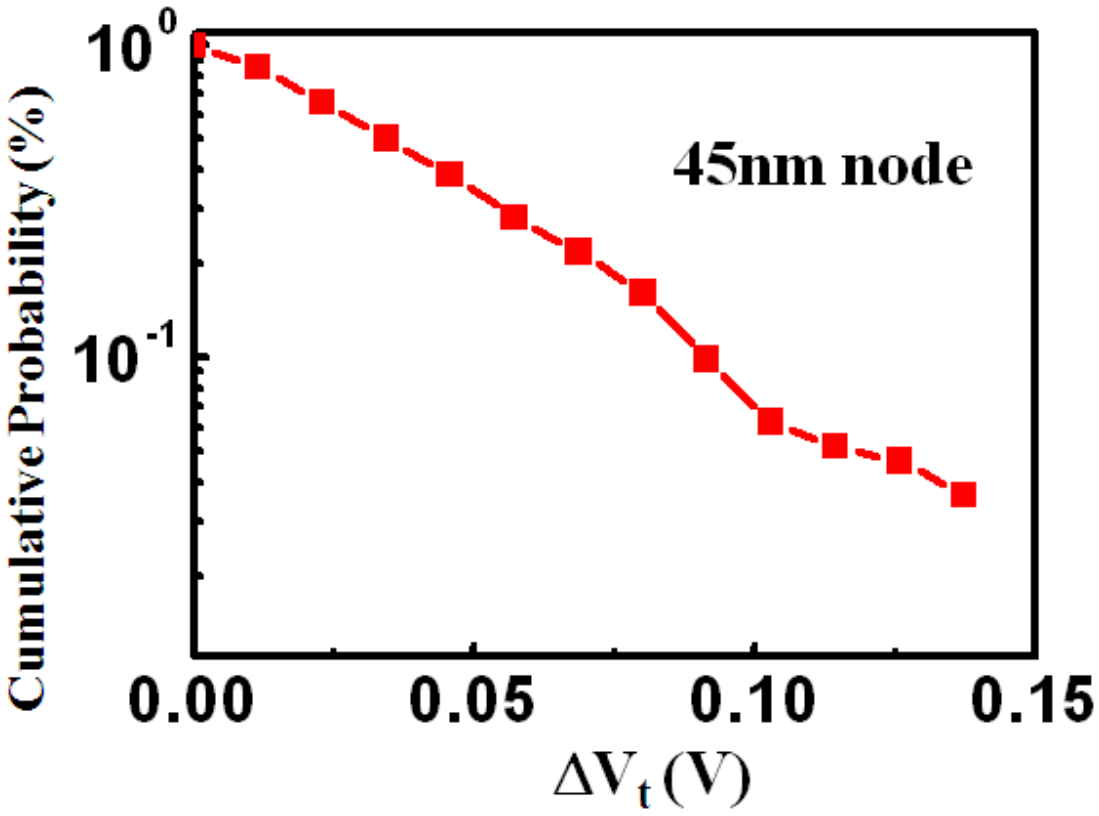


Fig3.9 Simulation of cumulative probability distribution of single-trap RTN induced Vt shift in 45nm node SONOS cells.

Fig. 3.10(a)

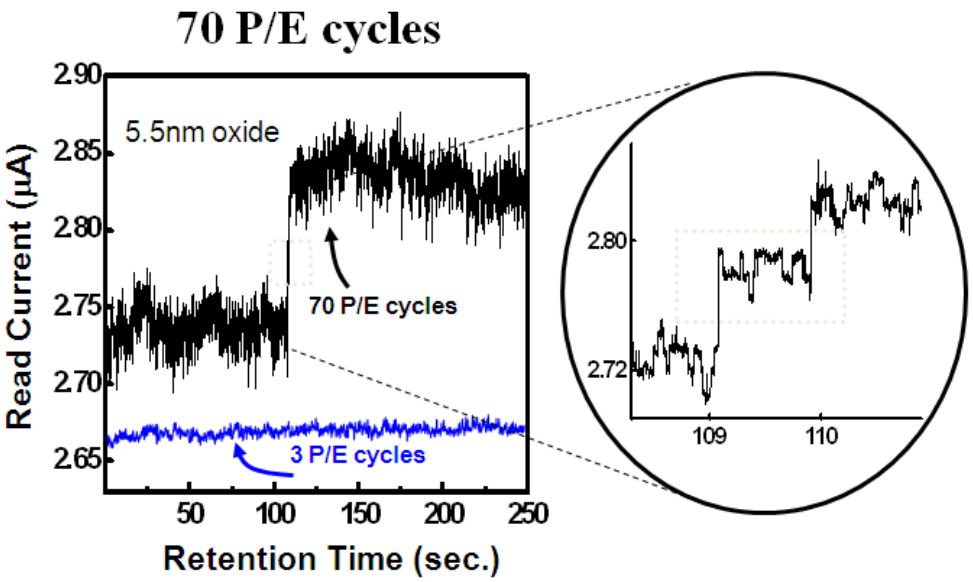


Fig. 3.10(b)

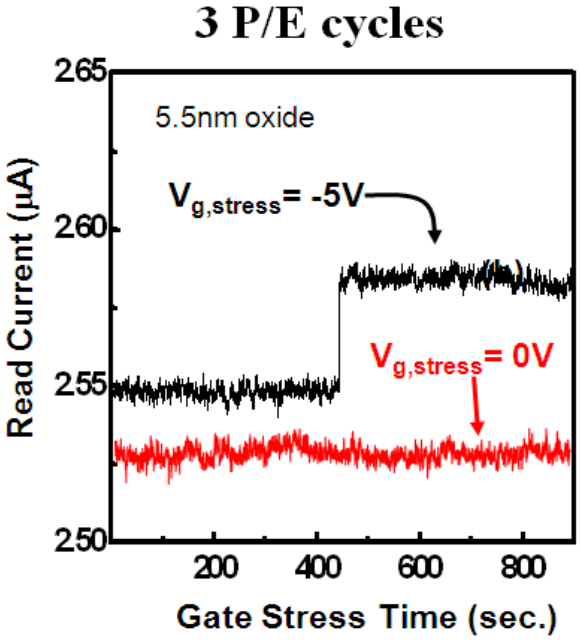


Fig. 3.10 Result of program charge loss in 5.5nm oxide SONOS.

(a) Measured after 3 and 70 P/E cycles.

(b)) Program charge loss behavior at different gate stress voltages.

Fig. 3.11(a)

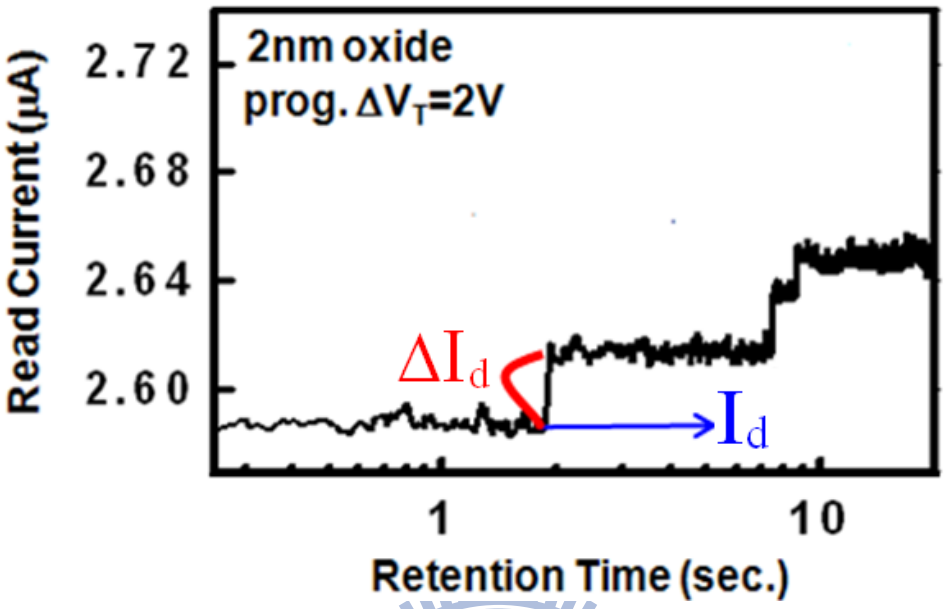


Fig. 3.11(b)

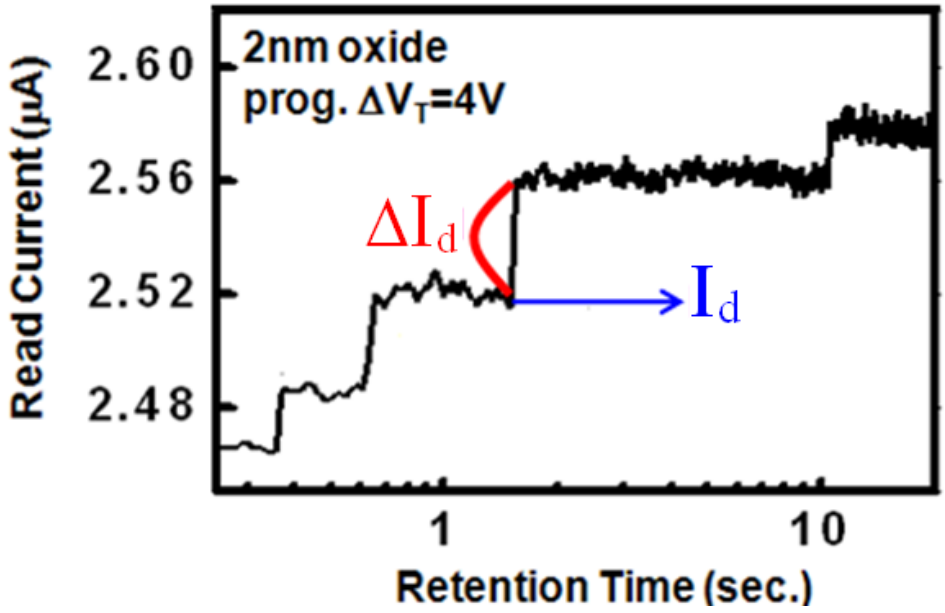


Fig. 3.11 Program charge loss in program window is (a) 2V (b) 4V

More charges escape for ΔVt=4V.

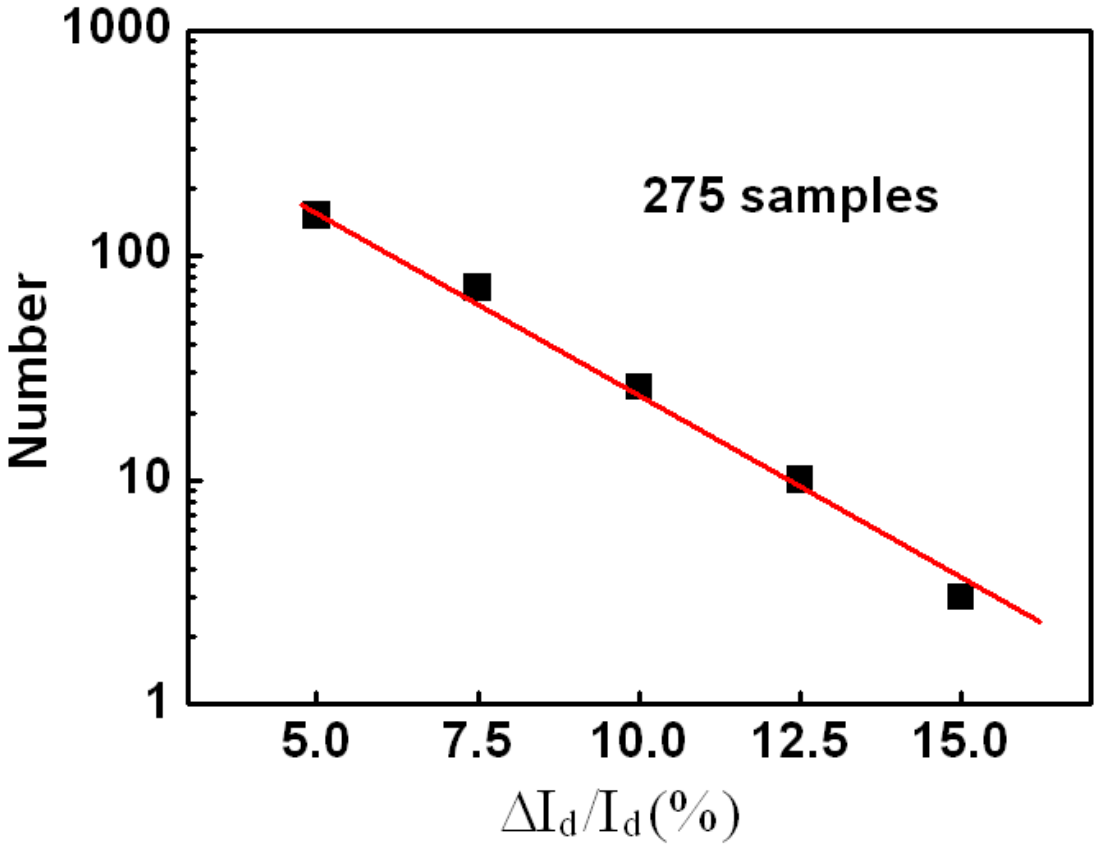


Fig. 3.12 Statistic of $\Delta I_d/I_d$ for 275 samples. A single program charge loss shows an exponential distribtion.

Chapter 4

Modeling of Retention V_t Distribution

4.1 Introduction

In the past few years, the number of electrons in each program level of a MLC cell reduces greatly as the scaling of the flash memory technology advances aggressively. A single charge loss may cause large variations in read current and have a chance to induce a read failure [4.1]. For this reason, we build a model to simulate the distribution of V_t retention loss.

Two assumptions are considered in our model: First, the ΔV_t distribution due to a single charge loss is exponential like in the case of RTN in SONOS cells. To verify this assumption is true, the simulation result of the ΔV_t distribution is represented. Second, in each device, the defect numbers is Poisson distributed. By this two assumptions, model of ΔV_t distribution can be build.

For further investigation, we perform bit-by-bit tracking in a 8MB SONOS array to characterize V_t retention loss at different retention times. Monte Carlo simulation is used to analyze V_t tail bits. The flow of Monte Carlo simulation is shown in the last section and the spread of V_t tail bits is inspected.

4.2 Modeling of Charge Retention Loss Distribution

In this section, a numerical to simulate a program charge loss V_t distribution is represented in Table.1, where σ is the standard variation, g(t) is V_t distribution immediately after program, h(t) is V_t distribution after retention, $P_\lambda(n)$ is the Poisson distribution and the symbol * represents a convolution integral. A 512MB SONOS flash memory is used to our simulation.

To confirm that a single charge loss V_t distribution is exponential distributed, we simulate the cumulative probability versus ΔV_t as shown in Fig. 4.1. From the result of simulation, probably function of a single charge loss induced ΔV_t (eq.(1) in Table.1) can be used in our model. Two different σ, 0.022V and 0.04V are chosen for our simulation. Eq.(1) in Table.1. is the probability function of a single charge loss induced ΔV_t. For two different σ are chosen, we can have two different curves of $f(\Delta V_t)$ as shown in Fig. 4.2(a). As σ is larger, the slope of the curve is smaller, which is consistent with the probability function. Next step, we simulate g(t), which is the V_t distribution immediately after program. The schematic diagram is represented in Fig. 4.2(b).

Since $f(\Delta V_t)$ and g(t) are simulated, the convolution of $f(\Delta V_t)$ and g(t) is calculated. The formula of convolution is shown in Table.1. The convolution result of $f(\Delta V_t)$ and g(t) is the new distribution by losing a charge from the previous program V_t distribution. $f(\Delta V_{t1})$ indicates the distribution of losing the first charge, $f(\Delta V_{t2})$ indicates the distribution of losing the second charge…etc. Therefore, we can have the new distribution of one charge loss by calculating the convolution of $f(\Delta V_{t1})$ and g(t).

From the second assumption described in section 4.1, the defect numbers in each cell is Poisson distributed, we can use Poisson distribution, $P_\lambda(n)$, to calculate the distribution of charge loss numbers, where λ is an average number of program charge lost in cell during retention and n is the number of charge loss. For example, $P_{0.2}(1)$ means the probability of losing a charge in a cell with average charge loss is 0.2. Since we would like to inspect charge loss under low P/E cycles condition, λ must be a small value. In our simulation, we choose λ=0.1, which is reasonable for low P/E cycles cells. Besides, when the P/E cycles number is not large, most cells must remain their V_t distributions unchanged, i.e., no charge loss for most cells. Some cells would lose a charge, and few cells would lose more than one charge. $P_{0.1}(0)=0.9048$ and

$P_{0.1}(1)=0.0905$ are calculated, which is confirmed to our description.

At last, we combine the Poisson distribution $P_{0.1}(n)$ and the convolution of $f(\Delta V_{t1})$ and g(t), as shown in eq.(2) in Table.1, the V_t distribution after retention, h(t) can be simulated, the result is represented in Fig. 4.3. In Fig. 4.3, as σ increases, the fluctuation of program V_t distribution becomes larger. As we know, σ is dependent on the area of device, i.e., for smaller device area, σ is larger, therefore, smaller MLC cells may have more chances to get read failure compared to larger ones.

4.3 Monte Carlo Analysis of V_t Tail Bits

The model of charge loss distribution is built in section 4.2. In this section, further investigation of the V_t tail bits spread is described by a Monte Carlo analysis. The procedure of Monte Carlo is shown in Fig. 4.4.

First, for a σ, for example σ=0.022V, and a main distribution g(t), an initial V_{to} is generated randomly based on g(t). Then, number of program charges lost is generated randomly from the Poisson distribution. Next, randomly generating ΔV_{t1}, ΔV_{t2}, ΔV_{t3}…etc. based on $f(\Delta V_t)$. After the three steps described above is done, the final V_t can be calculated by the difference between the initial V_{t0} and the summation of ΔV_t, i.e., $V_t=V_{t0} - (\Delta V_{t1}+\Delta V_{t2}…..)$. By this Monte Carlo analysis, the spread of V_t tails can be investigated. 100 Monte Carlo simulations for two σ (=0.022V and 0.4V) are shown in Fig. 4.5. As we can see in Fig. 4.5, although the distribution of tail bits spread in both σ=0.022V and 0.04V, all values of (V_t –PV) tail bits in σ=0.04V is larger than in σ=0.022V. In addition, for σ=0.04V, the largest simulated V_t shift exceeds 0.5V, which is due to a single program charge loss. A read error may be caused by the large V_t tail in a MLC SONOS memory and requires the use of an error code correction (ECC) technique.

(i) Probability function of a single charge loss induced ΔV_t

$$f(\Delta V_t)=\frac{1}{\sigma}\exp(-\frac{\Delta V_t}{\sigma}) \quad (1)$$

(ii) Vt distribution immediately after program, $g(V_t)$

(iii) Vt distribution after retention, $h(V_t)$

$$h(V_t)= \underbrace{P_\lambda(0)g(V_t)}_{\text{no charge loss}} + \underbrace{P_\lambda(1)f(\Delta V_{t1})*g(V_t)}_{\text{one-charge loss}} \quad (2)$$

$$+ \underbrace{P_\lambda(2)f(\Delta V_{t2})*(f(\Delta V_{t1})*g(V_t))}_{\text{two-charge loss}} + \cdots\cdots$$

where $P_\lambda(n)=\frac{e^{-\lambda}\lambda^n}{n!}$ is the Poisson distribution and

$$f(\Delta V_{t1})*g(V_t)\equiv\int f(\Delta V_{t1})g(V_t+\Delta V_{t1})d\Delta V_{t1}$$

Table 1. A numerical model of program charge loss induced Vt distribution.

A random program charge induced percolation effect is taken into account.

λ is an average number of program charges lost during retention in a cell.

The symbol * represents a convolution integral.

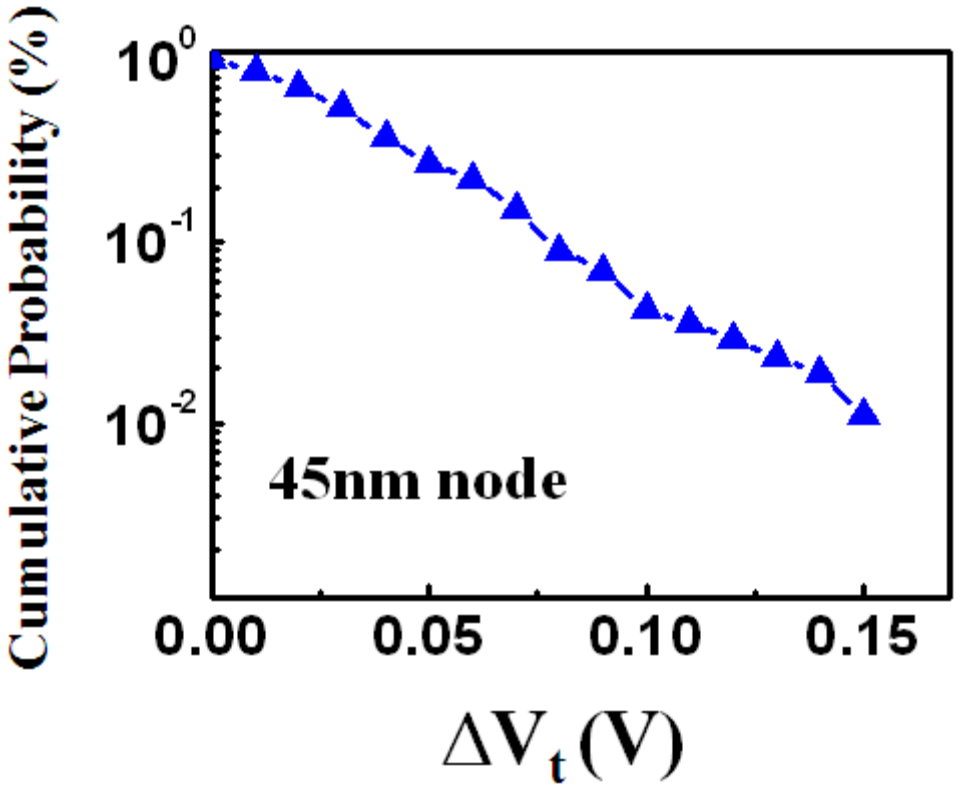


Fig. 4.1 Simulation of cumulative probability distribution of a single charge loss induced Vt shift in 45nm node.

Fig. 4.2(a)

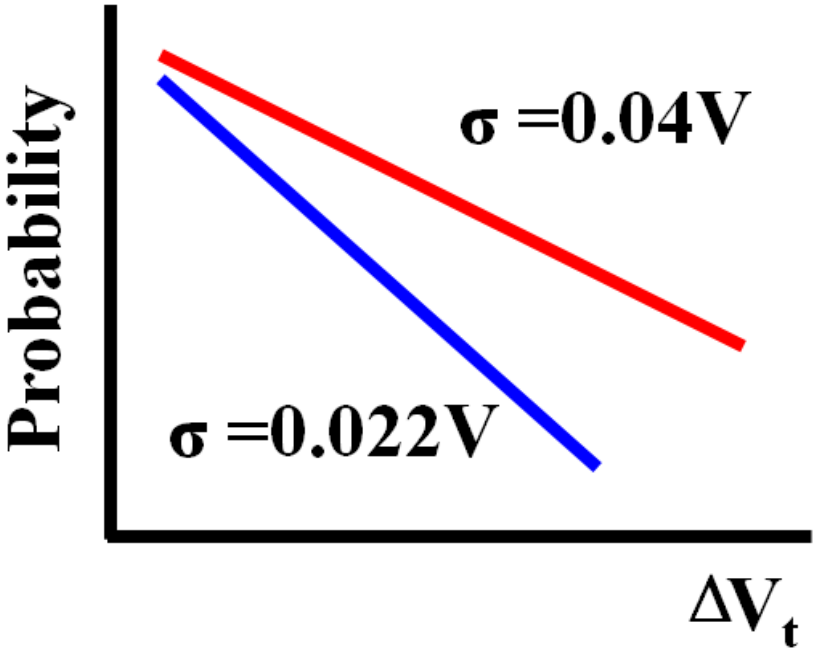


Fig. 4.2(b)

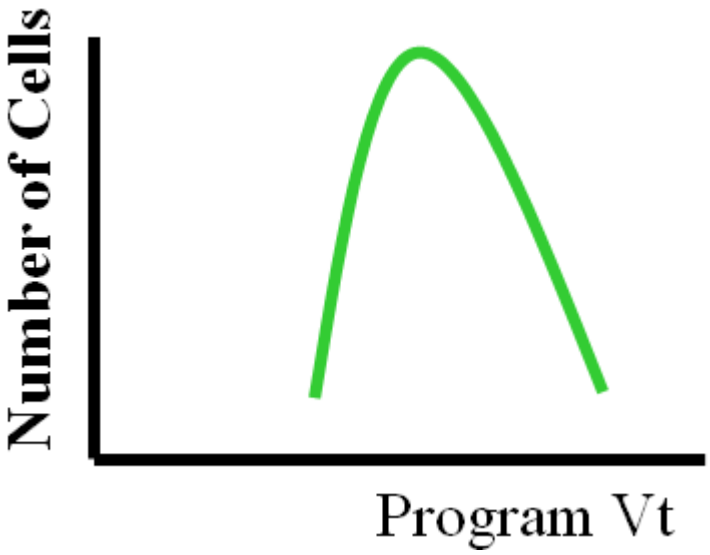


Fig. 4.2 (a) Probability function $f(\Delta V_t)$ for two σ, 0.022V and 0.04V.

(b) Schematic diagram for V_t distribution after program.

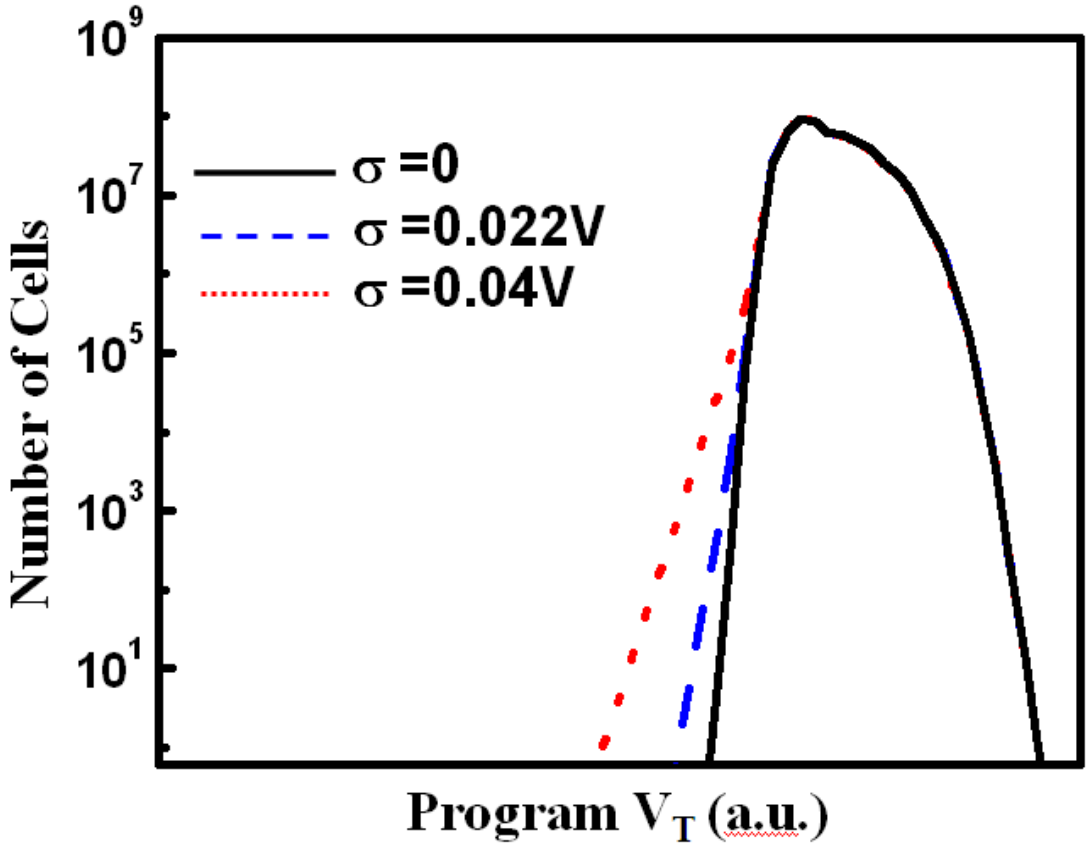


Fig. 4.3 Simulation result of Vt distribution after retention.

σ=0.022V and σ=0.04V are used in simulation with λ=0.1.

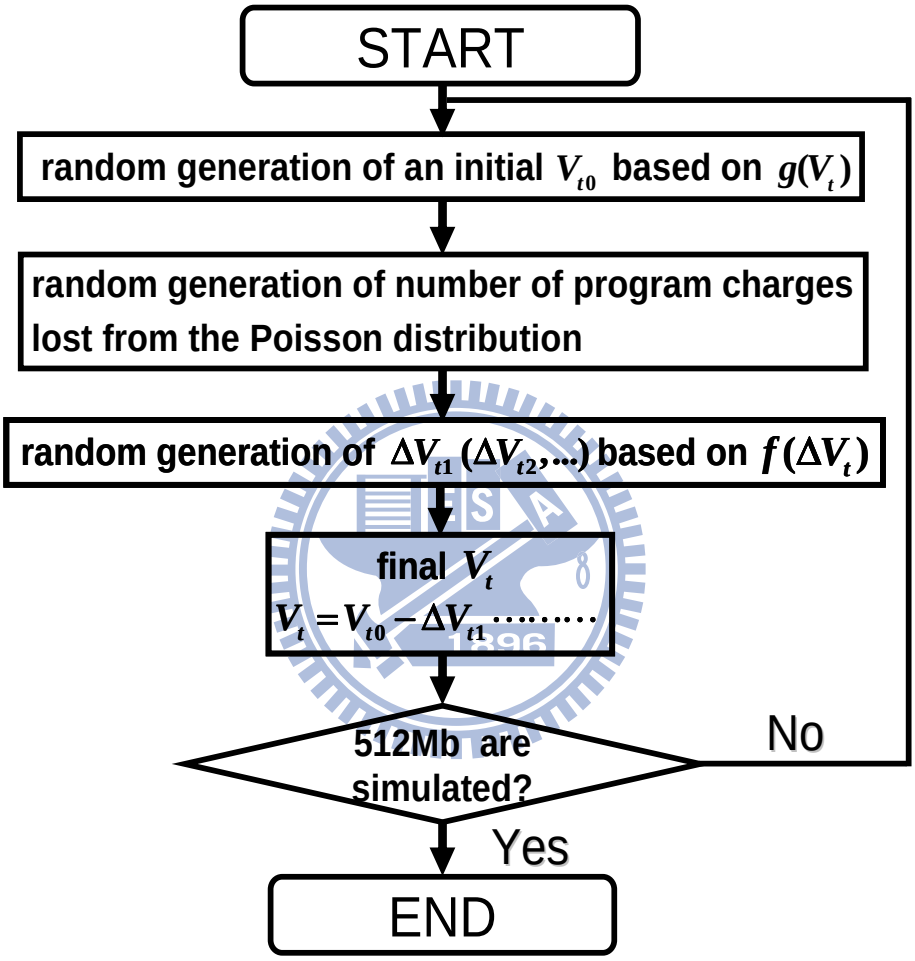


Fig. 4.4 Flow chart of Monte Carlo simulation for Vt retention tail bits.

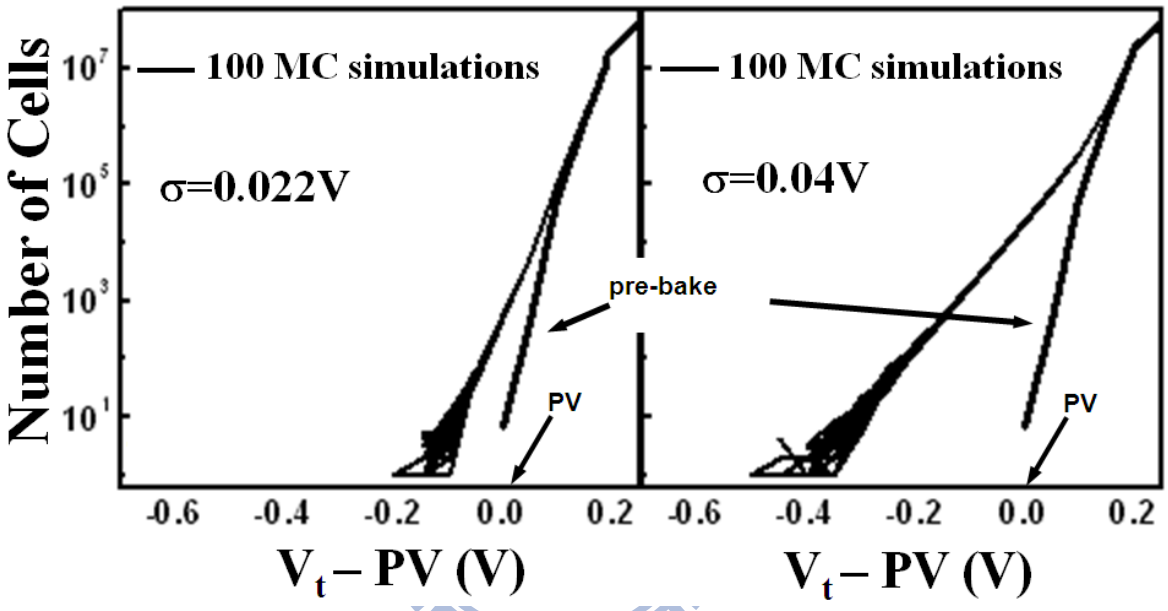


Fig. 4.5 100 Monte Carlo simulations of Vt retention tail bits in a 512Mb SONOS memory for σ=0.022V and σ=0.04V are performed, respectively.

PV denotes a “program verify” voltage.

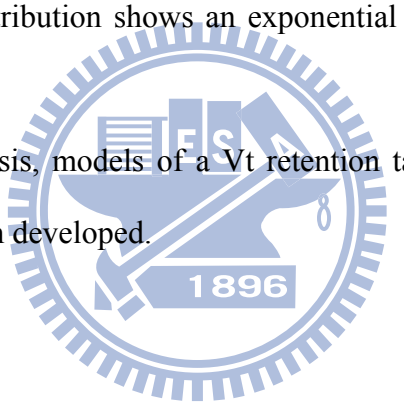
Chapter 5

Conclusion

A novel RTS method has demonstrated in this thesis to characterize program charge lateral profile in a SONOS flash memory without knowing a doping profile. The RTS method can provide a better solution than a charge pumping method or an inverse I-V modeling approach. CHE program electrons lateral distribution is observed by RTS method.

Program charge retention loss is considered to vertical charge loss. The statistic of a single charge loss distribution shows an exponential distribution as percolation effect.

At the end of this thesis, models of a Vt retention tail taking into account the percolation effect have been developed.



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Chapter 4

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碩士論文題目:

單一電子在 SONOS 快閃式記憶體中的現象，物理以及特性研究

Single Charge Phenomena, Characterizations and Physics