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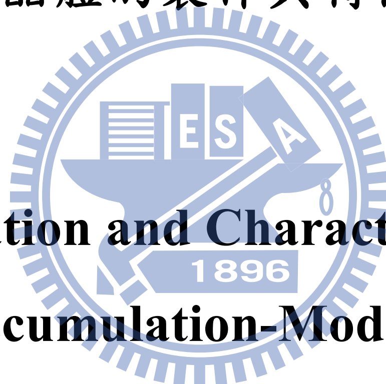
碩 士 論 文

具獨立雙閘極之 P 型聚集模式多晶矽奈米線電晶體的製作與特性分析



Fabrication and Characterization of P-Type Accumulation-Mode Independent Double-Gated Poly-Si Nanowire Transistors

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中 華 民 國 一 百 年 三 月

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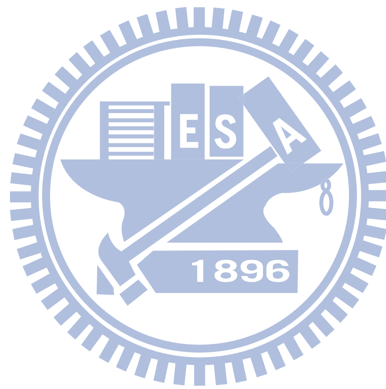
摘要

在本篇論文中，我們成功製作出操作在聚集模式(accumulation mode, AcM)下，具獨立雙閘極之 P 型多晶矽奈米線電晶體。此元件在通道中擁有高濃度的摻雜，且由於具有極小的奈米線尺寸，因此閘極可以有效的控制並開關元件。另外，此種元件的電性表現，包含基本特性以及次臨界特性，都將與操作在加強模式(inversion mode, IM)下，具有無摻雜通道的傳統元件做個比較。

在整個多晶矽通道導通的情況下， AcM 元件明顯具有較 IM 元件大的電流驅動力。此外，在兩個獨立閘極所提供多元操作的彈性下，我們將這兩種元件間不同的傳導機制成功地做區隔，並利用 TCAD 的模擬結果來做驗證。其次，由於 AcM 元件所提供的表面空乏區使得實質閘極介電層厚度的增加，因此具有較差的短通道效應。另一方面，我們也將討論元件跨導的特性，並利用其結果探索閘極耦合

效應對兩種元件的影響。最後，我們也發現在同樣的閘極驅動下，AcM 元件在閘極氧化層與通道的接面上具有較小的垂直電場，且由於 AcM 元件的實質通道涵蓋整個奈米線，使得載子受到表面粗糙與介面缺陷散射的影響較小，因此對於 AcM 元件而言，其跨導隨閘電壓增加而衰退的現象會比 IM 元件來得輕緩。



Fabrication and Characterization of P-Type Accumulation-Mode Independent Double-Gated Poly-Si Nanowire Transistors

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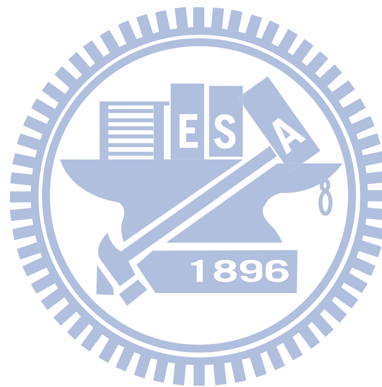
Abstract

In this thesis, we have successfully fabricated p-type accumulation-mode (AcM) independent double-gated poly-Si nanowire (NW) transistors which contain a high doping concentration in the channel and can be effectively turned off on account of the ultra-small feature size of NW. In addition, the electrical characteristics are well compared to the conventional devices with undoped channels which operate in the inversion mode (IM).

Owing to the current conduction through the whole channel, the I_{on} characteristics are obviously better for the AcM devices, so do the output characteristics. Moreover, due to the flexibility in device operation by the two independent gates, the differences of conduction mechanisms between the two types of devices can be clarified, and are also confirmed by the TCAD simulation

results. We also found that short channel effects (SCEs) are more severe for the AcM devices, which is ascribed to the additional effective oxide thickness (EOT) contributed by the surface depletion layer. The G_m characteristics are also characterized and compared between the two types of devices, from which the influences of gate coupling effect for each device are well discussed. On the other hand, the AcM devices have a smaller electric field at the interface at the same gate overdrive, and the carriers also inherently suffer less from the scattering of the surface roughness and the interface traps on account of the whole channel conduction. Thus, the G_m degradation with increasing gate overdrive is more severe for the IM devices.



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時光飛逝，很快的，碩士生涯即將告一段落，曾經傻呼呼的以為念研究所跟大學差不多，但自從進來實驗室後，才發現”研究”這兩字還真不是件容易的事。各種學習與挑戰讓我在這一年多也成長了不少，我了解到做研究跟大學寫寫報告有著天壤地別的差別，即便如今我即將要拿到了碩士文憑，但其實我知道，我離真正的做學問還是差了十萬八千里。但這些日子下來，我主要學到的東西並不是學術知識，而是做事情的態度，學習與研究就跟做人處事一樣，必須要誠實面對自己，挖掘自己的淺力並且勇敢面對問題，這些才是我這段日子下來最大的收穫。

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Chapter 1

Introduction

1.1 Overview of Multiple-Gated and Poly-Si Nanowires Transistors

Since the invention of the first transistor by John Bardeen and Walter Brattain in 1947, the revolution of semiconductor industry had spread up like a raging fire. The related applications have advanced the science and technology enormously and improved human's life in the same time. In order to achieve better electrical performance, many engineers strove to scale down the semiconductor device. They tried to increase the amount of transistors on a chip, expecting to enhance the electrical performance and reduce the cost of the integrated circuits. According to Moore's Law, the number of transistor on a chip doubles every 18 months. In the early stage of development which roughly followed the constant electric-field (CEF) scaling rules [1], the device scaling could smoothly follow the Moore's Law without facing too many fatal problems. Unfortunately, when devices scaled dimensions were approaching their physical limitations, many critical problems began to appear, such as short channel effect (SCE) [2], gate leakage current [3] and discrete dopants fluctuation [4], etc. As a result, new materials and/or modifications in device structure came into play in order to extend the Moore's law.

Recently, as device became increasingly difficult to scale down on account of these problems, many different types of device structure were constantly being

proposed, like multiple-gated field effect transistor (MuG-FET) [5]. These schemes can effectively reduce the impacts of bulk leakage encountered in planar devices, and is thus helpful in improving the control over the SCE. The concept of MuG-FET is extended to lots of novel device structures. A recent typical example is FINFET, which is basically a kind of double-gated device with a fin-like structure. While the planar silicon-on-insulator (SOI) [6] device is considered as a potential device structure in the future, these novel non-planar devices are also receiving considerable attentions in semiconductor industry.

In the meantime, many researches on poly-Si nanowire (NW) channel were invested [7-8]. NW is a one-dimensional structure with its cross-sectional feature size smaller than 100nm. As a result, the NW channel could confine the carriers and enhance their mobility due to its large surface-to-volume ratio. Although it is well known that the defects contained in the granular poly-Si films would aggravate the device characteristics, the adoption of NW structures could help alleviate the effects. Nowadays, the applications of poly-Si NW on thin film transistor (TFT) are seriously considered as an important topic for the future development of semiconductor industry.

For the past several years, more and more researches on the multiple-gate and poly-Si NWs have been presented. There have been many works reported on the fabrication and characterization of devices combining the multiple-gate and poly-Si NW channel [9], and the electrical performance not far behind that of planar CMOS was demonstrated. Due to the convenient and low-cost fabrication process, the devices are appealing for a number of applications like memory [10] and sensor [11].

1.2 Overview of Accumulation-Mode Devices

In essence, the operation principle of the accumulation-mode (AcM) device is similar to the junction field-effect transistor (JFET) [12-13] and the buried-channel MOS device [14-15]. All of them involve the body (or bulk) conduction mechanism, and the current path in the body is modulated by the depletion width controlled by the gate. For the JFET, it can solve the problem from the oxide-semiconductor interface, like the interface traps or the surface roughness scattering. However, the problem for JFET is that the gate-bias range is limited, because the junctions can't be biased beyond the flat-band voltage (V_{fb}), otherwise a high leakage current will flow to gate [16]. For the buried-channel MOS device, the surface doping can be of the type opposite to that of the bulk substrate doping. However, this type of device suffers from more severe SCEs than the surface-channel type, thus putting a serious hurdle in device scaling.

For the AcM device, unlike the inversion-mode (IM) device, the source/drain (S/D) and the channel are of the same doping type. To avoid excess bulk leakage current, such type of devices is mainly realized with SOI structure [17]. The operation mechanism of the AcM devices is quite different from that of the IM ones. With a sufficiently thin SOI, the body can be completely depleted by the applied gate bias to avoid the drain-to-source leakage current when device is turned off. With the shrinking of depletion width by decreasing the gate voltage (for p-channel), the cross-sectional area through which holes flow will continue to increase until the depletion regions vanish. For the AcM device, when it is turned on, the current conduction occurs through the whole channel layer rather than the surface. The body current density in the whole channel

region can be expressed as

$$J_{body} = q\, n\, \mu_b\, E \ , \qquad \text{(Eq. 1-1)}$$

where n is the average carrier concentration, μ_b is the effective carrier mobility, and E is the horizontal electric field. When the total body region is conducting, the cross-sectional area through which holes flow can be expressed as the total body cross-sectional area. By assuming the carrier concentration as the doping concentration and the horizontal electric field as the drain voltage divided by channel length, according to the model of the AcM device in [18], we can further derive the body current as

$$I_{body} = J_{body}\, A = q\, N_a\ \mu_b\, E\, W\, t_{Si} = q\, N_a\, \mu_b \frac{W}{L}\, t_{Si}\, V_d \ , \qquad \text{(Eq. 1-2)}$$

where N_a is the doping concentration, t_{Si} is the channel thickness and V_d is the drain voltage. For the body current, the whole channel acts just like an electrical resistance in relation to the doping concentration, the carrier effective mobility in the bulk and the device dimension. While continuing to reduce the gate voltage, the accumulation charges will be gradually induced and the current conduction on the surface will be added to the drain current. In the same time, the body current will tend to saturate and become independent of the gate voltage, which is also referred in [18].

For the AcM device, the most crucial issue is whether the device can be successfully turned off to evade the large drain-to-source leakage current. In this regard, the gate controllability should be enhanced by thinning the gate dielectric, or the channel thickness should be thin enough for the gate to effectively deplete the carriers. In the past, the relevant technology was not mature and hard to control precisely. The most effective method is to lower the doping concentration in the channel [19], in order to deplete the carriers easily

by the gate bias. In conclusion, on account of the many technical concerns, although several researches had dedicated to the AcM device, such as the analytical model [20] or the extraction method for threshold voltage [21], it was still rarely applied to the planar devices, except for the SOI devices. Recently, due to the rising of the non-planar devices with enhanced gate controllability on channel, many related researches on the AcM non-planar device have been presented, and more and more studies are devoted to this application [22].

1.3 Motivation

For non-planar devices like FinFET, it is becoming more difficult to achieve uniform S/D doping by using implantation on account of shadowing effects caused by tightened pitch with each technology node [23]. Meanwhile, S/D regions for the cell device contained in a high-density 3D memory technology such as BiCS [24] are formed by gate fringing fields from neighboring cells, which are hard to manipulate and may easily result in degradation of read current. In line with this, recently much attention has been paid to the device without junction [25]. In other words, S/D and channel have the same type of doping and the device operates in the AcM.

Our group previously introduced a poly-Si NW transistor with rectangular-shaped NW channels and two independent gates [26]. The two independently controllable gates allow higher flexibility in device operation and provide a unique insight into the conduction mechanism of the NW device. More than this, when the channel thickness is thin enough, the gate-coupling effect with the double gates could occur and enhance the gate controllability on the channel, improving the electrical characteristics like on-current and

subthreshold swing (SS) [27]. Because of these advantages, we tried to apply the double-gated configuration to the AcM device. In this study, we fabricated the p-type AcM double-gated device with a high doping concentration in the channel, expecting to obtain better electrical characteristics via the effective controllability by the double gates. A comparison in device characteristics between the devices with the conventional ones with undoped channels is also made in this study.

1.4 Organization of the Thesis

In Chapter 2, we present the fabrication of the p-type AcM double-gate TFT, and the basic process flow will be briefly described. The measurement setups are also presented in this chapter.

In Chapter 3, we present and discuss the electrical characteristics of the fabricated devices, which include the on-current, SS and SCE. The results of the two single-gated (SG) modes and the double-gated (DG) mode will be discussed respectively. Also, we compare the electrical characteristics with the conventional device.

Finally, we summarize the conclusion from our experimental results and suggest future work in Chapter 4.

Chapter 2

Device Fabrication and Measurement Setup

2.1 Device Fabrication and Process Flow

In this section, we introduce the basic process flow of the p-type AcM double-gated device. Figure 2.1 shows the schematic process flow of the proposed device. First, a 60 nm-thick SiN layer was deposited on a Si wafer capped with a 100 nm-thick thermal oxide. Because of the p-type doping of the channels, the AcM device prefers a gate material with a low work function such as n^+ polycrystalline silicon in order to achieve a suitable threshold voltage (V_{th}) (that is, not too positive for p-type device). Therefore, a 100 nm-thick *in-situ* doped n^+ poly-Si and 50 nm-thick SiN were deposited sequentially to serve as the 1st gate stack. After the gate stack patterning (Fig. 2.1(a)), a plasma etching with high selectivity to SiN was used for lateral etching of the n^+ poly-Si (Fig. 2.1(b)). Then 10 nm-thick TEOS oxide and 100 nm-thick amorphous Si were deposited, which subsequently underwent 600°C annealing in N_2 ambient for 24 hours (Fig. 2.1(c)). After P^+ doping using BF_2^+ at a dose of 5×10^{14} cm^{-2} (Fig. 2.1(d)), samples were annealed in nitrogen ambient at 900°C for 30 min to drive the dopants into the NW channels (Fig. 2.1(e)). To avoid large S/D resistance, an additional S/D doping was performed by implanting BF_2^+ at a dose of 5×10^{15} cm^{-2} (Fig. 2.1(f)). Next, the channel and S/D regions were defined by reactive plasma etching (Fig. 2.1(g)). The 2nd gate electrode comprising of 10 nm-thick TEOS oxide and 100

nm-thick *in-situ* doped n$^+$ poly-Si was then deposited followed by patterning (Fig. 2.1(h)). A 200 nm-thick oxide was subsequently deposited as passivation layer. The device was completed after standard metallization steps. For the IM device with undoped channels, the fabrication flow is similar to what was described above except that steps in Fig. 2.1(d) and Fig. 2.1(e) are omitted.

The layout of the double-gated device is shown in Fig. 2.2(a). Fig. 2.2(b) is a cross-sectional view of the device along line $\overline{ab}$ in Fig. 2.2(a). It can be seen that the 1st gate is surrounded by the SiN layers and two rectangular NW channels.

2.2 Images of Fabricated Devices

In Chapter 3 we will discuss the electrical characteristics of the fabricated devices including the AcM and the IM devices. However, for the AcM device, its fabrication contained additional channel implant and drive-in steps for driving the dopants into the NW channels, as shown in Fig. 2.1(d) and Fig. 2.1(e). Hence it is imperative to check the texture and grain size of the fabricated NW channels to see if there exists any physical difference between the two devices. Such information is useful for us to compare their electrical characteristics more objectively.

The cross-sectional transmission electron microscope (TEM) images for the fabricated devices are given in Fig. 2.3, from which the rectangular NW channels can be observed. It can be seen that the channel thickness is about 20nm for the IM device and 23nm for the AcM device. From these TEM images, it can be seen that the channel thicknesses for the two devices are roughly the same, though a little thicker for the AcM device.

Due to the high temperature drive-in steps for the AcM device, the grain

size in NW channels may become larger. However, prior to the above steps, the AcM device had undergone a 600°C annealing in N_2 ambient for 24 hours to transform the amorphous Si into polycrystalline state, and the grain size for the AcM device may not increase dramatically. This is conformed with the scanning electron microscope (SEM) images of the two types of poly-Si films shown in Figs. 2.4(a) and (b). As can be seen in the figures, the grain sizes for the poly-Si films are similar. Actually the grain size for the AcM device is even slightly smaller than that for the IM device. This phenomenon may be due to the diffusion of high doping concentration of BF_2^+ [28]. In conclusion, we can approximately regard the grain sizes for both devices as the same.

2.3 Measurement Setup

In our study, electrical measurements of all devices were evaluated by an HP4156A precision semiconductor parameter analyzer, and the measurement temperature was maintained at 25°C.

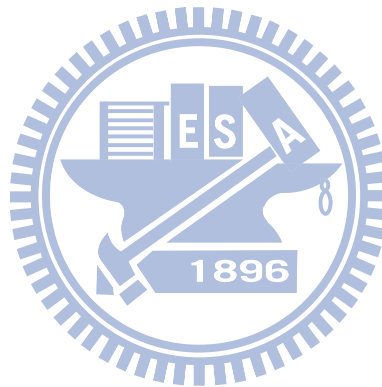
The basic electrical parameters of the fabricated device were extracted from the electrical characteristics. By the way, the V_{th} was not extrapolated from the I_d-V_g curves. Due to the contribution of body conduction for the AcM device, its operation is different from that of the IM device and the extrapolation technique could be inaccurate [29]. Instead, it is suitable to define the V_{th} for a fixed drain current level. The surface potential (Φ_S) criterion can be set to zero for the AcM device [30]. For our experiment, the V_{th} was defined as the value of V_g when I_d equals 10nA $\times \frac{W}{L}$ under V_d of 0.5V, where W and L are the channel width and the channel length, respectively. For the channel width W, the value was estimated from the TEM images shown in Figs. 2.3(a) and (b) for the IM and

AcM devices, respectively. The SS is calculated by the following equation:

$$SS = \frac{d\log(I_d)}{dV_g} , \qquad \text{(Eq. 2-1)}$$

and for both AcM and IM devices, the minimum value in the subthreshold swing is extracted. The transconductance (G_m) was also extracted from the I_d-V_g curves, and for on-current (I_{on}), the value was defined as the I_d when V_g–V_{th} = -3V.

For our double-gated structure, the operation modes of measurements are described as below: SG-1 and SG-2 modes denote the scheme when the 1st or 2nd gate serves as the driving gate while the other gate electrode is grounded. In DG mode, both gates are connected together to serve as the driving gate.



Chapter 3

Results and Discussion

3.1 Basic Electrical Characteristics

3.1.1 Transfer Curves

Figure 3.1 shows the transfer curves of an IM device. Due to the existence of un-gated regions which contribute extra parasitic resistances in the SG-1 mode [31], the electrical performance of the SG-1 mode is basically worse than that of the SG-2 mode. For the IM devices, the drain current conducts when the inversion layer is formed near the interface between the channel and gate dielectric. From the plot, we can see the drain currents in the three operation modes rise up at almost the same gate voltage. From the TEM images in Chapter 2, the channel thickness for our fabricated device is quite thin (down to about 20nm), and hence the gate coupling effect [32] is pretty strong so that the gate controllability and electrical performance are obviously enhanced in the DG mode [26]. As is evident in the current-drive of a single device, the I_{on} of the DG mode is larger than the sum of those of the two SG modes. Also, owing to the effect of volume-inversion on account of the thin channel thickness [33], the SS under the DG mode is better than that in the SG mode.

The transfer curves of the AcM device are given in Fig. 3.2. There are some differences in electrical characteristics from those of the IM device. First, it can be seen that the curves of the AcM device apparently shift to the right (more positive value of V_{th}), showing the normally-on characteristics. Moreover, due to

the different conduction mechanisms for the AcM devices [34], the characteristics of I_d-V_g curves are different from those of the IM devices. In the AcM case, the key point is whether the device can be effectively turned off. When the AcM device is turned on, the channel flowed through by the carriers contained in the accumulation region at the surface and the quasi-neutral region in the film center. On the other hand, for the PMOS devices, if the gate bias isn't sufficiently positive to deplete the free holes in the channel, a high leakage current will flow and the device cannot be effectively turned off. Thanks to the ultra-thin channel thickness in our fabricated devices, the AcM device can still be successfully turned off in all operation modes despite the very high channel doping (>10^{18}/cm^{-3}). Moreover, for the 0.7µm channel length, the drain-to-source leakage current in each operation modes is significantly larger than that for the device with 2µm channel length. It may be due the severe SCE and the large bulk leakage current for the AcM devices, which will be discussed in the next section.

For the AcM devices, the gate coupling effect is also obvious under the DG mode. However, its influence is quite different from that of the IM device. For the DG mode, the two gates are simultaneously used to deplete the channel and can therefore more effectively turn off the device, leading to a smaller SS and a smaller V_{th}.

Figure 3.3 shows the threshold voltage (V_{th}) of the three operation modes for the two types of devices with 0.7µm channel length. For the IM devices, the conduction is through inversion carriers induced near the channel interface by the gate bias. The V_{th} is more positive for the DG mode than the SG-2 mode and SG-1 mode, indicating the IM device can be more effectively switched with the switching mode [27]. However, for the AcM device, the device is normally on and its switching depends on the ability of depleting the carriers in the body. As

shown in Fig. 3.3, the order in the magnitude of V_{th} among various modes for the AcM device is opposite to that of the IM one, and the V_{th} of the DG mode, which has the strongest gate controllability over the channel, is the smallest. This is reasonable since the DG mode depletes the channel from the two opposite channel interfaces and the two depletion regions would merge at around the center of the channel as the device is turned off. For the SG modes, the depletion starts from only one of the two channel interfaces where the driving bias is applied and it needs to deplete the whole channel for effectively switching off the device, thus the SS is worse while the V_{th} is larger.

Figure 3.4 shows the I_{on} characteristics as a function of channel length for both devices. In the AcM devices, the carriers flow through the whole channel, thus their current level is significantly larger than that of the IM ones in which the conduction is mainly through the channel interface. For the two types of devices, the current of SG-1 mode is smaller than that of SG-2 mode. As explained in [31], the current path of the SG-1 mode contains un-gated regions, as shown in Fig. 3.5, which drastically increase the series resistance. Regarding this problem which leads to the degraded performance, the I_{on} of the SG-1 mode is obviously lower than that of the SG-2 mode for the IM devices, and under the DG mode, the I_{on} is almost dominated by that of the SG-2 mode. This issue is slightly ameliorated when adopting the AcM scheme, and due to the high doping concentration in the channel, impact of the un-gated regions is relieved, as evidenced by the smaller difference in I_{on} between the two SG modes.

3.1.2 Output Characteristics

Figure 3.6 shows the output characteristics for both devices. For the AcM devices, the current conduction occurs through the whole channel layer rather

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than the surface, and it is apparent that the output current is enhanced significantly for the AcM devices, which can provide about 328% enhancement of saturation current at V_g-V_{th} = -4V and V_D = -5V for the 2μm channel length, and 198% enhancement for the 0.7μm channel length over the IM devices.

The S/D resistance can be extracted from the I_d-V_g curves in Fig. 3.6 by using the linear regression method. Fig. 3.7 shows the total resistance (R_{tot}, = $\frac{V_d}{I_d}$) as a function of channel length. The S/D resistance can be extracted from the intercept of y-axis of the plots. Because we had performed an extra implantation on the AcM devices to reduce the S/D resistance [35], the extracted S/D resistances are almost the same for the two devices. The value of the AcM devices is about 12.4kΩ, just a little smaller than 13.8kΩ of the IM devices, presumably due to the lower-resistivity path in the AcM device between the channel and the S/D as explained in [36]. The channel resistance can be obtained by extracting the S/D resistance from the R_{tot}, and the results for both devices are shown in Fig. 3.8. Due to the high channel doping for the AcM devices, the channel resistance is much smaller than that for the IM devices with undoped channel. For the long channel length, the difference of channel resistance between the two devices is more obvious, and the difference diminishes with decreasing channel length. The outcome is consistent with the results shown in Fig. 3.6 that the enhancement of the output characteristics is more prominent for the long-channel device.

3.1.3 Simulation Results

Here we use the TCAD simulation to analyze the differences in conduction mechanisms between the two types of devices in the subthreshold region. The simulated structures have a uniform doping concentration in the channel and S/D regions for the AcM devices. The channel has boron doping at a

concentration of 5 × 10^{18} cm^{-3}, and the channel thickness is 20nm while the gate oxide thickness is 10nm. The work function of gate electrode is 4.15eV, and here we ignore the quantum effect to simplify the condition. The V_{th} is defined as the value of V_g when I_d equals 10nA. Figure 3.9 shows the simulation results along the channel depth for the IM devices. As the absolute value of gate overdrive increases in Fig 3.9(a), the energy bands near the interfaces gradually bend and invert the surface region. Then we can see from Fig. 3.9(b) that the concentration of the inverted holes induced near the two interfaces increases with increasing gate overdrive.

The simulation results for the AcM device are shown in Fig. 3.10. In Fig 3.10(a), when the absolute value of gate overdrive increases, the surface bend bending is relieved while the width of a flat-band region (zero electric field) in the central Si channel increases with increasing gate overdrive. It can be noted from Fig. 3.10(b) that the carriers are concentrated at the center of the Si bulk [37]. Unlike the IM device whose channel body is nearly depleted when the device is turned on, the quasi-neutral region of the AcM device gradually expands from the channel center to the interfaces with increasing gate overdrive.

In conclusion, from the simulation results, we can define the differences of conduction mechanisms between the two devices. For the IM devices, the conduction carriers are from the surface charges induced by the gate bias, and for the AcM devices with doped channel, the conduction is mainly through the center of the Si bulk opened by the gate bias.

3.2 Subthreshold Characteristics

3.2.1 Short Channel Effects

The SS characteristics as a function of channel length for both devices are given in Fig. 3.11. For the AcM devices, both SG modes start to exhibit obvious rise in SS when the channel length is smaller than 1μm. Such phenomenon is relaxed with the DG mode, indicating it has the highest immunity to SCEs among the three modes. Moreover, it is interesting to note that when the channel length is larger than 1μm, the SS in the DG mode for the AcM devices is better than that for the IM ones. However, the overall SS degradation with decreasing channel length is still more severe for the AcM devices. The V_{th} as a function of channel length is given in Fig. 3.12. It can be seen that the values of V_{th} for the AcM devices are all positive, exhibiting the feature of normally-on transistor. However, for the AcM devices, the V_{th} roll-off is still more severe, and, with channel length of 0.4μm, V_{th} as high as 2.3V is recorded.

As mentioned above, both SS degradation and V_{th} roll-off are severer for the AcM devices, which seem to have worse SCEs than the IM devices, and such phenomenon can be explained from the perspective of the difference in effective oxide thickness (EOT) between the two types of devices. Fig. 3.13 is the schematic illustration of current paths under DG mode of operation for the two types of devices. For the IM devices, the current is mainly conducted along the inversion layer induced near the interfaces and the EOT is approximately equal to the physical oxide thickness. However, for the AcM devices, because the current path in the subthreshold region is mainly along the central Si channel, the physical distance between the gate and the channel is larger than the case of the IM. In other words, there is an additional gate dielectric contributed by the Si depletion layer, resulting in an increase in the EOT of the devices. Moreover, this additional gate dielectric layer not only exhibits in the AcM devices, but also depends on the gate bias. Here we use the TCAD simulation to explain such

situation for the AcM devices with the simulated structures described in the last section, and we use the SG mode to demonstrate in the following simulation.

Figure 3.14 shows the simulation results of the hole density along the channel depth with varying gate overdrive for the AcM device. Gate overdrive conditions used in the simulation for the PMOS device is when the device is turned on, or when the gate voltage is more negative than the V_{th}. It is seen that the peak of carrier concentration is moving toward the interface with increasing gate overdrive. Figure 3.15 demonstrates such a trend that the EOT for the AcM devices will change with varying gate bias. Here we define the thickness of the surface Si depletion layer as the average location of the holes with respective to the channel surface, as shown in Fig. 3.16, which can be calculated with the formula given in the figure. We can then quantitatively acquire the contribution of the Si depletion layer to the EOT with the results shown in Fig. 3.17. It can be seen that the additional EOT contributed by the depleted Si channel increases with increasing gate bias. (Note: for PMOS, the increase in gate voltage means the device is turning off). Moreover, the value saturates at around 3.8 nm as the V_g-V_{th} reaches 2.4V. As a result, for the AcM devices, the EOT is strongly dependent on the gate bias condition and gradually increases when the device is turned off, explaining the worse SCEs as compared with the IM ones. Such situation can be improved with the DG mode of operation in which the depletion of the channel originating from the two opposite channel surfaces and the EOT contributed by the Si depletion layer can be reduced. This is evidenced with the SS improvement and less SS degradation of the DG mode over the SG modes in Fig. 3.11(b), which is more significant than the effects DG-mode makes for the IM ones shown in Fig. 3.11(a). .

In conclusion, SCEs is more severe for the AcM devices due to the larger

EOT, but the DG mode is still strongly immune to it in terms of the substantially better performance over the SG modes, especially for the short-channel devices.

3.2.2 Variation of Electrical Parameters

Figure 3.18 shows the SS characteristics of the two types of devices under the three operation modes. The results were measured from 10 devices with channel length of 1μm. First, for the AcM devices, the SS fluctuation of the SG modes is quite large while the DG mode exhibits relatively smaller one. In contrast with this observation, the IM devices exhibit much smaller SS fluctuation for all operation modes.

Here we also perform simulation to analyze and discuss such a phenomenon. Figures 3.19(a) and (b) show the simulation results of the V_{th} and SS, respectively, as a function of channel thickness for both IM and AcM devices operated in the SG mode. It can be seen that, for the AcM devices, the electrical parameters are more sensitive to the channel thickness or the channel doping concentration than those for the IM devices. Actually, such phenomenon has been reported in previous researches [38-39]. According to [39], since the built-in potential between the S/D and channel is lower for the AcM devices than for the IM ones, depletion of the carriers in the center region by the gate biasing is necessary in order to shut the off-state leakage current. However, the higher channel doping concentration gives the shorter depletion width, which results in lower gate controllability at the center of the channel. As a result, the gate controllability is more sensitive to the channel thickness for the AcM devices, and also to the channel doping concentration which will affect the depletion width.

Here we can find out the root cause of such a phenomenon more quantitatively. For the IM devices, the relationship between V_{th}, channel

thickness and channel doping concentration is analytically given by [40]

$$\Delta V_{th} = \frac{q \cdot N_{body} \cdot T_{Si}}{C_{ox}} , \qquad \text{(Eq. 3-1)}$$

where N_{body} is the channel doping concentration, T_{Si} is the channel thickness, and C_{ox} is the oxide capacitance. From this equation, a larger fluctuation can be expected for the AcM devices which have much higher channel doping and thicker EOT. Figures 3.20(a) and (b) show the simulation results of the hole density along the channel depth at V_g=V_{th} for devices with different channel thicknesses and channel doping concentrations, respectively. It is obvious that the Si depletion layer between the conductive channel and the gate oxide of the driving gate is becoming larger with increasing channel thickness or the channel doping concentrations, which results in a larger EOT and smaller C_{ox} for the AcM devices. Such trends would worsen the fluctuation issues and well explain the above experimental results.

Back to the plot of Fig. 3.18(b), for the AcM devices operated under the DG mode, the two gates only need to control a half of the channel thickness which is much thinner as compared to that in the SG mode. The EOT turns out to be thinner and thus the high SS fluctuation described above for the SG mode can be reduced with the DG mode. Convincing data are given in Figs. 3.18(a) and (b).

Based on the above results and analysis we can also infer that the bias condition applied to the back gate may also affect the device characteristics. We can use the schemes shown in Fig. 3.21 to help understand the consequence. In this figure, the two depletion regions, i.e., front (driving)-gate and back-gate sides, in devices operated under the SG mode at V_g=V_{th} with different bias applied to the back gate are illustrated. Since V_{th} is defined as the gate voltage when the drain current is constant (=10nA), thickness of the conductive region in

the channel should be roughly a constant. This means that the back-gate bias may also affect the thickness of channel depletion region of the driving-gate side. As can be seen in the figure that a more positive back-gate bias tends to widen the channel depletion region of the back-gate side, and thus shrink that of the front-gate side. This will reduce the EOT of the device during operation, and thus a reduction in the fluctuation of device characteristics is expected. Conversely, a more negative back-gate bias will worsen the fluctuation issue. Figure 3.22(a) shows the V_{th}-vs.-SS characteristics measured from 20 devices with L= 2μm under the SG-2 mode. In the figure, 1st gate serves as the back-gate and three biases, namely. -1.5, 0, and 1,5V, are applied. Figure 3.22(b) shows the distribution of measured SS versus G1 bias. Clearly the above inference is confirmed with the measured results. Such dependence is not obvious for the IM devices with the data shown in Fig. 3.23. Fig. 3.24 shows the simulated V_{th} of the AcM devices as a function of channel thickness and back-gate bias under the SG mode. It is seen that the dependence on channel thickness is reduced as the back-gate bias increases (or becomes more positive). This well explains and is consistent with the data shown above.

3.3 Transconductance Characteristics

3.3.1 Gate Coupling Effects

Figure 3.25 shows the ratio of transconductance (G_m) under the DG mode to the sum of G_m of the two SG modes for the two types of devices. The phenomenon of gate coupling effects can be observed when the channel thickness is thin enough. There are some differences between the two types of devices, and we'll discuss its influences respectively.

For the IM devices, in general, mobility enhancement can be observed and is attributed to the gate coupling effect which would lead to the occurrence of volume-inversion [41]. In the weak inversion, when the channel thickness is thin enough, the surface band bending at the two sides of the channel would couple with each other under the DG mode, and the whole Si channel could be totally inverted, which is called the volume-inversion [42]. At this moment, the carrier distribution peaks at the center of the poly-Si film where the primary conductive channel is located. As a result, the current-drive is dominated by these minority carriers, which are less confined at the interfaces and won't suffer from serious surface roughness scattering and the interface states as compared with the cases of the SG mode [32]. The advantage of such effect is shown in the experimental difference in G_m between the SG mode and DG mode (exceeding a factor of 2), and this enhancement is primarily related to the increase in carrier mobility. In Fig. 3.25 we can see that, for the IM device, the peak value of G_m ratio is almost up to 1.5. In the DG mode, as the gate overdrive increases the carrier distribution moves gradually closer to the two interfaces and the situation becomes more like the SG modes. This explains why the G_m ratio is close to unity with increasing gate overdrive, which is the theoretical value if the gate coupling effect doesn't exist.

However, for the AcM devices, the influence of the gate coupling effect is different from the IM devices. Specifically, when the AcM device is turned on, most of the Si channel is in quasi-neutral condition. The current-drive is mainly conducted through the whole channel for both SG and DG modes, thus the mobility enhancement mentioned above is not obvious here. Here we extract the values of potential barrier height to confirm such mechanisms. According to the Levinson's mode based on the thermionic field conduction model [43], the

channel mobility μ_{eff} can be divided into the intragrain mobility μ_G and the mobility at the grain boundary ($qv_cL_g/kT \cdot \exp[-E_b/kT]$). Thus the μ_{eff} can be expressed as

$$\mu_{eff}{}^{-1} = \mu_G{}^{-1} + \left[q\frac{v_cL_g}{kT}\exp\left(\frac{-E_b}{kT}\right)\right]^{-1} , \qquad \text{(Eq. 3-2)}$$

where v_c is the collection velocity, L_g is the grain size and E_b is the potential barrier height at the grain boundary [44]. If the intragrain mobility is assumed to be the same as that in single crystal Si bulk and much higher than the mobility at the grain boundary, then μ_{eff} can be reduced to

$$\mu_{eff} \sim q\frac{v_cL_g}{kT}\exp\left(\frac{-E_b}{kT}\right) . \qquad \text{(Eq. 3-3)}$$

When device is turned on, the drain current can be expressed as

$$I_d = \mu_{eff}\, C_{ox}\, \frac{W}{L}\left[(V_g - V_{th})V_d - \frac{1}{2}V_d{}^2\right] \propto \exp\left(\frac{-E_b}{kT}\right) . \qquad \text{(Eq. 3-4)}$$

Here we can approximately regard the potential barrier height E_b as the activation energy of drain current, which can be obtained from the slope of the Arrhenious plot of drain current.

Figure 3.26 shows the potential barrier height as a function of gate overdrive in the three operation modes. The data give some clues for understanding the difference in conduction between the two types of devices. For the IM devices, due to the aforementioned gate coupling effect, the barrier height for the DG mode is lower than those for the SG modes with varying gate overdrive. This is consistent with the superior DG performance in terms of better SS and the larger I_{on}. However, for the AcM devices, it can be seen that the barrier height for the DG mode is not only lower than those for the SG modes, but also decreases more quickly with increasing gate overdrive. The greater G_m enhancement for AcM devices shown in Fig. 3.25 can be attributed to the charge effect accounting for the quicker lowing in barrier height as

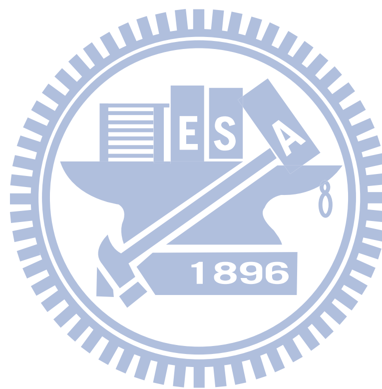
compared with the IM devices. The results of the TCAD simulation for the electrical potential along the channel depth of the AcM device under SG and DG operations with the same gate overdrive of 1V are shown in Fig. 3.27. When the AcM devices are turned on under the DG mode, the two gates simultaneously relieve the surface bend bending while the width of a quasi neutral region in the central Si channel increases with increasing gate overdrive. This means the conductive region in the channel would be wider than that of the SG mode. This is convinced with the results shown in Fig. 3.28 which illustrates the simulated hole concentration under the conditions of Fig. 3.27. It is seen that the carrier density in the DG mode is significantly larger than that in the SG mode with the same gate overdrive, and the significant G_m enhancement of the DG operation is also attributed to the larger amount of holes.

Another important finding for the AcM devices is that the peak value of G_m ratio shows dependence on the channel length. Such trend is not obvious for the IM devices. Figure 3.29 shows the G_m ratio with different channel lengths for the AcM devices. It can be seen that as the channel length is shorter, the peak value becomes larger, e.g., up to 4.6 with channel length of 0.7μm. The reason is attributed to the severer SCEs for the AcM devices. As mentioned above, the SG modes exhibit a worse SS degradation which also degrades the G_m. Since the DG mode shows higher immunity to the SCEs, the G_m difference between the SG mode and DG mode becomes more prominent with shorter channel length.

3.3.2 Transconductance Degradation

As we mentioned earlier, for the AcM devices, when the device is turned on, most of the channel is basically in quasi-neutral condition. For the IM devices, the carriers in the inversion layer are attracted by the gate bias, resulting in a

severe band bending [45]. The TCAD simulation results are shown in Figs. 3.30(a) and (b) for the IM and AcM devices, respectively. As can be seen in the figures, the electric field at the surfaces is much larger for the IM devices. Besides, for the AcM devices, the much lower gradient of electric field near the central region also indicates that the central bulk is a quasi-neutral region when the device is turned on. The normalized G_m ($G_m/G_{m.max}$) as a function of gate overdrive is given in Fig. 3.31, from which we can see that the G_m degradation in high gate overdrive regime is more severe for the IM device [46]. For the AcM devices, the conduction is through the whole channel and thus the carriers might inherently suffer less from the scattering of the surface roughness and the interface traps.



Chapter 4

Conclusion and Future Work

4.1 Conclusion

In this work, we have fabricated and characterized a novel p-type AcM double-gated poly-Si NW transistors featuring an independent double-gated configuration. Thanks to the ultra-thin channel thickness of 20nm, the AcM devices can still be turned off under all operation modes, despite a high doping concentration is contained in the channel. Moreover, as compared with the IM counterparts, some intriguing characteristics are revealed. As the AcM devices are on, the carriers flow mainly through the whole channel, thus the current level is significantly larger than that of the IM ones in which the conduction is mainly through the induced inversion layer near the channel interface. From the TCAD simulation results, distribution of the carriers in the channel and the operation mechanisms of the two types of devices are analyzed. Unlike the IM device whose channel body is essentially depleted when the device is turned on, the quasi-neutral region of the AcM device gradually expands from the channel center to the interfaces with increasing gate overdrive.

For the subthreshold characteristics, due to the additional EOT contributed by the surface depletion region, the AcM devices exhibit worse SCEs than the IM devices, resulting in severer SS degradation and V_{th} roll-off. Moreover, the variation of electrical parameters is also severer for the AcM devices due to the higher EOT and high channel doping concentration, representing another major

issue for the AcM devices. Fortunately, these problems for the AcM devices would be ameliorated with a thinner channel thickness and DG operation. Our analysis and experimental results pointed out that the bias condition applied to the back gate would also affect the fluctuation in device characteristics.

On the other hand, from the transconductance characteristics and simulation results, for the AcM devices, the influence of the gate coupling effect is different from the IM devices. The greater G_m enhancement with the DG operation relative to SG modes for the AcM devices can be attributed to the quicker lowing in barrier height and the larger amount of holes as compared with the IM devices. Moreover, the peak value of G_m ratio shows dependence on the channel length. That's because the DG mode has higher immunity to the SCEs than the SG mode. Moreover, from the simulation results, the electric field at the surfaces of the IM device is larger than that of the AcM device at the same gate overdrive. For the AcM devices, the conduction is through the whole channel and thus the carriers inherently suffer less from the scattering of the surface roughness and the interface traps, as we can see that the G_m degradation in high gate overdrive regime is more severe for the IM device.

4.2 Future Work

In this study, we've successfully fabricated the p-type AcM double-gated poly-Si NW devices and compared their electrical characteristics with those of the IM devices with undoped channels. One of our initial goals is to perform in-situ doped deposition for preparing the poly-Si films so the device's S/D and channel have the same doping type and level. But being limited by the available techniques, such goal is not achieved in this work. This topic, however, deserves

future effort to achieve. Besides, effects of the doping concentration in the channel and the channel thickness remain not so clear and should be further investigated in the future.

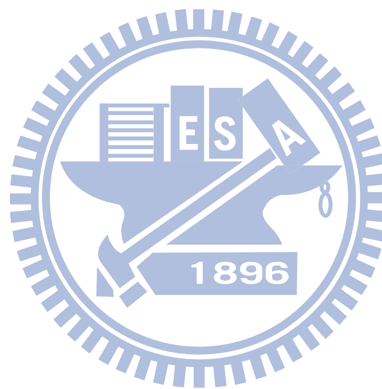


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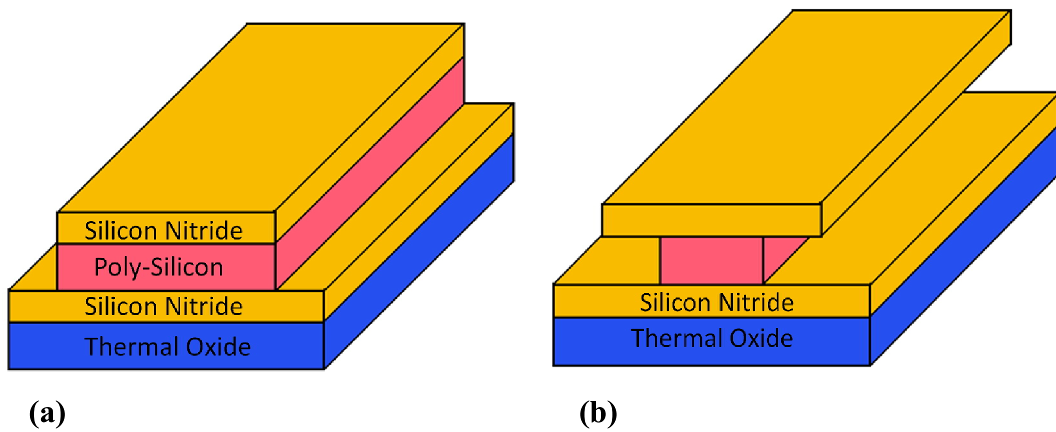
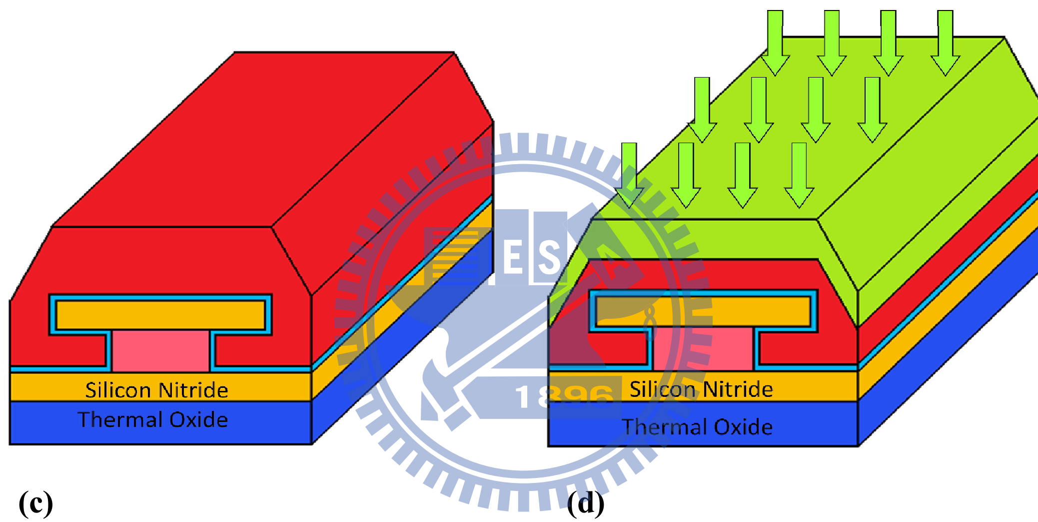
Figure Captions



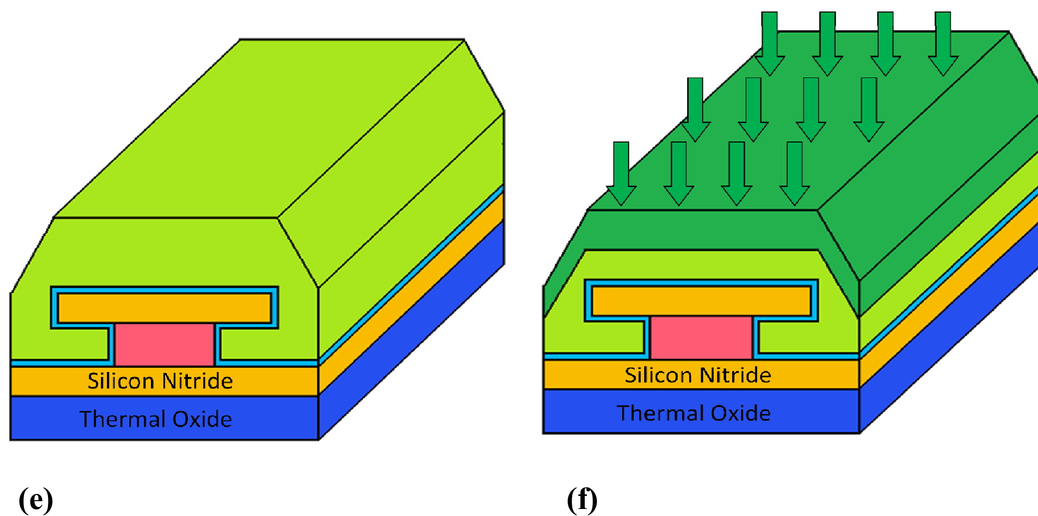
(a) **(b)**

Fig. 2.1. (a) 1st gate definition and (b) lateral etching of poly-Si for NW channels.



(c) **(d)**

Fig. 2.1. (c) α-Si deposition followed by SPC and (d) implantation of BF_2^+ at a dose of 5 × 10^{14} cm^{-2}.



(e) **(f)**

Fig. 2.1. (e) Drive-In at 900°C for 30 min and (f) S/D implantation using BF_2^+ at a dose of 5 × 10^{15} cm^{-2}.

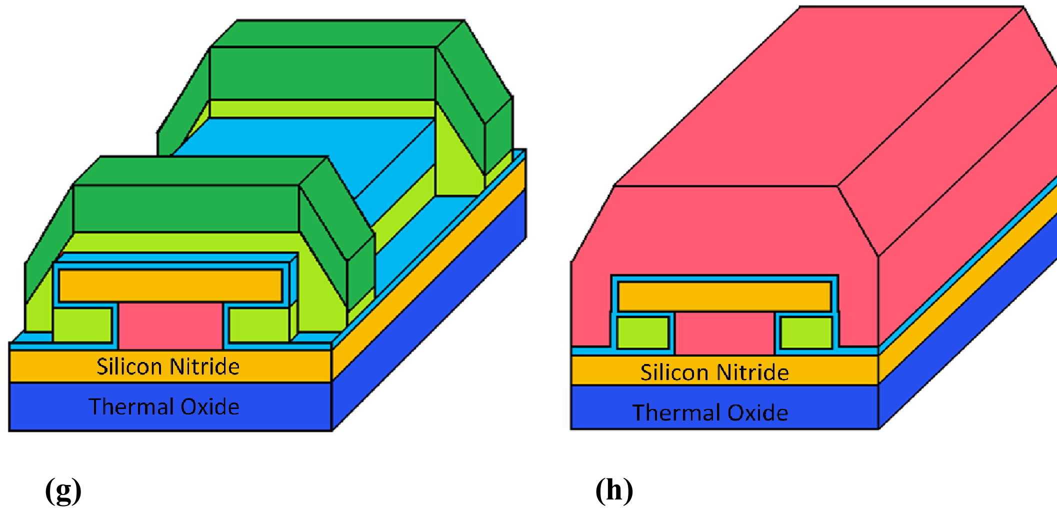


Fig. 2.1. (g) S/D and NW channels definition and (h) n^+ poly-Si for 2nd gate.

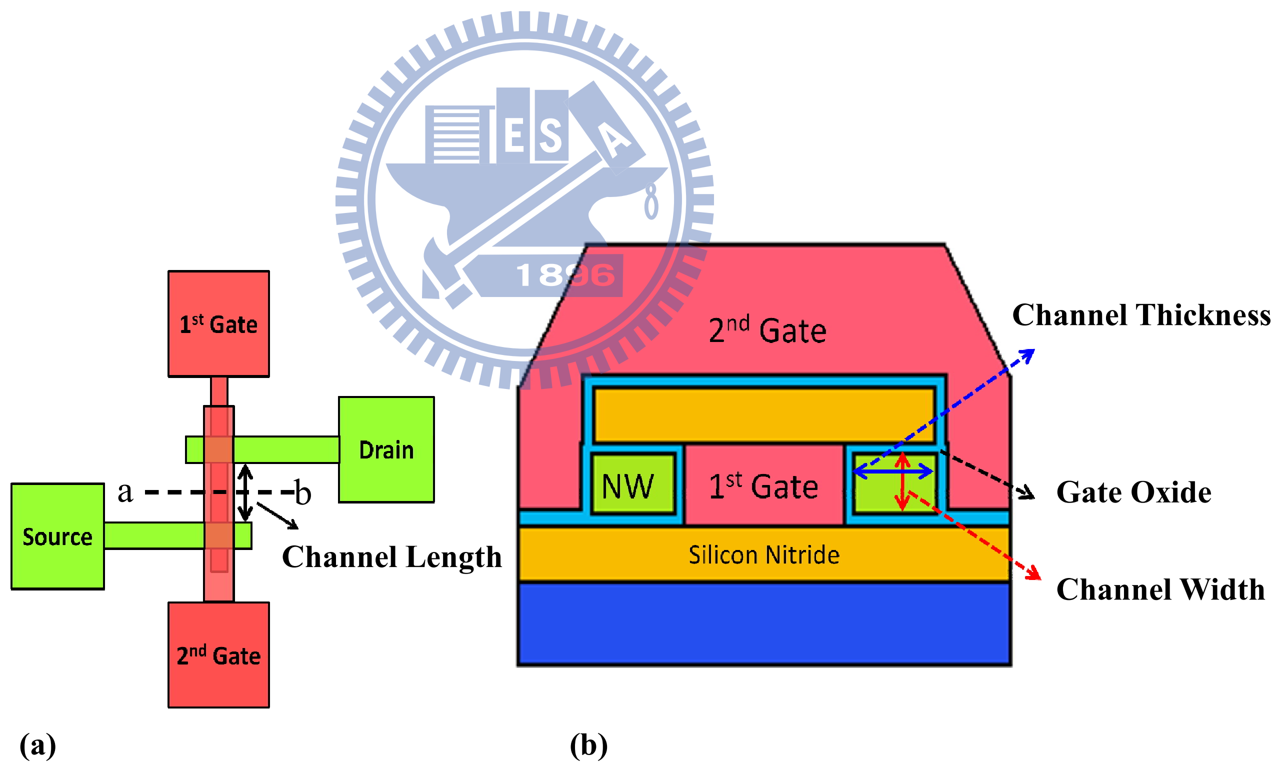
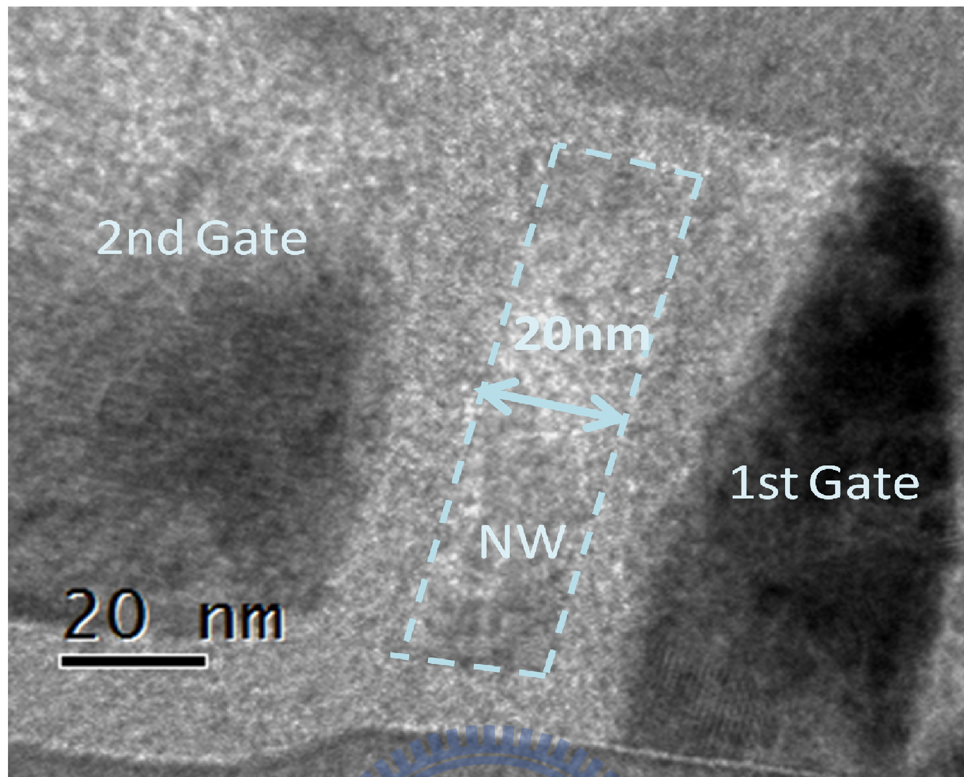
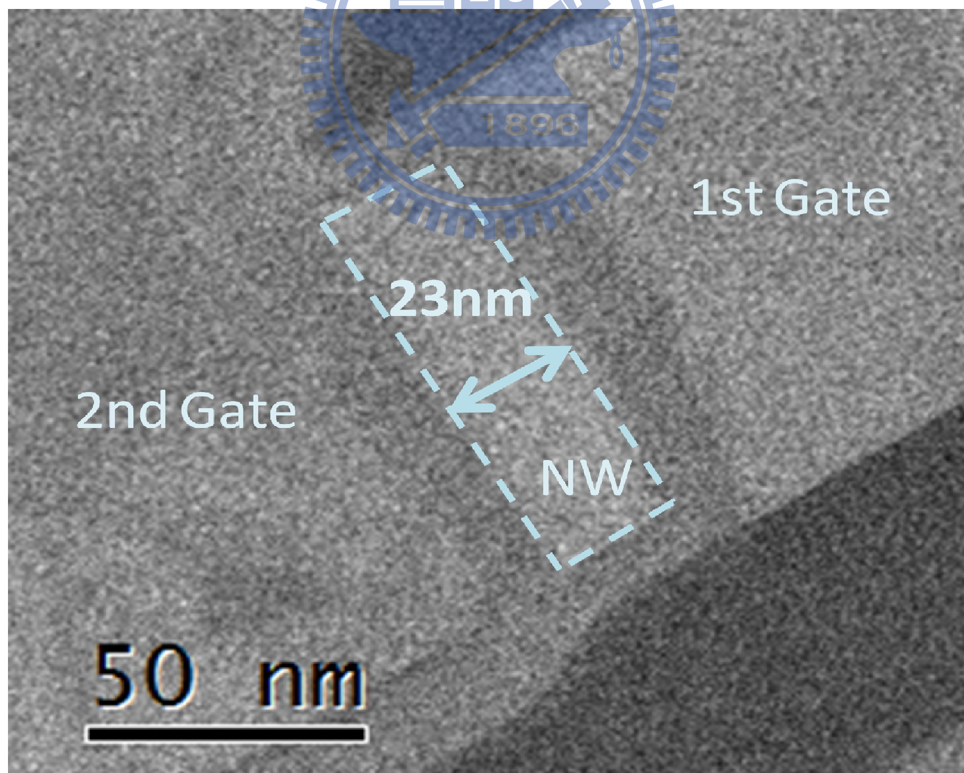


Fig. 2.2. (a) Layout and (b) cross-section view of the double-gated device.

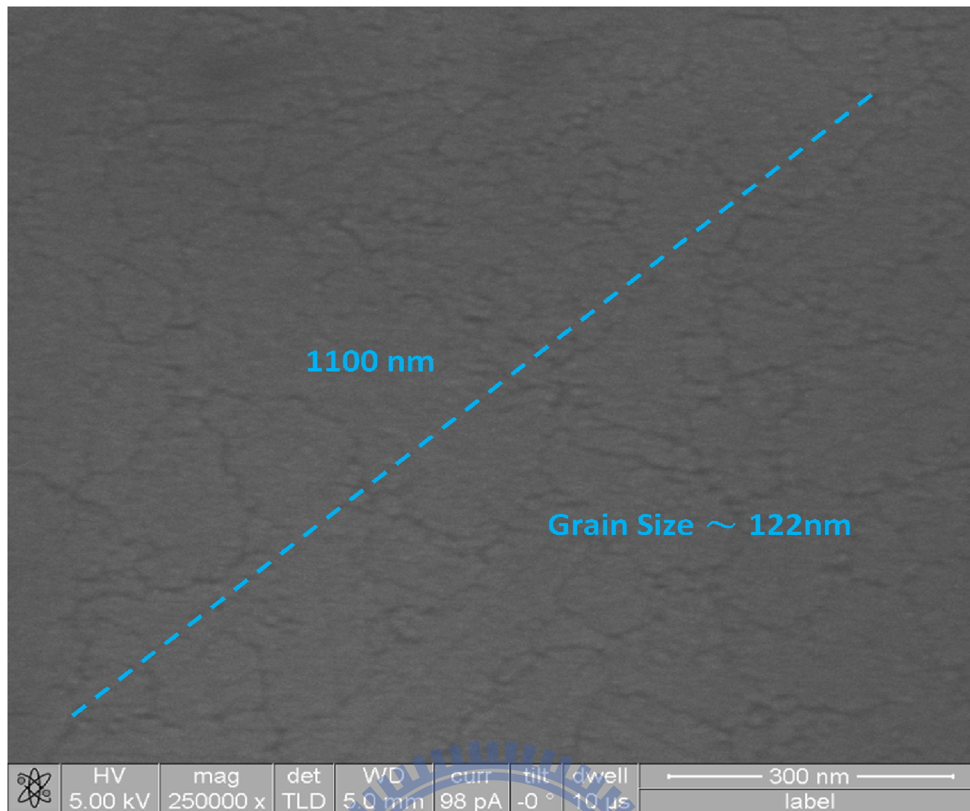


(a)



(b)

Fig. 2.3. TEM images of (a) an IM device and (b) an AcM device.



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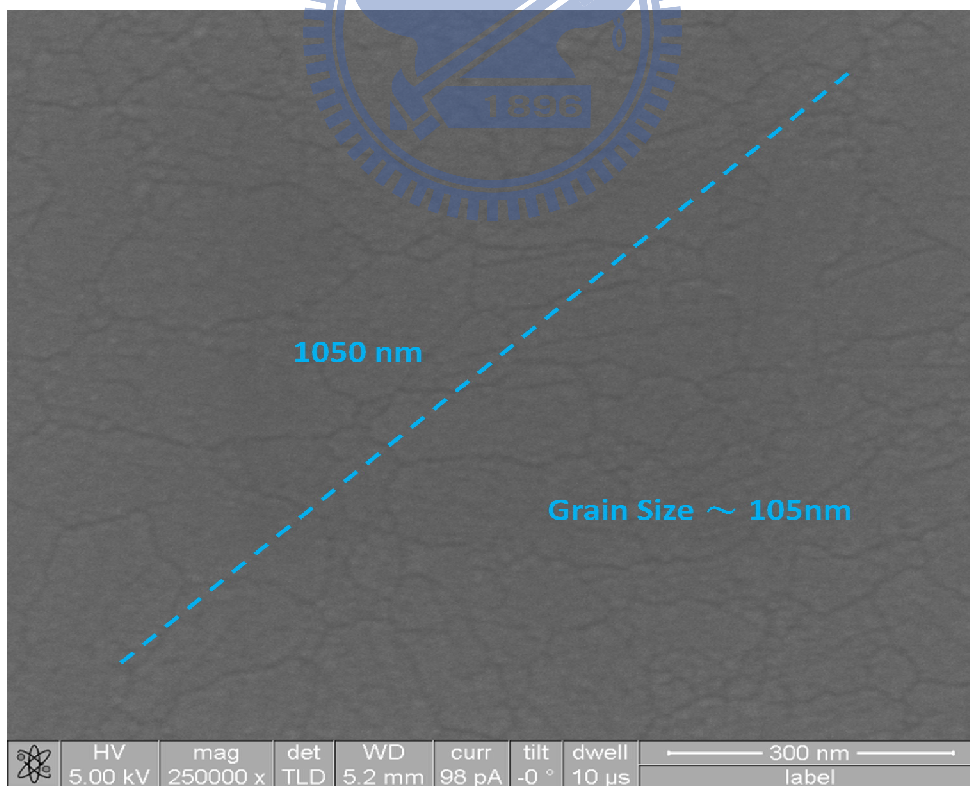
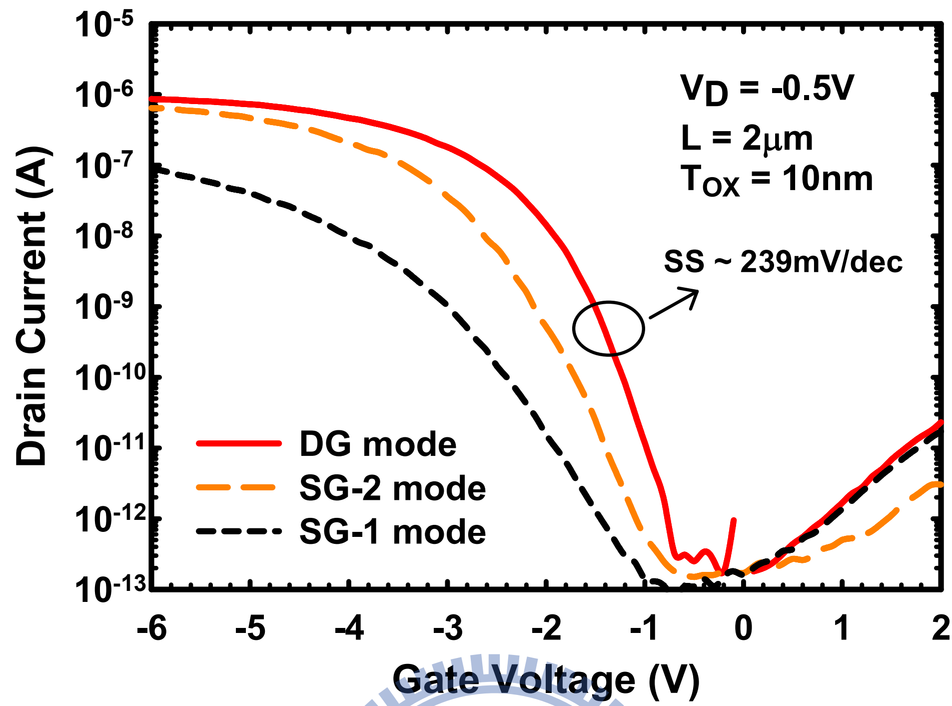


(b)

Fig. 2.4. SEM images for grain size of (a) an IM device and (b) an AcM device.



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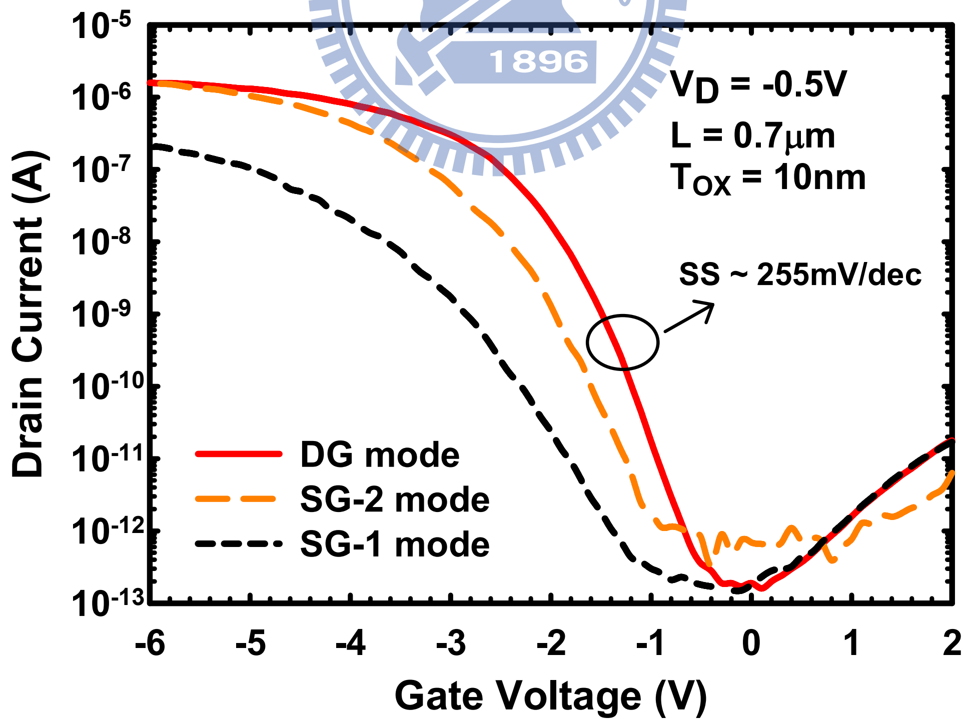
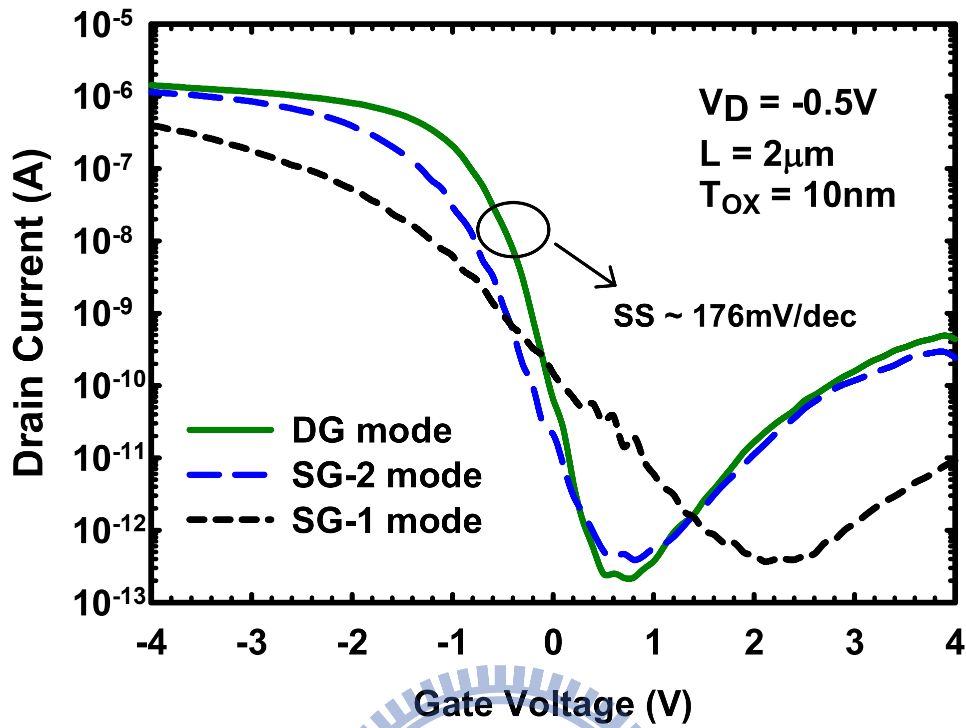


(b)

Fig. 3.1. Transfer characteristics of the IM device for (a) 2μm channel length and (b) 0.7μm channel length.



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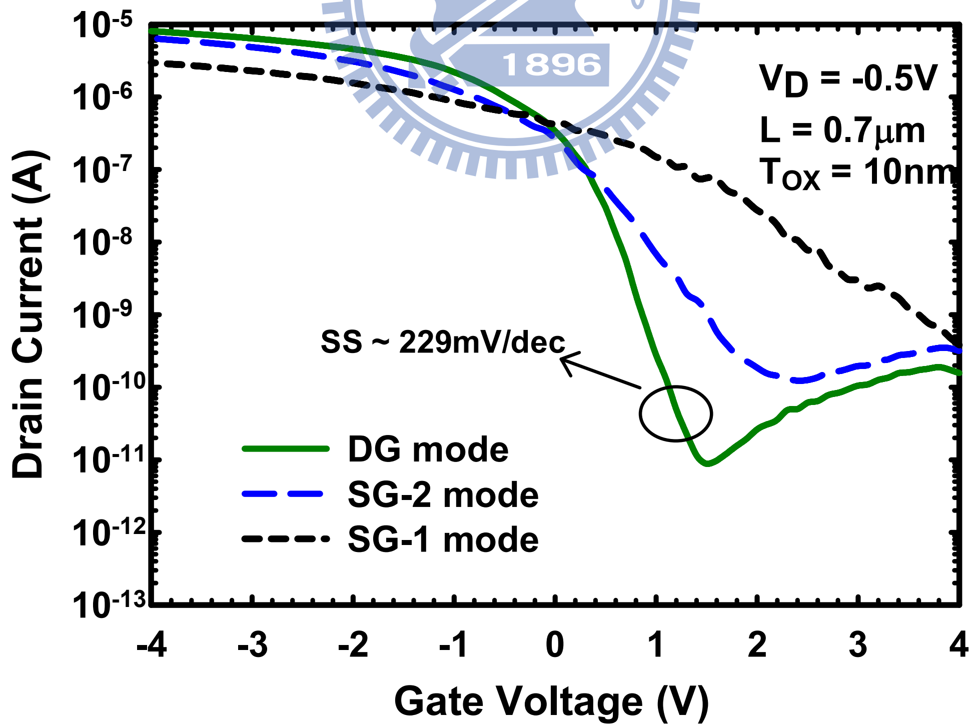


(b)

Fig. 3.2. Transfer characteristics of the AcM device for (a) 2μm channel length and (b) 0.7μm channel length.

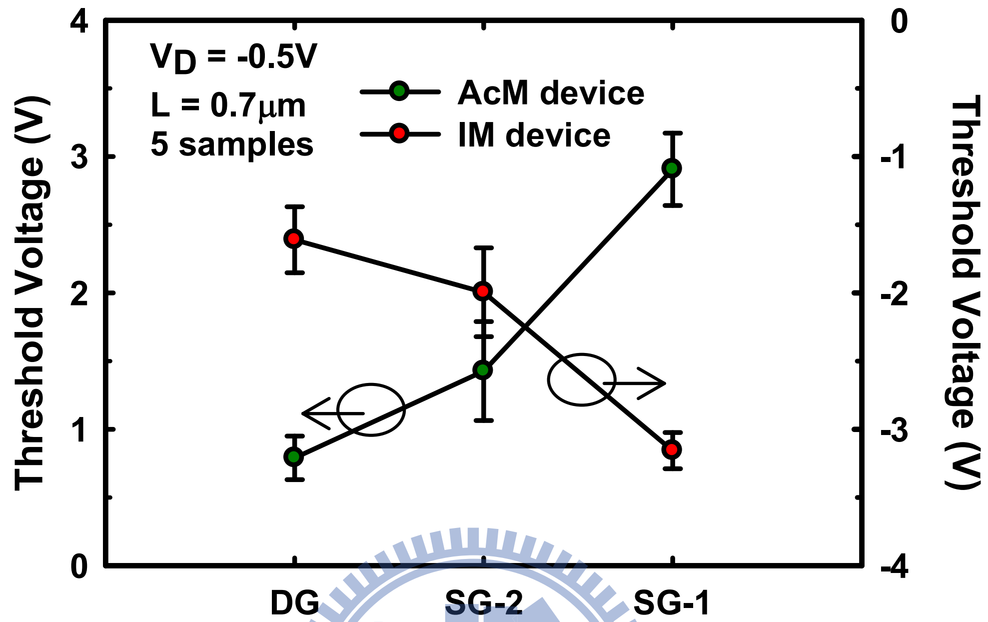
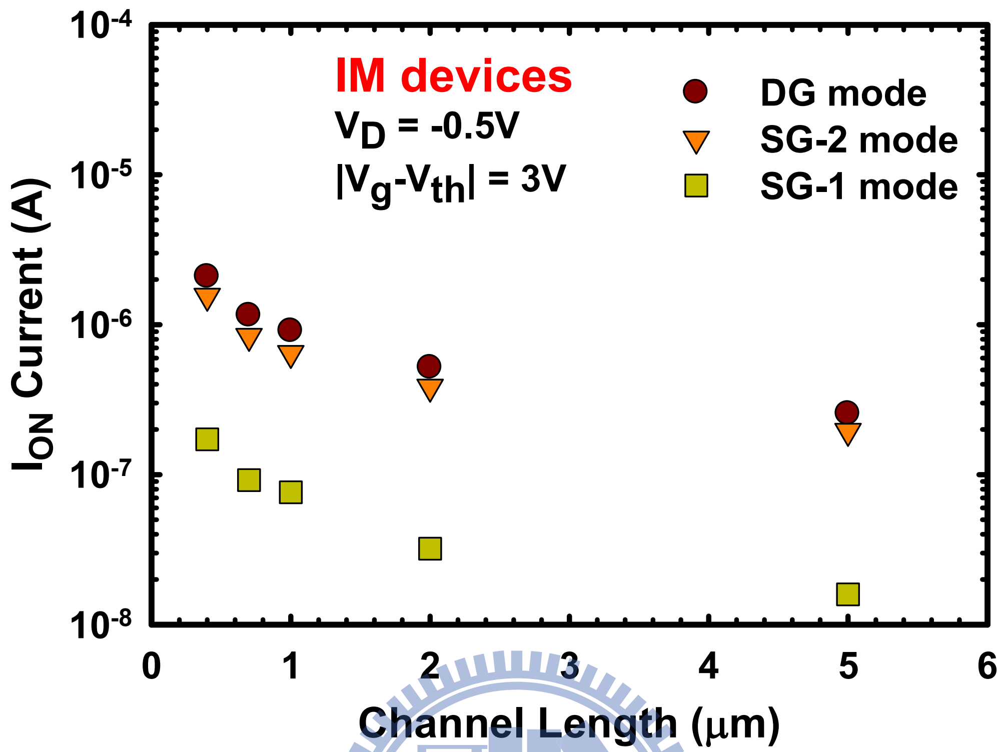
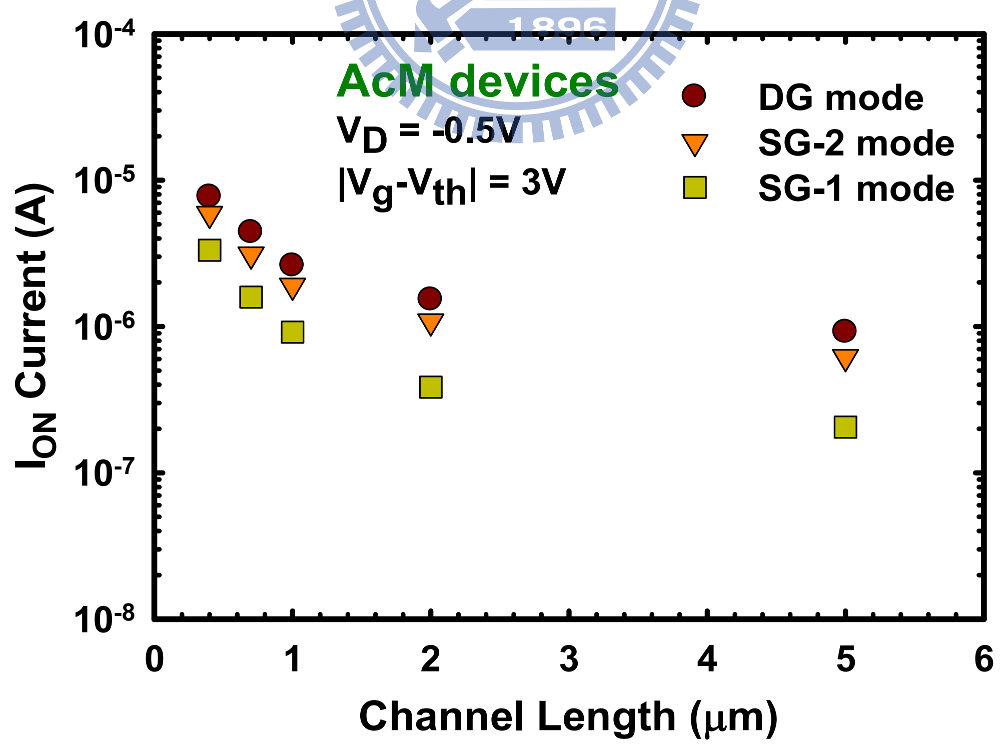


Fig. 3.3. Threshold voltage of the three operation modes for 0.7μm for both devices.



(a)



(b)

Fig. 3.4. I_{on} characteristics of the (a) IM device and (b) AcM device.

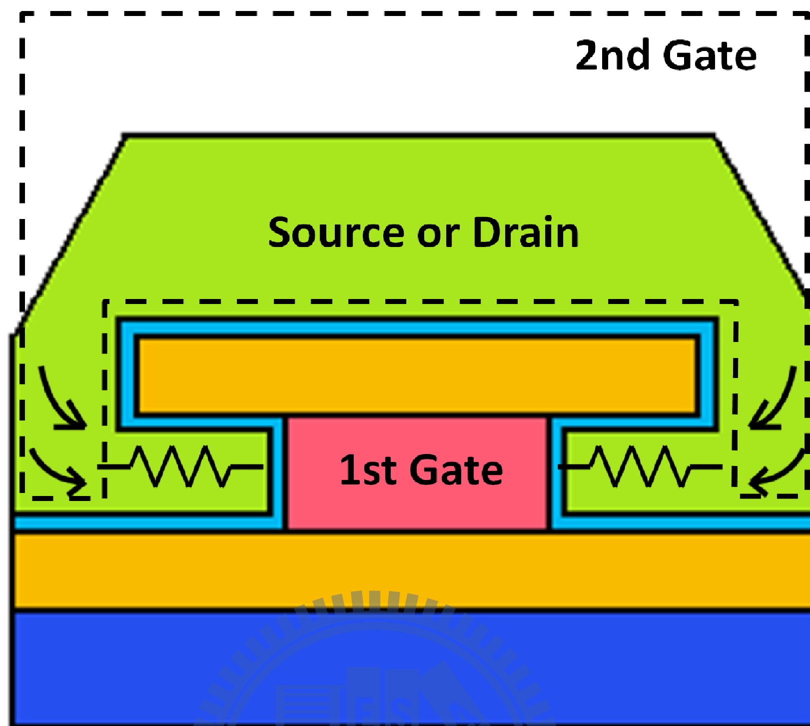
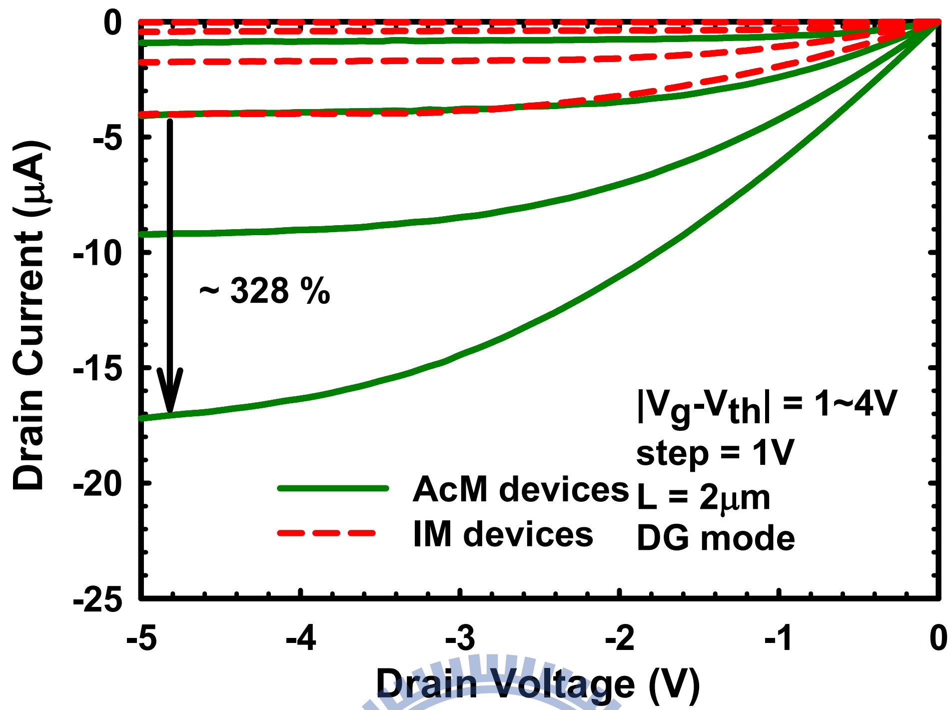


Fig. 3.5. Schematic illustrating the existence of an un-gated region for the current path from S/D to channel in the SG-1 mode, resulting in an extra series resistance.



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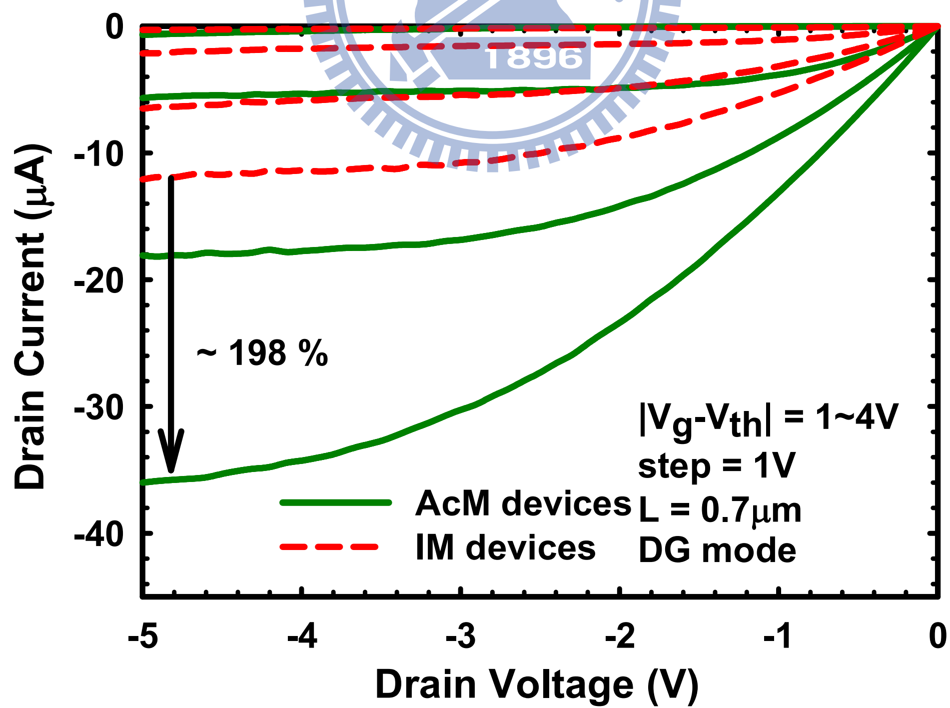
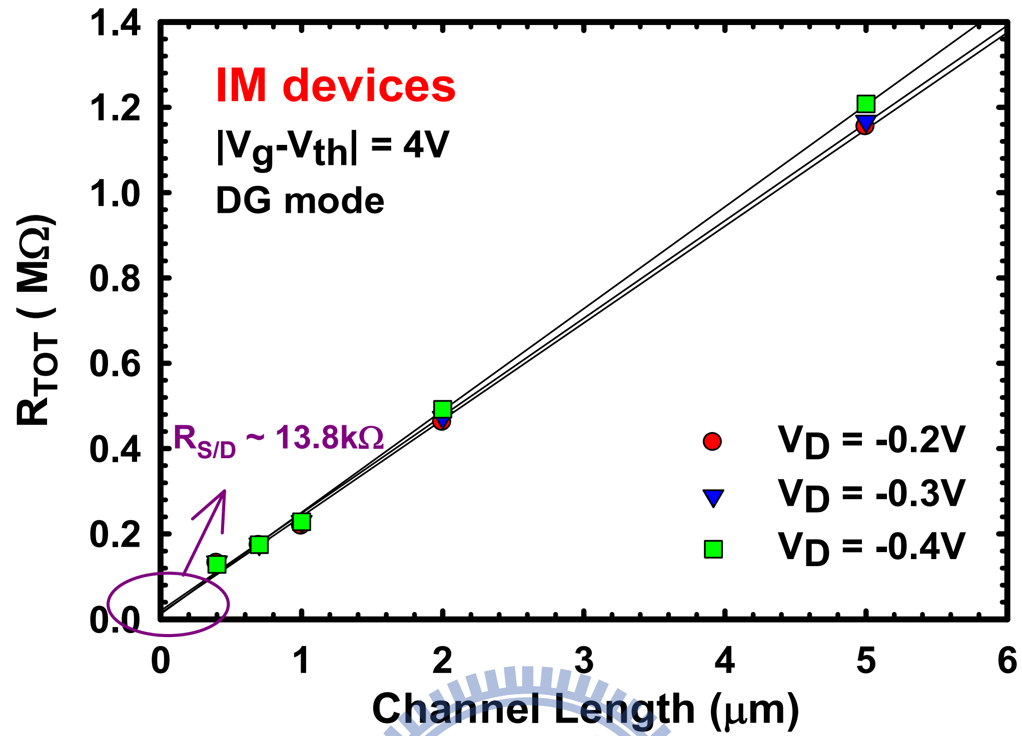
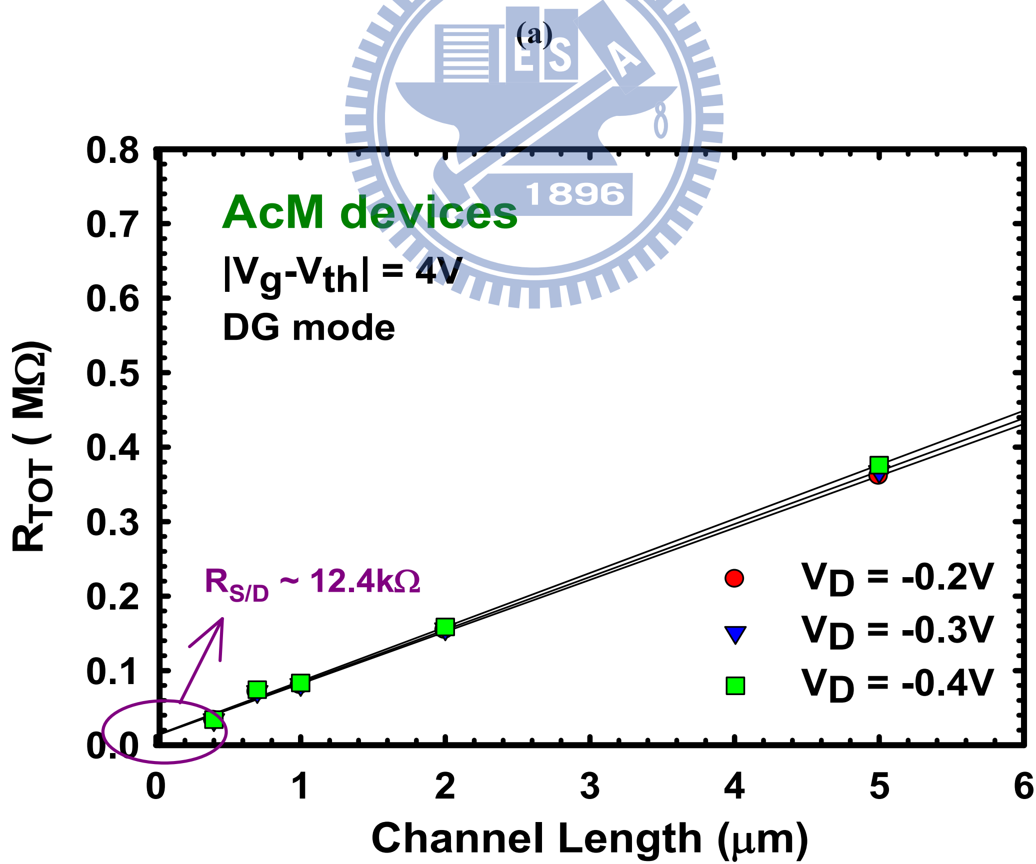


(b)

Fig. 3.6. Output characteristics for both devices in the DG mode for (a) 2μm channel length and (b) 0.7μm channel length.



(a)



(b)

Fig. 3.7. Total resistance as a function of channel length for (a) IM device and (b) AcM device.

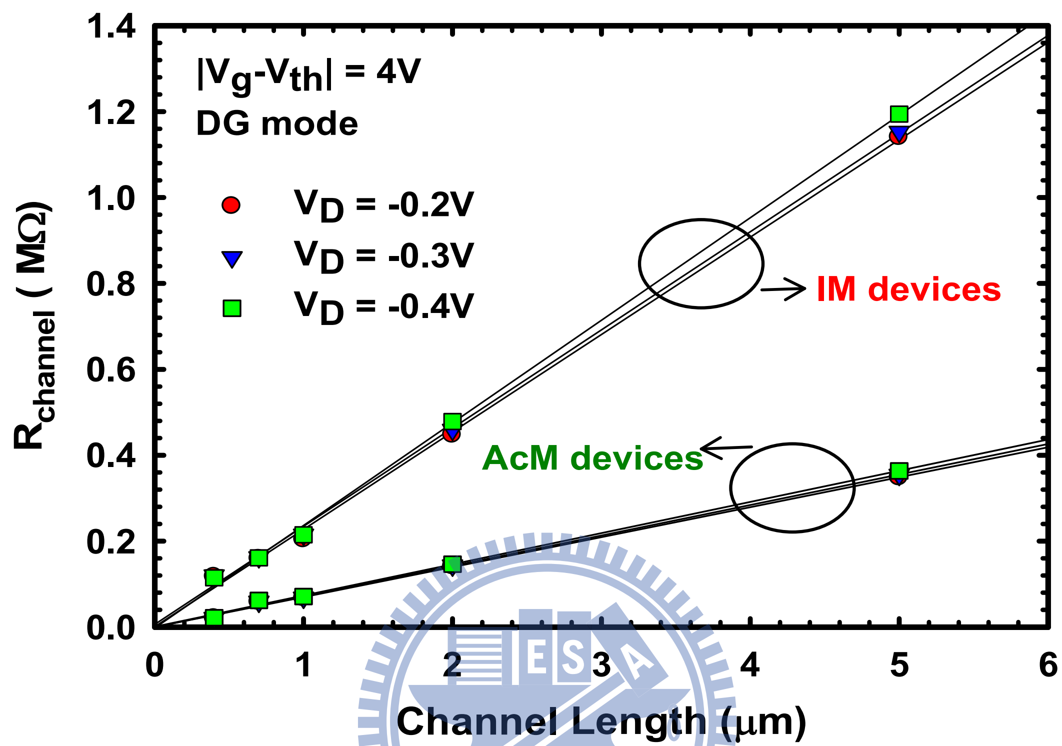
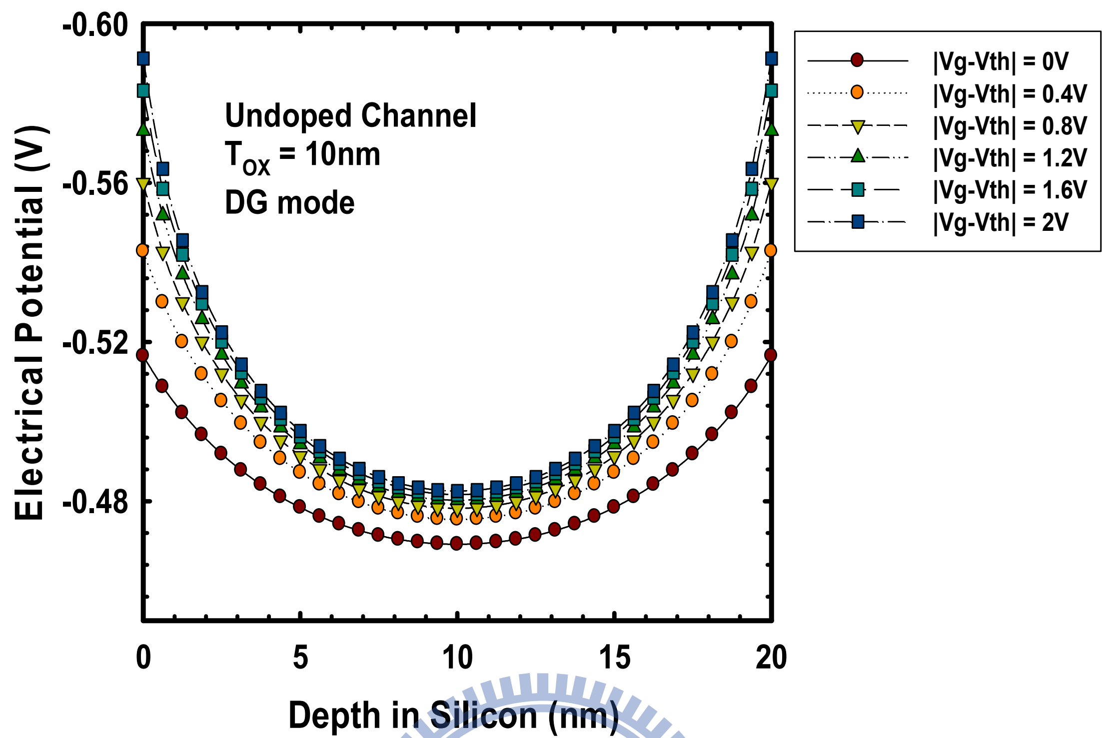
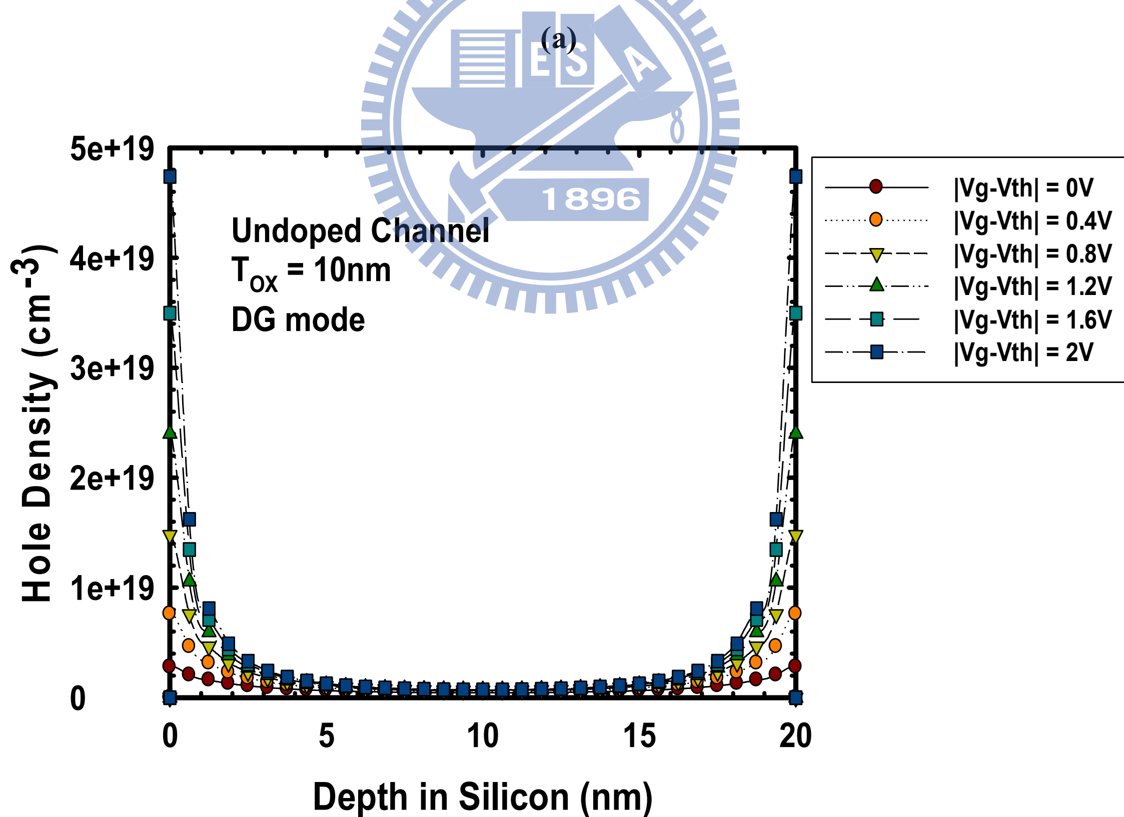


Fig. 3.8. Channel resistance (R_{TOT}-$R_{S/D}$) as a function of channel length for both devices.

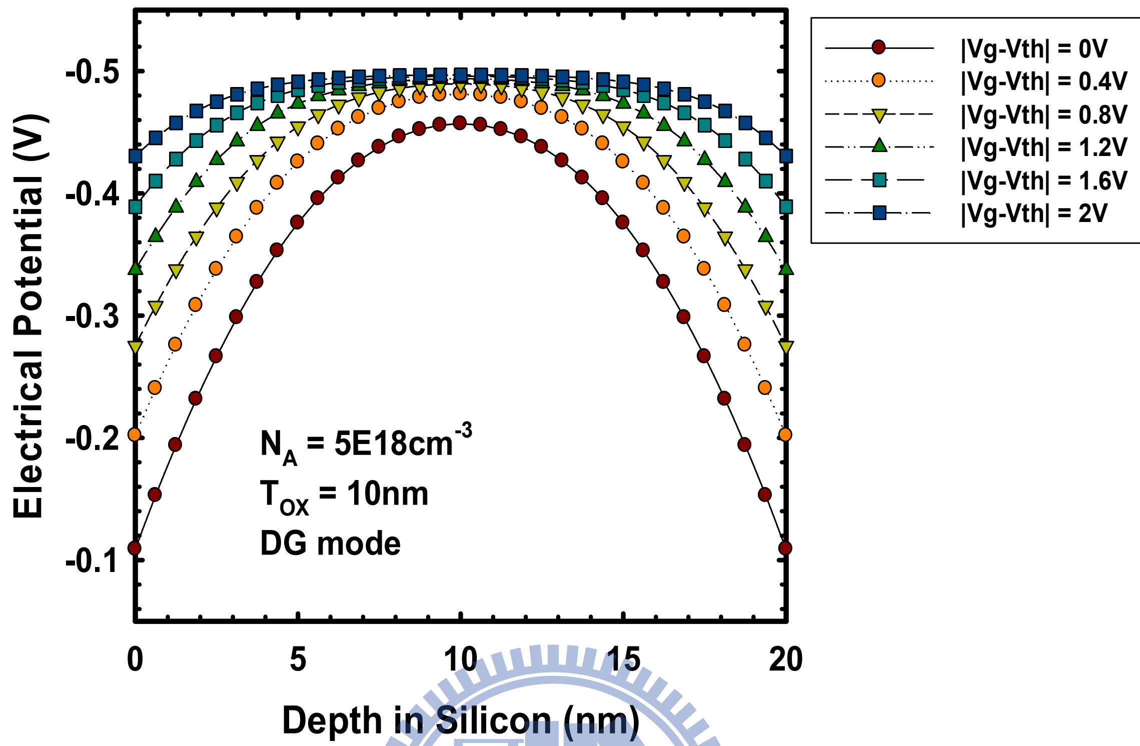


(a)

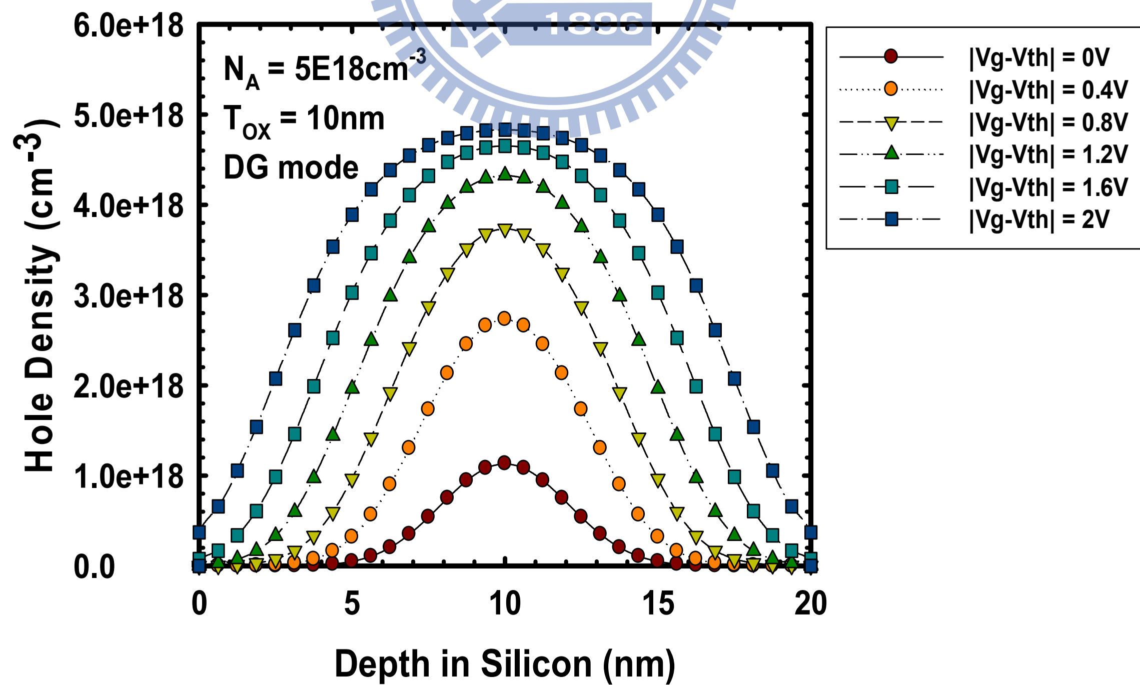


(b)

Fig. 3.9. Simulation results of (a) electrical potential and (b) hole density along channel depth with varying gate overdrive for the IM device.

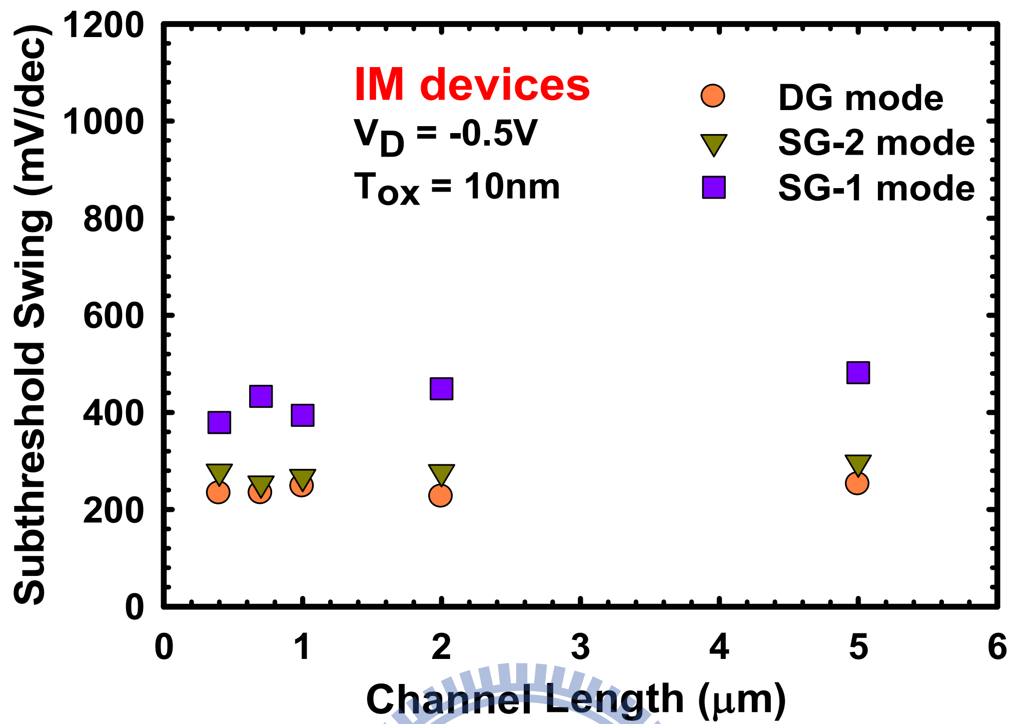


(a)

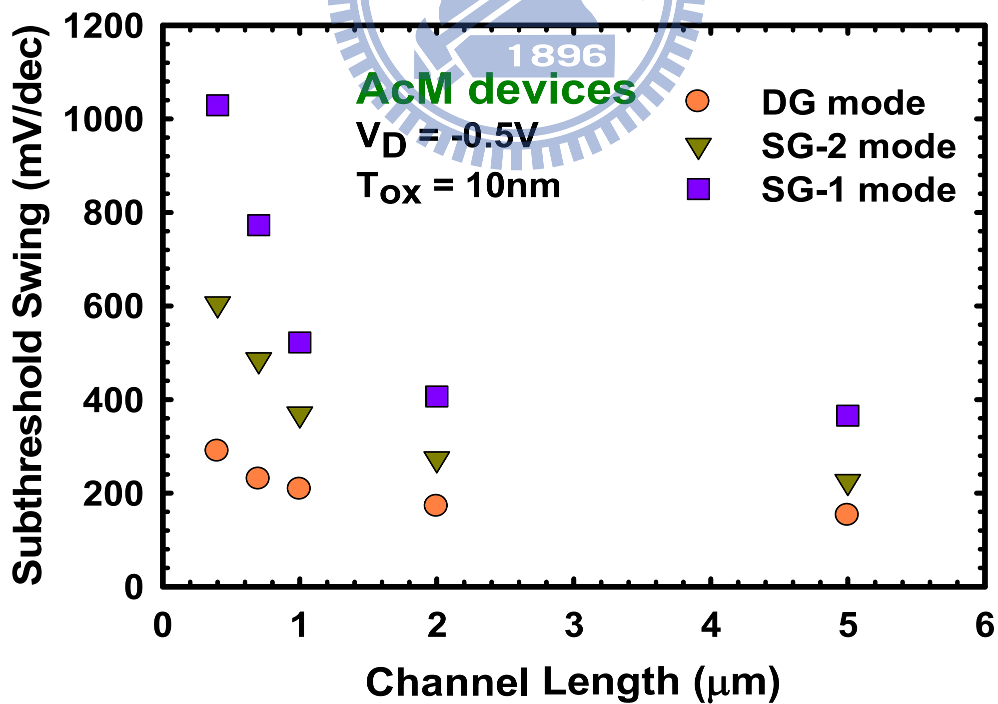


(b)

Fig. 3.10. Simulation results of (a) electrical potential and (b) hole density along channel depth with varying gate overdrive for the AcM device.



(a)



(b)

Fig.3.11. SS characteristics of the three operation modes for (a) IM and (b) AcM devices.

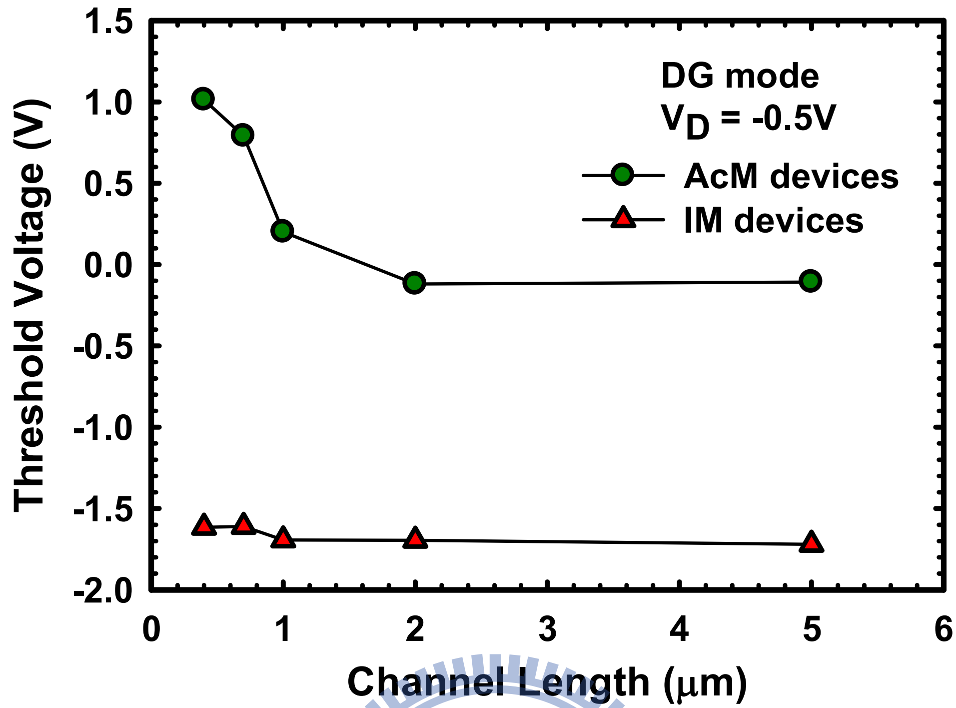


Fig. 3.12. Threshold voltage as a function of channel length for the two types of devices.

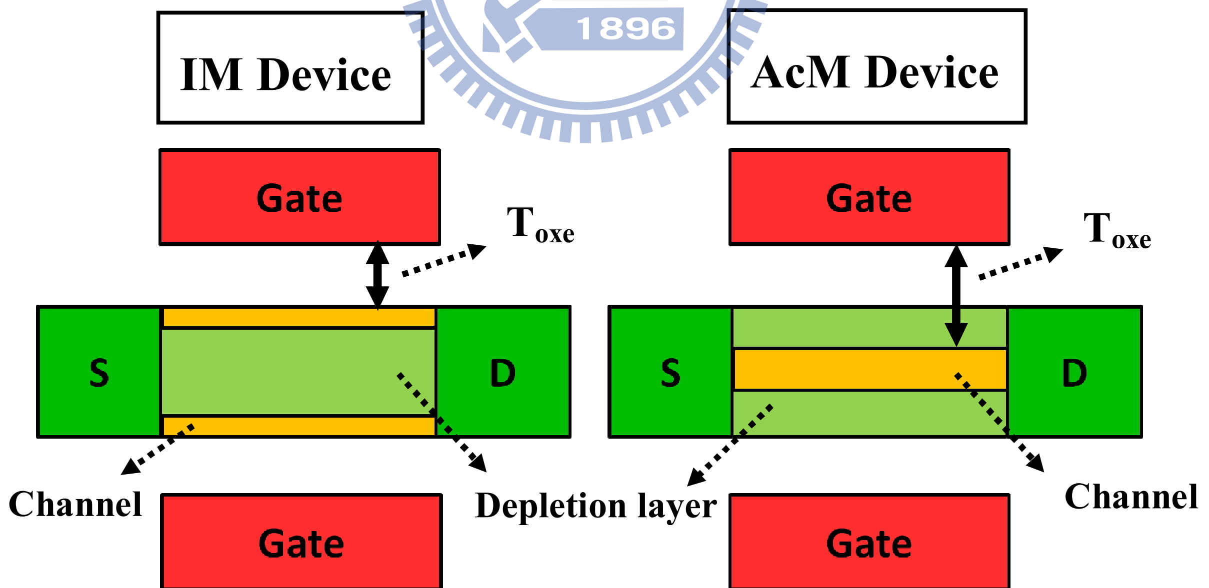


Fig. 3.13. Location of the conductive channel layer(s) inside the IM and AcM devices under DG mode of operation at V_g=V_{th}. Unlike the IM devices, the current is mainly conducted through the central Si channel and the surface depletion regions result in an additional gate dielectric for the AcM devices.

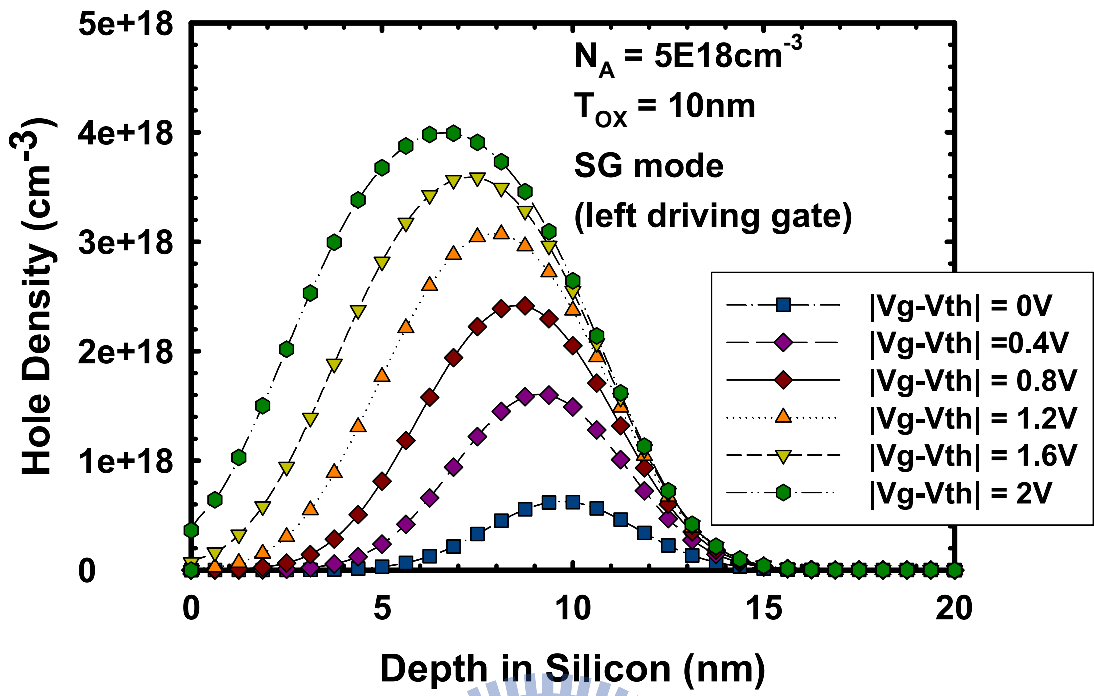


Fig. 3.14. Simulation results of hole density along channel depth with varying gate overdrive for the AcM device.

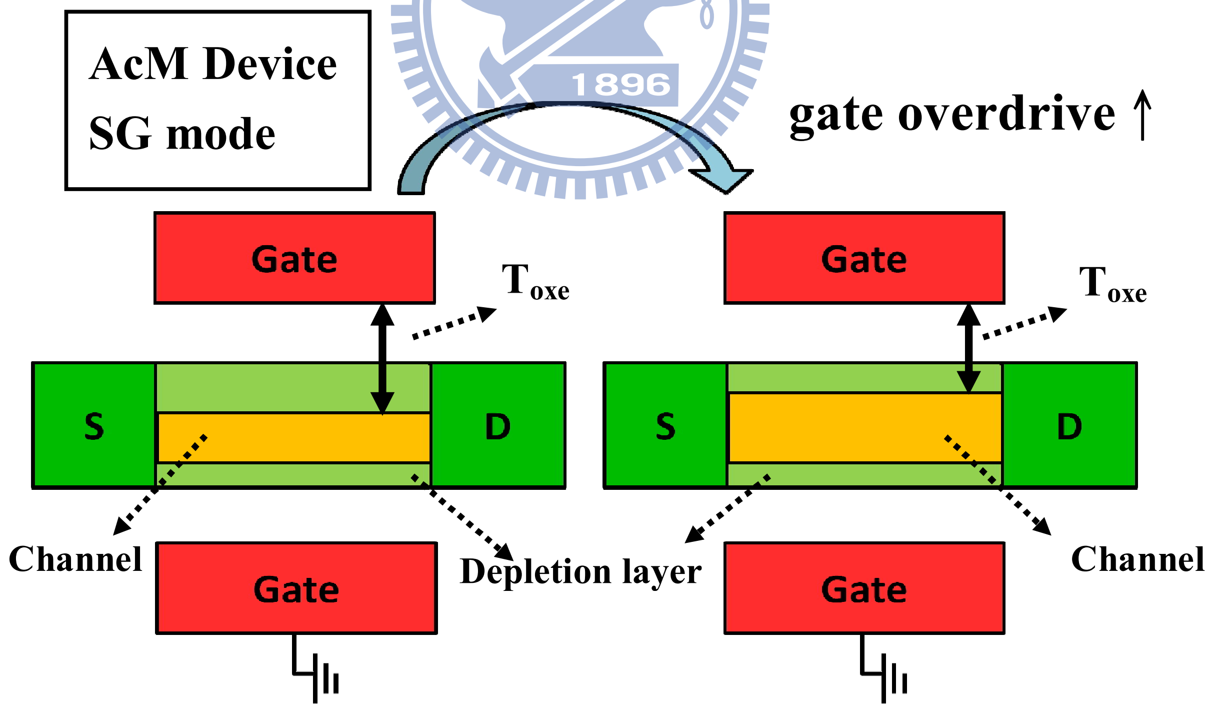


Fig. 3.15. Schematic illustrating that the EOT for the AcM devices will change with varying gate bias, which would affect the thicknesses of the depletion regions and the central conductive layer.

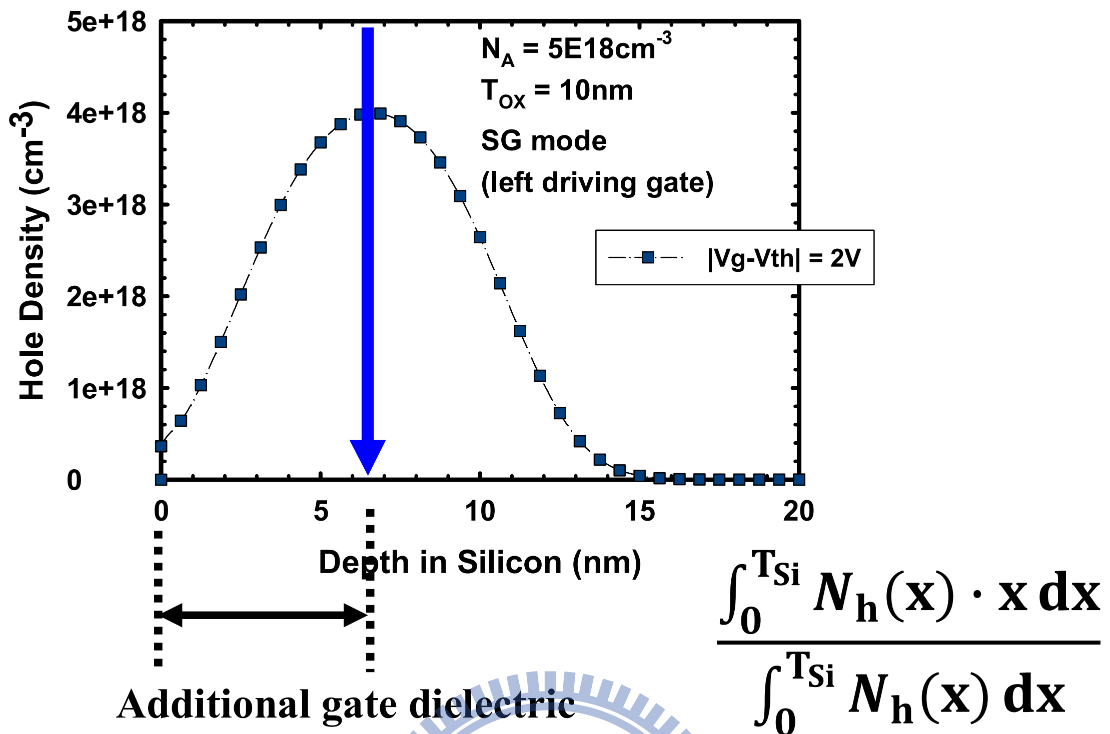


Fig. 3.16. A simple calculation and definition for the thickness of the additional gate dielectric of the surface depletion region.

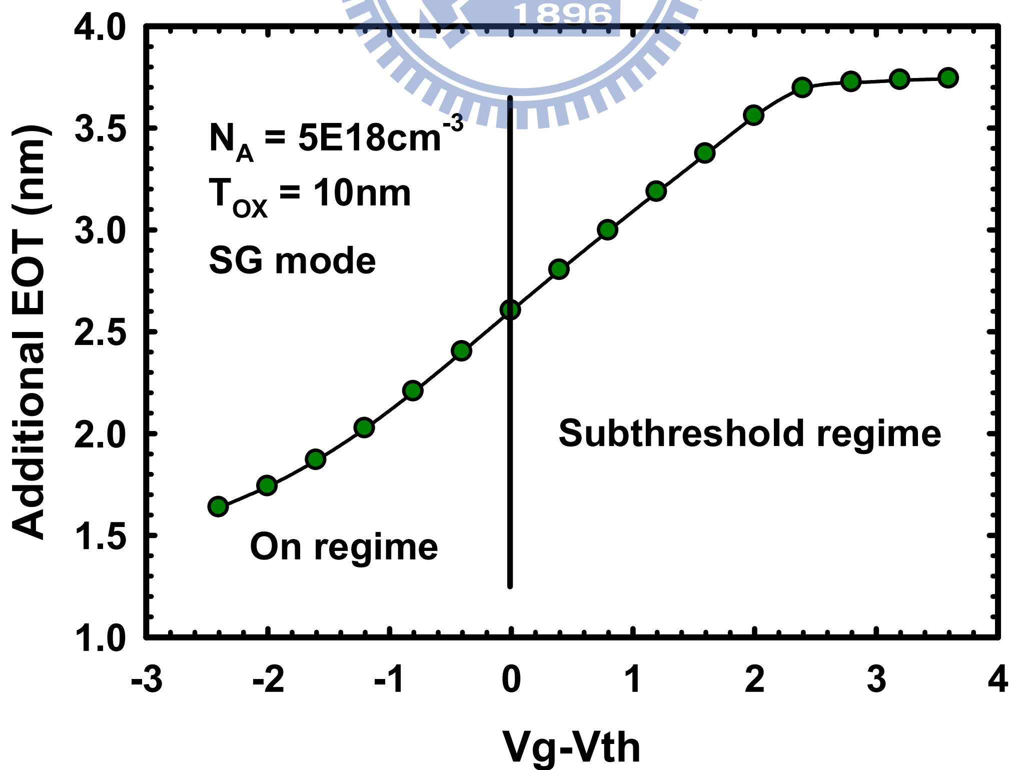
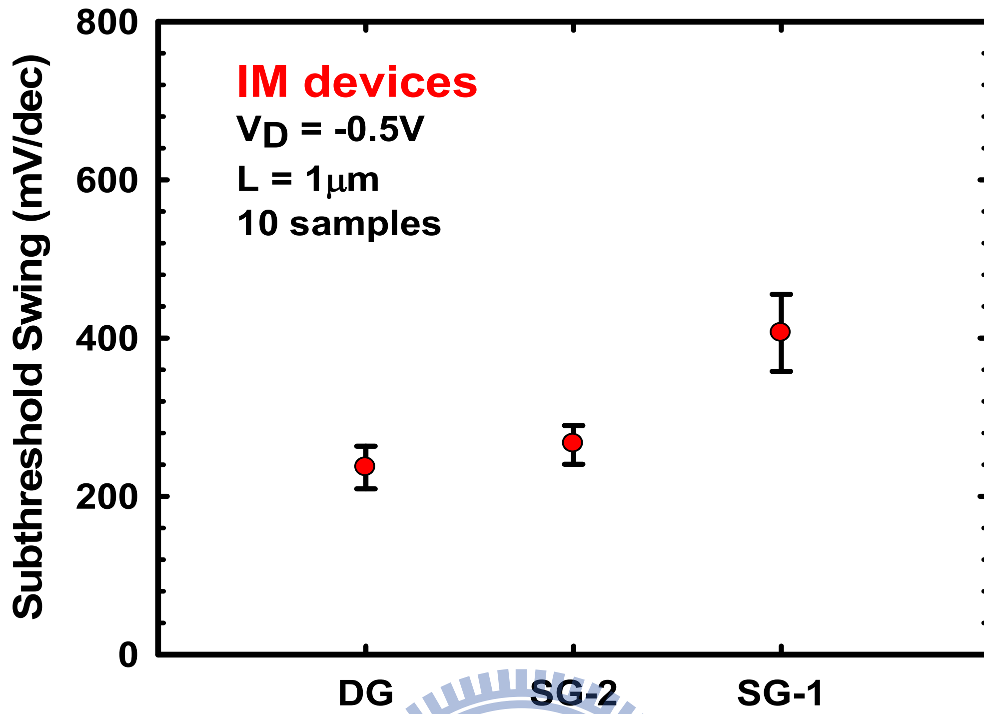
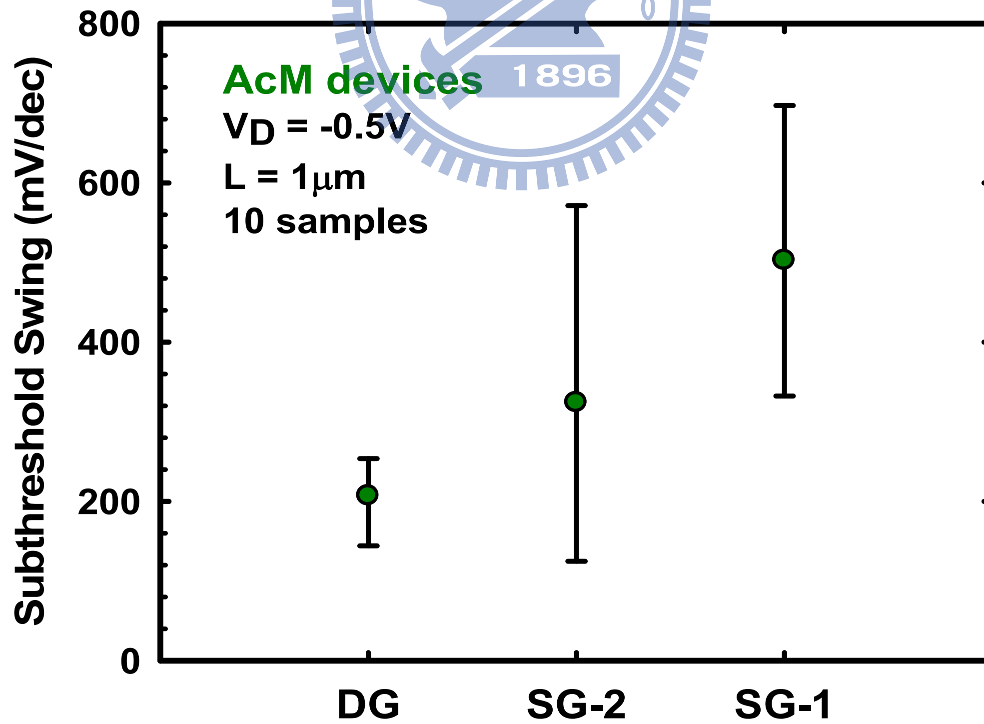


Fig. 3.17. EOT of the additional gate dielectric as a function of the gate bias.

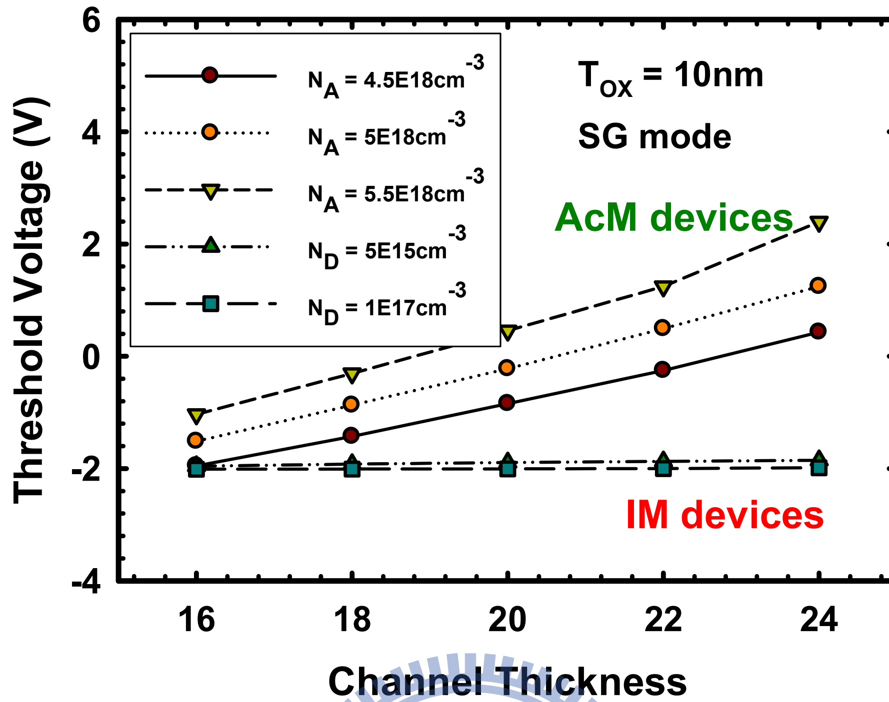


(a)

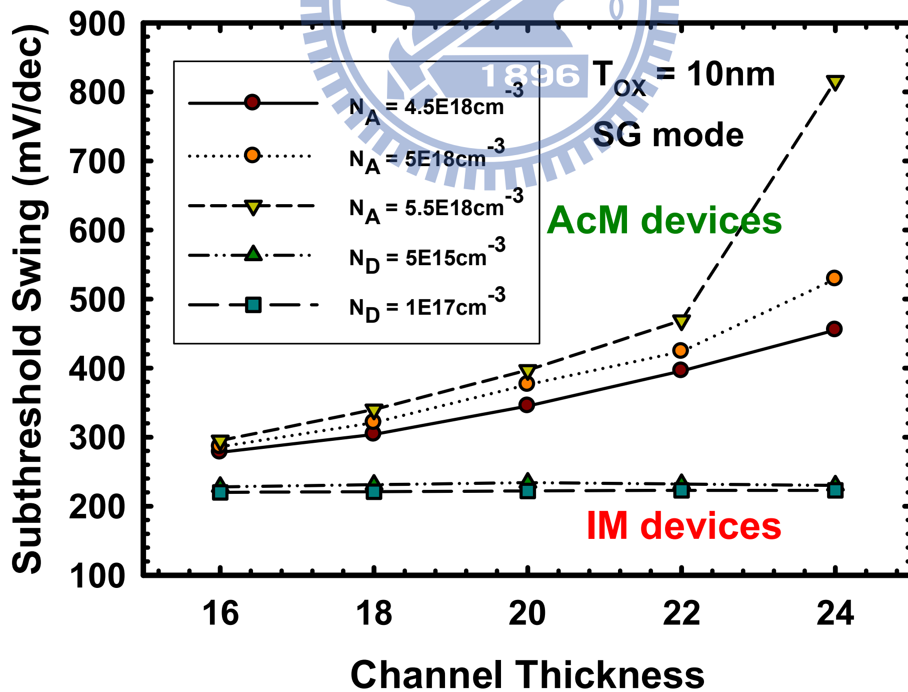


(b)

Fig. 3.18. SS characteristics of the three operation modes for the (a) IM and (b) AcM devices with L= 1μm.

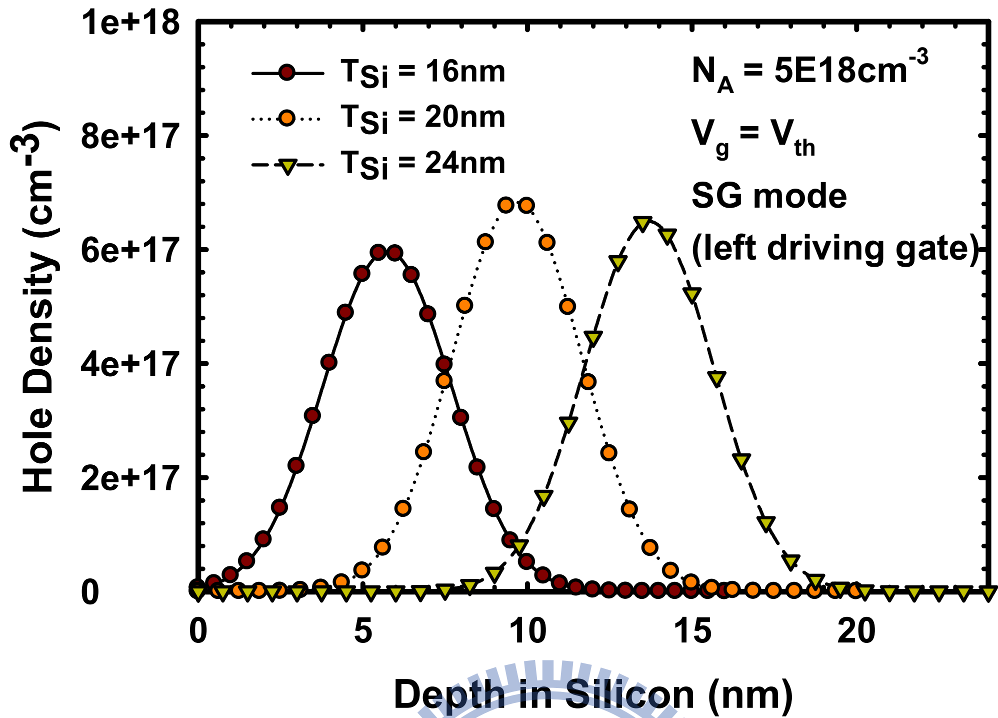


(a)

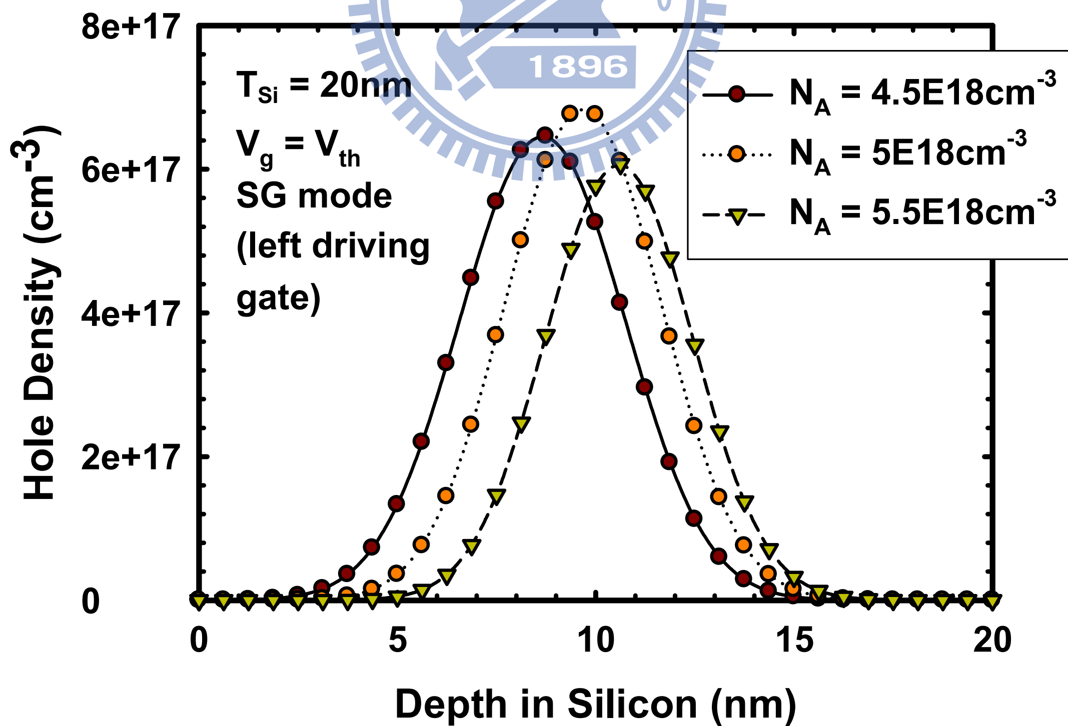


(b)

Fig. 3.19. Simulation results of (a) threshold voltage and (b) subthreshold swing as a function of channel thickness and the channel doping concentration for IM and AcM devices.



(a)



(b)

Fig. 3.20. Simulation results of hole density along channel depth with varying (a) channel thickness and (b) channel doping concentration for the AcM devices.

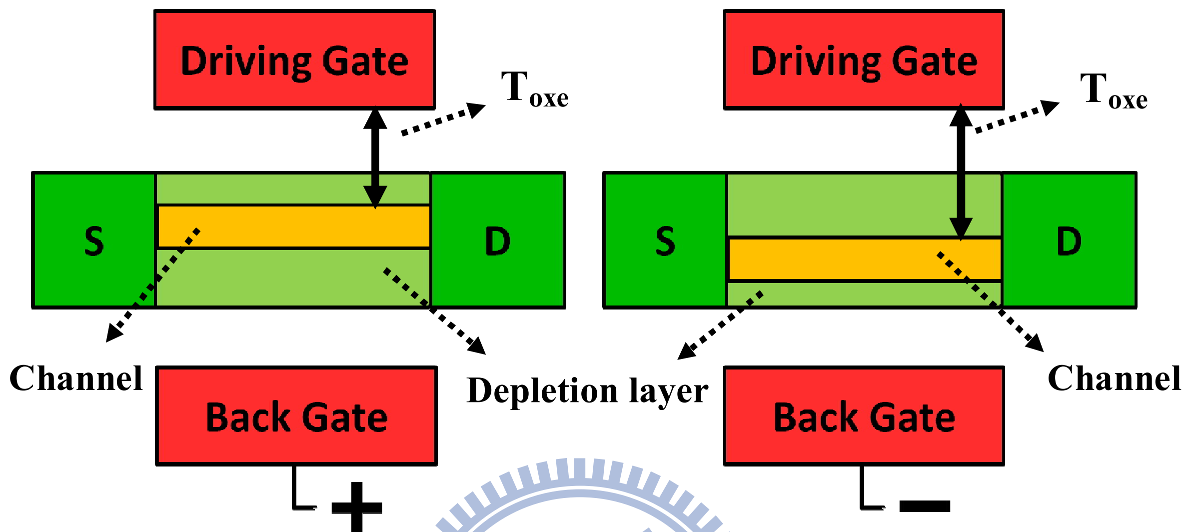
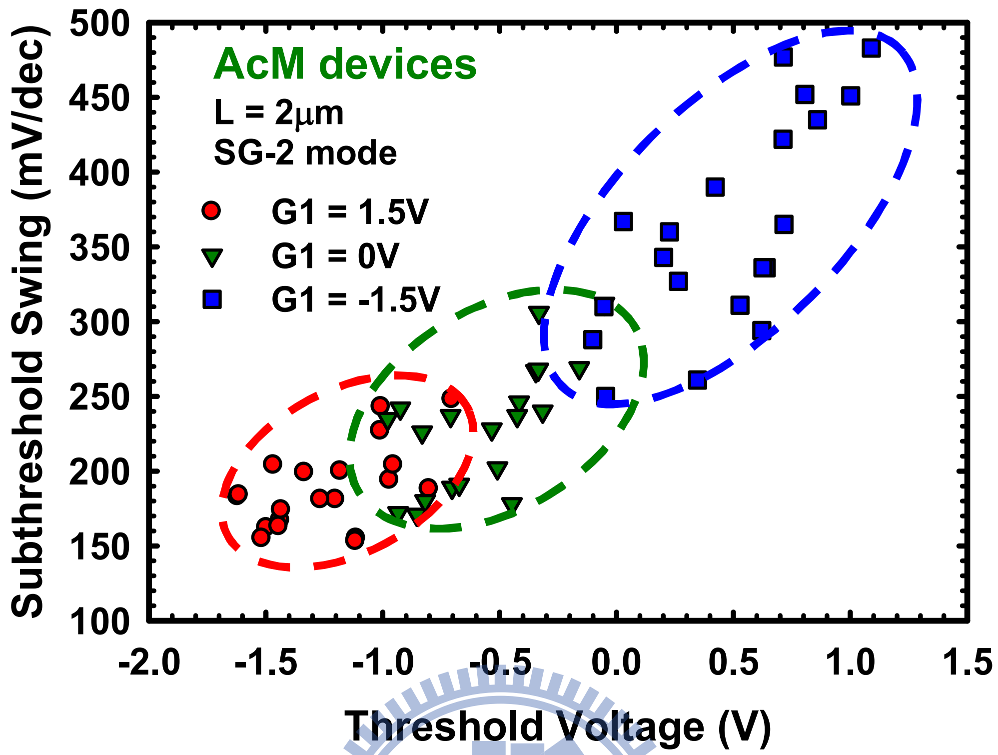
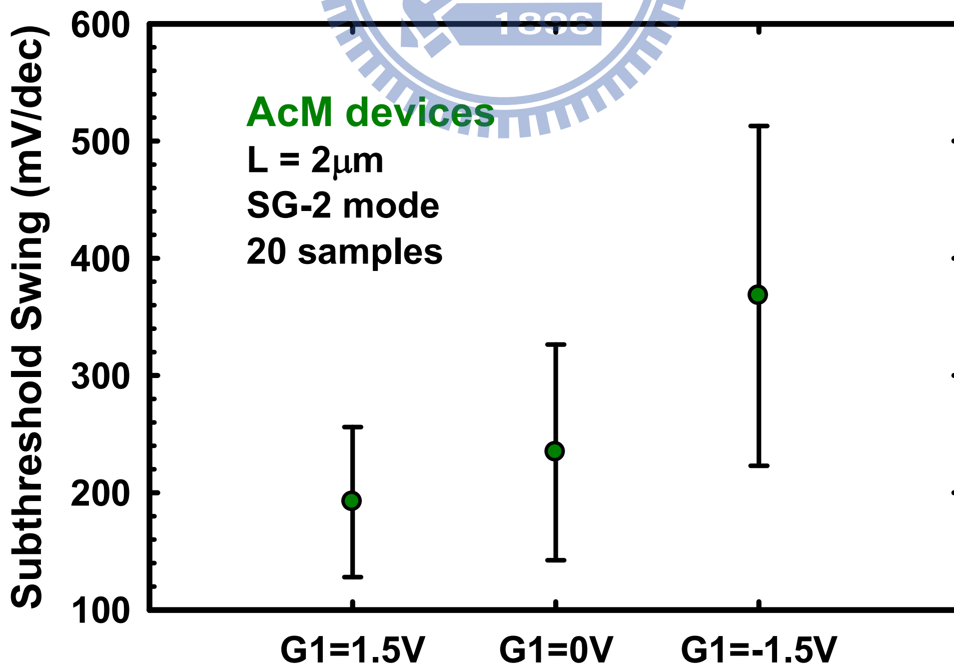


Fig. 3.21. Illustration of the conductive channel and depletion regions of AcM devices at V_g=V_{th} under SG mode with a positive or negative back-gate bias. Since the drain current is constant as V_g=V_{th}, thickness of the conductive channel is roughly a constant, so does the sum of thickness of the two (front- and back-side) depletion regions.

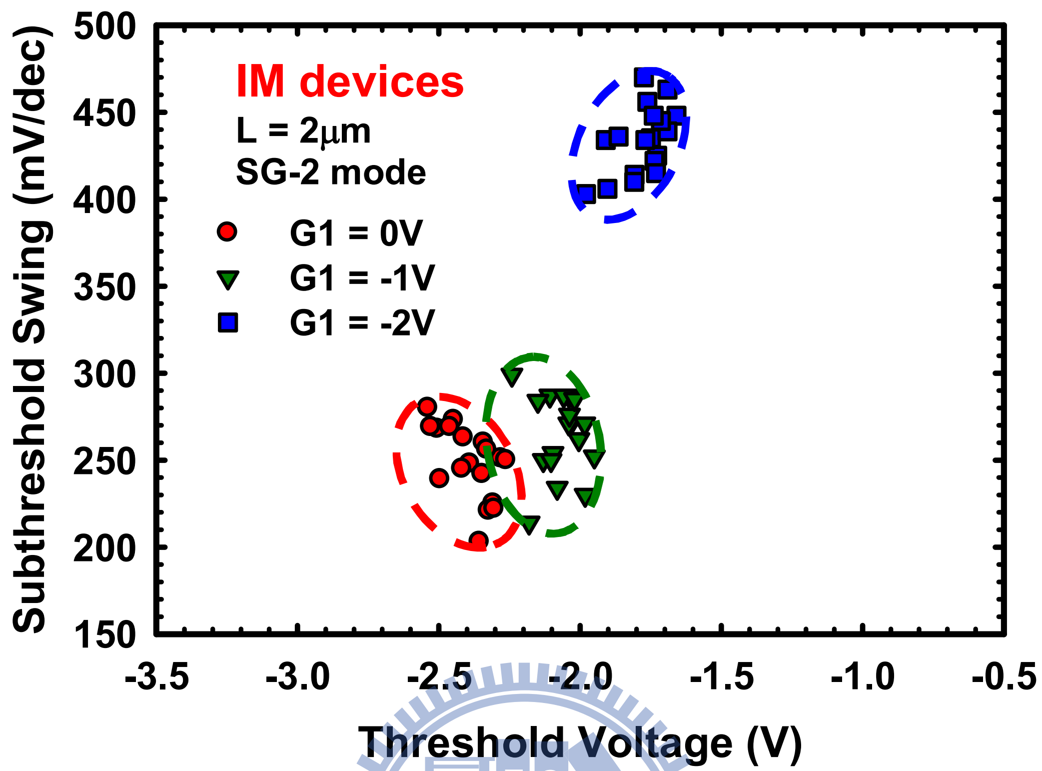


(a)

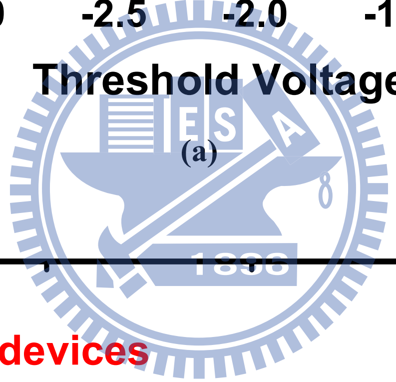


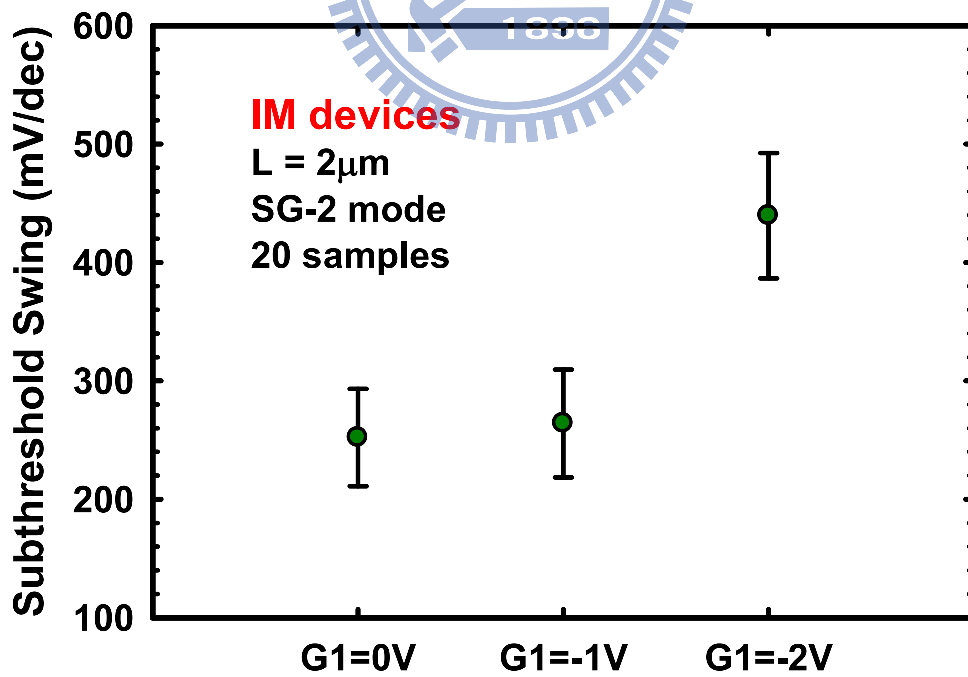
(b)

Fig. 3.22. (a) SS-vs.-V_{th} and (b) distribution of SS measured from 20 AcM devices under SG-2 mode with varying 1st gate bias.



(a)





(b)

Fig. 3.23. (a) SS-vs.-V_{th} and (b) distribution of SS measured from 20 IM devices under SG-2 mode with varying 1st gate bias.

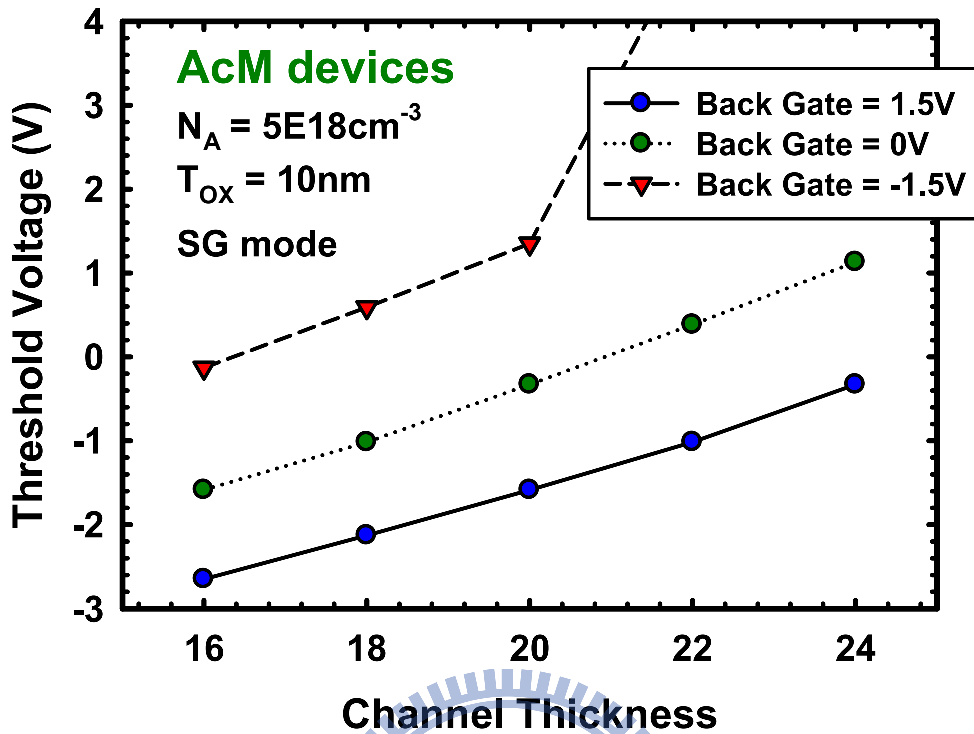


Fig. 3.24. Simulated V_{th} as a function of channel thickness and back-gate bias for AcM devices.

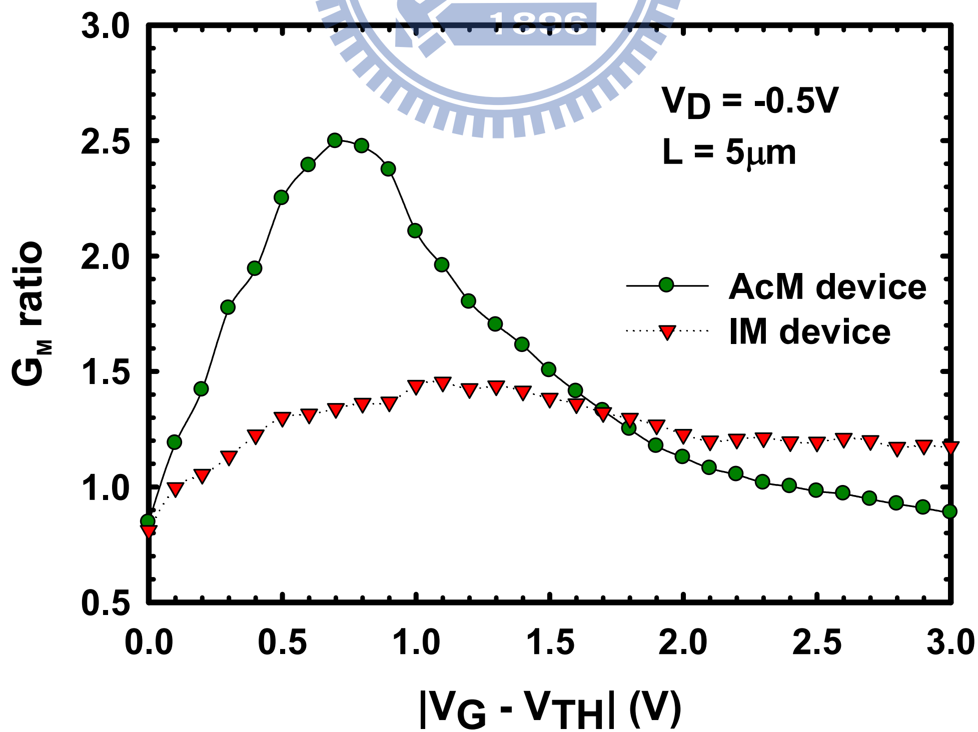
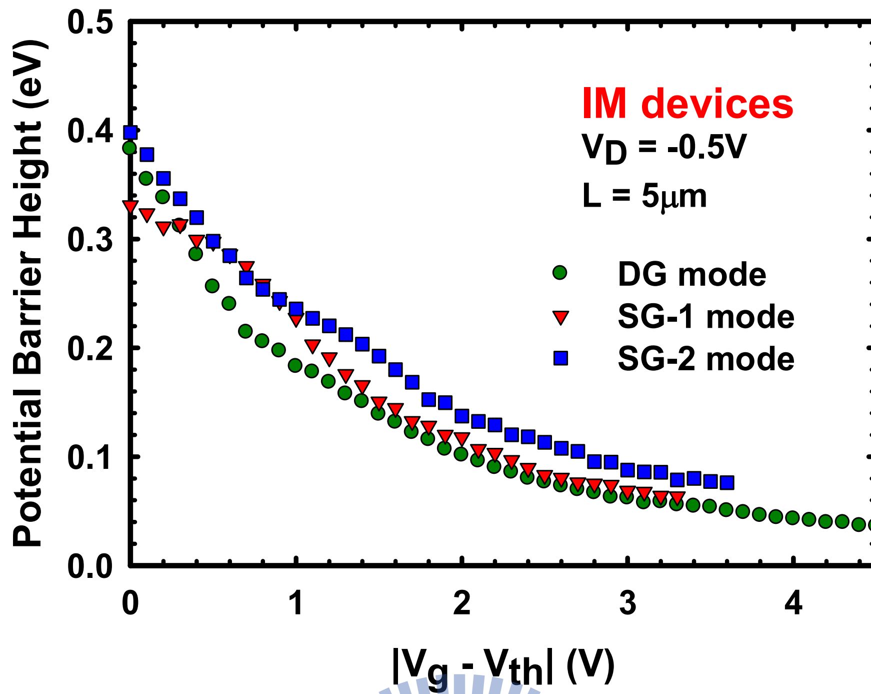
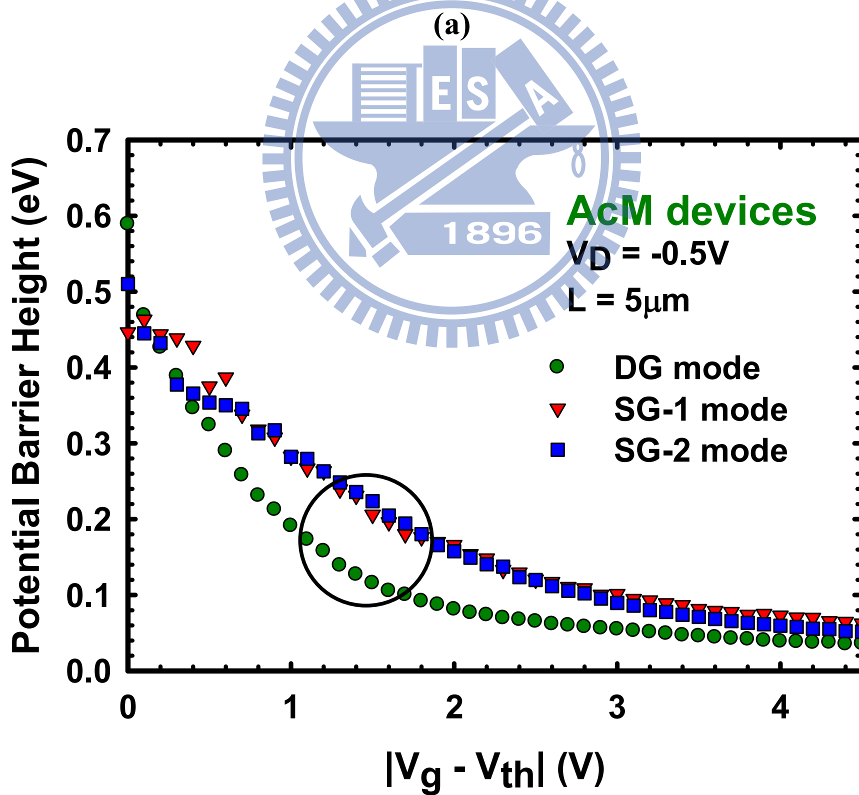


Fig. 3.25. Ratio of transconductance (G_m) under DG mode to the sum of G_m of two SG modes for the two types of devices.



(a)



(b)

Fig. 3.26. Potential barrier height as a function of gate overdrive under the three operation modes for the (a) IM device and (b) AcM device. For the AcM device, the barrier height for DG mode is not only lower than those for SG modes but also decreases more quickly with increasing gate overdrive.

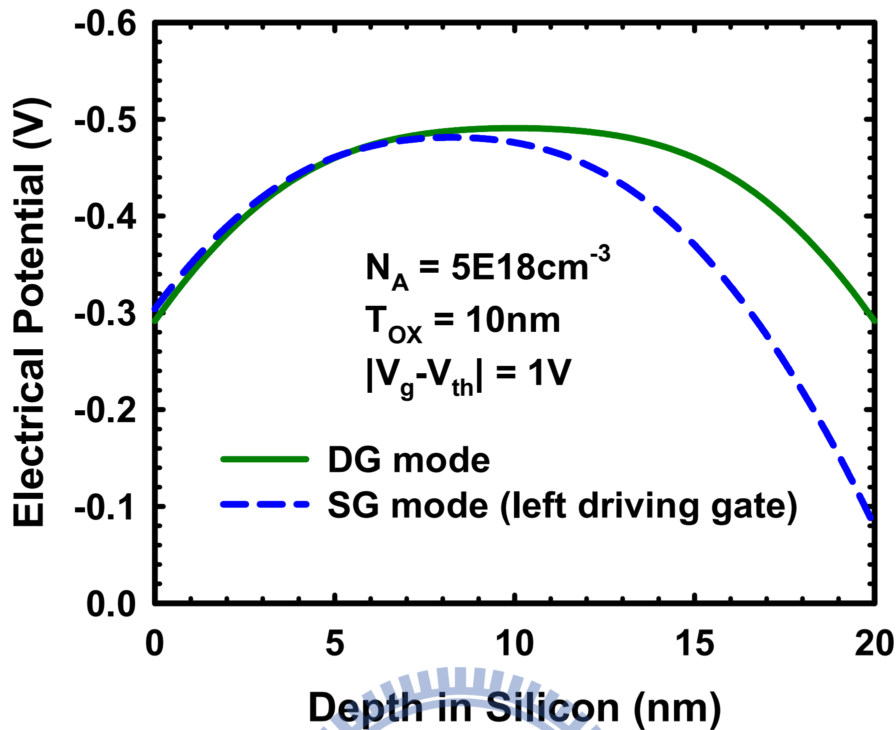


Fig. 3.27. Simulation results of electrical potential along the channel depth under DG and SG modes with the same gate overdrive of 1V for the AcM device.

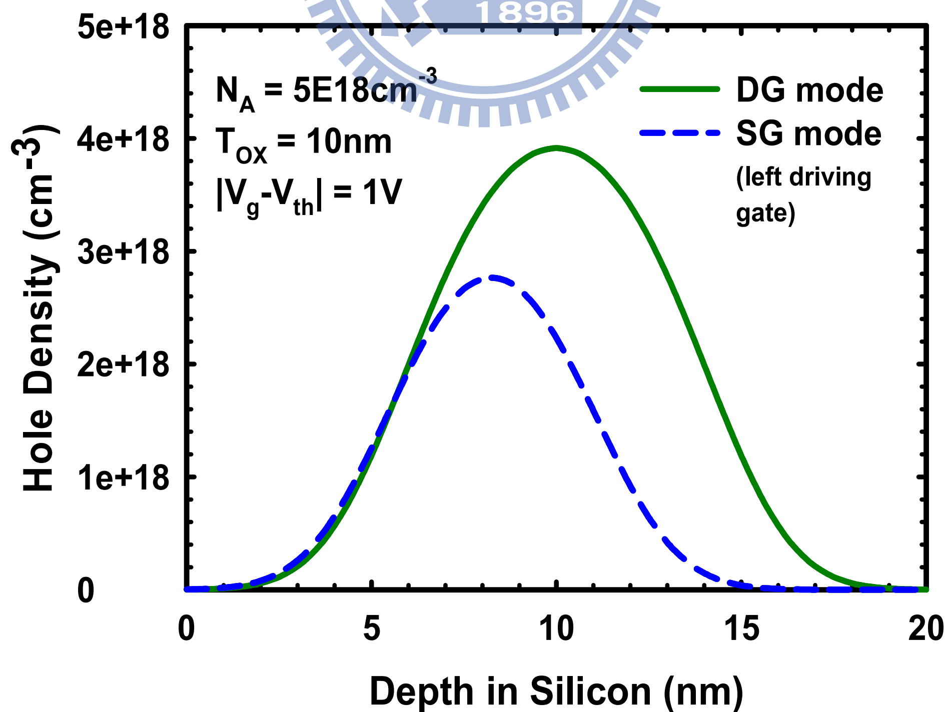


Fig. 3.28. Simulation results of hole density along channel depth under DG and SG modes with the same gate overdrive of 1V for the AcM device.

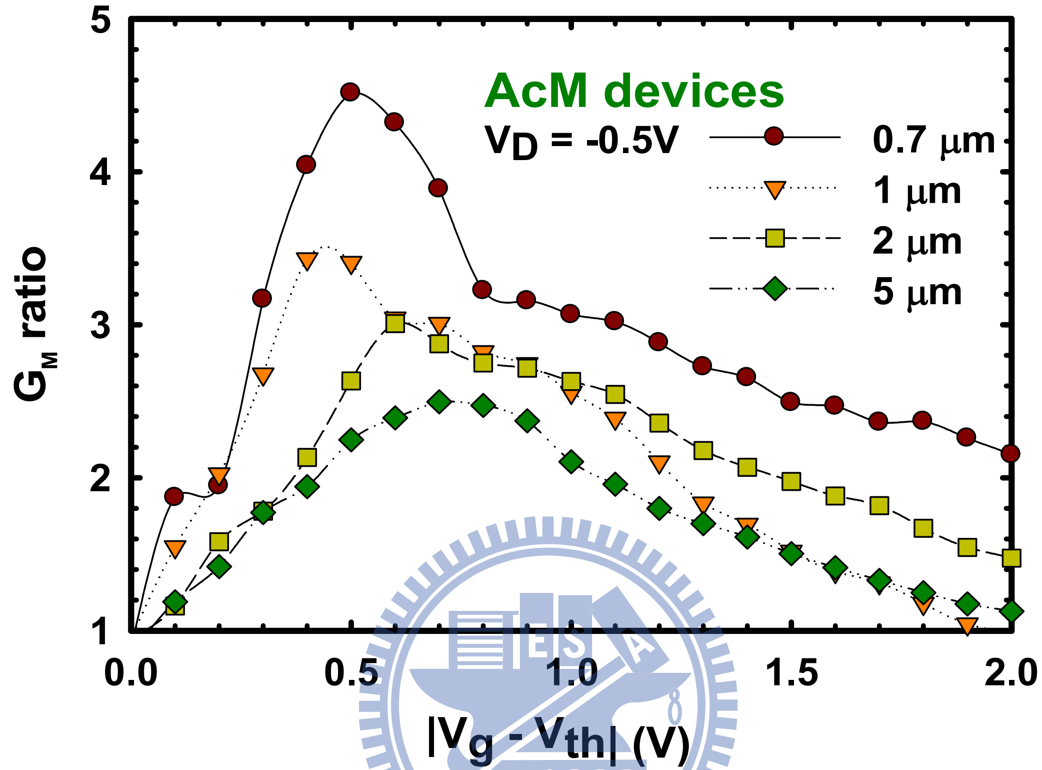
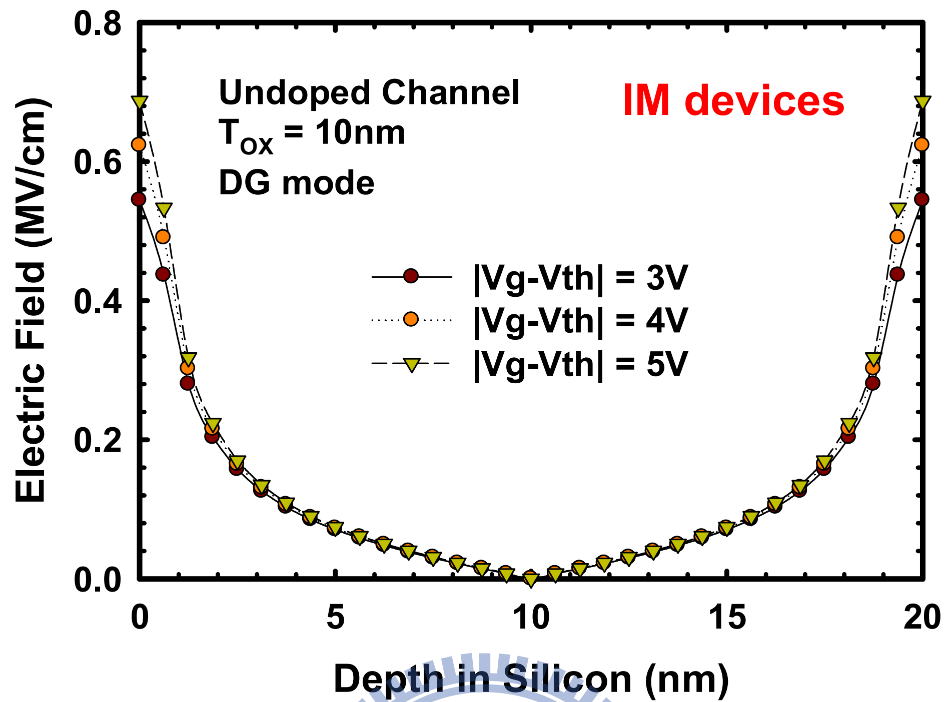
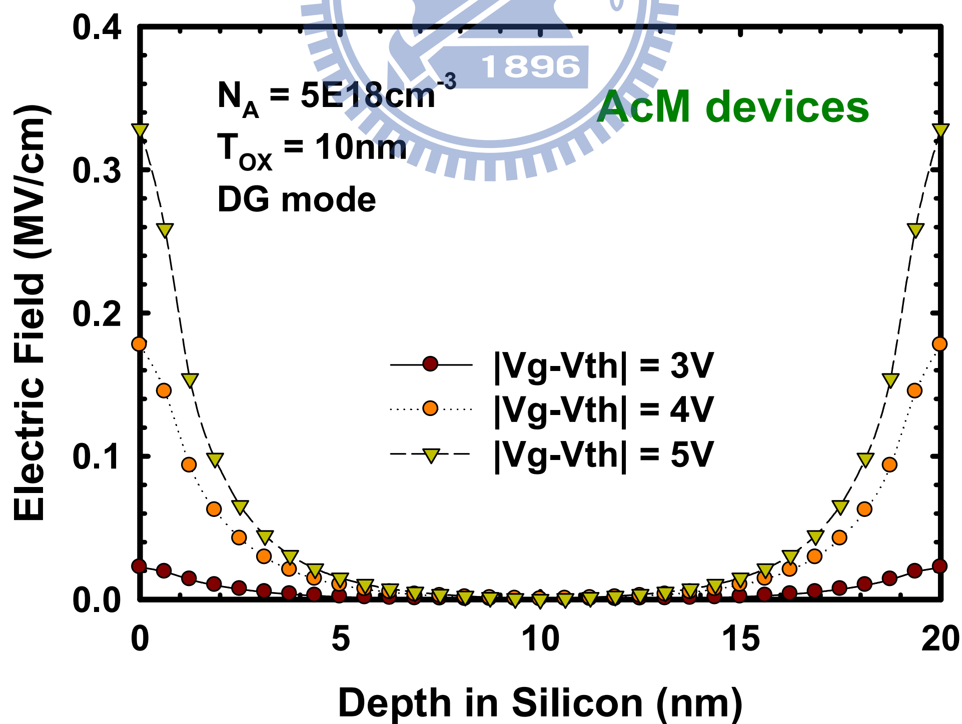


Fig. 3.29. G_m ratio for the AcM devices with different channel lengths. As the channel length gets smaller, the peak value gradually becomes larger.



(a)



(b)

Fig. 3.30. Simulated electric field along channel depth with varying gate overdrive for (a) IM device and (b) AcM device.

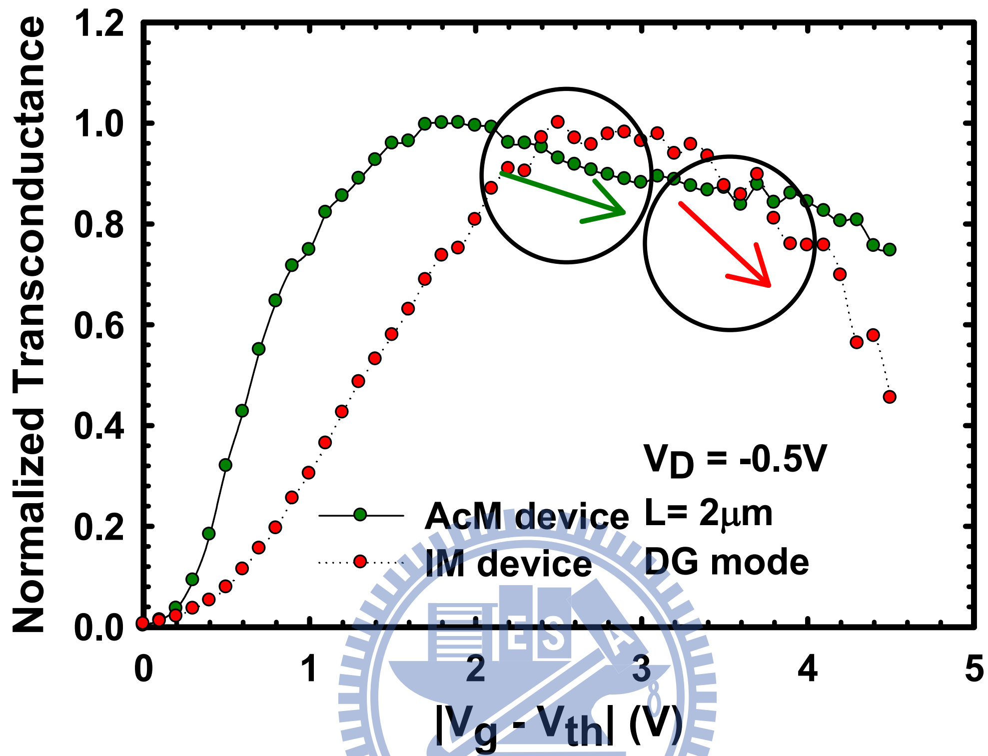


Fig.3.31. Normalized transconductance $G_m/G_{m,max}$ as a function of gate overdrive for the two types of devices. The G_m degradation in high gate overdrive regime is obviously more severe for the IM device.

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論文題目：

具獨立雙閘極之 P 型聚集模式多晶矽奈米線電晶體的製作與特性分析

Fabrication and Characterization of P-Type Accumulation-Mode Independent Double-Gated Poly-Si Nanowire Transistors

Publication List

[1] **<u>Jiun-Peng Wu</u>, Wei-Chen Chen, Horng-Chih Lin, and Tiao-Yuan Huang, "Fabrication and characterization of a p-type junction-free double-gated poly-Si nanowire transistor," *Int. Electron Devices and Materials Symp. (IEDMS)*, Nov 18-19, 2010.**

[2] **<u>Jiun-Peng Wu</u>, Horng-Chih Lin, Zer-Ming Lin and Tiao-Yuan Huang, "Fabrication and characterization of a p-type accumulation-mode independent double-gated poly-Si nanowire transistor," submitted to *IEEE Electron Device Lett.*, 2011.**