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碩　士　論　文

高壓製程靜電放電防護元件設計與其安全操作範圍之研究

Study of Electrostatic Discharge Protection Devices and Their Safe Operating Area in High-Voltage BCD SOI Process

ESA

研 究 生：黃筱晴　　(Hsiao-Ching Huang)

指導教授：柯明道教授 (Prof. Ming-Dou Ker)

中華民國一百年七月

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ABSTRACT (CHINESE)

在智慧型高功率科技中，高壓電晶體已經廣泛運用於顯示器積體電路、電源供應、電源管理，和汽車電子等應用上。然而，隨著製程複雜度的提升以及工作環境日益惡化，高壓積體電路的各種可靠度議題逐漸受到重視，其重要性不容小覷。在許多可靠度的規範守則當中，靜電放電防護 (ESD) 以及安全操作範圍 (SOA) 已成為不可或缺的可靠度議題。為了減少晶片總面積，希冀設計出同時擁有穩健之靜電放電防護能力以及廣大之安全操作範圍的高壓電晶體。因此，本論文旨在探討高壓電晶體之靜電放電防護以及安全操作範圍議題。

本篇論文提出以圓形以及橢圓形之佈局方式呈現橫向擴散金屬氧化物半導體 (LDMOS) ，並實現於 0.5-µm 100-V bipolar CMOS DMOS (BCD) silicon on insulator (SOI) 製程。在許多高壓應用當中，高壓電晶體本身具備抵擋靜電放電之能力是較受歡迎的。因此本文提出於橫向擴散金屬氧化物半導體嵌入矽控整流器 (silicon controlled rectifier, SCR) 以提高靜電放電防護能力。實驗數據顯示，嵌入矽控整流器確實可有效提升靜電放電防護能力。然而，嵌入矽控整流器的相對位置安排對靜電放電防護能力有不可忽視的影響。此外，本文也探討各種佈局參數對於靜電放電防護能力的影響。

雖然嵌入矽控整流器的橫向擴散金屬氧化物半導體擁有極佳的靜電放電防

護能力，但其電性安全操作範圍 (electrical SOA) 嚴重縮小，而且承受未箝制電感性切換 (unclamped inductive switch, UIS) 的能力也大幅降低。此外，本文探討未箝制電感性切換的特性，並發現若橫向擴散金屬氧化物半導體之啟動電流越大，其承受未箝制電感性切換的能力就越好，因此，在未來的未箝制電感性切換之研究中，可朝著研究其啟動電流方向努力

Study of Electrostatic Discharge Protection Devices and Their Safe Operating Area in High-Voltage BCD SOI Process

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1896

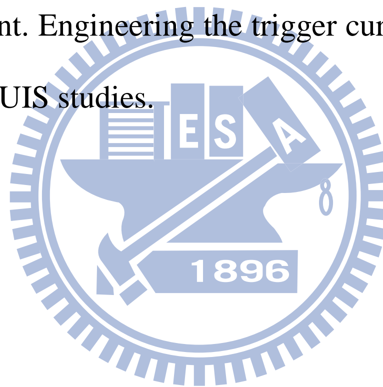
ABSTRACT (ENGLISH)

High-voltage (HV) transistors in smart power technologies have been extensively used for display driver integrated circuits (ICs), power supplies, power management and automotive electronics. The importance of reliability issue should not be underestimated in HV ICs as a result of the process complexity and stringent operating environments. Among the various reliability specifications, electrostatic discharge (ESD) protection and safe operating area (SOA) are becoming the essential issues for HV ICs. A HV transistor simultaneously exhibiting excellent ESD robustness and wide SOA is preferable to minimize the total chip area; hence, the aim of the thesis is to investigate the ESD performance and SOA of HV transistors.

In this thesis, lateral double-diffused metal oxide semiconductor (LDMOS) with circular and elliptic layout shapes are fabricated in a 0.5-μm 100-V bipolar CMOS DMOS (BCD) silicon on insulator (SOI) process. The self-protected HV transistor

against ESD stress is popular in HV applications. The insertion of silicon controlled rectifier (SCR) to LDMOS is proposed to improve the ESD robustness. Experimental results show that it can effectively improve the ESD robustness. However, the arrangement of placing embedded SCR significantly affects the ability to withstand the ESD stress. In addition, the influence of various layout parameters on ESD robustness is studied in the thesis.

Though LDMOS with embedded SCR exhibits excellent ESD robustness, it suffers from a severe degradation of electrical SOA and a poor ability to withstand the unclamped inductive switch (UIS) stress. Besides, the characteristic of UIS is studied and it is discovered that a LDMOS has better ability to withstand the UIS stress when it has a higher trigger current. Engineering the trigger current of LDMOS accordingly can be a direction of future UIS studies.



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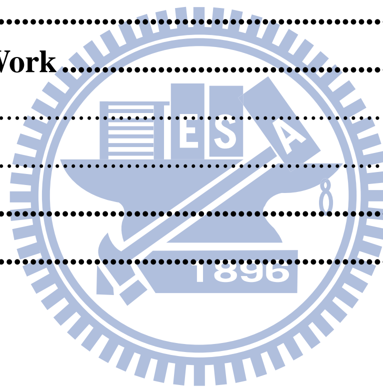

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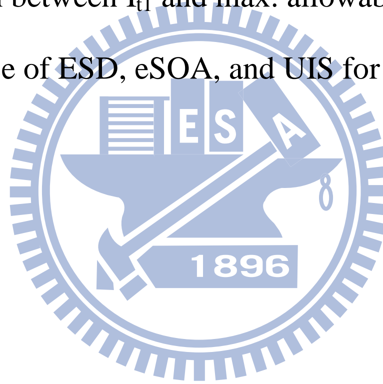

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Chapter 1

Introduction

1.1 Motivation

Recently, the high-voltage (HV) technology is prospering due to its extremely extensive applications such as power management integrated circuits (ICs), automotive electronics, light-emitting diode (LED) and liquid-crystal-display (LCD) driver ICs. The higher breakdown voltage and the higher speed are popular achievements in HV applications [5]-[7]. However, the importance of reliability issue should not be underestimated in HV ICs as a result of stringent operating environments. Furthermore, electrostatic discharge (ESD) protection and safe operating area (SOA) have been essential issues of reliability for HV ICs [8]-[10]. The incident of ESD takes place by accident. On the other hand, SOA is concerned about the reliability during normal circuit operating conditions. The HV transistors simultaneously exhibits excellent ESD robustness and wide SOA is preferable to minimize the total chip area; hence, it is importance to have a deeper investigation on the reliability issue of ESD and SOA. ESD design rules are usually not accepted for the purpose of minimizing the device area; therefore, the self-protected HV ICs against ESD stress is popular in HV applications. The insertion of SCR to lateral double-diffused MOS (LDMOS) is an effective technique in improving the ESD robustness [11]; however, the influence of inserting SCR on SOA is seldom referred. As a result, the deeper research concerning the influence of the embedded SCR structure on SOA is important for LDMOS.

1.2 Investigation on the Impact of Junction Curvature Effect on HV ICs

The influence of curved P/N junction on breakdown voltage is considerable. To predict the breakdown characteristics of curved-abrupt P/N junctions, the junction curvature effect is discussed in this chapter [12]-[14]. The P^+/N-well junction is formed by implanting impurities of p-type into N-well through windows in an impervious masking layer. To activate the impurities of p-type, the thermal process is needed. High temperature results in the diffusion of impurities. Hence, the curved junction is formed as illustrated in Fig. 1-1 where r_j represents the radius of metallurgical junction, x_j represents the distance from surface of silicon to the metallurgical junction, r_d is the radius of outer depletion boundary, x_d is the distance from surface of silicon to the outer depletion boundary. If the shape of masking layer is rectangle as illustrated in Fig. 1-2, the cylindrical curved junction is formed at the edge of mask and the spherical curved junction is formed at the corner of mask. The junction will avalanche breakdown if the junction is reversed bias. The following equations are derived to analysis the relation between avalanche breakdown voltage (BV_{dss}) and r_j.

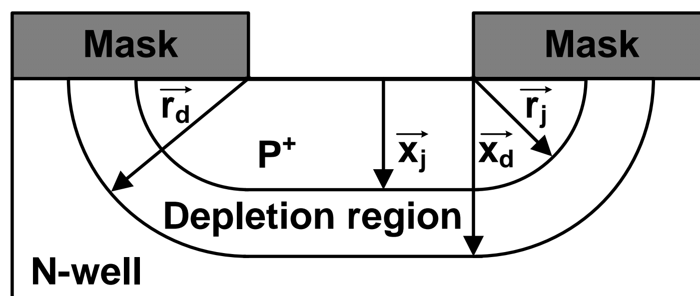


Fig. 1-1. The formation of curved P^+/N-well junction [12].

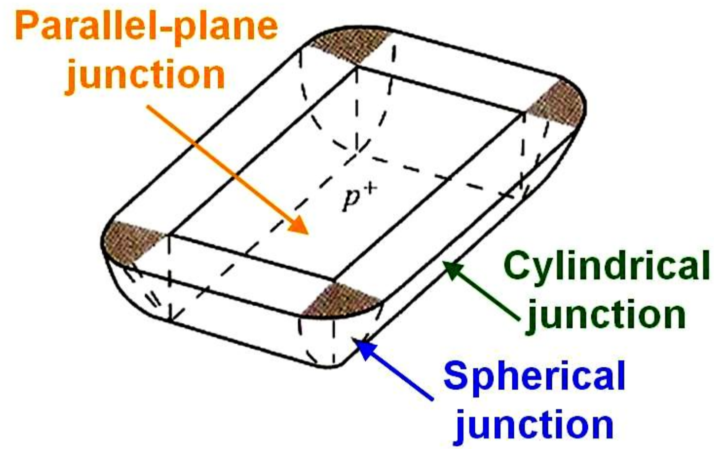


Fig. 1-2. The 3-D diagram of curved P^+/N-well junction [13].

The potential (V) and the electric field (E) in a P/N junction can be calculated from the Poisson's equation, as shown in equation (1.1) [12].

$$\frac{\rho}{\varepsilon} = \frac{1}{r^n}\frac{d(r^n E)}{dr} = -\frac{d^2V}{dr^2} \tag{1.1}$$

where ε is the permittivity of silicon and ρ is the space charge density. n = 0 for parallel-plane junction, n = 1 for cylindrical-junction, and n = 2 for spherical-junction. Hence, the electric field (E) and potential (V) can be written as equation (1.2) and (1.3). In addition, the space charge density of abrupt junction is given by equation (1.4).

$$E(r') = \frac{1}{r^n \varepsilon}\int_{r_d}^{r'} r^n \rho dr + \frac{c}{r^n} \tag{1.2}$$

$$V(r') = -\int_{r_j}^{r'} E dr \tag{1.3}$$

$$\rho(r) = -qN_B \tag{1.4}$$

For parallel-plane junction (n = 0), the electric field and potential can be written as equation (1.5) and (1.6) by replacing the ρ with $-qN_B$.

$$E(x)=\frac{qN_B}{\varepsilon}(x-x_d)+c \tag{1.5}$$

$$V(x)=\frac{qN_B}{2\varepsilon}(x_j^{2}-x^2)+\frac{qN_B x_d}{\varepsilon}(x-x_j) \tag{1.6}$$

For cylindrical-abrupt junction (n = 1), the electric field and potential can be written as equation (1.7) and (1.8) by replacing the ρ with $-qN_B$.

$$E(r)=\frac{qN_B}{2\varepsilon}\frac{(r^2-r_d^{2})}{r}+\frac{c}{r} \tag{1.7}$$

$$V(r)=\frac{qN_B}{2\varepsilon}\left[\frac{(r_j^{2}-r^2)}{2}+r_d^{2}\ln\left(\frac{r}{r_j}\right)\right] \tag{1.8}$$

For spherical-abrupt junction (n = 2), the electric field and potential can be written as equation (1.9) and (1.10) by replacing the ρ with $-qN_B$.

$$E(r)=\frac{qN_B}{3\varepsilon}\frac{(r^3-r_d^{3})}{r^2}+\frac{c}{r^2} \tag{1.9}$$

$$V(r)=\frac{qN_B}{3\varepsilon}\left[\frac{(r_j^{2}-r^2)}{2}+r_d^{3}\left(\frac{1}{r_j}-\frac{1}{r}\right)\right]+c\left(\frac{1}{r}-\frac{1}{r_j}\right) \tag{1.10}$$

To simplify the calculation, the cylindrical-abrupt and spherical-abrupt junctions are transferred to parallel-plane abrupt junction through N_{eq} and W_{eq} [14]. N_{eq} is the background doping concentration of equivalent parallel-plane abrupt junction. W_{eq} is the depletion width of equivalent parallel-plane abrupt junction. There are three

assumptions shown as following to obtain N_{eq} and W_{eq}.

(1) The original and equivalent junctions are in the avalanche breakdown state.

(2) The total net charge in the depletion region is conserved during breakdown.

(3) The voltage is conserved during breakdown.

As a result, the E_{max} and BV_{dss} can be respectively written as equation (1.11) and (1.12) [14].

$$E_{max} = \frac{qN_{eq}W_{eq}}{\varepsilon} \tag{1.11}$$

$$BV_{dss} = \frac{qN_{eq}W_{eq}^{2}}{2\varepsilon} \tag{1.12}$$

The maximum electric field is located at the metallurgical junction while the maximum potential is located at the depletion outer boundary. For cylindrical-abrupt junction, combining the equation (1.7) and (1.11), the E_{max} can be written as equation (1.13); combining the equation (1.8) and (1.12), the BV_{dss} can be written as equation (1.14) for cylindrical junction. Similarly, the E_{max} and BV_{dss} can be respectively written as equation (1.15) and (1.16) for spherical junction.

$$E_{max} = \left|E(r_j)\right| = \frac{qN_B}{2\varepsilon}\frac{(r_d^{2} - r_j^{2})}{r_j} = \frac{qN_{eq}W_{eq}}{\varepsilon} \tag{1.13}$$

$$BV_{dss} = V(r_d) = \frac{qN_B}{2\varepsilon}\left[\frac{(r_j^{2} - r_d^{2})}{2} + r_d^{2}\ln\left(\frac{r_d}{r_j}\right)\right] = \frac{qN_{eq}W_{eq}^{2}}{2\varepsilon} \tag{1.14}$$

$$E_{max} = \left|E(r_j)\right| = \frac{qN_B}{3\varepsilon}\frac{(r_d^{3} - r_j^{3})}{r_j^{2}} = \frac{qN_{eq}W_{eq}}{\varepsilon} \tag{1.15}$$

$$BV_{dss} = V(r_d) = \frac{qN_B}{3\varepsilon}\left[\frac{(r_j^2 - r_d^2)}{2} + r_d^3\left(\frac{1}{r_j} - \frac{1}{r_d}\right)\right] = \frac{qN_{eq}W_{eq}^2}{2\varepsilon} \tag{1.16}$$

According to the assumption (1), the relation between N_{eq}, W_{eq}, and BV_{dss} is given as equation (1.17) and (1.18) [12].

$$N_{eq} = 9.3 \times 10^{11} \times W_{eq}^{(-8/7)} \tag{1.17}$$

$$BV_{dss} = 6.4 \times 10^{13} \times N_{eq}^{(-3/4)} \tag{1.18}$$

It is necessary to solve the combinational group of equation (1.13), (1.14) and (1.17) to get N_{eq}, W_{eq}, and r_d with given N_B and r_j for cylindrical-abrupt junction. BV_{dss} is calculated by equation (1.18) and N_{eq}. For spherical-abrupt junction, we can get the N_{eq}, W_{eq}, r_d, BV_{dss} by equation (1.15), (1.16), (1.17), and (1.18). Fig. 1.3 demonstrates the calculating value of breakdown voltage with different r_j and N_B for cylindrical-abrupt junction and parallel-plane junction; likewise, Fig. 1.4 demonstrates that for spherical-abrupt junction and parallel-plane junction. It is observed that the breakdown voltage of cylindrical-abrupt junction and spherical-abrupt junction approaches that of parallel-plane junction with longer r_j. In other words, the curved junction is similar to parallel-plane junction when the radius of metallurgical junction is large enough. With the same r_j and N_B, parallel-plane junction exhibits the largest BV_{dss} while the BV_{dss} of spherical-abrupt junction is the smallest. In other words, the spherical-abrupt junction is prone to breakdown among the junctions discussed above. Furthermore, BV_{dss} decrease with decreasing r_j both for cylindrical-abrupt and spherical-abrupt junctions. As a result, the radius of spherical-abrupt junction dominates the BV_{dss} for HV transistors.

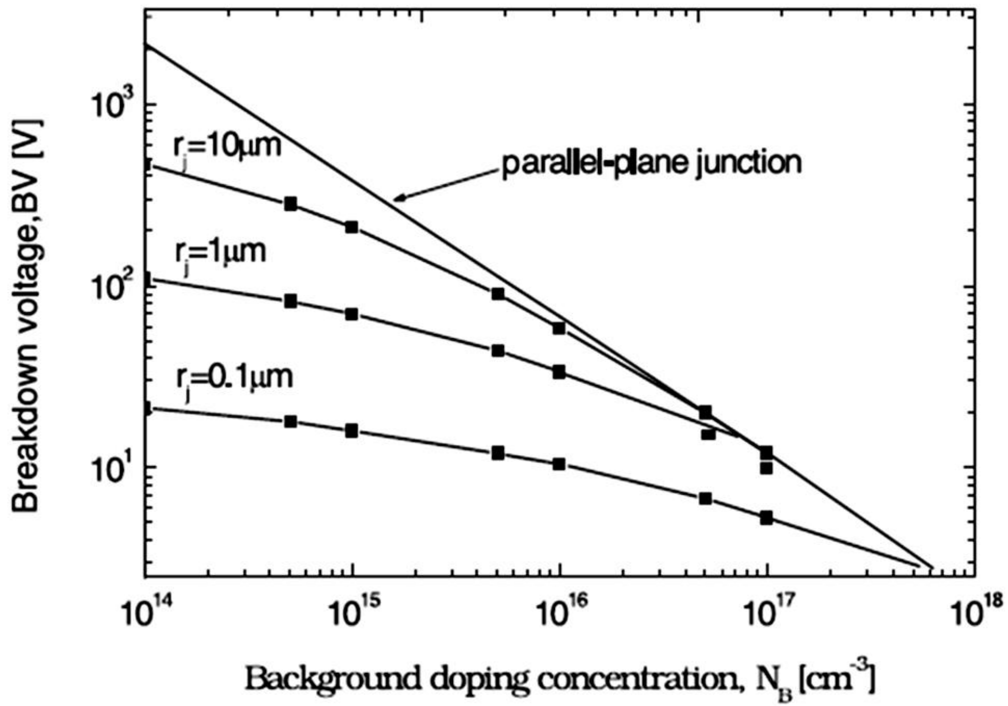


Fig. 1-3. The avalanche breakdown voltage versus background doping concentration for different r_j of the cylindrical-abrupt junction [14].

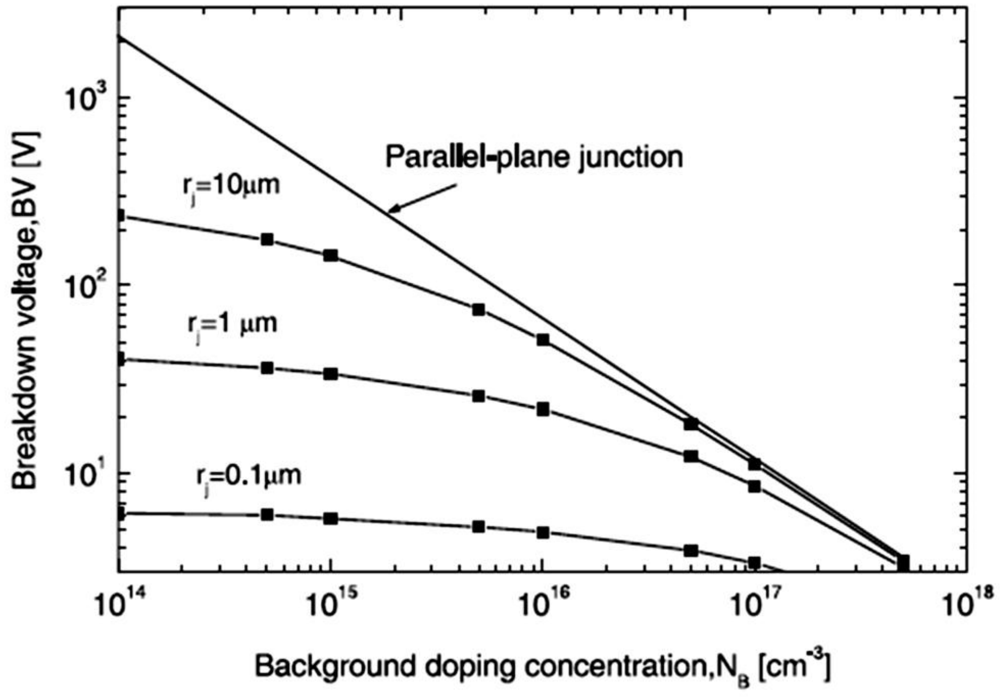


Fig. 1-4. The avalanche breakdown voltage versus background doping concentration for different r_j of the spherical-abrupt junction [14].

1.3 Thesis Organization

The chapter 1 of this thesis is the motivation of the research and the introduction of junction curvature effect.

The chapter 2 of this thesis includes the device structure of standard LDMOS and the modified LDMOS which is studied in the work. The experimental results comprise the DC I_{DS}-V_{DS} characteristics and the avalanche breakdown voltage.

The chapter 3 of this thesis introduces ESD events and ESD test methods. The experiment includes the TLP, MM, HBM, and failure analysis. The ESD performance with different device structures is discussed, and the causing of poor ESD robustness is discovered according to the failure analysis.

The chapter 4 of this thesis investigates the measured methods and properties of safe operating area (SOA). The classification of SOA is concisely introduced in the chapter. The characteristic of unclamped inductive switch (UIS) is investigated in detail. The experimental results include electrical SOA and UIS for standard nLDMOS and modified nLDMOS. The causing of wide eSOA and excellent UIS level is discussed.

The chapter 5 of this thesis refers to the methods to improve the SOA without paying for the poor ESD robustness.

In the end of this thesis, a short conclusion and future work are given in the chapter 6.

Chapter 2

Proposed Device Structure Designs of LDMOS

2.1 The Standard Device Structure of LDMOS

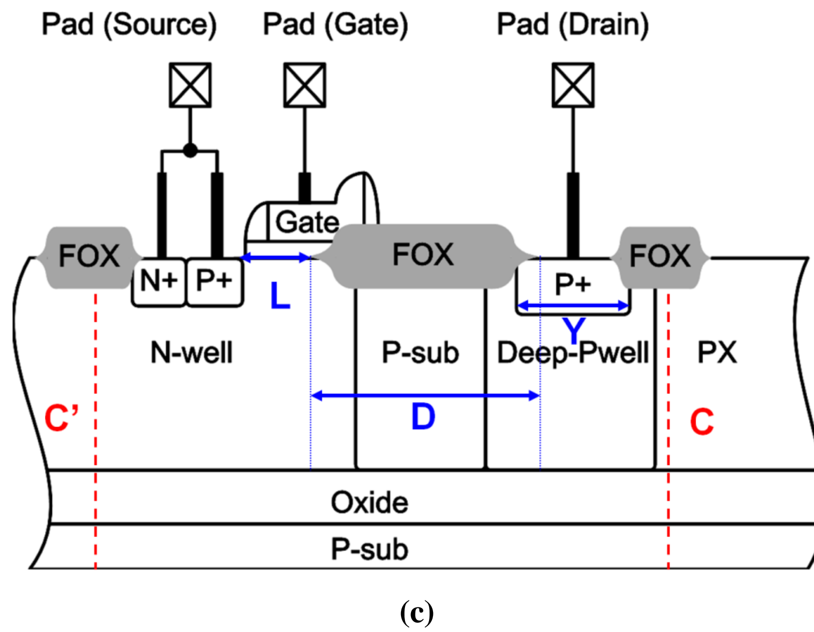
Fig. 2-1 shows the cross-sectional view of LDMOS which is realized in a 0.5-μm 100-V SOI BCD process. The depth of buried oxide is 2 μm, gate oxide is 15 nm, field oxide is 570 nm, and active region is 3 μm. The devices are separated from each other by trench isolation and buried oxide which can minimize the device area. To prevent the current from concentrating at the device surface, the sheet resistance of PM is larger than HV N-Well to disperse the current. According to the principle of RESURF, HV N-Well is fully depleted with the aid of PM, buried oxide, and P-sub [15] [16].

Radius of spherical P/N junction dominates the breakdown voltage according the curvature junction effect [12]-[14]. Fig. 2-2 shows three types of mask results in different radius of spherical P/N junction. Region in gray color represent the mask and outer region represents the junction after diffusion. The shape of mask in type A is a rectangle and the spherical P/N junctions with the smallest radius (r_A) are formed at the corner. The shape of mask in type B is a rectangle with half circle at top and bottom. In this thesis, the substitutive name of shape in type B is elliptic shape. The radius of spherical P/N junction in type B (r_B) is medium. The shape of mask in type C is a rectangle with one third of circle at top and bottom. The radius of spherical P/N junction of type C (r_C) is the longest, but the electric charges accumulates at the sharp corner which lead to a reduction of avalanche breakdown voltage. In conclusion, the shape of mask in type B has the highest avalanche breakdown voltage. Fig. 2-3 shows

the proposed layout styles of LDMOS. In this thesis, the LDMOS are in elliptic layout style except for circular_nLDMOS. The definitions of layout parameters are shown in Fig. 2-1 and Fig. 2-3. W is the channel width. The channel width of circular_nLDMOS is 2πr. D represents the drift length. e is the clearance between the contact edge and the center of circle. x is the clearance between the contact and the FOX at drain region while s is the clearance between the contact and the polygate at source region.

(a)

(b)



(c)

Fig. 2-1. The cross-sectional view of (a) nLDMOS, (b) circular_nLDMOS, and (c) pLDMOS.

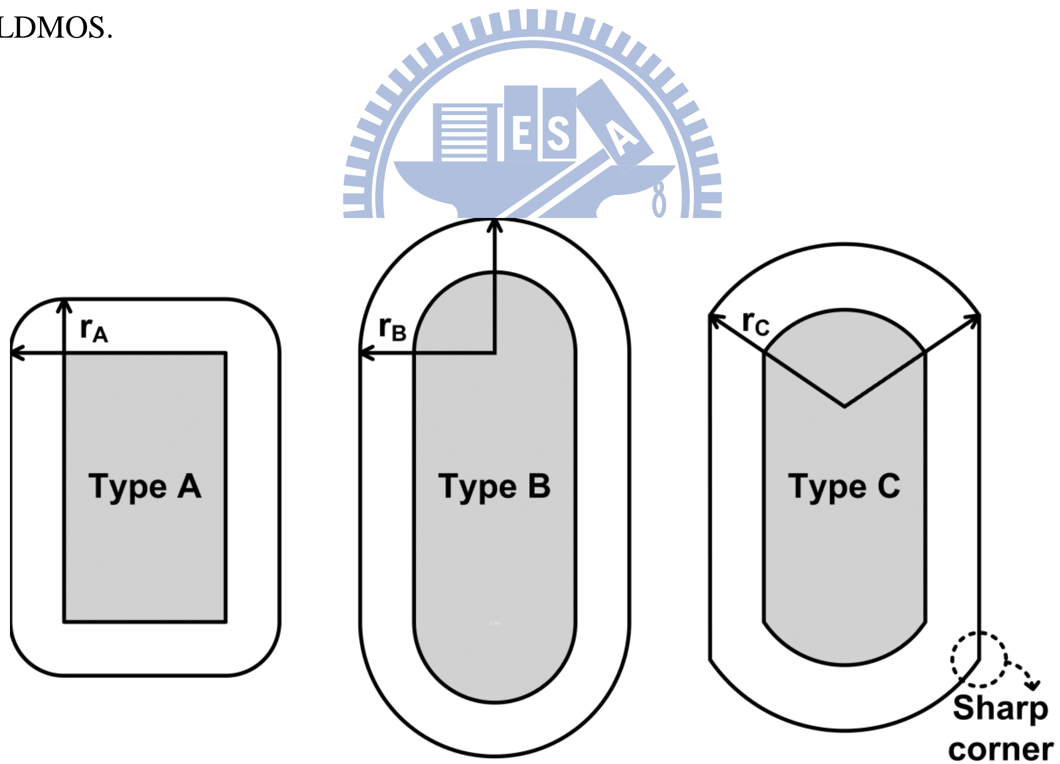


Fig. 2-2. Top view of diffused junction through three types of mask.

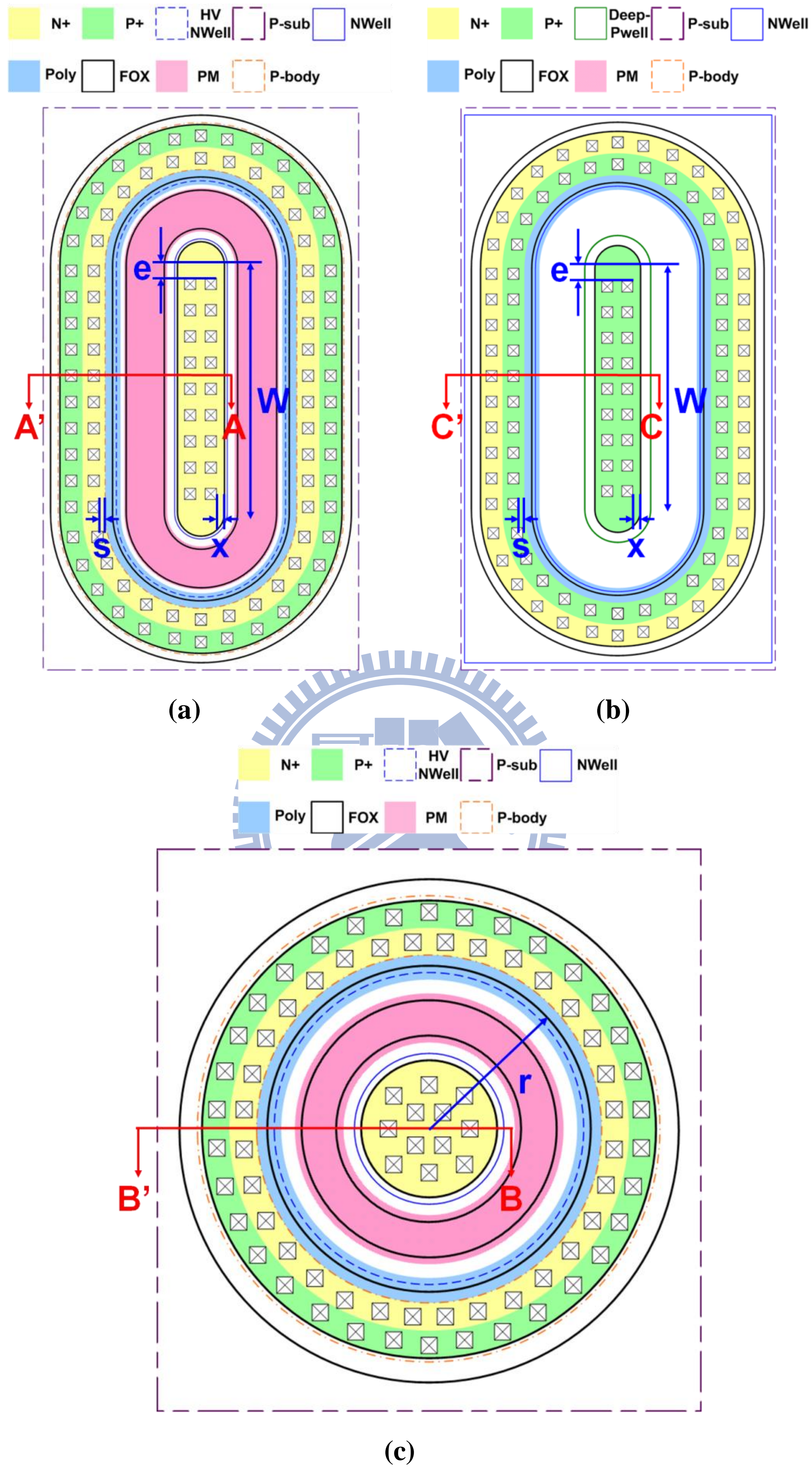


Fig. 2-3. Top view of (a) nLDMOS (b) pLDMOS in elliptic shape and (c) circular_nLDMOS in circular shape.

The field oxide (FOX) under the poly gate plays an important role [17]. Fig. 2-4 demonstrates P/N junction below gate oxide under the condition of reversed bias. W_d is the depletion width of P/N junction and t_{ox} is the thickness of oxide. Electric filed is shown in dashed line with arrow. For $t_{ox} < W_d$, the maximum electric filed occurs in the oxide and the oxide would be catastrophically damaged when the maximum electric field is equal to critical electric field. Numerical analysis has shown that the avalanche breakdown occurs in the oxide for W_d/t_{ox} higher than 12 [18]. As a result, the FOX is utilized to keep the ratio lower than 12 for LDMOS.

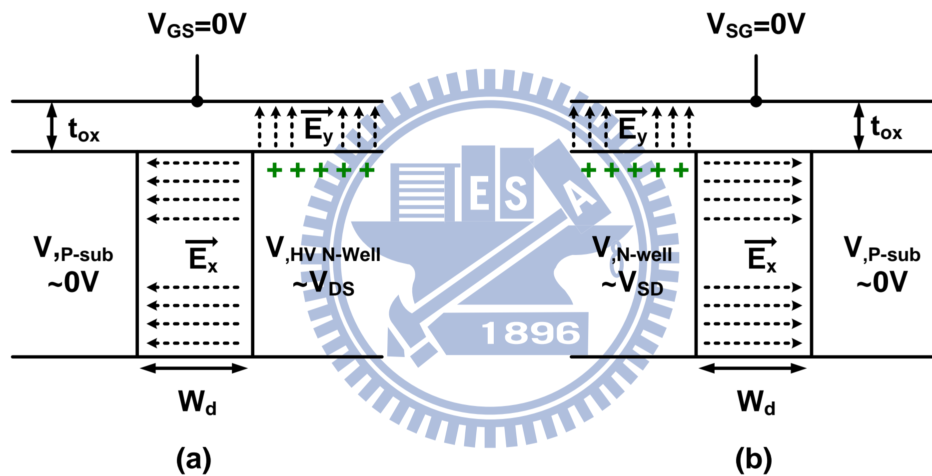


Fig. 2-4. The P/N junction of (a) nLDMOS and (b) pLDMOS below gate oxide under the condition of reversed bias: (a) $V_{DS} > 0$ V and $V_{GS} = 0$ V. (b) $V_{SD} > 0$ V and $V_{SG} = 0$ V.

The operating voltage of drain to source (V_{DS}) is 100 V and the operating voltage of gate to source (V_{GS}) is 5 V. To consider the gate-oxide reliability, the voltage across drain and gate (V_{DG}) can't be higher than V_{DD} for a long time. The protective low-voltage MOS (LV MOS) is added to prevent the gate oxide of high-voltage MOS

(HV MOS) form damage, as illustrated in Fig. 2-5. If V_{DG} is accidentally higher than V_{DD}, the parasitic diode of LV MOS will turn on and clamp V_{DS} to V_{DD}. The parasitic diode of LV MOS doesn't affect the normal operation of HV MOS because it is off during normal operation.

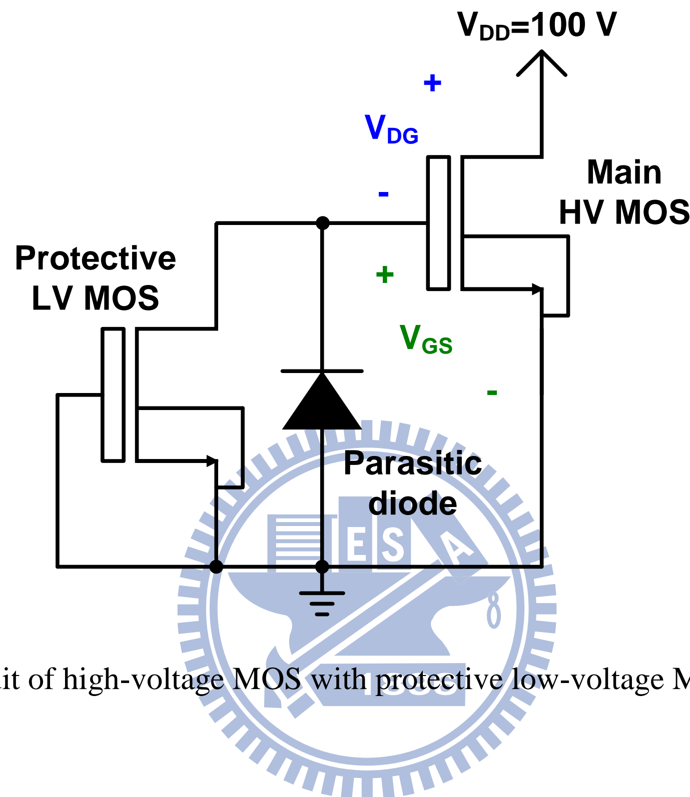


Fig. 2-5. Circuit of high-voltage MOS with protective low-voltage MOS.

2.2 The Device Structure of LDMOS with embedded SCR

The insertion of silicon controlled rectifier (SCR) to MOS is a popular technique to improve ESD robustness [11]. Fig. 2-6 shows the LDMOS with embedded SCR. SCR-nLDMOS and SCR-pLDMOS respectively represents the n-type and p-type LDMOS with embedded SCR. The current path of SCR and BJT are respectively located at the side and the center of drain region for SCR-LDMOS_A, as illustrated in Fig. 2-6 (a) and (c). SCR-LDMOS_B alters the relative position of N+ and P+ at drain region, so the orientation of BJT and parasitic SCR is changed as illustrated in Fig. 2-6 (b) and (d). The influence of the embedded SCR structures on the ESD and SOA of LDMOS is one of the important topics in the thesis. The definitions of layout

parameters are shown in Fig. 2-6. The definitions of W, D, and e are the same as illustrated in Fig. 2-1 and Fig. 2-3. z is the clearance between the contact and the FOX at drain region for SCR-nLDMOS. s is the clearance between the contact and the polygate at source region for SCR-nLDMOS. The similar definitions of SCR-pLDMOS are illustrated in Fig. 2-6 (c) and Fig. 2-6 (d).

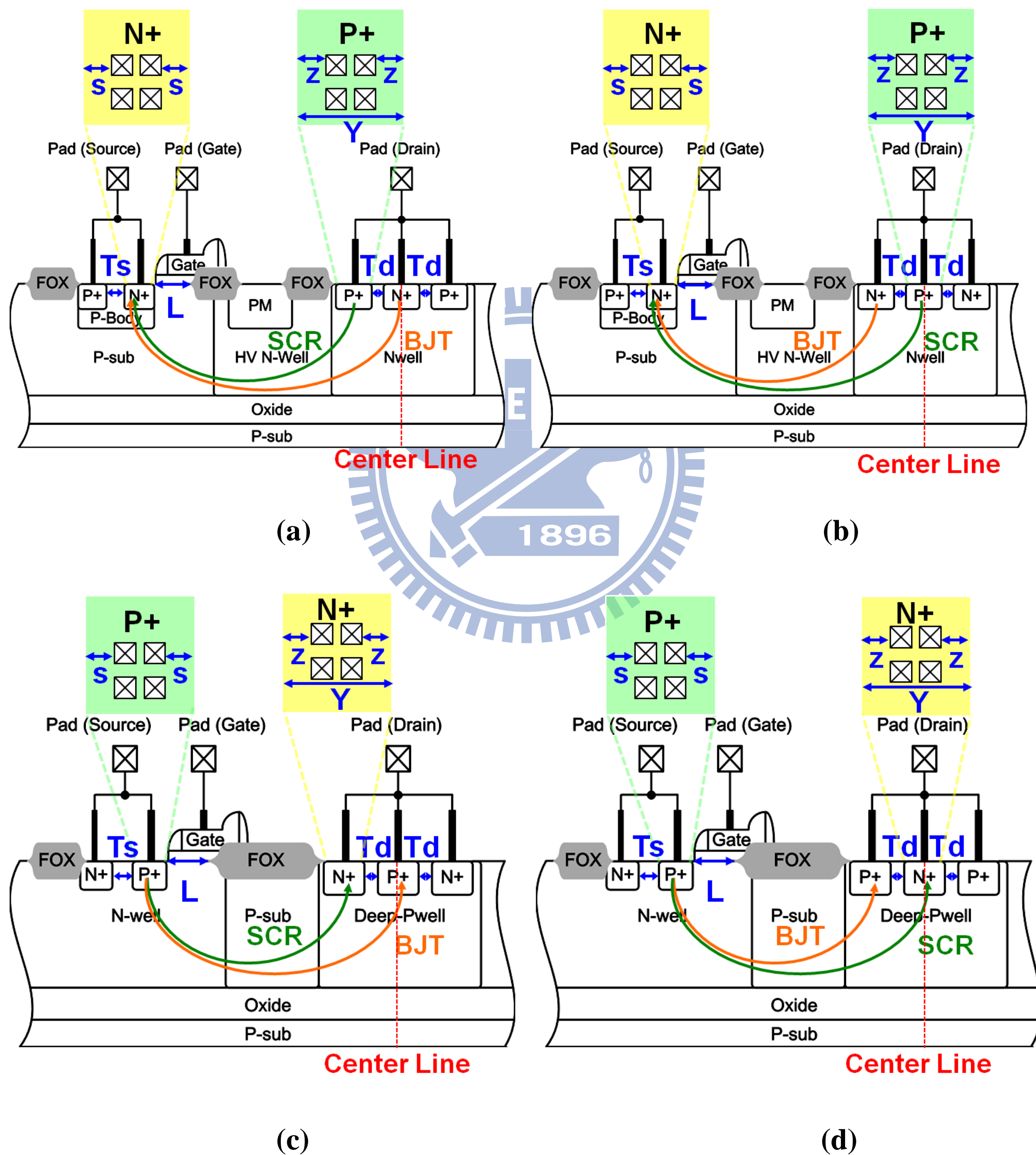


Fig. 2-6. The cross-sectional view of (a) SCR-nLDMOS_A (b) SCR-nLDMOS_B (c) SCR-pLDMOS_A (d) SCR-pLDMOS_B.

2.3 I_{DS}-V_{DS} Characteristics

Fig. 2-7 demonstrates the DC I_{DS}-V_{DS} characteristics of nLDMOS with W = 40 μm, L = 2 μm, D = 12 μm, Y = 13 μm, x = 6 μm, s = 1 μm, and e = 2 μm. The gate bias voltage is varied from 0 V to 5 V. The higher V_{GS} results in higher I_{DS} at the same V_{DS}. However, the negative differential output resistance is observed at high V_{DS} region. It was reported that the reduction of I_{DS} at high V_{DS} region arose from self-heating effect [19]. At saturation region, the carriers are travelling at the saturated velocity in the drift region. The lattice temperature increases as a result of power dissipation. The high lattice temperature causes a severe degradation of carrier mobility [20]; hence, the travelling velocity is smaller. As a result, the drain current decreases with increasing drain voltage. Fig. 2-8 shows the I_{DS}-V_{DS} characteristics of a SOI LDMOS with the 50-μm drift length, the 0.2-μm silicon thin-film, the 1.2-μm buried oxide, and the 0.3-mm^2 device area [19]. The experimental results reveal that the self-heating effect is serious under DC condition while it is unapparent under 2-μs power pulse condition. It is due to the higher lattice temperature which results from higher power dissipation under DC condition.

Fig. 2-9 and Fig. 2-10 demonstrate the DC I_{DS}-V_{DS} characteristics of all typical HV DMOS whose layout parameters are listed in Table 2.1. The range of gate bias is from 0 V to 5 V. SCR-nLDMOS_A tends to snapback at small V_{DS} when the gate bias is larger than 2.4 V, so the measurement is done under the condition of V_{GS}=0 V~2.4 V. Because the mobility of N-type carrier is larger than that of P-type carrier in nature, the drain current of N-type DMOS are larger than that of P-type DMOS at the same absolute value of V_{GS}.

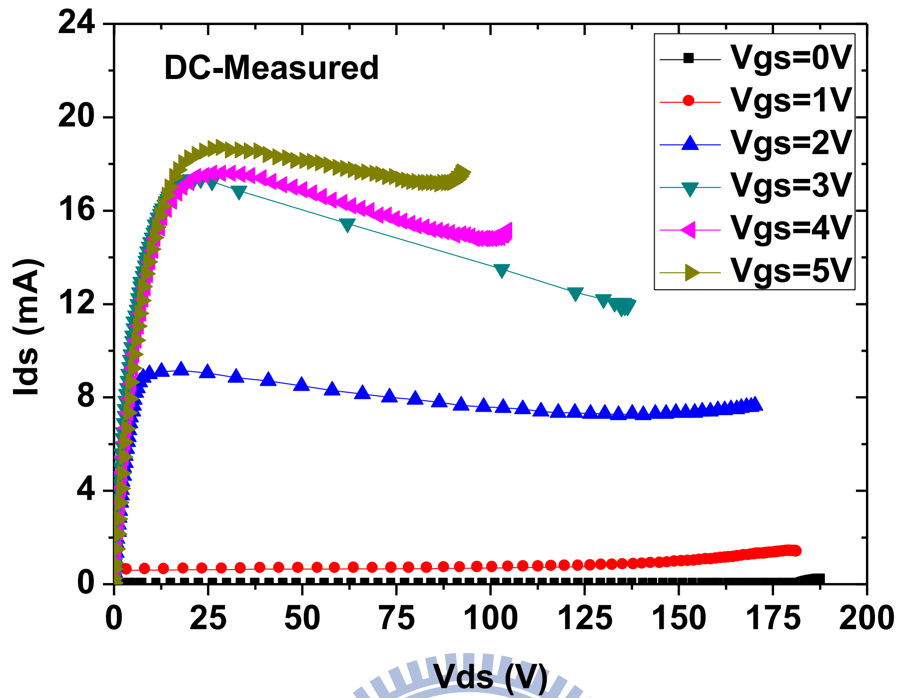


Fig. 2-7. The DC I_{DS}-V_{DS} characteristics of nLDMOS with V_{GS} = 0 ~ 5 V.

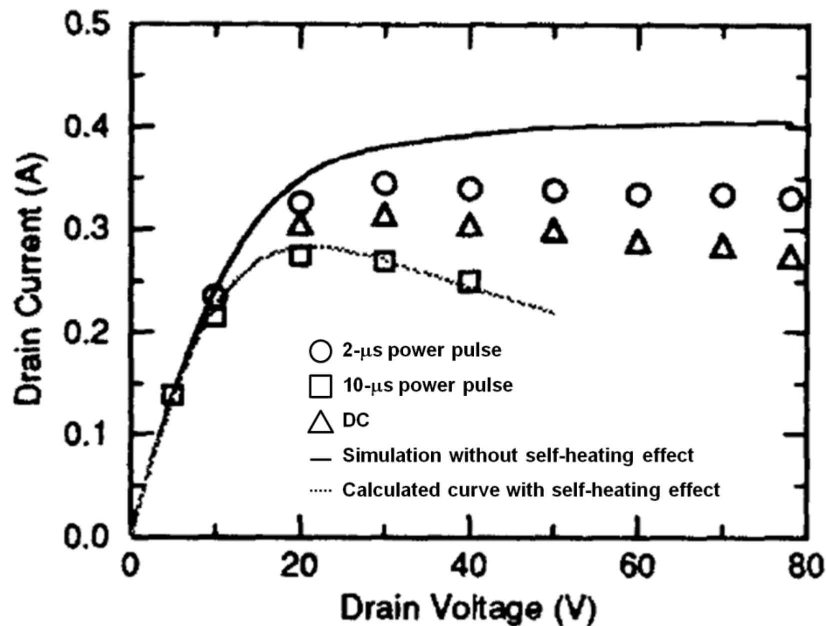
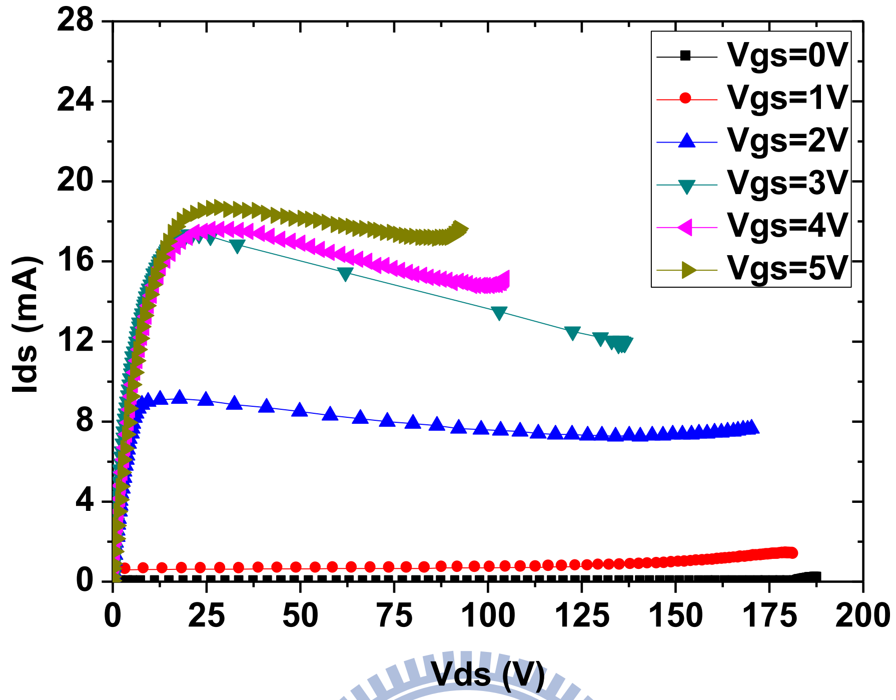
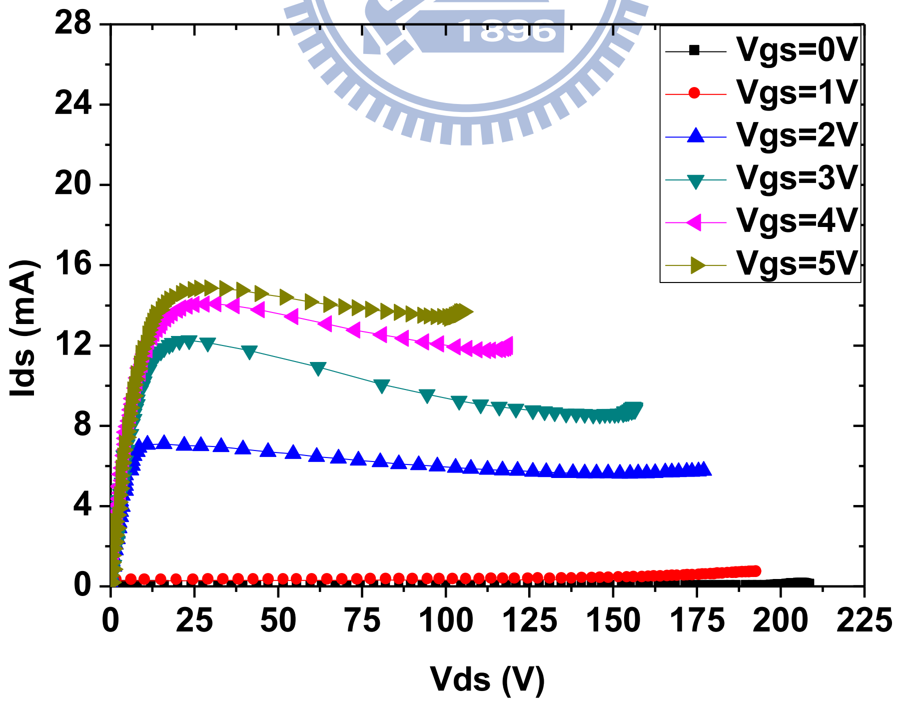


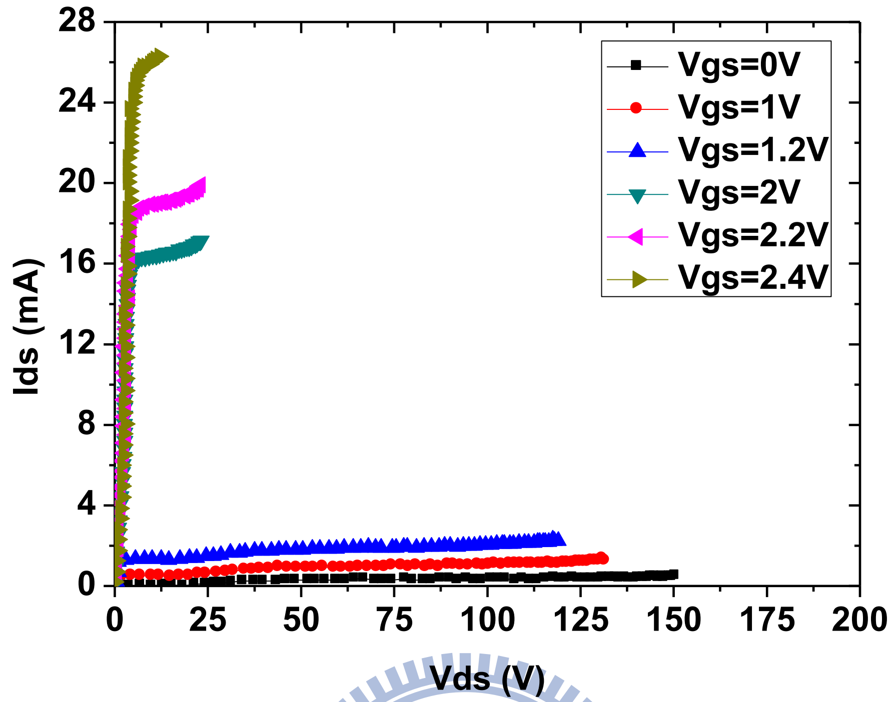
Fig. 2-8. The I_{DS}-V_{DS} characteristics of a SOI LDMOS transistor. Solid line: simulated curve without self-heating effect. Dotted line: calculated curve which take self-heating effect into account. Experimental data which are measured under the 2-μs, 100-μs power pulses, and DC conditions [19].



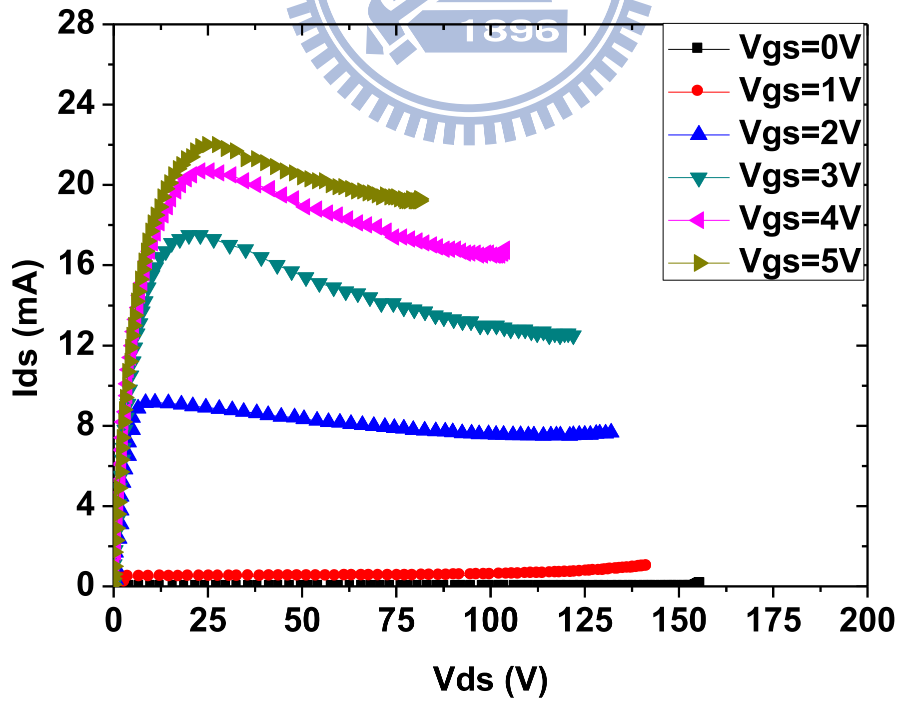
(a) nLDMOS



(b) Circular_nLDMOS

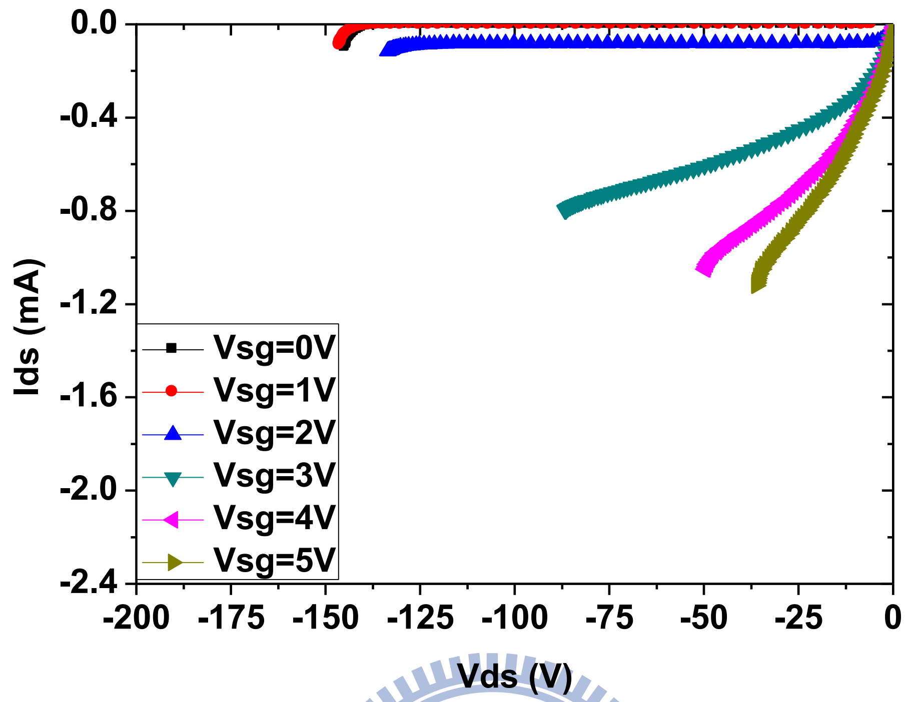


(c) SCR-nLDMOS_A

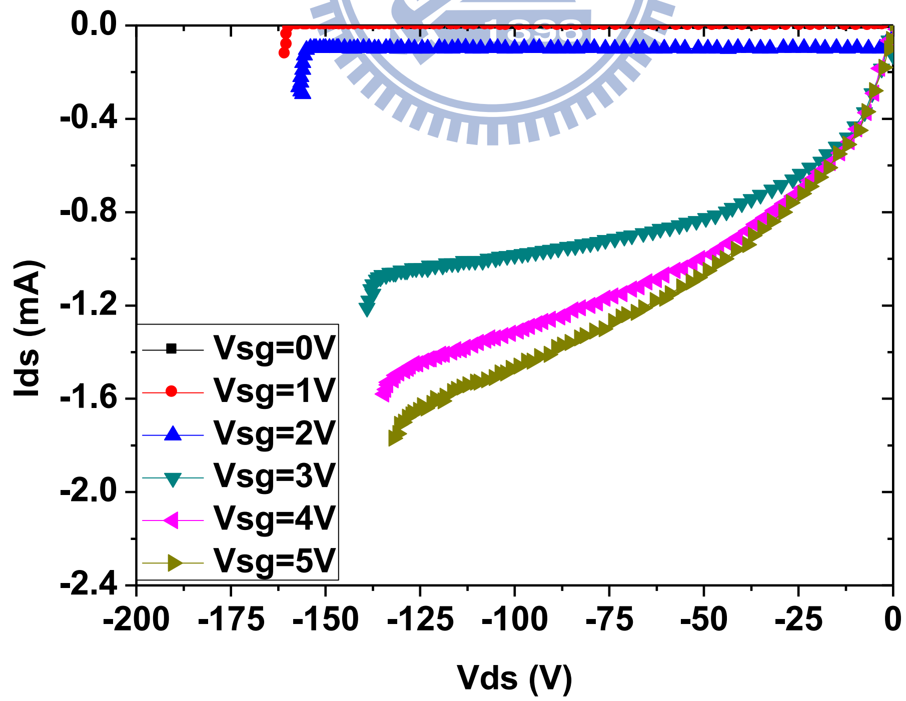


(d) SCR-nLDMOS_B

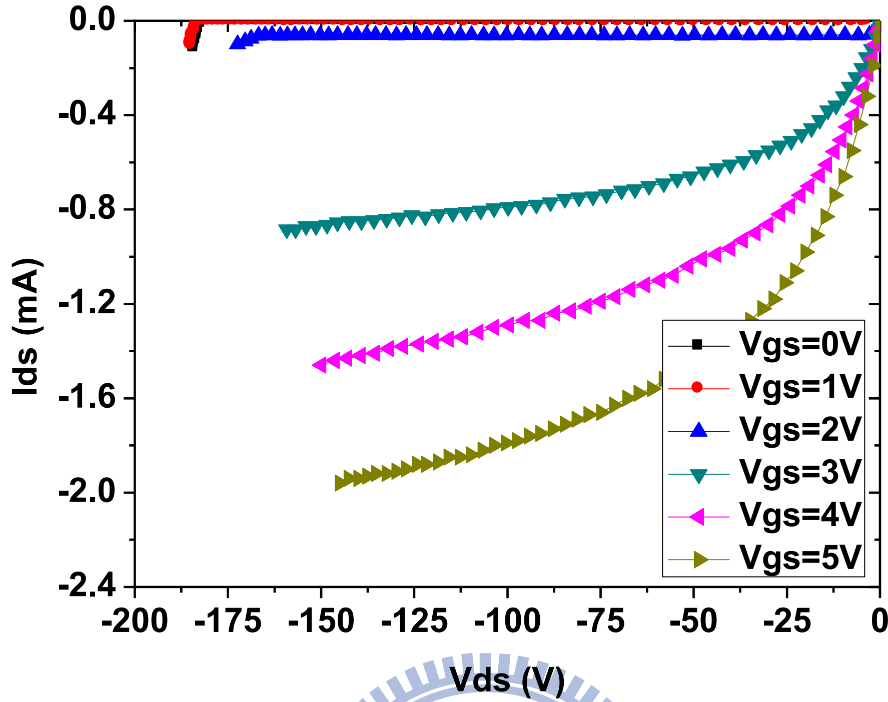
Fig. 2-9. The DC I_{DS}-V_{DS} characteristics of N-type typical DMOS.



(a) pLDMOS



(b) SCR-pLDMOS_A



(c) SCR-pLDMOS_B

Fig. 2-10. The DC I_{DS}-V_{DS} characteristics of P-type typical DMOS.

TABLE 2.1

The layout parameters of typical DMOS

Typical Device Structure	Layout Parameters (μm)
nLDMOS	W = 40, L = 2, D = 12, Y = 13, x = 6, s = 1, and e = 2.
Circular_nLDMOS	r = 23, L = 2, D = 12, Y = 23, x = 6, and s = 1.
SCR-nLDMOS_A	W = 40, L = 2, D = 12, Y = 7, z = 3, s = 1, e = 2, and $T_d = T_s = 0$.
SCR-nLDMOS_B	W = 40, L = 2, D = 12, Y = 7, z = 3, s = 1, e = 2, and $T_d = T_s = 0$.
pLDMOS	W = 40, L = 2, D = 12, Y = 13, x = 6, s = 1, and e = 2.
SCR-pLDMOS_A	W = 40, L = 2, D = 12, Y = 3, z = 1, s = 1, e = 2, and $T_d = T_s = 0$.
SCR-pLDMOS_B	W = 40, L = 2, D = 12, Y = 3, z = 1, s = 1, e = 2, and $T_d = T_s = 0$.

2.4 Avalanche Breakdown Voltage

The definition of avalanche breakdown voltage (BV_{dss}) is the drain voltage when the drain current is equal to 10 μA under the condition of V_{GS} = 0 V. The following shows the BV_{dss} of typical HV DMOS whose parameters are listed in Table 2.1. Fig. 2-11and Fig. 2-12 demonstrate the I_{DS}-V_{DS} curves with V_{GS} = 0 V for n-type HV DMOS; similarly, Fig. 2-13 shows the I_{SD}-V_{SD} curves with V_{SG} = 0 V for p-type HV DMOS. First of all, Fig. 2-11 reveals that the BV_{dss} of circular_nLDMOS is larger than that of nLDMOS. Secondly, Fig. 2-12 exhibits that the BV_{dss} of nLDMOS, SCR-nLDMOS_A, and SCR-nLDMOS_B are almost identical. Finally, Fig. 2-13 manifests that the BV_{dss} of SCR-pLDMOS_A is the highest while the BV_{dss} of pLDMOS is the lowest. Table 2.2 lists the BV_{dss} and radius of spherical P/N junction with different device structure. The radius of spherical P/N junction dominates the BV_{dss} [12]-[14]; therefore, BV_{dss} increases with increasing radius.

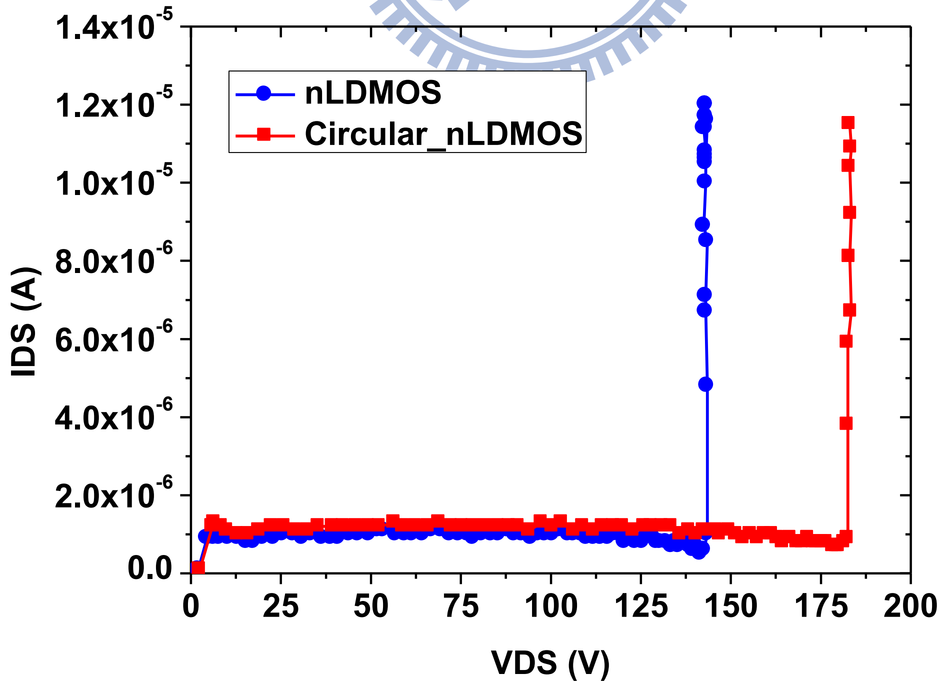


Fig. 2-11. The DC I_{DS}-V_{DS} curves of nLDMOS and circular_nLDMOS (V_{GS} = 0 V).

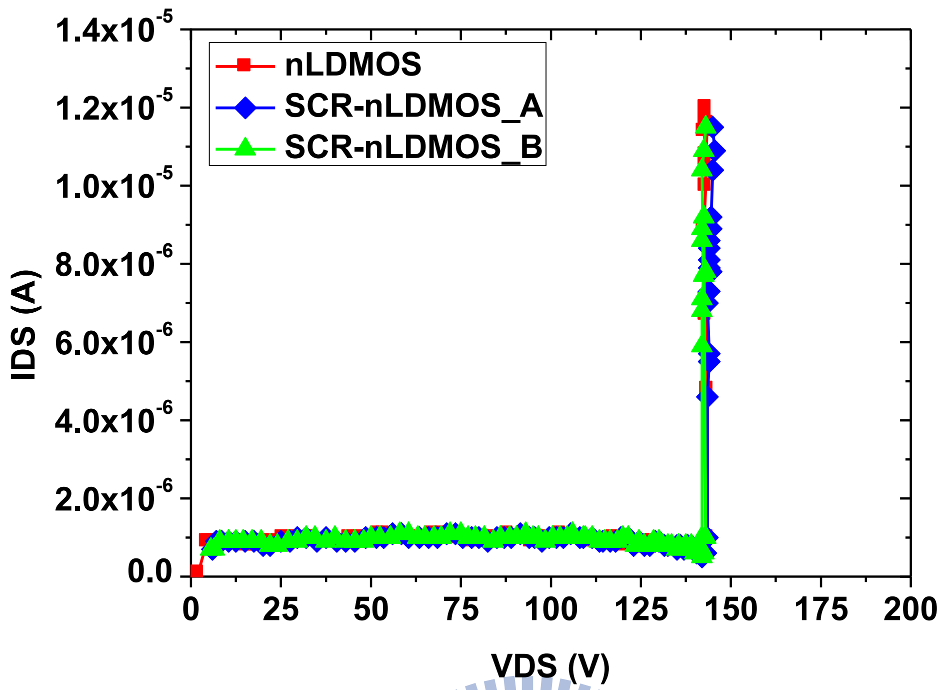


Fig. 2-12. The DC I_{DS}-V_{DS} curves (V_{GS} = 0 V) of nLDMOS, SCR-nLDMOS_A, and SCR-nLDMOS_B.

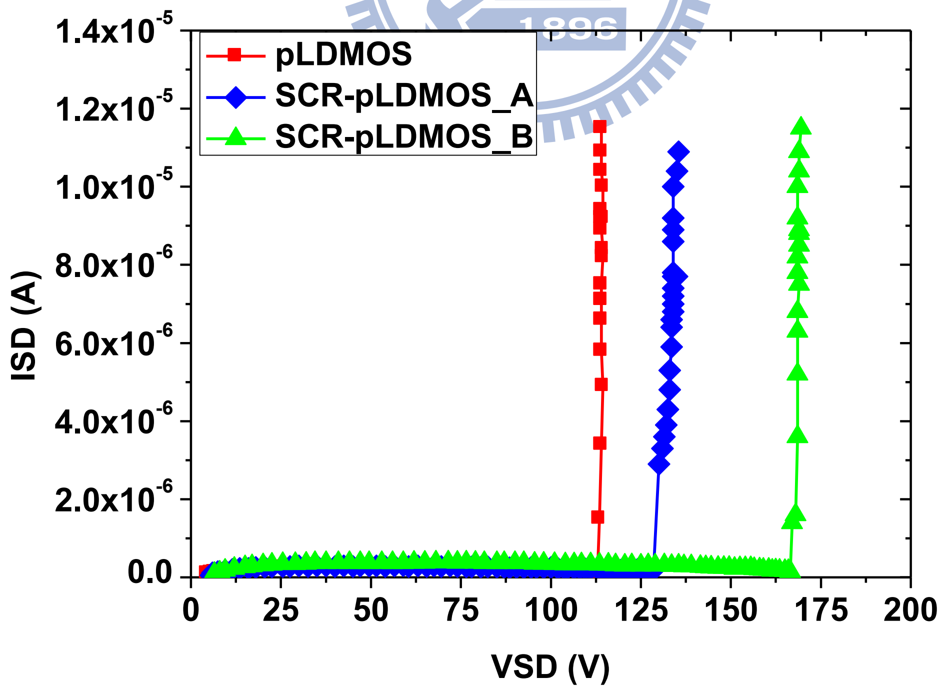
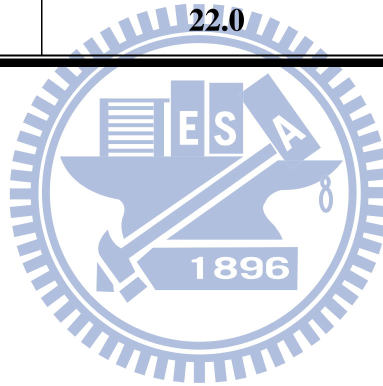


Fig. 2-13. The DC I_{SD}-V_{SD} curves (V_{SG} = 0 V) of pLDMOS, SCR-pLDMOS_A, and SCR-pLDMOS_B.

TABLE 2.2

The avalanche breakdown voltage of typical DMOS

Typical Device Structure	Radius of Spherical P/N Junction (μm)	Avalanche Breakdown Voltage (V)
nLDMOS	17.0	143.0
Circular_nLDMOS	21.0	183.0
SCR-nLDMOS_A	18.5	145.0
SCR-nLDMOS_B	16.0	142.0
pLDMOS	19.0	114.5
SCR-pLDMOS_A	20.0	134.0
SCR-pLDMOS_B	22.0	168.5



Chapter 3

Introduction to Electrostatic Discharge and Experimental Results

3.1 Introduction to Electrostatic Discharge (ESD)

ESD is an instantaneous discharging of electrostatic charges on IC pins. It take place under the situations such as a physical touch of a human body and an IC products, contact of manufacturing machines and wafers, or discharge of secondhand induced electrical field on an IC chips. According to the different discharge conditions and sources of electrostatic charges, ESD can be classified to human-body model (HBM), machine-model (MM), and charged-device model (CDM).

3.1.1 Human Body Model (HBM)

HBM is a common ESD event that arose from the contact of a charged human body and an IC product. The friction between human body and an object results in the charged human body, thus the electrostatic charge transfers into the IC products when the charged human body touches the IC products. To prevent the catastrophically failure on IC products, the human body model is established to simulate this kind of ESD event and quantify the IC robustness against the HBM ESD event. The equivalent circuit for HBM ESD event is shown in Fig. 3-1 [21], where the 1.5-kΩ resistor and the 100-pF capacitor represent the equivalent parasitic resistor and capacitor of a human body. The DUT represents the device under test. The HBM design eliminates the weak ESD protection designs and protects the susceptible devices. Commercial ICs are generally demanded to pass 2-kV HBM ESD stress at

least, which can generate ESD current with a peak value about 1.3 A and a rise time about 10 ns. Fig. 3-2 shows the typical HBM ESD waveform generated by the ESD HBM tester to a short wire [21]. In particular, most of the HBM ESD energy is concentrate on the time interval between 0 ns to 100 ns.

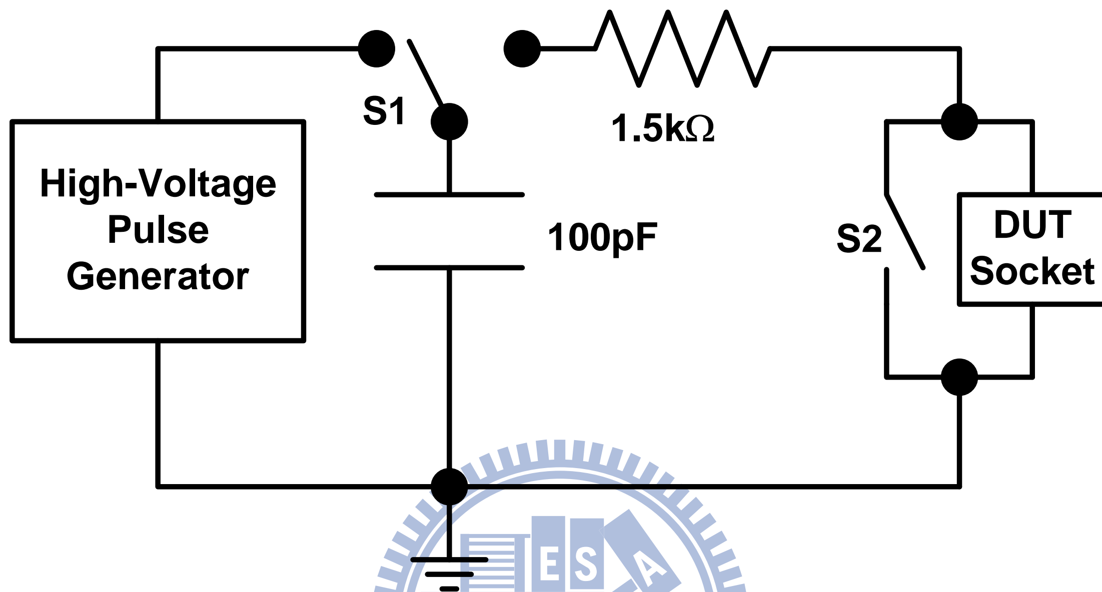


Fig. 3-1. The equivalent circuit of the human body model ESD event [21].

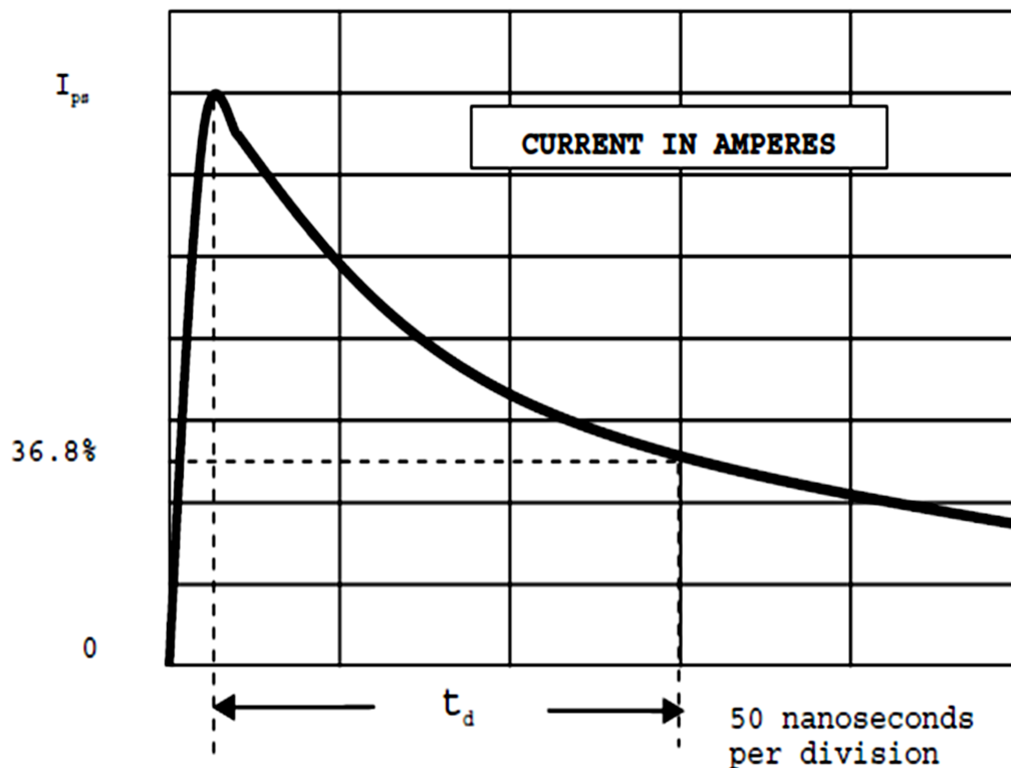


Fig. 3-2. Definition of the HBM pulse decay time (t_d) [21].

3.1.2 Machine Model (MM)

The MM ESD event arose from the contact of a machine and IC products. The equivalent circuit diagram of MM ESD event is shown in Fig. 3-3 [22], where there is no equivalent resistor on the equivalent discharging path because the electrostatic charge source is charged machine with 0-Ω resistor.

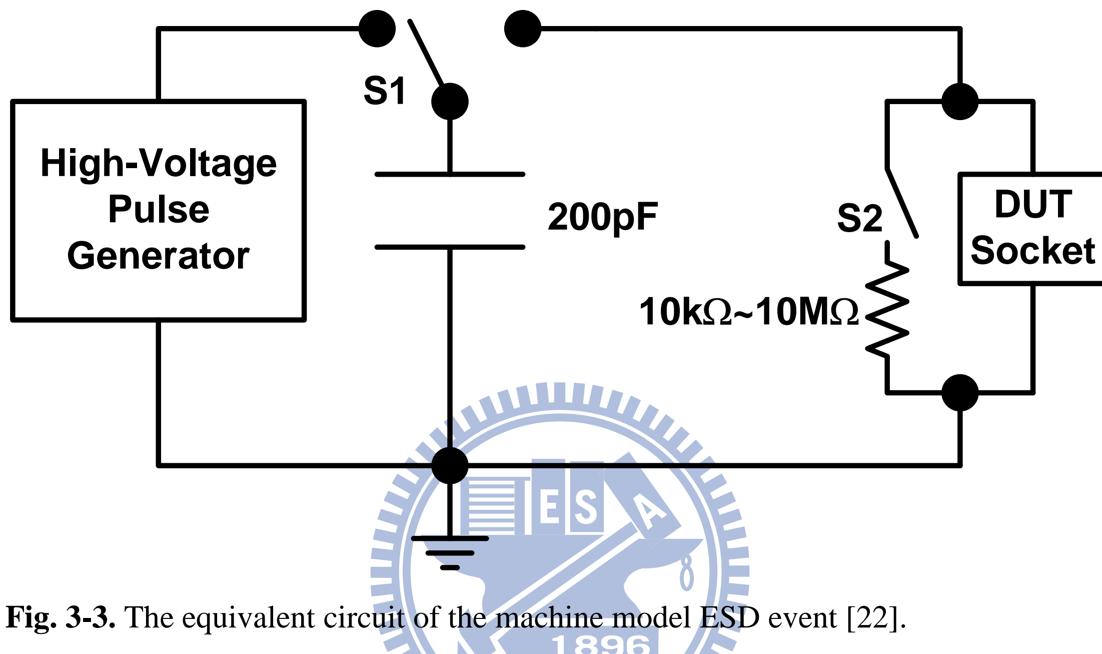


Fig. 3-3. The equivalent circuit of the machine model ESD event [22].

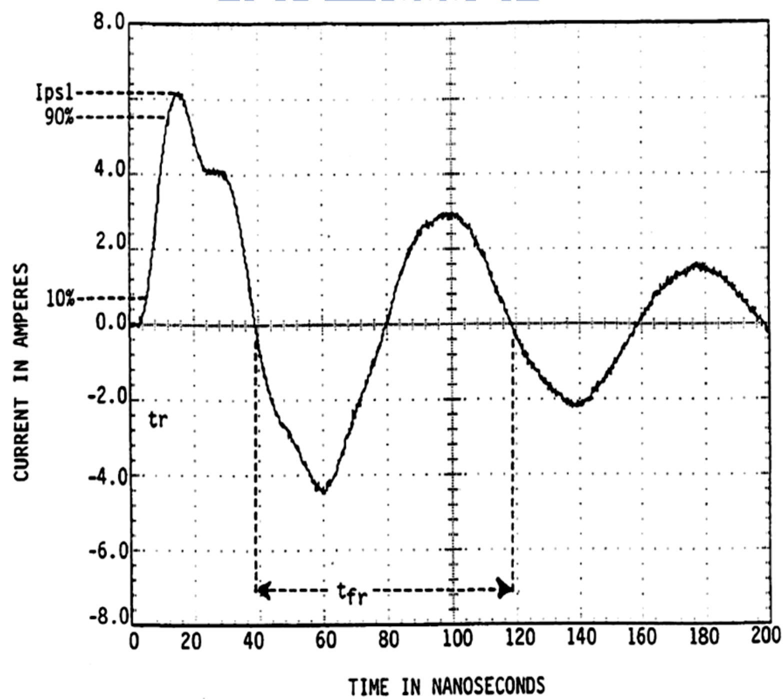


Fig. 3-4. The current waveform of a 400-V MM ESD stress through a short wire [22].

Fig. 3-4 shows the waveform of a 400-V MM ESD pulse generated by the MM ESD tester [22]. A commercial IC product is generally required to pass at least 200-V MM ESD stress, which can generate an ESD current with a peak value about 3.5 A and a rise time about 10 ns. The MM ESD level of a semiconductor device is generally 8 ~ 12 times smaller than its HBM ESD level due to the faster rise time and voltage resonance of a MM ESD pulse.

3.1.3 Charged Device Model (CDM)

The CDM ESD event happens under the condition of the contact of charged IC and external grounded object. The IC is charged through the mechanism of electrostatic induction, and most of the CDM charges are initially stored in the body (the p-substrate) of a CMOS IC. When one or more pins of this charged IC is touched by an external grounded object, CDM charges in the p-substrate will be discharged from the IC inside to the grounded object outside. There is no standard equivalent parasitic capacitor and resistor for the CDM ESD stress because different dimension of chips, different form and size of packages result in different values of the parasitic capacitor and resistor of IC chips. Fig. 3-5 shows the simplified CDM test circuit. R_d, L_d and C_d represents the equivalent parasitic resistor, inductor and capacitance of DUT. The DUT is initially charged through the large resistor R_g with relatively small current, and then DUT contact the grounded object and discharge immediately. A commercial IC is generally requested to pass at least 1-kV CDM ESD stress, which can generate an ESD current with peak current value about 15 A within a rise time less than 200 ps [23]. Fig. 3-6 makes a contrast with the waveforms of a 2-kV HBM ESD stress, a 200-V MM ESD stress, and a 1-kV CDM ESD stress which has 4-pF equivalent capacitor of the device under test. Table 3.1 shows the commercial specification for the HBM, MM and CDM level.

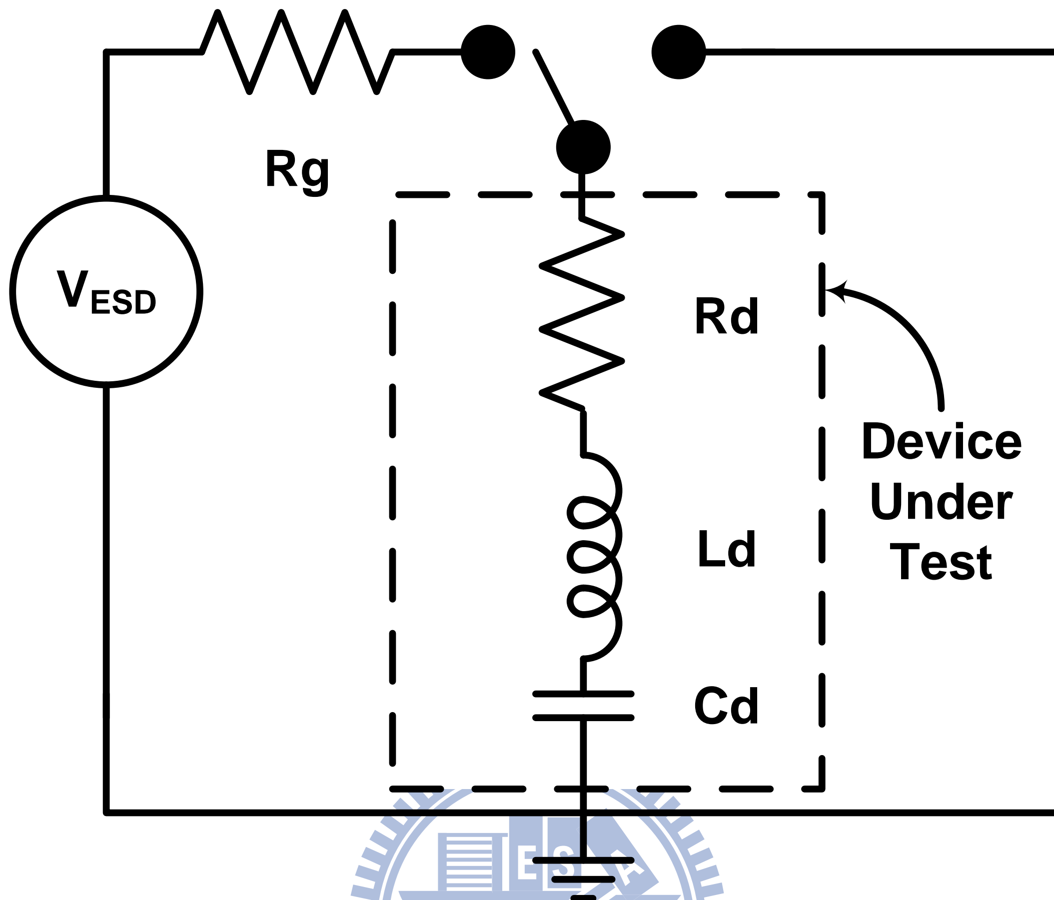


Fig. 3-5. The equivalent circuit of the charged device model ESD event [23].

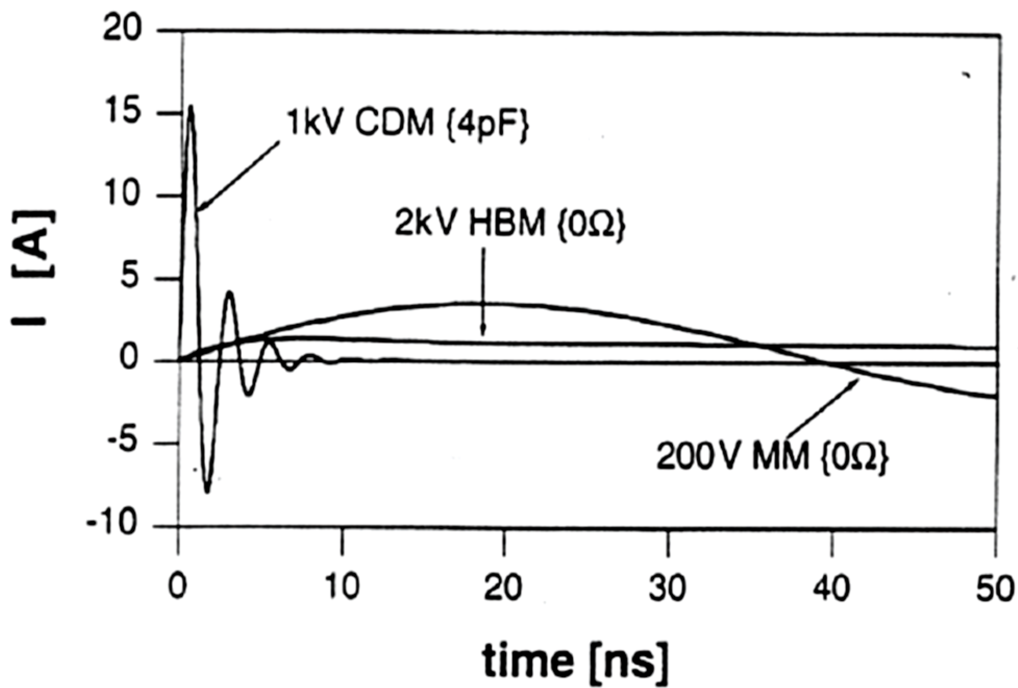


Fig. 3-6. The waveforms of a 2-kV HBM ESD stress, 200-V MM ESD stress, and a 1-kV CDM ESD stress.

TABLE 3.1

The commercial specification for the HBM, MM and CDM level.

	HBM (kV)	MM (V)	CDM (kV)
Okay	+/- 2	+/- 200	+/- 2
Safe	+/- 4	+/- 400	+/- 1.5
Super	+/- 10	+/- 1000	+/- 2

3.1.4 Transmission Line Pulse (TLP) System

The equivalent circuit of TLP system is shown in Fig. 3-7 The TLP system applied the voltage pulse, which pulse amplitude is Vin and the pulse width is t, to the device under test (DUT). The oscilloscope measured the voltage and current during the TLP stress, and then the source-meter measured the leakage under certain bias condition.

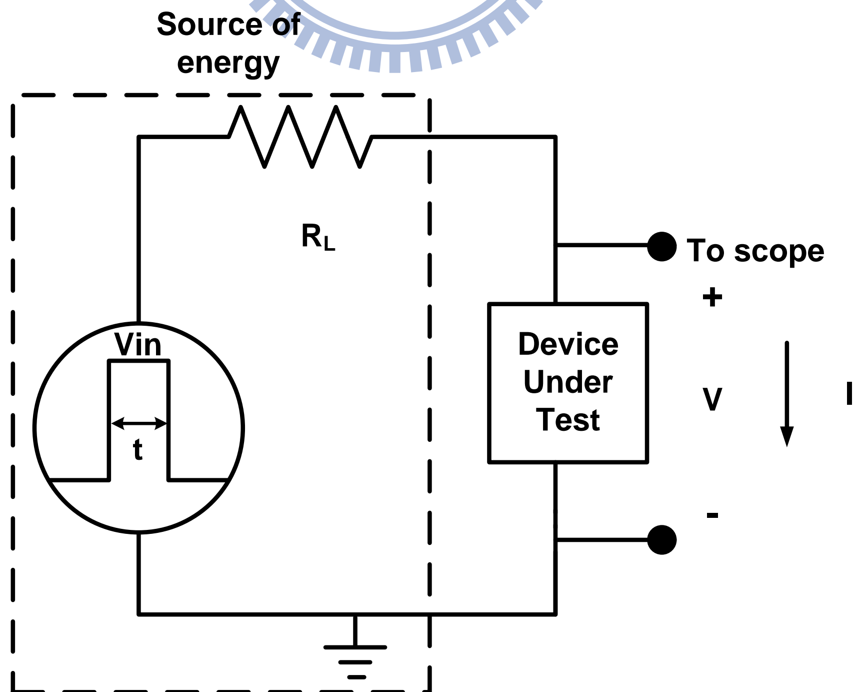


Fig. 3-7. The equivalent circuit of the TLP system.

The steps above are sequentially repeated with increasing TLP pulse amplitude until the device satisfies the failed criteria. In this thesis, the definition of failed criteria is $I_{leakage} > 100* I_{leakage,\ initial}$, where $I_{leakage}$ is the leakage current measured after TLP zapping and $I_{leakage,\ initial}$ is the leakage current of fresh transistor. The I-V curve measured by TLP system is shown in Fig. 3-8. Trigger point represents the triggering of parasitical bipolar junction transistor (BJT). Secondary breakdown current (I_{t2}) represents the maximum allowable current. In other words, the device is judged to failure as the current is higher than I_{t2}. Interestingly, the HBM ESD waveform reveals that the ESD energy is concentrate on the time interval between 0 ns to 100 ns and it is observed that the HBM level is proportional to I_{t2} [24]. With the information provided by TLP system, IC designers can easy choose the direct device under the guide of design window, as illustrated in Fig. 3-9 [25].

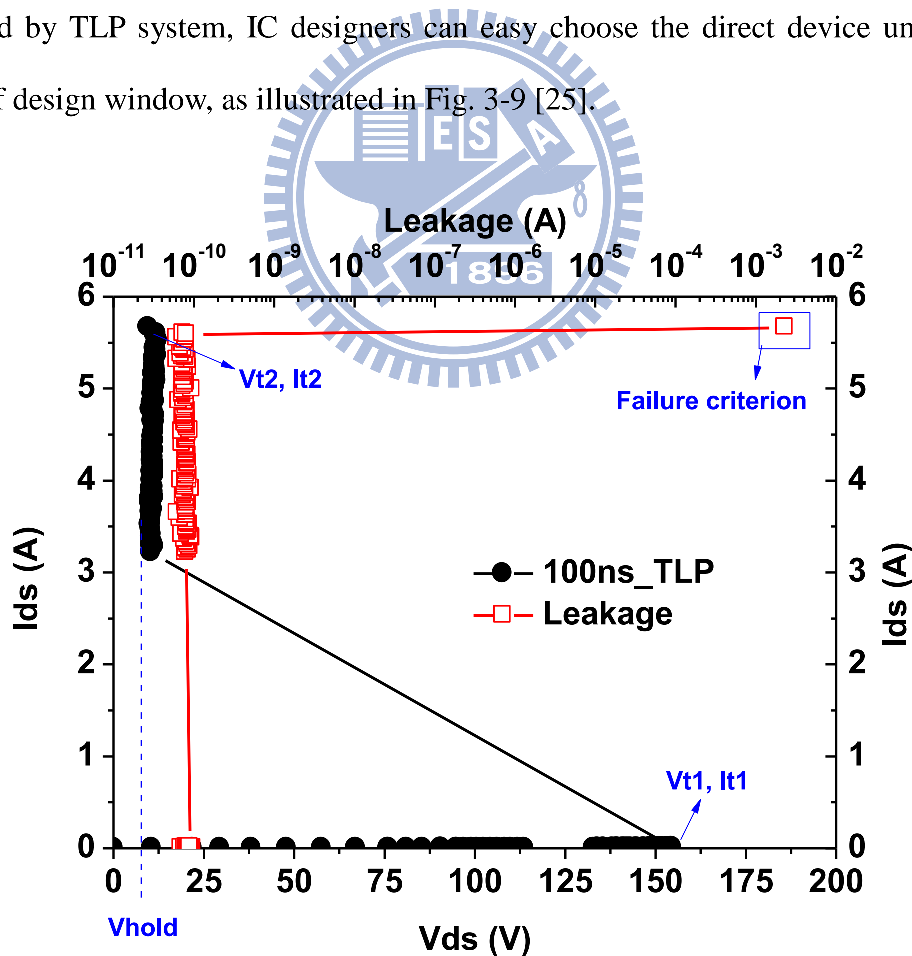


Fig. 3-8. The I-V curve measured by 100-ns TLP system.

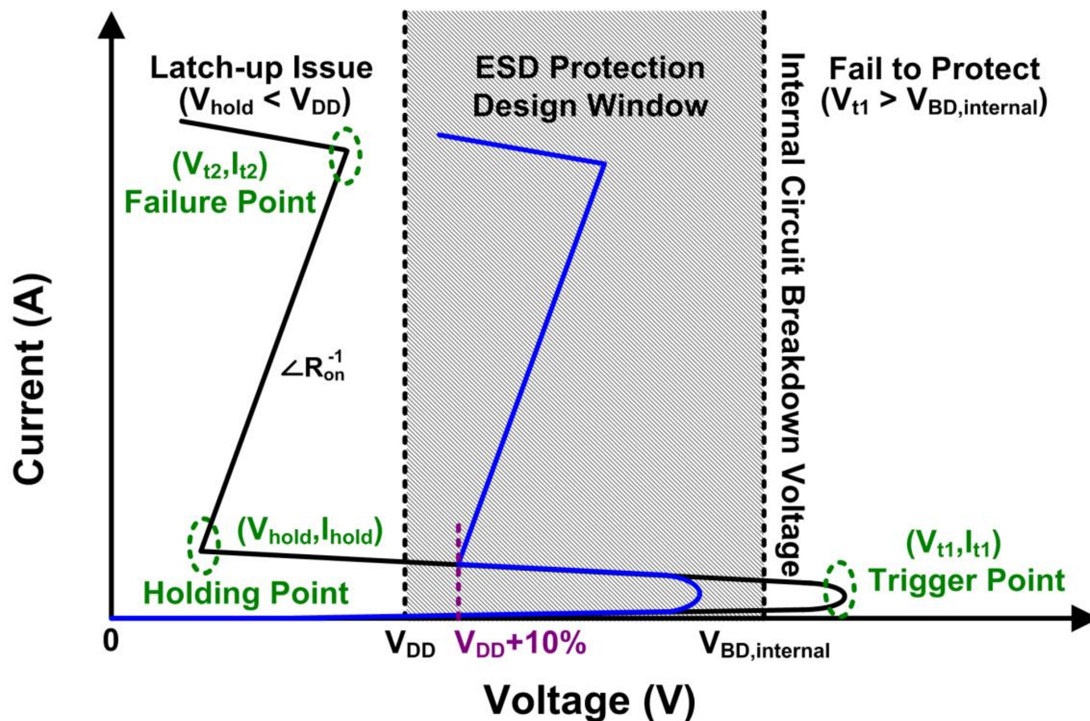


Fig. 3-9. The ESD protection design window of HV ESD protection devices [25].

3.2 ESD Test Methods

ESD test has positive and negative type in order to simulate the positive and negative electrical charges in natural environment. Furthermore, IC chip have several input/output (I/O) pins and power pins; therefore, ESD test can occur on different pin combinations. The major pin combinations of ESD test are shown as following.

3.2.1 ESD Test on I/O Pins

The human-body model and the machine-model ESD stress on each I/O pins with the VDD or VSS pins relatively ground are illustrate through Fig. 3-10(a) to 3-10(d) [27], [28]:

(1) PS mode

Positive ESD voltage is applied to the tested I/O pin with VSS pins relatively grounded, as shown in Fig. 3-10(a). VDD pins and all other pins are kept floating during the test.

(2) NS mode

Negative ESD voltage is applied to the tested I/O pin with VSS pins relatively grounded, as shown in Fig. 3-10(b). VDD pins and all other pins are kept floating during the test.

(3) PD mode

Positive ESD voltage is applied to the tested I/O pin with VDD pins relatively grounded, as shown in Fig. 3-10(c). VSS pins and all other pins are kept floating during the test.

(4) ND mode

Negative ESD voltage is applied to the tested I/O pin with VDD pins relatively grounded, as shown in Fig. 3-10(d). VSS pins and all other pins are kept floating during the test.

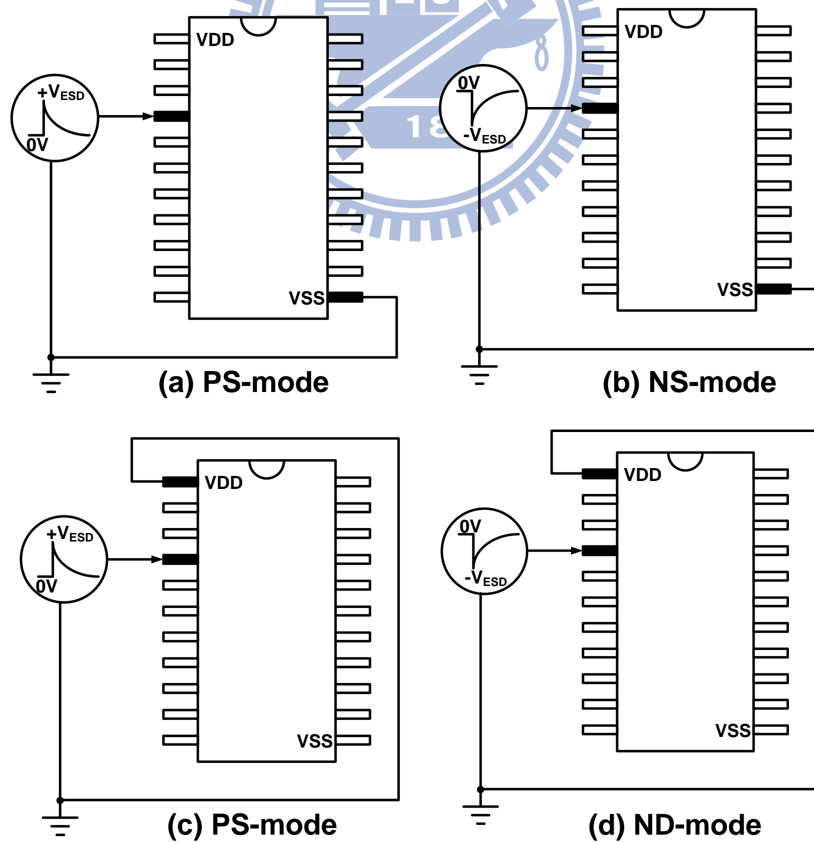


Fig. 3-10. (a) PS-mode, (b) NS-mode, (c) PD-mode, and (d) ND-mode, ESD test on I/O pins.

3.2.2 Pin to Pin ESD Test

ESD events would occur on one of the I/O pins with another I/O pin relatively grounded. In other words, power lines are floating during the pin to pin ESD test. The pin to pin ESD test can easily cause ESD damage located at the internal circuits if the ESD protective design is poor. The common pin to pin ESD path is shown in Fig. 3-11. If every two of I/O pins is tested one by one, the ESD test is inefficient and uneconomic. In order to shorten the testing period, ESD stress is applied on the tested I/O pin with all other I/O pins relatively grounded. The pin to pin ESD test is subdivided into positive-mode and negative-mode as illustrated in Fig. 3-12(a) and Fig. 3-12(b).

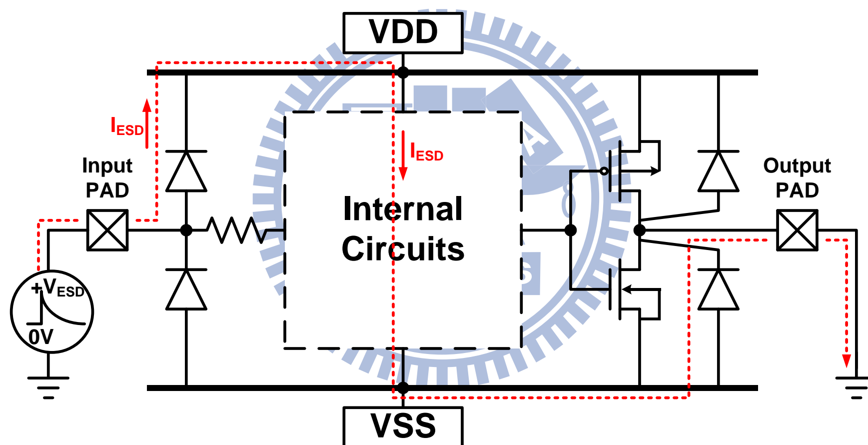


Fig. 3-11. The internal ESD damage due to the pin to pin ESD stress.

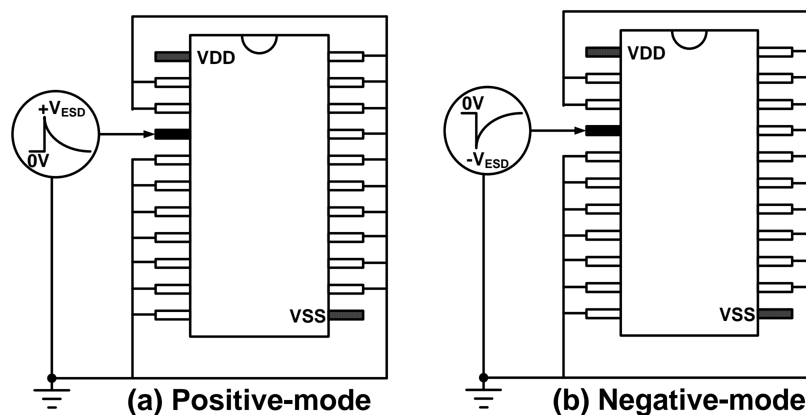


Fig. 3-12. The pin-to-pin ESD test of (a) positive mode and (b) negative-mode.

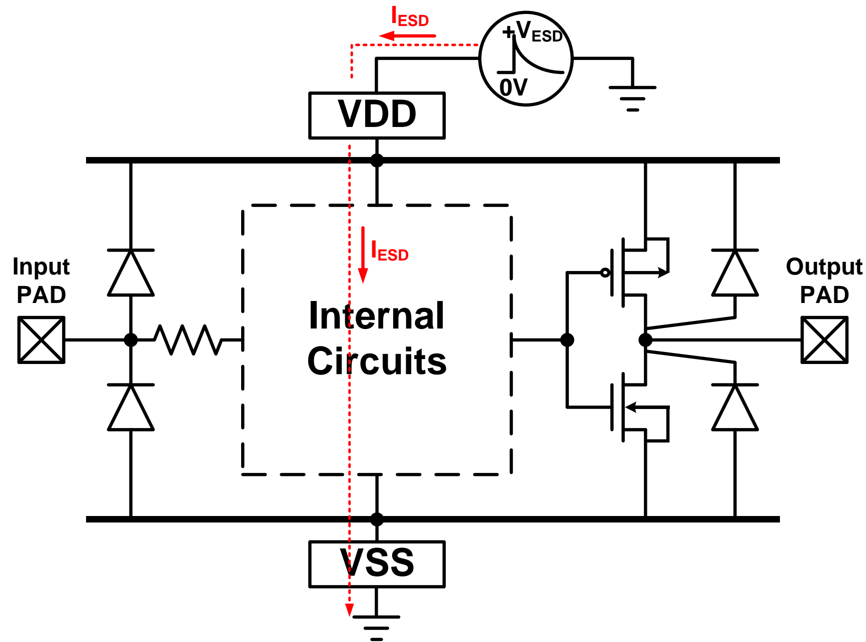


Fig. 3-13. The internal ESD damage due to the VDD-to-VSS ESD stress.

3.2.3 VDD-to-VSS ESD Test

The ESD event may happen between two power pins. The internal circuits are vulnerable to ESD stress under the condition that ESD voltage is applied to VDD with VSS relatively ground, as shown in Fig. 3-13. To simulate this kind of ESD-stress condition, a positive or a negative ESD voltage is applied to the VDD pin of an IC chip while VSS pin is relatively grounded, as illustrated in Fig. 3-14(a) and Fig. 3-14(b).

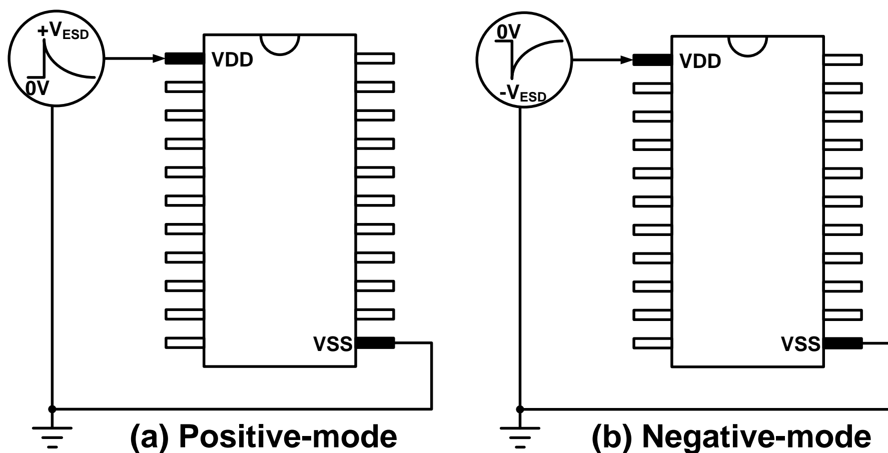


Fig. 3-14. The VDD-to-VSS ESD tests of (a) positive mode and (b) negative-mode.

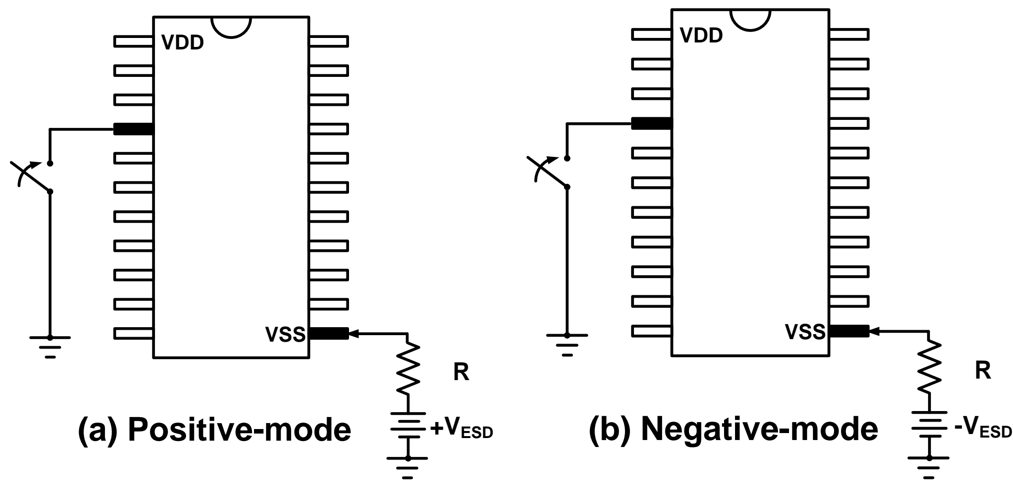


Fig. 3-15. The CDM ESD tests of (a) positive mode and (b) negative-mode.

3.2.3 CDM ESD Test

The mechanism of CDM ESD event differs from the HBM and MM ESD events; therefore, the CDM ESD test is especially defined. The substrate of an IC product is initially full of electrostatic charge, and then the device instantaneously discharged when one of the IC pin is ground. In other words, the ESD path is from the inside of IC chip to the outside of grounded object. In order to fill IC substrate with electrostatic charges, the ESD voltage is applied to the VSS pin through the large resistor, as shown in Fig. 3-15(a) and Fig. 3-15(b). With the large resistor, the electrical current is small during charging the device under test, otherwise, the charging current will directly damage the VSS pin and the electrostatic charges will not remain in IC substrate. The ESD voltage is instantly discharged through the pins included the input, output, and VDD pins. To simulate the electrostatic charge in nature, the CDM ESD test is classified into positive-mode and negative-mode, as shown in Fig. 3-15(a) and Fig. 3-15(b).

3.3 Experimental results

First of all, the investigation is focus on the typical HV DMOS as listed in Table 2.1 for the purpose of verifying the effect of different device structures on ESD robustness. Consequently, the following experimental results include TLP, HBM, MM, and failure analysis. The second part is the analysis of ESD robustness with different layout parameters. A brief summary about the ESD robustness of HV DMOS is in the end.

3.3.1 ESD Robustness

The following is the ESD experimental results of typical HV DMOS. Fig. 3-16~18 show the TLP-measured results under the same condition of $V_{GS} = 0$ V. The solid line presents the I-V curve while the dotted line is the leakage current which is measured after every TLP ESD stress. The data of V_{t1}, I_{t1}, V_{hold}, and I_{t2} are extracted from TLP-measured I-V curve, as illustrated in Table 3.2. The drift length of circular_nLDMOS is longer than that of nLDMOS, so circular_nLDMOS needs higher energy to trigger the parasitic BJT. In other words, the V_{t1} and I_{t1} of circular_nLDMOS are larger than that of nLDMOS. Both nLDMOS and circular_nLDMOS are damaged while entering the snapback region. As a result, the I_{t2} are poor for both devices. The SCR device exhibits the excellent ESD robustness within small layout area due to its low holding voltage. Accordingly, the insertion of SCR to HV DMOS is applied to improve the ESD robustness. Fig. 3-17 demonstrates that the I_{t2} of SCR-nLDMOS_A is excellent while the I_{t2} of SCR-nLDMOS_B is almost identical to that of nLDMOS. It is supposed that the triggering of parasitic SCR is failed in SCR-nLDMOS_B. Therefore, the SCR-nLDMOS_B acts like nLDMOS when entering the snapback region. Fig. 3-18 shows the TLP-measured I-V

curve for p-type HV DMOS. Likewise, the SCR-pLDMOS_A exhibits excellent failure current while SCR-pLDMOS_B behaves like pLDMOS which fails while entering the snapback region. Hence, it is supposed that the triggering of parasitic SCR is failed in SCR-pLDMOS_B.

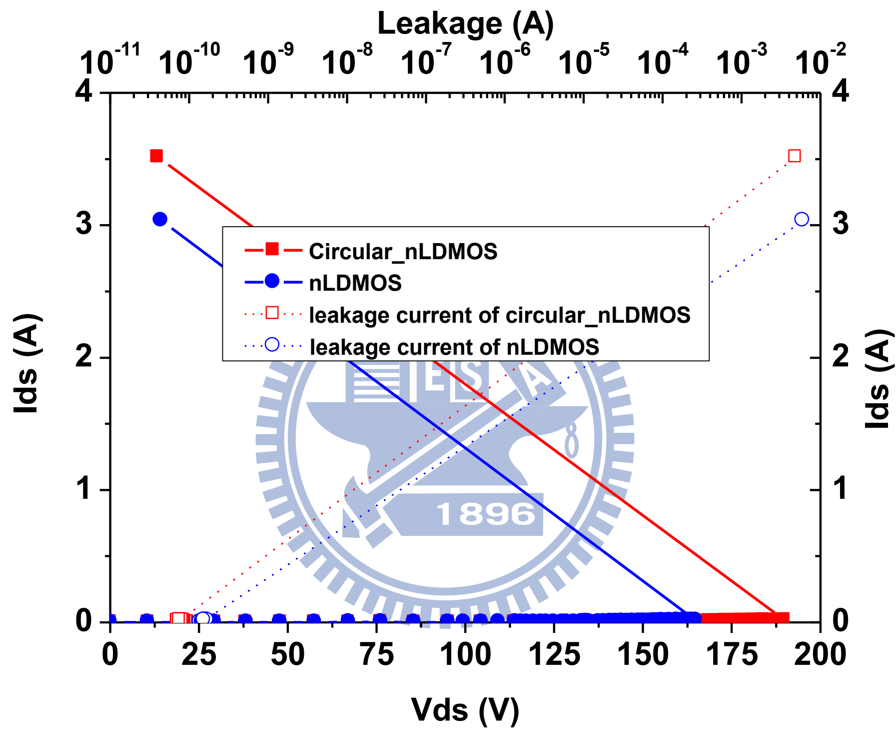


Fig. 3-16. TLP-measured results of (in circular symbol) nLDMOS and (in square symbol) circular_nLDMOS.

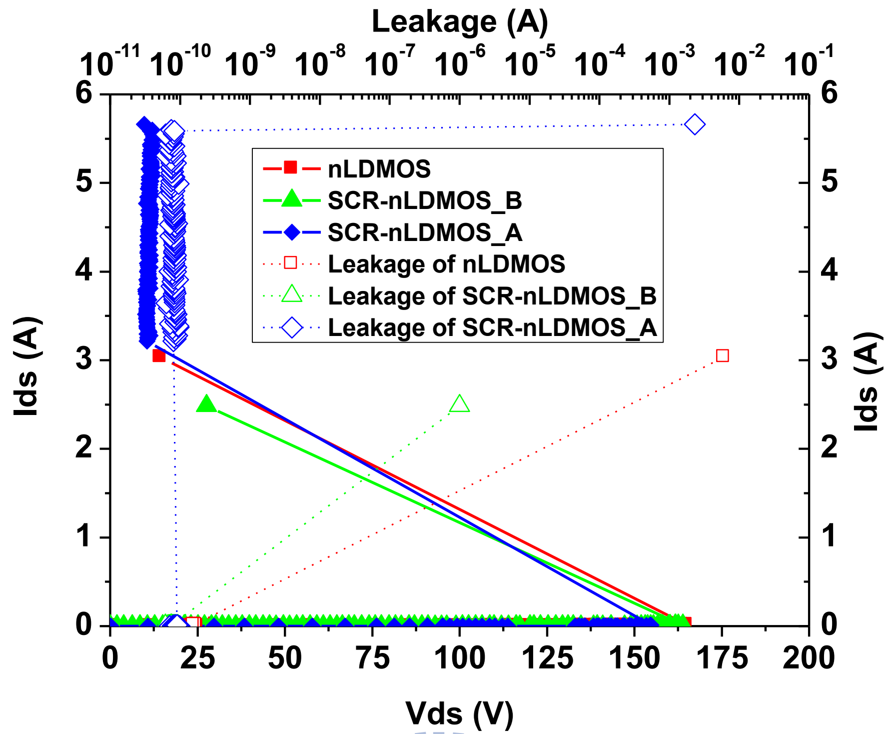


Fig. 3-17. TLP-measured results of (in square symbol) nLDMOS, (in diamond symbol) SCR-nLDMOS_A, and (in triangular symbol) SCR-nLDMOS_B.

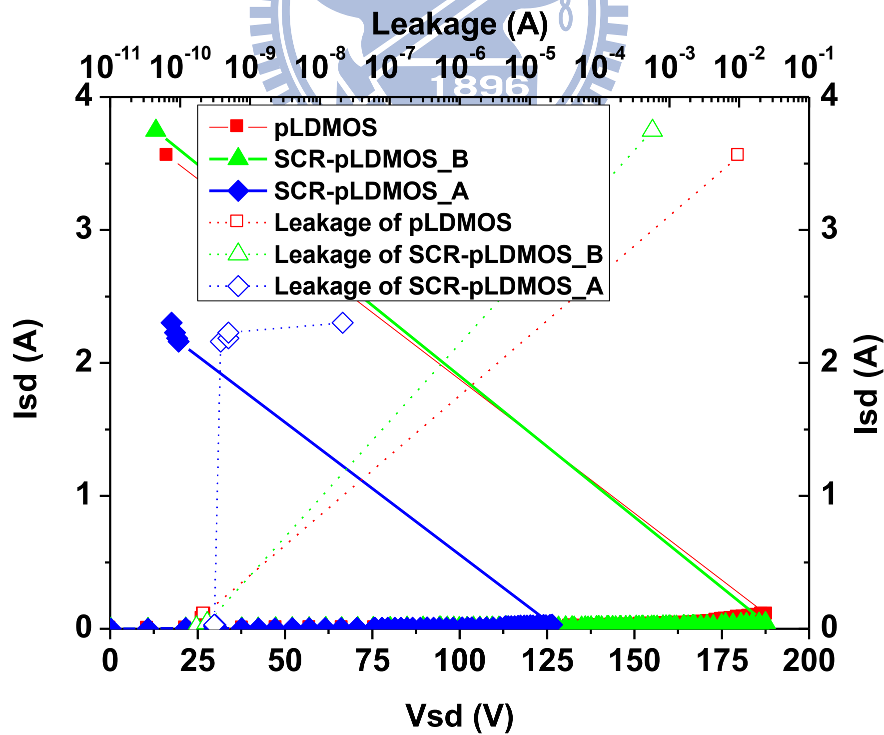


Fig. 3-18. TLP-measured results of (in square symbol) pLDMOS, (in diamond symbol) SCR-pLDMOS_A, and (in triangular symbol) SCR-pLDMOS_B.

TABLE 3.2

The TLP-measured results of typical HV DMOS.

Typical Device Structure	V_{t1} (V)	I_{t1} (mA)	V_{hold} (V)	I_{t2} (A)
nLDMOS	**164.9**	**14.9**	**14.4**	**~ 0.0149**
Circular_nLDMOS	**190.0**	**16.5**	**13.5**	**~ 0.0165**
SCR-nLDMOS_A	**154.7**	**10.1**	**10.5**	**5.6**
SCR-nLDMOS_B	**163.9**	**7.9**	**27.6**	**~ 0.0079**
pLDMOS	**187.9**	**107.1**	**16.4**	**~ 0.1071**
SCR-pLDMOS_A	**126.5**	**29.6**	**19.6**	**2.2**
SCR-pLDMOS_B	**187.5**	**43.7**	**13.1**	**~ 0.0437**

The common estimation of the ability against the ESD stress includes I_{t2}, HBM, and MM is shown in Table 3.3. The sample size is one for TLP-test and the sample size is three for HBM-test and MM-test. Sample one is simplified as "#1". Sample two and three are analogically simplified as "#2" and "#3". The voltage step of HBM-test is 0.5 kV while that of MM-test is 50 V. HBM and MM tests are in positive-mode for n-type DMOS and in negative-mode for p-type DMOS. The HBM level is below 0.5 kV for n-type HV DMOS which fails while entering the snapback region in TLP-test. The MM level is below 50 V for n-type HV DMOS of which the I_{t2} is poor. Likewise, the HBM level is below -0.5 kV and the MM level is below -50 V for p-type HV DMOS which fails while entering the snapback region in TLP-test. On the contrary, the HBM level is 6 kV and the MM level is 200 V for SCR-nLDMOS_A. The HBM level is -3 kV and the MM level is -100 V for SCR-pLDMOS_A. The insertion of SCR to HV DMOS is useful to improve ESD

robustness. Table 3.4 demonstrates the ESD ranking according to I_{t2} per unit device area. The first price is the SCR-nLDMOS_A and the second price is the SCR-pLDMOS_A which agrees with the results of HBM and MM.

TABLE 3.3

The ESD performance of typical HV DMOS includes I_{t2}, HBM, and MM.

Typical Device Structure	I_{t2} (A)	HBM (kV)			MM (V)		
	#1	#1	#2	#3	#1	#2	#3
nLDMOS	~ 0.0149	Below 0.5			Below 50		
Circular_nLDMOS	~ 0.0165	Below 0.5			Below 50		
SCR-nLDMOS_A	5.6	6	6.5	6.5	200	200	300
SCR-nLDMOS_B	~ 0.0079	Below 0.5			Below 50		
pLDMOS	~ 0.1071	Below -0.5			Below -50		
SCR-pLDMOS_A	2.2	-3	-3.5	-3.5	-100	-100	-150
SCR-pLDMOS_B	~ 0.0437	Below -0.5			Below -50		

TABLE 3.4

The ESD ranking of typical HV DMOS.

ESD Ranking	Device Structure	Device Area (μm^2)	I_{t2} (A)	I_{t2}/Device Area (mA)
1st place	SCR-nLDMOS_A	8380.0	5.6	668.3
2nd place	SCR-pLDMOS_A	7990.5	2.2	275.3
3rd place	pLDMOS	7783.0	0.1071	13.8
4th place	Circular_nLDMOS	5975.0	0.0165	2.8
5th place	SCR-pLDMOS_B	7794.0	0.0437	5.6
6th place	nLDMOS	7162.0	0.0149	2.1
7th place	SCR-nLDMOS_B	7468.0	0.0079	1.1

3.3.2 Failure Analysis

To further support the ESD levels shown in Table 3.3 and the supposition mentioned at 3.3.1, failure analyses on these failed typical HV DMOS is carried out through the way of taking scanning electron microscope (SEM) images. Fig. 3-19 shows the ESD failure locations of nLDMOS which suffers from a 0.5-kV HBM ESD stress. The contacts of drain N^+ region are permanently damaged by HBM ESD stress. The catastrophic contact spike of drain N^+ region causes the increase in leakage of HV N-well/P-sub junction. The phenomenon is called contact-spike-induced junction leakage. Furthermore, because the finger edge is easily crowded with electron and vulnerable to ESD stress, the damage at finger edge is more serious than that at finger side. Fig. 3-20 shows the ESD failure locations of circular_nLDMOS which suffers from a 0.5-kV HBM ESD stress. The device structure of circular_nLDMOS is identical to that of nLDMOS; hence, the contact spike happens at drain N+ region and the leakage of HV N-well/P-sub junction increases. Besides, the smallest parasitic resistance from drain to source (R_{DS}) is the resistance from the outer contact-ring at drain region to the contact at source region. Therefore, the ESD current crowds at the outer contact-ring and causes the catastrophic damage at the outer contact-ring. The SEM image of SCR-nLDMOS_A which suffers from a 6-kV HBM ESD stress is illustrated in Fig. 3-21. The contact spike occurs at drain P^+ region. The metal of contact causes the HV N-well/P-sub junction short and the leakage increases. Furthermore, because the contact spike is located at the contacts of drain P^+ region, the ESD current path is parasitic SCR path as shown in Fig. 2-6 (a). Moreover, the contacts of drain N^+ region are intact. That is, the parasitic SCR of SCR-nLDMOS_A effectively bypass the high current during the HBM ESD stress. On the contrary, the contact spike of SCR-nLDMOS_B is located at the drain N^+ region, which verifies that the triggering of parasitic SCR is failed for SCR-nLDMOS_B and the ESD

current path is parasitic BJT path as shown in Fig. 2-6 (b). Hence, the insertion of SCR can't improve the ESD robustness for SCR-nLDMOS_B. Fig. 3-23 shows the SEM images of pLDMOS which suffers a -0.5kV HBM ESD stress. The contact spike is located at the drain P^+ region. The leakage of N-well/P-sun junction increases due to the contact spike. The contact spike of SCR-pLDMOS_A is located at the drain N^+ region while the contacts of drain P^+ region are intact, as illustrated in Fig. 3-24. It proves that the ESD current path is SCR path for SCR-pLDMOS_A. In addition, the contact spike of SCR-pLDMOS_B is located at the drain P^+ region while the contacts of drain N^+ region are intact, as illustrated in Fig. 3-25. It gives the evidence that the triggering of SCR is failed for SCR-pLDMOS_B and the ESD current path is parasitic BJT path as shown in Fig. 2-6 (d). The supposition which is made in 3.3.1 is verified by the evidence of the SEM images.

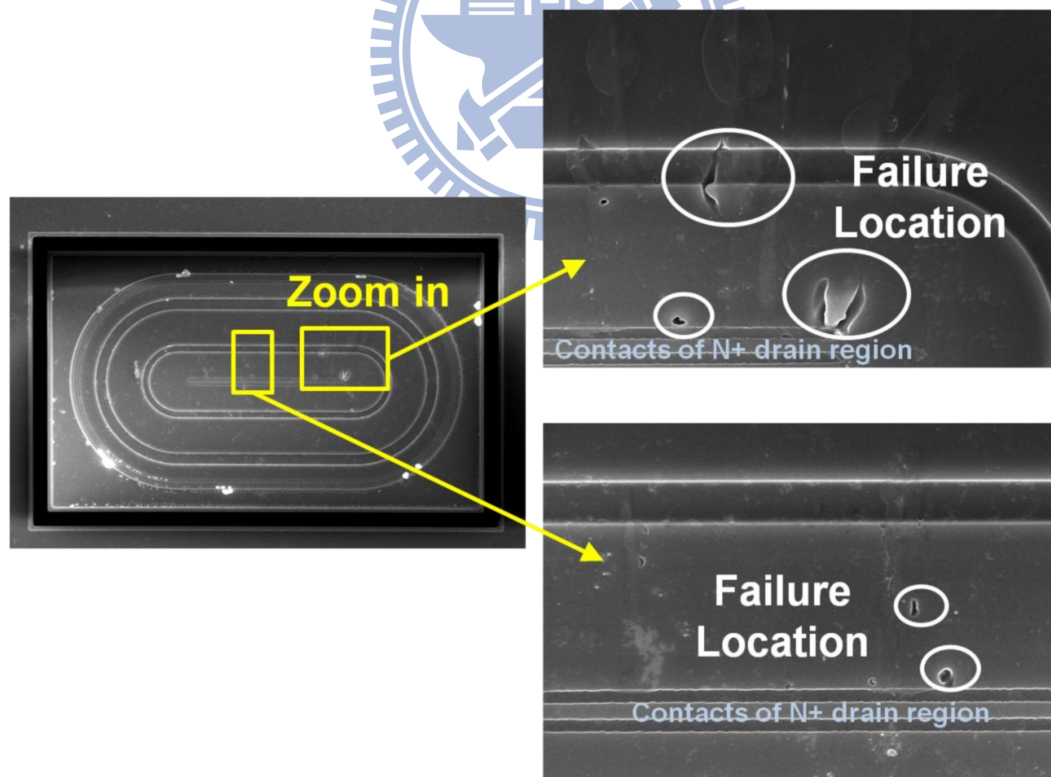


Fig. 3-19. SEM images of typical nLDMOS which suffers from a 0.5-kV HBM ESD stress.

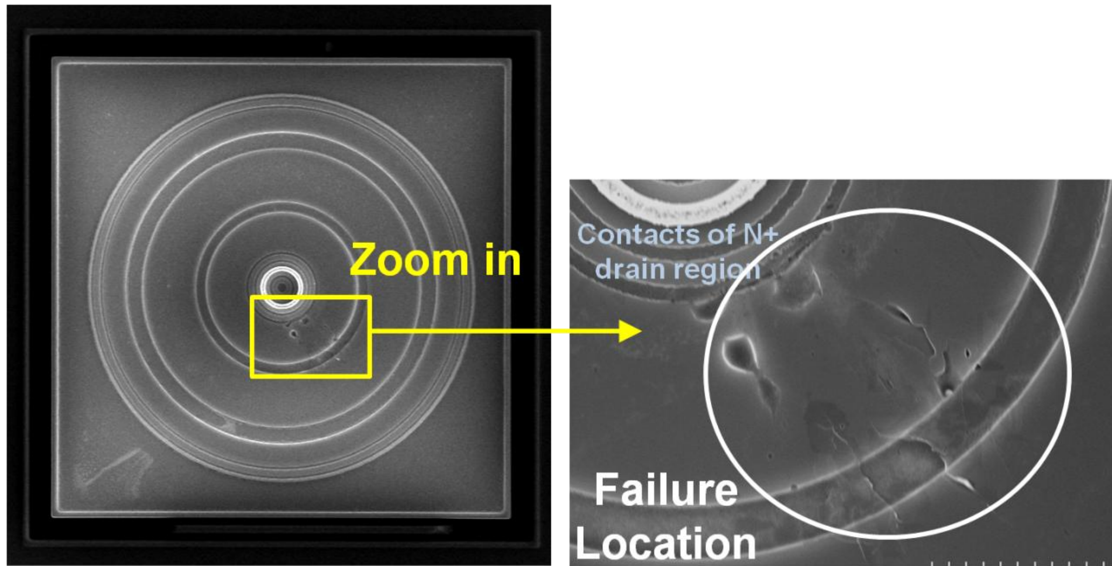


Fig. 3-20. SEM images of typical circular_nLDMOS which suffers from a 0.5-kV HBM ESD stress.

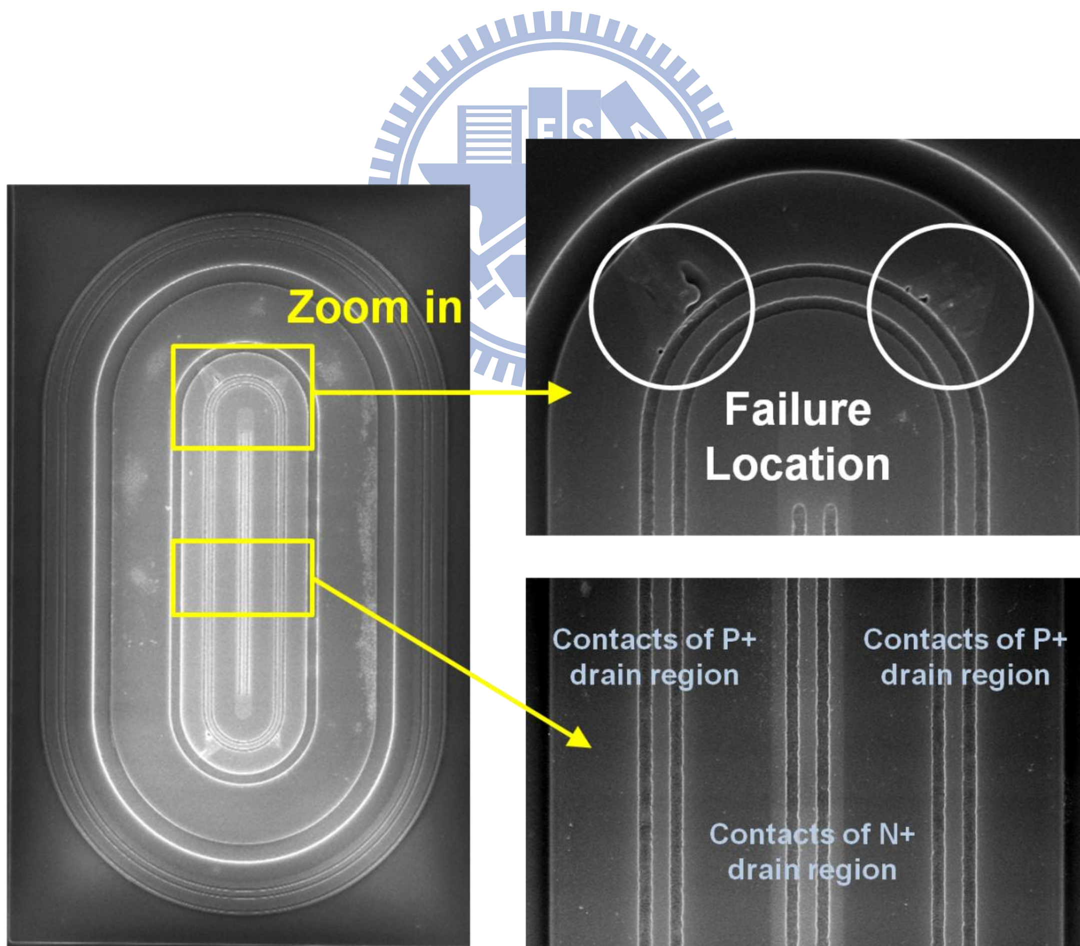


Fig. 3-21. SEM images of typical SCR-nLDMOS_A which suffers from a 6-kV HBM ESD stress.

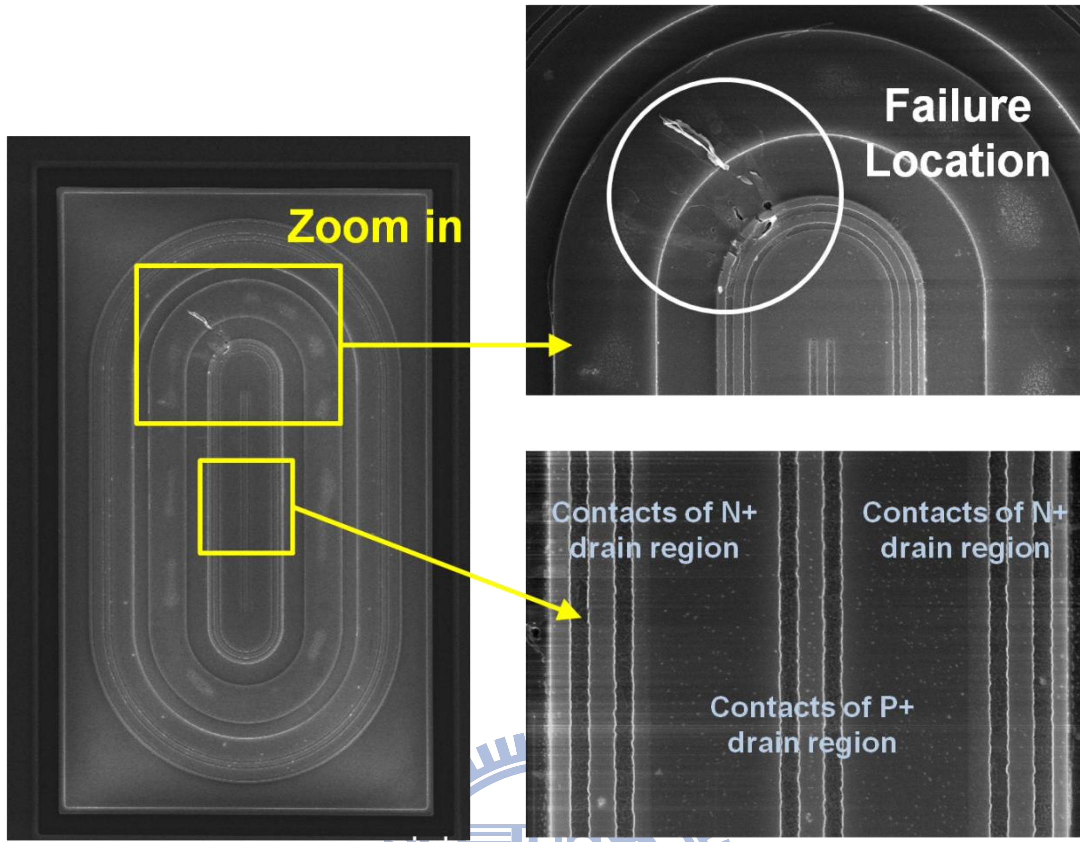


Fig. 3-22. SEM images of typical SCR-nLDMOS_B which suffers from a 0.5-kV HBM ESD stress.

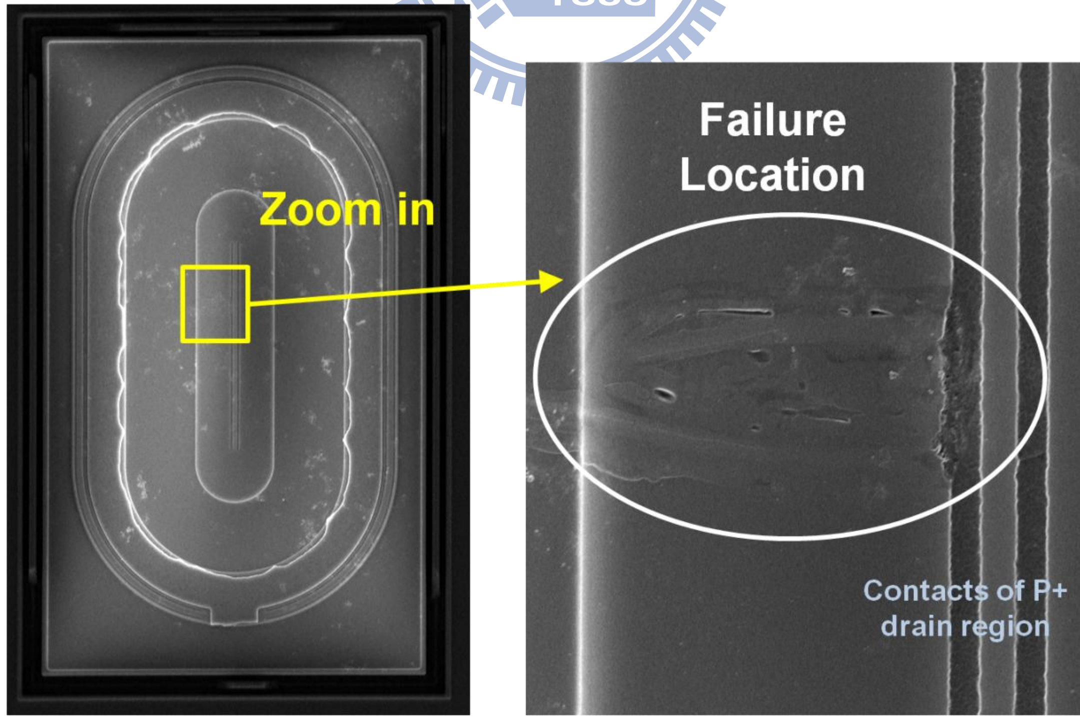


Fig. 3-23. SEM images of typical pLDMOS which suffers from a -0.5-kV HBM ESD stress.

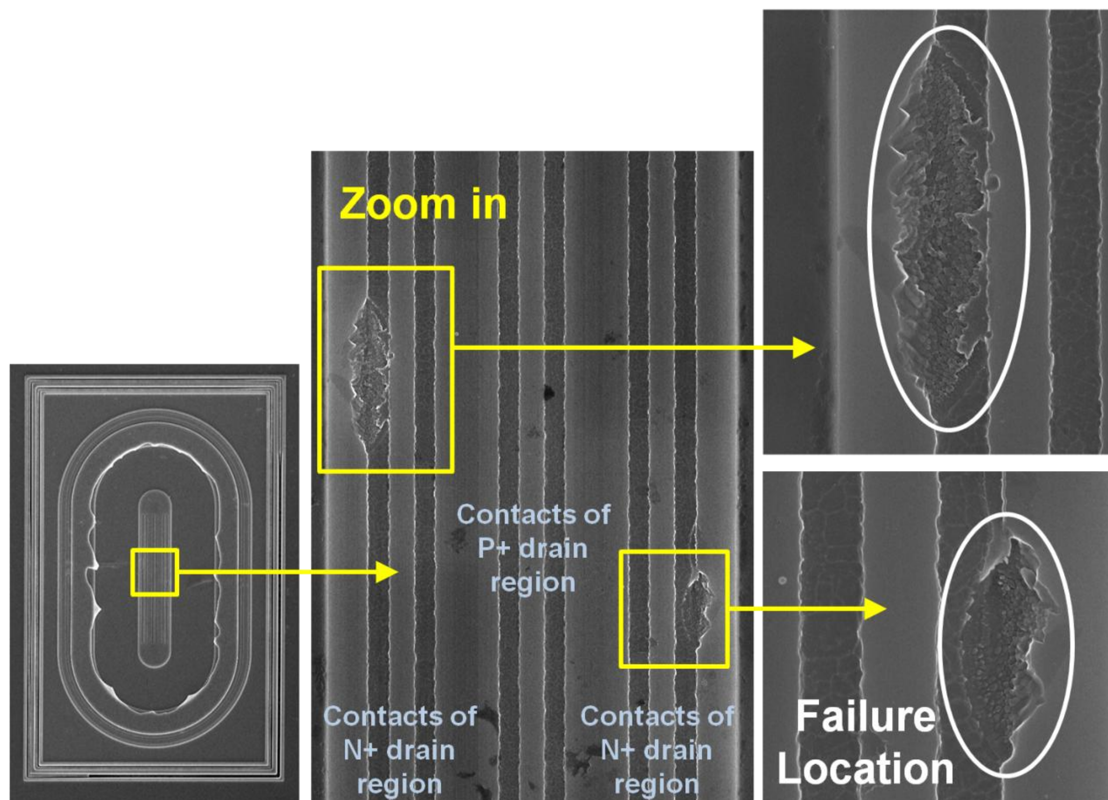


Fig. 3-24. SEM images of typical SCR-pLDMOS_A which suffers from a -3.5-kV HBM ESD stress.

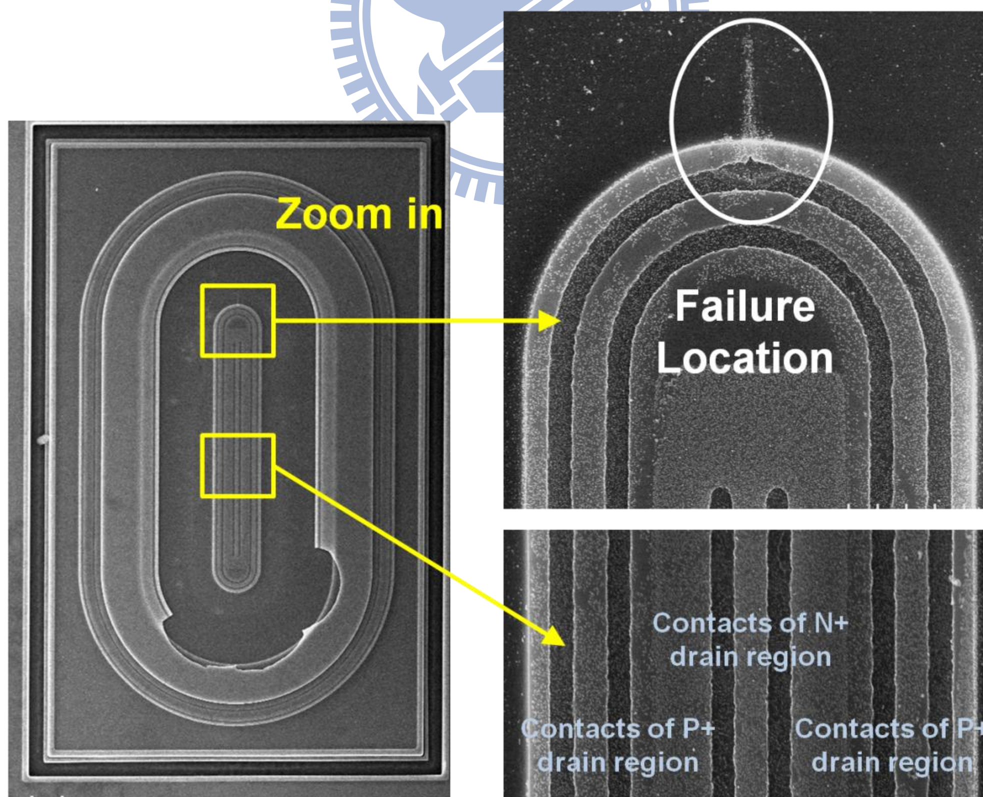


Fig. 3-25. SEM images of typical SCR-pLDMOS_B which suffers from a -0.5-kV HBM ESD stress.

3.3.3 The influence of layout parameters on ESD robustness

The investigation of layout parameters can be sorted into three parts. The part one is focused on the HV DMOS which fails while entering the snapback region. Secondly, the part two discusses the SCR-LDMOS_A which exhibits excellent failure current. The ineffectual layout parameters are discussed in the end.

Fig. 3-26 shows the failure current with different channel width (W). The I_{t2} of nLDMOS is proportional to channel width for W < 80 μm. For W > 80 μm, the I_{t2} gradually diminishes as a result of non-uniform turn-on effect. Similarly, the I_{t2} increases with increasing channel width for pLDMOS, as illustrated in Fig. 3-27.

The drift length (D) shown in Fig. 2-1(a) has considerable effect on I_{t2} for nLDMOS and circular_nLDMOS. The longer drift length, the higher energy the triggering of parasitic BJT needs. The energy is equal to the product of V_{DS}, I_{DS}, and pulse width of TLP. Hence, the I_{t2} increases with increasing drift length under the condition of approximately the same V_{DS} and fixed pulse width of TLP, as illustrated in Fig. 3-28.

The contact spike occurs at drain both for nLDMOS and pLDMOS; hence, the parameter at drain is critical to the ESD performance. The parameter "Y" represents the width of N+ drain for nLDMOS and P+ drain for pLDMOS, as illustrated in Fig. 2-1. The cross-sectional area of ESD current is enlarged by increasing Y; hence, it needs much more ESD current to cause contact spike at drain. As a result, the contact-spike-induced junction leakage occurs at higher ESD current when Y is increased. As illustrated in Fig. 3-29 and Fig. 3-30, I_{t2} is proportional to Y.

Fig. 3-31(a) shows the parasitic current path and resistor in SCR-nLDMOS_A. Failure analysis demonstrates that the main ESD current path is SCR path and the contact spike occurs at drain P^+ region; hence, the parameter Y has great influence on ESD performance. It needs much more ESD current to cause contact spike at drain

when the cross-sectional area of ESD current is enlarged by increasing Y. I_{t2} increases with increasing Y, as illustrated in Fig. 3.32. Furthermore, the wider T_d results in higher parasitic resistor (R). Taking the ESD current path of SCR and $BJT_{,NPN}$ into account, the ESD current prone to flow through SCR path due to the higher R. In other words, the portion of ESD current through $BJT_{,NPN}$ path which exhibits poor ESD performance decreased and the portion of ESD current through SCR path which exhibit excellent ESD performance increases with wider T_d. Consequently, I_{t2} is proportional to T_d, as illustrated in Fig. 3-33. The parameter T_s doesn't affect the parasitic current path and resistor, so T_s is ineffectual in improving ESD robustness.

Fig. 3-31(b) shows the parasitic current path and resistor in SCR-pLDMOS_A. Because the contact spike occurs at drain N^+ region, the parasitic current path which is related to drain P^+ region is neglect. Taking the ESD current path of SCR and $BJT_{,NPN}$ into account. The resistor (R) is higher with wider T_s, so the ESD current prone to flow through SCR path. In other words, the portion of ESD current through $BJT_{,NPN}$ path which exhibits poor ESD performance decreased and the portion of ESD current through SCR path which exhibit excellent ESD performance increases with wider T_d. Consequently, I_{t2} is proportional to T_s, as illustrated in Fig. 3-34. The parameter T_d doesn't affect the parasitic current path and resistor, so T_d is ineffectual in improving ESD robustness in SCR-pLDMOS_A.

Table 3.5 lists some ineffectual layout parameters for ESD level. The definitions of layout parameters are shown in Fig. 2-1, Fig. 2-3, and Fig. 2-6. The variation of ESD level is small; therefore, it is suggested that this parameters are ineffective to improve the ESD robustness.

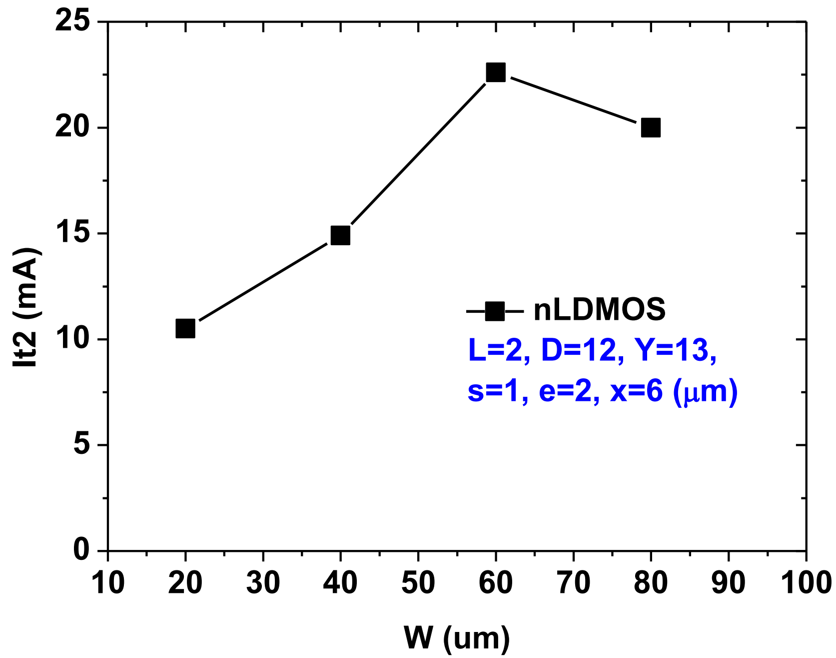


Fig. 3-26. The failure current under different channel width (W) for nLDMOS.

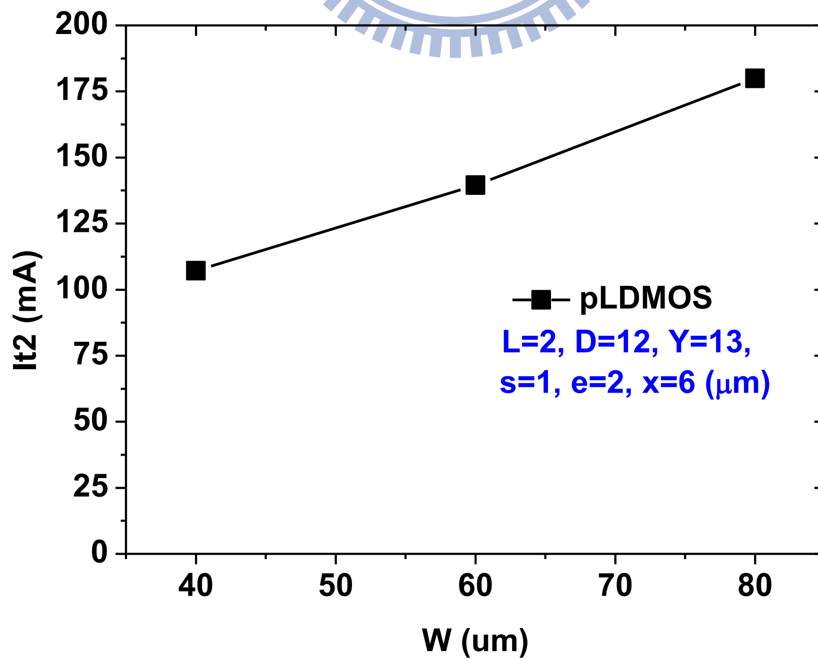


Fig. 3-27. The failure current under different channel width (W) for pLDMOS.

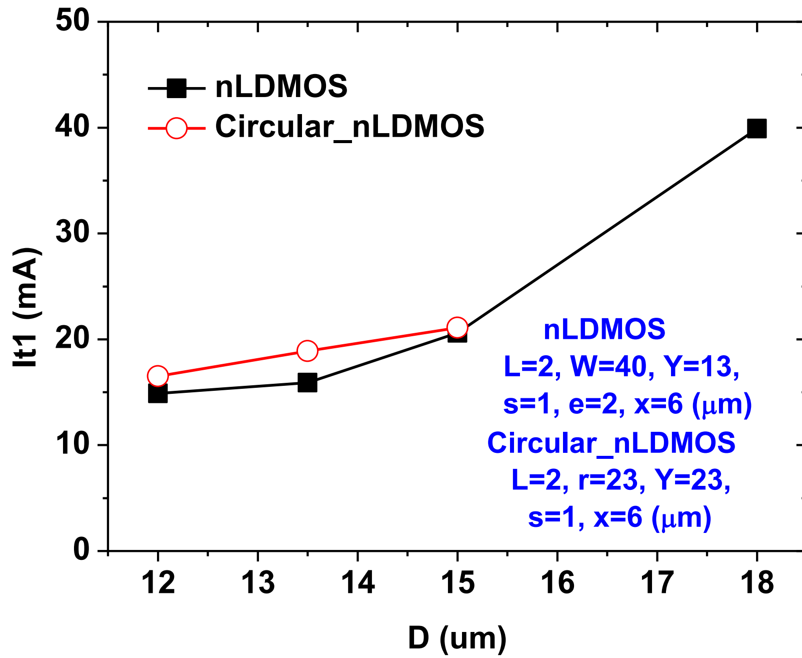


Fig. 3-28. The failure current under different Drift length (D) for nLDMOS.

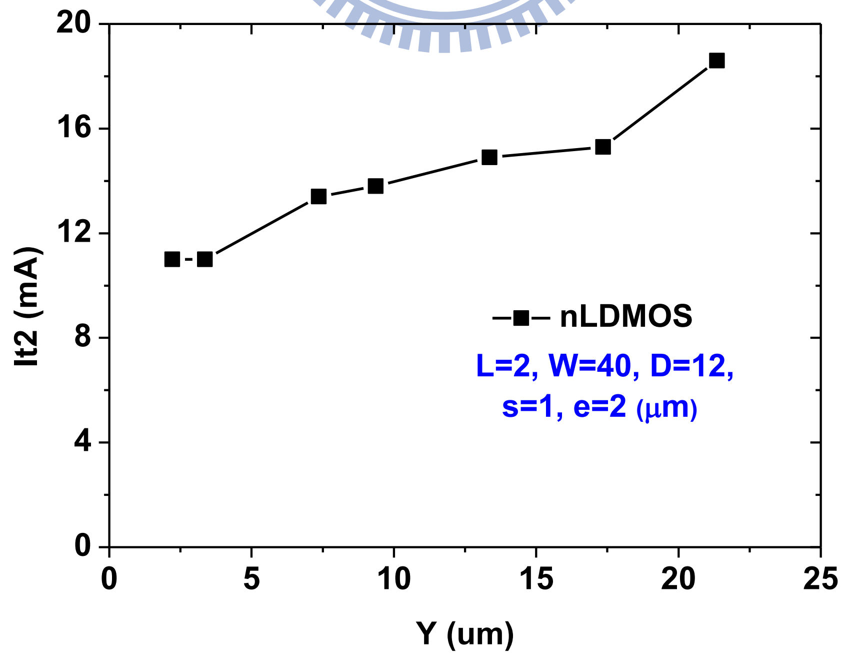


Fig. 3-29. The failure current under different Y for nLDMOS.

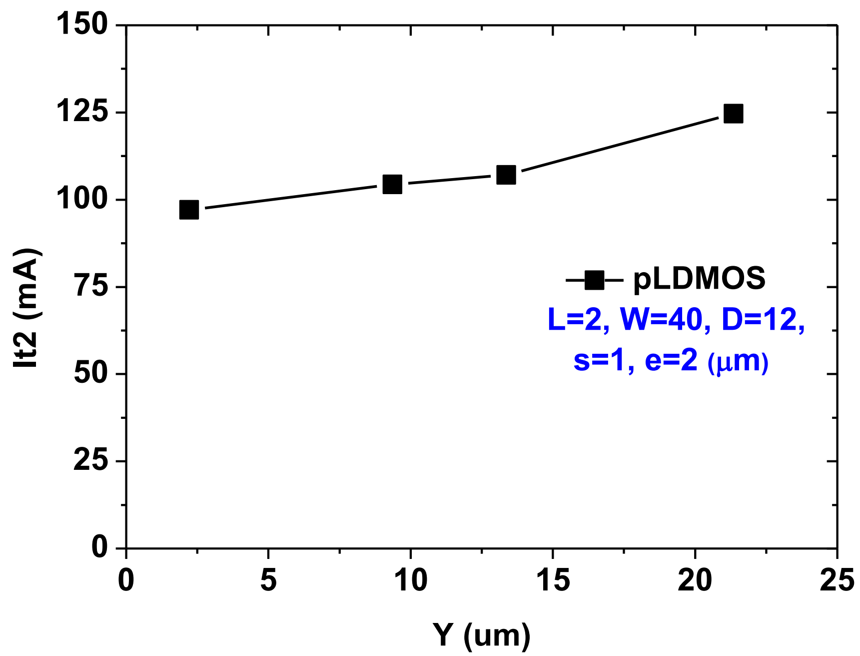
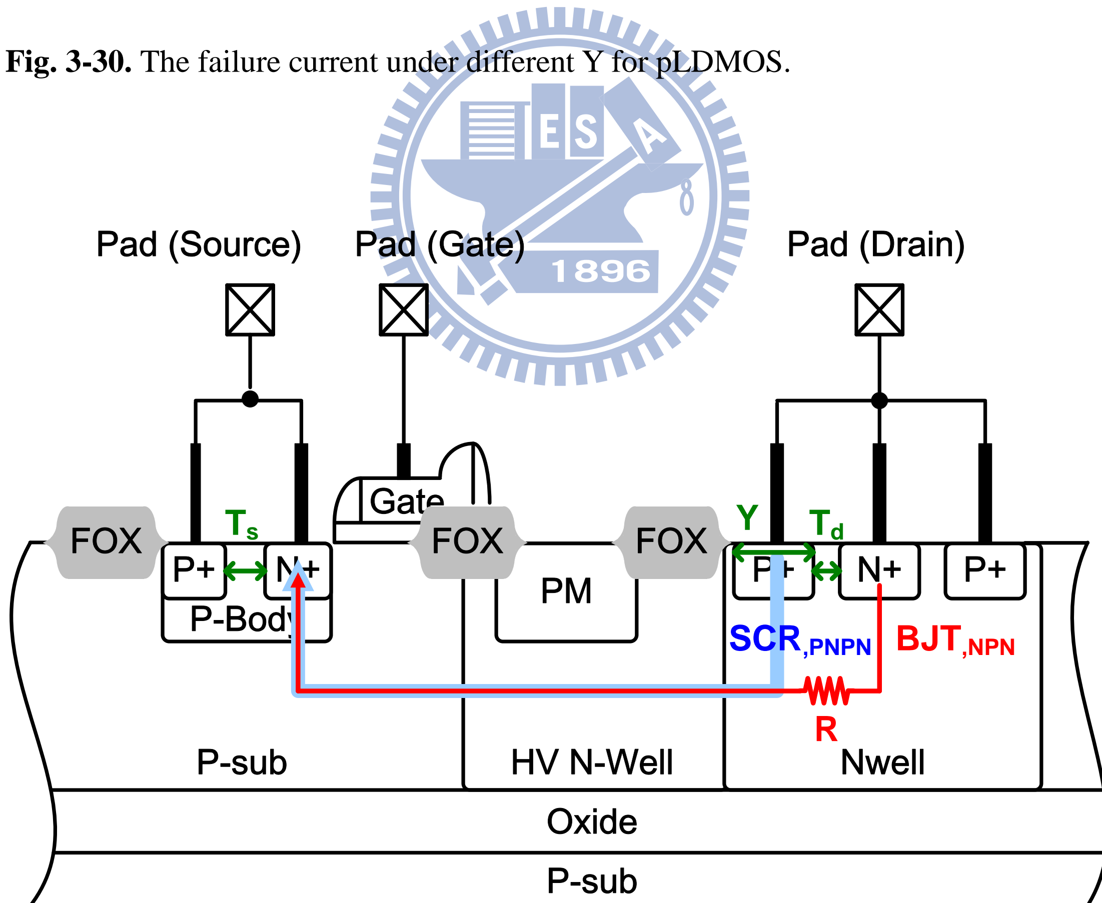
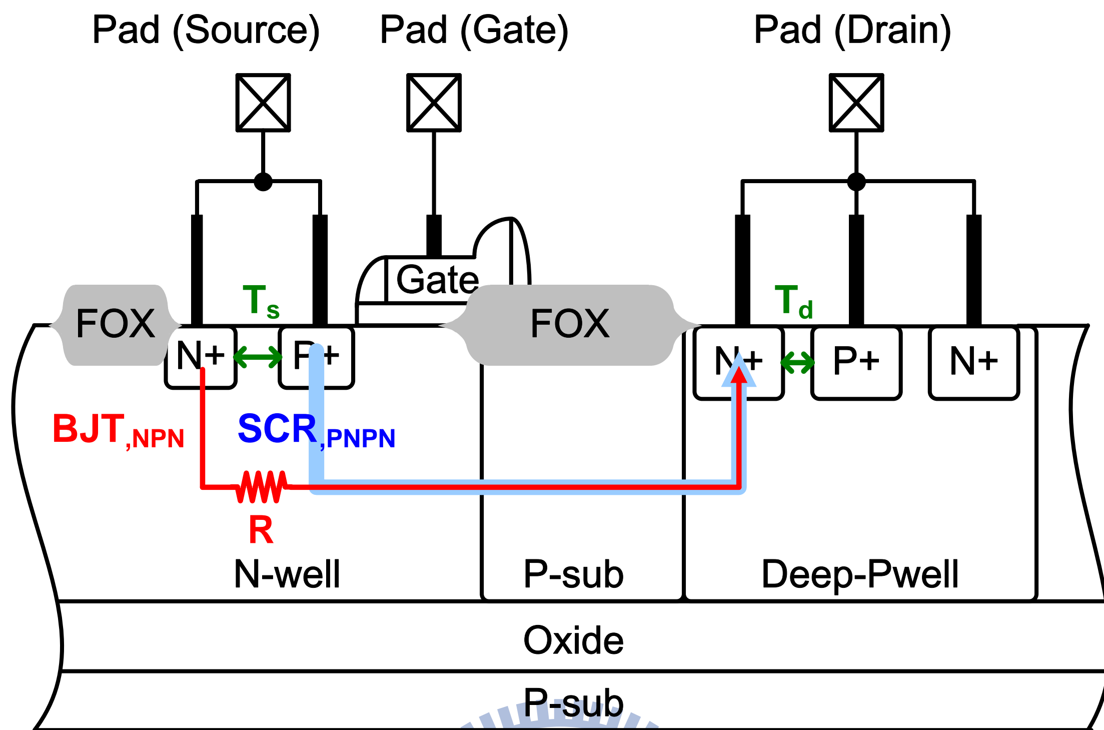


Fig. 3-30. The failure current under different Y for pLDMOS.



(a)



(b)

Fig. 3-31. The parasitic current path and resistor in (a) SCR-nLDMOS_A and (b) SCR-pLDMOS_A.

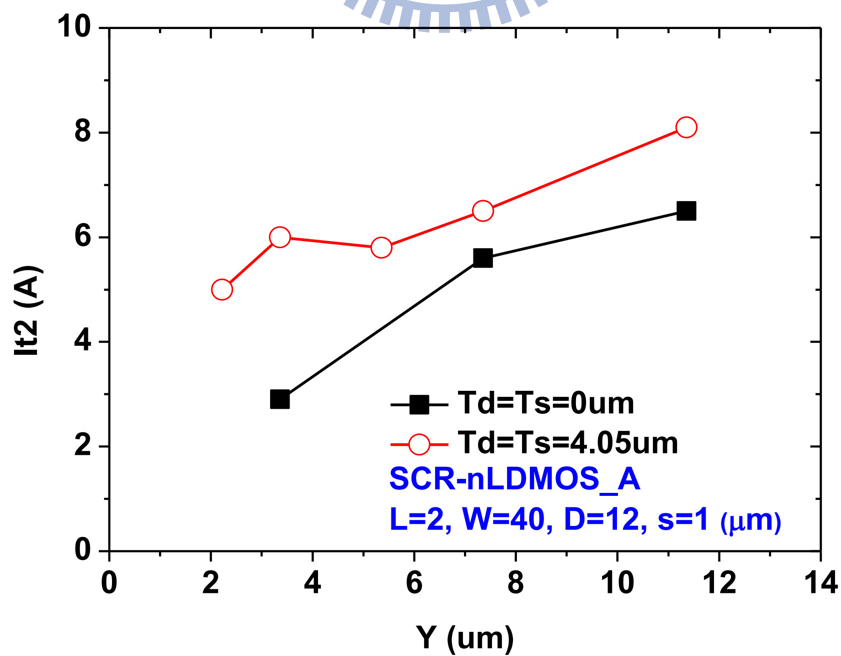


Fig. 3-32. The failure current under different Y for SCR-nLDMOS_A.

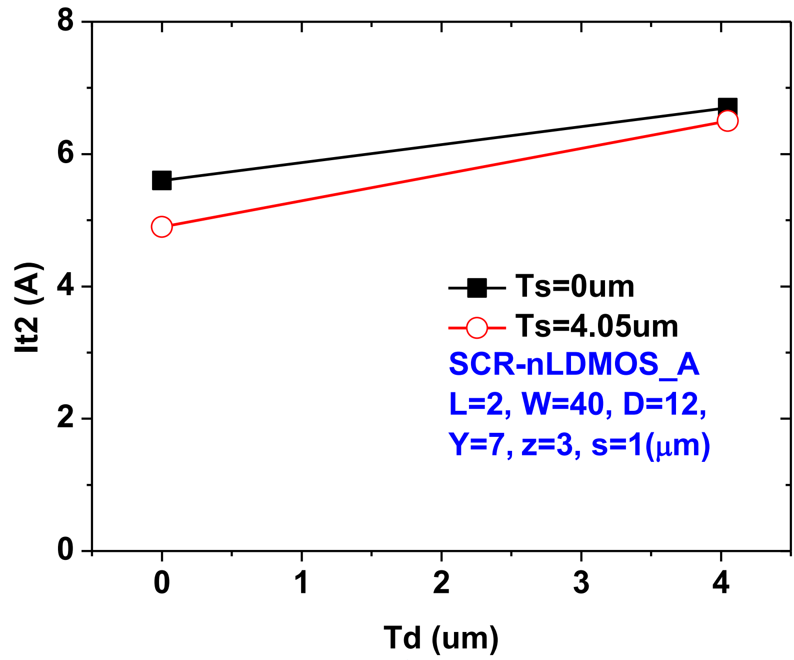


Fig. 3-33. The failure current under different spacing between the N^+ and P^+ at drain region (T_d) for SCR-nLDMOS_A.

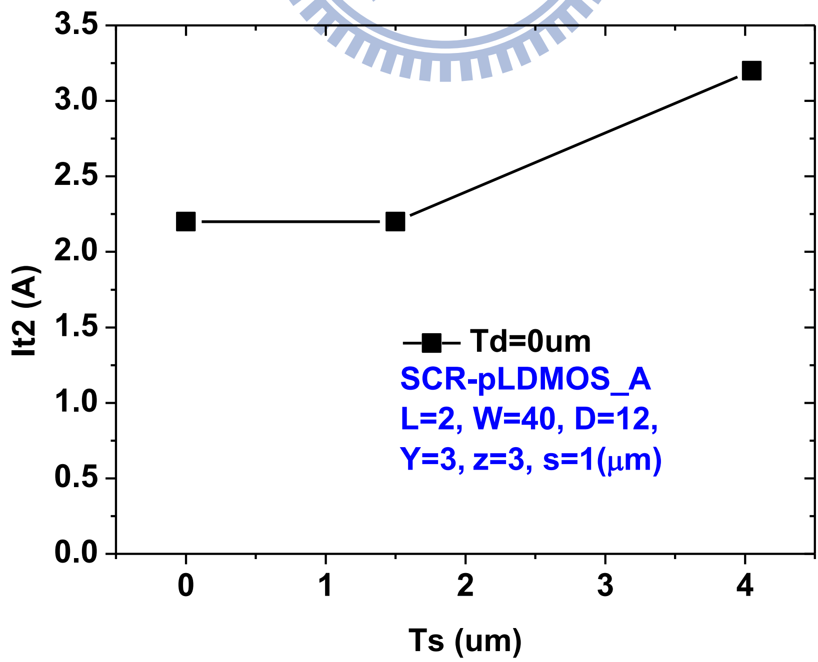


Fig. 3-34. The failure current under different spacing between the N^+ and P^+ at source region (T_s) for SCR-pLDMOS_B.

TABLE 3.5

The ineffectual layout parameters for ESD robustness.

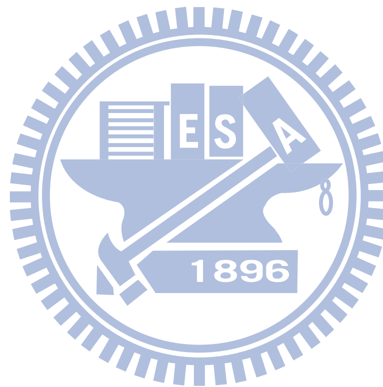
Device Structure	Fixed Parameters (μm)	Split Parameters (μm)	I_{t2} (A)
nLDMOS	**W = 40, D = 12, x = 6**	**L = 2 ~ 4, e = -2 ~ 5, s = 0.5 ~ 1**	**0.013 ~ 0.019**
Circular_nLDMOS	**R = 23, D = 12**	**L = 2 ~ 4, x = 2 ~ 8**	**0.016 ~ 0.018**
SCR-nLDMOS_A	**W = 40, D = 12, T_d = 4.05, z = 3**	**T_s = 0 ~ 4.05, s = 0.43 ~ 1.5**	**6.5 ~ 6.8**
SCR-nLDMOS_B	**W = 40, D = 12, s = 1, z = 3**	**T_d = 0 ~ 4.05, T_s = 0 ~ 4.05**	**0.006 ~ 0.008**
SCR-pLDMOS_A	**W = 40, D = 12,T_s = 0**	**T_d = 0 ~ 4.05, s = 1 ~ 3**	**2.1 ~ 2.3**
SCR-pLDMOS_B	**W = 40, d = 12, s = 1, z = 1**	**T_d = 0 ~ 4.05, T_s = 0 ~ 4.05**	**0.035 ~ 0.056**

3.3.4 Summary

The failure analysis demonstrates that SCR-LDMOS_B acts as LDMOS while entering the high current region; consequently, the insertion of SCR is ineffective to improve ESD robustness for SCR-LDMOS_B. On the contrary, SCR-LDMOS_A exhibits excellent ESD robustness. The arrangement of placing embedded SCR significantly affects the ESD robustness.

For nLDMOS, I_{t2} per unit width (W) gradually diminishes with increasing W as a result of non-uniform turn-on effect. I_{t2} increases with increasing drift length (D) and parameter Y. The parameter Y and the spacing between N^+ and P^+ at drain region

(T_d) are critical for SCR-nLDMOS_A. Hence, the I_{t2} increases with increasing Y and T_d for SCR-nLDMOS_A. The I_{t2} increases with increasing T_s for SCR-pLDMOS_A. Moreover, some ineffectual layout parameters listed in Table 3.5 has no influence on ESD level. Hence, it is suggested that this parameters are ineffective in improving the ESD robustness.



Chapter 4

Investigation on Safe Operating Area (SOA) and Experimental Results

4.1 Introduction to SOA

Many applications require power devices to operate under the condition of high voltage and high current simultaneously, so it is important to quantify the ability to withstand the high power. The SOA defines the operating limits without damaging the IC products. The "SOA" is the abbreviation of "Safe Operating Area", that is, power devices can operate and switch safely inside this area. Furthermore, the SOA is classified according to the duration of high power. If the duration of high power is long enough to generate the energy as heat, the device is destroyed due to the heat instead of instantaneously electrical power.

4.1.1 Classification of SOA

The high-voltage devices have various applications such as display driver integrated circuits, power supplies, power management and automotive electronics. The bias condition is different among the applications of high-voltage devices. To take account of all possible bias conditions, SOA is roughly sorted into forward bias SOA (FBSOA) and reversed bias SOA (RBSOA) [8]. FBSOA analyzes the on-state devices and RBSOA studies the off-state devices. The FBSOA specification takes the form illustrated by the sketch in Fig. 4-1. The FBSOA is the region inside the connection of the six points A, B, C, D, E and F.

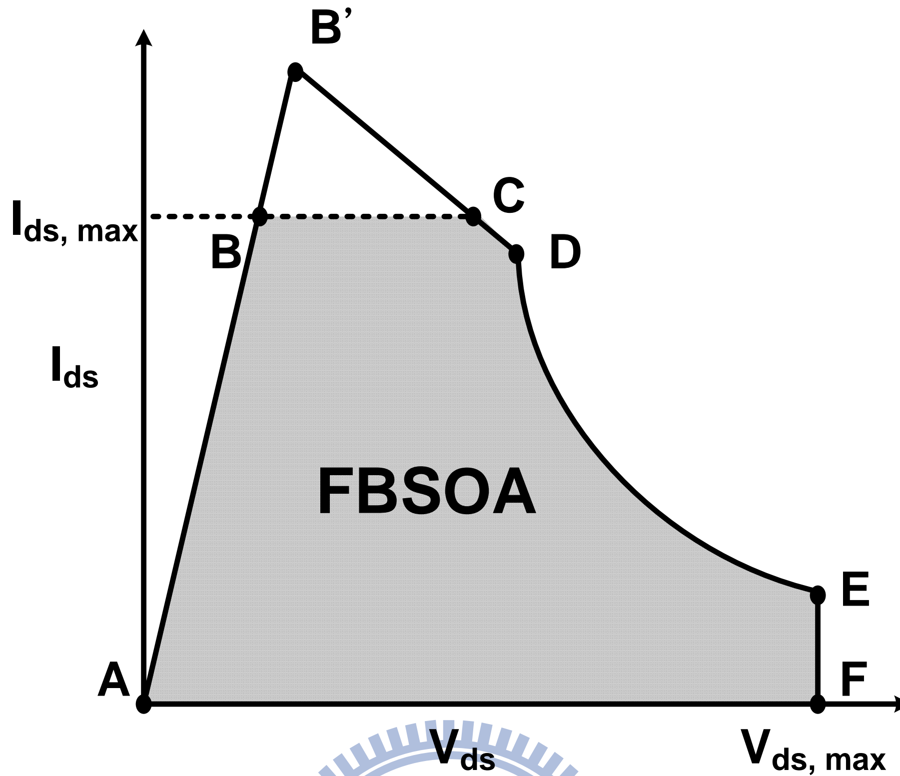


Fig. 4-1. Forward bias safe operating area (meshed region) [8].

The five curves illustrated at Fig. 4-1 have respectively definition and meaning [8]:

(1) Line of AB'

The on-resistance which is limited by the current capability. Increasing the slope of line AB' with decreasing the on-resistance can obtain the better SOA.

(2) Line of BC

$I_{ds,\ max}$ is the maximum allowable drain current of on-state. The bonding wires between the device and the package terminals will melt as the I_{ds} continuously exceed the $I_{ds,\ max}$.

(3) Line of B'D

The maximum average power dissipation curve which can be expressed as $I_{ds}*V_{ds} = P_{Dmax}$ (at $T_C = T_{C0}$), where T_C is the transistor-case (package) temperature

and P_{Dmax} is the maximum average power dissipation [28]. It is mainly determined by the heat-sinking capability of the packaged device. Fig. 4-2 shows the typical P_{Dmax} versus T_C curve, where θ_{JC} is the thermal resistance between junction and transistor case. The power dissipation is allowed to temporarily exceed the curve; however, the average power dissipation can't above the curve. The curve shifts to satisfy the equation $I_{ds}*V_{ds} = P_{Dmax}$ (at T_C) for the transistor-case temperature T_C is larger than T_{C0}.

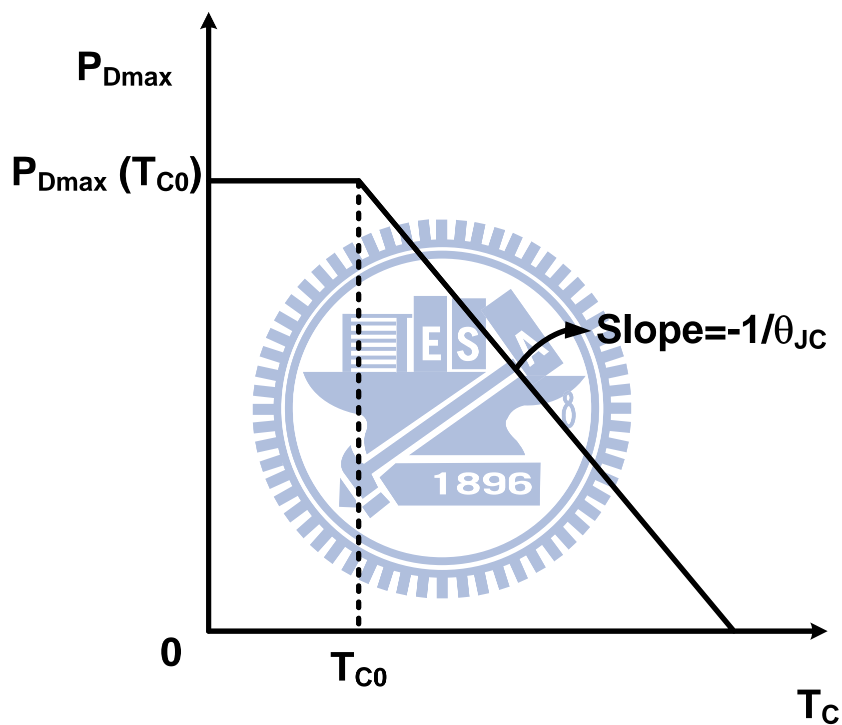


Fig. 4-2. Maximum allowable power dissipation versus device-case temperature [28].

(4) Line of DE [8] [9] [29]

The curve of electrical SOA (eSOA). This is the locus of the trigger points which are measured by TLP system under fix TLP pulse width and different gate bias. Fig. 4-3 and Fig. 4-4 respectively demonstrate the measured circuit and the typical eSOA measured by 100-ns TLP system. The device under test is typical nLDMOS. The parasitical BJT of transistor turns on and enters the snapback region if the operating

point is temporarily above the curve. The mechanism of generating hot carrier and turning on the parasitical BJT of transistor is impact ionization for eSOA [29]. The high electrical field in the depletion region accelerates the carriers. The carriers get sufficient kinetic energy and transfer it into potential energy. The abundant electron-hole pairs make the junction breakdown and turn on the parasitical BJT. The critical condition of turning on the parasitical BJT is $V_{BE} = I_{BE} * R_{BE} > V_{BE,ON} \sim 0.7$ V.

Fig. 4-5 demonstrates the eSOA measured by the 200-ns TLP system. The 200-ns eSOA is narrower than 100-ns eSOA. The energy which a device can withstand is constant. In addition, the energy of TLP pulse is equal to the product of V_{DS}, I_{DS}, and the pulse width of TLP. Hence, the eSOA boundary degrades with increasing pulse width of TLP, as illustrated in Fig. 4-6.

Latch up occurs when $V_{hold} < V_{DD}$, where V_{hold} is the holding voltage. Besides, the high-voltage devices usually suffer permanent damage when they just enter the snapback region. In conclusion, the eSOA is the limit of normal operation.

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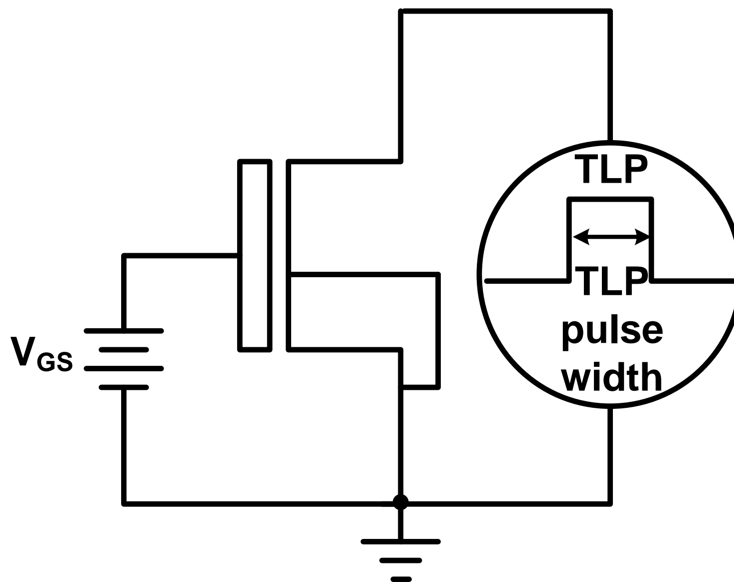


Fig. 4-3. The test circuit of eSOA.

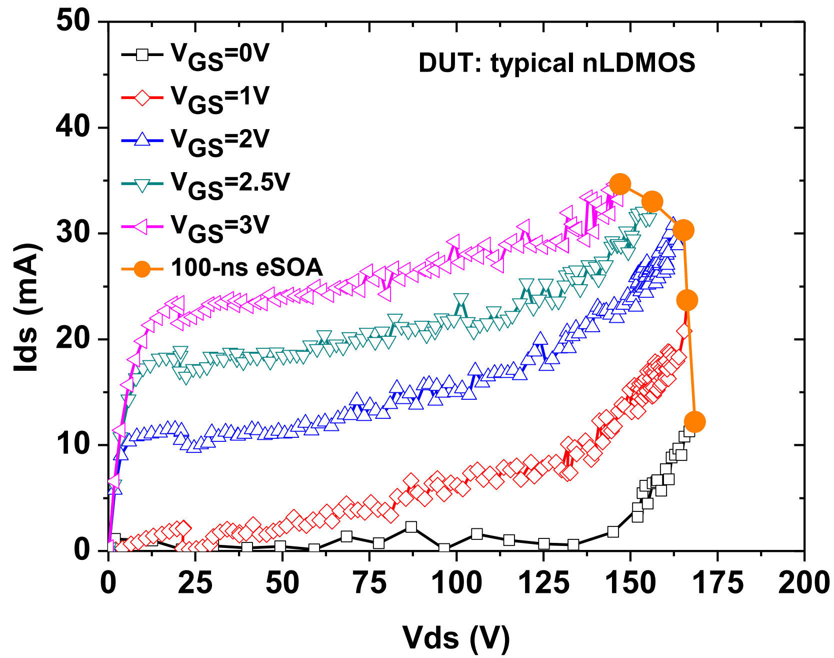


Fig. 4-4. The I-V characteristics measured by 100-ns TLP system. The 100-ns eSOA boundary is shown in orange color and circular symbol.

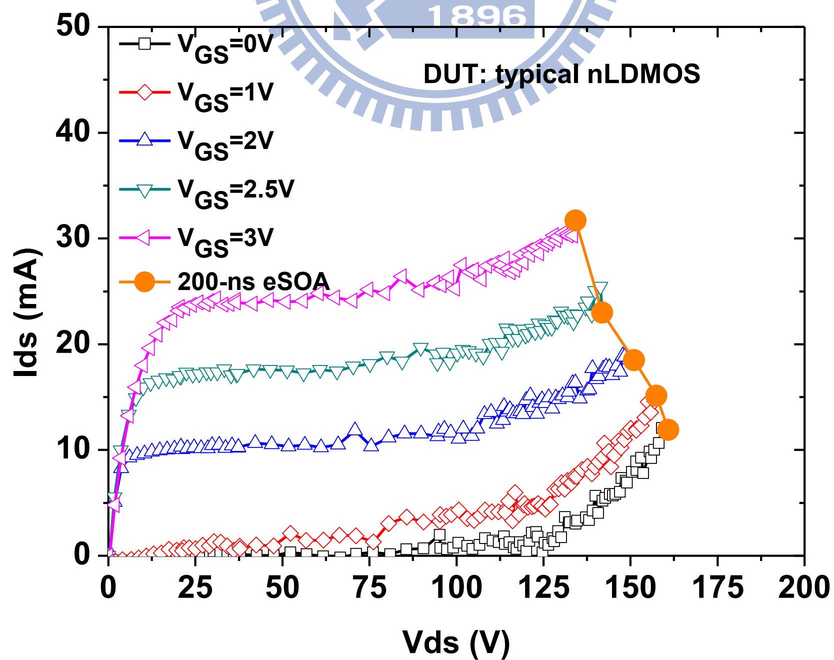


Fig. 4-5. The I-V characteristics measured by 200-ns TLP system. The 200-ns eSOA boundary is shown in orange color and circular symbol.

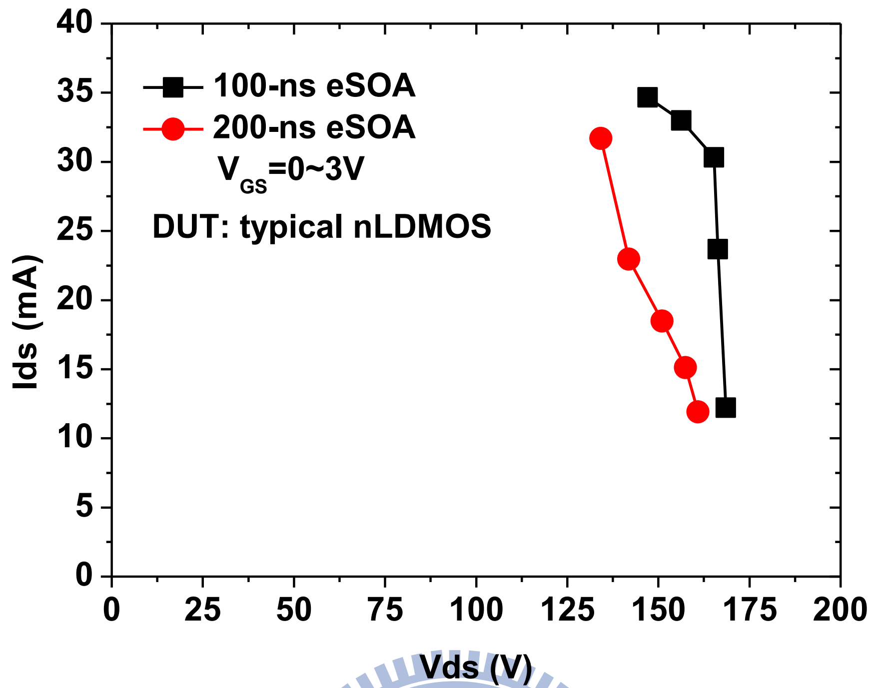


Fig. 4-6. The comparison of eSOA with different pulse width of TLP.

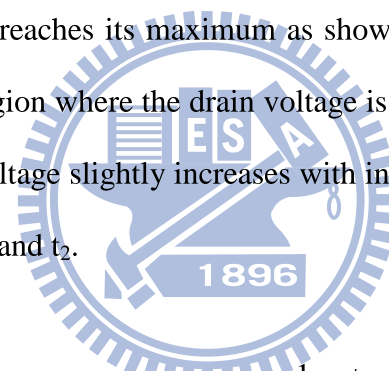
(5) Line of EF

The maximum operating voltage ($V_{ds,max}$) is generally determined by eSOA with zero gate bias, $V_{ds,\,max} = V_{t1}$ ($V_{gs} = 0$ V). The transistor will enter the snapback region and be damaged if the operating point is instantaneously above $V_{ds,\,max}$.

FBSOA is decided by the factors such as manufacture, material, package and device structure. The emphasis of FBSOA is eSOA in this thesis. On the other hand, RBSOA is the allowed operation range when the device is off but forced to conduct current. The information of RBSOA is important for the applications such as flyback convertor. The voltage and current of transistor are simultaneously high during the inductive switch which can result in catastrophic damage. The unclamped inductive switch (UIS) [30] [31] which is the most popular test method of RBSOA is established to estimate the capability to sustain the stress of inductive switch. The detailed information is discussed in the following chapter.

4.1.2 Characteristic of Unclamped Inductive Switch (UIS)

Fig. 4-7 demonstrates the test circuit of UIS and Fig. 4-8 shows the typical waveform of UIS. The DUT in Fig. 4-8 is typical nLDMOS. The voltage pulse which amplitude is equal 5 V (V_{GS}) is applied to gate pad through R_{gs}. The R_{gs} protects the gate oxide from direct damage which results from voltage pulse of V_{GS}. The voltage pulse width of V_{GS} is named as T_p and the inductive current is named as I_{switch}, as illustrated in Fig. 4-7 and Fig. 4-8. The waveform can be divided by nodes of t_1, t_2, and t_3. The voltage pulse (V_{GS}) is applied to gate pad through R_{gs} during the period of time between t_1 and t_2. The DUT is turned on and the drain current (I_{ds}) is equal to the I_{switch}. Moreover, the I_{switch} increases with time according to the equation (4.1) when the DUT is on. The I_{switch} reaches its maximum as shown in equation (4.2). Besides, the DUT is at the linear region where the drain voltage is proportional to drain current. Consequently, the drain voltage slightly increases with increasing drain current during the time period between t_1 and t_2.



$$I_{ds}(t') = I_{switch}(t') = \frac{1}{L_{ext}} \int_{t_1}^{t'} V_{cc}\, dt \tag{4.1}$$

$$I_{ds,max} = I_{switch,max} = I_{switch}(t_2) = \frac{V_{cc} \bullet T_p}{L_{ext}} \tag{4.2}$$

The I_{switch} degrades when the voltage pulse is removed. The inductive current gradually decreases with time according to the equation (4.3). The channel of DUT is off but forced to conduct the inductive current; hence, the DUT is compelled in a state of avalanche breakdown. In consequence, the drain voltage (V_{ds}) reaches a maximum ($V_{ds,max}$). The drain voltage and drain current of DUT are simultaneously high during the period of time between t_2 and t_3. Equation (4.4) shows the total energy that the

DUT withstands during the inductive switch. The energy may results in catastrophic damage. To quantify the ability to withstand the avalanche energy during the inductive switch, it is defined that the maximum allowable UIS $I_{switch,max}$ is the inductive current when the DUT reach is maximum allowable E_{AS}.

$$I_{ds}(t') = I_{switch}(t_2) + \frac{1}{L_{ext}} \int_{t_2}^{t'} (V_{cc} - V_{ds}) dt \tag{4.3}$$

$$E_{AS} = \int_{t_2}^{t_3} (V_{ds} \bullet I_{ds}) dt \tag{4.4}$$

The inductive current is equal to 0 A at time of t_3. Hence, drain voltage is restored to V_{cc} after time of t_3. Fig. 4-9 shows the circuit trajectory of UIS. The definition time of t_1, t_2, and t_3 are identical to that in Fig. 4-8. The drain current increases with time during the period of time between t_1 and t_2. The DUT is at linear region; as a result, the drain voltage slightly increases with increasing I_{ds}. The drain current and drain voltage reach their maximum ($I_{switch,max}$ and $V_{ds,max}$) at t_2. In Fig. 4-9 (a), the drain current and drain voltage degrade with time during the period of time between t_2 and t_3. The drain current is equal to 0 A and the drain voltage is return to V_{cc} at t_3. If the unstable state is over the boundary of eSOA as illustrated in Fig. 4-9 (b), the DUT will enter the snapback region and the drain current will increase until the DUT is failed. Hence, it is important to ensure that operates the DUT inside the boundary of eSOA.

The aim of following test is to verify the equation (4.2). Fig. 4-10 shows the waveform of inductive current with different power supply (V_{cc}). The fixed parameters are T_p and L_{ext}. Hence, the $I_{switch,max}$ is proportional to V_{cc} as illustrated in Fig. 4-11.

Fig. 4-12 demonstrates the waveform of inductive current with different pulse

width (T_p). The fixed parameters are V_{cc} and L_{ext}. The slope of current waveform during the period time between t_1 and t_2 is equal to a constant, as shown in equation (4.5). Accordingly, $I_{switch,max}$ is proportional to T_p as illustrated in Fig. 4-13.

$$Slope = \frac{V_{cc}}{L_{ext}} = c \tag{4.5}$$

where c is a constant for fixed V_{CC} and L_{ext}. Fig. 4-14 demonstrates the waveform of inductive current with different inductive impedance (L_{ext}). The fixed parameters are T_p and L_{ext}. According to equation (4.2), $I_{switch,max}$ is reciprocal to L_{ext} as illustrated in Fig. 4-15. Moreover, the DUT is failed when the inductive impedance is equal to 1 mH. Fig. 4-16 shows the waveform with L_{ext} = 1 mH. The unstable state is outside the boundary of eSOA as shown in Fig. 4-9 (b) for L_{ext} = 1 mH. Hence, the drain current increases until the DUT is failed. The DUT is short and the drain voltage is equal to 0 V in the end.

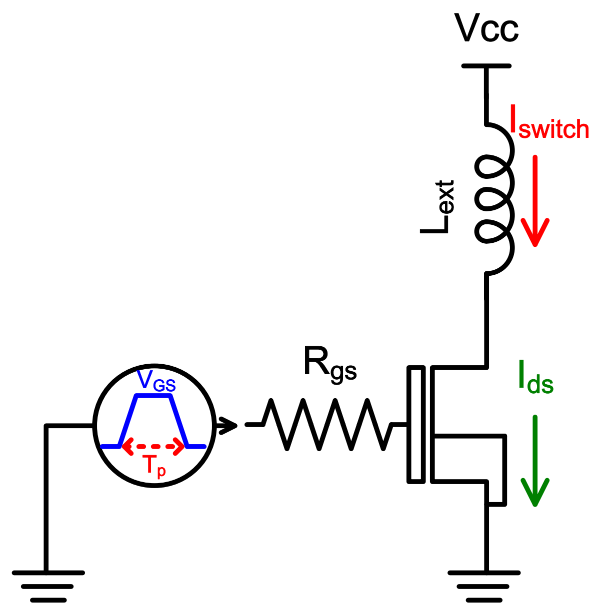


Fig. 4-7. The test circuit of unclamped inductive switch [30].

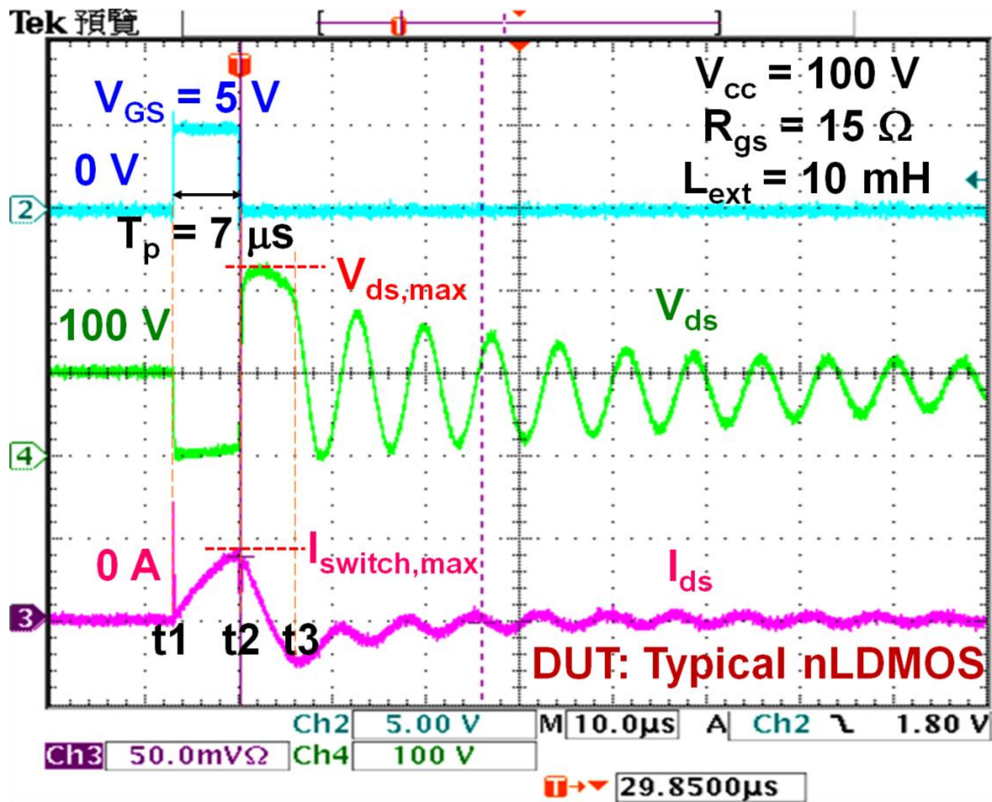


Fig. 4-8. The waveform of unclamped inductive switch.

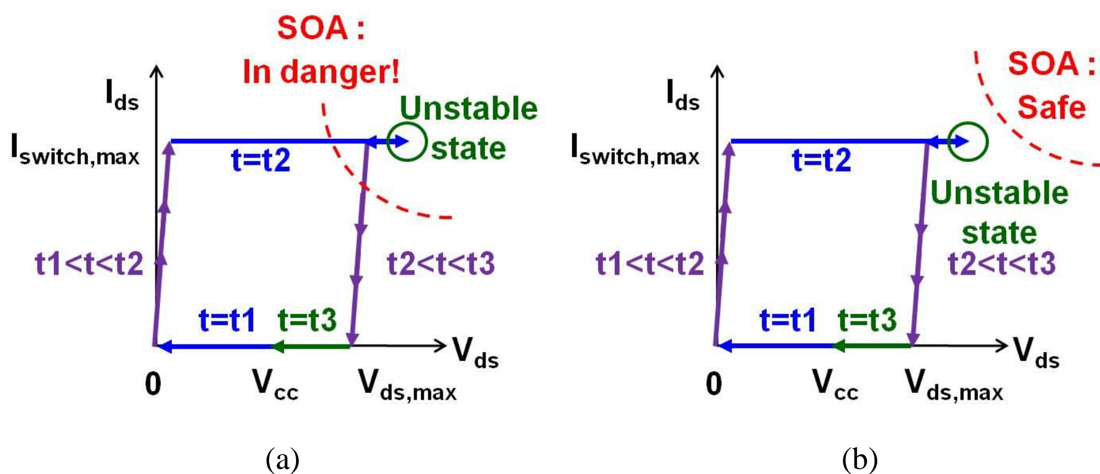


Fig. 4-9. The circuit trajectory of unclamped inductive switch. The unstable state is (a) inside and (b) outside the boundary of eSOA.

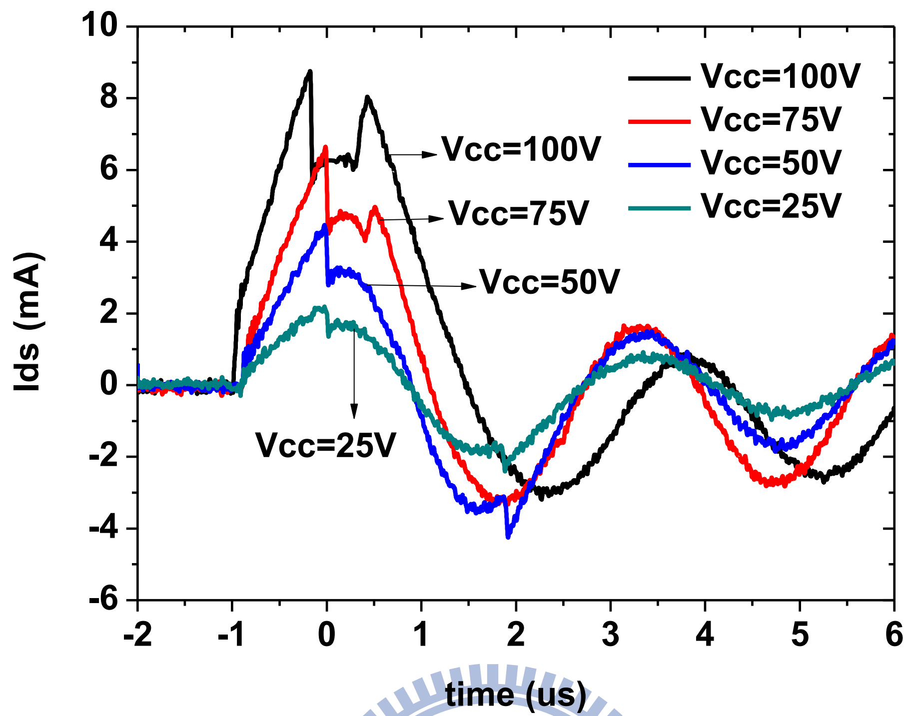


Fig. 4-10. The waveform of inductive current with different power supply (V_{cc}).

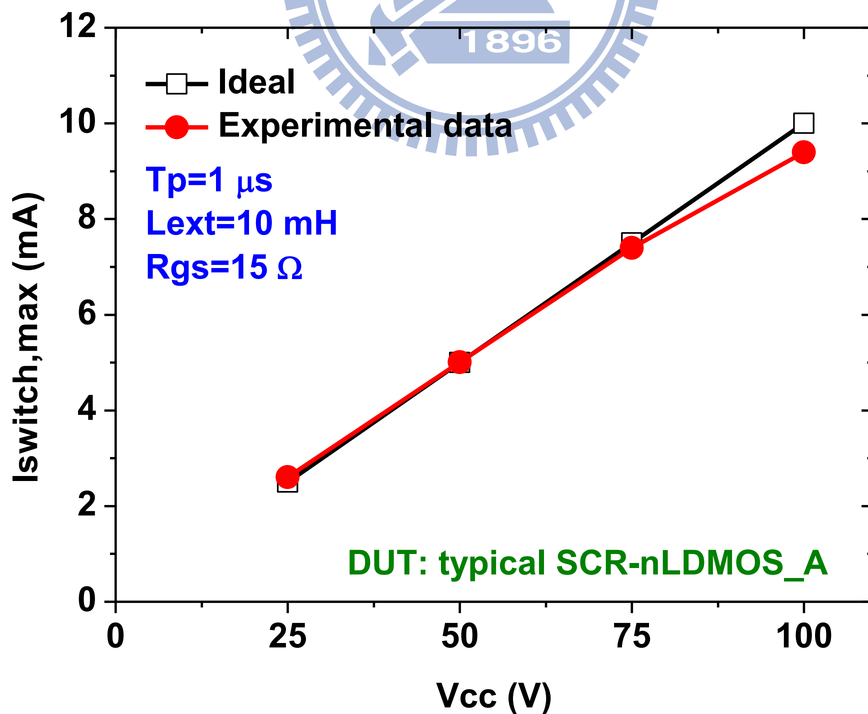


Fig. 4-11. The inductive current with different power supply (V_{cc}).

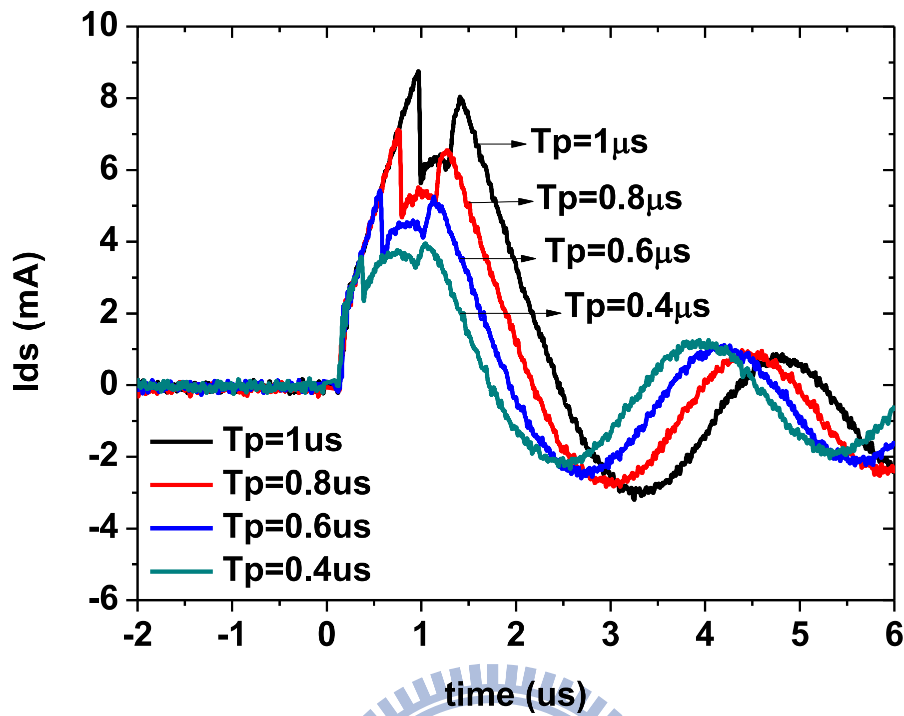


Fig. 4-12. The waveform of inductive current with different pulse width (T_p).

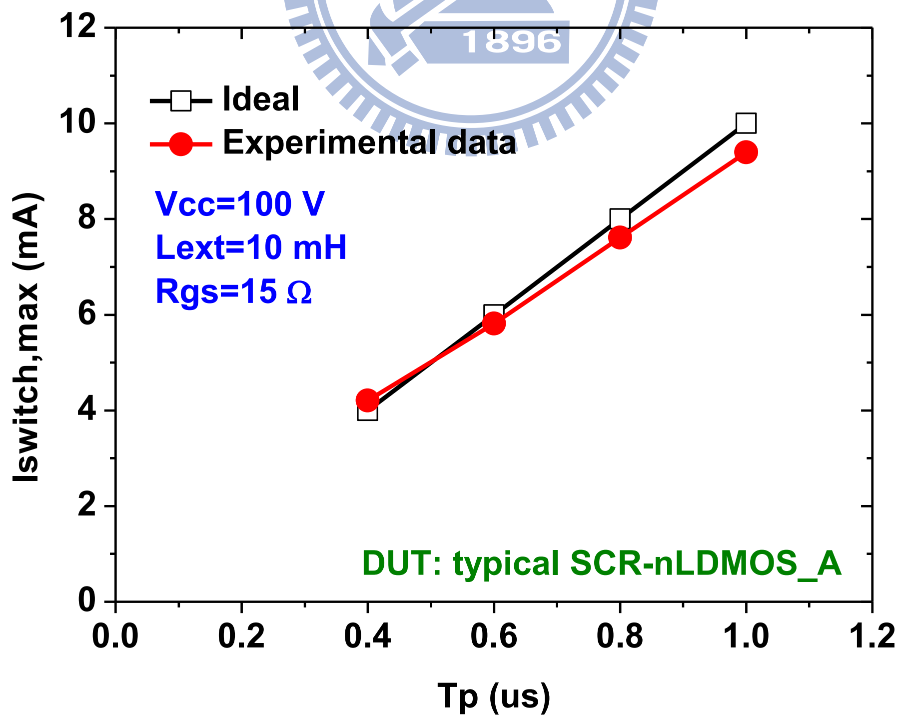


Fig. 4-13. The inductive current with different pulse width (T_p).

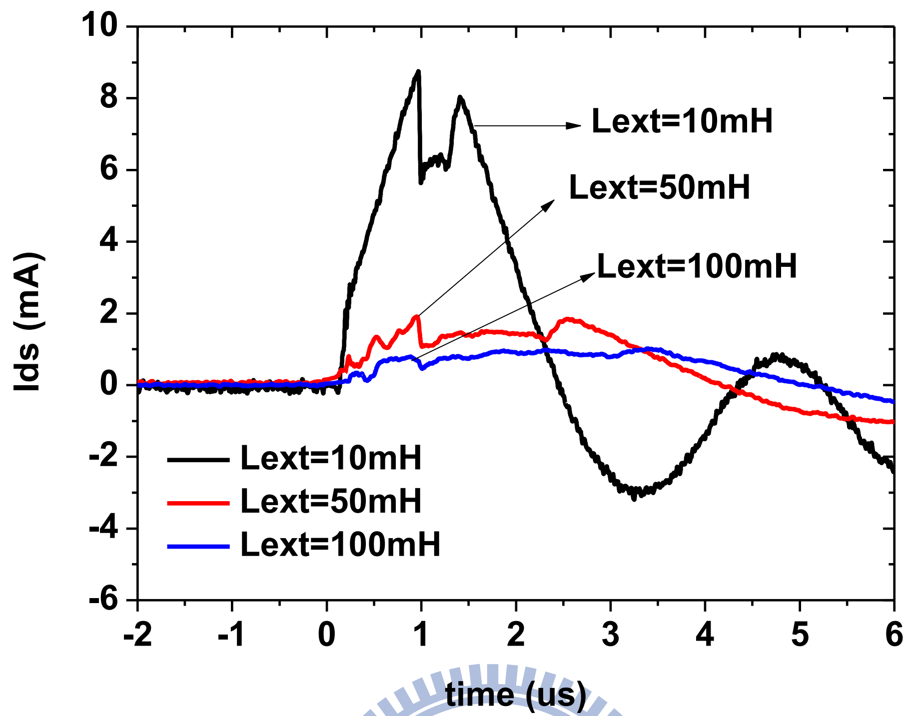


Fig. 4-14. The waveform of inductive current with different inductive impedance (L_{ext}).

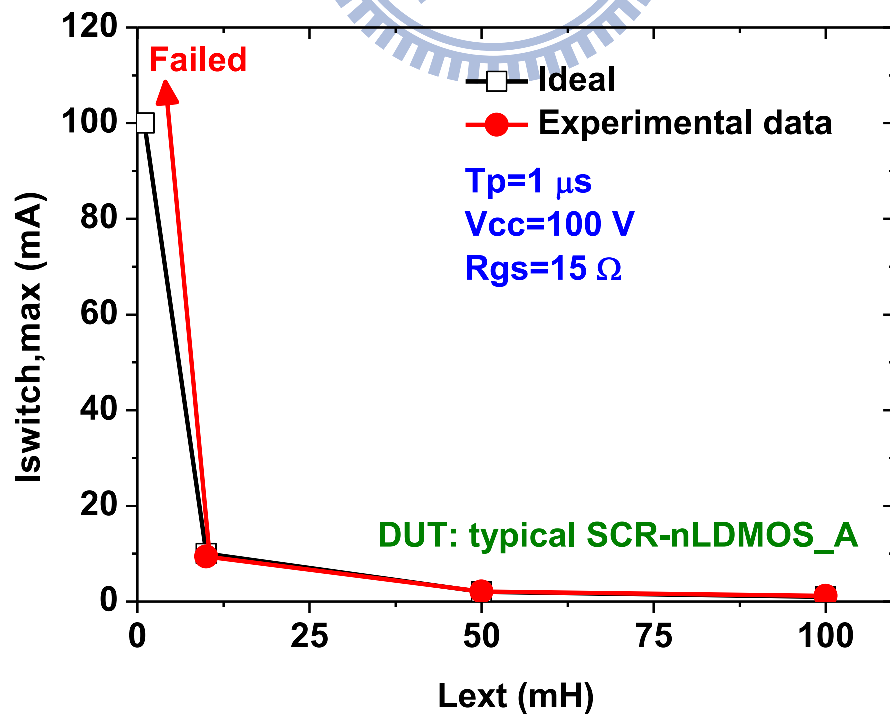


Fig. 4-15. The inductive current with different inductive impedance (L_{ext}).

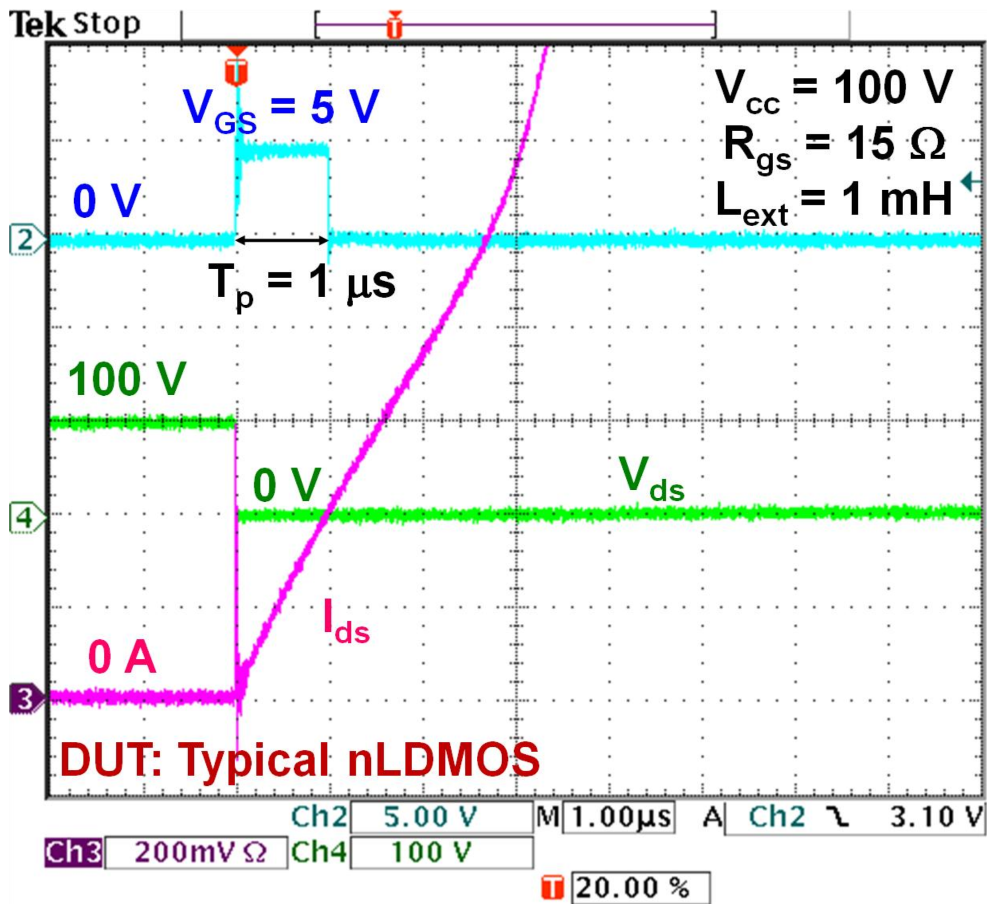


Fig. 4-16. The waveform of UIS when device is failed.

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The energy stored in the inductor totally transfers into the DUT during the UIS stress. The maximum energy that the DUT can withstand during the UIS stress is constant. Moreover, the energy stored in the inductor is proportional to L_{ext} as shown in equation (4.6).

$$Energy = \frac{I_{switch,max}{}^2 \bullet L_{ext}}{2} \quad (4.6)$$

Hence, the max. allowable UIS $I_{switch,max}$ is reciprocal to the L_{ext}, as shown in Fig. 4-17.

Fig. 4-18 and Fig. 4-19 respectively show the waveform of drain voltage and

drain current with different gate bias.

To investigate the influence of gate bias on the UIS characteristic, the UIS tests with different amplitude of gate voltage pulse. For the amplitude of gate voltage pulse is larger than 1.5 V, the I_{ds} increases with time. User can adjust the parameters of T_p, V_{cc}, and L_{ext} to get the proper operating current. For the amplitude of gate voltage pulse is smaller than 1.5 V, the Ids is limited by the DMOS channel current. Hence, it can't reach normal operating current at real application.

To take the accuracy of Iswitch into account, the UIS tests as illustrated in Fig. 4-20 and Fig. 4-21 is repeated with different sample whose device structure and layout parameters are the same. Table 4-1 lists the corresponding values of UIS $I_{switch,max}$ and $V_{ds,\ max}$ in Fig. 4-21 and Fig. 4-21. The standard deviation of UIS $I_{switch,max}$ is slight. The standard deviation of $V_{ds,\ max}$ is 6.4 V.

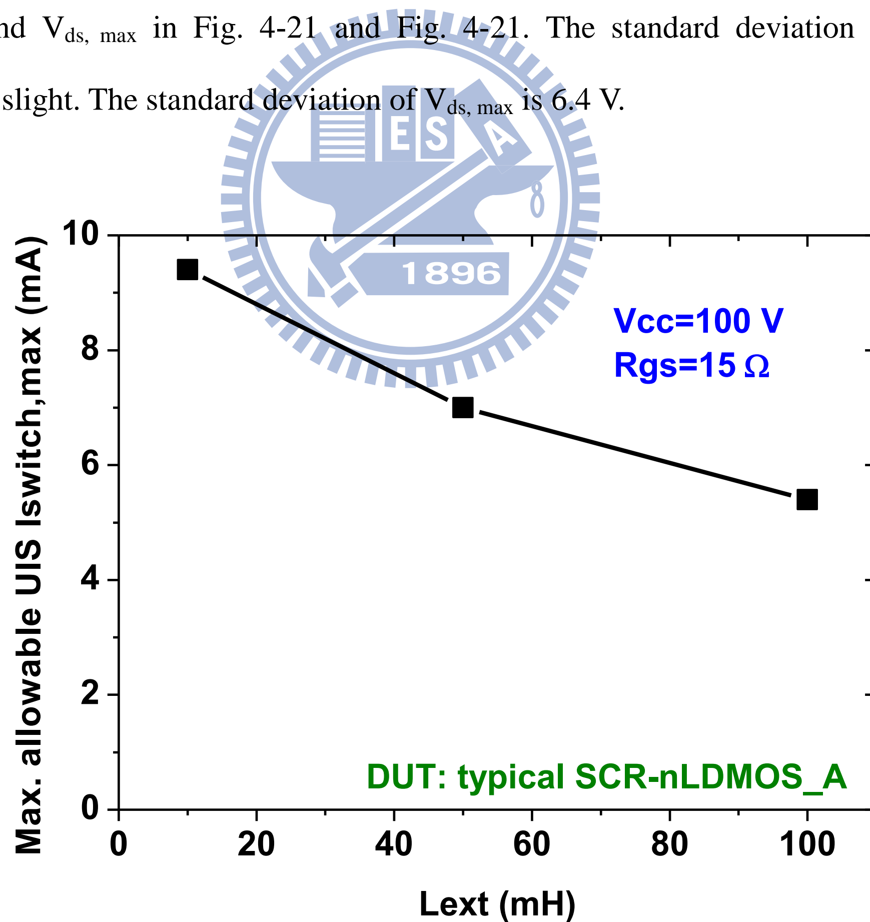

Fig. 4-17. The maximum allowable UIS $I_{switch,max}$ with different inductive impedance (L_{ext}).

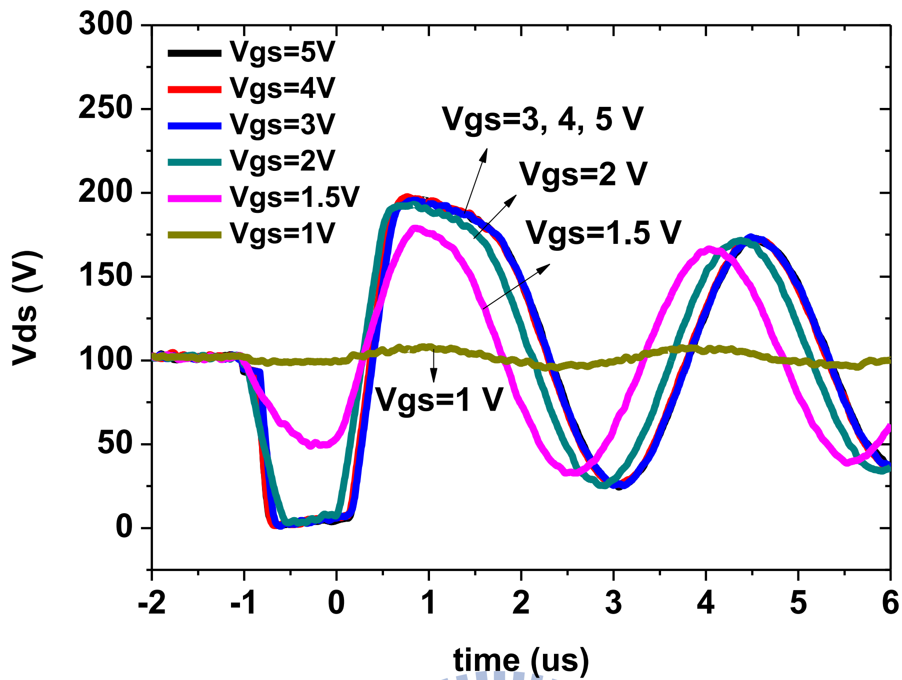

Fig. 4-18. The waveform of drain voltage (V_{ds}) with different gate bias (V_{gs}) during UIS stress.

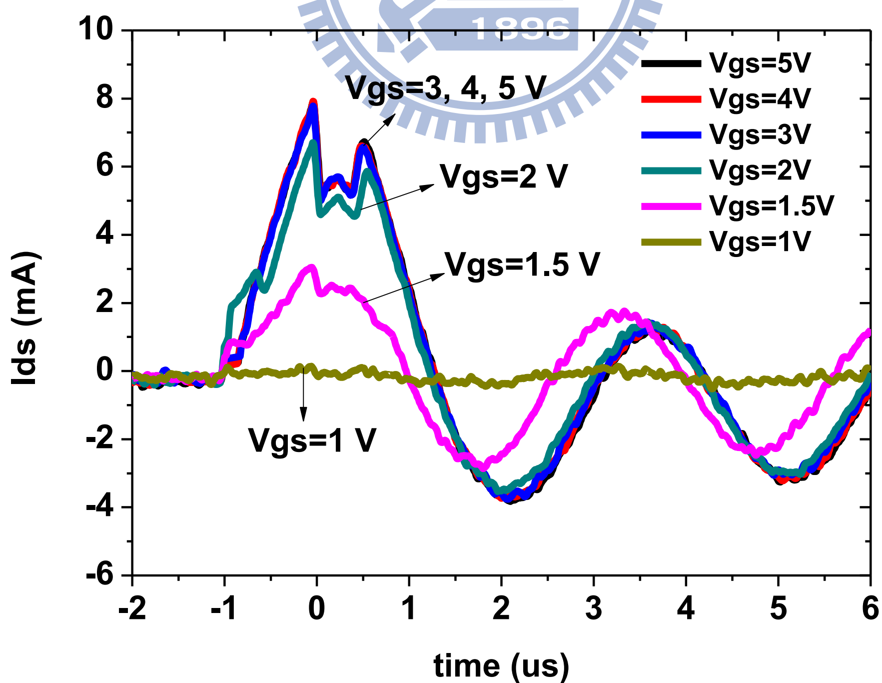

Fig. 4-19. The waveform of drain current (I_{ds}) with different gate bias (V_{gs}) during UIS stress.

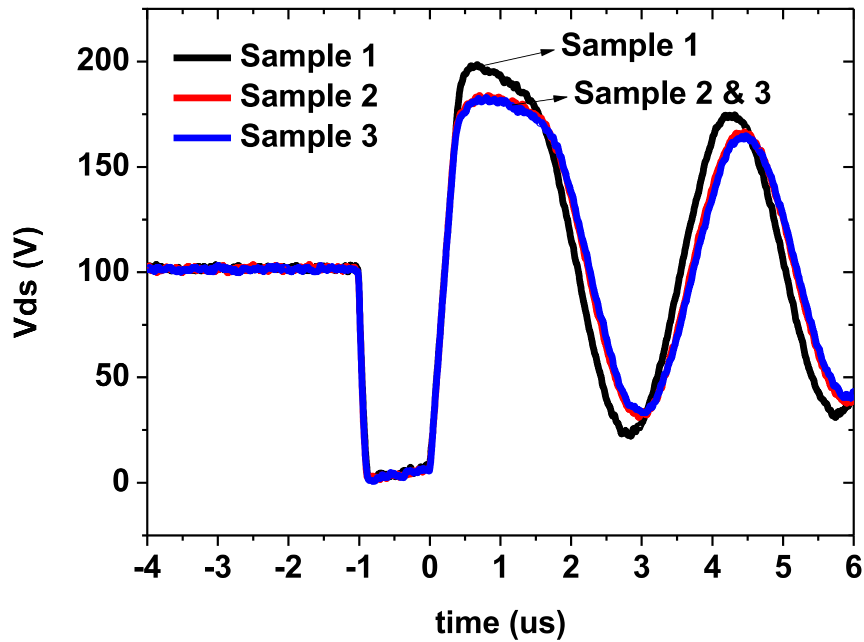

Fig. 4-20. The waveform of drain voltage (V_{ds}) with different samples whose device structure and layout parameters are the same during UIS stress.

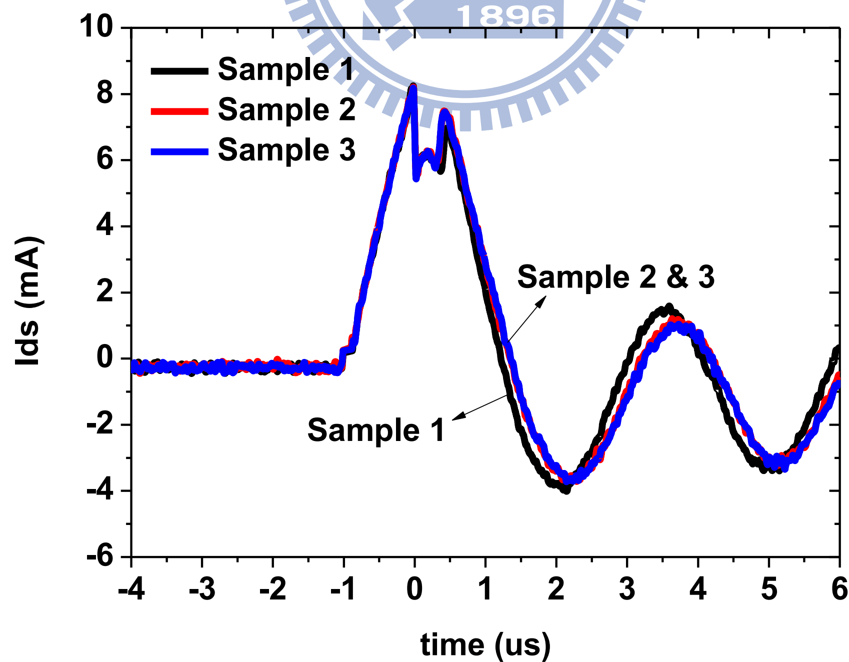

Fig. 4-21. The waveform of drain current (I_{ds}) with different samples whose device structure and layout parameters are the same during UIS stress.

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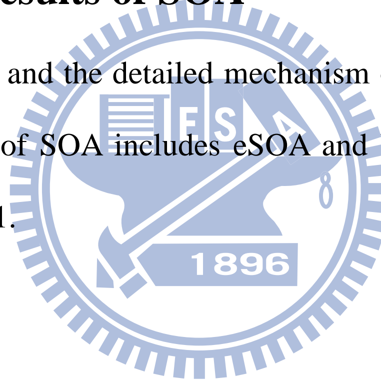
TABLE 4.1

The UIS tests with different sample

	UIS $I_{switch,max}$ (mA)	$V_{ds,max}$ (V)
Sample 1	8.8	204
Sample 2	8.8	192
Sample 3	8.6	194
Average	8.7	197
Standard deviation	0.1	6.4

4.2 Experimental Results of SOA



The measured method and the detailed mechanism of SOA are discussed in 4.1. The following experiment of SOA includes eSOA and UIS with typical n-type HV DMOS as listed in Table 2.1.

4.2.1 electrical SOA

Fig. 4-22 shows the boundary of 100-ns eSOA with different device structures. The drain current is normalized to the channel width; hence, the comparison is reasonable. The 100-ns eSOA of nLDMOS is the greatest; on the contrary, the 100-ns eSOA of circular_nLDMOS is the worst. It is due to the crowded heat effect. The device area of circular_nLDMOS is the smallest; as a result, the heat is hard to be dispersed for circular_nLDMOS. The triggering of embedded SCR is failed for SCR-nLDMOS_B, so the eSOA of SCR-nLDMOS_B is similar with that of nLDMOS. In addition, the serious degradation of eSOA is observed in Fig. 4-22 for SCR-nLDMOS_A. In other words, the insertion of SCR effectively improves ESD robustness while worsening the eSOA performance.

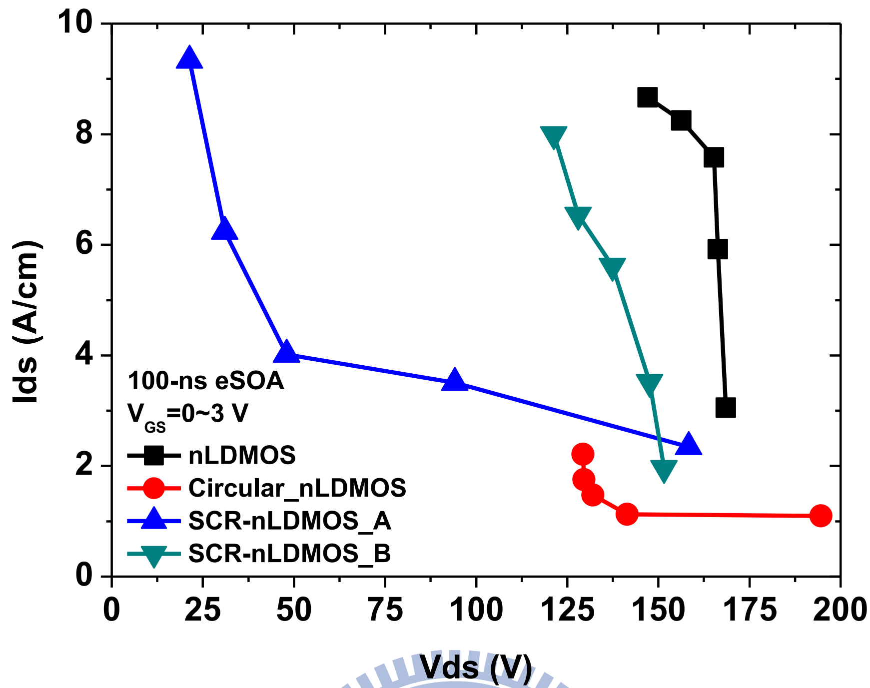


Fig. 4-22. The 100-ns eSOA with different device structure.

4.2.2 Unclamped Inductive Switch

Fig. 4-23 demonstrates the UIS waveform with different device structure. The waveform shows the maximum energy that the DUT can withstand. In other words, the DUT is suffered from the permanent damage with longer pulse width (T_p) under the condition of V_{cc} = 100 V, L_{ext} = 10 mH, R_{gs} = 15 Ω. Table 4.2 lists the maximum allowable UIS $I_{switch,max}$ and the trigger current which is measured by the 100-ns TLP system. The maximum allowable UIS $I_{switch,max}$ is slightly smaller than the trigger current. If the $I_{switch,max}$ is larger than the I_{t1}, the unstable state is over the boundary of eSOA as illustrated in Fig. 4-9 (b) and results in catastrophic damage. In consequence, the I_{t1} is critical parameter for performance of UIS. Circular_nLDMOS exhibits the greatest UIS level; on the contrary, the ability to withstand the UIS stress is the worst for SCR-nLDMOS_B.

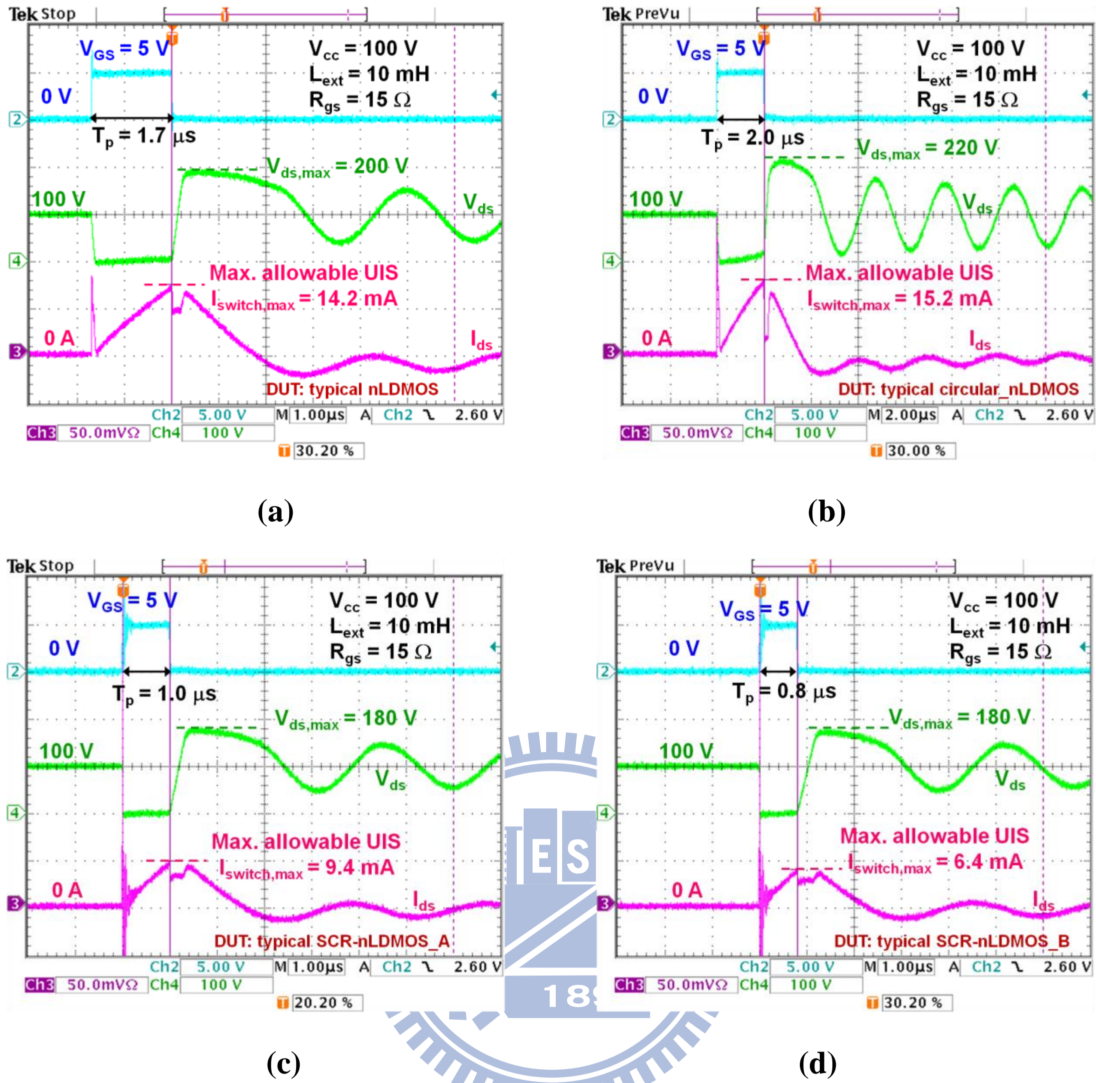


Fig. 4-23. The UIS waveform of typical (a) nLDMOS, (b) circular_nLDMOS, (c) SCR-nLDMOS_A, and (d) SCR-nLDMOS_B.

TABLE 4.2

The comparison between I_{t1} and max. allowable UIS $I_{switch,max}$

Device structure	I_{t1} (mA)	Max. allowable UIS $I_{switch,max}$ (mA)
nLDMOS	14.9	14.2
Circular_nLDMOS	16.5	15.2
SCR-nLDMOS_A	10.1	9.4
SCR-nLDMOS_B	7.9	6.4

Chapter 5

Discussion

5.1 The Trade-off Between ESD and SOA

Among the various reliability specifications, ESD and SOA are important issues for HV transistors. Table 5.1 lists the performance of ESD, eSOA, and UIS for typical n-type HV DMOS. It shows that the embedded SCR can efficiently improve ESD robustness for SCR-nLDMOS_A. Nevertheless, the severe eSOA degradation and the poor UIS level are observed. Hence, the insertion of SCR to HV DMOS is not a win-win solution for ESD and SOA. The methods to enlarge the boundary of eSOA and improve the ability of withstanding the UIS stress without paying for the poor ESD robustness are discussed in 5.2.

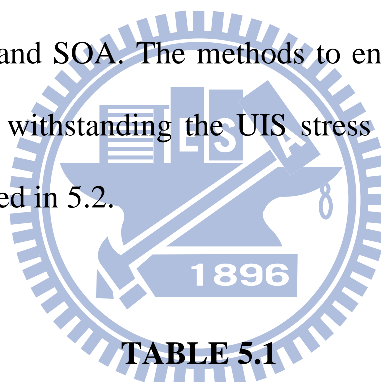


TABLE 5.1

The performance of ESD, eSOA, and UIS for n-type typical DMOS

Type / Ranking	ESD	eSOA	UIS
1st place	SCR-nLDMOS_A	nLDMOS	Circular_nLDMOS
2nd place	Circular_nLDMOS	SCR-nLDMOS_B	nLDMOS
3rd place	nLDMOS	SCR-nLDMOS_A	SCR-nLDMOS_A
4th place	SCR-nLDMOS_B	Circular_nLDMOS	SCR-nLDMOS_B

5.2 Methods to Improve SOA

The trade-off between ESD and SOA is observed in traditional HV DMOS and the HV DMOS with embedded SCR. There are three methods to overcome the dilemma. The methods of improving SOA without paying for the poor ESD level includes circuit solution [1], process solution [2] [3], and layout solution [3] [4]. First of all, the circuit solution is the clamped inductive switch (CIS). It improves the ability to withstand the UIS stress. Secondly, an additional implantation is applied to alter the equivalent R_{BE} of parasitic BJT. The higher R_{BE} is, the higher trigger current is. As a result, the improvement of eSOA and UIS is achieved. In the end, a novel layout style is proposed in [3] to improve eSOA of nDMOS with embedded SCR which exhibits excellent ESD robustness.

5.2.1 Circuit Solution to improve UIS [1]

The DUT is forced to conduct the inductive current when it is off during the UIS stress. The diode is added to bypass the I_{switch} when DUT is off, as illustrated in Fig. 5-1. The drain current is clamped to 0 A, so the circuit is named as clamped inductive switch (CIS). Fig. 5-2 shows the diagram of waveform during the UIS stress. The avalanche breakdown voltage of diode is named as BV_Z. The BV_Z is larger than V_{CC}; hence, the diode is off and the waveform of UIS is identical to that of CIS until t_2. The voltage pulse of gate (V_{GS}) is removed and the DUT is off at t_2. The diode bypasses the I_{switch}; therefore, the drain current is clamped to 0 A and the drain voltage is immediately clamped V_{cc} at t_2. Fig. 5-3 shows the waveform of UIS and CIS. The SCR-nLDMOS_A exhibits poor UIS level. However, the dramatically improvement is observed in waveform of CIS. The maximum allowable $I_{swtich,max}$ of CIS is almost three times larger than that of UIS.

The CIS tests with different number of diode are done for the purpose of further knowing the influence of diode on the ability to withstand the CIS stress. Fig. 5-4 shows the test circuit of UIS with different number of diode. The corresponding waveform of drain current is identical to each other, as illustrated in Fig. 5-5. It clarify that the number of diode is ineffectual to improve the CIS level.

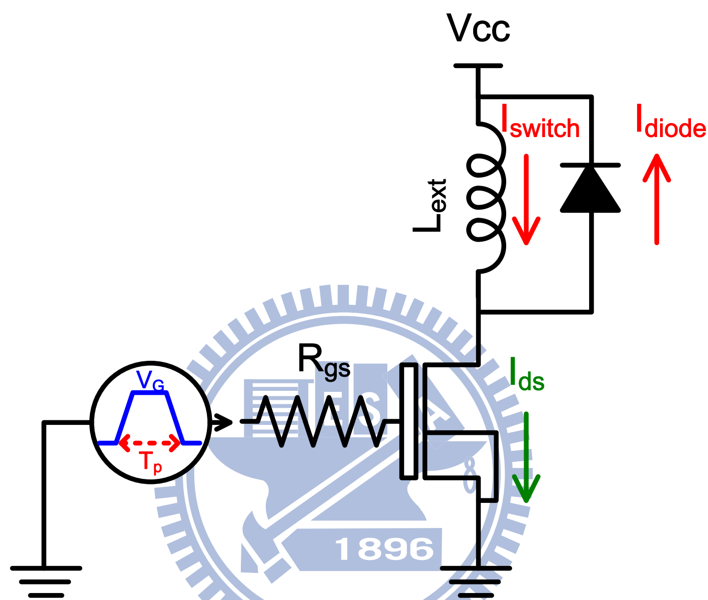


Fig. 5-1. The test circuit of clamped inductive switch [1].

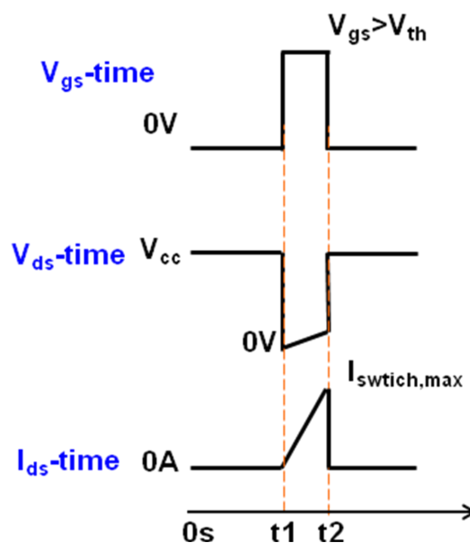
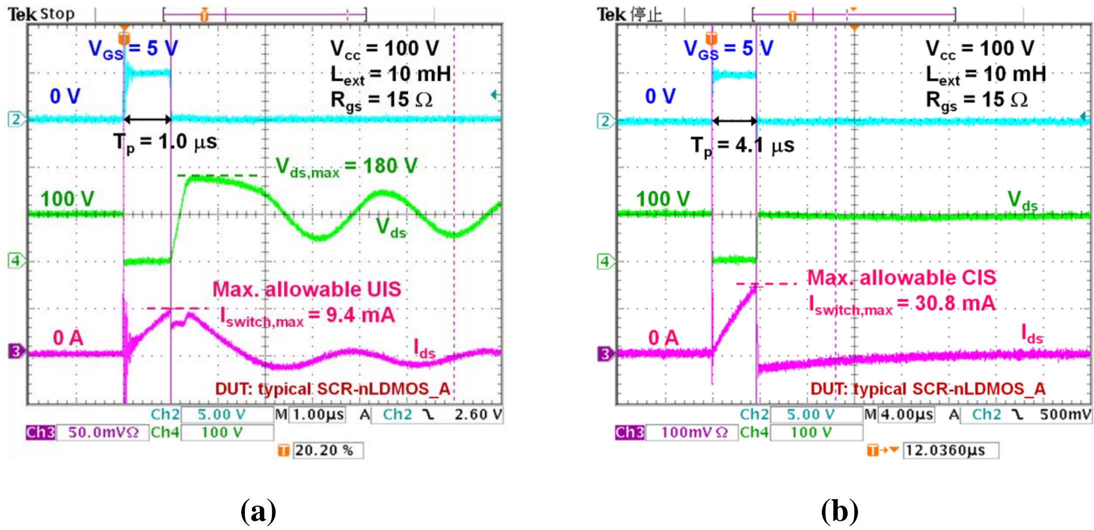


Fig. 5-2. The diagram of waveform during the CIS stress.



(a) (b)

Fig. 5-3. The waveform of (a) UIS and (b) CIS.

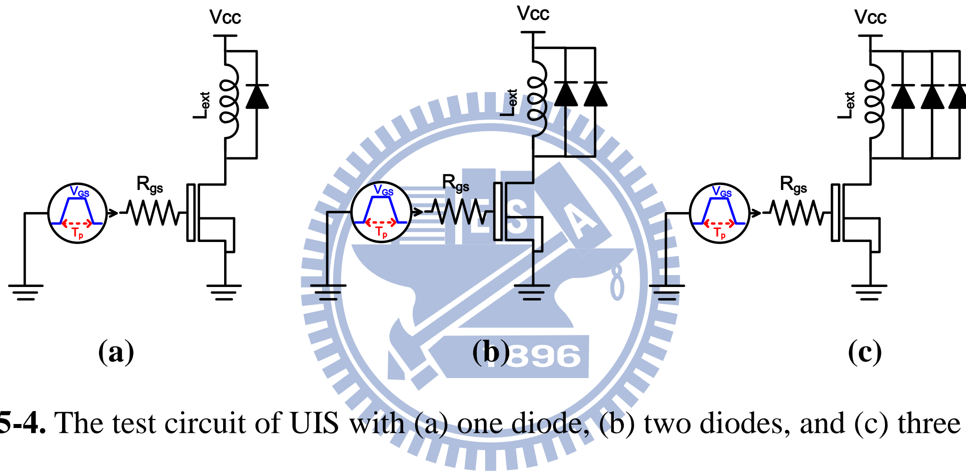


Fig. 5-4. The test circuit of UIS with (a) one diode, (b) two diodes, and (c) three diodes.

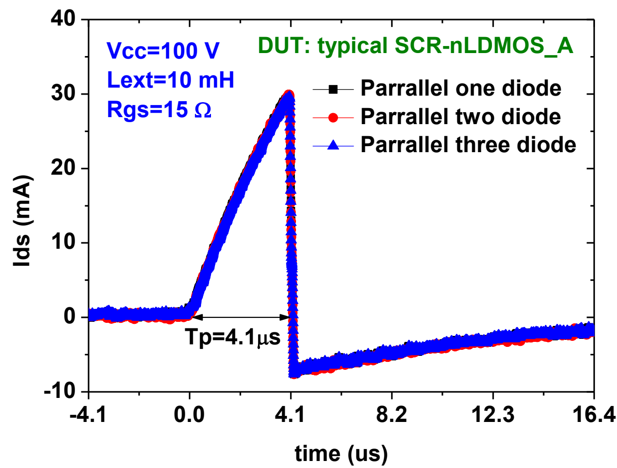


Fig. 5-5. The waveform of drain current with different number of diode during the CIS stress.

5.2.2 Process Solution to improve eSOA [2] [3]

Fig. 5-6 shows the cross-sectional view of nLDMOS with buried body which is arranged beneath the n+ source region. The current path of parasitic BJT is shown in blue line with arrow. The equivalent resistance of parasitic BJT between base and emitter (R_{BE}) is equal to the resistance of p-type region. The doping concentration of buried body is larger than that of p body; hence, the R_{BE} is reduced as a result of buried body. In addition, the V_{BE} has to larger than $V_{BE,ON}$ (usually equal to 0.7 V) to turn on parasitic BJT. The lower R_{BE} is, the higher trigger current is. In other words, the triggering of parasitic BJT is harder and the boundary of eSOA is widened. Fig. 5-7 shows the experimental results of eSOA with and without buried body. The data demonstrates that the buried body can improve eSOA. The buried body can theoretically enhance the ability to withstand the UIS stress due to the increased trigger current.

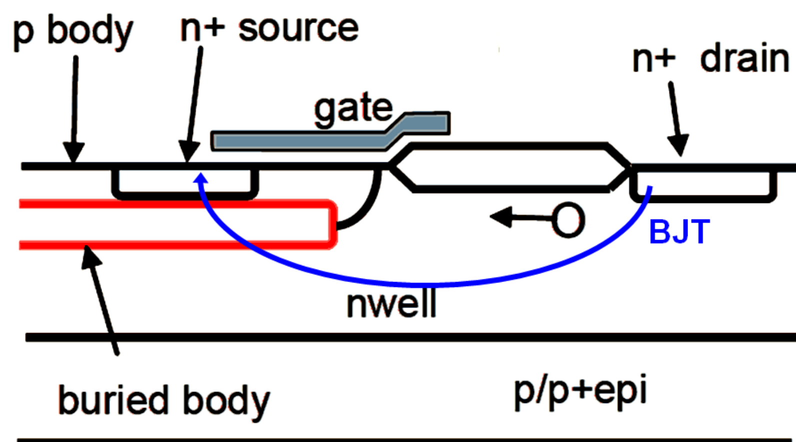


Fig. 5-6. The cross-sectional view of nLDMOS with buried body which is shown in red rectangle [2].

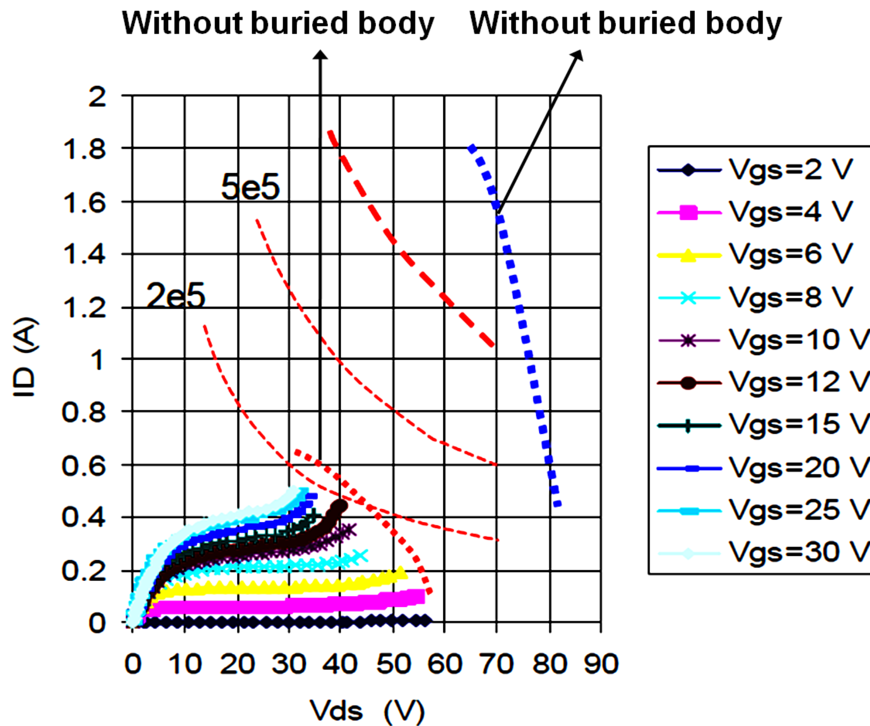
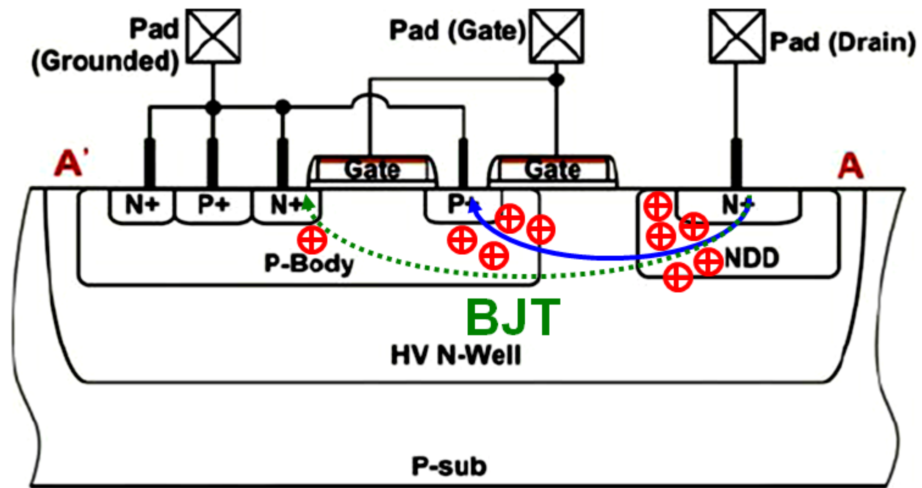


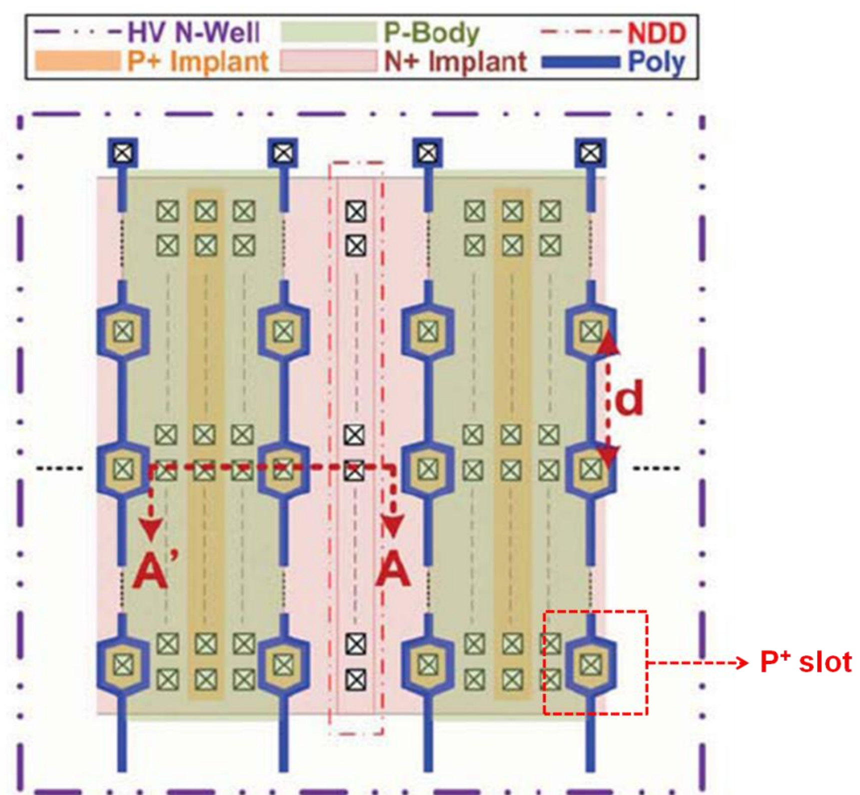
Fig. 5-7. The 100-ns eSOA with and without buried body [2].

5.2.3 Layout Solution to improve eSOA [3] [4]

Fig. 5-8 shows the novel layout style of nLDMOS. The polygate is bent according to the shape of hexagon, so the layout style is named as polybending. The void inside the hexagon is filled with P^+, and it is named as P^+ slots. The P^+ slots are short to ground pad through the internal metal. The avalanche current path is from drain to source region. The P^+ slots can shunt the avalanche-generated holes to ground during the TLP stress as illustrated in Fig. 5-8 (a). Hence, it needs more avalanche-generated holes to trigger the parasitic BJT. In other words, the trigger current is increased. As the polygate arrangement is applied to the nLDMOS with embedded SCR, the ESD robustness and the boundary of eSOA will simultaneously improved. It is a win-win solution for the reliability issues of ESD and SOA.



(a)



(b)

Fig. 5-8. (a) The cross-sectional view along A-A' line and (b) the layout top view of the nLDMOS with the polybending layout arrangement [3].

Chapter 6

Conclusions and Future Work

6.1 Conclusions

The new proposed structures for HV LDMOS in a 0.5-μm 100-V BCD SOI technology have been presented. Measurements include the I_{DS}-V_{DS} characteristics and avalanche breakdown voltage are measured by curve tracer; trigger voltage, trigger current, failed current, and 100-ns eSOA are measured by the 100-ns TLP; HBM and MM levels are measured by ESD simulator with model ets910. The experimental results show that the insertion of SCR increases ESD performances of HV LDMOS but degrades eSOA and the capability of withstanding the UIS stress.

To minimize the junction curvature effect as mentioned in chapter 2, the layout styles of HV LDMOS are in circular and elliptic shape. Furthermore, the experimental data illustrates that the avalanche breakdown voltage increases with increasing radius of metallurgical junction.

The insertion of SCR to LDMOS is not always effective in improving the ESD robustness. The ESD robustness of SCR-LDMOS_B in which the equivalent SCR path is located at center of drain region is poor; on the contrary, the ESD robustness of SCR-LDMOS_A in which the equivalent SCR path is located at side of drain region is excellent. Consequently, the arrangement of placing embedded SCR significantly affects the ability to withstand the ESD stress.

The influence of various layout parameters on ESD robustness has been presented. For nLDMOS, I_{t2} per unit width (W) gradually diminishes with increasing W as a result of non-uniform turn-on effect.

The contact spike occurs at drain both for nLDMOS and pLDMOS; hence, the parameter Y at drain is critical to the ESD performance. The cross-sectional area of ESD current is enlarged by increasing Y; hence, it needs much more ESD current to cause contact spike at drain. As a result, the contact-spike-induced junction leakage occurs at higher ESD current when Y is increased. Consequently, I_{t2} is proportional to Y both for nLDMOS and pLDMOS.

For SCR-nLDMOS_A, the main ESD current path is SCR path and the contact spike occurs at drain P^+ region. It needs much more ESD current to cause contact spike at drain when the cross-sectional area of ESD current is enlarged by increasing Y; hence, I_{t2} increases with increasing Y. Furthermore, we take the ESD current path of SCR and $BJT_{,NPN}$ into account to investigate the influence of spacing between N+ and P+ at drain region (T_d) on ESD robustness. The ESD current prone to flow through SCR path due to the higher R which arose from wider T_d. The SCR exhibits excellent ESD performance while the BJT exhibit poor ESD robustness. Consequently, I_{t2} is proportional to T_d due to the increment of SCR ESD current and the reduction of BJT ESD current. The parameter T_s doesn't affect the parasitic current path and resistor, so T_s is ineffectual in improving ESD robustness of SCR-nLDMOS_A.

For SCR-pLDMOS_A, the main parasitic ESD current path is SCR and $BJT_{,NPN}$. Similarly, the ESD current prone to flow through SCR path due to the higher R which arose from wider T_s. As a result, I_{t2} is proportional to T_s due to the increment of SCR ESD current and the reduction of BJT ESD current. The parameter T_d doesn't affect the parasitic current path and resistor, so T_d is ineffectual in improving ESD robustness of SCR-pLDMOS_A.

The I_{t2} is approximately equal to I_{t1} for LDMOS without embedded SCR; as a result, I_{t2} increases with increasing D. Moreover, some ineffectual layout parameters listed in Table 3.5 has no influence on ESD level. Hence, it is suggested that this

parameters are ineffective in improving the ESD robustness.

Though LDMOS with embedded SCR exhibits excellent ESD robustness, it suffers from a severe degradation of electrical SOA and a poor ability to withstand the unclamped inductive switch (UIS) stress. There are three feasible ways to improve SOA without paying for the poor ESD robustness.

(1) Clamped inductive switch [1]

The DUT is forced to conduct the inductive current (I_{switch}) when it is off during the UIS stress. The V_{DS} and I_{DS} are simultaneously high; hence, a destructive energy E_{AS} causes catastrophic damage in DUT. To bypass the I_{switch}, UIS circuit is incorporated with a diode. Experimental result shows that it can improve the maximum allowable $I_{swtich,max}$ by three times.

(2) Doping concentration under the source region is light [2] [3]

The doping concentration of the additional implantation (buried body) is higher than original doping concentration; hence, the R_{BE} is reduced. With buried body, it needs higher trigger current to turn on the parasitic BJT. In other words, the action of snapback is harder, so it successfully widens the eSOA of LDMOS.

(3) Novel layout arrangement: polybending [3] [4]

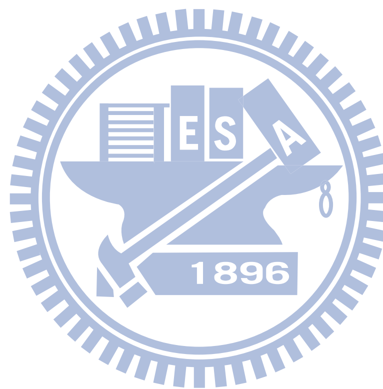
The polygate is bent to insert P^+ slots. Such layout style is named as polybending. The P^+ slots can shunt the avalanche-generated holes to ground during the TLP stress; hence, it needs more avalanche-generated holes to trigger the parasitic BJT. In other words, the trigger current is increased. Consequently, an improvement of eSOA can be achieved by polybending.

Therefore, the suppression of triggering parasitic BJT or SCR by increasing the trigger current is a win-win solution for ESD and SOA.

6.2 Future Work

The LDMOS is functional in circular and elliptic layout style. Hence, the deeper investigation on the LDMOS is feasible. For LDMOS in circular layout style, the multiple DMOS in waffle type and the insertion of SCR are worth to try. For LDMOS in elliptic layout style, the multiple finger layout arrangement is challenging.

It is discovered that a LDMOS has better ability to withstand the UIS stress when it has a higher trigger current. Engineering the trigger current of LDMOS accordingly can be a direction of future UIS studies.



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國立交通大學電子研究所碩士班　　(98 年 9 月~100 年 7 月)

研究所修習課程：

積體電路之靜電放電防護設計特論	柯明道教授
半導體物理及元件（一）	汪大暉教授
積體電路技術（一）	張國明教授
積體電路技術（二）	林鴻志教授
固態物理	顏順通教授
數值半導體元件模式	李義明教授
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