# 國立交通大學

## 電子工程學系電子研究所碩士班

## 碩士論文

# 在鍺通道金氧半場效電晶體上去釘札後蕭特基二極體以及 n$^+$/p 二極體的研究

# Investigation of the Depinning Schottky Junction and n$^+$/p Junction on Ge-Channel MOSFETs

研 究 生：陳韋志

指導教授：簡昭欣　教授

中華民國一零一年八月

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研究生：陳韋志　　Student：Wei-Chih Chen

指導教授：簡昭欣　　Advisor：Chao-Hsin Chien

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學生：陳韋志　　　　　　指導教授：簡昭欣 教授

國立交通大學電子

工程學系電子研究所碩士班

## 摘要

此論文中，首先我們分析金屬/絕緣體/鍺二極體的接面特性，並且成功的利用二氧化鍺以及三氧化二鋁來緩解了費米能階釘札(Fermi-level pinning)的現象，並在 p 型鍺基板上達到相當高的電洞蕭特基能障(Schottky barrier for hole)。經過計算，在使用二氧化鍺的情況下,釘札係數(pinning factor)在 p 型與 n 型鍺基板上各是 0.41 和 0.59。而在使用三氧化二鋁的情況下, 釘札係數在 p 型與 n 型鍺基板上各是 0.347 和 0.495。其中,使用二氧化鍺當作去釘札層(depinning layer)會有比使用三氧化二鋁還要來的好的去釘札(depinning)效果；這是因為二氧化鍺與鍺的接面品質比三氧化二鋁的要來的高。再來，我們透過不同金屬的使用，發現了在金屬/n 型鍺接面中加入一層二氧化鈦，可以使得原本的整流特性轉變成了歐米特性，而這原因是由於二氧化鈦有 n 型半導體的特性。

根據去釘札的蕭特基二極體的經驗，我們成功的利用二氧化鍺以及二氧化鈦來製作出金屬源汲極(metal S/D)的純鍺 n 型場效電晶體。在比較下，由於二氧化鈦與鍺之間有較低的導帶能帶差(conduction band offset)，以至於在小的汲集電壓下，利用二氧化鈦所製作的電晶體會比用二氧化鍺的有較好的電流特性。利用我們的實驗結果分析在傳統鍺

n 型場效電晶體中使用二氧化鈦接面層的優缺點。透過在 n$^+$鍺與金屬間加入一層二氧化鈦可以有效降低蕭特基能障，然而這層二氧化鈦也帶來了額外的電阻效應。而且隨元件尺寸的微縮，這額外的電阻效應將會更加嚴重。

最後，我們研究在不同離子佈植的劑量與不同的退火溫度下的鍺 n$^+$/p 接面特性。總結來說，透過使用適當的離子佈植劑量($2 \times 10^{14}\mathrm{cm}^{-2}$)可以讓我們得到淺的接面深度也可以減低來自於劑量增加所帶來額外的擴散(concentration- enhanced diffusion)。而根據我們在鍺 n$^+$/p 接面的經驗，我們成功製作出通道長度 500 奈米的鍺 n 型場效電晶體。並且其有著良好源極電流開關比($1.67 \times 10^5$)以及很低的次臨界擺幅並且沒有明顯的汲極引致能障降低效應。

# Investigation of the depinning Schottky Junction and $n^+$/p Junction on Ge-Channel MOSFETs

**Student：Wei-Chih Chen** **Advisors：Dr. Chao-Hsin Chien**

**Department of Electronic Engineering & Institute of Electronics**
**National Chiao Tung University**

## *ABSTRACT*

In this thesis, firstly, metal/insulator/Ge (MIS) junctions were fabricated and analyzed electrically. We successfully release the FLP both on n and p type Ge by inserting the interfacial layer of $GeO_2$ and $Al_2O_3$, and make the high SHB for hole in p-Ge case. The pinning factor of $GeO_2$ case is 0.41 for p-Ge and 0.59 for n-Ge, while in $Al_2O_3$ case the pinning factor is 0.347 for p-Ge and 0.495 for n-Ge. The effect of de-pinning by using $GeO_2$ is better than one by using $Al_2O_3$, which resulting from the better quality of $GeO_2$/Ge interface. By applying $TiO_2$ as the interfacial layer to different metal contacts, we find that the reason of I-V characteristic changing from rectifying to ohmic by the insertion of $TiO_2$ layer is due to the n type semiconductor-like characteristics of $TiO_{2.}$

Secondly, basing on the experiences in the de-pinned junctions, we successively demonstrate the device characteristics of the metal S/D Ge n-MOSFETs with $GeO_2$ and $TiO_2$ as depinning layer. Compared to $GeO_2$, the smaller conduction band offset of $TiO_2$ lead to the better drain current characteristic at low drain voltages. Furthermore, pros and cons of adding the $TiO_2$ interfacial layer to the conventional Ge n-MOSFETs have been discussed according

to our experimental data. The insertion of $TiO_2$ layer at metal/n-Ge interface cannot only reduce the Schottky barrier height but also induce an additional resistance. As the channel length scaling down, the effect of additional resistance will be more serious.

Finally, we investigate the characteristics of Ge $n^+$/p junction with different implantation dosages and activation temperatures. It is concluded that medium implantation dosage ($2 \times 10^{14} \mathrm{cm}^{-2}$) enables us to obtain the shallow junction and suppress the effect of concentration-enhanced diffusion. According to the experiences in $n^+$/p junctions, the 500nm Gate-length n-MOSFET was achieved with high $I_{on}/I_{off}$ ration ($1.67 \times 10^5$ for $I_S$), low S.S, and no obvious DIBL.

# 誌謝

總算，我的碩士生涯要告一段落了，這幾年來的努力總算結成了果實。記得剛推甄上研究所的時候，還是懵懵懂懂的不知道方向。如今，經過這幾年在實驗室的教授以及學長同學們的幫助下，總算讓我有了這點成果。

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# Chapter 1

# Introduction

## 1.1 General Background

Ge was the predominant material as the pioneer for semiconductor industry through the 1950s and early 1960s. In 1947, the first transistors were invented using germanium in Bell Laboratories by Brattain, Bardeen and Shockley. About a dozen years later, the first integrated circuits developed in 1958 by Kilby also was made of germanium. However, since the 1st MOSFET fabricated in 1960 by Kahng and Atalla was made of Si, Ge was largely replaced with silicon. Compared with the water-soluble and thermal instable $GeO_2$, the thermal $SiO_2$ as a gate dielectric for silicon showed excellent properties. Therefore, Si-based MOSFETs have become the driving force for the semiconductor industry in the last four to five decades. Based on the Moore's law [1], the physical dimensions have been continually reduced to double the number of transistors on a chip every eighteen months, although architecture and working principle of MOSFET have remained the same. However, the conventional device dimension scaling cannot continue forever.

The scaling roadmap in the process of Si MOSFETs was demonstrated by R. Chau, Intel Corporaion, as shown in **Fig. 1.1.** As device scalding down to the nanoscale regime, hybrid orientation and strain engineering were introduced to increase performance [2]. But these methods may not be sufficient to continue Moore's law. Replacing Si with high mobility material is another way to boost performance. In addition, great progression in the deposition of high-k material demonstrates that the gate dielectrics are no longer restricted to the thermal oxide [3]. Therefore, there is a resurgence of interest in Ge due to its higher electron and hole mobility compared to Si.

## 1.2 Motivation

In **Table 1.1,** the material properties of bulk Si, Ge, GaAs, and InAs at 300K are compared [4]. There are many advantages of Ge: (1) 2×higher electron and 4× higher hole mobility than Si. (2) The lower band gap (0.66eV) enables to lower the Schottky barrier height so that the contact resistance could be lower than one of Si. (3) Low melting point by which process temperature could be decreased.

In recent years, Ge p-MOSFET with mobility 3X higher than Si universal curve has been reported [5], but the Ge n-MOSFET still exhibits the inferior performance. Because n-type dopant in Ge shows low solid solubility and fast diffusion rate so that low contact resistance and shallow junction were hard to be achieved. Hence, the metal S/D seems to be one of the solutions, because the low resistance of metal and the abrupt junction formed at the interface of metal and semiconductor.

Therefore, Ge $n^+$/p junction and Schottky junction are worthy to study.

## 1.3 Scope and Organization of the Thesis

The promising high-mobility substrate material, Ge, was investigated in this thesis. In this thesis, we focus on the research of Schottky junction and $n^+$/p junction for metal S/D MOSFET and high performance n-MOSFET. The thesis is divided into five chapters and arranged as follows:

**Chapter 1**, a brief overview of background and motivation is described.

**Chapter 2**, Ge Schottky junctions with n-and p-type substrate were fabricated, and the basic characteristics of Fermi-Level Pinning (FLP) on Ge and the extraction of Schottky barrier height were studied. In order to mitigate the FLP, we inserted an interfacial layer with $Al_2O_3$, $GeO_2$, and $TiO_2$ at metal/Ge interface. The characteristics of each material as the interfacial layer were compared.

**Chapter 3**, Ge metal S/D p- and n- MOSFETs were fabricated. The different current behavior between $GeO_2$ and $TiO_2$ as depinning layer on n-MOSFETs was discussed. Conventional Ge n-MOSFETs with and without $TiO_2$ layer at the interface of metal/$n^+$-Ge contact on S/D region were fabricated, and the effects of $TiO_2$ layer were studied.

**Chapter 4**, Ge $n^+$/p junctions were fabricated, and the effects of implant dose and activation temperature on junction were discussed. With the $n^+$/p junction formed by medium dosage of phosphorous, high performance 500nm-gate length Ge n-MOSFET was achieved.

**Chapter 5**, we summarize the experimental results and give the conclusions in the thesis.

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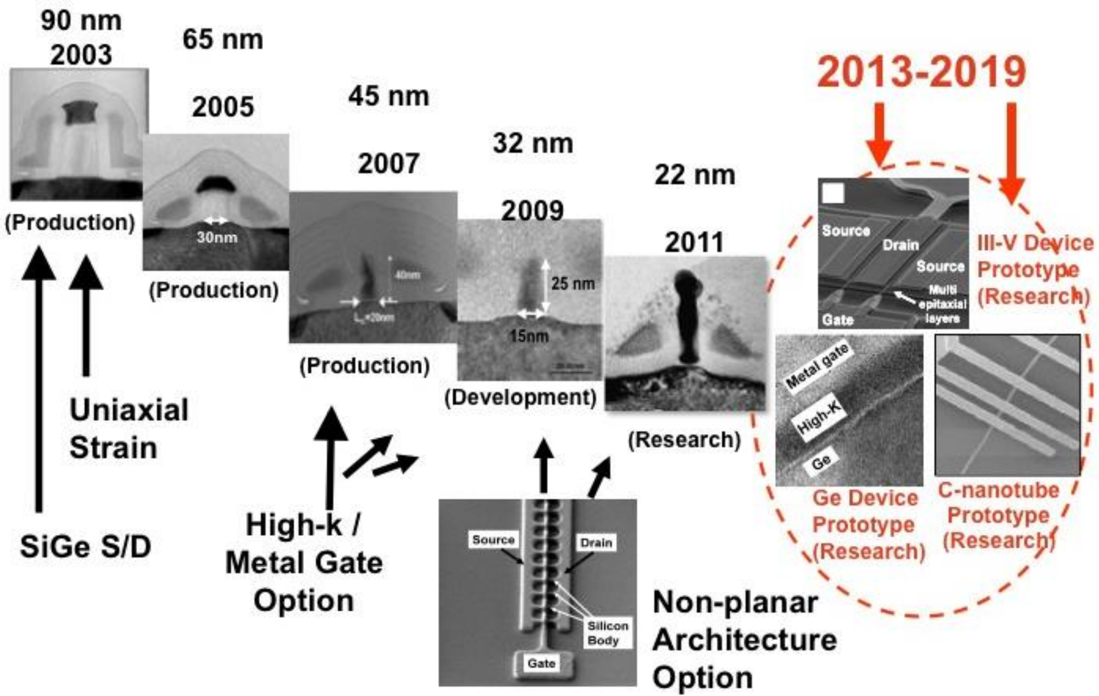

Fig. 1.1 Sub 100nm transistor technology scaling (source: R. Chau, Intel Corp.)

| | Ge | Si | GaAs | InAs |
|---|---|---|---|---|
| Bandgap (eV) | 0.66 | 1.12 | 1.42 | 0.35 |
| Hole mobility(cm$^2$/V-S) | 1900 | 450 | 400 | 460 |
| Electron mobility(cm$^2$/V-S) | 3900 | 1500 | 8500 | 33000 |
| Conduction band DOS Nc (cm$^{-3}$) | 1.04E19 | 2.8E19 | 4.7E17 | 8.7E16 |
| Valance band DOS Nv (cm$^{-3}$) | 6E18 | 1.04E19 | 7E18 | 6.6E18 |
| Lattice constant(Å) | 5.646 | 5.431 | 5.653 | 6.058 |
| Dielectric constant | 16 | 11.9 | 13.1 | 15.2 |
| Melting point(℃) | 937 | 1412 | 1240 | 942 |
| Dopant activation limit (cm$^{-3}$) | P: (4-6)E19 | P: (1-2)E20 | P: (4-6)E18 | P: (1-3)E18 |

**Table 1.1** Material properties of bulk Ge, Si, GaAs, and InAs at 300K are compared.

# Chapter 2

# De-pinning of Germanium Schottky Diode by Inserting an Interfacial Layer

## 2.1 Introduction

Unfortunately, the Ge $n^+/p$ junction has serious problems because n-type dopants in Ge show low solid solubility and faster diffusion rate, so that high S/D resistance and hard execution of shallow junction are the problems in the future. [1] The metal S/D seems to be one of the solutions, because the low resistance of metal and the abrupt junction formed at the interface of metal and semiconductor. [2] Thus, the control of Schottky barrier height at the metal/Ge interface is necessary to achieve high performance Ge CMOS. But Ge has the characteristics of Fermi-level pinning (FLP), which makes the Schottky barrier height of Schottky contact can't be controlled by changing the metal work function. [3]

Although the mechanism of FLP on Ge still can't be fully explained, the density of states at the metal/Ge interface determines how serious the pinning is. [4-6] Many groups assume that the main reason of the pinning is due to the metal-induced-gap-states (MIGS), which are the energy states at the interface between metal and semiconductor owing to the penetration of electron wave function from metal to semiconductor. [7-9]Base on this assumption, inserting an interfacial layer can reduce the penetration of wave function, as seen in **Fig. 2.1**. [8-11]

In this chapter, the basic characteristics of FLP on Ge and the extraction of Schottky barrier height are shown first. Next, the effects of de-pinning by different interfacial layer which include $Al_2O_3$, $GeO_2$, and $TiO_2$ are shown. Finally, we discuss the different behavior of $TiO_2$ as the depinning layer.

## 2.2 Characteristic of FLP of germanium

### 2.2.1 Fabrication of metal/Ge Schottky diode

(100)-oriented P-Ge substrate and N-Ge substrate with doping concentration 2E15cm$^{-3}$ (resistivity ca. 2Ω · cm) and 1.5E14cm$^{-3}$(resistivity ca. 10Ω · cm) were used for Schottky diode fabrication. Before metal contact formation, all of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide. On the clean Ge surface, three different metal were deposited as the front electrodes patterned through shadow mask. These metals included Al, Cr and Au with the higher to lower work function respectively, which were deposited by thermal coater (Al-4000Å) and E-gun (Cr-1500 Å, Au-500 Å). Then, a thermal coater 4000 Å Al layer was deposited as the backside contact.

The process flow and device structure are shown in **Fig. 2.2**

### 2.2.2 Ideal factor and Schottky barrier height measurement

The band diagram of a Schottky barrier diode on an n-type substrate is shown in **Fig2.3.** The Schottky barrier height and metal work function are $\emptyset_B$ and $\emptyset_m$ respectively.$\chi$ is the electron affinity and $\emptyset_{bi}$ is the build in potential. In thermionic emission model, the current and voltage relationship of a Schottky barrier diode is given by eq. (2.1).

$$I=AA^*T^2\exp\left(-\frac{e\emptyset_B}{k_BT}\right)\exp\left(\frac{eV}{nk_BT}\right)\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right] \qquad (2.1)$$

Where A is the junction area and $A^*$ is Richardson constant.

Eq. (2.1) can also be expressed as eq. (2.2).

$$\ln\left(\frac{J}{\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right]}\right)=\ln\left[A^*T^2\exp\left(-\frac{e\emptyset_B}{k_BT}\right)\right]+\frac{eV}{nk_BT} \qquad (2.2)$$

A plot of $\ln\left(\frac{J}{\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right]}\right)$ versus voltage can define the ideal factor n by its slope as seen in **Fig2.4**. And then change eq. (2.2) into the form of eq. (2.3)

$$\ln\left(\frac{J}{\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right]T^2}\right) = \ln(A^*) - \frac{e\left(\emptyset_B - V/n\right)}{k_BT} \qquad (2.3)$$

We can make a plot of $\ln\left(\frac{J}{\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right]T^2}\right)$ versus $^1/_T$ through the measurement by changing temperature as seen in **Fig. 2.5**. This plot as seen in **Fig. 2.5,** sometimes will be called as Richardson plot, which has a slope of $\frac{e(\emptyset_B-V/n)}{k_BT}$.

A plot of the slope versus voltage can define the Schottky barrier height by its intercept on the vertical axis as seen in **Fig. 2.6**

### 2.2.3 IV characteristics of Ge Schottky diode

In ideal case, the Schottky barrier height $\emptyset_B$ as seen in **Fig. 2.3** can be defined by eq. (2.4)

$$\emptyset_B = \emptyset_m - \chi \qquad (2.4)$$

Based on eq. (2.4), Schottky barrier height can be controlled by changing metal work function; we can make $\emptyset_B$ lower by using the metal with lower work function or higher by using the metal with higher work function. In other words, we can make the diode with ohmic or Schottky behavior by using the appropriate metal.

But all of the metal/N-Ge samples show the rectifying behavior and the metal/P-Ge samples show the ohmic behavior, as seen in **Fig. 2.7**. In this situation, which is called Fermi-level pinning (FLP),$\emptyset_B$ can't be modulated because Fermi-level is pined at somewhere. In order to obtain more detail, we measured samples with different temperature. The measurement by changing temperature as we mentioned before, which can be used to extract the Schottky barrier height, but the precondition is that must be measured in appropriate temperature range. According to the ideal factor measured in the range of 298~323 K as seen in **Table2.1**, we think this range is appropriate to use. Because the ideal factor in this range are closed to 1 and show the temperature independent behavior.

In order to find out the location where FLP occurred and how serious it was, we can use eq. (2.5).

$$\emptyset_B = S(\emptyset_m - \emptyset_{CNL}) + (\emptyset_{CNL} - \chi_S) \qquad (2.5)$$

Where the pinning factor is defined by $S \equiv \partial\emptyset_B / \partial\emptyset_m$ and $\emptyset_{CNL}$is charge neutrality level. Therefore, we make the plot of barrier height versus metal work function, as seen in **Fig. 2.8.** From the eq. (2.5) we obtain $S \sim 0$ and $\emptyset_{CNL} = 0.01eV$ above valance band by assuming that $\chi_S = 4eV$ and Ge band gap is 0.66eV. The Fermi-level pinning is more serious as pinning factor is more close to zero. Because strong Fermi-level pinning around the charge neutrality level (only 0.01eV above valence band), all metals give high barrier height for electron and also low barrier height for hole. It agrees with the experiment we did.

## 2.3 Effect of inserting an interfacial layer for depinning

### 2.3.1 Fabrication of depinning experiment

We select three sorts of material as interfacial layer to release FLP by inserting this interfacial layer between metal and germanium. Those material include $Al_2O_3$ was deposited by ALD; $GeO_2$ was formed by rapid thermal oxidation; $TiO_2$ was deposited by ALD. The fabrication is base on the metal/Ge sample’s fabrication. The only one different thing is forming the interfacial layer before metal contact formation. At first, we found the best condition by changing the thickness of interfacial layer on the p-Ge sample. And then, we applied the best condition on N-Ge and P-Ge with different metal in order to find the pinning factor. Those metals were deposited by thermal coater (Al) or E-gun (Ti, Cr, Au, and Pt). Because the thickness was increased as we increased the counts of ALD cycle, we can roughly use the counts number represent the different thickness.

The process flow and device structure are shown in **Fig. 2.9.**

### 2.3.2 $Al_2O_3$

As the ALD cycle numbers of $Al_2O_3$ was increased to 8cycles, the barrier height for hole was increased (represents the decrease of barrier height for electron), as seen in **Fig. 2.10.** This is because the metal induced gap state (MIGS) was reduced by inserting the interfacial layer of $Al_2O_3$.As the thickness of $Al_2O_3$ was increased the more penetration of wave function from metal electrodes was blocked. Therefore, the rectifying behavior was seen in the sample of 8cycles.The ideal factor n=1.01 and barrier height for hole=0.59eV also imply that the sample of 8cycles is a good Schottky diode. However, the off current increased when the counts of ALD cycle was increased to 10cycles, which can't be explanted by MISG model. Further investigation is obviously needed.

In **Fig. 2.11 (a),** the best condition of $Al_2O_3$ was applied on P-Ge with different metal, and we can see that the current behavior changed from ohmic to rectifying when the metal work function changed from high to low. In **Fig. 2.11 (b),** the pinning factor we measured was 0.347. The similar situation we can see when we applied the best condition of $Al_2O_3$ on N-Ge, as shown in **Fig. 2.12**; and the pinning factor we measured was 0.495 for N-Ge, as seen in **Fig. 2.12 (b).** Indeed, Fermi-level pinning can be released by inserting the interfacial layer of $Al_2O_3$.

**Fig. 2.13**and **Fig. 2.14**display the I-V characteristics of P-type and N-type depinning sample respectively, which were measured by changing temperature for barrier height extract.

### 2.3.3 $GeO_2$

$GeO_2$ was formed by RTO at 550 ℃ and 500 ℃. In the case of 550 ℃, the off current was saturated even increased the time of RTO from 5s to 10s. The results implied that the interfacial layer was as thick as enough to passivate MIGS. And interfacial layer was too thick so that the additional series resistance degraded the on current, as seen in **Fig. 2.15 (a)**. In the case of 500 ℃, as seen in **Fig. 2.15 (b)**we can see the similar situation like the samples of $Al_2O_3$.When interfacial layer increased the off current decreased, and the best condition is RTO at 500 ℃ in 10s.In the best condition, ideal factor n=1.02 and barrier height for hole=0.58eV showed the good Schottky characteristics.

In **Fig. 2.16 (a),** the best condition of $GeO_2$ was applied on P-Ge with different metal, and we can see that the current behavior changed from ohmic to rectifying when the metal work function changed from high to low. In **Fig. 2.16 (b),** the pinning factor we measured was 0.41. The similar situation we can see when we applied the best condition of $GeO_2$ on N-Ge, as shown in **Fig. 2.17**; and the pinning factor we measured was 0.59 for N-Ge, as seen in **Fig. 2.17 (b).** Indeed, Fermi-level pinning can be released by inserting the interfacial layer of $GeO_2$.

**Fig. 2.18** and **Fig. 2.19**display the I-V characteristics of P-type and N-type depinning sample respectively, which were measured by changing temperature for barrier height extract.

### 2.3.4 $TiO_2$

The insertion of $TiO_2$ also can change the behavior from ohmic to rectifying, and the best recipe is that the thickness of $TiO_2$ is 6nm,as seen in **Fig. 2.20**.By the best recipe, ideal factor n=1.01 and barrier height for hole=0.6eV showed the good Schottky characteristics. But still a little increase of off current was observed as the thickness of $TiO_2$ was increased to 9nm, and the certain reason was unknown.

In **Fig. 2.21 (a),** the best condition of $TiO_2$ was applied on P-Ge with different metal, and we can see that all of the samples showed rectifying behavior. In **Fig. 2.21 (b),** the pinning factor was 0.13 also implied that that's still pinned. But in **Fig. 2.22,** the Schottky barrier height changed when the metal work function changed, and the pinning factor we measured was 0.409. The FLP seemed to be released as the best condition of $TiO_2$ was applied on N-Ge.

**Fig. 2.23** and **Fig. 2.24**display the I-V characteristics of P-type and N-type depinning sample respectively, which were measured by changing temperature for barrier height extract.

The strange phenomenon of $TiO_2$ samples can't be explanted by the reduction of MIGS. But the phenomenon can be explanted if the role of $TiO_2$ is not only the blocking layer but also the semiconductor. We regard the $TiO_2$ as the n-type semiconductor [12], and the band structure [13] was shown in **Fig. 2.25.** The off current of the metal/$TiO_2$/P-Ge was limited by N-P ($TiO_2$-Ge) junction, so that the off current of each samples were same. On the other hand, the barrier height at the interface between metal and $TiO_2$ could be the reason of degradation of on current when using the high work function metal as the electrode. And in metal/$TiO_2$/N-Ge case, the barrier height we measured was at the interface between metal and $TiO_{2,}$ so that the barrier height can be modulated is reasonable.

## 2.4 Conclusion

We showed that's strong FLP on both n- and p-type Ge .Next we successful released the effects of pinning both on n and p type Ge by inserting the interfacial layer of $GeO_2$ and $Al_2O_3$, and made the high SHB for hole in P-Ge case. The pinning factor of $GeO_2$ case was 0.41 for P-Ge and 0.59 for N-Ge, while in $Al_2O_3$ case the pinning factor was 0.347 for P-Ge and 0.495 for N-Ge. According to the pinning factor we calculated of each sample, the effect of de-pinning by using $GeO_2$ was better than one by using $Al_2O_3$, because the interfacial layer of $GeO_2$ cannot only reduced MIGS but also passivated the dangling bonds at the interface. [14]

Finally, we found out the different behavior of $TiO_2$ as a blocking layer by applying it to different metal contact. The insertion of $TiO_2$ layer at the metal/n-Ge interface could change the I-V characteristic from rectifying into ohmic, which is due to the semiconductor-like characteristics of $TiO_2$.

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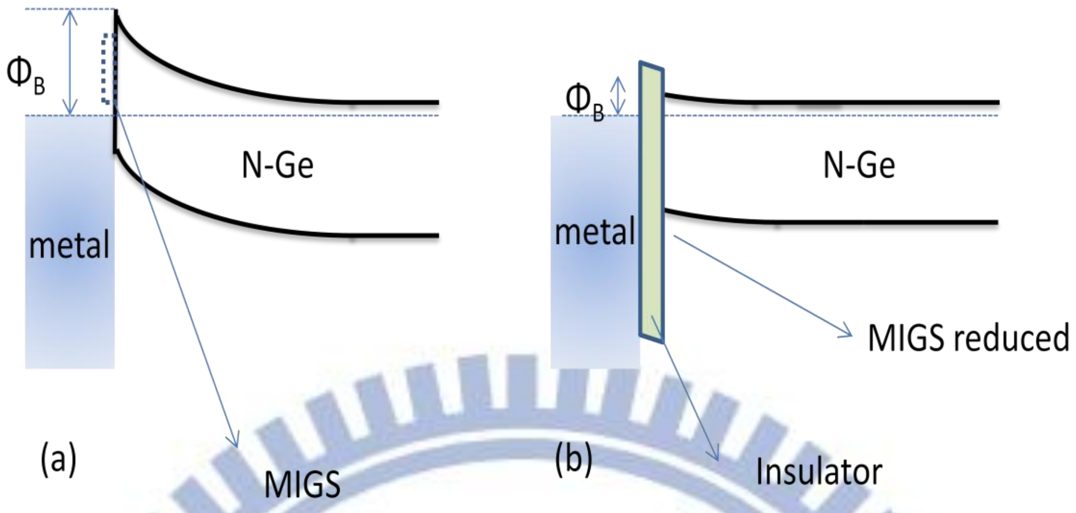
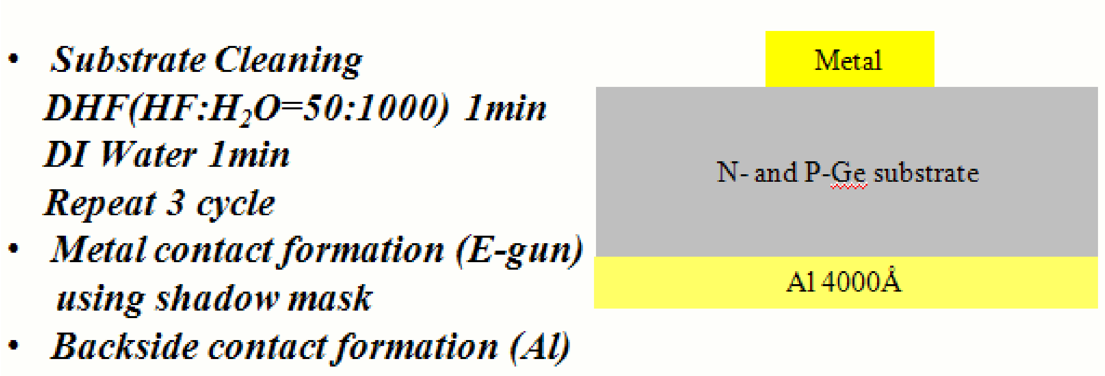


Fig.2.1 In MIGS model, insertion of interfacial layer can reduce MIGS and release FLP. (a) Before. (b) After.



- *Substrate Cleaning*
  *DHF(HF:$H_2O$=50:1000) 1min*
  *DI Water 1min*
  *Repeat 3 cycle*
- *Metal contact formation (E-gun) using shadow mask*
- *Backside contact formation (Al)*

Fig.2.2 Process flow of Ge Schottky junctions and their device structure.

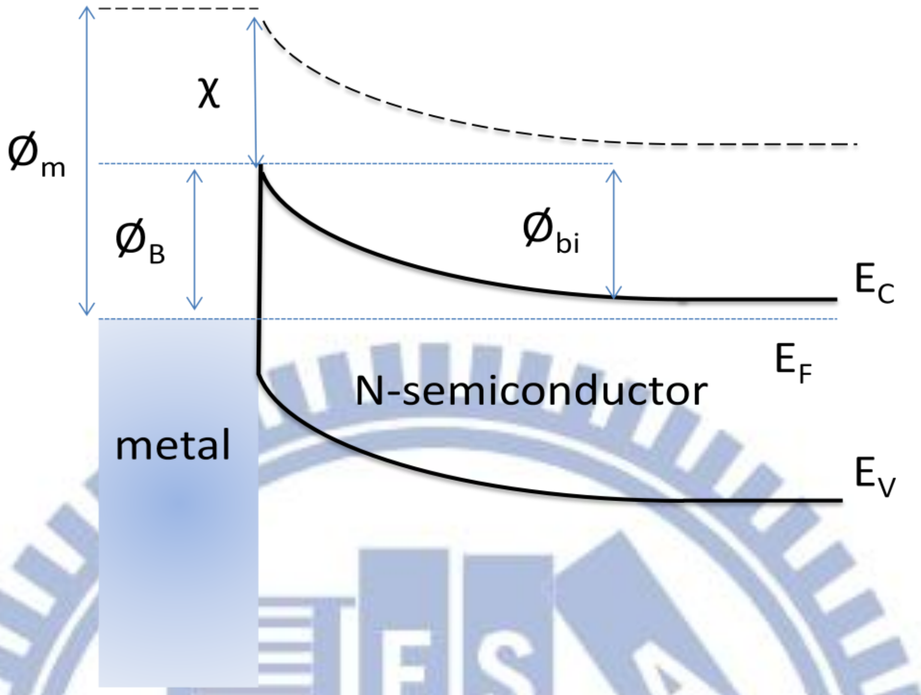


Fig.2.3 Band diagram of a Schottky barrier diode on an n-type substrate.

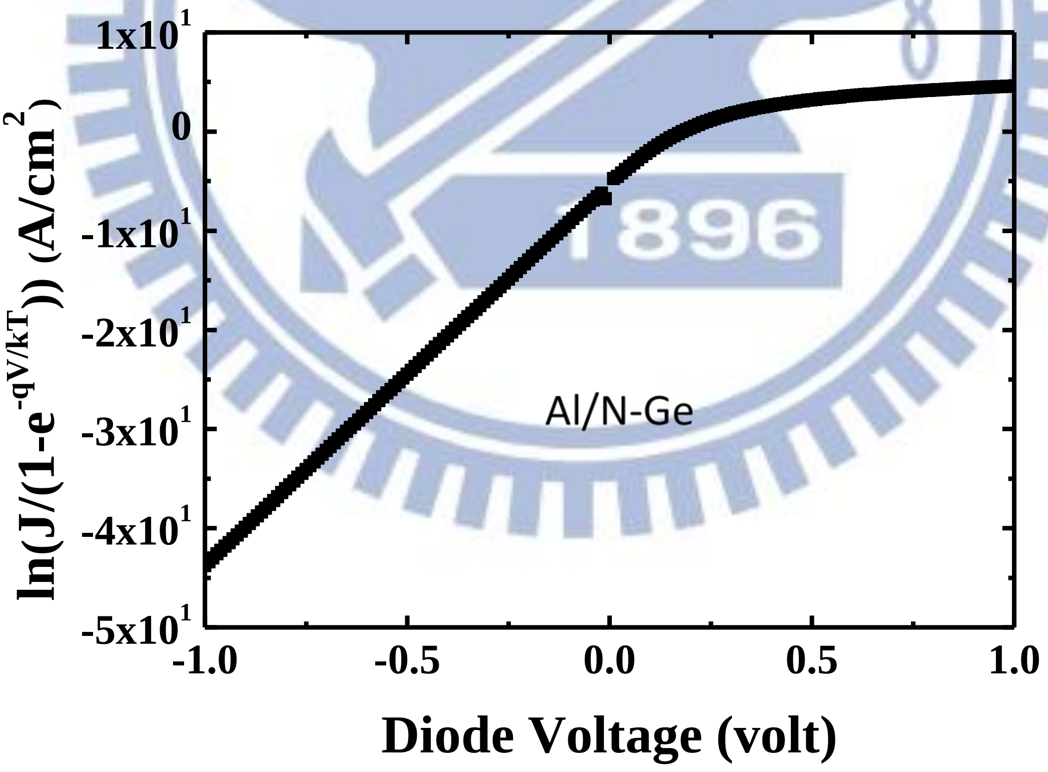


Fig.2.4 A plot of $\ln\left(\frac{J}{\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right]}\right)$ versus voltage.

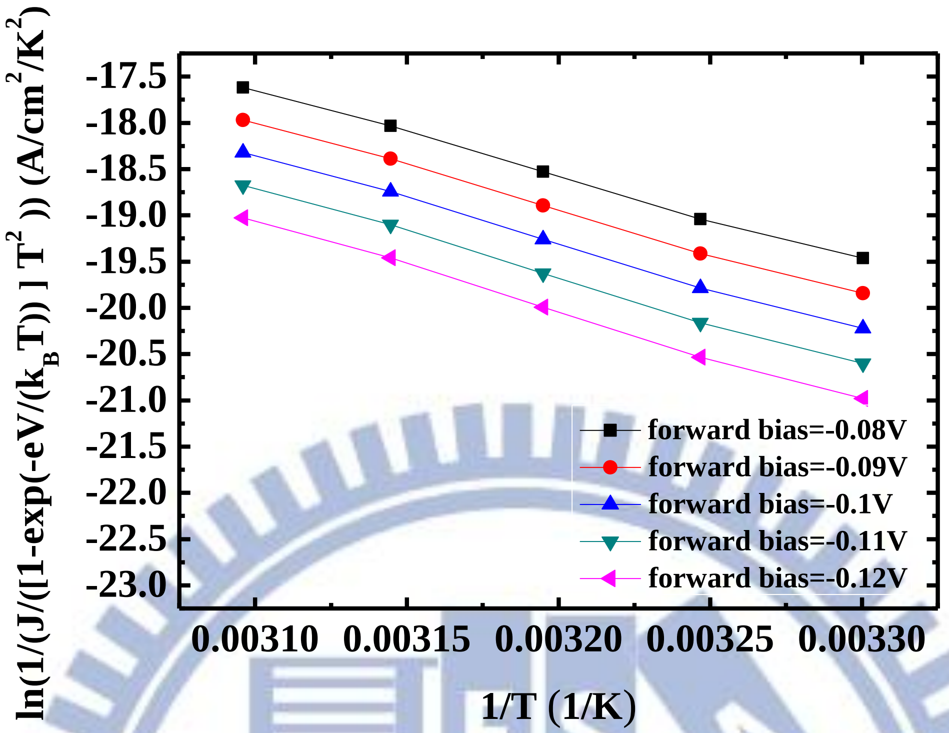


Fig.2.5 A plot of $\ln\left(\frac{J}{\left[1-\exp\left(-\frac{eV}{k_BT}\right)\right]T^2}\right)$ versus $^1/_T$

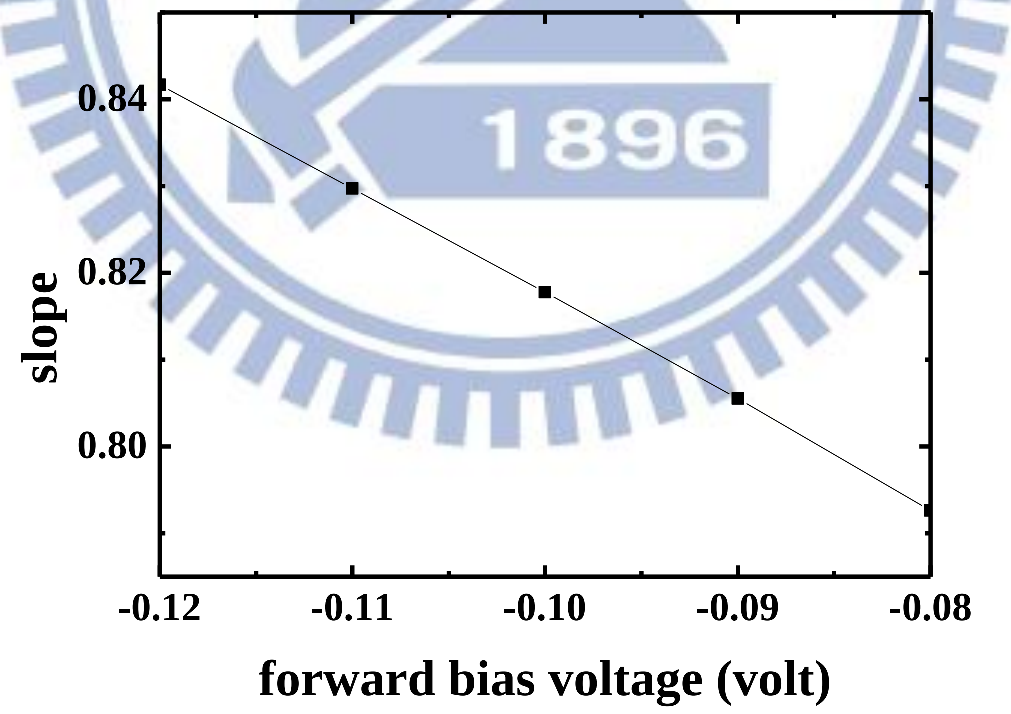
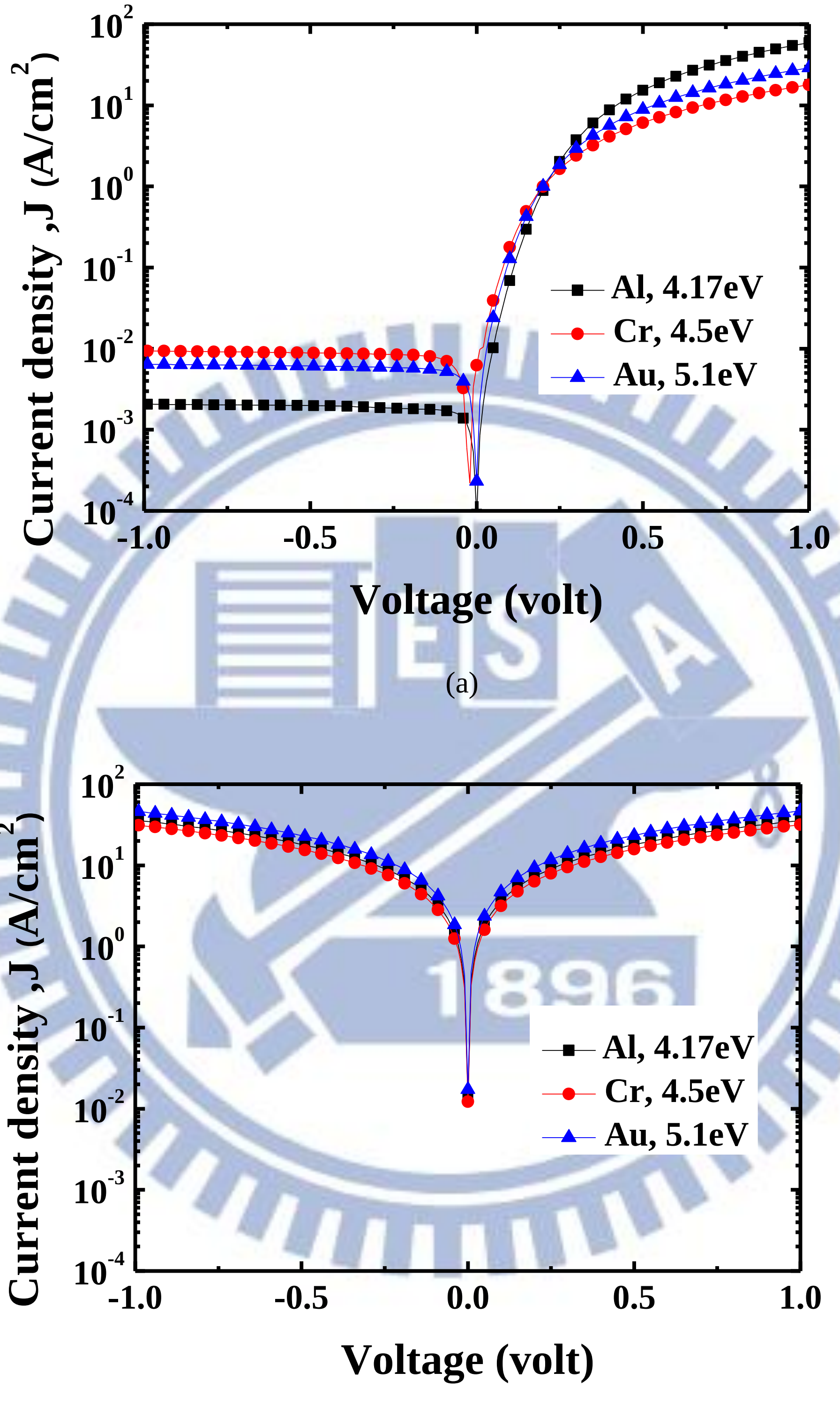


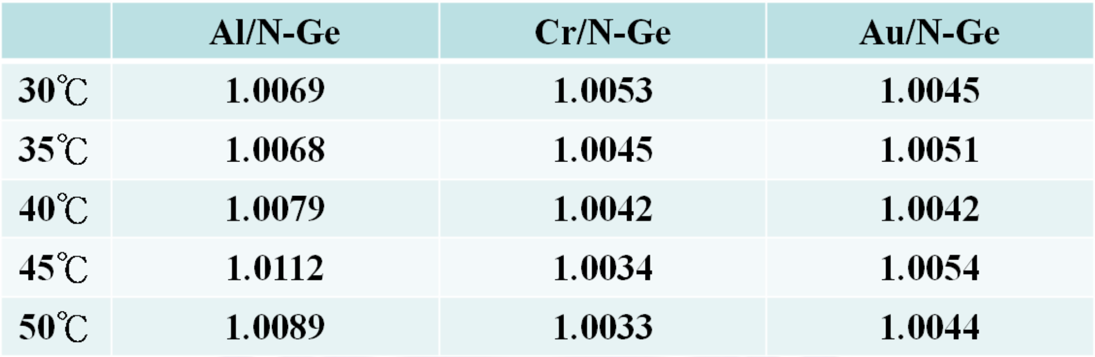
Fig.2.6 A plot of the slope $\frac{e(\emptyset_B - V/n)}{k_BT}$ versus voltage



(a)

(b)

Fig.2.7 I-V characteristics of metal/Ge junction. (a) metal/n-Ge. (b) metal/p-Ge.



| | Al/N-Ge | Cr/N-Ge | Au/N-Ge |
|---|---|---|---|
| 30℃ | 1.0069 | 1.0053 | 1.0045 |
| 35℃ | 1.0068 | 1.0045 | 1.0051 |
| 40℃ | 1.0079 | 1.0042 | 1.0042 |
| 45℃ | 1.0112 | 1.0034 | 1.0054 |
| 50℃ | 1.0089 | 1.0033 | 1.0044 |

Table 2.1 Ideal factor of Al, Cr, and Au at temperature 30℃~50℃

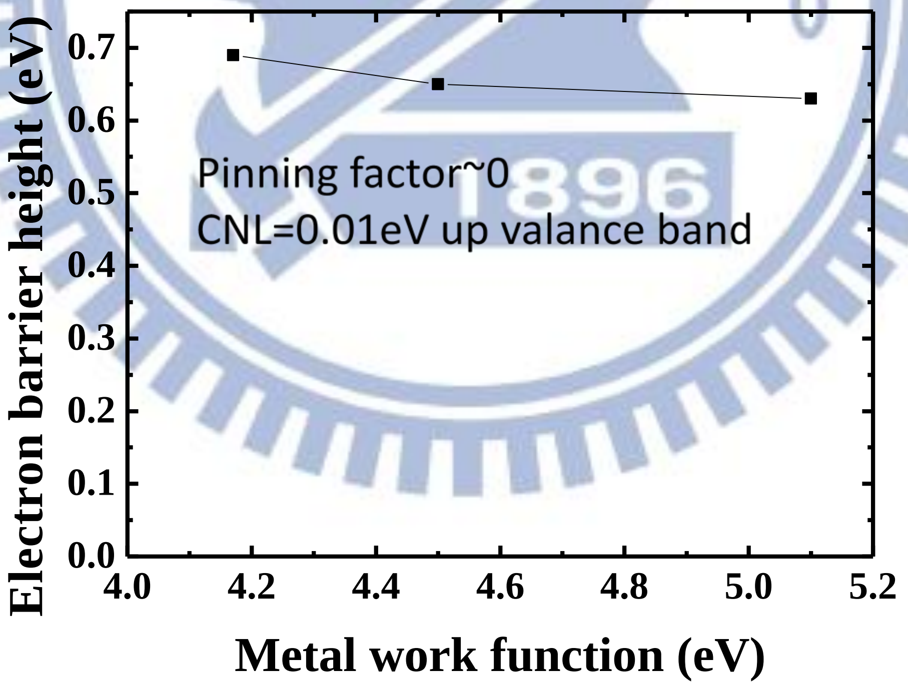
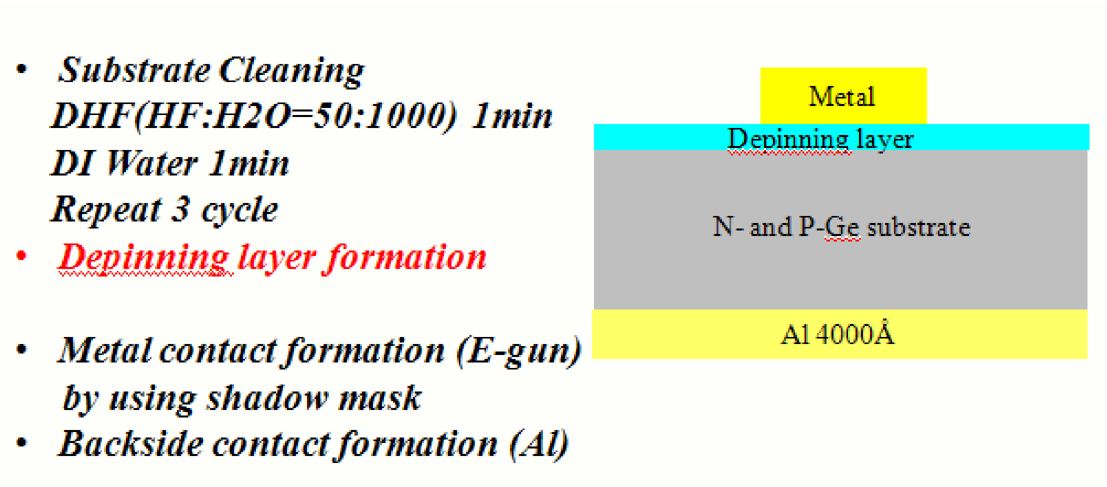


Fig.2.8 Barrier height versus metal work function



- *Substrate Cleaning*
  *DHF(HF:H2O=50:1000) 1min*
  *DI Water 1min*
  *Repeat 3 cycle*
- *Depinning layer formation*

- *Metal contact formation (E-gun)*
  *by using shadow mask*
- *Backside contact formation (Al)*

Fig.2.9 Process flow of Ge Schottky junctions with depinning layer and their device structure.

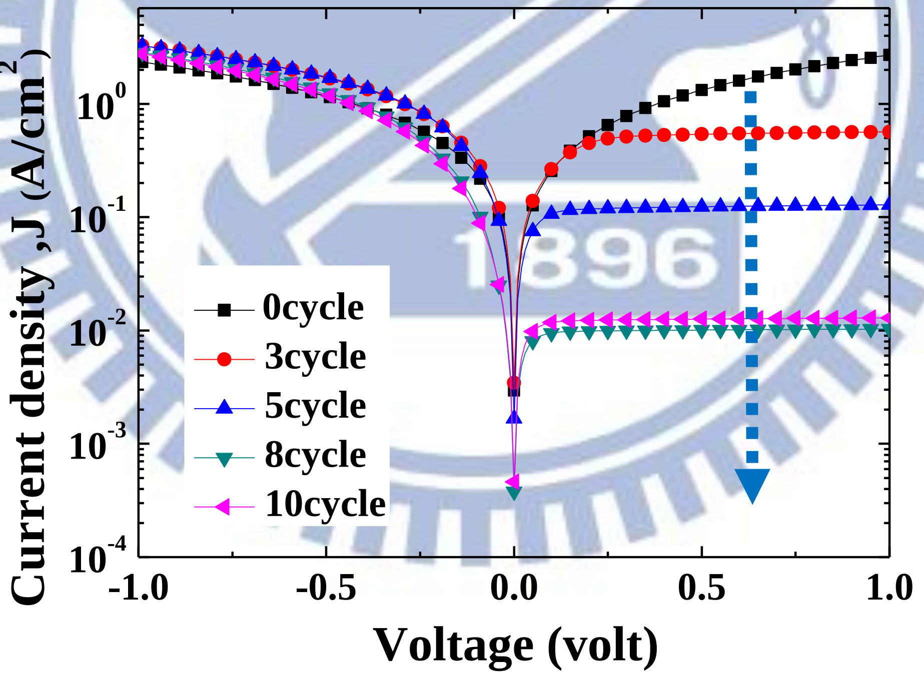
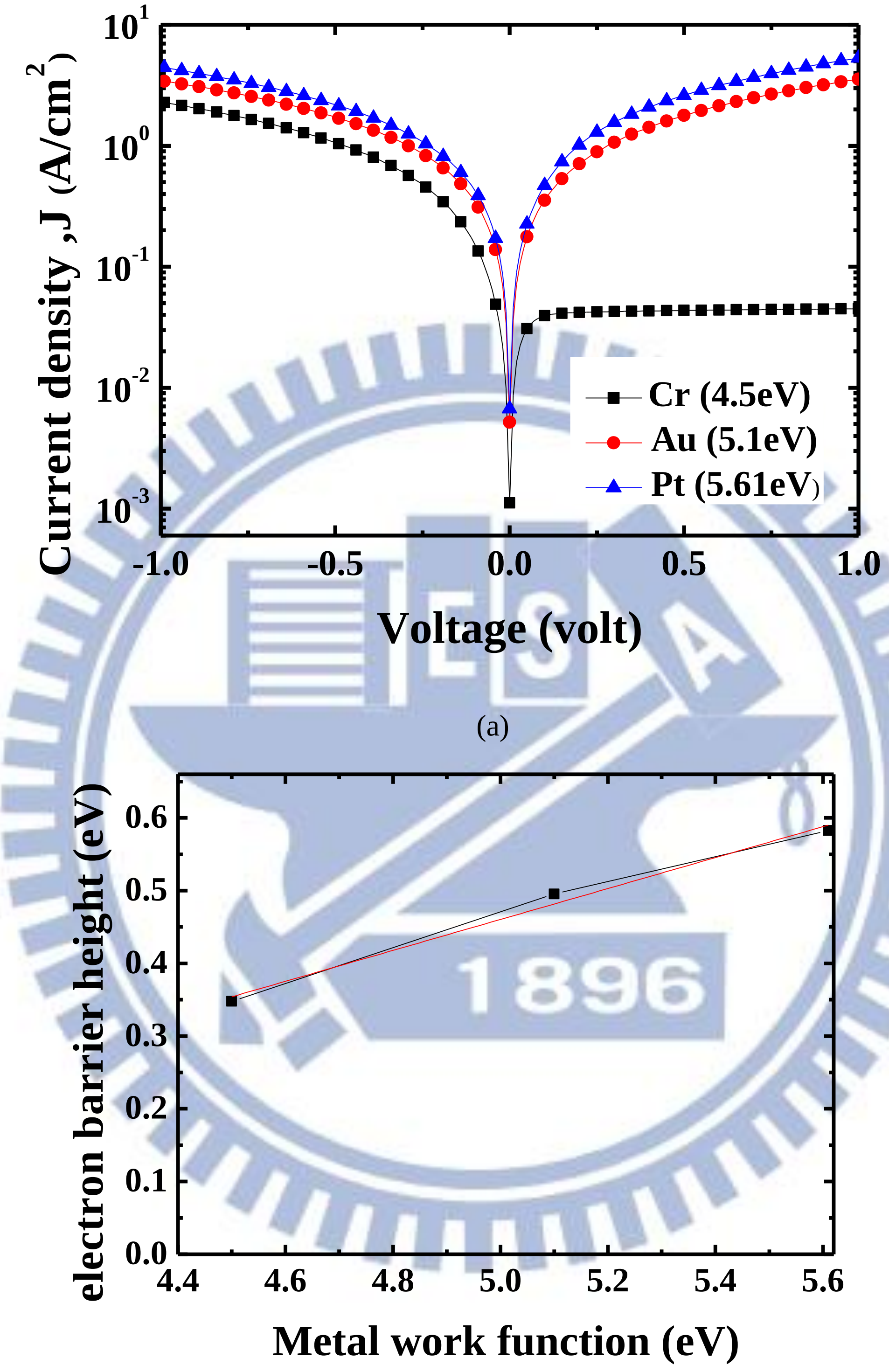


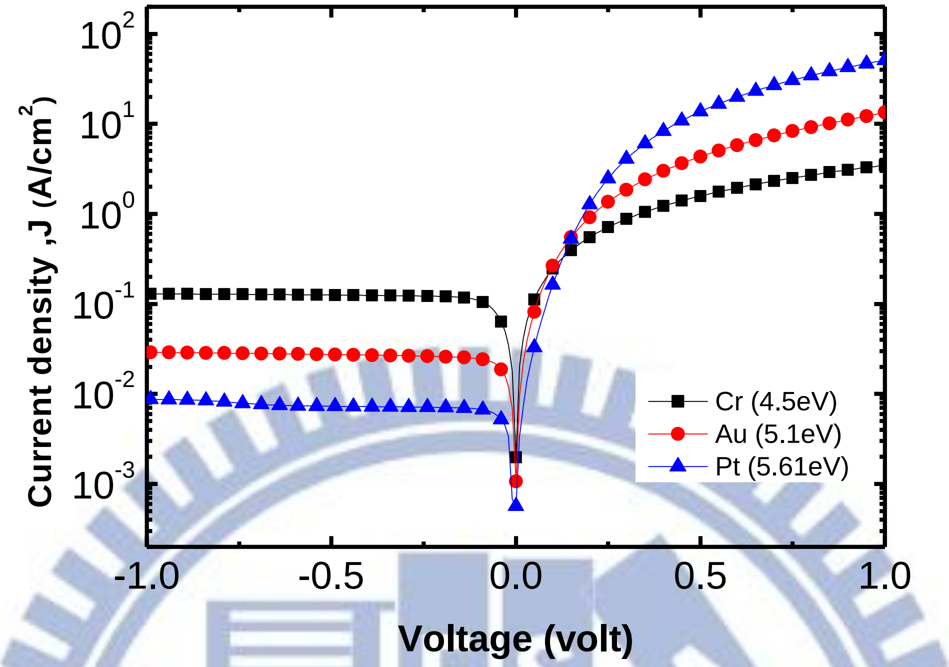
Fig.2.10 I-V characteristics of Ti/p-Ge junction with different thickness of $Al_2O_3$ interfacial layer.



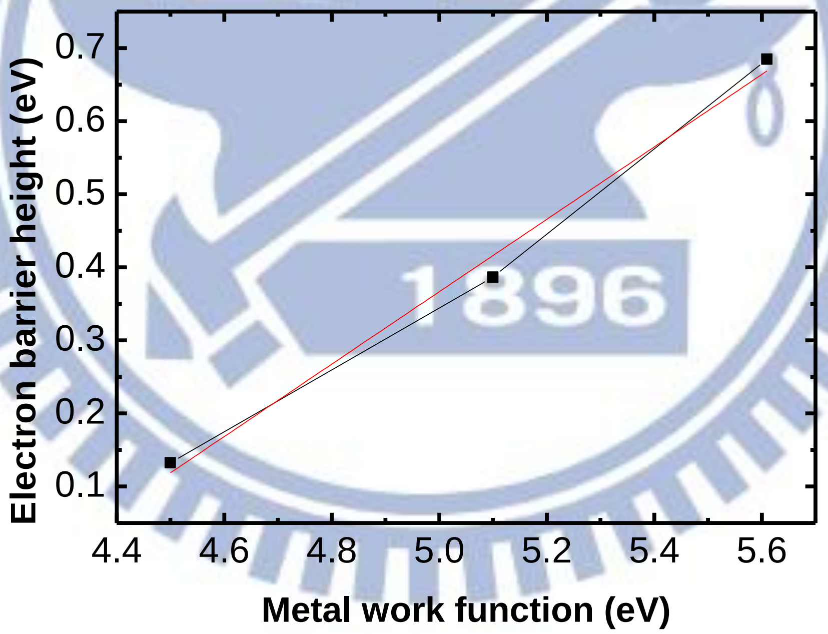
(a)

(b)

Fig.2.11 (a) I-V characteristics and (b) barrier height versus metal work function of metal/p-Ge junction with 8cycles $Al_2O_3$ interfacial layer.

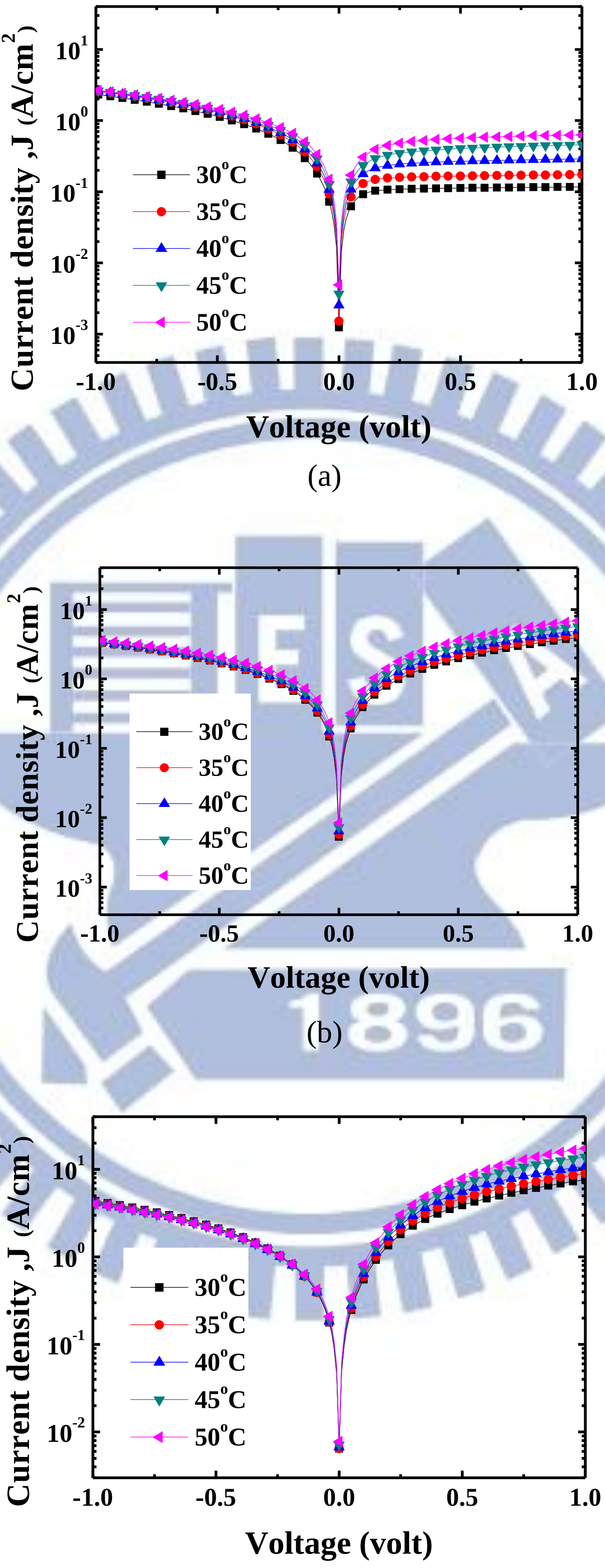


(a)



(b)

Fig.2.12 (a) I-V characteristics and (b) barrier height versus metal work function of metal/n-Ge junction with 8cycles $Al_2O_3$ interfacial layer.

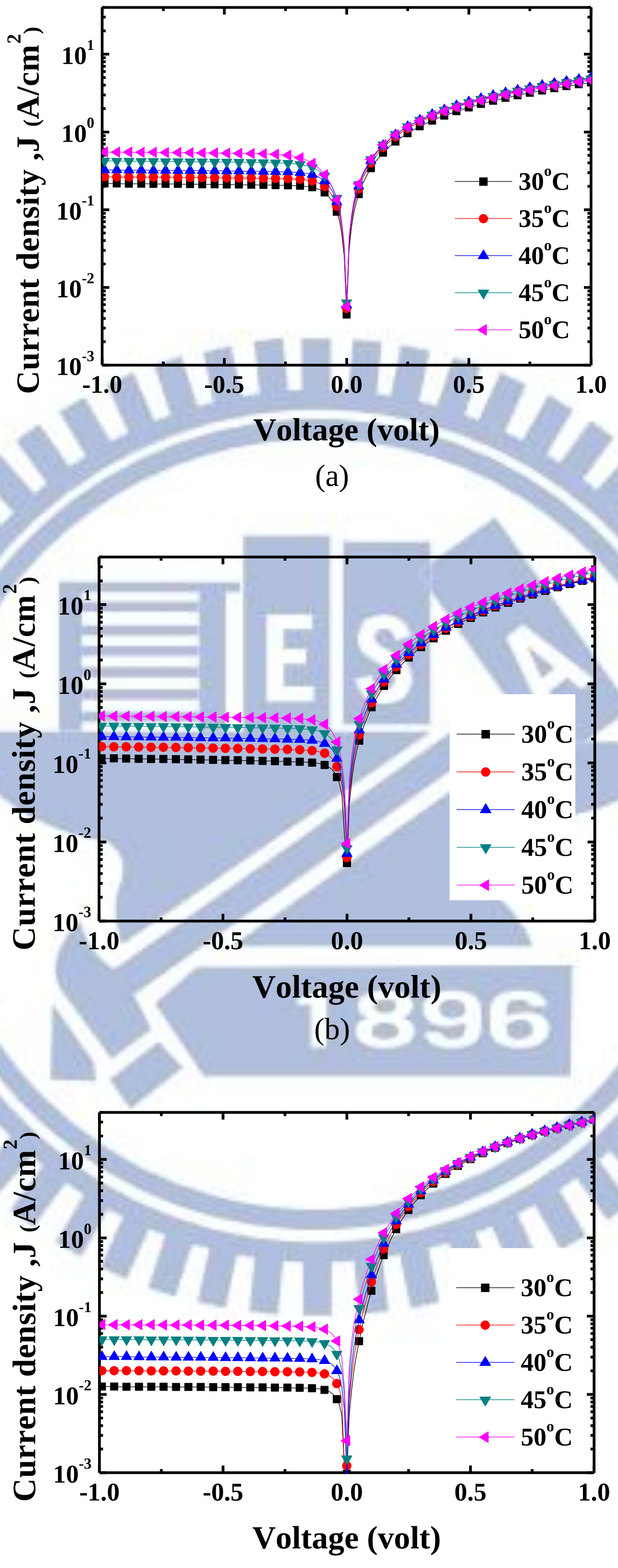


(a)

(b)

(c)

Fig.2.13 I-V characteristics of junction with 8cycles ALD $Al_2O_3$ interfacial layer at 30 ℃ ～ 50 ℃ .(a)Cr/p-Ge. (b) Au/p-Ge. (c) Pt/p-Ge.

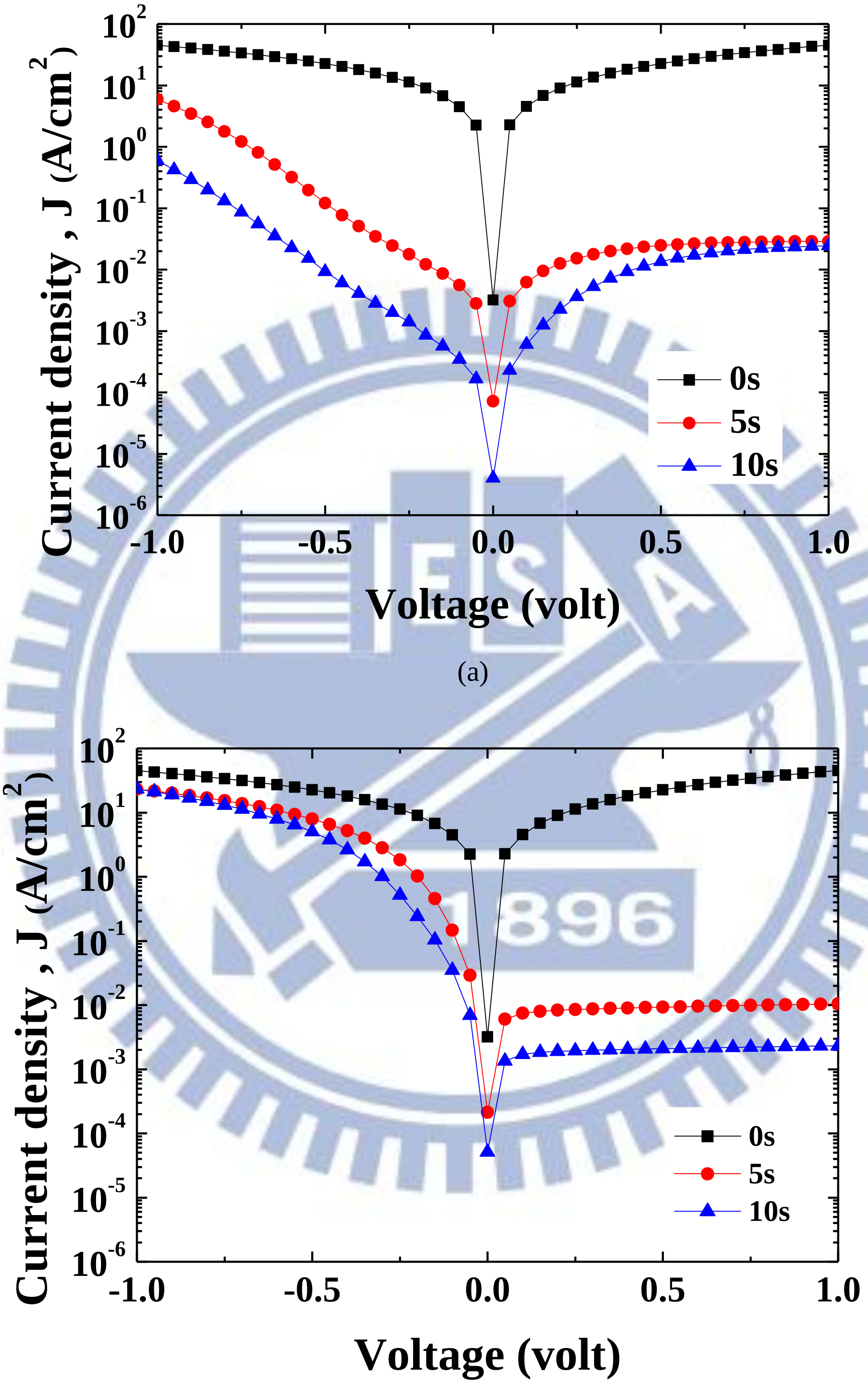


(a)

(b)

(c)

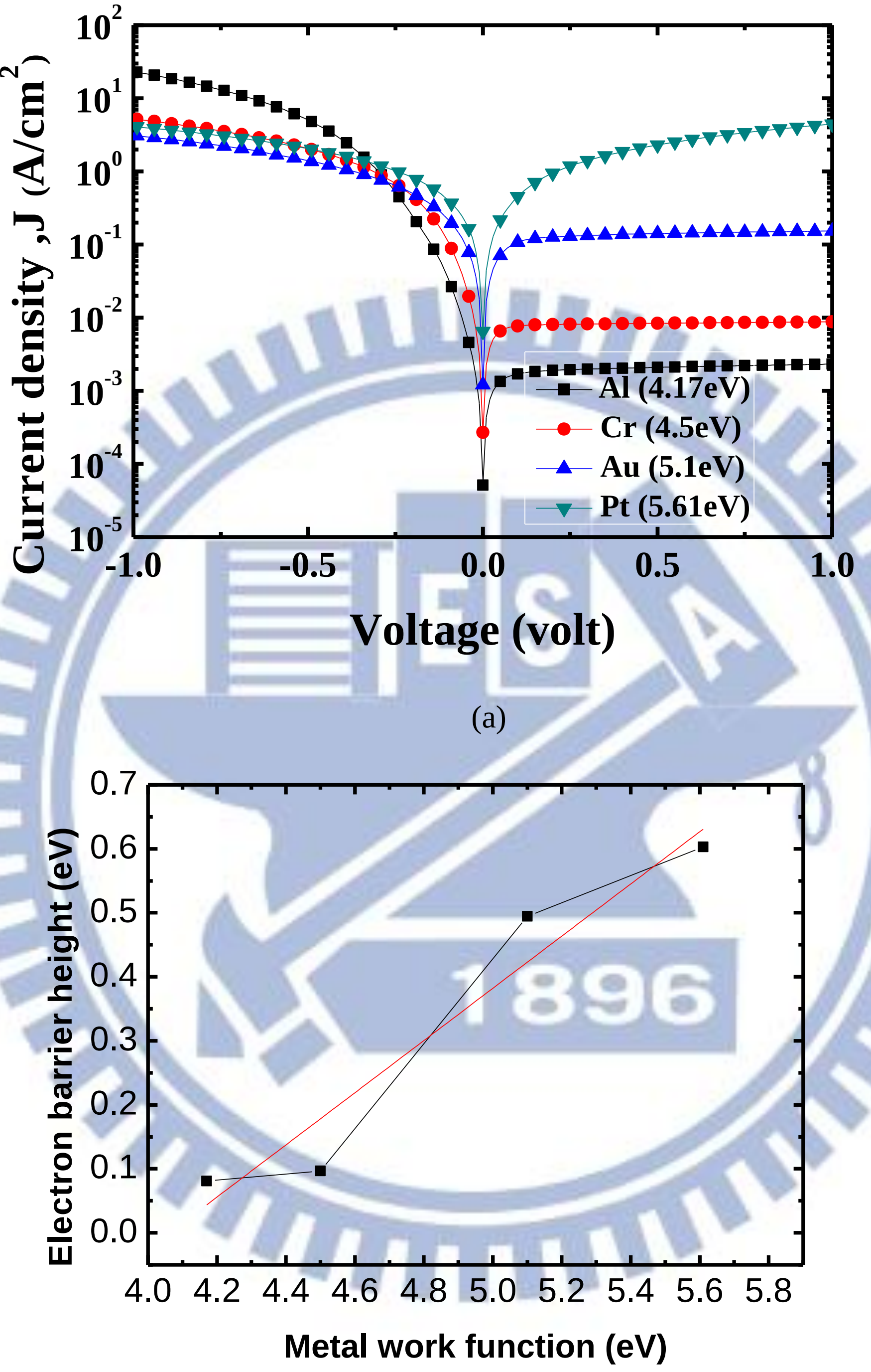
Fig.2.14 I-V characteristics of junction with 8cycles ALD $Al_2O_3$ interfacial layer at 30 ℃ ～ 50 ℃ .(a)Cr/n-Ge. (b) Au/n-Ge. (c) Pt/n-Ge.



(a)

(b)

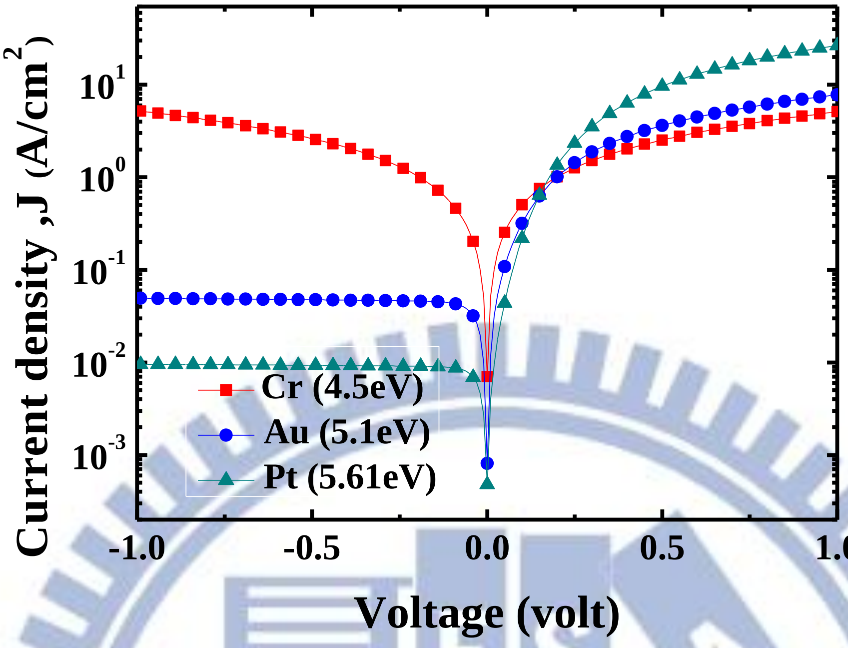
Fig.2.15 I-V characteristics of Al/p-Ge junction with $GeO_2$ interfacial layer formed by (a) 550 ℃ (b) 500 ℃.



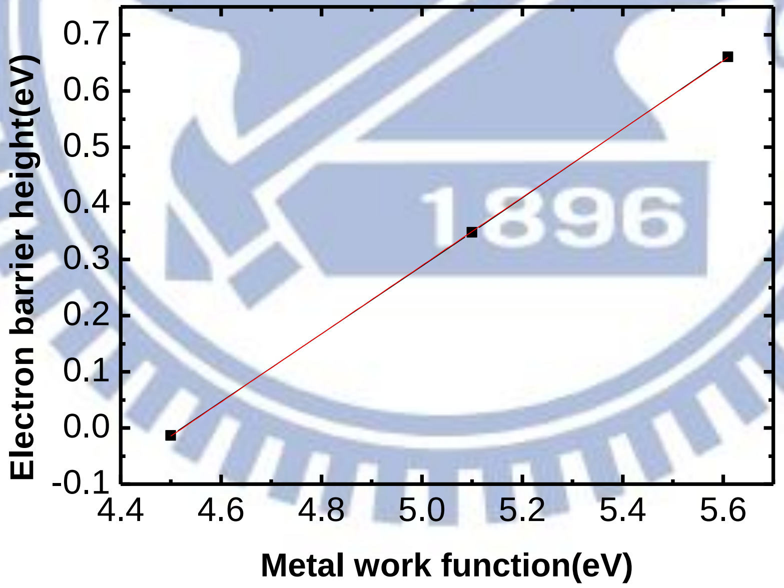
(a)

(b)

Fig.2.16 (a) I-V characteristics and (b) barrier height versus metal work function of metal/p-Ge junction with 500 ℃ 10s $GeO_2$ interfacial layer.

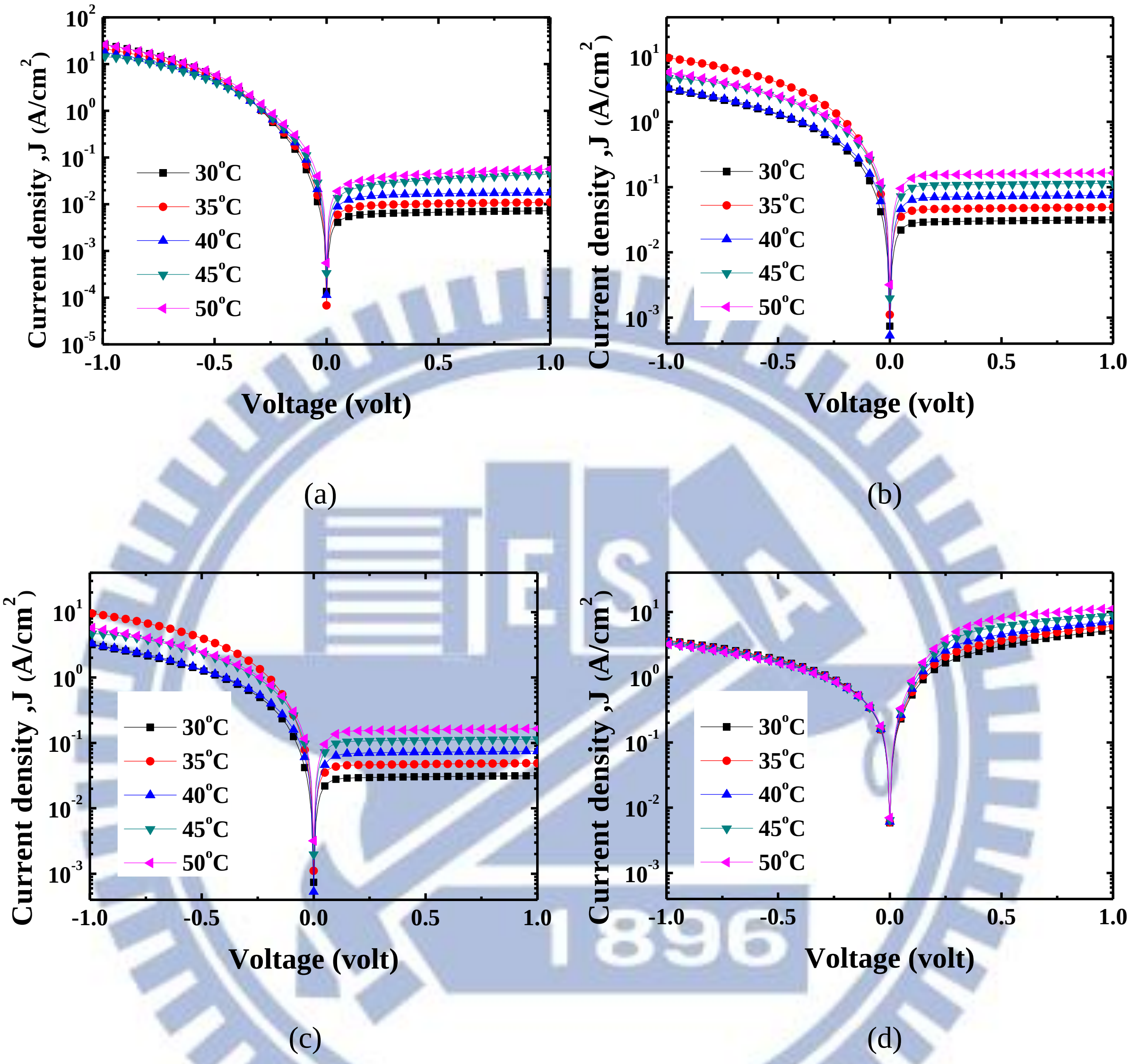


(a)



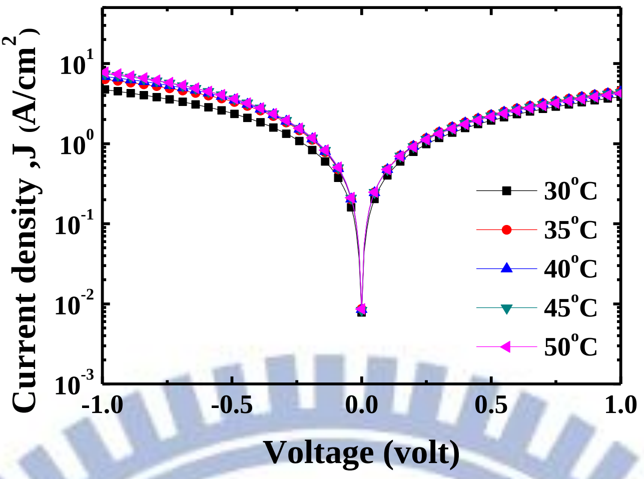
(b)

Fig.2.17 (a) I-V characteristics and (b) barrier height versus metal work function of metal/n-Ge junction with 500 ℃ 10s $GeO_2$ interfacial layer.

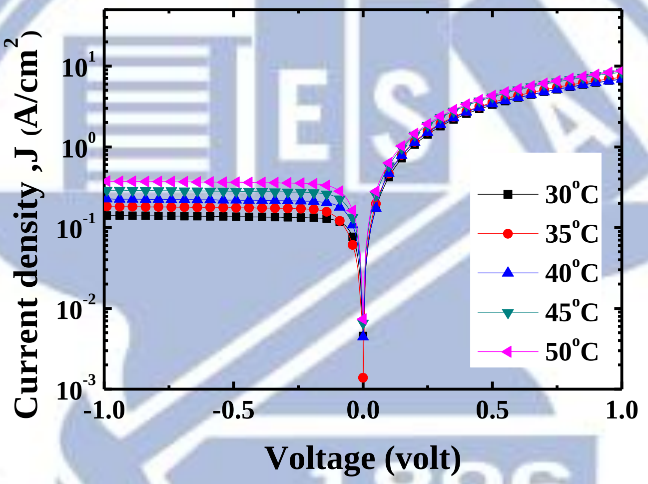


(a) (b) (c) (d)

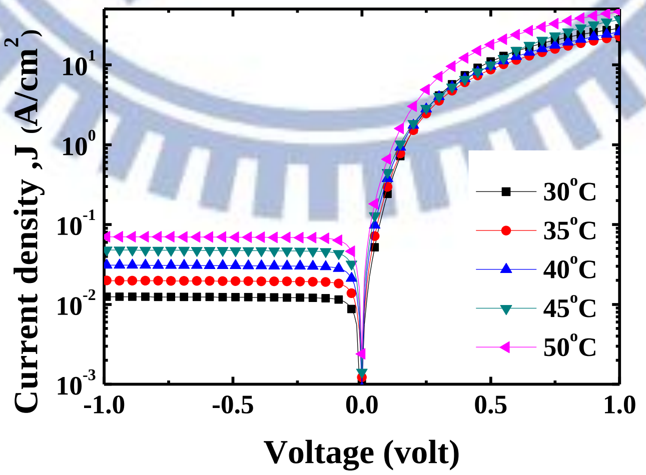
Fig.2.18 I-V characteristics of junction with 500 ℃ 10s $GeO_2$ interfacial layer. at 30 ℃ ～ 50 ℃ .(a) Al/p-Ge. (b) Cr/p-Ge. (c) Au/p-Ge. (d) Pt/p-Ge.



(a)



(b)



(c)

Fig.2.19 I-V characteristics of junction with 500 ℃ 10s $GeO_2$ interfacial layer. at 30 ℃ ～ 50 ℃ .(a) Cr/n-Ge. (b) Au/n-Ge. (c) Pt/n-Ge.

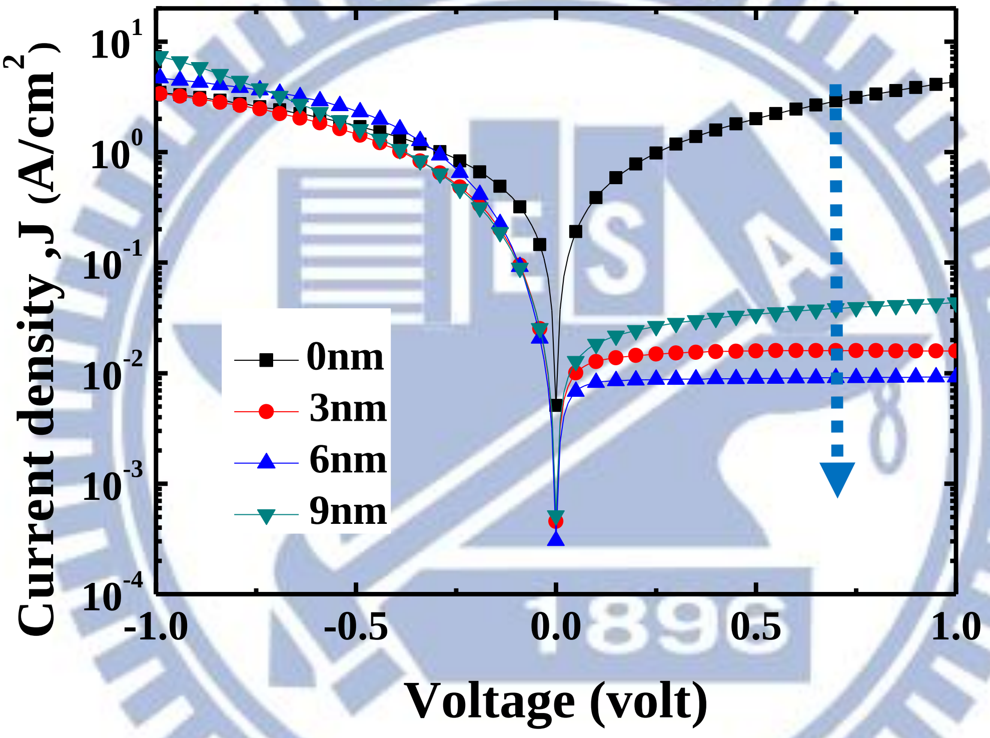
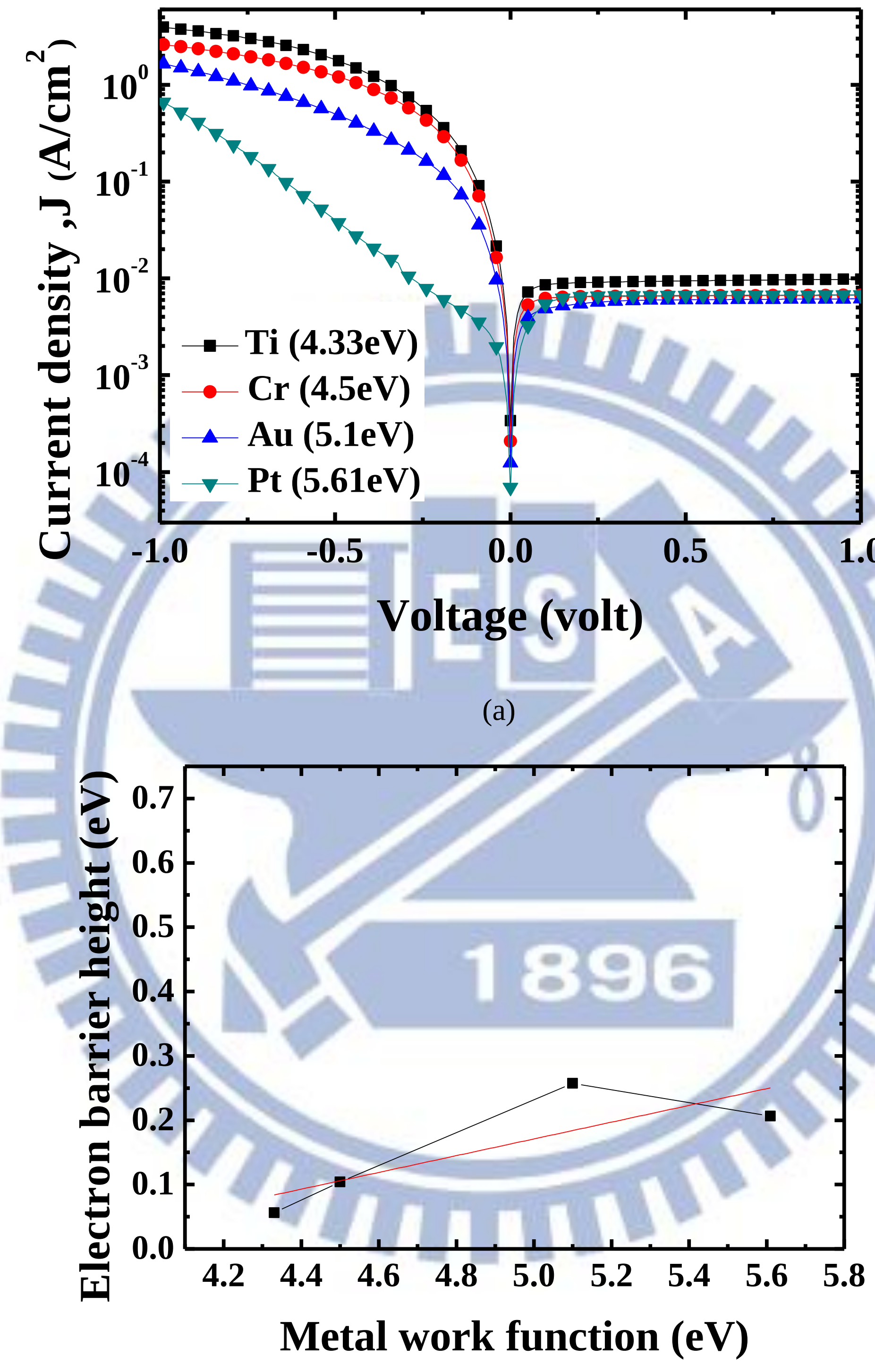


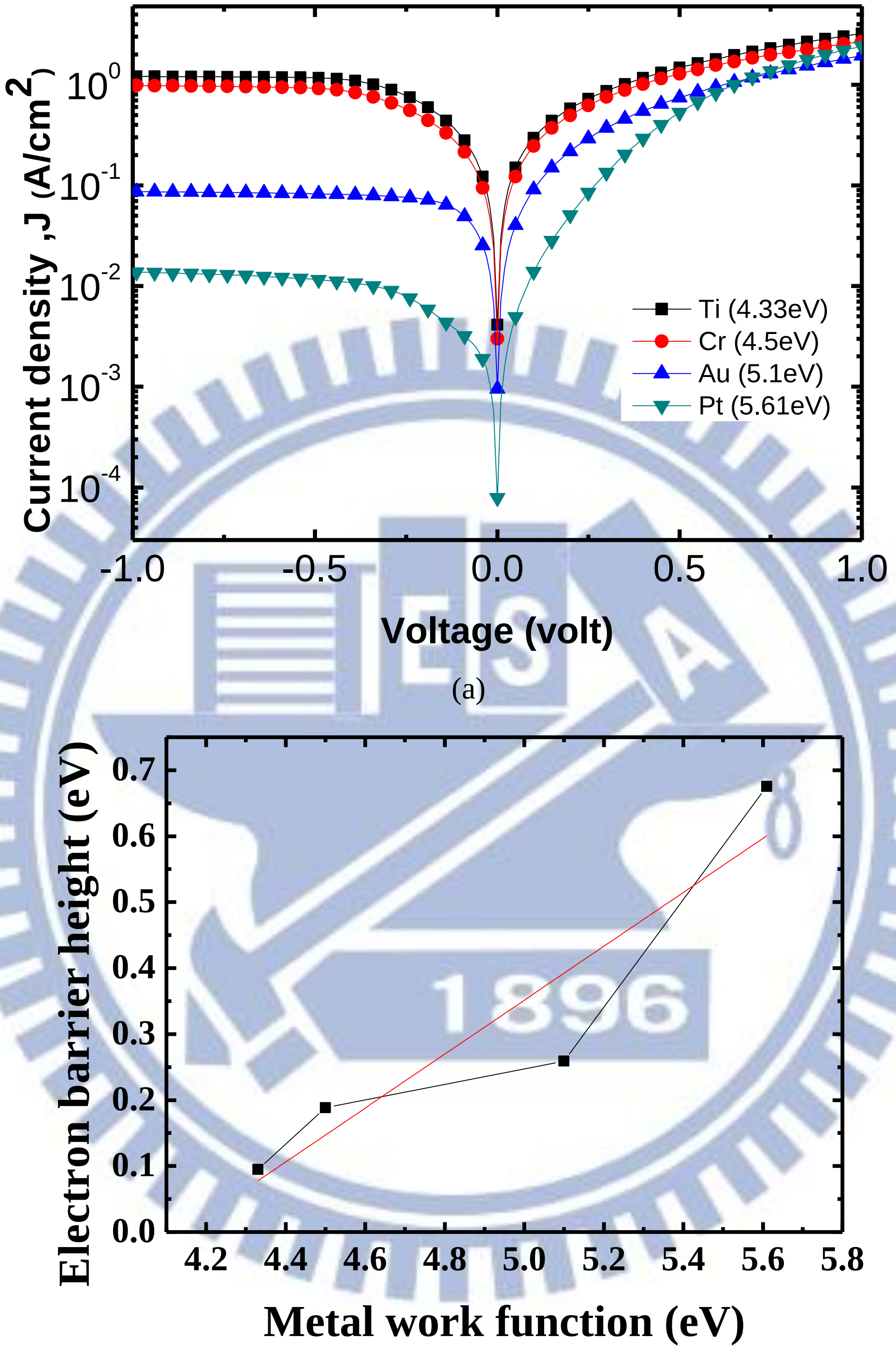
Fig.2.20 I-V characteristics of Ti/P-Ge junction with different thickness of $TiO_2$ interfacial layer.



(a)

(b)

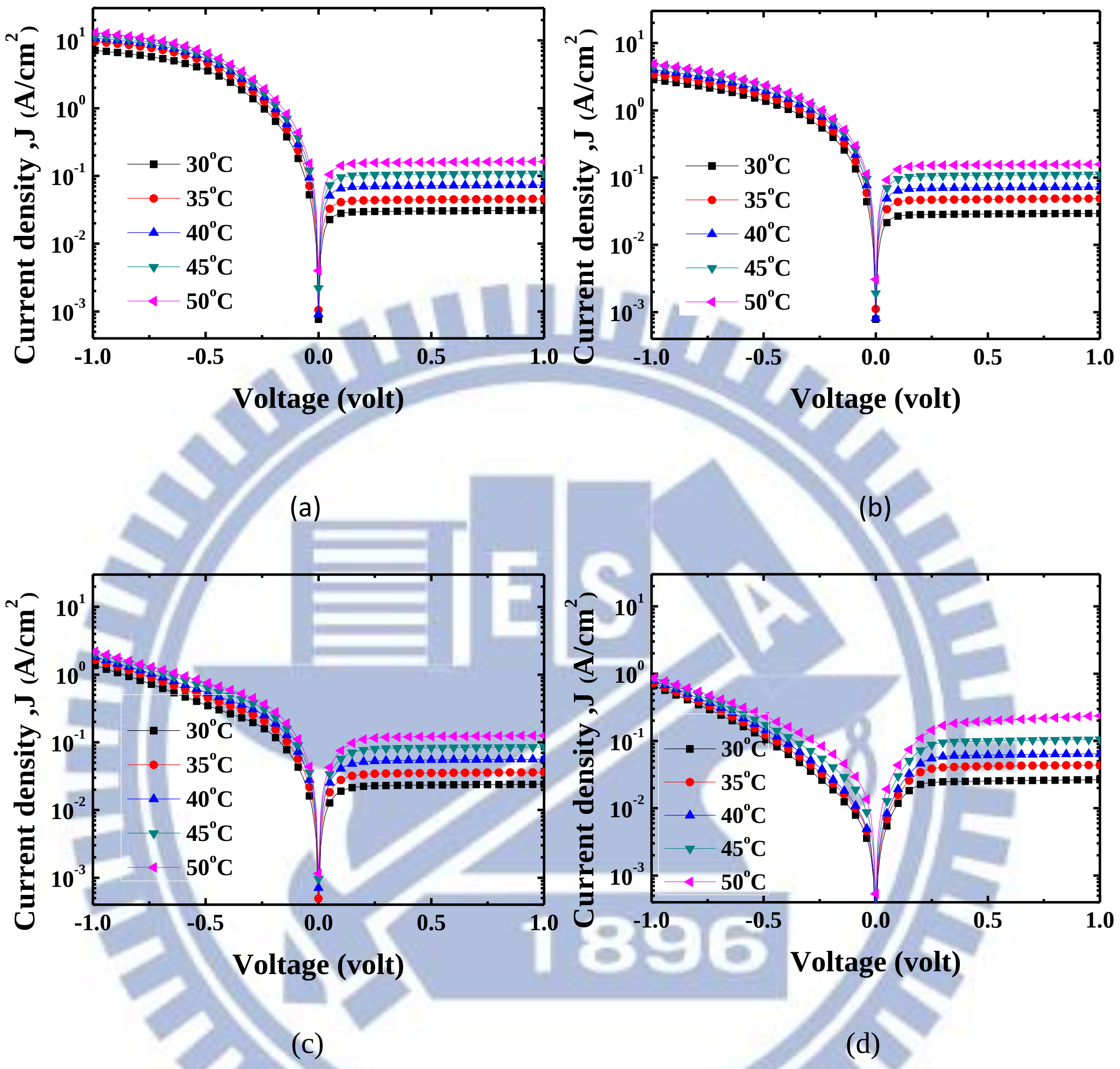
Fig.2.21 (a) I-V characteristics and (b) barrier height versus metal work function of metal/p-Ge junction with 6nm $TiO_2$ interfacial layer.



(a)

(b)

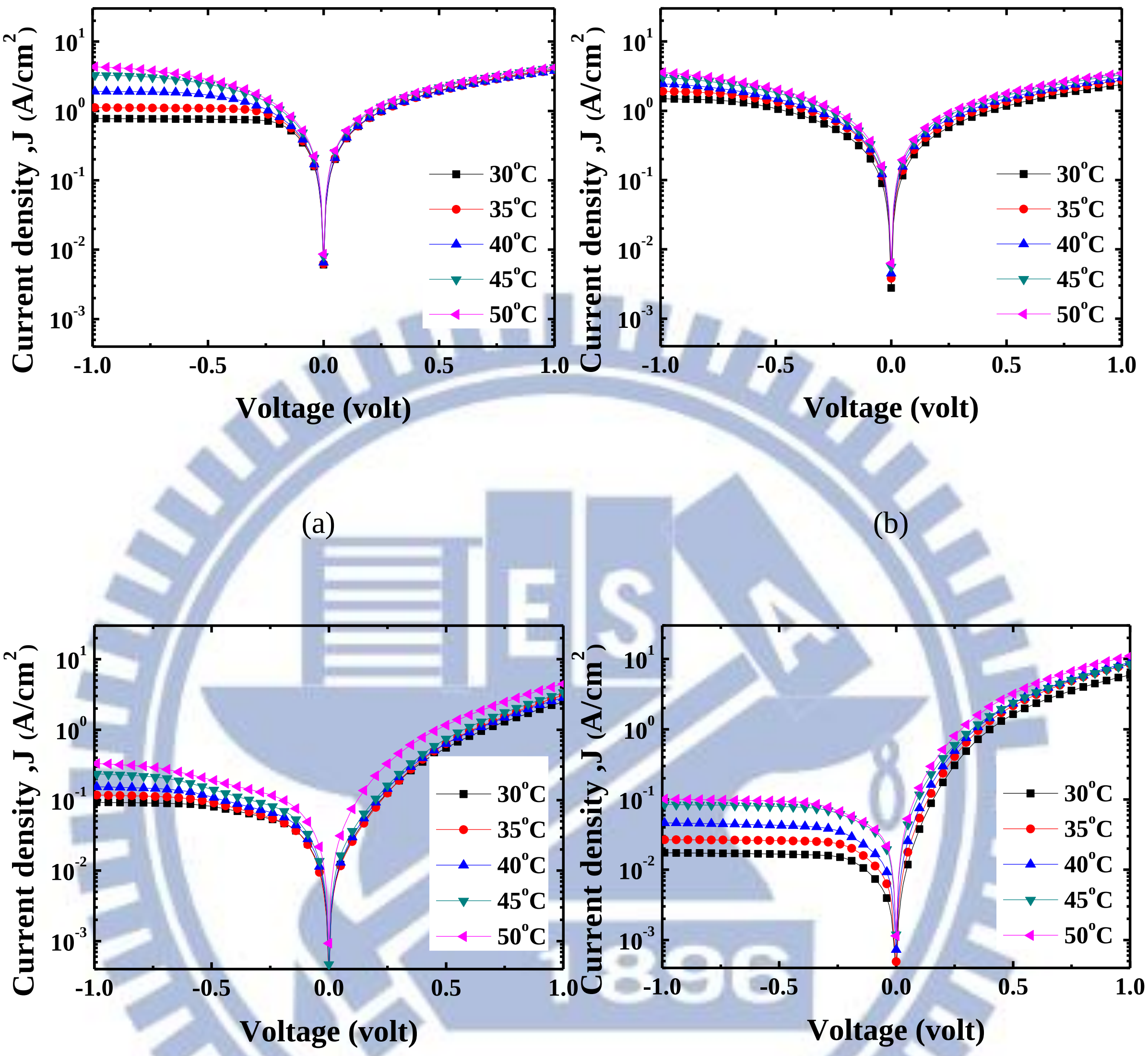
Fig.2.22 (a) I-V characteristics and (b) barrier height versus metal work function of metal/n-Ge junction with 6nm $TiO_2$ interfacial layer.



(a) (b)

(c) (d)

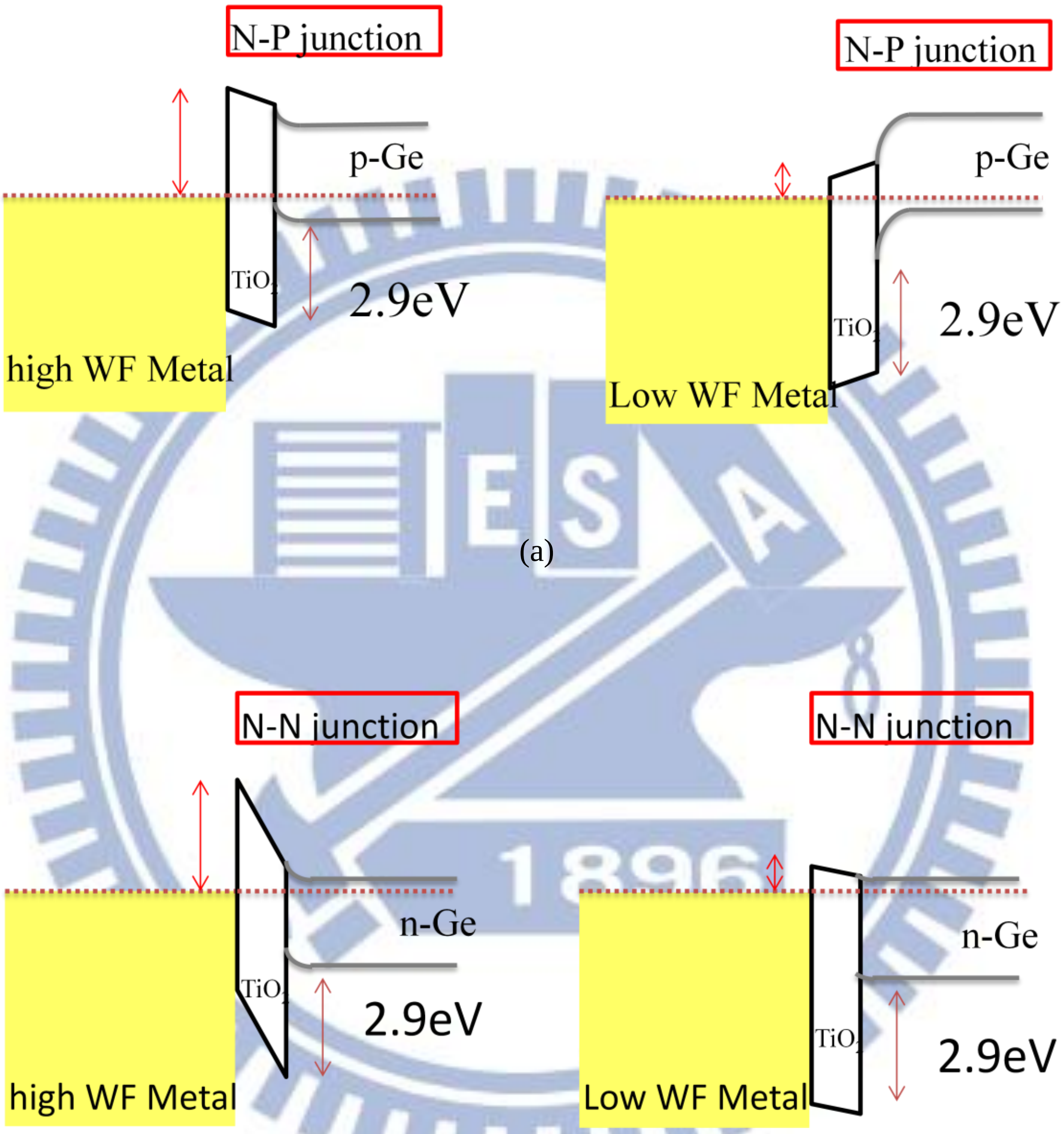
Fig.2.23 I-V characteristics of junction with 6nm $TiO_2$ interfacial layer. at 30 ℃ ～50 ℃ .(a) Ti/p-Ge. (b) Cr/p-Ge. (c) Au/p-Ge. (d) Pt/p-Ge.



(a) (b)

(c) (d)

Fig.2.24 I-V characteristics of junction with 6nm $TiO_2$ interfacial layer. at 30 ℃ ～50 ℃ .(a) Ti/n-Ge. (b) Cr/n-Ge. (c) Au/n-Ge. (d) Pt/n-Ge.



(a)

(b)

Fig.2.25 Band structure of junctions as $TiO_2$ was regarded as an n-type semiconductor (a) metal/$TiO_2$/p-Ge (b) metal/$TiO_2$/n-Ge

# Chapter 3

# Metal S/D Ge-MOSFET and Conventional N-MOSFET with a Depinning Layer

## 3.1 Introduction

When the technology node of Si complementary metal-oxide-semiconductor (CMOS) comes to 22nm node, people are looking for new material to replace Si to achieve much higher performance. Ge is one of potential candidates to replace Si due to the higher electron and hole mobility of Ge. Although high hole and electron mobility have been reported for Ge p-FET[1] and Ge n-FET[2-5], the S/D junction technologies for Ge MOSFETs have still some problems such as low solid solubility, and a faster diffusion rate, especially the n-type MOSFET.[6] To make matters worse, Fermi-level was pinned near valance band in Ge, which made the barrier height at metal/n-Ge interface always high and leads to a large series resistance in Ge n-MOSFET.[7-8]

To reduce S/D parasitic resistance, metal S/D could be a promising candidate. But the FLP effect makes the realization of n-Ge metal S/D MOSFET difficult, because the Schottky barrier height (SBH) for electron is high and that for hole is small. Therefore, releasing FLP is necessary to achieve the high performance Ge CMOS. We adopt the depinning layer experience from Chapter 2 to release the FLP on both conventional and metal S/D n-MOSFET.

In this chapter, metal S/D p-MOSFET was fabricated at first. Next, metal S/D n-MOSFET was fabricated with the $GeO_2$ and $TiO_2$ depinning layer. Finally, we tried to use the insertion of $TiO_2$ at metal/n-Ge interface to reduce the parasitic S/D resistance by declining SBH.

## 3.2 Metal S/D MOSFET

### 3.2.1 Fabrication of Metal S/D Ge p-MOSFET

(100)-oriented n-Ge substrate doped with Sb at level of 1.5E14cm$^{-3}$ (resistivity ca. 10Ω · cm) was used for Ge p-MOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide, then a 420-nm-thick $SiO_2$ layer was capped for the field oxide by PECVD.

First, active area (AA) was opened through the 1$^{nd}$ Mask, followed by deposition of Pt as metal S/D through the 2$^{nd}$ Mask by lift-off method. Next, $GeO_2$ was formed by 500 ℃ 10s RTO process as passivation layer, followed an 80 cycles ALD-$Al_2O_3$ was deposited as the high-k gate dielectric. After that, a 400nm Al metallization was performed which was then patterned to define the gate metal pad through the 3$^{nd}$ Mask. Finally, a thermal coater 400nm Al layer was deposited at the backside contact.

The process flow and device structure are shown in **Fig. 3.1.**

### 3.2.2 Basic Device Characteristics

The $I_D$-$V_G$ characteristics of the p-MOSFET are shown in **Fig. 3.2(a)**. The $I_{on}/I_{off}$ ratio was almost 3 orders, and the subthreshold swing was 306mV/decade. **Fig. 3.2(b)** showed the $I_D$-$V_D$ characteristics of the p-MOSFET.

### 3.2.3 Fabrication of Metal S/D Ge n-MOSFET

(100)-oriented n-Ge substrate doped with Ga at level of 2E15cm$^{-3}$ (resistivity ca. 2Ω · cm) was used for Ge p-MOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide, then a 420-nm-thick $SiO_2$

layer was capped for the field oxide by PECVD.

First, active area (AA) was opened through the 1$^{nd}$ Mask, followed by the formation of depinning layer by $GeO_2$ and $TiO_2$. $GeO_2$ was formed by RTO 500 ℃ 10s and 6nm $TiO_2$ was formed by ALD. Right after the formation of depinning layer, a 400nm Al layer was deposited and then defined as S/D through the 2$^{nd}$ Mask. After that, an 80 cycles ALD-$Al_2O_3$ was deposited as the high-k gate dielectric. Because the Al/$TiO_2$/Ge junction exhibited the poor thermal stability, the operation temperature of ALD must to be down to 100 ℃ for $TiO_2$ sample, as seen in **Fig. 3.3.**A 400nm Al metallization was performed which was then patterned to define gate metal pad through the 3$^{nd}$ Mask. Finally, a400nm Al layer was deposited as the backside contact.

The process flow and device structure are shown in **Fig. 3.4.**

### 3.2.4 Device Characteristics

Because the thermal budget of S/D, we can't make the same passivation layer by RTO $GeO_2$ just like the manufacture of p-MOSFET. Without the passivation layer, device exhibited the poor performance. The $I_D$-$V_G$ and $I_D$-$V_D$ characteristics of the n-MOSFET with $GeO_2$ interfacial layer are shown in **Fig. 3.5(a)** and **Fig. 3.5(b)**. Apart from the poor gate control ability as seen in $I_D$-$V_G$ plot, the drain current at low drain voltages was not linearly increasing as $V_D$ increased, which implied that was a barrier between channel and S/D. **Fig. 3.6(a)** and **Fig 3.6(b)** show the $I_D$-$V_G$ and $I_D$-$V_D$ characteristics of the n-MOSFET with $TiO_2$ interfacial layer. The poor device performance still was a problem in the case of $TiO_2$. But the drain current was not limited at low drain voltage, as seen in **Fig 3.6(b).**

The drain current at low drain voltages was different between the $TiO_2$ case and $GeO_2$ case, which could be due to the different conduction band offset of each other. As we know, electron current is the major current when n-MOSFET at on-state. Therefore, apart from the good Schottky junction for reducing leakage current, the small barrier height between metal S/D and channel is essential to realize a good SB MOSFET. The metal/n-Ge with $TiO_2$ interfacial layer could be more ohmic than the one with $GeO_2$ interfacial layer, as seen in **Fig. 3.7(a)** and **Fig. 3.7(b)**. This is due to the smaller conduction band offset of $TiO_2$ [9-10], as seen as **Fig. 3.8**.

## 3.3 Effect of $TiO_2$ Interfacial Layer at Metal/n-Ge Junction on n-MOSFET

### 3.3.1 Fabrication of n-MOSFET

(100)-oriented n-Ge substrate doped with Ga at level of 2E17cm$^{-3}$ (resistivity ca. $0.02\Omega \cdot cm$) was used for Ge p-MOSFET fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide. Then, a $GeO_2$ layer was formed by RTO at 500 ℃ 30s before a 420-nm-thick $SiO_2$ layer capped for the field oxide by PECVD.

First, the S/D region was opened through the 1st Mask, followed by implantation of the P ($1 \times 10^{15} cm^{-2}$, 30keV) into the p-Ge, while dopant activation condition was 600 ℃, 10s. Next, active area (AA) was opened through the 2nd Mask, followed by 500 ℃ 10s $GeO_2$ passivation layer, and then an 80 cycles ALD-$Al_2O_3$ was deposited as the high-k gate dielectric. After that, the wafers were split into two conditions: a 6nm $TiO_2$ layer was deposited after and before the excavation of contact hole on S/D region through the3rd Mask. A 400nm Al metallization was performed which was then patterned to define metal pads through the 4th Mask. Finally, a 400nm Al layer was deposited as the backside contact.

The process flow and device structure are shown in **Fig. 3.9.**

**Fig. 3.10** displays the TEM pictures of Al/n-Ge and Al/$TiO_2$/n-Ge junction. The thickness of $TiO_2$ was 5~6nm.

### 3.3.2 $N^+P$ Ge Junction Characteristics

The off current and the ideal factor are defined by the characteristics of $n^+p$ junction. Therefore, the current was affected obviously by insertion of $TiO_2$ at high forward voltages. As seen in **Fig. 3.11(a)**, junction with an insertion of $TiO_2$ could degrade the on current duo to the additional resistance. The series resistance was 18.56Ω and6.76Ω, with and without insertion of $TiO_2$ respectively. The additional resistance caused by insertion of $TiO_2$ was almost twice as bigger as the one without $TiO_2$ layer at Al/$n^+$Ge interface, as seen in **Fig. 3.11(b)**

### 3.3.3 Device Characteristics

The serous junction leakage was the critical issue in our samples, which degraded the performance and showed the inferior on/off ratio, as seen in **Fig. 3.12(a).** In the plot of $I_S$-$V_G$, we found that the S.S. was 150mV/decade and the on/off ratio was more than 5 orders for each samples, as seen in **Fig. 3.12(b)**.

The insertion of $TiO_2$ couldn't improve the device performance but also degrade the on current due to the additional resistance, as seen in **Fig. 3.12.** But in long channel device, the channel resistance was so big so that the effect of the additional resistance was lightened. Therefore, the benefit of decreasing the Schottky barrier height by inserting $TiO_2$ layer could be revealed in long channel device, as seen in **Fig. 3.13(a)** and **Fig. 3.13(b).** Finally, we calculated the S/D series resistance by the Terada and Muta method. The equation we used is

$$R_{TOT}=R_{SD}+AL_{eff}=(R_{SD}-A\Delta L)+AL=B+AL \qquad (3.1)$$

By eq. (3.1) we found that the S/D resistance of the sample with $TiO_2$ layer was bigger than one without $TiO_2$ layer, as seen in **Fig. 3.14.**

## 3.4 Conclusions

In Chapter 3, we fabricated the metal S/D p MOSFET, and on/off ratio reached 3orders and subthreshold swing was 306mV/decade. And then, we realized the metal S/D n MOSFET by using $GeO_2$ and $TiO_2$ layer. The sample with $TiO_2$ exhibited better drain current behavior at low drain voltages than one with $GeO_2$, because $TiO_2$ has the smaller conduction band offset than Ge.

Pros and cons of adding the $TiO_2$ layer to conventional Ge n-MOSFETs were discussed according to our experimental data. The insertion of $TiO_2$ interfacial layer at metal/n-Ge interface could reduce the Schottky barrier height but also induce an additional resistance. As the channel length scaling down, the effect of additional resistance will be more serious.

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- Cyclic DHF clean of N-Ge
- 4200 Å $SiO_2$ isolation layer
- 1st litho. : AA region define
- 2nd litho. : define S/D metal pad by lift-off Pt 50nm
- 500°C 10s $GeO_2$ passivation
- 80 cycles ALD $Al_2O_3$
- Al deposition
- 3th litho. : define metal pad
- Backside contact (Al)

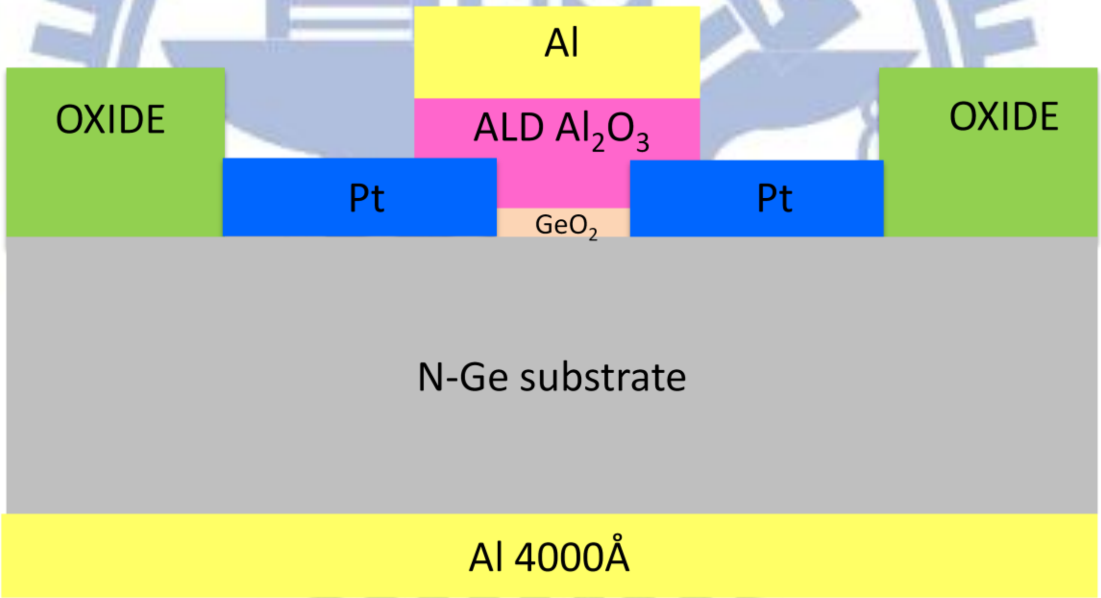
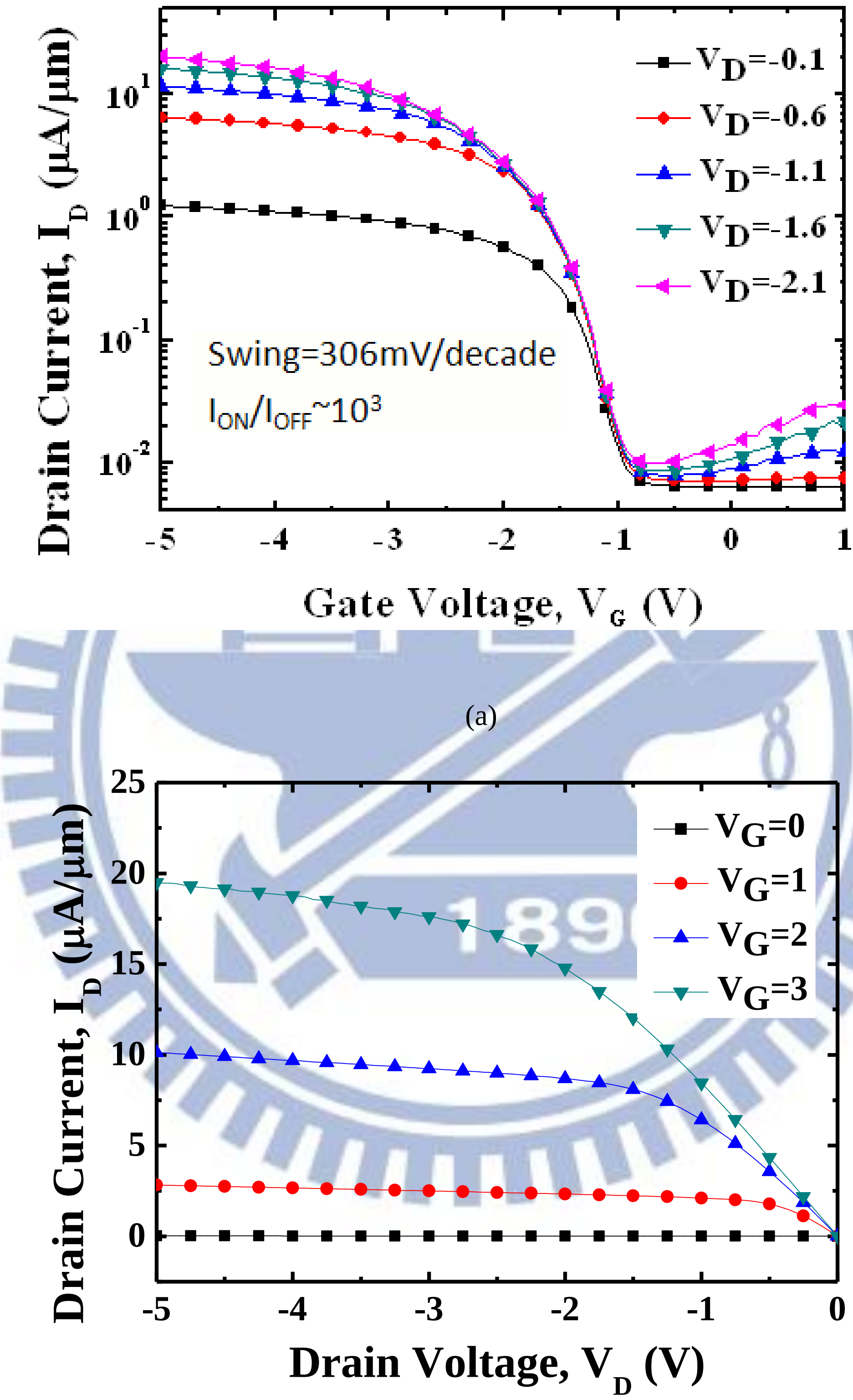


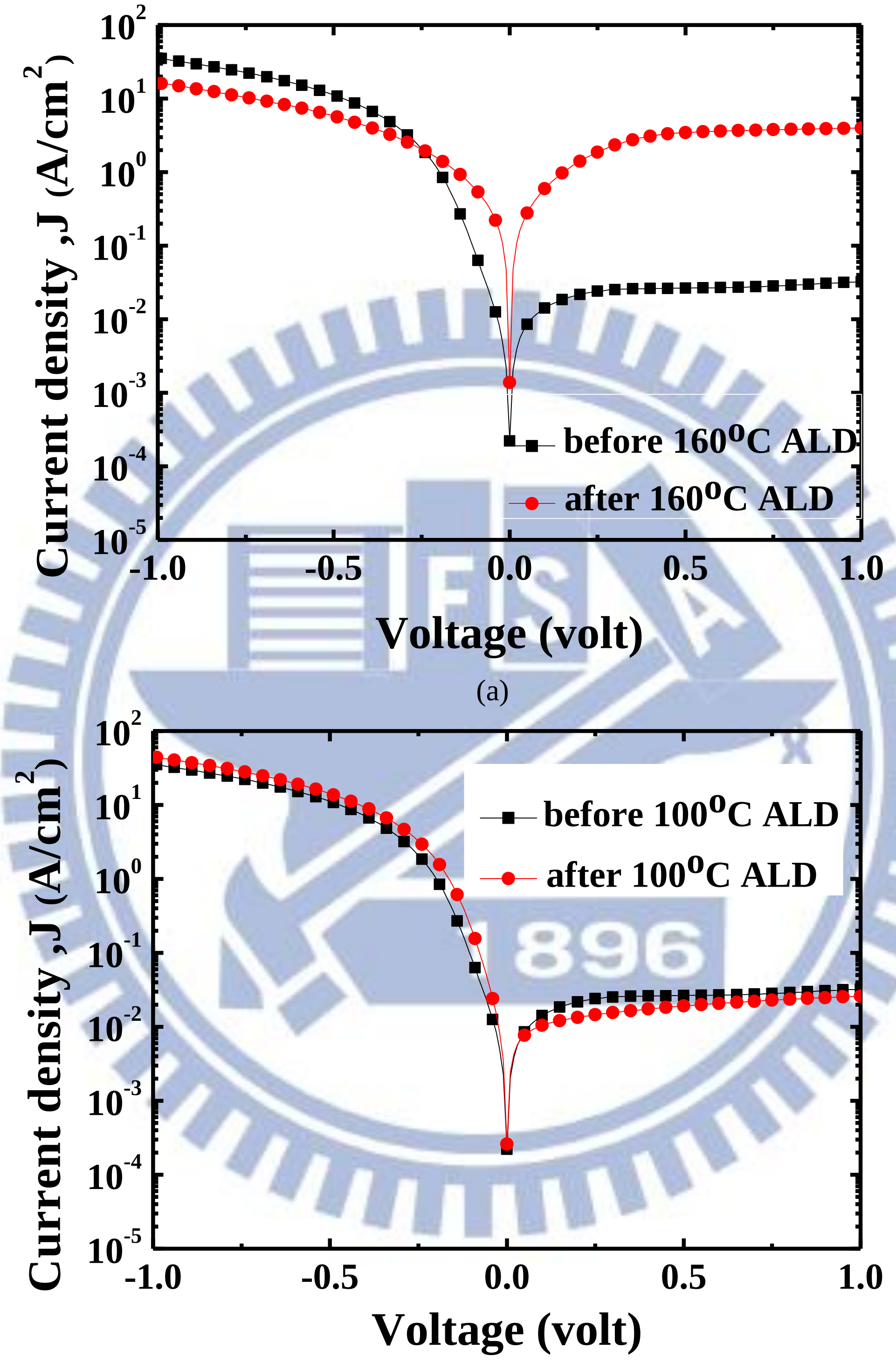
Fig. 3.1. Process flow of Ge metal S/D p-MOSFET and their device structure.



(a)

(b)

Fig. 3.2. (a) $I_D$-$V_G$ and (b) $I_D$-$V_D$ characteristic of Ge metal S/D p-MOSFET.(W/L=100μm/5μm)



(a)

(b)

Fig. 3.3. I-V characteristics of Al/$TiO_2$/p-Ge junction before and after the thermal budget from ALD. (a)ALD at 160 ℃. (b) ALD at100 ℃.

- Cyclic DHF clean of P-Ge
- 4200 Å $SiO_2$ isolation layer
- 1st litho. : AA region define
- Depinning layer formation($GeO_2$, $TiO_2$ )
- Al deposition
- 2nd litho. : define S/D metal pad
- 80 cycles ALD $Al_2O_3$
- Al deposition
- 3th litho. : define gate metal pad
- Backside contact (Al)

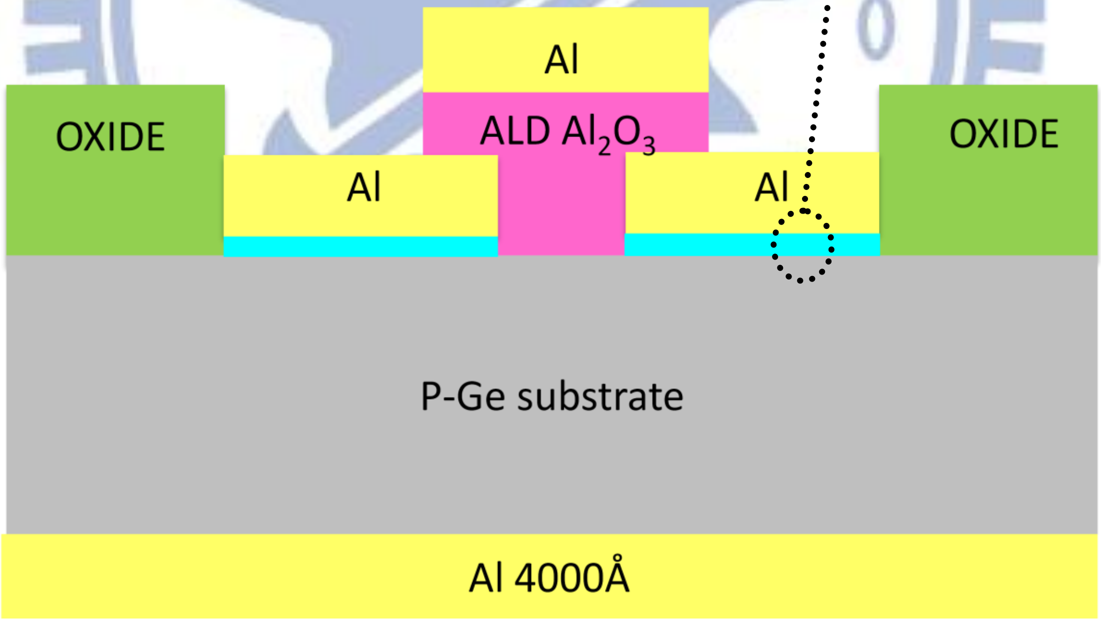
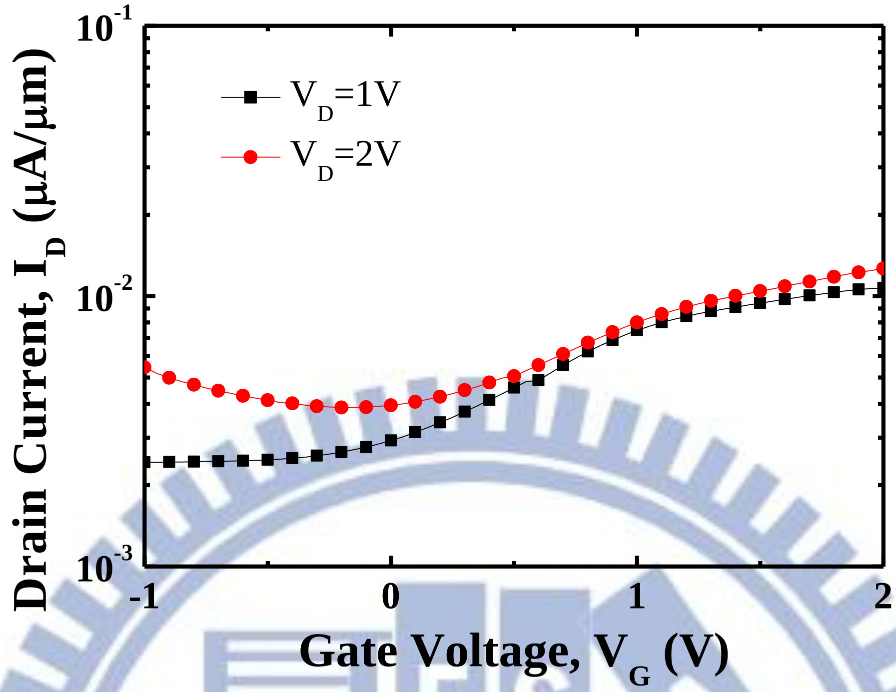
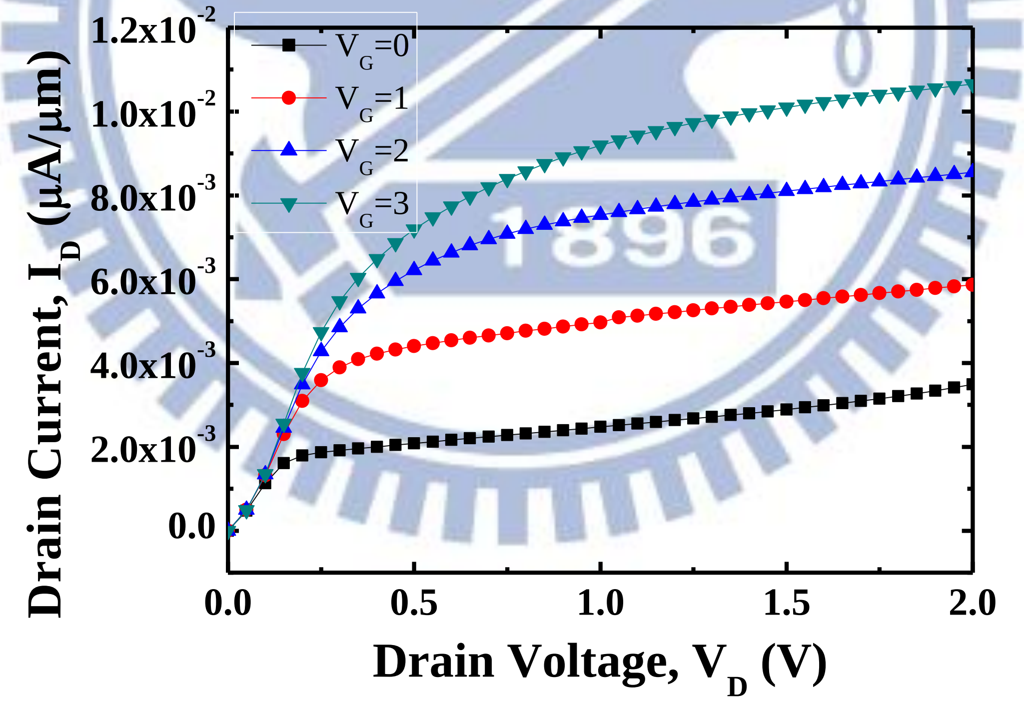


Fig. 3.4. Process flow of Ge metal S/D n-MOSFET and their device structure.

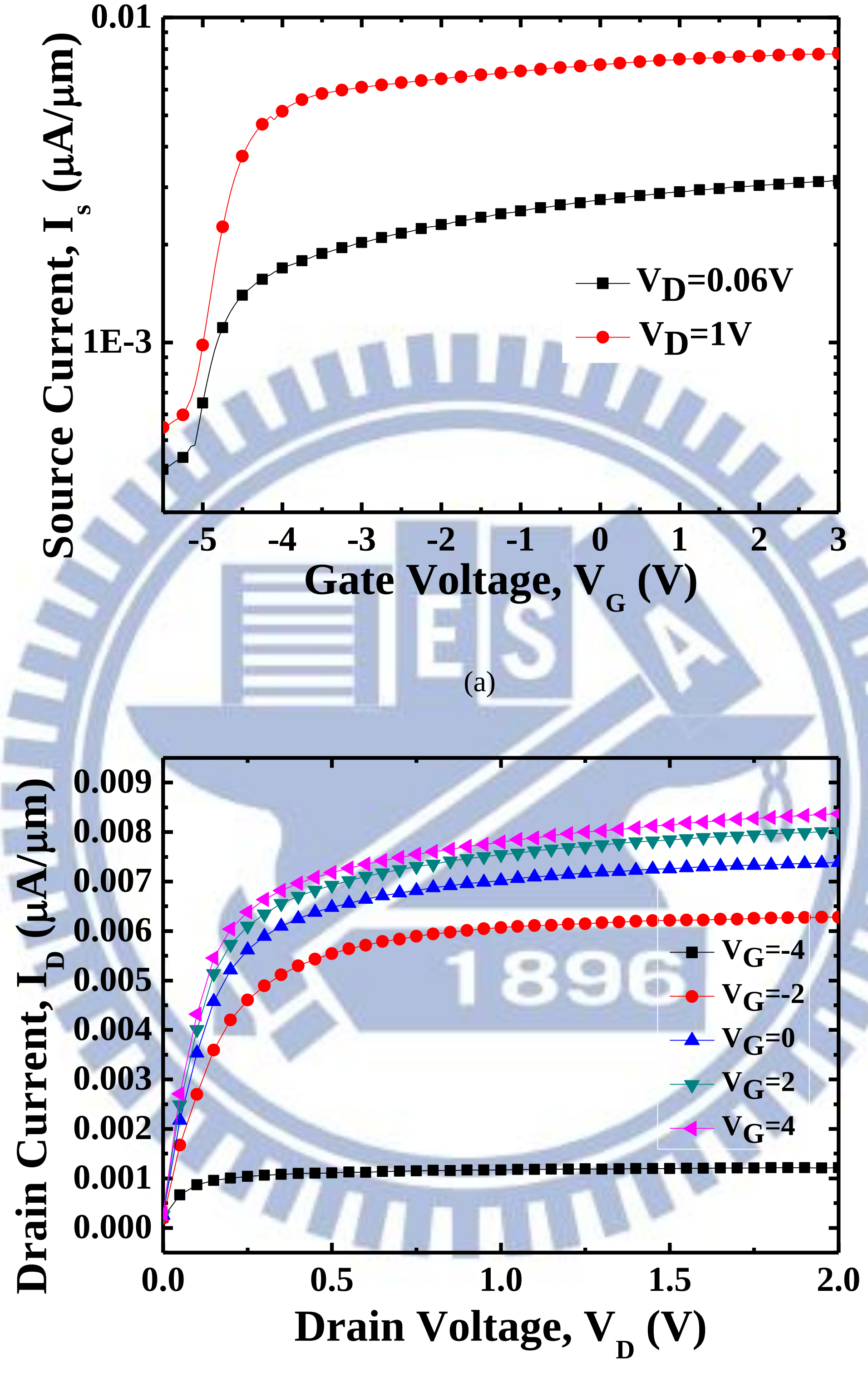


(a)



(b)

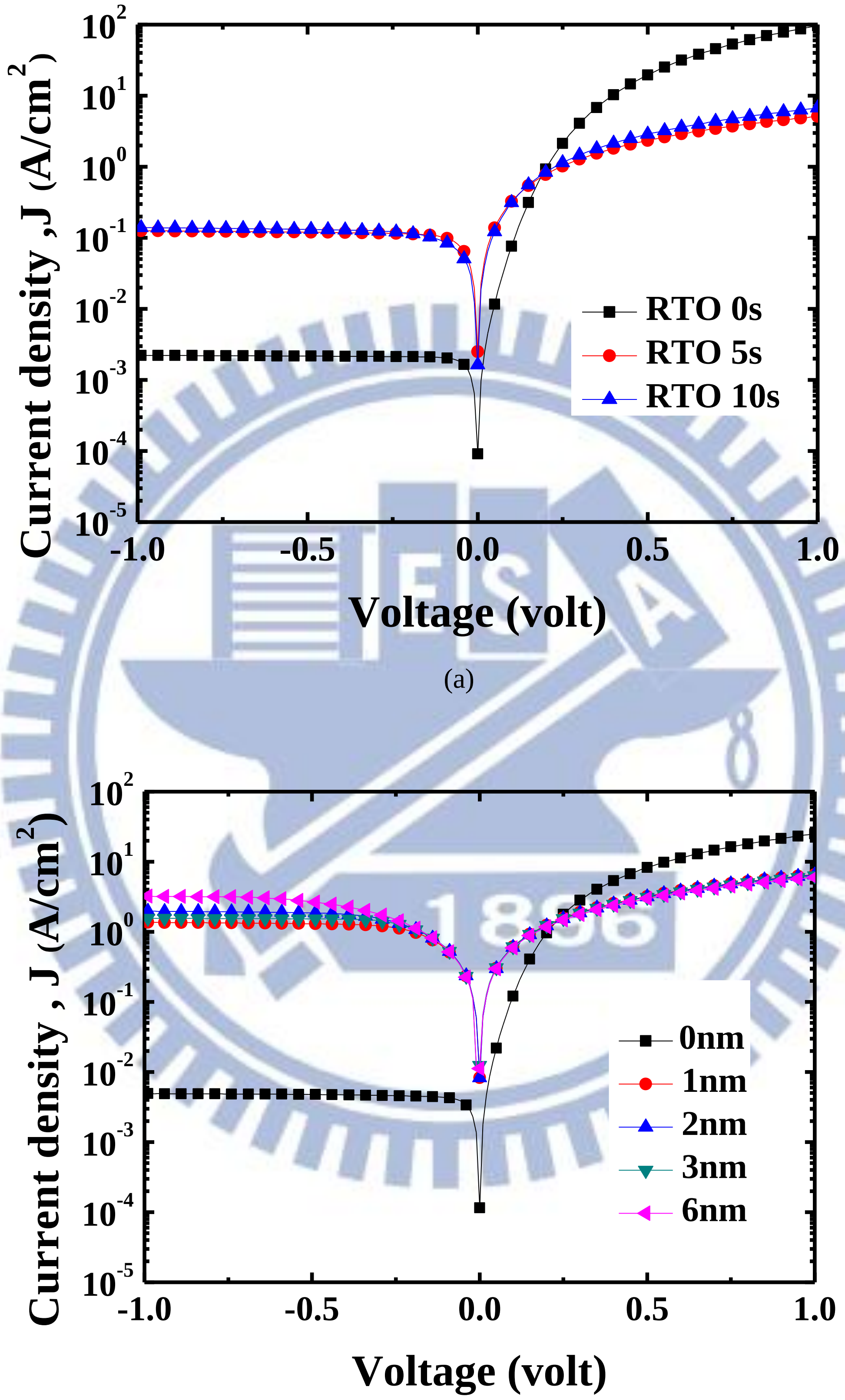
Fig. 3.5. (a) $I_S$-$V_G$ and (b) $I_D$-$V_D$ characteristic of Ge metal S/D n-MOSFET with 500°C 10s $GeO_2$ depinning layer. (W/L=100μm/5μm)



(a)

(b)

Fig. 3.6. (a) $I_S$-$V_G$ and (b) $I_D$-$V_D$ characteristic of Ge metal S/D p-MOSFET with 6nm $TiO_2$ depinning layer. (W/L=100μm/5μm)



(a)

(b)

Fig. 3.7. I-V characteristics of (a) Al/GeO2/n-Ge and (b) Ti/TiO2/n-Ge junction. GeO2 layer was formed by RTO, and TiO2 layer was formed by ALD.

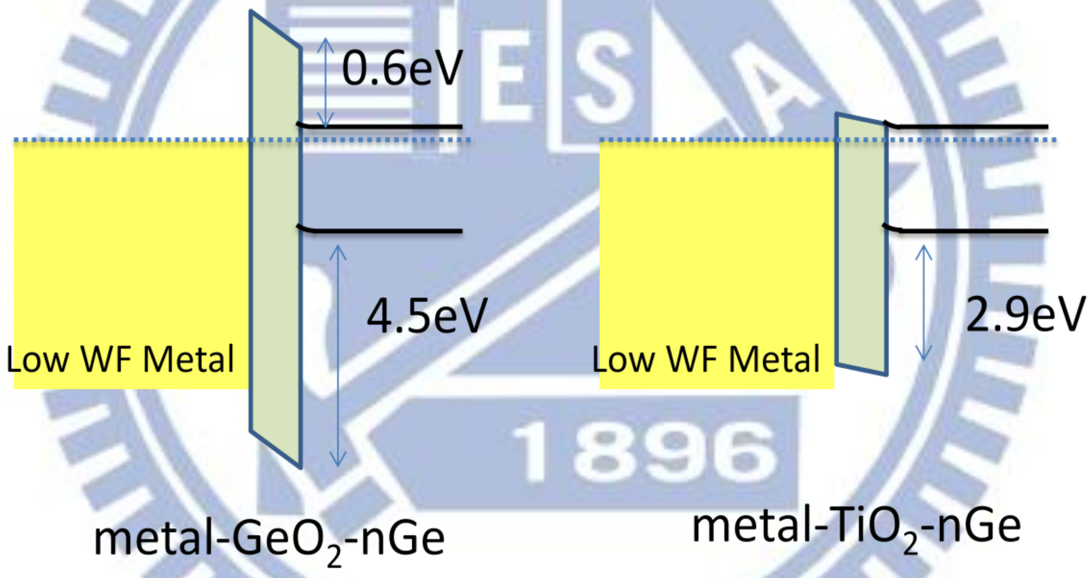
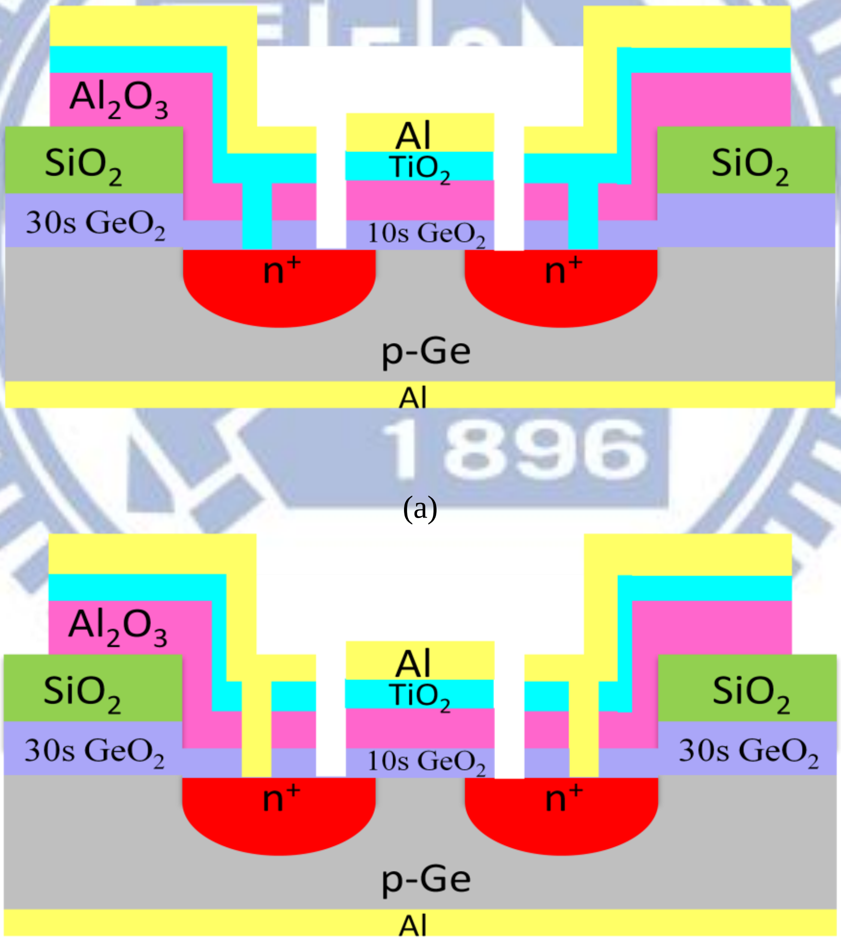


Fig. 3.8. Band structure of metal/GeO$_2$/n-Ge junction and metal/TiO$_2$/n-Ge.

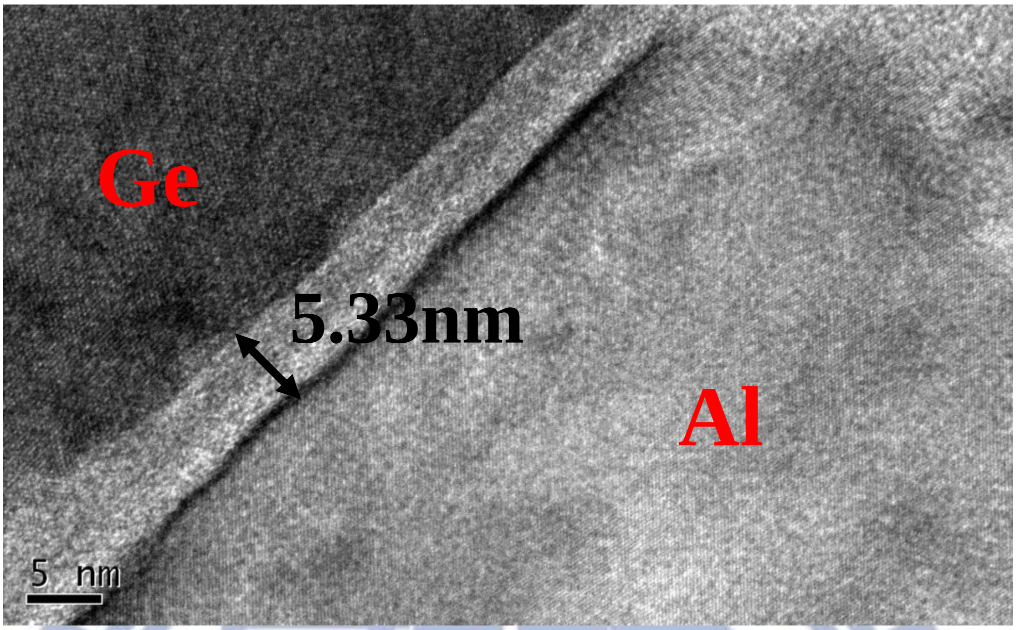
- Cyclic DHF clean of P-Ge
- (500°C 30s $GeO_2$) + $SiO_2$ isolation layer
- 1st litho. and P imp.(20keV, 1×15cm$^{-2}$)
- Dopant activation (600°C 10s)
- 2nd litho. : define AA
- $GeO_2$ passivation (500°C 10s)
- 80 cycles ALD $Al_2O_3$
- 3rd litho. : define contact hole before or after ALD $TiO_2$ 6nm
- Al deposition
- 4th litho. : define metal pad
- Etching $TiO_2$ for isolation by BOE
- Backside contact (Al)



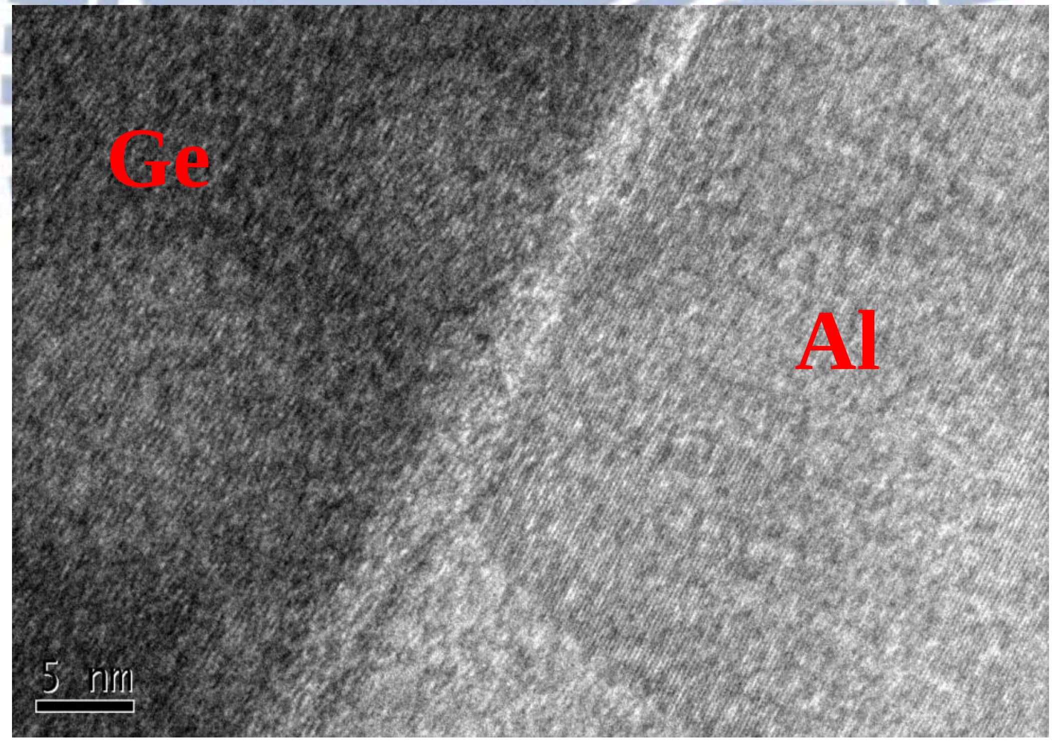
(a)

(b)

Fig. 3.9. Process flow and device structure of Ge n-MOSFET (a) with and (b) without 6nm $TiO_2$ layer at metal/$n^+$Ge interface.

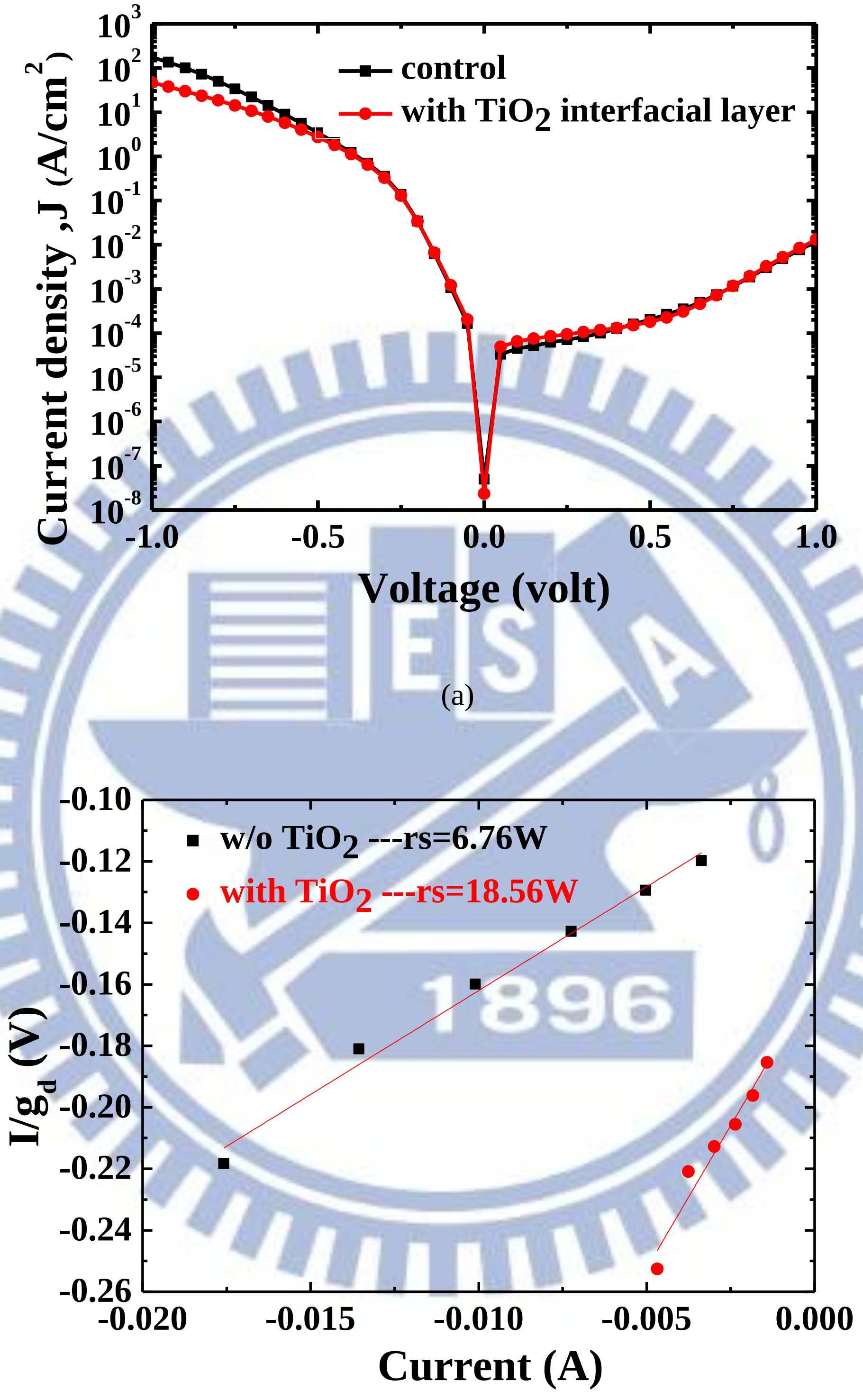


(a)



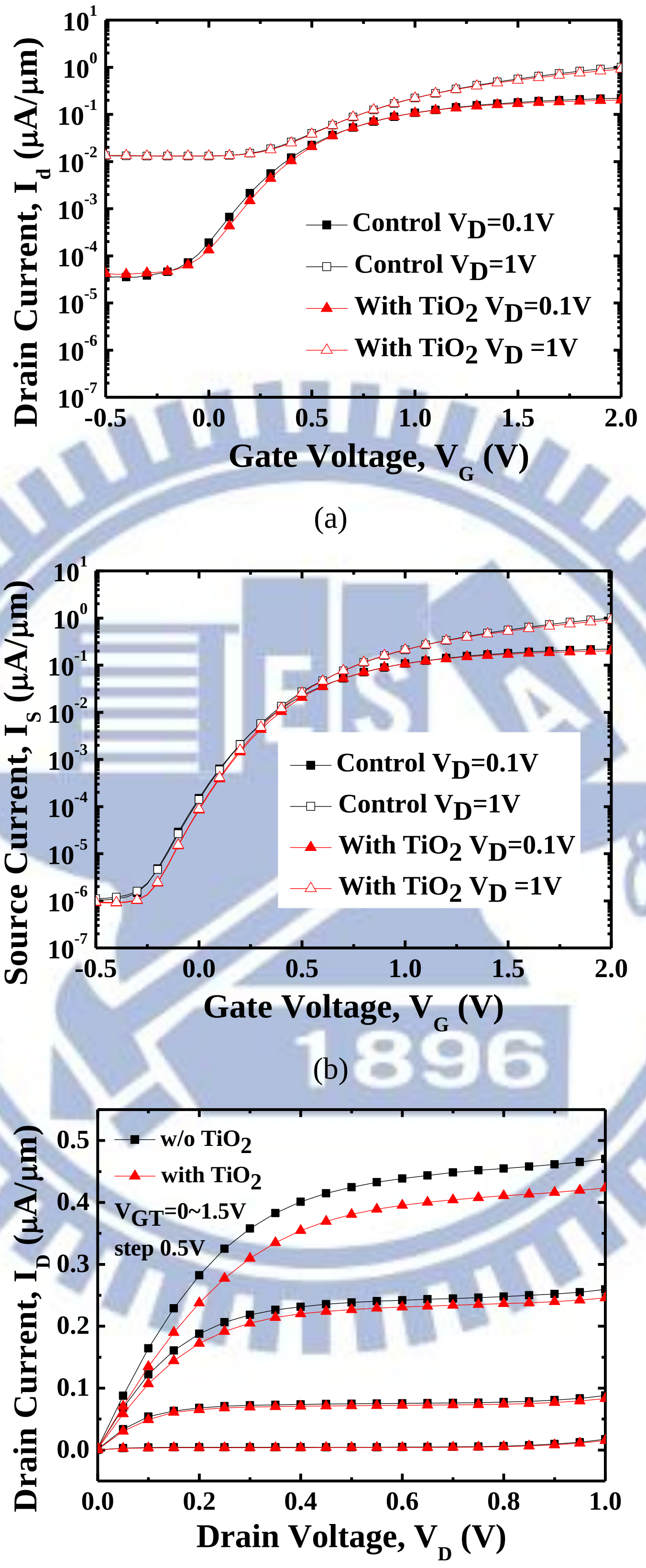
(b)

Fig. 3.10. TEM of junction (a) with (b) without 6nm $TiO_2$ layer at metal/$n^+$Ge interface.



(b)

Fig. 3.11. I-V characteristics and series resistance extraction of $n^+/p$ junctions with and without 6nm $TiO_2$ layer at metal/$n^+$Ge interface. (a) I-V characteristics(b) series resistance extraction.

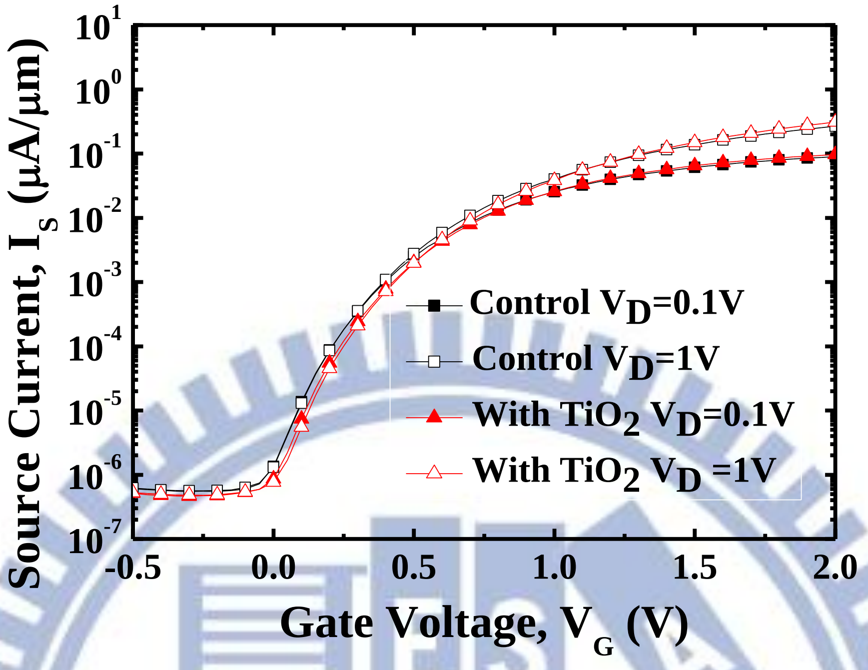


(a)

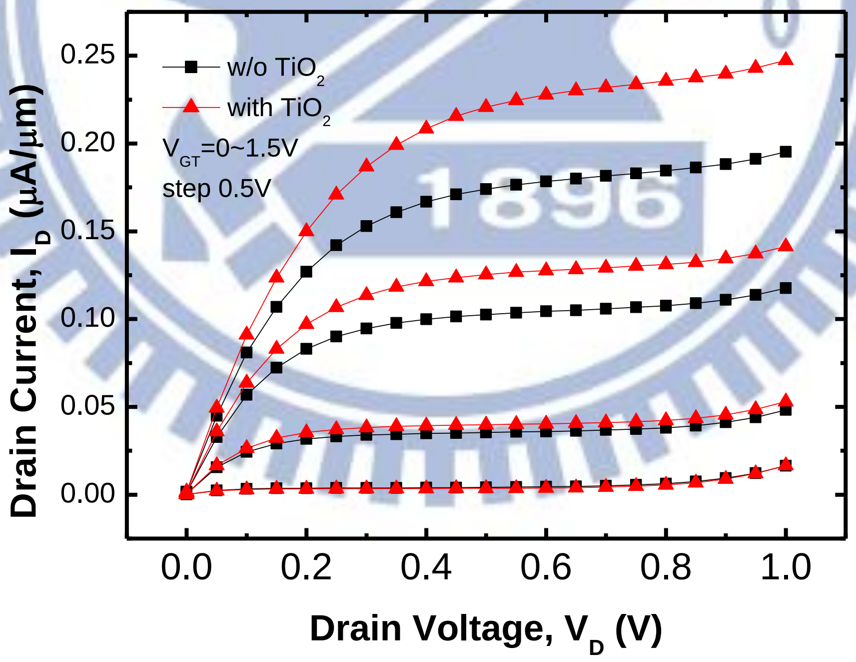
(b)

(c)

Fig. 3.12. (a) $I_D$-$V_G$ and (b) $I_S$-$V_G$ and (c) $I_D$-$V_D$ characteristics of Ge n-MOSFET with and without 6nm $TiO_2$ depinning layer. (W/L=100μm/4μm)

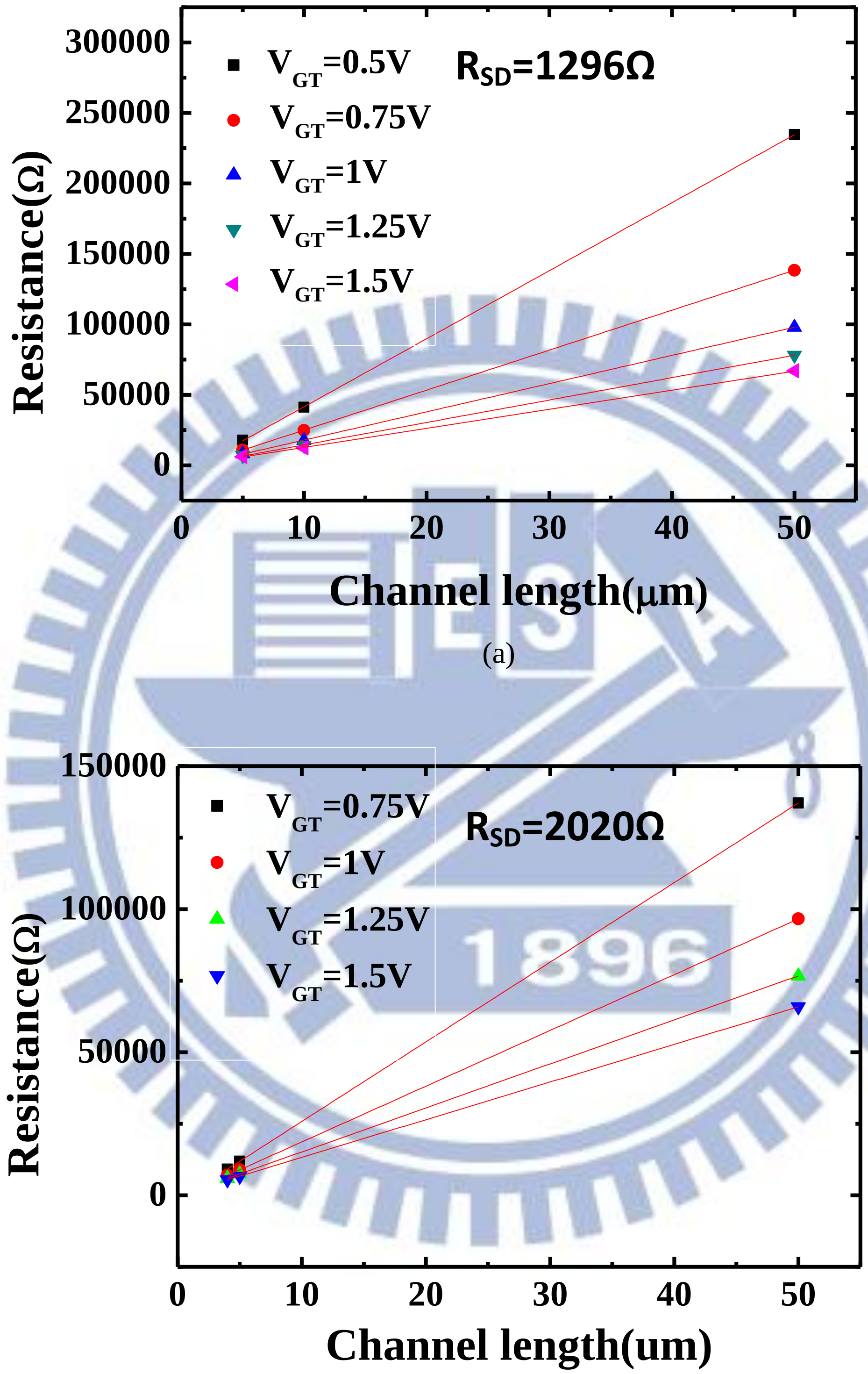


(a)



(b)

Fig. 3.13. (a) $I_D$-$V_G$ and (b) $I_S$-$V_G$ and (c) $I_D$-$V_D$ characteristics of Ge n-MOSFET with and without 6nm $TiO_2$ depinning layer. (W/L=100μm/10μm)



(a)

(b)

Fig. 3.14. Series resistance extraction from Terada and Muta method. (a) no $TiO_2$ interfacial layer. (b) with $TiO_2$ interfacial layer.

# Chapter 4

# Research of $n^+$/p Junction for High-performance Short-channel Germanium n-MOSFETs

## 4.1 Introduction

As the semiconductor industry has entered the era of material-limited device scaling [1], people are looking for new channel material to boost the device performance. Ge is an attractive material for future semiconductor devices due to its higher electron and hole mobility compared to Si. Recently, Ge p-MOSFET with mobility 3X higher than Si universal curve has been reported [2], but the Ge n-MOSFET still exhibits the unsatisfactory performance due to the high interface density of state ($D_{it}$) and the poor $n^+$/p junctions. Although several promising passivation schemes using $GeO_2$-based gate dielectrics have been reported with low $D_{it}$ recently [3-5], the $n^+$/p junctions still suffer from the low activation and fast diffusion rate of n-type dopants in Ge. Therefore, shallow junction is hard to be achieved for short channel device [6].

In this chapter, effects of implant dose and activation temperature on junction are discussed. Next, medium dosage of phosphorous was adopted to form $n^+$/p junction for short-channel device. Finally, the 500nm gate-length Ge n-MOSFETs with high $I_{on}/I_{off}$ ratio and excellent subthreshold swing (S.S) were achieved.

## 4.2 $N^+$/P Ge Junction Characteristics

### 4.2.1 Fabrication of $N^+$/P Junction

(100)-oriented p-Ge substrate doped with Ga at level of 2E17cm$^{-3}$ (resistivity ca.

$0.02\Omega \cdot \mathrm{cm}$) was used for $n^+$/p junction fabrication. All of the samples were pre-cleaned by successive diluted HF (20:1) and DI water rinsing to remove the native oxide. Then, a $GeO_2$ layer was formed by RTO at 500 ℃ 30s before a 420-nm-thick $SiO_2$ layer capped for the field oxide by PECVD.

First, the (source/drain) region was opened through the 1st Mask, followed by implantation of the P with conditions ($1 \times 10^{15}\mathrm{cm}^{-2}$, 20keV) ($2 \times 10^{14}\mathrm{cm}^{-2}$, 20keV) into the p-Ge, and the wafers were split into two conditions: 600 ℃, 30s and 500 ℃, 30s as the activation condition. Next, right after excavating the contact hole through the 2nd Mask, a 400nm Al metallization was performed which was then patterned to define metal pads through the 3rd Mask. Finally, a 400nm Al layer was deposited as the backside contact.

The process flow and device structure are shown in **Fig. 4.1**

### 4.2.2 Results and Discussion

**Fig. 4.2(a) and Fig. 4.2(b)** displays the effects of different activation temperature on junctions at the dose of $1 \times 10^{15}\mathrm{cm}^{-2}$ and $2 \times 10^{14}\mathrm{cm}^{-2}$ respectively. The difference between different implant dosages was invisible through I-V plot of junctions. Previous studies of P ion implantation into Ge, have revealed that an RTA temperature above 500 ℃ is necessary to produce sufficient dopant activation [7-8]. In this study, although we found that an annealing temperature of 500 ℃ was in sufficient to repair all of the implant-induced damage, but the acceptable $I_{on}/I_{off}$ (4.2 orders) was achieved. Raising the temperature to 600 ℃ could decrease the value of $J_R$ and ideal factor, but also made the junction depth deeper than one of 500 ℃ annealing, as seen in **Fig. 4.3.** The dopant distribution was almost unchanged after annealing at 500 ℃, which was suitable for short channel device.

After annealing at 600 ℃, the dose loss and the increase of junction depth were more severe at the dose of $1 \times 10^{15}\mathrm{cm}^{-2}$ than one at the dose of $2 \times 10^{14}\mathrm{cm}^{-2}$ due to the concentration-enhanced diffusion [9]. Even in the condition of 500 ℃, the $2 \times 10^{14}\mathrm{cm}^{-2}$ dosage sample exhibited the higher $I_{on}/I_{off}$ ($1.61 \times 10^4 > 1.34 \times 10^4$) and smaller ideal factor ($1.49 < 1.56$) factor than the $1 \times 10^{15}\mathrm{cm}^{-2}$ dosage sample. The results imply that overdose dopants in Ge will cause deeper junction depth and degrade the performance.

Therefore, the dose of $2 \times 10^{14}\mathrm{cm}^{-2}$ and the 500 ℃ 30s annealing were used for the fabrication of short channel Ge n-MOSFET.

## 4.3 Ge n-MOSFET with Gate Length-500nm

### 4.3.1 Fabrication of Gate -First Ge n-MOSFET

(100)-oriented p-Ge substrates with resistivity of 1.6-2.1 $\Omega \cdot \mathrm{cm}$ were used for self-aligned gate-first n-MOSFETs fabrication. First, Boron was implanted into Ge and annealed to provide well doping of $\sim 5 \times 10^{17}\mathrm{cm}^{-3}$.

All of the samples were cleaned by diluted HF to remove native oxide, followed by 500 ℃ 3min $GeO_2$ passivation layer, and then an 80 cycles ALD-$Al_2O_3$ was deposited as the high-k gate dielectric. A TiN layer was deposited by PVD and patterned as gate using lithography and dry etching. Next, Phosphorus was implanted at dose of $2 \times 10^{14}\mathrm{cm}^{-2}$ at 20keV as source and drain, while dopant activation condition was 500 ℃ in $N_2$ ambient for 30sec. Finally, a TiN layer was deposited as the backside contact.

The process flow and device structure are shown in **Fig. 4.4.**

### 4.3.2 Results and Discussion

Device characteristics of Ge n-MOSFET are shown in **Fig. 4.5(a)** and **Fig. 4.5(b).** The $I_{on}/I_{off}$ ration was about $1.67 \times 10^5$ for source current ($I_S$) and $1 \times 10^4$ for drain current ($I_D$) at $V_D$=0.05V. With $GeO_2$ passivation layer, the subthreshold swing (S.S) can be improved by reduced density states at interface. In this work, low S.S value of ~100mV/decade was achieved and there is no significant difference between S.S ($I_D$) and S.S ($I_G$).

By medium implantation dosage ($2 \times 10^{14}$cm$^{-2}$), high performance short channel (gate lengeth=500nm) Ge n-MOSFET was demonstrated without serious drain induced barrier lowering (DIBL).

## 4.4 Conclusions

In Chapter 4, we investigated the characteristics of Ge $n^+/p$ junction with different implantation dosage and activation temperature. It was concluded that medium implantation dosage ($2 \times 10^{14}$cm$^{-2}$) enable us to obtain the shallow junction and suppress the effect of concentration-enhanced diffusion. An annealing temperature of 500 ℃ was suitable for our fabrication of n-MOSFET due to the shallower junction depth than one of 600 ℃.

Finally, the 500nm Gate-length n-MOSFET was achieved with high $I_{on}/I_{off}$ ration ($1.67 \times 10^5$ for $I_S$), low S.S (~100mV/decade), and no obvious DIBL.

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- Cyclic DHF clean of P-Ge
- (500°C 30s $GeO_2$) + $SiO_2$ isolation layer
- 1st litho. and P imp.(20keV, $1\times15cm^{-2}$)
- Dopant activation (600°C 10s)
- 2nd litho. : define AA
- $GeO_2$ passivation (500°C 10s)
- 80 cycles ALD $Al_2O_3$
- 3rd litho. : define contact hole before or after ALD $TiO_2$ 6nm
- Al deposition
- 4th litho. : define metal pad
- Etching $TiO_2$ for isolation by BOE
- Backside contact (Al)

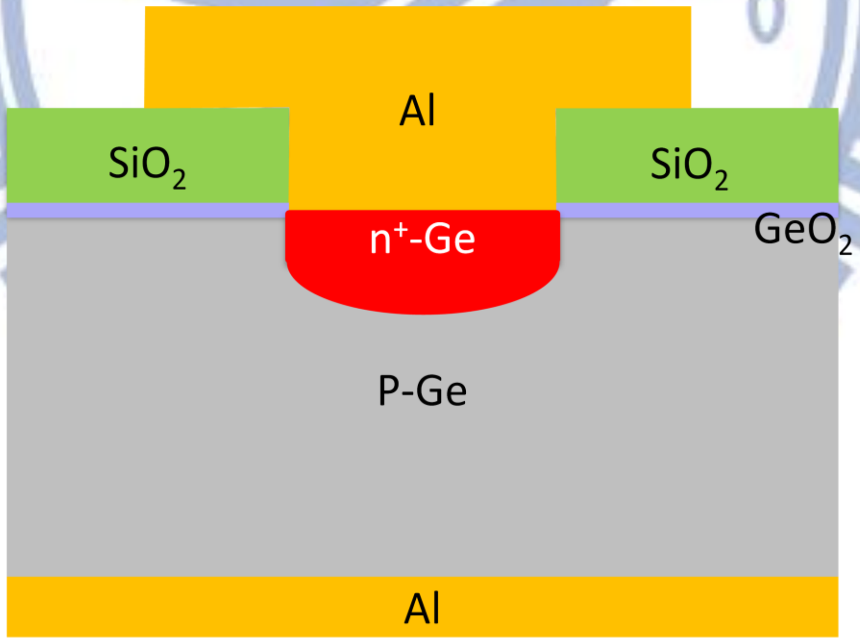
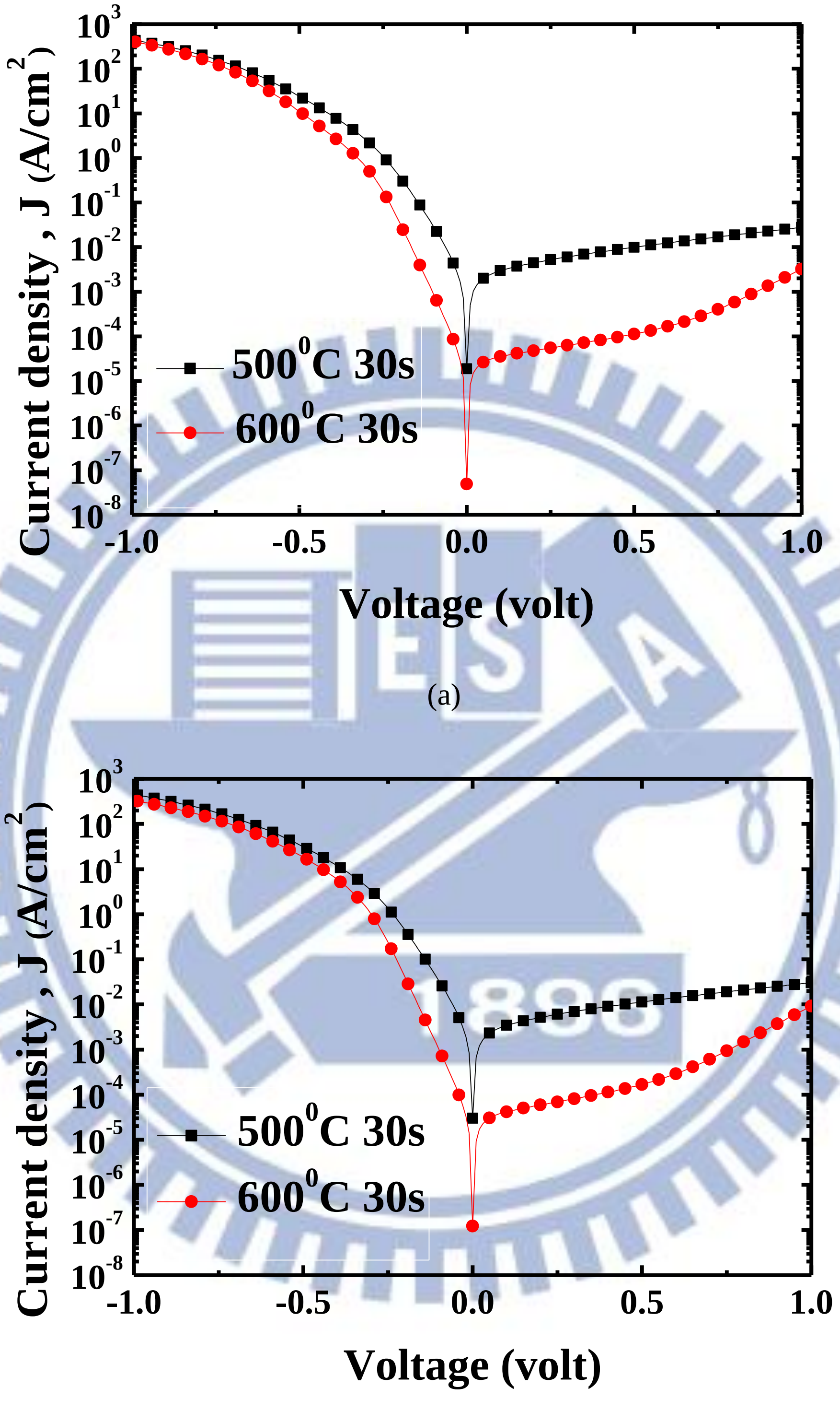


Fig. 4.1. Process flow of Ge $n^+/p$ junctions and their device structure.



(a)

(b)

Fig. 4.2. I-V characteristics of $n^+/p$ junctions activated at 500 ℃ and 600 ℃. (a) implant dose $2 \times 10^{14}\text{cm}^{-2}$ (b) implant dose $1 \times 10^{15}\text{cm}^{-2}$

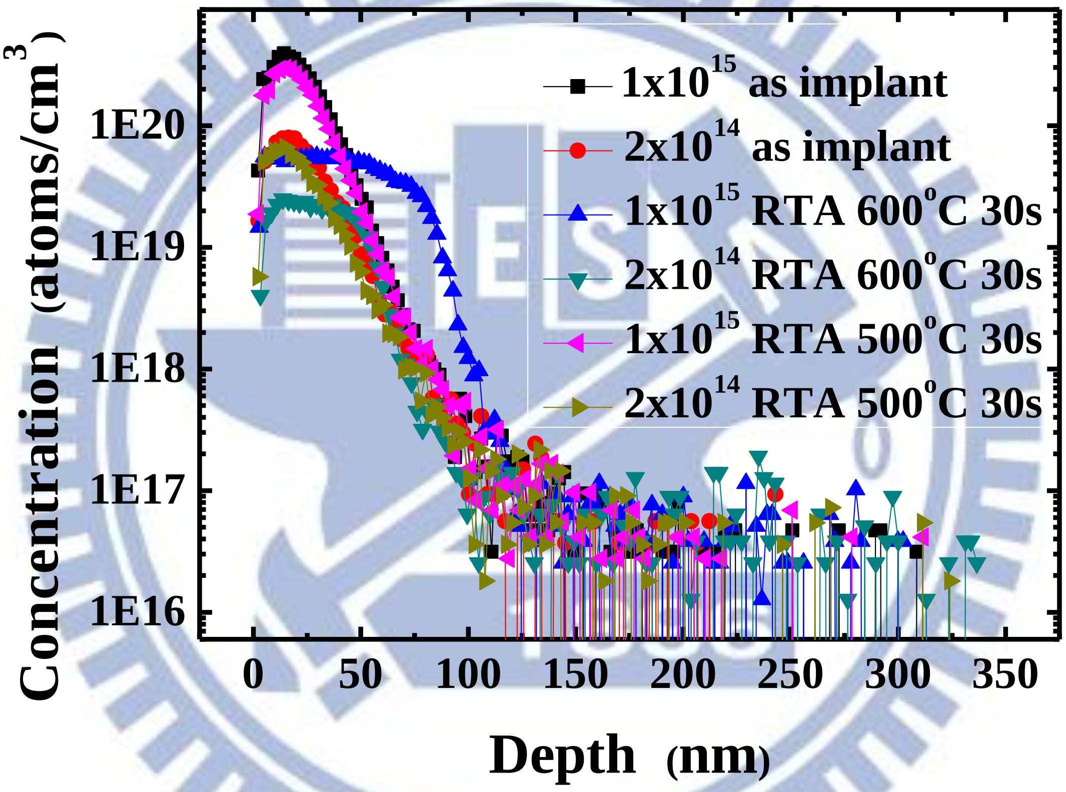
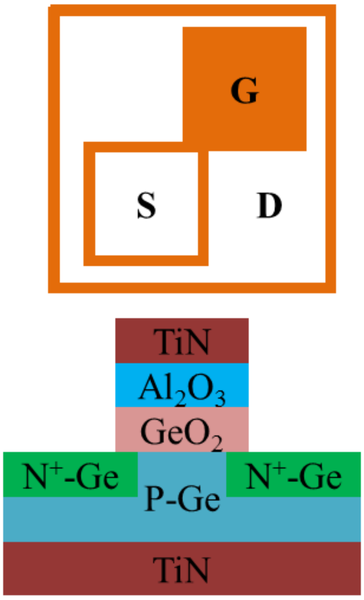
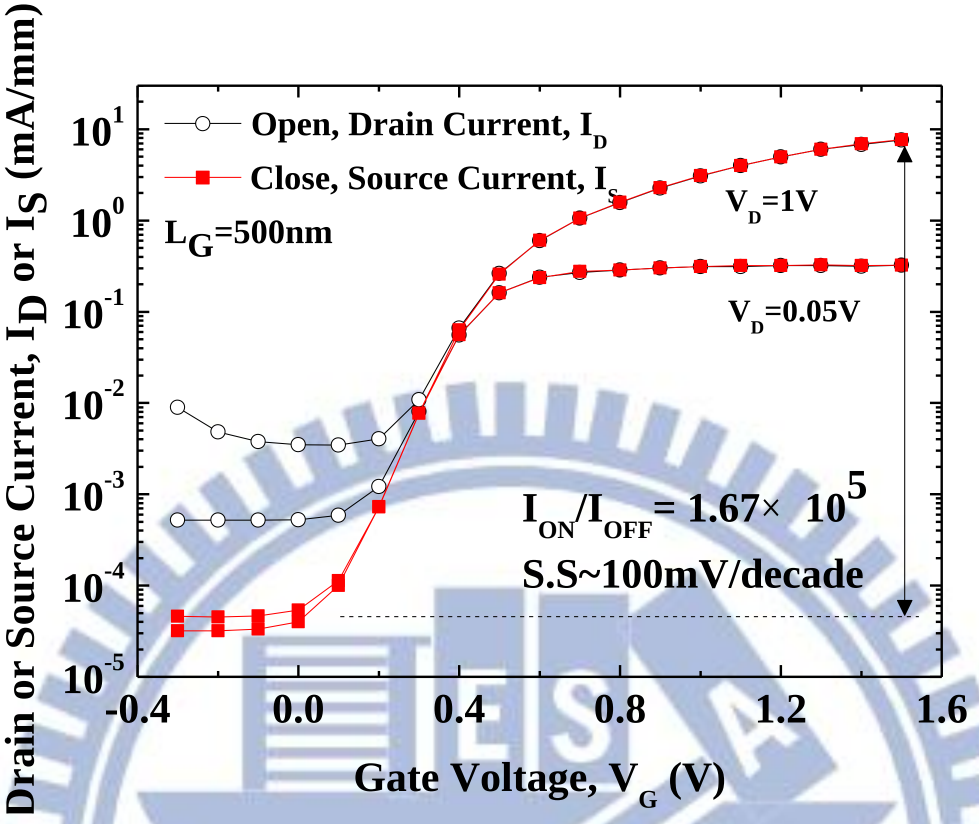


Fig. 4.3. SIMS profile of P with different dosage after RTA at varying temperature of 500 ℃-600 ℃

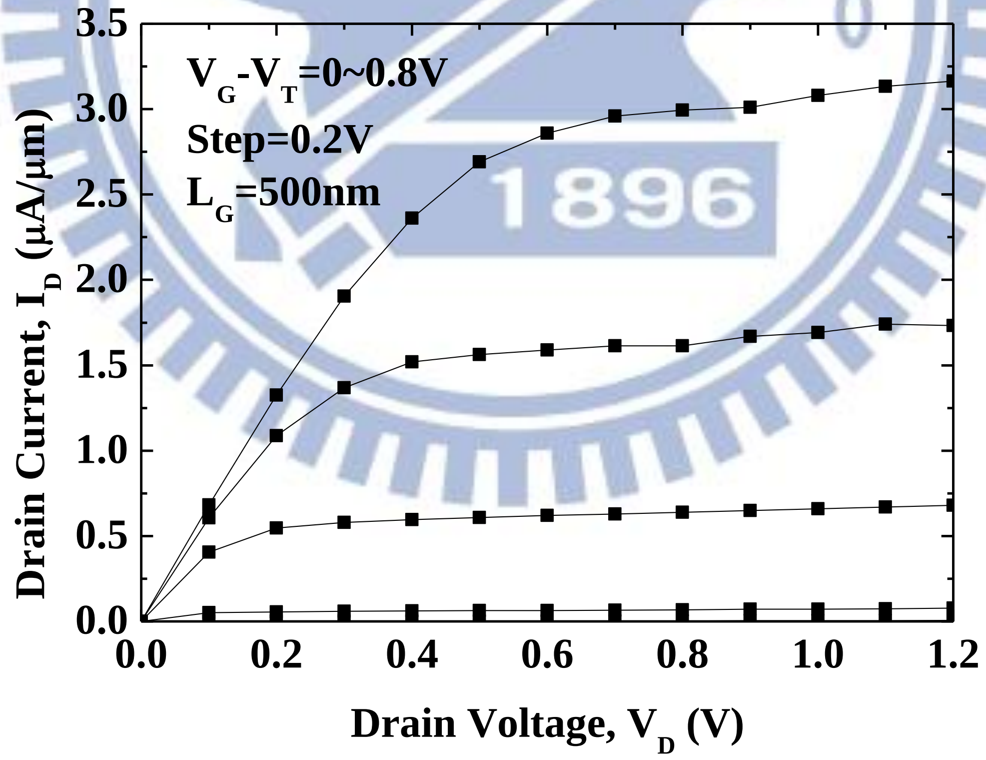


- $B^{11+}$ implant ~5×$10^{17}$ $cm^{-3}$ for well doping
- Activation, 520˚C, 20min
- $GeO_2$ growth, 550˚C, 3min, $O_2$ ambient
- ALD $Al_2O_3$, 160˚C, 80 cycle
- TiN Gate, 75nm
- Gate Lithography
- Dry etching
- $P^{31+}$, 20keV, 2×$10^{14}$ $cm^{-2}$
- Activation, 500˚C, 30sec
- TiN Contact, Backside

Fig. 4.4. Process flow of Ge n-MOSFETs and their device structure. One-mask process was used in this work. The channel length was 500nm.



(a)



(b)

Fig. 4.5. (a) $I_D$-$V_G$ and (b) $I_D$-$V_D$ characteristic of Ge n-MOSFET. The channel length was 500nm and implantation dosage was $2\times10^{14}$ cm$^{-2}$.

# Chapter 5

# Conclusions

## 5.1 Conclusions

In this thesis, firstly, we release the FLP both on n and p type Ge by inserting the interfacial layer of $GeO_2$ and $Al_2O_3$ successfully, and make the high SHB for hole in p-Ge case. The pinning factor of $GeO_2$ case is 0.41 for p-Ge and 0.59 for n-Ge, while in $Al_2O_3$ case the pinning factor is 0.347 for p-Ge and 0.495 for n-Ge. The effect of de-pinning by using $GeO_2$ is better than one by using $Al_2O_3$, which resulting from the better quality of $GeO_2$/Ge interface. By applying $TiO_2$ as the interfacial layer to different metal contacts, we find that the reason of I-V characteristic changing from rectifying to ohmic by insertion of $TiO_2$ layer is due to the n type semiconductor-like characteristics of $TiO_2$.

Secondly, basing on the experiences in de-pinned junctions, we successively demonstrated the device characteristics of the metal S/D Ge n-MOSFETs with $GeO_2$ and $TiO_2$ as depinning layer. Compared to $GeO_2$, the smaller conduction band offset of $TiO_2$ lead to the better drain current characteristic at low drain voltages. Furthermore, pros and cons of adding the $TiO_2$ interfacial layer to conventional Ge n-MOSFETs have been discussed according to our experimental data. The insertion of $TiO_2$ layer at metal/n-Ge interface cannot only reduce the Schottky barrier height but also induce an additional resistance. As the channel length scaling down, the effect of additional resistance will be more serious.

Finally, we investigated the characteristics of Ge $n^+$/p junction with different implantation dosages and activation temperatures. It is concluded that medium implantation dosage ($2 \times 10^{14} \mathrm{cm}^{-2}$) enables us to obtain the shallow junction and suppress the effect of concentration-enhanced diffusion. Furthermore, an annealing temperature of 500 ℃ is suitable for our fabrication of n-MOSFET due to the shallower junction depth than one of 600 ℃. According to the experiences in $n^+/p$ junctions, the 500nm Gate-length n-MOSFET was achieved with high $I_{on}/I_{off}$ ration ($1.67\times10^{5}$ for $I_S$), low S.S (~100mV/decade), and no obvious DIBL.

# 簡 歷

姓 名:**陳韋志**

性 別:**男**

出生年月日:**民國 75 年 11 月 12 日**

籍 貫:**台灣省彰化縣**

住 址:**彰化縣埔鹽鄉永平村番金路 126 號**

學 歷:

**國立彰化師範大學電機工程學系（94.09~98.06）**

**國立交通大學電子研究所碩士班（98.09 ~ 101.06）**

碩士論文題目:

**在鍺通道金氧半場效電晶體上**

**去釘札後蕭特基二極體以及 $n^+$/p 二極體的研究**

**Investigation of the Depinning Schottky Junction and $n^+$/p Junction on Ge-Channel MOSFETs**