國立交通大學

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碩士論文

高介電金屬閘金氧半場效電晶體之隨機擾動電子訊號：實驗、建模與TCAD模擬

HKMG MOSFET Random Telegraph Signals (RTS): Experiment, Modeling, and TCAD Simulation

研 究 生：林煜翔

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摘要

在體積更小、更快、更省電等等便利性和經濟性的訴求下，電子元件尺寸的微縮便成為了未來的趨勢。而隨著電子元件尺寸的微縮，奈米尺度的隨機擾動電子訊號(RTS, Random Telegraph Signals)也因而越來越不可忽視。因此，研究小尺寸元件中 RTS 對元件電性所帶來的影響便成為了一門重要的課題。RTS 現象的發生普遍認為是載子被氧化層中的缺陷重複進行捕捉-釋放的過程。當載子被捕捉時，被捕捉的載子會在氧化層中產生一股額外的屏蔽庫侖電位，它將影響到通道中的載子，使得汲極／源極的電流大小隨著捕捉-釋放的過程而在兩個階段間波動。在實驗中，我們較不容易觀察到汲極／源極的電流變化量和這些可能影響 RTS 的參數之間的關係。其中一個理由是，我們無法自由地改變實際的元件的各項參數以改變其物理特性，而另一個理由則是，我們難以在一片晶片上找到足夠多具有 RTS 現象的

元件。然而， TCAD 模擬使得我們能夠解決這些問題。在 TCAD 模擬中，我們可以藉由設定我們所需要的參數，像是閘極長度、閘極寬度、摻雜濃度等等來控制元件的特性，並且可以插入一個缺陷到矽氧化層中以確保此結構具有 RTS 的現象。

本篇論文的主要目標是建立一個新穎的 RTS 物理模型。而在建立模型之前，我們須先量測實際的實驗數據，再佐以 TCAD 的模擬來了解 RTS 的各種特性。首先，藉由 TCAD 的模擬，我們調整了 MOSFET 尺寸的大小、trap 的大小、以及 trap 的位置。經由比較汲極／源極電流變化量和各種參數間的變化關係，我們能夠得出隨參數變化而導致的電流變化趨勢：(1)汲極電流變化率會隨著元件尺寸的漸小而漸增;(2) 汲極電流變化率的曲線圖上會有一個最大值同時也是曲線的轉折點，而此轉折點的轉折程度會隨著元件尺寸的漸小而逐漸變得劇烈；(3)當兩個元件有同樣閘極寬度時，汲極電流變化率曲線在次臨界電壓區域時的斜率也會一樣；(4)缺陷在閘極正中央的汲極／源極電流會比缺陷在閘極邊緣的汲極／源極電流來得小；(5)缺陷靠近源極的汲極／源極電流會比缺陷靠近汲極的汲極／源極電流來得小。

接下來在分析過模擬結果之後，我們假設當元件在次臨界電壓時，於相同的閘極偏壓下，汲極電流變化率將只和元件寬度有關

($\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$)而並非同時與元件寬度以及長度有關($\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$)。藉由從模型求出的缺陷尺寸來驗證模擬跑出來的缺陷尺寸、以及由模擬跑出來的缺陷尺寸來驗證模型求出的缺陷尺寸兩個相反的方式，可以證明這個假設。以此結果為根據，將 $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ 和 $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ 兩個模型藉由波茲曼函數合併起來，使得我們的新模型在次臨界電壓區域有 $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ 的特性、在強反轉區域有 $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ 的特性。並且，為了使此模型能夠應用在實際數據，我們適當地將其簡化。

HKMG MOSFET Random Telegraph Signals (RTS): Experiment, Modeling, and TCAD Simulation

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Abstract

Due to the request for smaller, faster, and more efficient metal-oxide-semiconductor field-effect transistors (MOSFETs), down-scaling has become a current trend of device development. As the dimensions of device are scaled, random telegraph signals (RTS) play an important role in the development of scaling technologies. Hence, researching the electronic property in the presence of RTS in nano-scale devices is becoming a challenging issue. These signals are generally considered as carrier trapping-detrapping from a defect situated in the silicon oxide. When a carrier is trapped, the trapped carrier will produce an additional screened Coulomb potential in the silicon oxide affecting the carriers in channel, and it makes the drain/source current fluctuate between two discrete levels as a trapping-detrapping process. In the experiment, it is not easy to observe the relation between drain/source current variation and the parameters which may impact RTS phenomenon. The one reason is that we cannot modify the characteristic of real devices as we want, and the other reason is that it is difficult to find RTS events across the whole wafer. However, we can solve these problems by using

TCAD simulation. In TCAD simulation, we can control the device characteristics by setting any parameters such as gate length, gate width, and doping concentrate, and insert a trap into silicon oxide to make sure the occurrence of RTS events in structure.

Building a new physical model of RTS is the major purpose in this thesis. Before building it, we have to characterize the practical device to get experimental data, and analyze its identity by simulating RTS phenomenon by TCAD. First, we built a MOSFET structure with different device sizes, different trap sizes, and different trap positions. By comparing the variation of drain/source current with different parameters, the trend of drain / source current variation changing with each of parameters can be obtained: (1) The rate of drain current change is larger when device size is smaller; (2) There is a peak in the curve for the rate of drain current change, and when device size is scaled, the peak will become sharper and sharper; (3) When the devices with the same width, the curve slopes for the drain current change rate in the subthreshold region are also the same; (4) Drain/source current of trap at gate center of device is smaller than trap at gate edge; and (5) Drain/source current of trap near the source is smaller than trap near the drain.

Second, after getting and analyzing the result, we assumed that in the same gate bias, the rate of drain current change would only relate to gate width ($\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$) instead of both gate width and gate length ($\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$) when it is in subthreshold region. Then, we verified the trap size in the TCAD simulation while determining the trap size in the model

derivation; and vice versa. Based on the simulated result, we combined the two models into a new one using Boltzmann function so that there are two distinct characteristics, $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ in subthreshold region and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ in strong inversion region. Then, it is a straight focused task to enable the application of the new model in the reproduction of experimental data.

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Figure Captions

Chapter 1

Introduction

1.1 Overview

As the dimensions of metal-oxide-semiconductor field-effect transistors (MOSFETs) were scaled in the last few years, random telegraph signals (RTS) had played an important role in the development of down-scaling technologies [1]-[6]. These signals are generally considered as carrier trapping-detrapping from a defect situated in the silicon oxide [1]-[6]. When a carrier is trapped, trapped carrier will produce an additional Coulomb energy in the silicon oxide affecting the carriers in channel, and it makes the drain/source current fluctuate between two discrete levels as a trapping-detrapping process. In the experiment, it is not easy to observe the relation between drain/source current variation and the parameters which may affect RTS phenomenon. The one reason is that we cannot modify the characteristic of real devices as we want, and the other reason is that it is difficult to find RTS events across the whole wafer. However, we can solve these problems by using TCAD simulator. In TCAD simulation, we can control the device characteristics by setting any parameters such as gate length, gate width, and doping concentrate, and insert a trap into silicon oxide to make sure the occurrence of RTS events in structure. If there are more traps in silicon oxide, several RTS events may occur, and the superposition of RTS in frequency domain is that of low frequency noise [3], [7]-[9].

Plural RTS events may make the drain/source current fluctuate between not only two but three, four, or more discrete levels. In this work, we focused on the two-level RTS originating from a single trap.

1.2 Arrangement of this Thesis

Different models trying to explain RTS amplitude have been proposed [3], [10]-[11], although the physical grounds of RTS phenomenon are not fully understood yet. Hence, building a new physical model of RTS is the major purpose of this thesis. Before building the model, we have to simulate RTS phenomenon of device by TCAD to observe its characteristics. The organization of this thesis is described below.

First, a brief introduction to the RTS was described in Chapter 1. There are two parts in Chapter 2: in Section 2.1, we showed our high-k metal gate device in terms of key parameters and RTS experimental data in this work; in Section 2.2, we built a MOSFET structure by TCAD simulation with certain parameters, and discussed RTS effect by changing the parameters. The parameters involved can be divided into three primary parts: gate size, trap size, and trap position. By comparing the variation of drain/source current with different parameters, the trend of drain/source current variation changing with each parameter could be obtained and it is shown in Chapter 3. The effect of gate size and trap size is introduced in Section 3.1, and the effect of trap position is introduced in Section 3.2.

Second, in Chapter 4, we started trying to build a model for RTS data fitting. After getting and analyzing the result, we assumed that in the same gate bias, the measured relative magnitude $\Delta I_d/I_d$ would only relate to gate width ($\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$) instead of both gate width and gate length ($\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$) when it is in subthreshold region, and we proved it by two different methods in Section 4.1. In Section 4.2, based on the simulated result, we combined the two models to constitute a new one via Boltzmann function so that there are two distinct characteristics in a new model in terms of $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ in subthreshold region and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ in strong inversion region. In Section 4.3, we made use of the new model to our experimental data to confirm the validity and applicability of the model. Finally, we summarized the conclusion of this work in Chapter 5.

Chapter 2

Device under Test

2.1 Experimental Device

The device under study was an *n*-channel MOSFET with a high-k metal gate stack. The key parameters were obtained by capacitance-voltage fitting: metal work function Ψ_m of 4.4V, effective oxide thickness EOT of 1.1nm, and body doping concentration N_{sub} of $4\times10^{18}cm^{-3}$. A semiconductor parameter analyzer HP4156 was utilized with the source and bulk tied to the ground and the drain connected to a bias V_d of 50mV. The measurement temperature was 300K. The probability of finding RTS events across the whole wafer was very low. Only a few devices were eventually identified with two-level RTS, as displayed in Fig. 1. The same RTS events in the drain current also simultaneously occurred in the source current. No noticeable change in the gate current has detected, meaning that the trap responsible for the RTS is an atomic-sized trap relative to the 1.1nm gate oxide used. This trap should be naturally created during the manufacturing process instead of the electrical stressing in the long-term RTS measurement.

To get $\Delta I_d/I_d$, we analyzed the RTS experimental data in terms of the frequence count. Frequence count is an analysis method which divides RTS data into few intervals and counts how many data points are there in each interval. After that, we fitted the data points by a normal distribution,

and we would get two fitting peaks which are two normal distribution curves. By calculating the expectation value of the two curves, high and low level of the RTS data could be obtained, and ΔI_d could be derived by subtracting low level from high level. Fig. 2 shows I_d - V_g curve and $\Delta I_d/I_d$ curve, respectively.

2.2 Simulation Device

The structure built by TCAD, as displayed in Fig. 3, was an *n*-channel MOSFET with the following key parameters: body doping concentration N_{sub} of $2\times10^{18}cm^{-3}$, drain/source doping concentration N_{ds} of $1\times10^{20}cm^{-3}$, n^+ polysilicon doping concentration N_{poly} of $1\times10^{20}cm^{-3}$, and gate oxide thickness t_{ox} of 2nm.

To simulate the effect caused by a trap, we built an isolated polysilicon rectangular window in the center of gate poly and gave it another bias V_{g2} differing from gate bias V_g. In contrast with setting a fixed charge into gate oxide, building an isolated polysilicon block into gate poly is easier to control and observe the effect range caused by trap. In this work, we set V_{g2} = -1V, V_d = 0.05V, and set V_g scanning from 0V to 1.2V with the interval of 0.1V.

In this work, we utilized TCAD to build the MOSFETs structure with a trap, and simulated RTS events in the structure to observe the effect of RTS. We discussed RTS effect in some aspects: (1) Changing gate width of devices to simulate I_d - V_g curves affected by RTS for

different gate widths; (2) Changing gate length of devices to simulate I_d - V_g curves affected by RTS for different gate lengths; (3) Changing trap size (L_t) to simulate different apparent Debye lengths; and (4) Changing trap position to simulate the effect of varying trap position.

Because we could not simulate dynamic trapping-detrapping process in TCAD, structures with a trap and without trap were built in each size to simulate static trapping and detrapping conditions respectively. Therefore, $\Delta I_d/I_d$ could be obtained by

$$\frac{\Delta I_d}{I_d} = \frac{I_{d(without\ trap)} - I_{d(with\ trap)}}{I_{d(without\ trap)}} \quad (2\text{-}1)$$

Fig. 4 displays I_d - V_g curves among the devices of different sizes. Fig. 5, Fig. 6, and Fig. 7 reveal comparisons of $\Delta I_d/I_d$ curves among the devices of different sizes. The data will be deeply analyzed in Chapter 3.

Chapter 3

Factors of RTS

As mentioned in Section 2.2, we built an isolated polysilicon rectangular window in the gate poly to simulate trap. Here, L_t is defined as the width and length of the rectangular window. L_t is set to simulate apparent Debye length that is the distance over which carriers screen out electric fields [12]. Generally, the relative amplitude $\Delta I_d/I_d$ is considered as a ratio of the trap induced cored-out area L_t^2 to the gate area so that $\Delta I_d/I_d$ of RTS can be expressed by a screened Debye length model [11]. Therefore, $\Delta I_d/I_d$ as a critical factor of RTS will be focused in this thesis.

3.1 Device Gate Size and Trap Size versus RTS

To observe I_d - V_g and $\Delta I_d/I_d$ curves affected by RTS for different gate widths and lengths, we changed device size in TCAD simulation. In this work, we simulated different devices with gate width W = 500, 100, and 60nm; gate length L = 500, 100, and 60nm; trap size L_t = 10, 5, and 2nm. Fig. 5, Fig. 6, and Fig. 7 all show the $\Delta I_d/I_d$ curves in devices with different gate sizes and different trap sizes.

From the diagrams three different observations can be drawn. First, $\Delta I_d/I_d$ is larger when device length is shorter. For physical description, it means RTS events are more obvious in short channel devices. Second, there is a peak in $\Delta I_d/I_d$ curve, and when device length is scaled, the peak will become sharper and sharper. The peak lies at about threshold voltage

which is the boundary between subthreshold and inversion region. Thus, $\Delta I_d/I_d$ decreases due to the extreme increase of I_d. Third, for the device with the same width, the slope of $\Delta I_d/I_d$ curves in the subthreshold region is also the same. It may act as evidence that $\Delta I_d/I_d$ is only related with device width in the subthreshold region.

3.2 Trap Position versus RTS

In Section 3.1, as the general case, trap is set in the center of gate polysilicon, but in the practical experiment, the trap may not locate right in the center of gate. Consequently, in this section we would change trap position for practical cases. To simplify the expression of trap position, we built a coordinate system on the gate: (1) Gate width direction is set to *x*-axis; (2) Gate length direction is set to *y*-axis where drain side is taken as positive side and source side is taken as negative side; and (3) The center of gate is set to the origin (0,0). After setting the coordinate system on the gate poly, we normalized it to that *x*-axis in the interval [1,-1] and *y*-axis in the interval [1,-1] as well. The pictures with traps at different positions are shown in Fig. 8, and the $\Delta I_d/I_d$ curves of different trap positions are shown in Fig. 9 and Fig. 10.

From Fig. 9, we can observe that trap at (0,0) is larger, and trap at (0,1) and (0,-1) is smaller. Besides, though the curves of (0,1) and (0,-1) are about the same, the value of (0,-1) is larger than (0,1). From Fig. 9 and Fig. 10, $\Delta I_d/I_d$ change with different trap positions in the width direction. However, $\Delta I_d/I_d$ for trap at gate center changes much more than

$\Delta I_d/I_d$ for trap at gate edge. Such result can be observed not only for different positions in the width directions, but also different positions in the length direction. It may prove that the influenced range of trap is large enough, so when trap position is at gate edge, the range of effect becomes smaller.

I_d of trap near source is smaller than trap near drain. From the $\Delta I_d/I_d$ diagram, we can observe that the largest change between $\Delta I_d/I_d$ curves is at about V_g = 0.3V. Therefore, electron density distribution along length direction (shown in Fig. 11) was extracted to compare the difference between gate edge of drain side and source side. We can observe that electron density is larger at source side, so trap has a larger effect when it is at source side.

Chapter 4

$\Delta I_d/I_d$ Modeling

From the TCAD simulated $\Delta I_d/I_d$ curves, we can observe that the trend of $\Delta I_d/I_d$ curves with V_g increasing is not continuously decreasing but increasing in subthreshold region and decreasing afterward. Based on the result, we assumed that there is another fitting model differing from $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ in subthreshold region. In subthreshold region, the energy band will be extremely sharp under the trap, and it may cause $\Delta I_d/I_d$ involving with only the width factor instead of both width and length. Thus, we will apply $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ simultaneously to fit $\Delta I_d/I_d$ curve in the following paragraphs.

4.1 Correction for $\Delta I_d/I_d$ Fitting

Fig. 12 shows the $\Delta I_d/I_d$ curve. From the model $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$, $L_t = \frac{\Delta I_d}{I_d} \times W$ and $L_t = \sqrt{\frac{\Delta I_d}{I_d} \times WL}$ was obtained, respectively. Therefore, we can observe the validity of L_t while verifying the models.

Fig. 13 shows the L_t curves which are obtained from $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ (red line) and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ (black line). Trap width defined by TCAD (10nm) and channel width (50nm) are also displayed in diagram as minimum and maximum value of L_t. From the diagram, we can observe that L_t obtained

by $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ is small than 10nm at high V_g, which is invalid. It means that $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ cannot be applied to strong inversion case.

Besides, we can observe that L_t curve obtained by $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ approaches L_t = 10nm line at high V_g, because V_g increasing makes screen effect increase. It means that $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ should be applied to strong inversion case.

Fig. 14(a) shows electron density at V_{g2} = -1V, electron density without trap, as well as *Δelectron density* curves. For example, to define L_t, we assumed that the length with *Δelectron density/electron density*$_{(without\ trap)}$ = 45% is L_t. Fig. 14(b) shows *Δelectron density/electron density*$_{(without\ trap)}$ at different V_g. From the intersection of *Δelectron density/electron density*$_{(without\ trap)}$ and 45% line, we can observe that L_t change with V_g. Besides, it is noticeable that L_t becomes larger from V_g = 0.1V to V_g = 0.3V, and then becomes smaller after V_g = 0.3V.

To fit $\Delta I_d/I_d$, we found different *Δelectron density/electron density*$_{(without\ trap)}$ to account for L_t. When *Δelectron density/electron density*$_{(without\ trap)}$ is 45%, $\frac{L_t}{W}$ curve matches $\Delta I_d/I_d$ in subthreshold region, and $\frac{L_t^2}{WL}$ curve matches $\Delta I_d/I_d$ in strong inversion region (shown in Fig. 15). The two matching curves in combination with $\Delta I_d/I_d$ curve is shown in Fig. 16.

By getting L_t from model $L_t = \frac{\Delta I_d}{I_d} \times W$ and $L_t = \sqrt{\frac{\Delta I_d}{I_d} \times WL}$, we can see that $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ is applicable in strong inversion, but $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ is not. By getting L_t from simulated electron density, we see that $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ can be applied to strong inversion case, while $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ is applied to subthreshold case. Therefore, we can confirm that in subthreshold case, we should use $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ instead of $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$.

4.2 New Physical Model for $\Delta I_d/I_d$ Fitting

To obtain the formula of $\Delta I_d/I_d$ fitting curve, a function

$$y = \frac{A_1 - A_2}{1 + e^{(x - x_0)/dx}} + A_2 \tag{4-1}$$

was used to combine $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ with $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$. This formula connects two different levels (A_1 and A_2) by a curve with a specific slope ($y' = (A_2 - A_1)/4dx$) and the midpoint (x_0).

Parameters x_0 and dx of $\Delta I_d/I_d$ curve can be obtained by a fitting technique. And then, let $\frac{L_t}{W}$ be A_1 and $\frac{L_t^2}{WL}$ be A_2, we got the formula

$$\frac{\Delta I_d}{I_d} = \frac{\frac{L_t}{W} - \frac{L_t^2}{WL}}{1 + e^{(V_g - V_{g0})/dV}} + \frac{L_t^2}{WL} \tag{4-2}$$

and the fitting curve is shown in Fig. 17.

In data fitting case, parameter V_{g0} and dV cannot be obtained

because $\Delta I_d/I_d$ data are usually limited. In formula (4-1), there are two extreme cases: (1) If $x \rightarrow 0$, $e^{(x-x_0)/dx} << 1$, $y = A_1$; and (2) If $x \rightarrow \infty$, $e^{(x-x_0)/dx} >> 1$, $y = A_2$.

Therefore, based on these two cases, we modify the formula to be

$$\frac{\Delta I_d}{I_d} = \frac{\frac{Lt}{W} - \frac{L_t^2}{WL}}{1+\frac{N_s}{N_{s0}}} + \frac{L_t^2}{WL} \tag{4-3}$$

where N_s is inversion carrier density, and N_{s0} is defined as a certain inversion carrier density at $V_g = V_{th}$. The formula has the identical extreme cases: (1) If $V_g \rightarrow 0$, $N_s << N_{s0}$, $\frac{N_s}{N_{s0}} << 1$, and $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$; and (2) If $V_g \rightarrow \infty$, $N_s >> N_{s0}$, $\frac{N_s}{N_{s0}} >> 1$, and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$.

N_{s0} is defined as the inversion carrier density at $V_g = V_{th}$ because threshold voltage V_{th} is the boundary between subthreshold and strong inversion region, and it can make $\frac{N_s}{N_{s0}} >> 1$ when operated in strong inversion and $\frac{N_s}{N_{s0}} << 1$ in subthreshold. The fitting curve is shown in Fig. 18.

4.3 Data Fitting

With the abovementioned experiment data, V_{th} can be obtained from I_d - V_g curve by $g_{m,max}$ method, and N_{s0} also can be determined from N_s curve obtained by capacitance-voltage fitting. Therefore formula (4-3) can be applied to this case to extract L_t, and to make a comparison with

$\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$, the two curves and new model fitting line are shown in Fig. 19. From the diagram we can observe that $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ is near the new model fitting line at high V_g, and it is not obvious that $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ is near the new model fitting line at low V_g because the experiment $\Delta I_d/I_d$ curve in the interval between V_g = 0.46V to V_g = 0.6V is distant from subthreshold region.

Chapter 5

Conclusion

$\Delta I_d/I_d$ fitting model has been established by analyzing both experimental and simulation data. In this thesis, by finding the RTS events in HKMG device, we built a structure by TCAD simulator to simulate RTS events and discussed about the relationship between various device parameters and RTS. In the over literal, the equation $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ was widely applied to the entire $\Delta I_d/I_d$ curves for different gate biases. We used TCAD to simulate structures with RTS events and extracted the practical range of trap L_t from electron density distribution while fitting $\Delta I_d/I_d$ data. Besides, we have proved that RTS is 1D effect in subthreshold region and 2D effect in strong inversion region. Finally, a new $\Delta I_d/I_d$ fitting formula was acquired by the two boundary conditions in this study.

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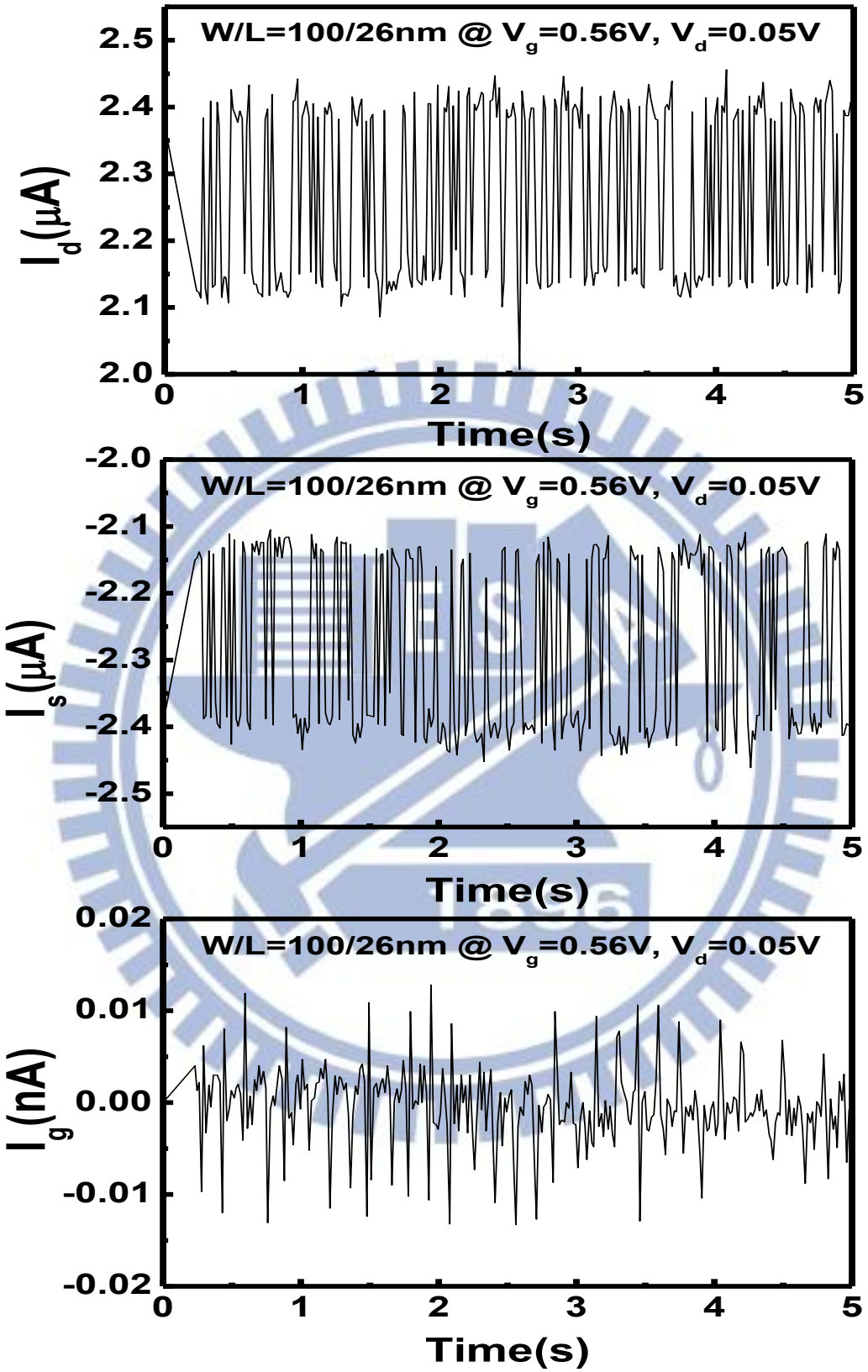


Fig. 1 Time records of the drain, source, and gate currents for *W/L* = 100/26nm device at V_g = 0.56V, and V_d = 0.05V.

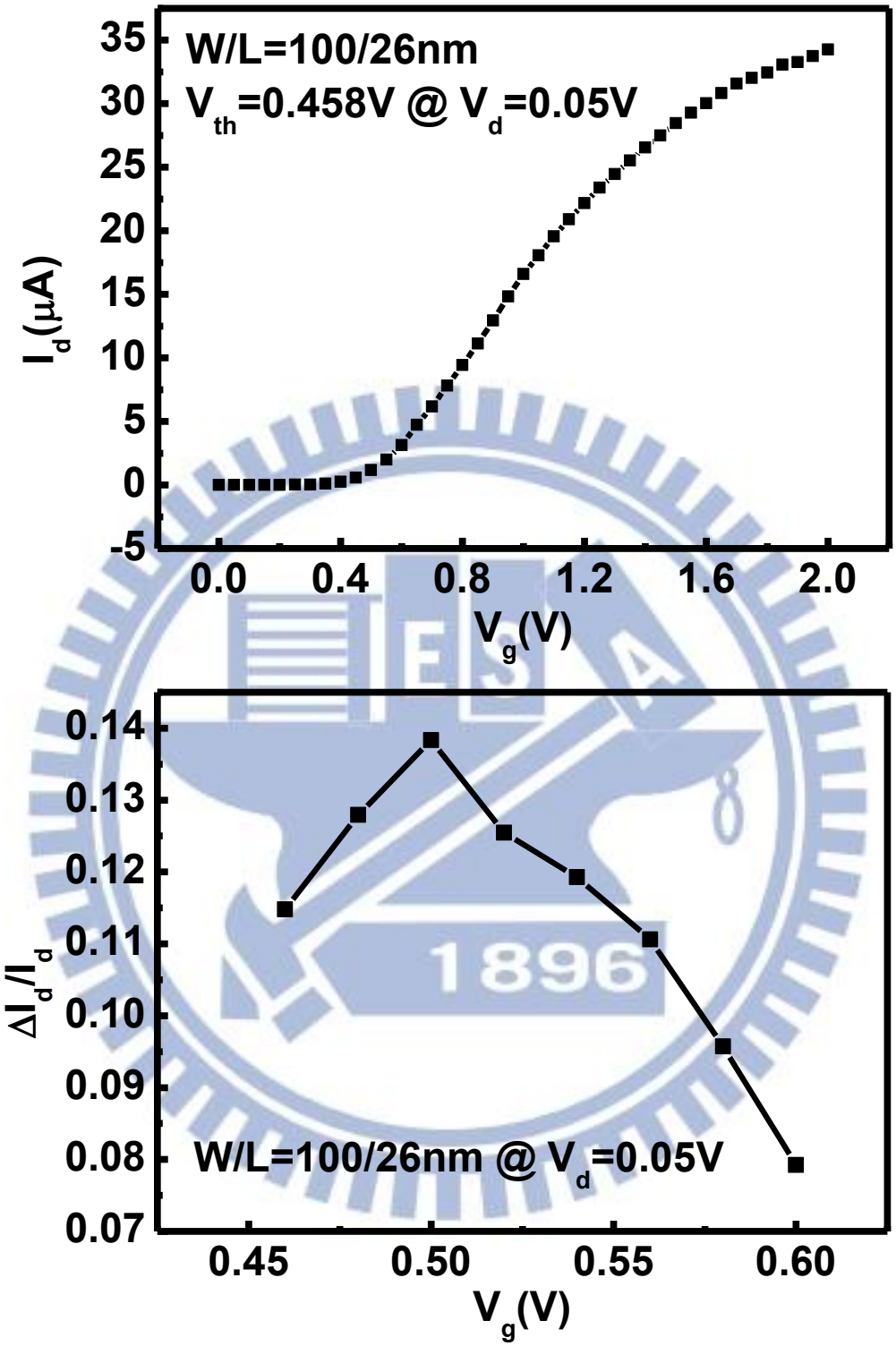


Fig. 2 The experimental data of I_d and $\Delta I_d/I_d$ versus V_g for W/L = 100/26nm device.

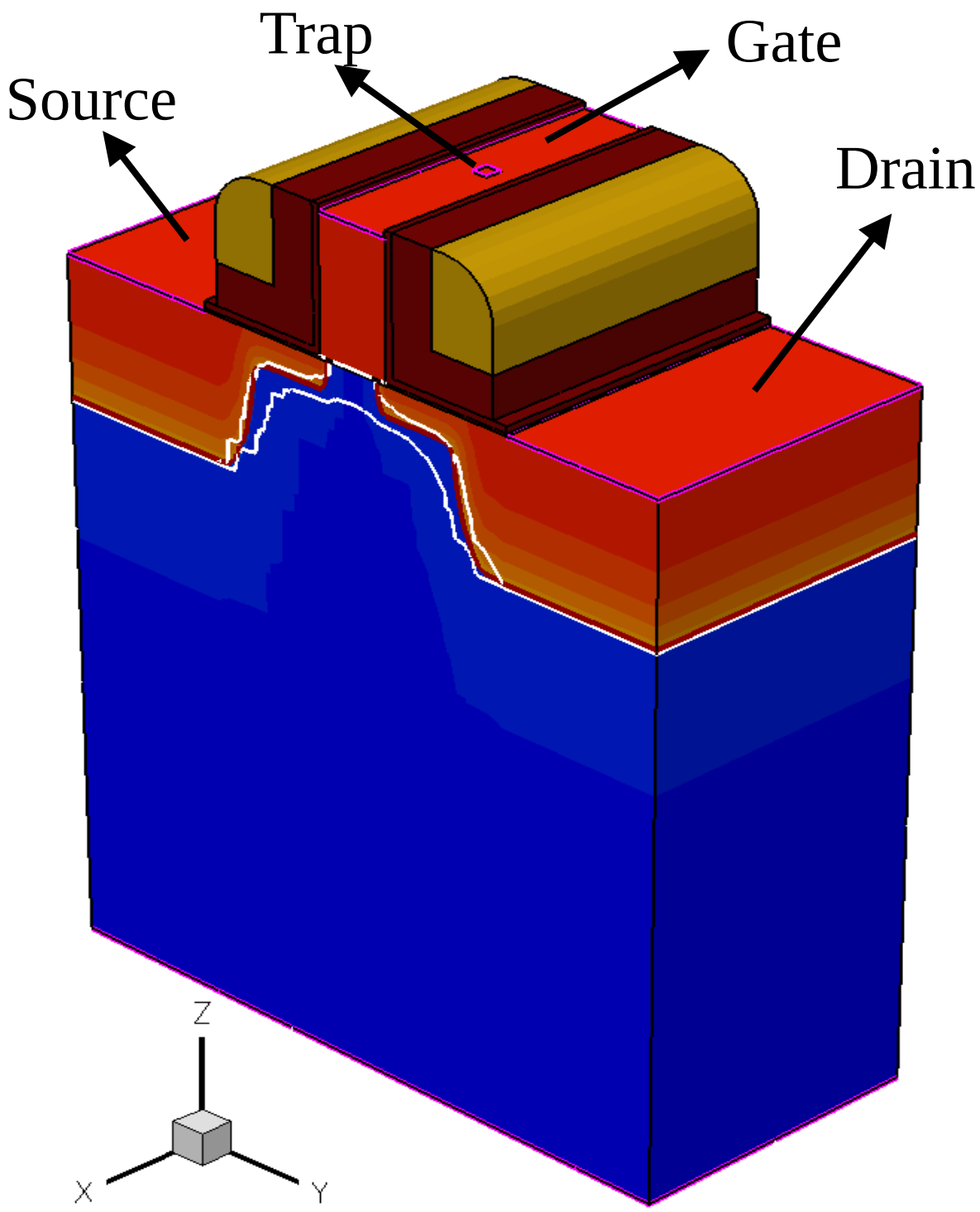


Fig. 3 The structure built in TCAD under study with N_{sub} = 2×10^{18}cm^{-3}, N_{ds} = 1×10^{20}cm^{-3}, N_{poly} = 1×10^{20}cm^{-3}, and t_{ox} = 2nm.

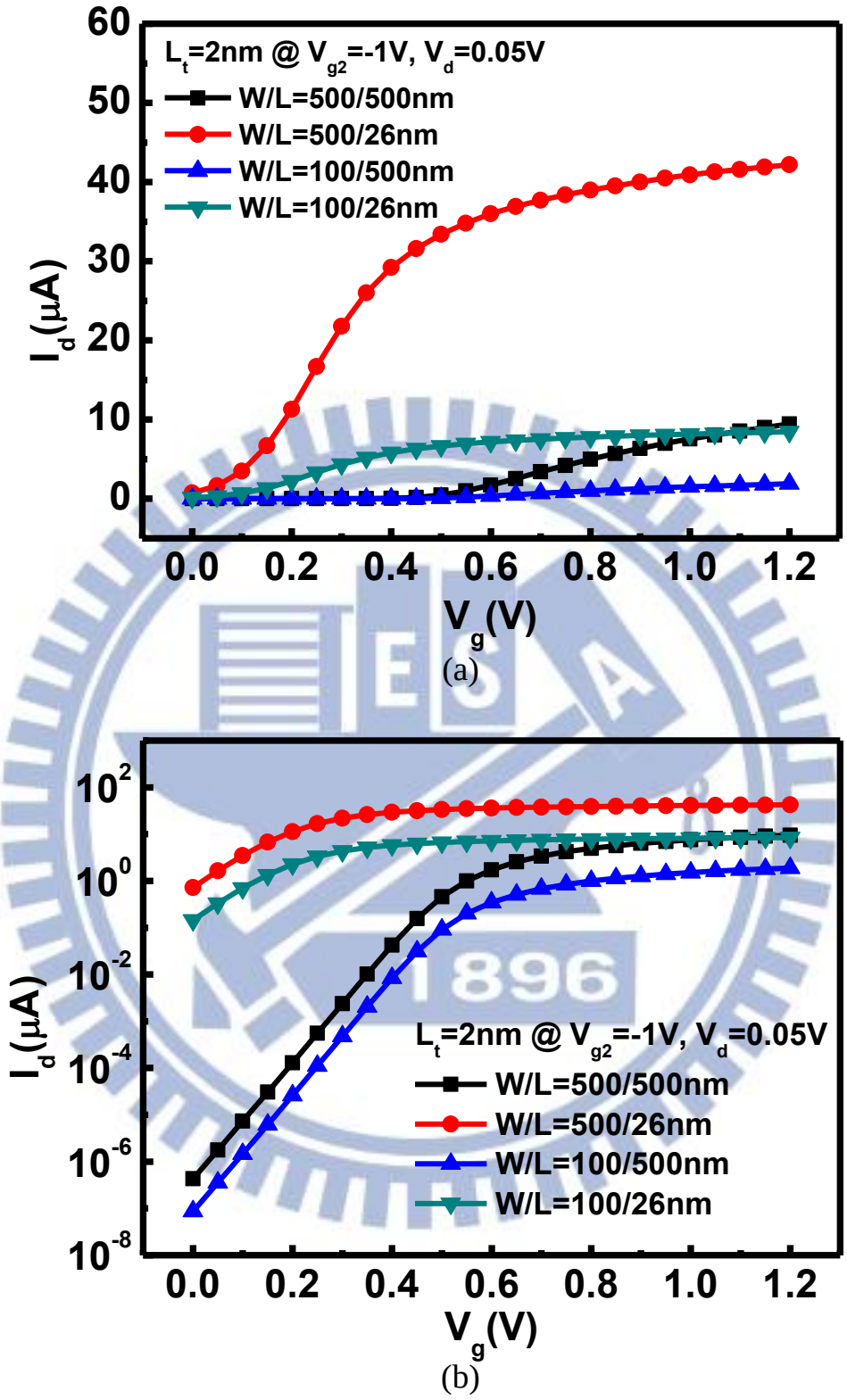


Fig. 4 (a) The simulated drain currents (I_d) versus gate voltage (V_g) of different sizes in linear scale. (b) The simulated drain currents versus gate voltage of different sizes in log scale.

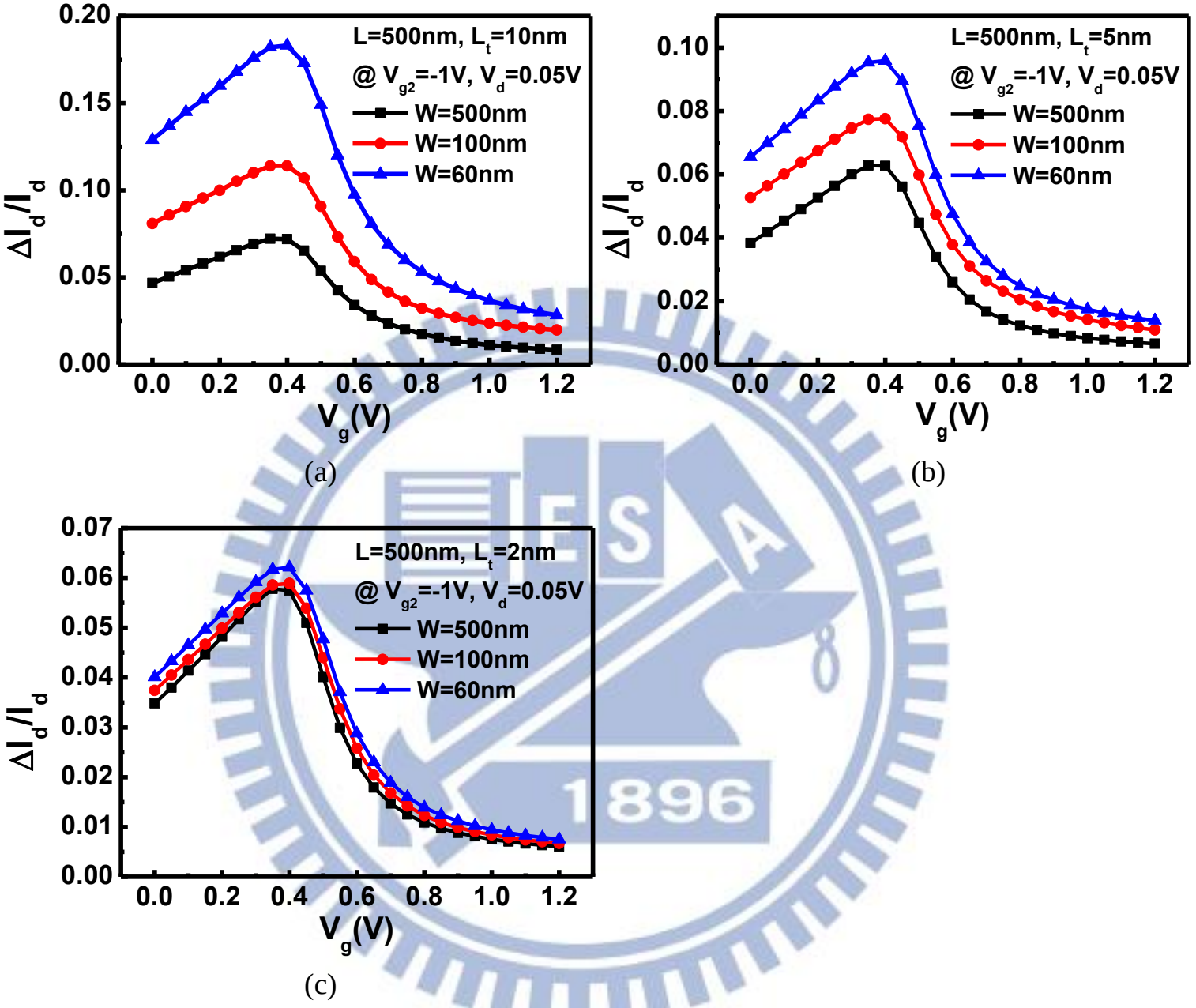


Fig. 5 The diagrams showing $\Delta I_d/I_d$ curves in devices with different sizes. (a) L = 500nm, and L_t = 10nm. (b) L = 500nm, and L_t = 5nm. (c) L = 500nm, and L_t = 2nm.

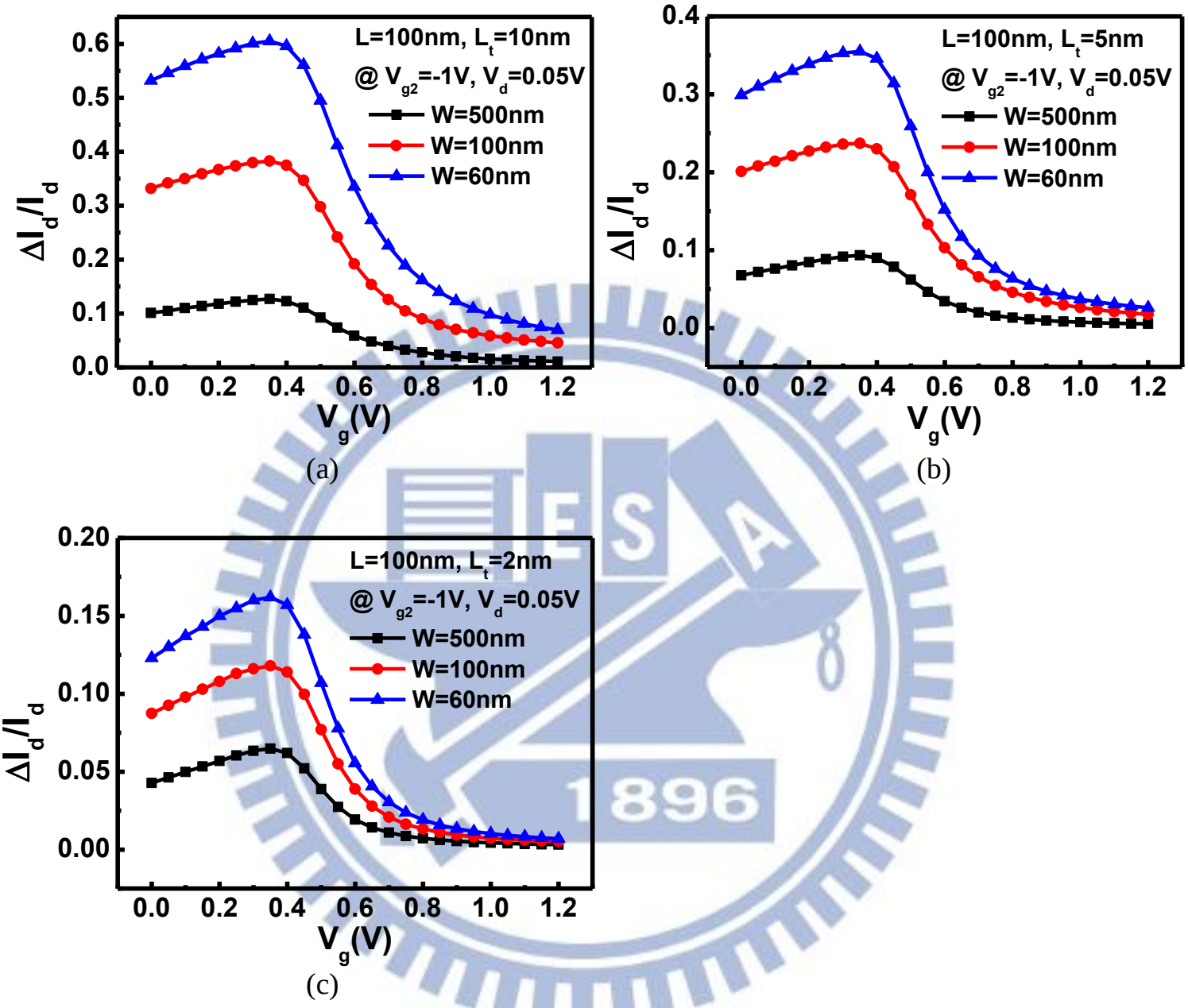


Fig. 6 The diagrams showing $\Delta I_d/I_d$ curves in devices with different sizes. (a) L = 100nm, and L_t = 10nm. (b) L = 100nm, and L_t = 5nm. (c) L = 100nm, and L_t = 2nm.

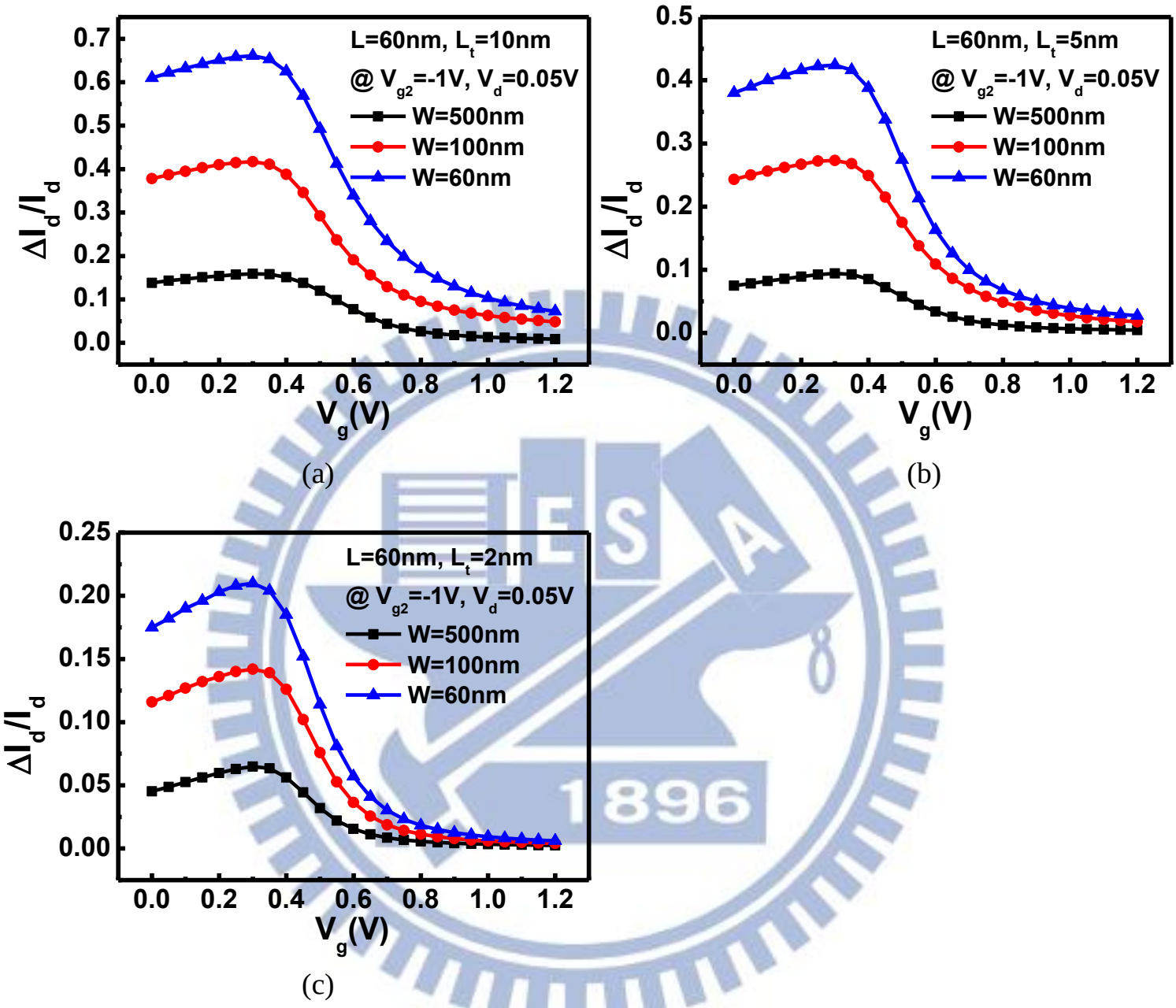


Fig. 7 The diagrams showing $\Delta I_d/I_d$ curves in devices with different sizes. (a) L = 60nm, and L_t = 10nm. (b) L = 60nm, and L_t = 5nm. (c) L = 60nm, and L_t = 2nm.

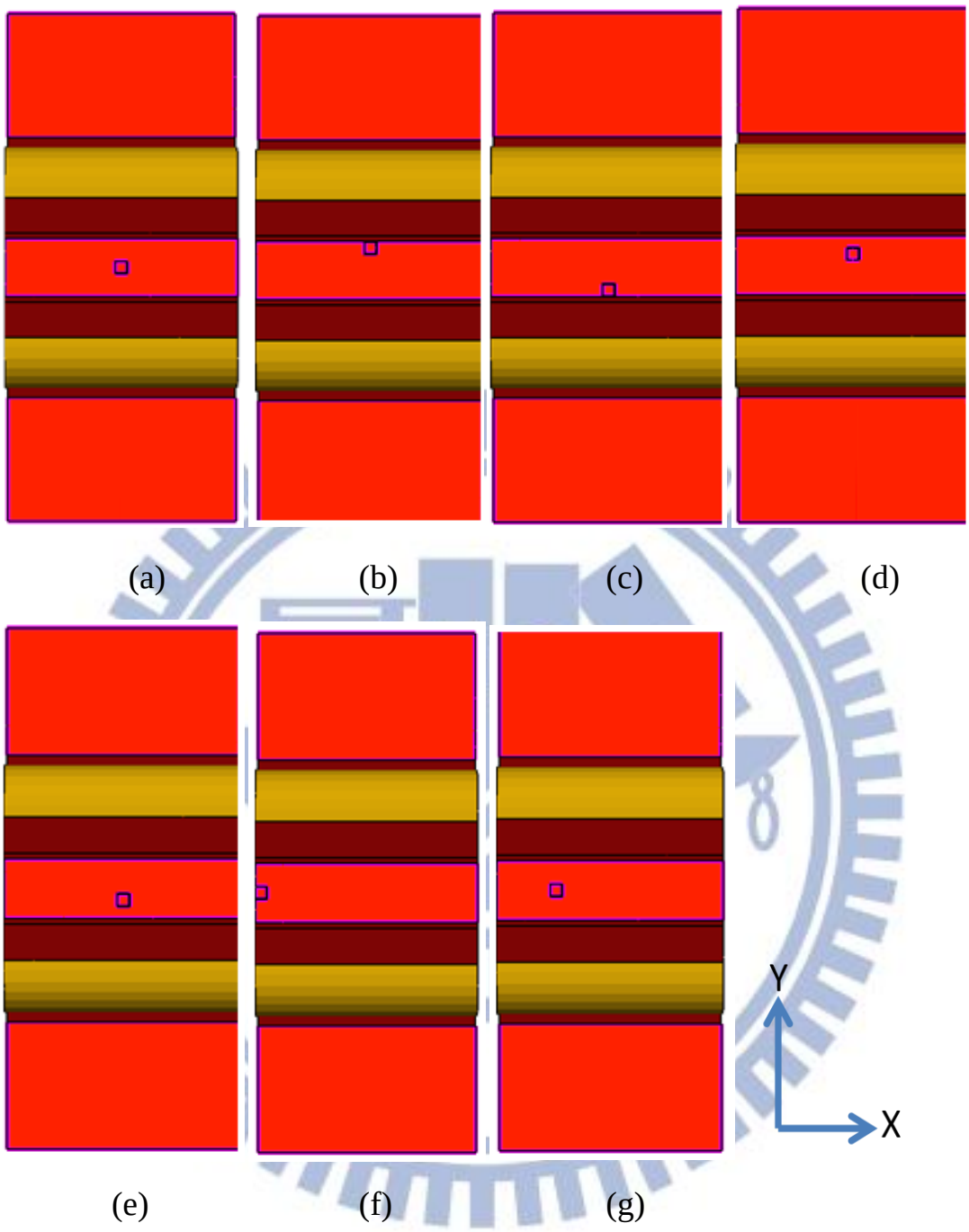


Fig. 8 The trap position presented in normalized form. (a) (0,0); (b) (0,1); (c) (0,-1); (d) (0,0.5); (e) (0,-0.5); (f) (-1,0); and (g) (-0.5,0).

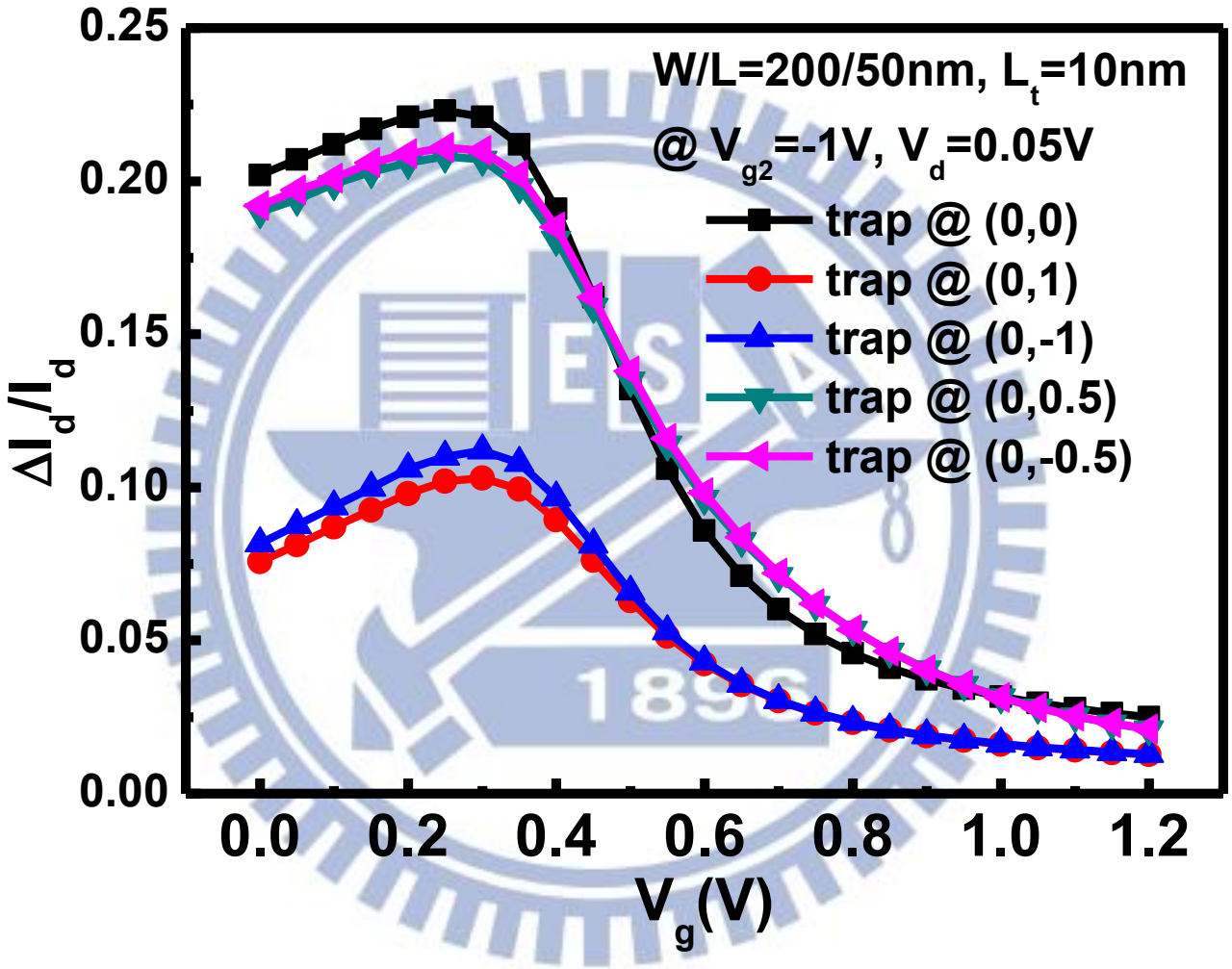


Fig. 9 $\Delta I_d/I_d$ curves in device with different trap positions in *x*-axis direction (width direction).

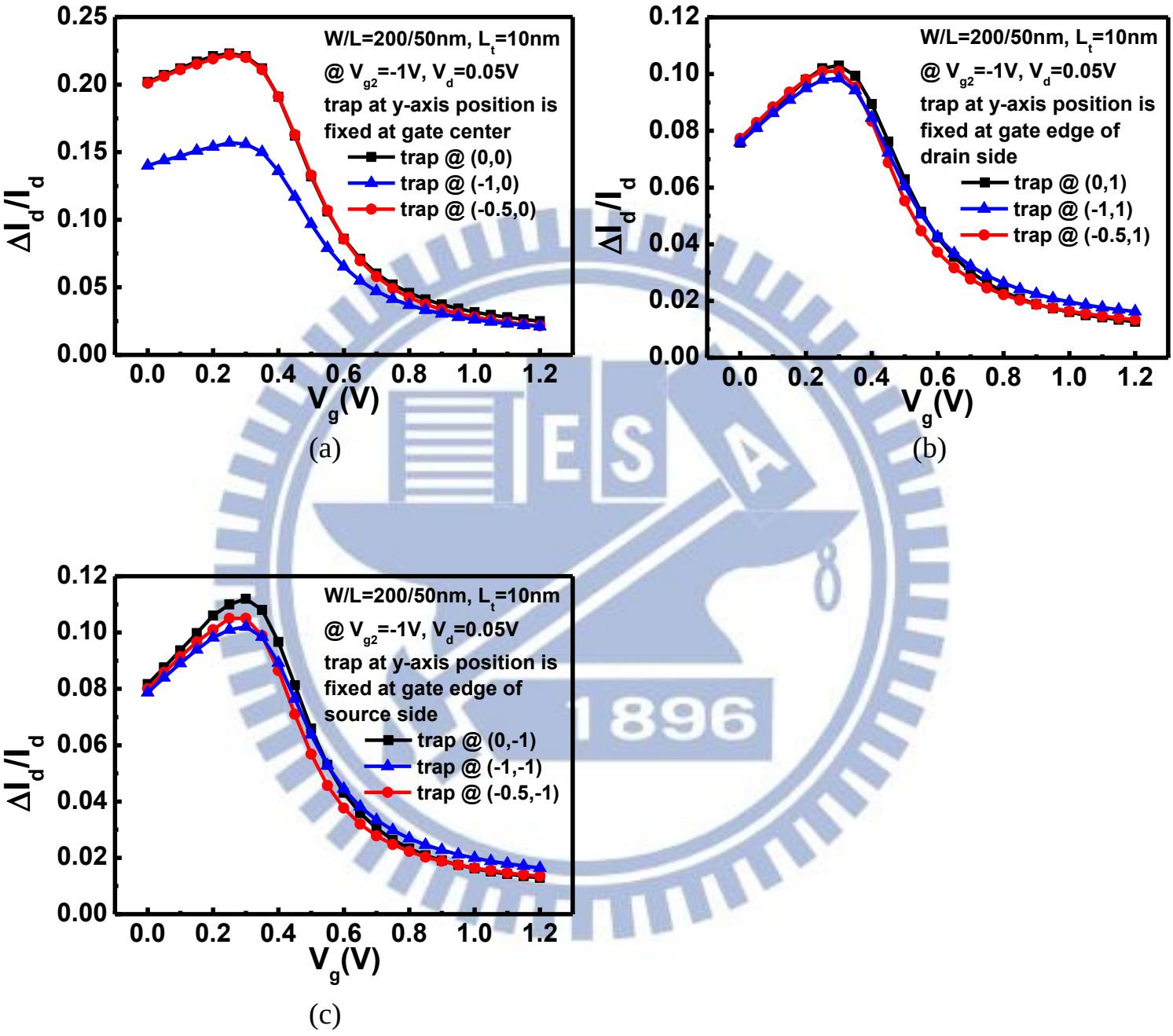


Fig. 10 The diagrams showing $\Delta I_d/I_d$ curves in device with different trap positions in *y*-axis direction (length direction). (a) Trap at the center; (b) Trap at gate edge of drain side; and (c) Trap at gate edge of source side.

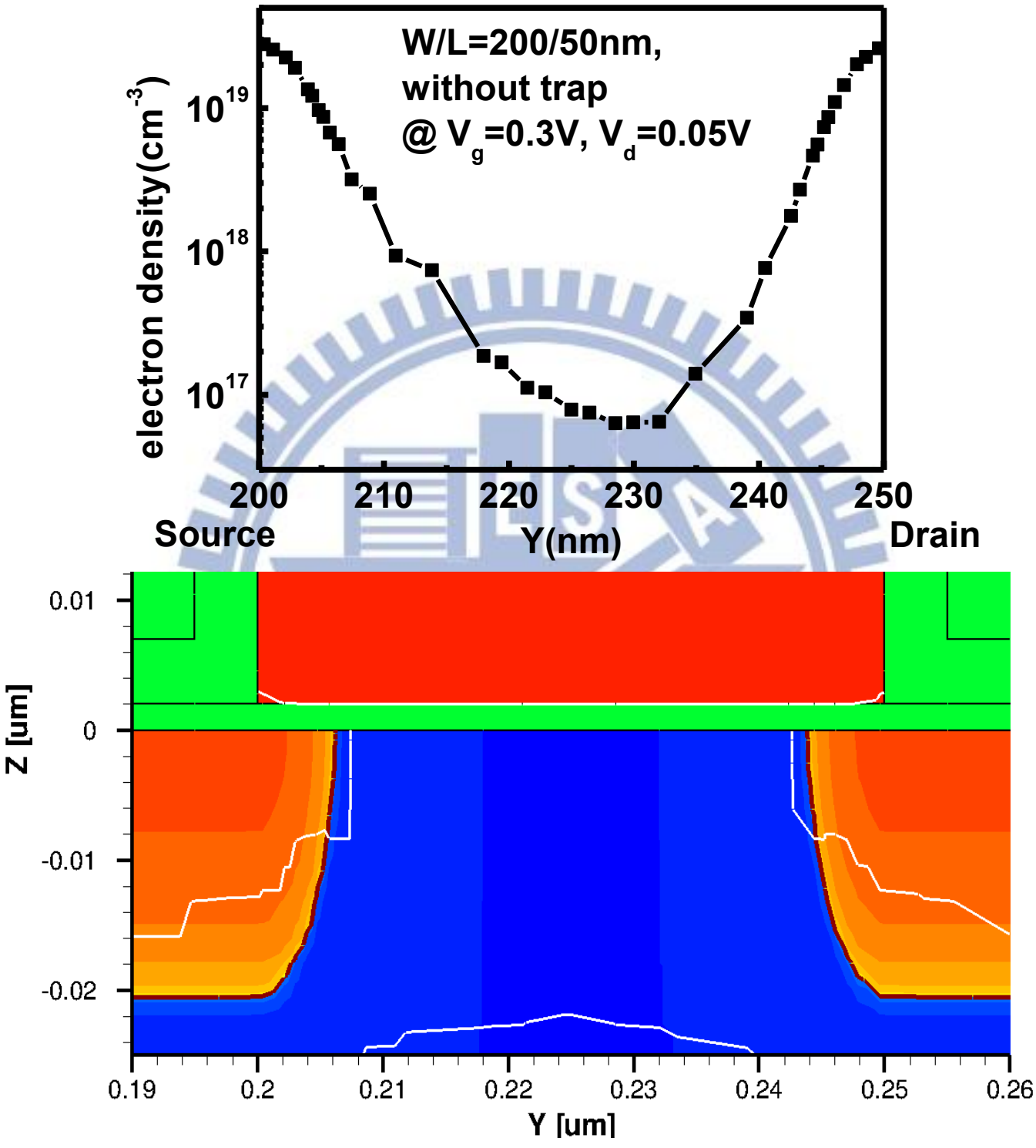


Fig. 11 Electron density distribution along length direction. The region of gate length is in the interval at Y = 200nm to Y = 250nm.

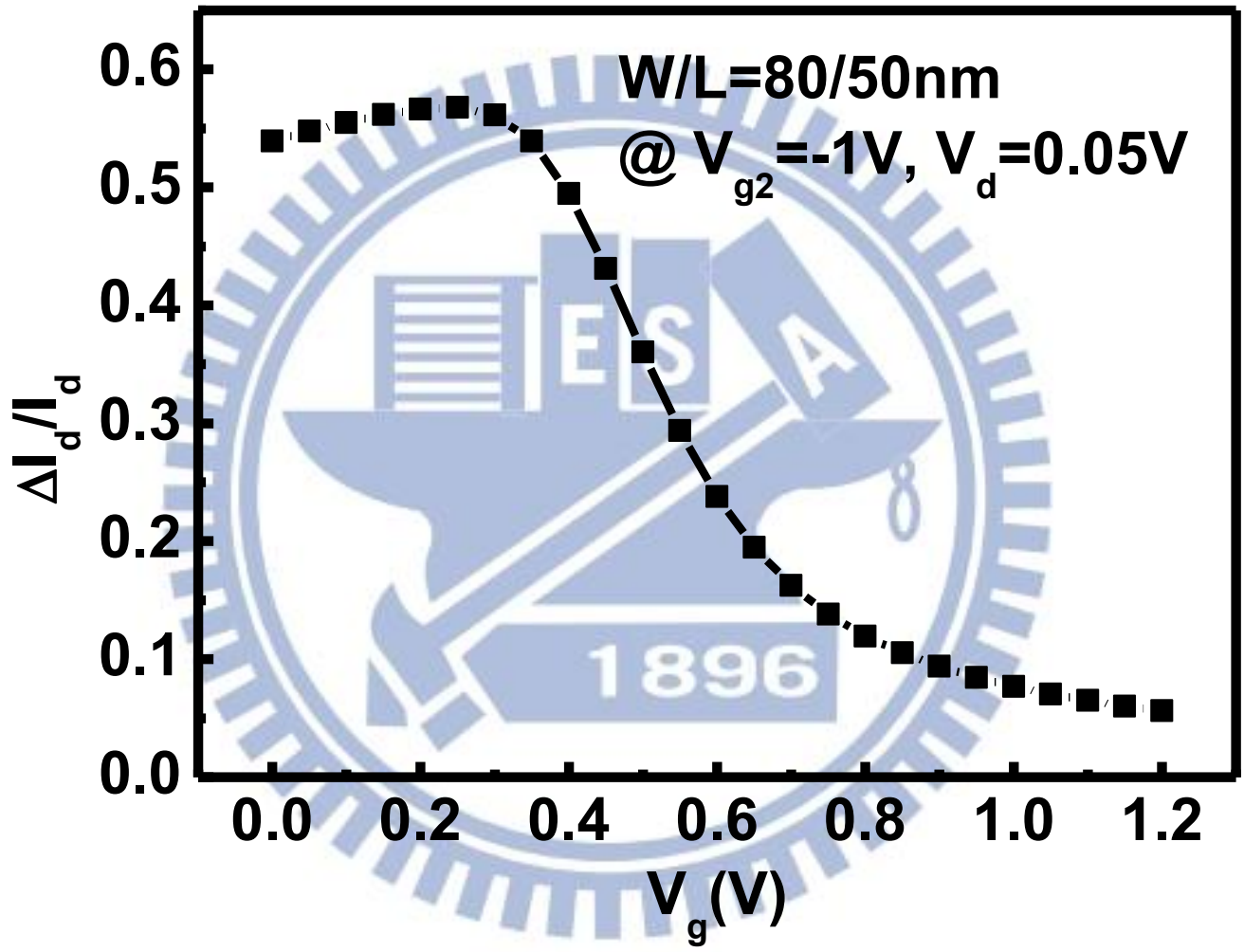


Fig. 12 The simulated $\Delta I_d/I_d$ curve in W/L = 80/50nm, L_t = 10nm device.

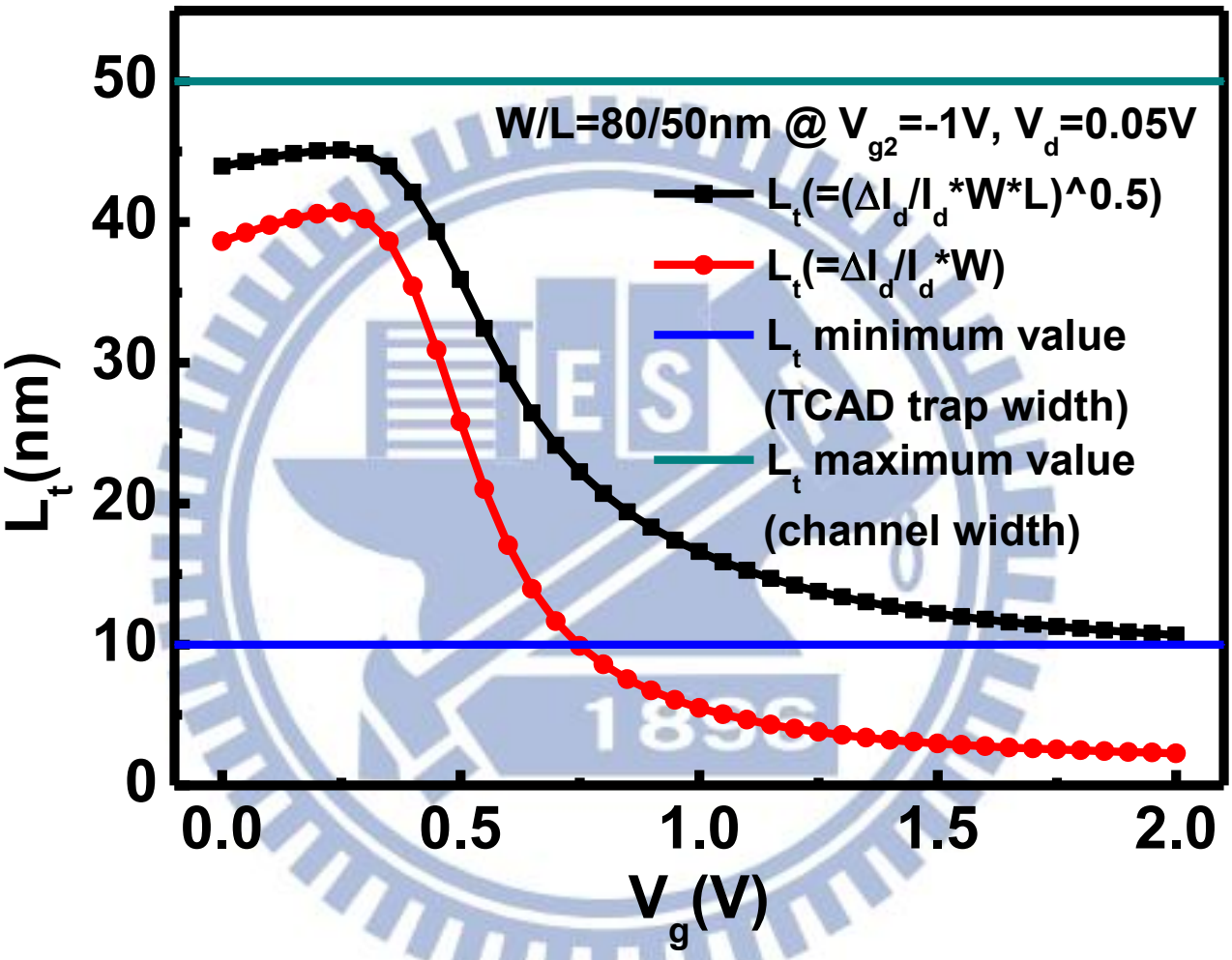


Fig. 13 L_t obtained from $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ (red line) and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$ (black line). Trap width defined by TCAD (10nm) and channel width (50nm) are also displayed in diagram as minimum and maximum value of L_t, respectively.

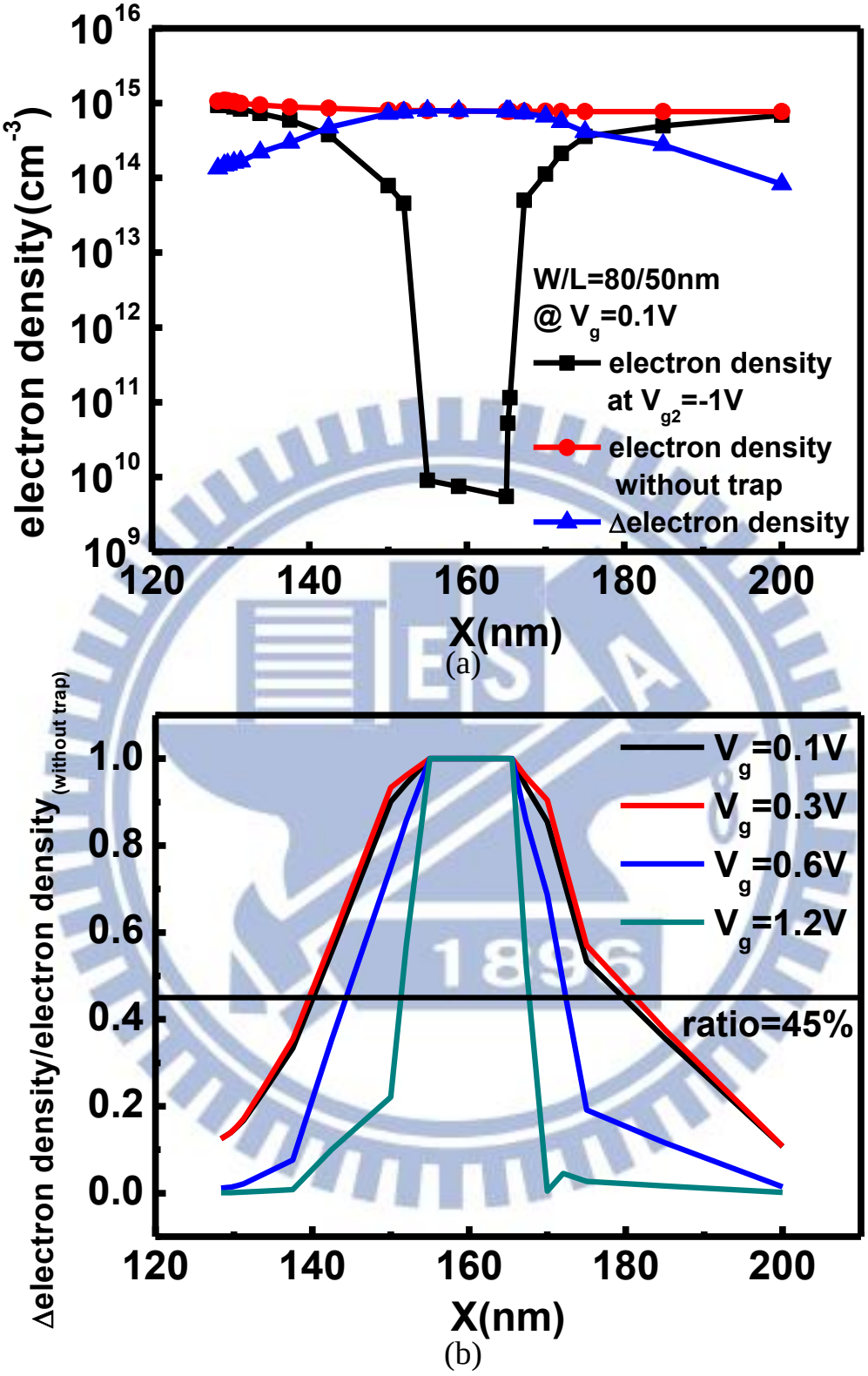
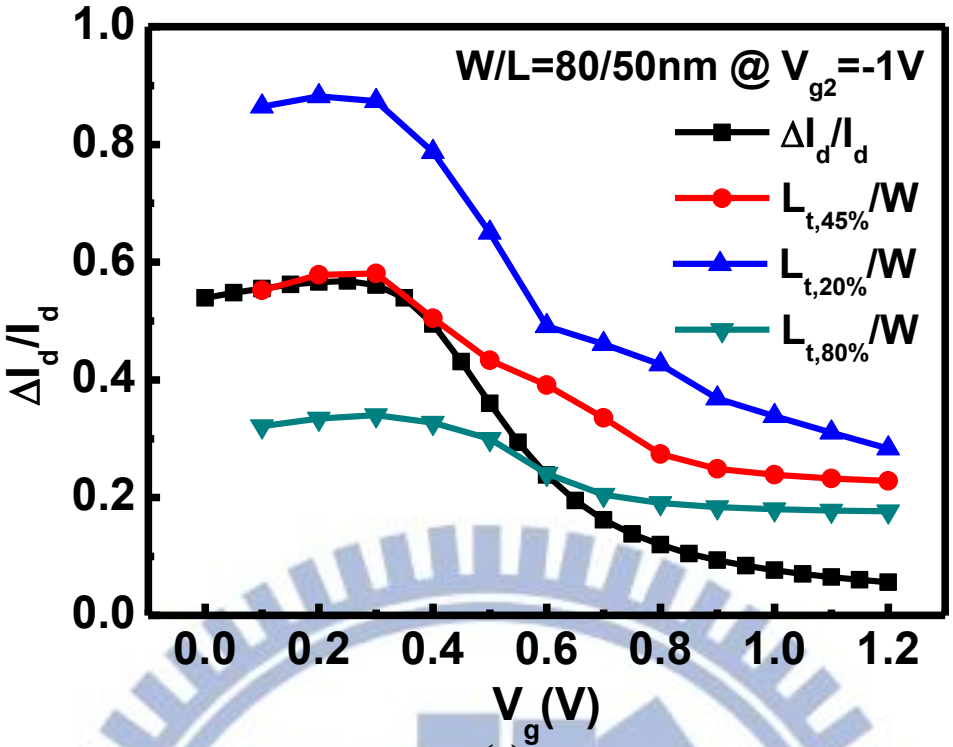
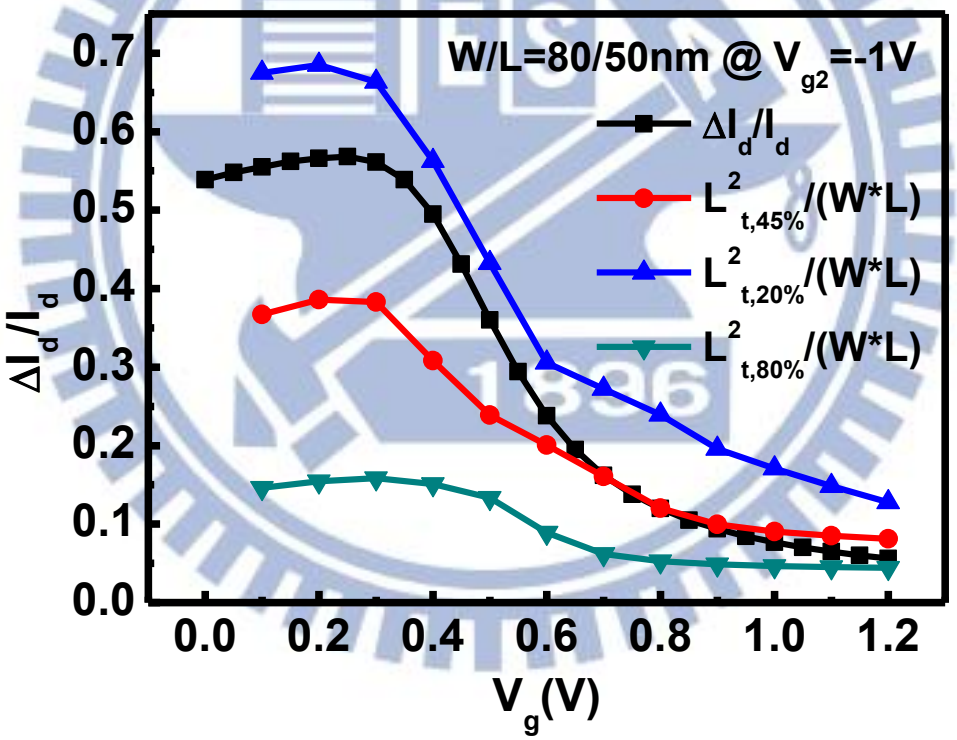


Fig. 14 (a) Electron density with a trap (giving V_{g2} = -1V) and without trap, as well as the *Δelectron density* curves. (b) *Δelectron density/electron density*$_{(without\ trap)}$ curves at different V_g.



(a)



(b)

Fig. 15 (a) $\frac{L_t}{W}$ and $\Delta I_d/I_d$ curves at Δ*electron density/electron density*$_{(without\ trap)}$ is 45%, 20%, and 80%. (b) $\frac{L_t^2}{WL}$ and $\Delta I_d/I_d$ curves at Δ*electron density/electron density*$_{(without\ trap)}$ is 45%, 20%, and 80%.

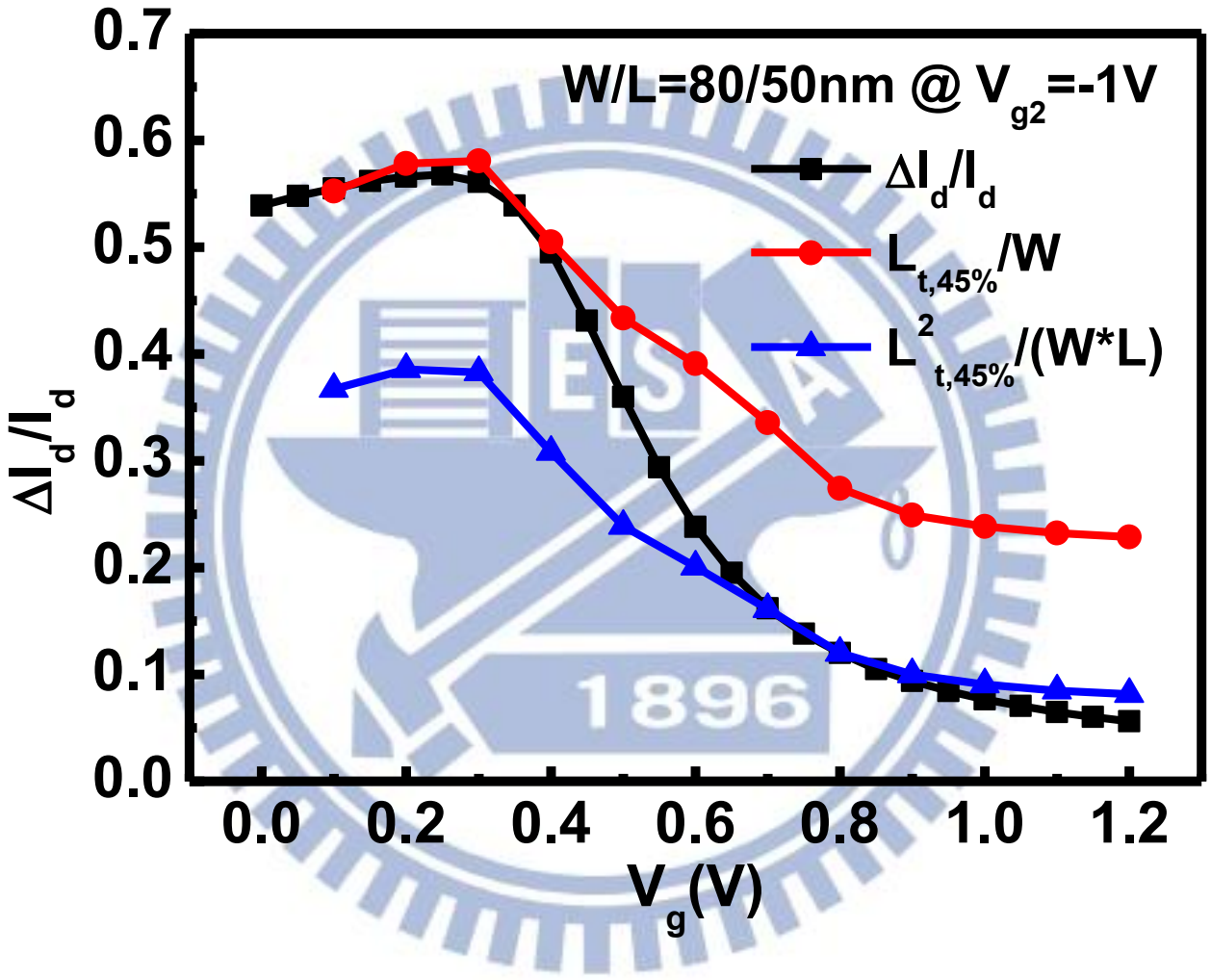


Fig. 16 Fit of $\frac{L_t}{W}$ and $\frac{L_t^2}{WL}$ to $\Delta I_d/I_d$ curve. $\frac{L_t}{W}$ curve matches the $\Delta I_d/I_d$ at low V_g and $\frac{L_t^2}{WL}$ curve matches $\Delta I_d/I_d$ at high V_g.

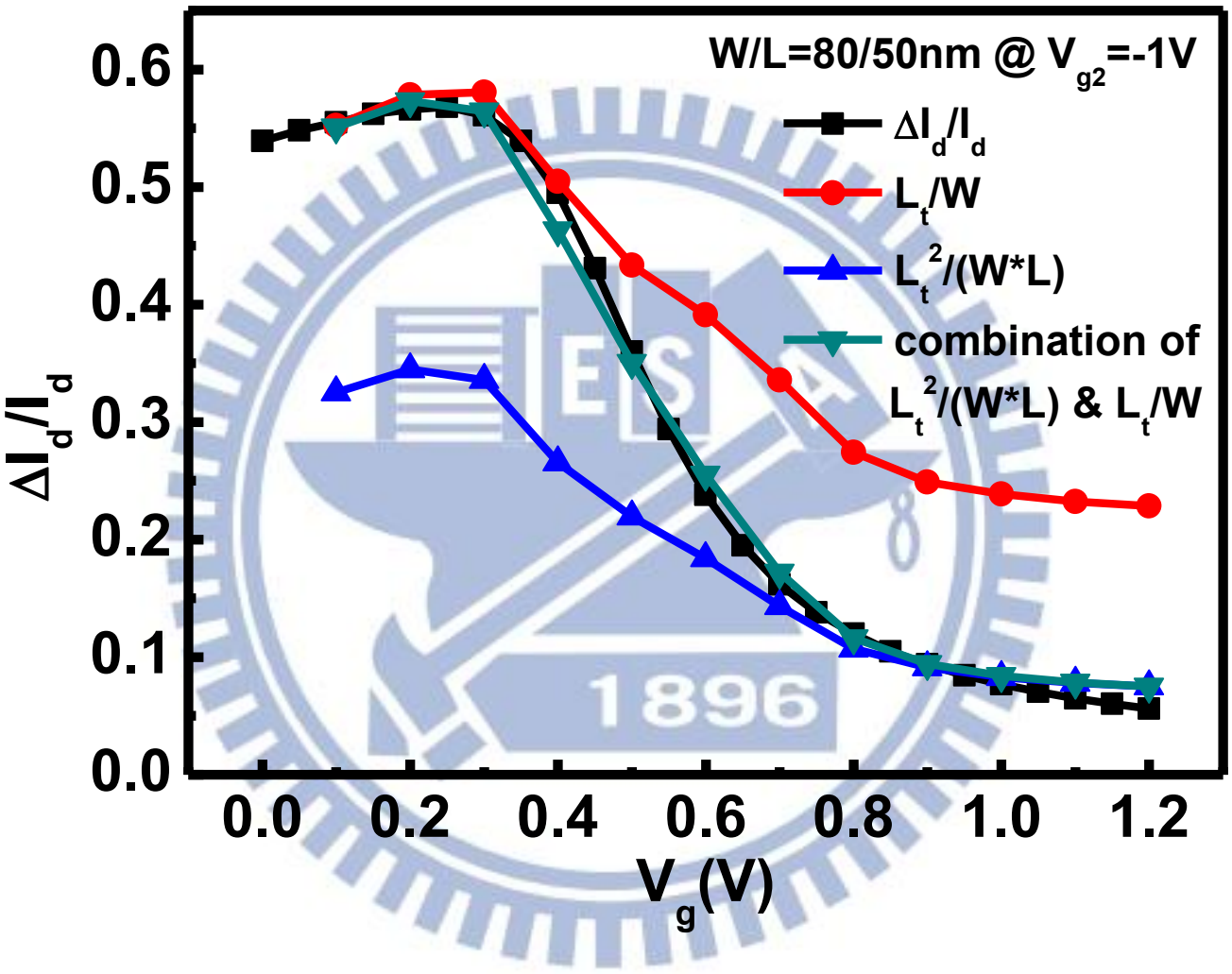


Fig. 17 $\frac{L_t}{W}$ and $\frac{L_t^2}{WL}$ combined by a single formula $\frac{\Delta I_d}{I_d} = \frac{\frac{L_t}{W} - \frac{L_t^2}{WL}}{1+e^{(V_g - V_{g0})/dV}} + \frac{L_t^2}{WL}$ and its fit to $\Delta I_d/I_d$ curve.

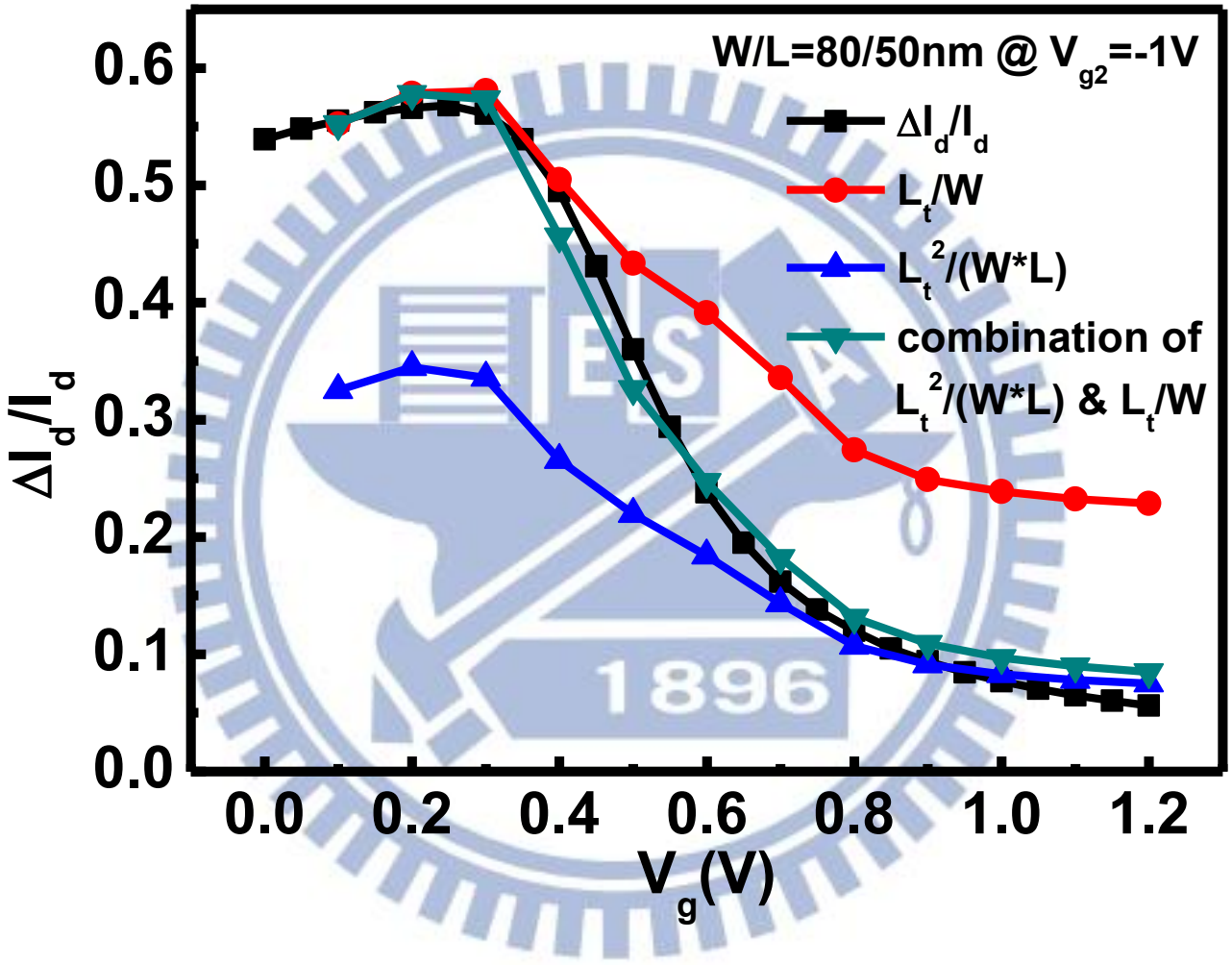


Fig. 18 $\frac{L_t}{W}$ and $\frac{L_t^2}{WL}$ combined by a single formula $\frac{\Delta I_d}{I_d} = \frac{\frac{L_t}{W} - \frac{L_t^2}{WL}}{1+\frac{N_s}{N_{s0}}} + \frac{L_t^2}{WL}$ and its fit to $\Delta I_d/I_d$ curve.

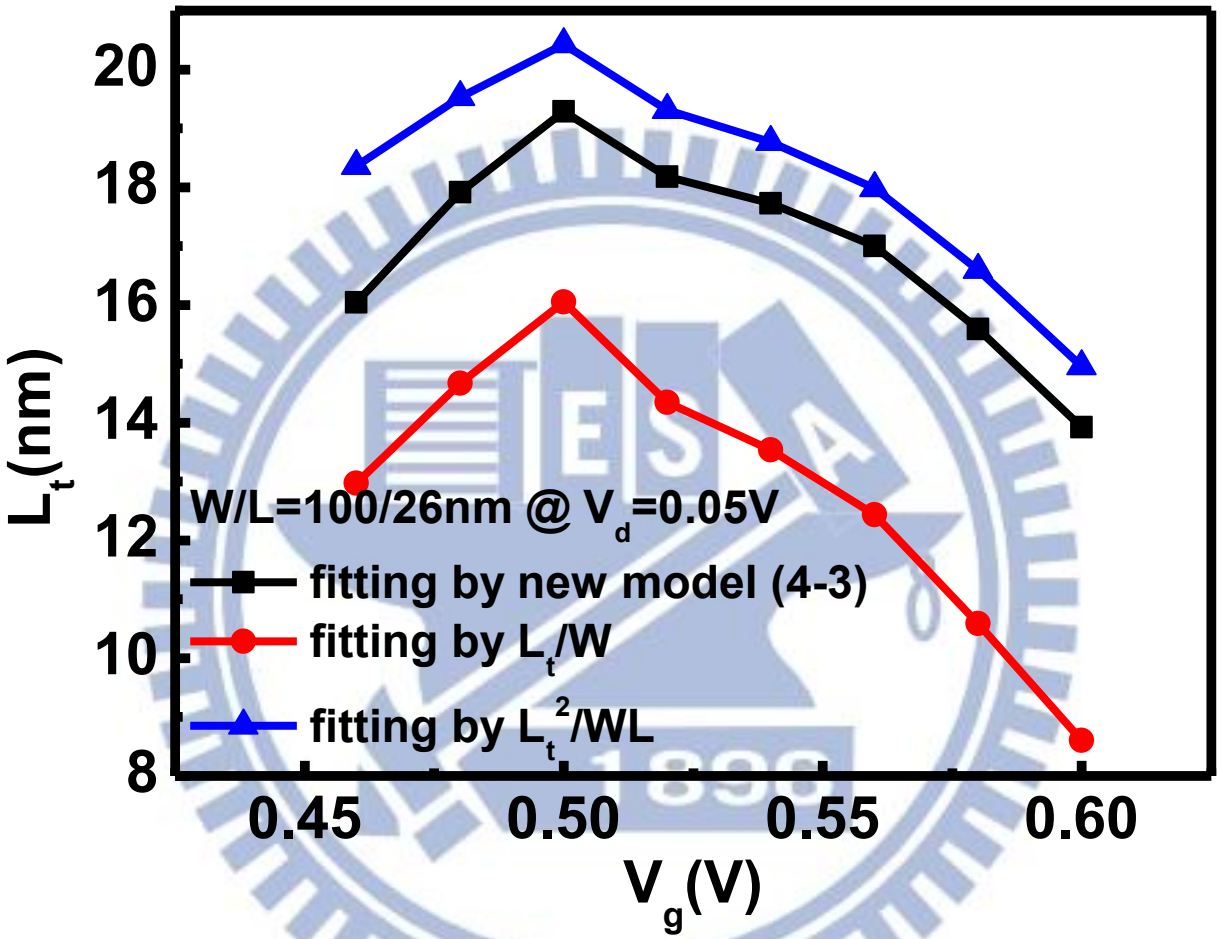


Fig. 19 L_t curve derived by $\frac{\Delta I_d}{I_d} = \frac{L_t}{W}$ and $\frac{\Delta I_d}{I_d} = \frac{L_t^2}{WL}$, as well as our new fitting model (4-3).