國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

α-IGZO 薄膜電晶體的製作與特性分析

Fabrication and Characterization of α-IGZO Thin Film Transistors

研 究 生：顏同偉

指導教授：林鴻志　博士

黃調元　博士

中 華 民 國 一〇〇 年 六 月

α-IGZO 薄膜電晶體的製作與特性分析

Fabrication and Characterization of α-IGZO Thin Film Transistors

研 究 生：顏同偉　　Student：Tung-Wei Yen

指導教授：林鴻志　博士　　Advisors：Dr. Horng-Chih Lin

黃調元　博士　　Dr. Tiao-Yuan Huang

國 立 交 通 大 學

電子工程學系　電子研究所碩士班

碩 士 論 文

A Thesis

Submitted to Department of Electronics Engineering & Institute of Electronics

College of Electrical and Computer Engineering

National Chiao-Tung University

in Partial Fulfillment of the Requirements

for the Degree of

Master of Science

in

Electronics Engineering

June 2011

Hsinchu, Taiwan, Republic of China

中 華 民 國 一〇〇 年 六 月

α-IGZO 薄膜電晶體的製作與特性分析

研究生 :顏同偉　　指導教授 : 林鴻志 博士

黃調元 博士

國立交通大學

電子工程學系　　電子研究所碩士班

摘要

在本篇論文中，我們成功利用射頻濺鍍的方式製造出α-IGZO 薄膜電晶體。由於射頻濺鍍擁有製程溫度低、大面積均勻性佳的薄膜特性，使得此項技術成為製作α-IGZO 通道層的主要方法。我們藉由調整α-IGZO 薄膜沉積製程參數，包括氧氣流量和製程功率控制，進行製作α-IGZO 通道層應用於薄膜電晶體的元件特性分析，以得到適切的製程參數。然後對利用適切的製程參數製作的α-IGZO 薄膜電晶體進行後段熱退火，或增加一層高摻雜濃度的 IGZO 薄膜於源/汲極和 α-IGZO 主動層之間，以了解其對於元件特性的影響。

此外，在適切的α-IGZO 薄膜電晶體上利用變溫量測來探討於元件電性的穩定性。最後，我們也發現在不同製程參數下所製作α-IGZO 通道層的薄膜電晶體擁有不同大小遲滯現象，因此對於遲滯現象而言，其α-IGZO 通道層的製程參數有顯著的影響。

Fabrication and Characterization of α-IGZO Thin Film Transistors

Student : Tung-Wei Yen Advisors : Dr. Horng-Chih Lin

Dr. Tiao-Yuan Huang

Department of Electronics Engineering and Institute of Electronics

National Chiao Tung University, Hsinchu, Taiwan

Abstract

In this thesis, we have successfully fabricated α-IGZO TFTs by depositing the channel films with a radio frequency (RF) sputter. Because the RF sputters have merits of low manufacture temperature and good uniformity on a large scale, making this deposition technique highly suitable for fabrication of the α-IGZO devices. In this thesis, the impacts of the deposition conditions, such as oxygen flow and deposition power, on the properties of the α-IGZO films are carefully explored in order to find suitable manufacture parameters. And then, the α-IGZO TFTs fabricated with the suitable manufacture parameters were subjected to different post annealing treatments to study the effects of the treatments. Moreover, effects of an n^+ layer inserted between S/D metal and α-IGZO channel are demonstrated to be useful for enhancing the device's output performance.

We've also investigated the temperature stability of the devices by measuring the device characteristics at different temperatures. Finally, the hysteresis properties of α-IGZO TFTs are addressed and verified that the deposition parameters of the α-IGZO channel layer have a significant impact on the hysteresis window.

Acknowledgement

Yes!!! 終於換我要畢業了，很快的，整整 18 年的學生生涯要告一個段落了，在研究的這段時間所學到的不僅僅是知識的學習和研究的技巧，還有更多做人處事的道理，謹言慎行，雖然我離真正厲害的做學問人還差了十萬八千里，不過在這些日子的訓練下來，雖然還有很多不懂，不知道的地方，但我會誠實得面對自己，勇敢面對問題，並解決問題，這是我在交大這個大寶庫所學到的。

在 ADTL 的時光裡，我先要特別感謝兩位指導教授，林鴻志 教授以及黃調元 教授，由於你們對於學生有著一定的堅持與把關，我才能有所收穫與成長，懂得去學習觀察問題，畢竟有你們，我才能真正在研究所學到該有的一些知識與態度，在這裡非常謝謝你們的指導。

另外，對於 ADTL 的所有夥伴，包含林哲民學長、蔡子儀學長、林政頤學長、郭嘉豪學長、李克慧學姐，感謝你們在實驗上和元件分析上對我所有的指導與幫忙！還有同屆的夥伴們，歷樺、宇賢、嘉文、段凱、崇名、孝雄，還有 my lover 俊鵬，有實驗室大家的陪伴、玩鬧和閒聊，讓我更加了解大家並且紓解自己做實驗的壓力，雖然我愛人先跑去 tsmc 也拋棄我了，但是我還是很愛你的!! 哈哈~也希望大家的實驗和論文都能順順利利的。當然還有一群很特別的碩一學弟妹們，我相信 ADTL 會更有生氣與活力，未來也請多多加油了!祝你們都能如期畢業。另外，也謝謝明新科技大學的:李億興老師、 偉哲、葉昀在實驗上的協助和幫忙。

另外，我還要感謝我的同學 and 室友們:佳信(賤王)、崇威(野人)、新鈞(楊宗緯)，有你們的陪伴和垃圾話，每次都讓我很開心，雖然每次我都被垃圾話攻擊到體無完膚，不過大家開心笑笑就好。雖然我是說好的博士班逃兵，SORRY，希望佳信和崇威的博士班生活能過的紮實和精彩，每年都能發 IEDM 和 APL。而新鈞呢，家裡很溫暖啊，幹嘛都不回家，實驗固然重要，但身體也很重要啊，你是我們家的無敵鐵金剛，PIE 真的很適合你，祝你快點嫁給美嫻!! XDD 還有一群小學以來的好兄弟、好朋友們，謝謝你們的陪伴，我愛大家!

另外，我最想感謝的是我的父母:顏榮珍 先生、曾美惠 女士，以及我真正的 lover，陳筱函 Lady，沒有你們，沒有今天的我，我希望你們知道，我所做的一切努力，都是為了你們，沒有你們，我不會有如此的好勝心以及積極的態度，一切只希望你們能夠幸福快樂，不要為我而擔心。同樣的，我也希望你們能因為有我而引以為傲，是你們引領著我，讓我想要為了你們而努力，想要讓你們感到有我而覺得開心與驕傲，非常感謝你們對我的照顧與栽培!

最後，這篇碩士論文和畢業的喜悅也分享給我的阿公，突然生病的他，現在還在跟病魔奮鬥，讓我體會到人生的無常，應該更加積極的活在當下，希望你的病情能更加的穩定，能夠快點康復起來與我一起分享這項喜悅。

顏同偉

誌於 風城交大

2011 年 6 月

Contents

List of Figure Captions

Chapter 1

Chapter 2

Chapter 3

Chapter 1

Introduction

1.1 General Background of Metal-Oxide-Based Thin-Film Transistors

With fast growth of consumer electronic market, the displays with light weight, slim, high resolution, low power consumption and high electrical performance have been substantially implemented to various commercial electronic products. At present, thin-film transistors (TFTs) device technologies used in flat-panel displays, such as liquid crystal display (LCD) and organic light emission displays (OLEDs), are mainly amorphous silicon (α-Si) TFTs and low-temperature poly silicon (LTPS) ones. However, the field-effect mobility (μ_{FE}) of α-Si TFTs is only 0.1~1 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and can't be applied to high speed logic circuitries. Although the LTPS TFTs have a much higher mobility up to 100 $cm^2 \cdot V^{-1} \cdot s^{-1}$, the higher fabrication cost as well as the issues associated with the grain boundaries contained in the channel layer limit their application to small-area version.

In recent years, many groups in the world start to explore alternative TFT technologies which can be manufactured at low temperatures and provide intriguing properties such as higher aperture ratio and high mobility. Metal-oxide semiconductor material is one of the possible candidates of channel material to solve the problems mentioned above in the silicon-based TFTs. Table 1.1 compares the properties of silicon-based TFTs with metal-oxide ones. Actually the metal-oxide TFTs have

attracted a lot of attentions in the fields of active-matrix liquid crystal display (AMLCD), e-paper, touch-screen technology, and flexible electronics [1-3], because they are transparent and can be fabricated at low temperatures. In 2003, Hoffman, a professor at Oregon State University, had demonstrated the first zinc oxide (ZnO) transparent TFTs (TTFTs) on a glass substrate [4] with excellent on-off ratio of 10^7 and μ_{FE} of around 2.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$. The transmittance in the visible light wavelength (400 nm~700 nm) is about 75%. In the next year, Hosono's group [5] showed an amorphous indium-gallium-zinc oxide (α-IGZO) film deposited on a polyethylene terephthalate substrate at room temperature exhibiting a Hall mobility exceeding 10 $cm^2 \cdot V^{-1} \cdot s^{-1}$. Such a value is an order larger than that of hydrogenated α-Si devices and is stable under repetitive bending test of the plastic substrate. Moreover, the high transmittance rate can effectively increase the aperture ratio of the device in a pixel. ZnO and α-IGZO both have wide band gap (above 3eV) [4, 6], therefore it would not have high photo-induced leakage current as visible lights irradiate the panel.

To develop TTFTs, we need to find suitable materials from the viewpoints of chemical bonding and electrical structure so that the devices can operate with better performance, such as good on-off current ratio (10^6) and μ_{FE} (~10 $cm^2 \cdot V^{-1} \cdot s^{-1}$) [7-8]. In 1996, Hosono *et al*. had proposed a hypothesis about how to choose the channel materials of TTFTs. The hypothesis predicts that the preferred metal-oxide film should be composed of heavy metal cations (HMCs) with an electron configuration $(n\text{-}1)d^{10}ns^0$ $(n \geqq 4)$ [1-3]. From Fig. 1.1, it shows that the possible elements which can use in metal-oxide film. Some elements are poisonous for human body, for example mercury (Hg), arsenic (As) and cadmium (Cd). Indium (In) is rare in the earth crust. Therefore, how to choose the suitable element from the HMCs is essential to the development of metal oxide TTFTs.

For most wide bandgap semiconductors, the valence band is formed by the *2p*

orbits of occupied oxygen. However, the bottom of conduction band is mainly constructed by the orbit of unoccupied metal cations. The unoccupied *s* orbit of HMCs is isotropic; if the crystal structure allows the HMCs to be close to each other and generate sufficient orbit overlap, the mobile paths of electrons can be formed. Fig. 1.2 shows that the carrier transport difference in crystalline and amorphous semiconductor. In covalent semiconductors such as α-Si the transport paths are composed of strongly directive sp^3orbitals, therefore structure randomness would greatly affect the orbital overlap and degrade the carrier mobility. In contrast, amorphous metal-oxide semiconductors (AMOS) are composed of post transition HMCs which provides spherical *s* orbital. The overlap of HMCs' orbitals and the oxygen's *2p* orbitals is rather large, and is not significantly affected even in an amorphous state [5]. As a result, AMOS has higher mobility.

ZnO [4, 9-12], α-IGZO [5, 7-8], aluminum-zinc oxide (AZO) [13-15], and indium-zinc oxide (IZO) [8, 16] are the materials that have been widely studied in recent years. ZnO and AZO films are polycrystalline, the film uniformity and controllability of the device characteristics are the issues that need to be concerned. General requirements for TTFTs include (1) good stability and uniformity, (2) low manufacture temperature, (3) excellent device characteristics, (4) low carrier concentration (10^{15} to $10^{20}cm^{-3}$) in the channel for the purposes of suppressing the off-current and control of threshold voltage (V_{th}) [8]. From literature survey, we choose α-IGZO TFTs as the major subject to study in this work. The reasons are following:

First of all, we could control the carrier concentration of the deposited α-IGZO film. A higher indium (In) content is expected to enhance μ_{FE} and promote the on current by a significant increase in the carrier concentration [17]. The gallium (Ga)-rich film suppresses the carrier generation because *Ga-O* has stronger strength

than *In-O* bonding and is effective in suppressing the formation of oxygen vacancy [17-18]. Thus, an appropriate addition of Ga is an effective way to attain lower off current and carrier concentration. The zinc (Zn) contributes to the reduction of shallow tail states [19] below the conduction band and interface states between gate oxide and channel, thus the sub-threshold swing (SS) would be reduced. Secondly, the α-IGZO films have the potential for better TFTs performance and stability than polycrystalline films because the films are free from grain boundaries in the channel. However, if the Zn composition of an α-IGZO film is too high, it tends to change the film texture from amorphous to polycrystalline which would draw some negative effects on device properties due to the existence of grain boundaries [18]. Finally, the higher μ_{FE} for α-IGZO films deposited at or slightly above room temperature (RT) is another major merit.

1.2 Overview of α-IGZO TFTs

There are many deposition methods available for forming the α-IGZO active channel in α-IGZO TFTs. Table 1.2 shows the advantages and disadvantages of different deposition techniques. Among them, pulse laser deposition (PLD) [5, 8, 20-21] and sputter are the most common deposition methods. PLD has fast deposition rate and high composition similarity between target and deposited films, but the cost of equipment, contamination and the difficulty to large scale deposition constrain its feasibility in commercial electronic products. Although sputter technique has limitations associated with the relatively low deposition rate, its good uniformity on large scale, precise composition control between target and deposited films and lower manufacture cost make it a suitable tool. Types of sputters can be divided into direct current (DC) sputters and radio frequency (RF) sputters. DC sputters are used to

deposit films with excellent electrical conductivity such as metal, while RF sputters are used to deposit insulating materials. Both DC [22-23] and RF sputters [7, 17-18] have been adopted to deposit α-IGZO films and used as the channel in the fabrication of α-IGZO TFTs.

In essence, to optimize the quality of α-IGZO film is important to achieve excellent device characteristics of α-IGZO TFTs. For sputtering deposition there are many process parameters such as power, deposition temperature, oxygen partial pressure, working pressure and the composition of IGZO target, that need to be considered. Different deposition conditions may result in different amount of oxygen vacancies which would release free electrons in the film. The HMCs and oxygen bonding (*M-O*) have the probability to break and restructure during the deposition, which in turn would induce oxygen vacancies. When the metal atom and oxygen come close, charge transfer occurs due to the different electron affinity of these atoms. We can use the following formula to represent the phenomenon during the deposition of α-IGZO film.

$$M - O + M - O \rightarrow M - O - M + \text{oxygen vacancy} + 2e^{-}, \qquad \text{(Eq. 1-1)}$$

In other words, the more oxygen vacancies the α-IGZO film has, the higher carrier concentration the film contains. Therefore, we need to carefully adjust the above deposition parameters to optimize the device characteristics in terms of a high μ_{FE}, steep SS, low V_{th} and large on-off current ratio. The device characteristics of α-IGZO TFTs deposited at room temperature reported in most of publish papers are not worse than those deposited at a high temperature. In addition, the passivation layer which directly contact with the channel film region, such as hydrogenated silicon nitride (SiN_x), would highly reduce the channel resistivity by enhancing carrier concentration and forming nearly ohmic contacts to reduce the parasitic source to drain resistance [24]. Hydrogen atoms diffusing into the α-IGZO film may act as donors to contribute

free electrons. This indicates that a low channel resistivity at contact interface is necessary to obtain good ohmic contact.

The nonlinearity of the output characteristics of the α-Si TFTs is caused by large contact resistances between the source/drain electrodes and the channel film. Similar effects have been observed in α-IGZO TFTs. The voltage drop across the contact should be small compared to the voltage drops across the active region and metal electrodes. The multilayer electrode structures such as titanium (Ti)/Al and Ti/Au are often used to decrease the contact resistance and improve the adhesion of channel and electrode.

Furthermore, argon (Ar) plasma treatment at source and drain metal contact regions in α-IGZO channel film also improve the contact resistance [25]. Different plasma treatments in various ambient, such as hydrogen (H_2), oxygen (O_2), nitrogen (N_2) and nitrous oxide (N_2O), are also investigated. For instance, hydrogen atoms serve as donors in hydrogen plasma treatment [25], O_2 plasma would cause oxygen adsorption onto the channel film and lead to the creation of acceptor-like states [26] which trap the conducting electrons in α-IGZO film, and N_2 plasma can break the bonding of HMCs and oxygen to generate free carriers [27]. Different post annealing environment [18, 28-29] and laser annealing [30-31] were also used to enhance and control device characteristics by reducing the channel resistivity and bulk defects.

AMOS research has made a large progress in the past few years, but the fundamental carrier transport mechanism and material properties are still not well known because of their complexity. Kamiya *et al*. had observed unusual behaviors in temperature dependences of free electron density and mobility for α-IGZO and crystalline IGZO (c-IGZO) [32]. For example, μ_{FE} at RT enhances with increasing carrier concentration. This is totally different from conventional crystalline semiconductors because of ionic impurity scattering. They proposed that the

percolation conduction is more suitable to explain the carrier transport properties observed in α-IGZO film [32, 34-35]. The basic theory of percolation conduction is that for electrons there are different mobile paths that exhibit different carrier transport properties. From Fig. 1.3 [32], electrons would take low barrier height and a winding path at a low temperature because the transmission probability is limited by the Boltzman factor which is expressed as

$$e^{-e\emptyset/k_BT}, \qquad \text{(Eq. 1-2)}$$

Electrons will take a shorter and straight path at higher temperature even a higher potential barrier height is encountered [32, 35-36]. On the other hand, Fig. 1.4 shows that Fermi level below or above the edge of the conduction band presents another way to describe the percolation and degenerate conduction mode [37].

To understand the subgap density of states (DOS) is important to improve the α-IGZO TFTs characteristics. The strained and disordered chemical bonds form deep and localized states between the conduction band minimum and the valence band maximum. These states act as trapping centers for electrons. The α-IGZO TFTs with the channel film deposited with different conditions have different subgap DOS. The larger DOS observed in the depletion-mode TFTs than in the enhancement-mode is explained by the larger density of donors in the depletion mode TFTs [36]. The annealed TFTs have smaller DOS, reduced defect density and shallow defects. Different methods were proposed by different groups to extract DOS, such as capacitance-voltage (C-V) characteristics of TFTs [38-39], simulation [40] and charge pumping [41]. A low density of subgap traps is important for reducing the SS and operation voltage of α-IGZO TFTs.

1.3 Motivation and Objective of this Thesis

Based on the successive research and innovation in recent years, metal-oxide TFTs may offer an attractive alternative for replacing silicon-based TFTs. Metal-oxide TFTs may even have the potential to the manufacturing of the consumer electronic products in the future. Nonetheless, from the historical background stated above, more efforts in understanding the effects of the film composition and the process treatments on the properties of the channel films are still urgently needed. In this thesis α-IGZO TFTs were fabricated and characterized with homemade α-IGZO targets. The advantages of homemade α-IGZO targets are low cost and the ability to tailor the composition of In:Ga:Zn. One of the objectives of this thesis is to find the best composition in the α-IGZO target in order to obtain the best device characteristics. Furthermore, by varying the composition of the α-IGZO target, we can compare and study the impacts drawn by different metal elements in the channel film. Since this is the first work on the metal-oxide TFTs conducted in our group, we also intend to optimize the device manufacture parameters and develop a fabrication technique of bottom-gate α-IGZO TFTs.

1.4 Organization of this Thesis

In Chapter 2, we present the fabrication of the n-type α-IGZO TFTs by describing the basic process flow The measurement setups employed for device characterization are also presented in this chapter.

In Chapter 3, we present and discuss the electrical characteristics of the fabricated devices, including the on-off current ratio, μ_{FE}, SS and V_{th}. The impacts of the deposition power and oxygen flow on the device characteristics will be discussed respectively. Also, we investigate the effects of various post treatments on the

electrical characteristics of the devices. Effects of an n^+ layer inserted between the α-IGZO channel region and source/drain metal contact are also studied.

Finally, we summarize the concluding remarks from our experimental results and the suggested future work in Chapter 4.

Chapter 2

Device Fabrication and Measurement Setup

2.1 Manufacturing Process of IGZO Targets and Characteristics of Deposited IGZO Films

In this study, the composition of the IGZO powder used in the experiment was mixed by an atomic ratio of In:Ga:Zn = 1:1:1. The target powder (In_2O_3, Ga_2O_3, ZnO) with high purity was purchased from Optotech Materials Co. The powders were then milled, followed by calcining at 1000°C for 1 hour. Next, the powders were ground and sieved through a 250-mesh screen. Afterwards, the material was further formed into the sputter target under a pressure of 60,000-70,000 kg/cm^2 at 1250°C for 60 minutes in Ar ambient.

After the IGZO target was formed, we mounted it in the sputter chamber for the deposition of IGZO thin films on glass substrates. Table 2.1 shows the major process parameters of the deposition. Certainly the process conditions may affect the properties of the deposited material, such as the atom ratio of deposited α-IGZO film and the deposition rate. In this work, we used n&k analyzer to measure the thickness of IGZO thin film. The atom ratio of the deposited α-IGZO films was investigated by X-ray photoelectron spectroscope (XPS). The surface roughness was investigated by atom force microscope (AFM). From Fig 2.1, we can see that higher deposition power has faster deposition rate owing to the higher sputter yield. However, the mean free

path of the sputtered species could be reduced as a higher oxygen partial pressure is implemented and, as a result, the deposition rate is slower. Form the X-Ray Diffraction (XRD) material analysis of IGZO films which was deposited in RT, we found out that the IGZO film without post annealing is always in amorphous state regardless of the deposition conditions.

2.2 Device Fabrication and Process Flow

In the section, we introduce the basic process flow of the α-IGZO TFT devices. The device structure belongs to the inverted-staggered type, which is the most commonly used structure for active matrix liquid crystal display (AMLCD). Figure 2.2 shows the schematic process flow for fabricating the devices. It can be seen that the α-IGZO TFT device was fabricated on the surface of a silicon dioxide film thermally grown on a silicon substrate. For fabricating this structure, a 100 nm Al-Si-Cu was first deposited by physical vapor deposition (PVD) as gate electrode and patterned by wet etching (Fig. 2.2(a)). Then, a 100 nm TEOS oxide was deposited by plasma-enhanced chemical vapor deposition (PECVD) as the gate dielectric (Fig. 2.2(b)). It is worth noting that before depositing the α-IGZO active layer, we had to pre-sputter the target for 15 minutes to prevent the contamination of IGZO target surface. Subsequently, a 50 nm α-IGZO film was deposited as the channel layer by the RF sputter at room temperature under different deposition power and oxygen partial pressure (Fig. 2.2(c)). The atomic ratio of IGZO target was In:Ga:Zn=1:1:1. The system's base and working pressures were 3×10^{-6} Torr and 5 m Torr, respectively. During sputtering, the flow rate of Ar was fixed at 50 standard cubic centimeter per minute (sccm), while the oxygen flow was set at 1sccm, 3sccm, or 5sccm, with oxygen partial pressure of 9.8 $\times10^{-5}$, 2.83 $\times10^{-4}$ or 4.54 $\times10^{-4}$ Torr, respectively, all

with a fixed deposition power (100W). The oxygen partial pressure was derived from $O_2/(Ar+O_2)$ × working pressure. In this work, we also explored the effect of the RF power by setting the power at 100, 125, 150, 200W at constant Ar/O_2 gas mixing ratio (50/1) and oxygen partial pressure of 9.8 $\times 10^{-5}$ Torr. After the α-IGZO channel film was deposited, an optional n^+ α-IGZO layer and a source/drain metal were deposited using lift-off process (Fig. 2.2(d)). The optional n^+ α-IGZO layer allows us to compare the electrical characteristics of devices with and without it. Such an n^+ α-IGZO film was deposited without flowing the oxygen during sputtering. The source/drain metal was a 300 nm Al/Ti metal compound which was deposited with deposition power fixed at 75W by a DC sputter and the working pressure was 3 m Torr (Fig. 2.2(e)). Afterwards, we performed a lithographic step to define the active device region (Fig. 2.2(f)). Since the etching rate of the α-IGZO with hydrochloric acid (HCl) was too fast, we used a diluted HCl solution (HCl: H_2O = 1:200) instead to avoid damage and severe lateral etching of the α-IGZO channel film (Fig. 2.2 (g), (f)). In order to contact the gate electrode, contact etching was performed by wet etching using buffer oxide etcher (B.O.E.). Fig. 2.2 (i) and Fig. 2.2 (j) show the cross-sectional views of the α-IGZO devices without and with the n^+ α-IGZO layer.

2.3 Measurement Setup

In our study, electrical measurements of all devices were executed by an HP4156A precision semiconductor parameter analyzer, and the measurement temperature was maintained at 25°C. Prior to the measurements, all α-IGZO TFTs samples used in this study were annealed at 200 °C for 40 minutes on the hot plate aiming to remove the excess moisture on TFTs.

The basic electrical parameters of the fabricated device were extracted from the

electrical characteristics. Note that the threshold voltage (V_{th}) was not extrapolated from the I_d-V_g curves, rather, the V_{th} was defined in this work as the value of V_g when I_d equals 1nA × $\frac{W}{L}$ under V_d of 0.1V, where W and L are the channel width and the channel length, respectively, as estimated from the patterns of the mask. The subthreshold swing (SS) was calculated by the following equation:

$$SS = \frac{d\log(I_d)}{dV_g} \quad , \qquad \text{(Eq. 2-1)}$$

the minimum SS value was extracted in the drain current region between 10^{-9}A to 10^{-12}A. The transconductance (G_m) was also extracted from the I_d-V_g curves, and we could calculate the linear μ_{FE} by the following equation with V_D=0.1V:

$$\mu_{FE} = \frac{L \cdot G_m}{W \cdot C_{OX} \cdot V_D} \, . \qquad \text{(Eq. 2-2)}$$

For on-current (I_{on}), the value was defined as the I_D when $V_G - V_{th}$ = 8V at V_D=10V.

Chapter 3

Results and Discussion

3.1 Effects of Deposition Conditions

3.1.1 Introduction

α-IGZO channel layers are usually deposited by sputters because of the low deposition temperature and thus the feasibility for manufacturing of devices on flexible substrates. It is well known that the properties of amorphous metal oxide semiconductor materials are strongly dependent on the processing conditions. In this regard, there had been several reports exploring the effects of deposition power [29], oxygen flow [18, 29] and working pressure [18], on the basic electrical characteristics of α-IGZO TFTs. The analysis of different process parameters are the major object of this section with an intent to acquiring suitable process parameters for deposition of α-IGZO layers with superior properties. In particular, the impact of different sputtering parameters is investigated.

3.1.2 Effects of Deposition Power

Figures 3.1(a)~(d) show the transfer characteristics of the α-IGZO devices deposited with deposition power of 100W, 125W, 150W and 200W, respectively, at a constant oxygen flow of 1sccm. In each figure at least 10 devices were measured in order to understand the uniformity of the characteristics. Overall the uniformity of the manufacture process is good as can be seen in the figures. Typical device characteristics of each split are put together in Fig. 3.2 for comparison. Some clear

trends are shown in the figures. First, the transfer curve is shifted to the left with increasing sputtering power. Second, a higher deposition power results in larger off-state current. The extracted V_{th}, SS, and on-current for each split are shown as a function of channel length in Figs. 3.3(a), (b) and (c), respectively. In Fig. 3.3(a) it is seen that the variation of V_{th} is reduced with increasing deposition power, though the trend of SS seems not clear in Fig. 3.3(b). As shown in Fig. 3.3(c), the on-current measured at the same gate overdrive is higher as the deposition power increases. It is known that the In^{3+} cations in α-IGZO channel film would extend the conduction band minimum and reduce the effective mass of the conduction electrons which would enhance μ_{FE} and reduce the resistivity of the α-IGZO film [17]. Moreover, the V_{th} is negatively shifted by increasing the carrier concentration. However, the carrier concentration of α-IGZO channel film is controlled by oxygen vacancies and the incorporated In concentration.

Table 3.1 shows that the value of In/(In+Ga+Zn) ratio of the deposited films which increases with increasing deposition power. The concentration of these metallic compositions was obtained with the XPS technique. The dependence of the In/(In+Ga+Zn) ratio on the deposition power is postulated to have a strong influence on device characteristics including V_{th}, μ_{FE}, carrier concentration and off current [17, 42]. However, as shown in Fig. 3.3(b), the SS is slightly deteriorated at a higher deposition power. This indicates that the interface traps between gate oxide and α-IGZO channel layer are not seriously affected by the deposition power. Fig. 3.4 shows that the field-effect mobility (μ_{FE}) extracted from the transconductance enhances with increasing deposition power. The μ_{FE} for the devices processed at a lower deposition power is slightly reduced as the channel length is shorter than 20μm. It is postulated to be related to the effect of the S/D parasitic resistance in these

devices with a shorter channel length. Next, this issue is clarified by measuring the resistance components in the devices.

The total resistance (R_{total}) as a function of channel length can be evaluated by using the total resistance method conducted in the linear region [24]:

$$R_{total} = \frac{V_D}{I_D} = \frac{L}{\mu_{FEi} \cdot C_{OX} W \cdot (V_G - V_{th})} + R_{SD}, \qquad \text{(Eq. 3-1)}$$

where C_{ox} is the oxide capacitance, W is the channel width, L is the channel length, μ_E is the effective mobility and R_{SD} is the S/D parasitic resistance. From this equation, we can evaluate μ_E and channel resistance per micrometer as a function of gate overdrive, and the results for devices with L/W = 100/400μm characterized at V_D= 0.1V are shown in Fig. 3.5(a). The extracted resistance components are shown in Fig. 3.5(b). The measured R_{SD} values are in the range from 3.5 to 6.7 kΩ, more than one order in magnitude smaller than the channel resistance in this case. On the other hand, the results for a device with a short channel length of 10 μm are shown in Fig. 3.6. In this case the extracted R_{SD} values are comparable to that shown in Fig. 3.5(b). However, due to the ten times smaller in channel length, the channel length is significantly reduced. As a result, the impact of the R_{SD} on device characteristics is no longer negligible in the short-channel devices.

In Figs. 3.7(a) and (b), it is seen that the channel resistance decreases while μ_E increases, respectively, with increasing gate overdrive voltage. It is obvious that a higher gate overdrive voltage induces more free electrons to transport in α-IGZO channel layer which is the main reason for the reduced channel resistance. On the other side, the more induced electrons would reduce the potential barrier for carrier conduction [32, 34-37]. As has been introduced in Chap. 1, the electrical behavior of the α-IGZO TFTs can be explained by a percolation model. As shown in Fig. 1.4(b), as the Fermi level is manipulated by the gate bias in the degenerate state, shorter

carrier transport paths around the valley of energy barrier could be formed as the gate voltages increases. The output characteristics of the devices with different deposition power are shown in Fig. 3.8. The differences among the splits in on-current at the same gate overdrive voltage are obvious.

3.1.3 Effects of Oxygen Flow

Figures 3.9(a) and (b) show the transfers characteristics of several α-IGZO devices with oxygen flow of 3sccm and 5sccm, respectively, at a constant deposition power of 100W. As compared with the results shown in Fig. 3.1(a) for the split with oxygen flow of 1sccm, the variation in device characteristics is not worse. Fig. 3.10 shows the typical transfer curves of the three splits. As described in Chap. 1, oxygen vacancies are the main source to release free electrons to transport in the metal-oxide semiconductors. This is clearly confirmed in the figure that the transfer curves are positively shifted with increasing oxygen flow. Therefore, a higher gate voltage is necessary to accumulate free electrons to form a conductive layer between the source and drain. In addition, the extracted electrical parameters are show in Figs. 3.11(a)~(d). Fig. 3.11(a) shows that the V_{th} has a weak dependence on the channel length. This is because the channel length is more than 30x longer than the gate oxide thickness, thus the short channel effects are expected to be small. In Fig. 3.11(b), the SS increases with increasing oxygen flow. It is known that the SS can be affected by the bulk defects in the α-IGZO channel film in addition to the interface traps, thus the reduction in SS might result from the greater densification and lower amount of the bulk defects as deposited at a lower oxygen partial pressure [18, 29, 43]. Fig. 3.11(c) shows the on-current measured under the same gate overdrive voltage of 8V. From this plot, we know that on-current reduces with increasing oxygen flow owing to

deficiency in carrier concentration. Fig. 3.11(d) shows that μ_{FE} is dependent on the channel length. The electrical behavior is similar to that described in pervious sub-section and R_{SD} should have drawn effect on the short-channel devices.

The channel resistance and μ_E extracted from total resistance method are shown as a function of gate overdrive in Fig. 3.12. It is obvious that a higher gate overdrive voltage induces more free electrons to transport in the channel, which is the main reason to reduce channel resistance. Because the deposited α-IGZO channel layer with a higher oxygen flow has less carrier concentration, a higher potential barrier height and longer transport path are expected from the percolation model (Fig. 1.14 (a)). Therefore, the channel resistance and μ_E are higher in the films with a lower oxygen flow. Fig. 3.13 shows the output characteristics of devices deposited with different oxygen flow. Despite the higher resistivity, the ohmic S/D contacts are still formed for the split with high oxygen flow as shown in the output characteristics, attributed to the large S/D contact area. However, the undesirable R_{SD} effects still need to be taken into consideration and solved in practical circuit applications in which the contacts are minimized for performance concern. In order to solve this problem, several methods have been proposed, such as plasma treatment [25-27], post-annealing treatment [28-29] and post-laser annealing [30]. In the next section, we explore an approach which adopts an n^+ insertion layer to improve the device characteristics.

Summary of the major effects of the deposition parameters on the electrical characteristics of α-IGZO TFTs are shown in the Table 3.2. Based on these observed trends, most of the devices characterized in the remaining sections of this thesis were fabricated with the following suitable sputtering parameters: deposition power is 150W, Ar/O_2 gas mixing ratio is 50/1, oxygen flow is 1sccm. Major electrical

characteristics of the fabricated devices are as follows: the V_{th} is 0.66±0.15V, SS is 0.476±0.023V/decade, μ_{FE} extracted by transconductance is 10.22±0.36 cm^2/Vs, and the on-current is $2.09\pm0.03\times10^{-5}$A at V_G-V_{th}=8V and V_D=10V.

3.2 Effects of the Insertion n^+ Layer between Source/Drain and the Channel

Deposition conditions of the n^+ insertion layer are described in Chap. 2. It is a heavily-doped α-IGZO layer which has a high carrier concentration in order to reduce the contact resistance of the S/D metal contacts. To confirm this point, we took the Hall measurements to probe the carrier concentration and resistivity of the deposited films. The resistivity of the n^+ α-IGZO layer is 2.85×10^{-2} Ω-cm and the carrier concentration is $1.28\times10^{19}cm^{-3}$. Details about the device fabrication are also given in Chap. 2. To reduce interface defects between the semiconductor layer and metal, the n^+ layer and the S/D metal were deposited sequentially in a sputter with base pressure of 2×10^{-6} Torr.

Fig. 3.14 shows the output characteristics of the α-IGZO devices with and without n^+ layer. From the output performance, we can see that the on-current of α-IGZO devices with n^+ layer is increased by 36% at the same gate overdrive. The transfer characteristics of the two devices are shown and compared in Fig. 3.15. As compared with the device without the n^+ insertion layer, both on and off currents increase with the n^+ insertion layer. The increase in on-current is attributed to the reduction in the parasitic resistance and is consistent with the results presented previously [44]. The main reason is attributed to the thinning of the tunneling width at the S/D contacts due to a high amount of carrier concentration [33]. However, the

causes for negative shift of the threshold voltage and increase in the off current are not clear at this stage, presumably due to the difference in film thickness because of the lack of reproducibility with the homemade sputtering system. Figures 3.16(a), (b), and (c) show μ_{FE}, V_{th}, and on-current of the two splits of devices. Effects of the insertion layer in improving the mobility and on current are clearly illustrated in the figures.

3.3 Effects of Different Annealing Ambient

The ambient for the post-annealing treatment of the fabricated devices was varied and studied in order to understand the effects on the characteristics of α-IGZO devices. The post annealing process is one of the major factors to dictate the electrical behavior because this process can generate or diminish free carriers in α-IGZO channel films and modulate the film's properties. In this study, the annealing ambient employed includes the forming gas ($95\%N_2/5\%H_2$) and nitrogen environment, and the annealing duration is one hour. Fig. 3.17 shows the representative transfer curves after the annealing treatment and Fig. 3.18 compares the extracted electrical parameters. The on-current measured at V_G-V_{th}=8V at V_D=10V are $2.01\pm0.03\times10^{-5}$A, $1.78\pm0.09\times10^{-5}$A and $1.66\pm0.03\times10^{-5}$A for fresh devices and annealed ones done in forming gas and nitrogen gas, respectively. As can be seen in Fig. 3.17 that the transfer characteristics of α-IGZO TFTs are dramatically affected by the annealing ambient. In order to explain these results, we postulate some possible schemes and explore their suitability for the observed electrical behaviors of the annealed samples.

In the α-IGZO films the metal species tend to bond with the oxygen ones. As oxygen vacancies are generated inside the films, more electrons are released. When the α-IGZO structure is annealed in a higher temperature, it generates oxygen vacancies and it is well known that one oxygen vacancy can release two free

electrons.

From the on-current performance, we find that the on-current of devices receiving post annealing treatment is smaller than that of fresh ones. It is postulated that the carrier concentration is reduced by the post annealing process and obviously the film's properties are dramatically affected by the treatments. Accounting for this point, three different possible conditions for the channel films are shown in Figs. 3.19(a) ~(c). Figure 3.19(a) corresponds to the situation of fresh devices in which a homogeneous film is assumed. In Figs. 3.19(b) and (c), we assume that, during the post-annealing treatment, the hydrogen and/or nitrogen atoms presenting in the environment may diffuse into the α-IGZO channel film from the back channel surface and modify the film with a high resistivity. However, in Fig. 3.19(b) it is assumed that thickness of such a modified resistive region is thinner than the original film thickness, while in Fig. 3.19(c) the whole film is modified. From Fig. 3.20, we find that the off-state current is not dependent on gate voltage but on drain voltage. Such a phenomenon implies that the performance of the off-current is related to intrinsic α-IGZO film resistivity which depends on the manufacturing parameters. Based on this hypothesis, the resistivity of α-IGZO channel film by different drain voltage at V_G=-3V can be calculated as follows:

$$R = \frac{VD}{ID} = \rho_{IGZO} \cdot \frac{L}{W \cdot t}, \qquad \text{(Eq. 3-2)}$$

where ρ_{IGZO} is the resistivity of α-IGZO channel film, t is the channel thickness of α-IGZO film, L is the channel length and W is the channel width. Fig. 3.21 confirms the linear relation between drain current and drain voltage for devices receiving different post-annealing treatment. Thus, the reciprocal of slope can be regarded as the resistance of the α-IGZO channel film. From the plots, the calculated resistivity of α-IGZO film without post annealing (the fresh devices) is about 2.11×10^5 Ω-cm. Such

a value can be adopted as the resistivity in the unmodified region in Fig. 3.19(b). Assuming the resistivity of the surface modified region is much higher than that of the unmodified region in Fig. 3.19(b), and the thickness of the unmodified region is t_1, we can estimate t_1 in the post-annealed devices with the following relation:

$$t_1 = \rho_{IGZO}(\text{fresh}) \cdot \frac{L}{W \cdot R}, \qquad \text{(Eq. 3-3)}$$

where R is the resistance for the post-annealed devices extracted from Fig. 3.20. t_1 is about 2.78 nm for the device annealed in forming gas and about 0.39 nm for the device annealed in nitrogen. The latter is so thin that we can regard the film as fully modified as the situation shown in Fig. 3.19(c).

The extracted electrical performance presented in Figs. 3.18(a) and (b) shows indirect evidence supporting the above hypothesis. In Fig. 3.18(a), the V_{th} is increased by the post annealing treatments, and is the highest for the split which received treatment in the nitrogen ambient because the α-IGZO channel film has been transformed into a highly resistive state. In summary, this study shows that the resistivity of post annealed devices is higher than that of the fresh ones, while the transfer curves show positive shift.

3.4 Temperature Instability

For circuit applications, it is also important to consider the electrical stability of α-IGZO TFTs under various gate bias [36, 39], temperature [39, 45-46] and lighting conditions [47-48]. Moreover, the electrical instability also has been reported by several groups that it strongly depends on the gate dielectric/α-IGZO channel interface properties [48-49]. In this section, we evaluate the temperature dependence of electrical behaviors on α-IGZO TFTs having PECVD TEOS oxide as the dielectric material.

The temperature-dependent measurements started at 25°C and increased to 125°C in 25°C increment per step. In order to minimize the measurement errors, 15 minutes hold time at each temperature step was used to ensure a steady state was achieved before the measurement. In Fig. 3.22, the transfer characteristics of α-IGZO TFTs measured at various temperatures from 25°C to 125°C with a fixed drain voltage V_D=0.1V are shown. As can be seen in this figure, the drain current in the off and sub-threshold regions increases with increasing temperature. Figs. 3.23(a) and 3.23(b) show the extracted SS and V_{th} as a function of temperature between 25°C and 125°C. The off and sub-threshold currents in TFTs with ZnO-based multi-component oxide are described by the thermally activated Arrhenius model where it is assumed that the thermally activated electrons from deep level trap states and tailing states are excited thermally into the conduction band and move toward the drain electrode by the lateral electric field [39]. In the metal-oxide semiconductor, the deep level trap states are caused by oxygen vacancies, while the tailing states are caused by the structural disorder of the semiconductor films. It is well known that the extra free carriers of metal-oxide semiconductor are mainly due to the generation of oxygen vacancies. The thermally activated oxygen atoms leave their original position and induce oxygen vacancies (deep states) with the remaining free electrons at the original sites. The activated oxygen atoms become interstitial and affect the electrical performance of α-IGZO TFTs. Therefore, the negative V_{th} shift with increasing temperature and the SS increase with increasing temperature can be understood as the consequence of thermal activation. The SS is deteriorated by the dramatic increase of trap density (N_t) including the density of states (DOS) of the α-IGZO film (N_s) and interface traps (N_{it}) at a higher temperature [43, 46] with the following relation:

$$\Delta N_t = \frac{C_{ox} \cdot \Delta SS}{\ln(10) \cdot kT}, \qquad \text{(Eq. 3-4)}$$

where Cox is the gate capacitance, k is the Boltzman constant, T is the measurement temperature, and ΔSS is the change of SS with increasing temperature.

According to the Arrhenius model [50-51], the drain current (I_{DS}) near the sub-threshold region can be expressed with the following equations:

$$I_{DS} = I_{D0} \cdot e^{\frac{-E_A}{kT}}, \quad \text{(Eq. 3-5)}$$

$$\ln(I_{DS}) - \ln(I_{D0}) = -E_A(\frac{1}{kT}), \quad \text{(Eq. 3-6)}$$

where I_{D0} is the pre-factor and E_A is the activation energy. Fig. 3.24 shows the Arrhenius plots of an α-IGZO device measured at drain biases of 0.1 and 5V. It is well known that, for amorphous-semiconductor TFTs, most of the free carriers induced by the gate electric field go into the tailing states but a small fraction go to the conduction band with higher electric field [52-53]. As shown in Fig. 3.23, the off current and sub-threshold current have strong temperature dependence implying a high activation energy. There have been many reports that the tailing states obey an exponential distribution and the characteristic energy of tailing states has been estimated to be less or comparable to the thermal energy (0.0259eV) at room temperature [33, 39,50-51]. As a result, E_A decreases exponentially as the gate bias increases in the on-state. Under such a situation, the Fermi level moves closer to the conduction band edge until it reaches the tailing states [45]. Thus, the high density of tailing states causes the pinning of Fermi level and reduces the slope, as shown in Fig. 3.24. Furthermore, the activation energy in the off current region is weakly dependent on the gate voltage. The activation energy for α-IGZO devices at different drain voltage (V_D=0.1V and 5V) are 0.13eV and 0.17eV, respectively, which is in contrast to the normal TFTs. This electrical behavior is still unknown and needs to be verified by more experiments.

Fig. 3.25 shows that the on-current of α-IGZO TFTs slightly increases when temperature increases to 75°C, but decreases as the temperature is further increased. In Fig. 3.26, a similar trend is exhibited on transconductance (G_m). These trends can be explained as follows: the enhancement in on-current and G_m is owing to the increase in carrier concentration due to the aforementioned thermal activation process. Nonetheless, as temperature is above 75°C, the mechanism of phonon scattering dominates the electrical performance and results in the degradation.

3.5 Hysteresis Characteristics

Several studies on the hysteresis phenomenon have been reported. In this thesis such an issue is also addressed. In the following analysis, the forward sweep (FS) refers to the sweeping of gate voltage from a negative value to a positive one, and the reverse sweeping (RS) refers to the sweeping in the opposite direction. Difference between the transfer characteristics of the two sweeping modes indicates the extent and effect of the hysteresis. In addition, it has been shown that the kind of gate dielectric used in devices may have effects on the hysteresis [54-55]. In this study, we explore the characteristics of devices with PECVD TEOS SiO_2/α-IGZO channel. Figs. 3.29(a), (b), (c), and (d) show the results of measurements performed on devices with the α-IGZO channel deposited with RF power of 100, 125, 150, and 200W, respectively. The O_2 flow is fixed at 1sccm for these devices. Figs. 3.30(a) and (b), show the results of measurements performed on devices with the α-IGZO channel deposited with O_2 flow of 3 and 5sccm, respectively. The RF power is 100W for the devices. In the figures, the hysteresis loops are clockwise.

The above results are presumably due to the electron trapping in the gate oxide which occurs mainly during the FS so that the Vth shifts positively in the RS curve.

The trapped electrons are injected from the channel into the gate oxide. The process parameters obviously play a role in affecting the hysteresis. The hysteresis window is defined as

$$\text{Hysteresis Window} = V_{th}(RS) - V_{th}(FS), \qquad \text{(Eq. 3-7)}$$

where V_{th} is defined as the value of V_g when I_d equals 1nA × $\frac{W}{L}$ under V_d of 0.1V. Fig. 3.31(a) shows the hysteresis window extracted from Figs. 3.29(a) ~(d) as a function of deposition power. It is seen that the window size shrinks with increasing deposition power. Fig. 3.31(b) shows that the hysteresis window extracted from Figs. 3.29(a), 3.30(a), and (b) as a function of oxygen flow with a fixed deposition power (100W). The hysteresis effect becomes more severe as oxygen flow is used.

During FS, the free electrons are accumulated near the interface by high electric field exerted by the gate voltage, and some of the electrons are injected into the gate dielectric and trapped therein. During RS and even subsequent FS, not all of the trapped electrons would de-trap. V_{th} thus becomes larger. The de-trap rate of the trapped electrons in the gate oxide depends on the trap level and distance from the channel. These properties are affected by the deposition conditions of the α-IGZO channel [55]. More efforts are needed for making these phenomena more clear.

Chapter 4

Conclusion

4.1 Conclusion

In this thesis, we have successfully fabricated and characterized α-IGZO TFTs with the α-IGZO channel layer deposited under various sputtering parameters. As the film was deposited with a higher RF power but a fixed oxygen flow conditions, we observed that the transfer curves are negatively shifted while μ_{FE} is improved without deteriorating the SS. It was confirmed by XPS measurements that the value of In/(In+Ga+Zn) ratio of the deposited films increases with a higher deposition power, presumably the reason that μ_{FE} is significantly enhanced. Moreover, by comparing the characteristics of devices deposited with different oxygen flow and a fixed deposition power, the carrier concentration of the α-IGZO channel is found to be reduced with increasing oxygen flow during sputtering. As a result, the transfer curves are positively shifted and μ_{FE} is significantly decreased. From the electrical results of the α-IGZO TFTs, the deposition power of 150W with oxygen flow of 1sccm was chosen as the sputtering conditions for preparing the α-IGZO channels in this study.

We've also investigated the effects of an n^+ insertion layer between S/D metal and α-IGZO channel layer. In this study, α-IGZO TFTs with the n^+ insertion layer exhibit less S/D parasitic resistance than the ones without n^+ insertion layer, which in turn enhances the on-current. Nonetheless, origins for the accompanying degradation in the off-current and the negative shift of V_{th} remain unclear at this stage. Besides, the changes of transfer performance with the variation of post annealing treatments

have been studied as well. It was observed that the resistivity of the α-IGZO channels receiving the post annealing treatment is higher than the control without the treatment, resulting in an increased V_{th} and mobility degradation.

Temperature-dependent sub-sthreshold characteristics *we*re also observed for the fabricated α-IGZO TFTs. The increase in sub-threshold current in α-IGZO TFTs is well described by the thermally activated electrons. The thermally activated Arrhenius model proposes that the activated electrons are released from traps into the conduction band and may increase the current by orders of magnitude. However, the transfer characteristics are degraded as temperature rises above 75^{o}C due to the dominance of phonon scattering. The differences in hysteresis characteristics of theα-IGZO TFTs are mainly from the contribution of trapped electrons in or near the gate dielectric and trapping/detrapping in α-IGZO channel layer.

References

[1] H. Hosono, N. Kikuchi, N. Ueda, and H. Kawazoe, “Working hypothesis to explore novel wide band gap electrically conducting amorphous oxides and examples,” *J. Non-Cryst. Solids*, vol. 165, pp. 198–200, 1996.

[2] H. Hosono, M. Yasukawa, and H. Kawazoe, “Novel oxide amorphous semiconductors: transparent conducting amorphous oxides,” *J. Non-Cryst. Solids*, vol. 203, pp. 334, 1996.

[3] J. S. Park; T. W. Kim, D. Stryakhilev, J. S. Lee, S. G. An, Y. S. Pyo, D. B. Lee, Y. G. Mo, D. U. Jin, and H. K. Chung, “Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors,” *Appl. Phys. Lett.*, vol. 95, pp. 013503-1-3, 2009.

[4] R. L. Hoffman, B. J. Norris, and J. F. Wager , “ZnO-based transparent thin film transistors,” *Appl. Phys. Lett.*, vol. 82, pp. 733-735, 2003.

[5] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, “Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors,” *Nature*, vol. 432, pp. 488-492, 2004.

[6] A. J. Leenheer, J. D. Perkins, M. F. A. M. Vanhest, J. J. Berry, R. P. O’Hayre, and D. S. Ginley, “General mobility and carrier concentration relationship in transparent amorphous indium zinc oxide films,” *Physical Review B*, vol. 77, pp. 115215-1-5, 2008.

[7] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, and H. Kumomi, “High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering,” *Appl. Phys. Lett.*,

vol. 89, pp. 112123-1-3, 2006.

[8] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano, and H. Hosono, “Amorphous oxide semiconductors for high-performance flexible thin-film transistors,” *Jpn. J. Appl. Phys.*, vol. 45, pp. 4303-4308, 2006.

[9] U. Ozgur, Y. I. Alivov, C. Liu, A. Teke, M. A. Reshchikov, S. Dogan, V. Avrutin, S. J. Cho, and H. MorKoc, “A comprehensive review of ZnO material and devices,” *J. Appl. Phys.*, vol. 98, pp. 041301-1-103, 2005.

[10] S. Masuda, K. Kitamura, Y. Okumura, S. Miyatake, H. Tabata, and T. Kawai, “Transparent thin film transistors using ZnO as an active channel layer and their electrical properties,” *J. Appl. Phys.*, vol. 93, pp. 1624-1630, 2003.

[11] E. Fortunato, P. Barquinha, A. Pimentel, A. Gonçalves, A. Marques, R. Martins, and L. Pereira, “Wide-bandgap high-mobility ZnO thin-film transistors produced at room temperature,” *Appl. Phys. Lett.*, vol. 85, pp. 2541-2543, 2004.

[12] J. Nishii, F. M. Hossain, S. Takgi, T. Aita, K. Saikusa, Y. Ohmaki, I. Ohkubo, S. Kishimoto, A. Ohtomo, T. Fukumura, F. Matsukura, Y. Ohno, H. Koinuma, H. Ohno, and M. Kawasaki, “High mobility thin film transistors with transparent ZnO channels,” *Jpn. J. Appl. Phys.*, vol. 42, pp. L 347–L 349, 2003.

[13] I. H. Kim, D. Y. Ku, J. H. Ko, D. Kim, K. S. Lee, J.-h. Jeong, T. S. Lee, B. Cheong, Y.-J. Baik, and W. M. Kim, “Improvement of the thermal and chemical stability of Al doped ZnO films,” *J. Electroceram*, vol. 17, pp. 241–245, 2006.

[14] D. H. Kim, H. R. Kim, S. H. Lee, E. Byon, and G. H. Lee, “Electrical and structural properties of multi-component transparent conducting oxide films

prepared by co-sputtering of AZO and ITO," *J. Non-Cryst. Solids*, vol. 356, pp. 1779–1783, 2010.

[15] P. Banerjee, W. J. Lee, K. R. Bae, S. B. Lee, and G. W. Rubloff, "Structural, electrical, and optical properties of atomic layer deposition Al-doped ZnO films," *J. Appl. Phys.*, vol. 108, pp. 043504-1-7, 2010.

[16] D. C. Paine, B. Yaglioglu, Z. Beiley, and S. Lee, "Amorphous IZO-based transparent thin film transistors," *Thin Solid Films*, vol. 516, pp. 5894–5898, 2008.

[17] T. Iwasaki, N. Itagaki, T. Den, H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Combinatorial approach to thin-film transistors using multi-component semiconductor channels: An application to amorphous oxide semiconductors in In–Ga–Zn–O system," *Appl. Phys. Lett.*, vol. 90, pp. 242114-1-3, 2007.

[18] P. Barquinha, L. Pereira, G. Gonçalves, R. Martins, and E. Fortunato, "Toward high-performance amorphous GIZO TFTs," *Journal of the Electrochemical Society*, vol. 156, pp. H161-H168, 2009.

[19] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, α-$InGaZnO_4$," *Thin Solid Films*, vol. 486, pp. 38–41, 2005.

[20] A. Suresh, P. Gollakota, P. Wellenius, A. Dhawan, and J. F. Muth, "Transparent, high mobility InGaZnO thin films deposited by PLD," *Thin Solid Films*, vol. 516, pp. 1326–1329, 2008.

[21] H. Hosono, K. Nomura, Y. Ogo, T. Uruga, and T. Kamiya, "Factors controlling electron transport properties in transparent amorphous oxide semiconductors," *J. Non-Cryst. Solids*, vol. 354, pp. 2796–2800, 2008.

[22] T. Aoi, N. Oka, Y. Sato, R. Hayashi, H. Kumomi, and Y. Shigesato, "DC sputter deposition of amorphous indium–gallium–zinc–oxide (α-IGZO) films with H_2O introduction," *Thin Solid Films*, vol. 518, pp. 3004–3007, 2010.

[23] Y. K. Moon, S. Lee, D. H. Kim, D. H. Lee, C. O. Jeong, and J. W. Park, "Application of DC magnetron sputtering to deposition of InGaZnO films for thin film transistor devices," *Jpn. J. Appl. Phys.*, vol. 48, pp. 031301-1-4, 2009.

[24] A. Sato, K. Abe, R. Hayashi, H. Kumomi, K. Nomura, T. Kamiya, M. Hirano, and H. Hosono, "Amorphous In–Ga–Zn–O coplanar homojunction thin-film transistor," *Appl. Phys. Lett.*, vol. 94, pp. 133502–1-3, 2009.

[25] B. D. Ahn, H. S. Shin, H. J. Kim, J. S. Park, and J. K. Jeong, "Comparison of the effects of Ar and H_2 plasmas on the performance of homojunctioned amorphous indium gallium zinc oxide thin film transistors," *Appl. Phys. Lett.*, vol. 93, pp. 203506-1-3, 2008.

[26] Y. K. Moon, S. Lee, W. S. Kim, B. W. Kang, C. O. Jeong, D. H. Lee, and J. W. Park. "Improvement in the bias stability of amorphous indium gallium zinc oxide thin-film transistors using an O_2 plasma-treated insulator" *Appl. Phys. Lett*, vol. 95, pp. 013507-1-3, 2009.

[27] K. S. Son, T. S. Kim, J. S. Jung, M. K. Ryu, K. B. Park, B. W. Yoo, K. C. Park, J. Y. Kwon, S. Y. Lee, and J. M. Kim. "Threshold voltage control of amorphous gallium indium zinc oxide TFTs by suppressing back-channel current" *Electrochemical and Solid-State Letters*, vol. 12, pp. H26-H28, 2009.

[28] H. S. Bae, J. H. Kwon, S. Chang, M. H. Chung, T. Y. Oh, J. H. Park, S. Y. Lee, J. J. Pak, and B. K. Ju, "The effect of annealing on amorphous indium

gallium zinc oxide thin film transistors," *Thin Solid Films*, vol. 518, pp. 6325–6329, 2010.

[29] P. Barquinha, L. Pereira, G. Gonçalves, R. Martins, and E. Fortunato, "The effect of deposition conditions and annealing on the performance of high-mobility GIZO TFTs," *Electrochemical and Solid-State Letters*, vol. 11, pp. H248-H251, 2008.

[30] M. Nakata, K. Takechi, S. Yamaguchi, E. Tokumitsu, H. Yamaguchi, and S. Kaneko. "Effects of excimer laser annealing on $InGaZnO_4$ thin-film transistors having different active-layer thicknesses compared with those on polycrystalline silicon," *Jpn. J. Appl. Phys.*, vol. 48, pp. 115505-1-6, 2009.

[31] Y. H. Yang, S. Yang, and K. S. Chou, "Characteristic enhancement of solution-processed In–Ga–Zn oxide thin-film transistors by laser annealing," *IEEE Electron Device Lett.*, vol. 31, pp. 969-971, 2010.

[32] T. Kamiya, K. Nomura, and H. Hosono, "Electronic structures above mobility edges in crystalline and amorphous In-Ga-Zn-O: percolation conduction examined by analytical model," *Journal of display technology*, vol. 5, pp. 462-467, 2009.

[33] K. Nomura, H. Ohta, N. Ueda, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport in transparent oxide semiconductor with intrinsic structural randomness probed using single-crystalline $InGaO_3(ZnO)_5$ films," *Appl. Phys. Lett.*, vol. 85, pp. 993-995, 2004.

[34] A. Takagi, K. Nomura, H. Ohta, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, "Carrier transport and electronic structure in amorphous oxide semiconductor, α-$InGaZnO_4$," *Thin Solid Films*, vol. 486, pp. 38-41, 2005.

[35] T. Kamiya, K. Nomura, and H. Hosono, “Origins of high mobility and low operation voltage of amorphous oxide TFTs: electronic structure, electron transport, defects and doping,” *Journal of display technology*, vol. 5, pp. 468-483, 2009.

[36] T. Kamiya, K. Nomura, and H. Hosono, “Present status of amorphous In–Ga–Zn–O thin-film transistors,” *Sci. Technol. Adv. Mater.*, vol. 11, pp. 044305, 2010.

[37] H. Hosono, “Ionic amorphous oxide semiconductors: Material design, carrier transport, and device application,” *J. Non-Cryst. Solids*, vol. 352, pp. 851–858, 2006.

[38] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya, and H. Hosono, “Trap densities in amorphous-$InGaZnO_4$ thin-film transistors,” *Appl. Phys. Lett.*, vol. 92, pp. 133512-1-3, 2008.

[39] K. H. Ji, J. I. Kim, H. Y. Jung, S. Y. Park, Y. G. Mo, J. H. Jeong, J. Y. Kwon, M. K. Ryu, S. Y. Lee, R. Choi, and J. K. Jeonga, “The effect of density-of-state on the temperature and gate bias-induced instability of InGaZnO thin film transistors,” *Journal of The Electrochemical Society*, vol. 157, pp. H983-H986, 2010.

[40] H. H. Hsieh, T. Kamiya, K. Nomura, H. Hosono, and C. C. Wu, “Modeling of amorphous $InGaZnO_4$ thin film transistors and their subgap density of states,” *Appl. Phys. Lett.*, vol. 92, pp. 133503-1-3, 2008.

[41] J. H. Park, K. Jeon, S. Lee, S. Kim, S. Kim, I. Song, C. J. Kim, J. Park, Y. Park, D. M. Kim, and D. H. Kim, “Extraction of density of states in amorphous GaInZnO thin-film transistors by combining an optical

charge pumping and capacitance–voltage characteristics,” *IEEE Electron Device Lett.*, vol. 29, pp. 1292-1295, 2008.

[42] J. K. Jeong, J. H. Jeong, H. W. Yang, J, S. Park, Y. G. Mo, and H. D. Kim, “High performance thin film transistors with cosputtered amorphous indium gallium zinc oxide channel ,” *Appl. Phys. Lett.*, vol. 91, pp. 133505-1-3, 2007.

[43] J. H. Jeong, H. W. Yang, J. S. Park, J. K. Jeong, Y. G. Mo, H. D. Kim, J. Song, and C. S. Hwang, “Origin of subthreshold swing improvement in amorphous indium gallium zinc oxide transistors,” *Electrochemical and Solid-State Letters*, vol. 11, pp. H157-H159, 2008.

[44] J. H. Na, M. Kitamura, and Y. Arakawa, “High field-effect mobility amorphous InGaZnO transistors with aluminum electrodes,” *Appl. Phys. Lett.*, vol. 93, pp. 063501-1-3, 2008.

[45] J. K. Jeong, H. W. Yang, J. H. Jeong, Y. G. Mo, and H. D. Kim, “Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors,” *Appl. Phys. Lett.*, vol. 93, pp.123508-1-4, 2008.

[46] S. S. Park, W. H. Choi, D. H. Nam, K. I. Chai, J. K. Jeong, H. D. Lee, and G. W. Lee, “Performance and stability characterization of bottom gated amorphous indium gallium zinc oxide thin film transistors grown by RF and DC sputtering,” *Jpn. J. Appl. Phys.*, vol. 48, pp. 04C134-1-5, 2009.

[47] H. W. Zan, W. T. Chen, H. W. Hsueh, S. C. Kao, M. C. Ku, C. C. Tsai, and H. F. Meng, “Amorphous indium-gallium-zinc-oxide visible-light phototransistor with a polymeric light absorption layer,” *Appl. Phys. Lett.*, vol. 97, pp.203506-1-3, 2010.

[48] K. H. Ji, J. I. Kim, Y. G. Mo, J. H. Jeong, S. Yang, C. S. Hwang, S. H. K. Park, M. K. Ryu, S. Y. Lee, and J. K. Jeong, "Comparative study on light-induced bias stress instability of IGZO transistors with SiN_x and SiO_2 gate dielectrics," *IEEE Electron Device Lett.*, vol. 31, pp. 1404-1406, 2010.

[49] J. M. Lee, I. T. Cho, J. H. Lee, W. S. Cheong, C. S. Hwang, and H. I. Kwon, "Comparative study of electrical instabilities in top-gate InGaZnO thin film transistors with Al_2O_3 and Al_2O_3/SiN_x gate dielectrics," *Appl. Phys. Lett.*, vol. 94, pp.222112-1-3, 2009.

[50] K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, and S. Kaneko, "Application of exponential tail-state distribution model to the above-threshold characteristics of Zn-based oxide thin-film transistors," *IEEE Trans. on Electron Devices*, vol. 56, pp.2165-2168, 2009.

[51] C. Chen, K. Abe, H. Kumomi, and J. Kanicki, "Density of states of α-InGaZnO from temperature-dependent field-effect studies," *IEEE Trans. on Electron Devices*, vol. 36, pp.1177-1183, 2009.

[52] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan, and L. M. Irving, "Stable ZnO thin film transistors by fast open air atomic layer deposition," *Appl. Phys. Lett.*, vol. 92, pp.192101-1-3, 2008.

[53] M. J. Powell, "The physics of amorphous-silicon thin-film transistors," *IEEE Trans. on Electron Devices*, vol. 36, pp.2753-2763, 1989.

[54] N. Lustig, and J. Kanicki, "Gate dielectric and contact effects in hydrogenated amorphous silicon-silicon nitride thin-film transistors," *J. Appl. Phys.*, vol. 65, pp. 343361-1-10, 1989.

[55] K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, “Constant-voltage-bias stress testing of a-IGZO thin-film transistors,” *IEEE Trans. on Electron Devices*, vol. 56, pp.1365-1370, 2009.

Figure Captions

Table 1.1 Comparison of silicon based semiconductor TFT and metal-oxide based semiconductor TFT.

	α-Si TFT	Poly-Si	Metal Oxide TFT
Phase	Amorphous	Polycrystalline	Amorphous or Polycrystalline
Channel Mobility	1 $cm^2/V^{-1}\cdot s^{-1}$	~200 $cm^2/V^{-1}\cdot s^{-1}$	10~40 $cm^2/V^{-1}\cdot s^{-1}$
Switching Characteristics	0.4~0.5 V/decade	0.2~0.3 V/decade	0.09~0.6 V/decade
Source/ Drain Leakage Current	~10^{-13} A	~10^{-12}A	~10^{-13}A
Uniformity	Good	Not Good	Good
Long-term TFT reliability	Low	High	Unknown
Maximum Process Temperature	~250°C	~400-500°C	RT to 350°C
Manufacturing Cost (Number of mask)	Low (4~6)	High (7~11)	Very low (4~6)
Application Display	LCD	LCD, OLED	LCD, OLED

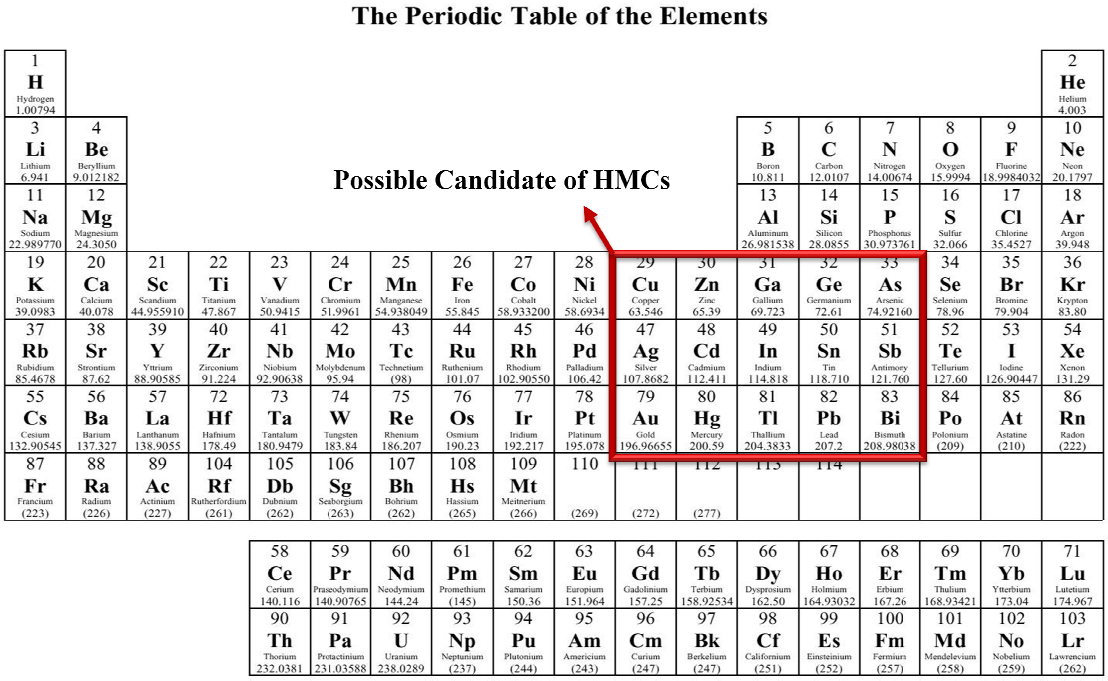
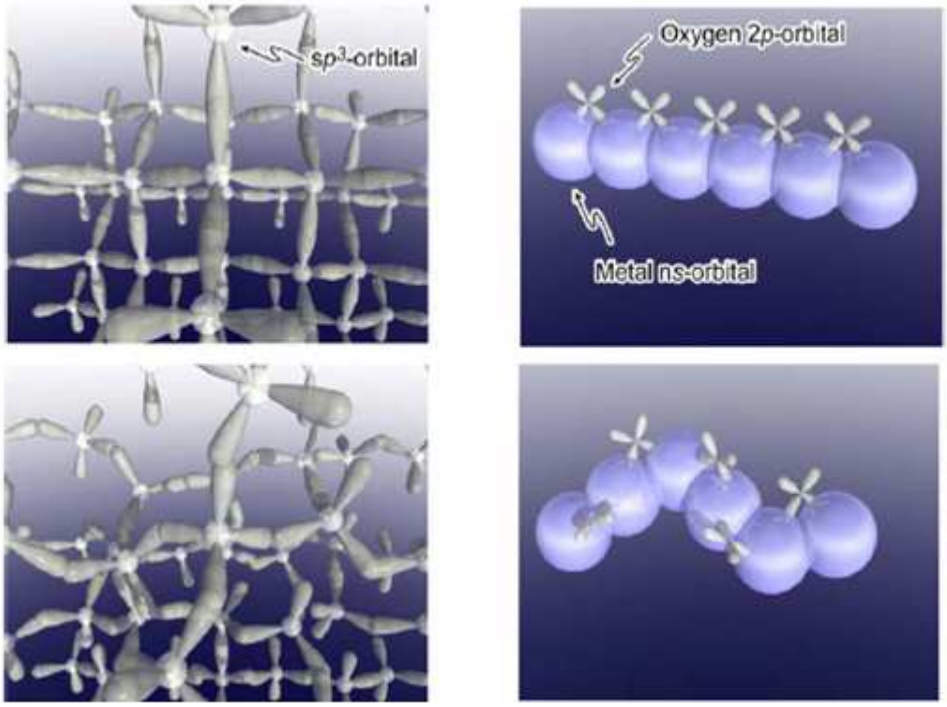


Fig.1.1. The elements of heavy metal cations with $(n\text{-}1)d^{10}ns^{0}$ electronic configuration on the Periodic Table.



(a) (b)

Fig. 1.2. Schematic drawings for the carrier transport paths (that is, conduction band bottoms) in the crystalline and amorphous semiconductor. (a) Covalent semiconductor, for example, silicon. (b) Post transition metal oxide semiconductors. [5]

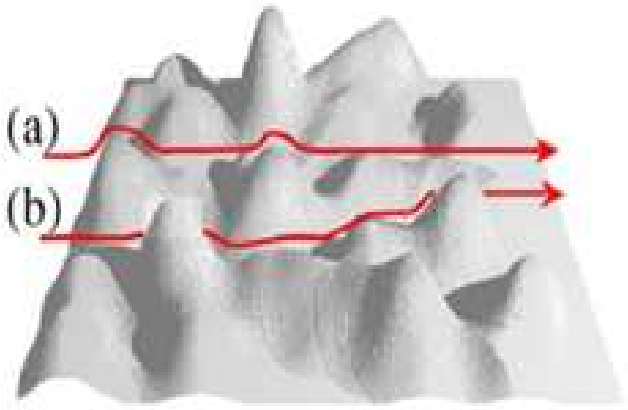


Fig. 1.3. Illustration of the image of percolation conduction over distributed potential barriers. The drawn surface shows a potential isosurface for electron transport. (a) High temperature case. An electron chooses a shorter but higher barrier path. (b) Low temperature case. An electron chooses a longer, but lower barrier path. [32]

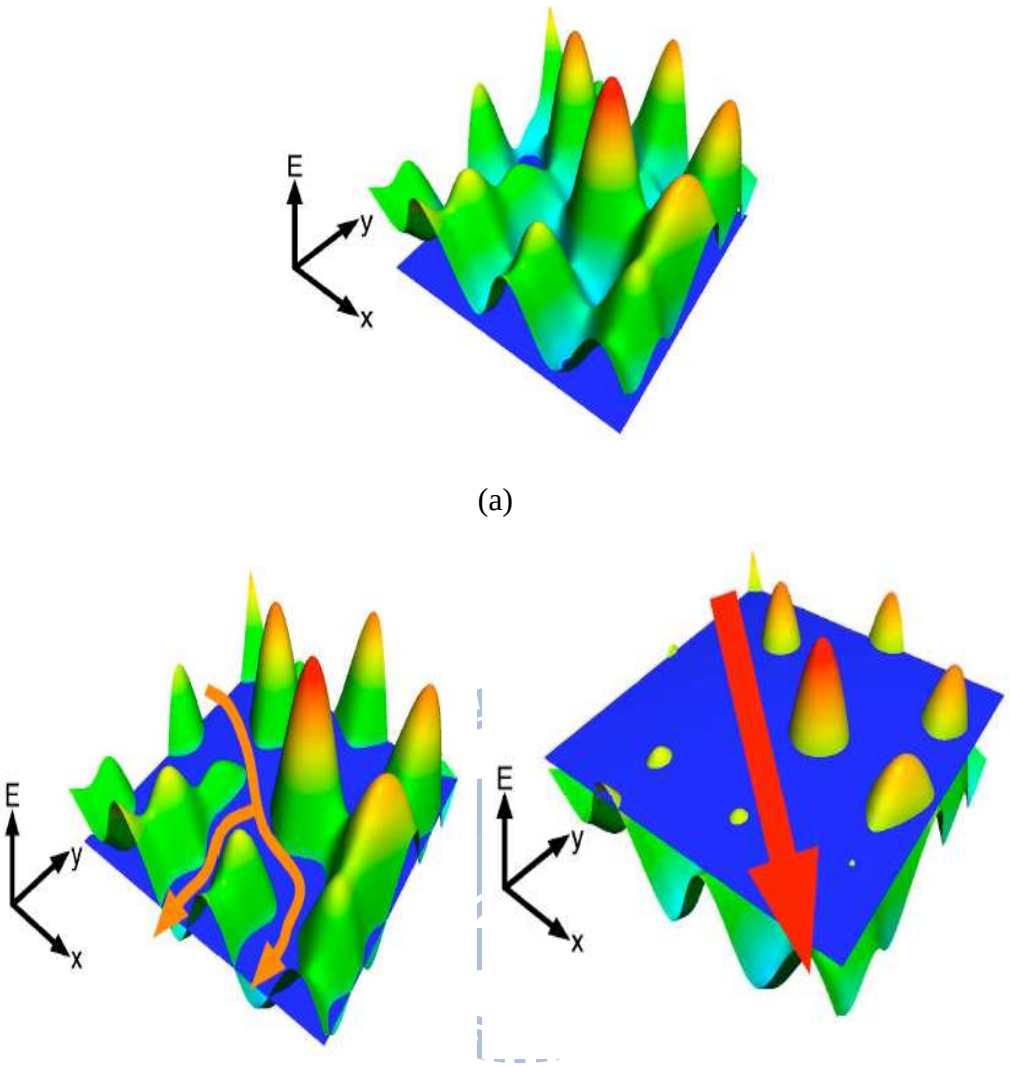


Fig. 1.4. The bumpy surface represents the conduction band edge and flat layer represents the Fermi level. The model is simplified by assuming that the temperature is close to 0 K. (a) when the Fermi level is low, there is not enough electron to induce above the conduction band edge. (b)As the Fermi level increases, electrons trickle through potential valley (percolation conduction) (c) when the Fermi level is high enough, almost all potential barriers are immersed under the Fermi level so that electrons more almost unhindered. [37]

Table 1.2. The common deposition methods for manufacturing ZnO and α-IGZO film as active channel of transparent TFTs.

Deposition Technology	Advantages	Disadvantages
Sol-gel method	Easy Processing Low Cost of Equipment	High manufacture temperature
Spray	Easy Processing Low Cost of Equipment	High manufacture temperature
Chemical Vapor Deposition (CVD)	High Film Quality High Productivity	High manufacture temperature Volatile material
Sputter	High Film Quality Low Manufacture Temperature Good Uniformity of Large Scale Good Adhesion	The damaged sputter target Low Deposition Rate
Evaporation	Fast Deposition Rate	Difficult to control the deposited film
Pulse Laser Deposition (PLD)	Good Surface Roughness Easy to Make Multilayer Fast Deposition Rate The deposited film reserves the stoichiometry of sputter target	Contamination (particle attached) Low productivity High cost of equipment Not easy to make large scale deposition

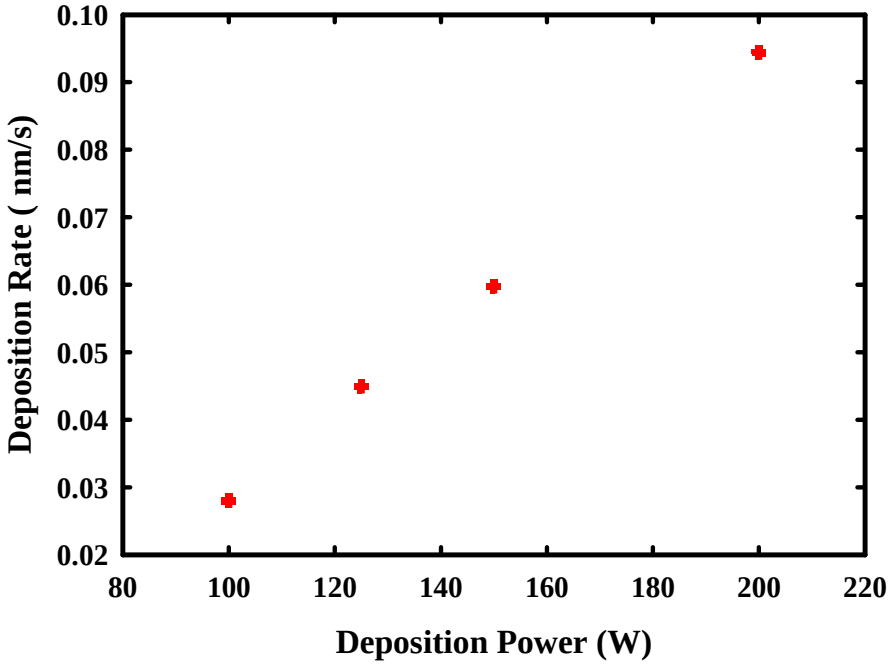
Table 2.1. Major deposition parameters for preparing the α-IGZO films. In (a) the deposition power was varied to study its impacts, while in (b) the oxygen flow was varied to study its impacts.

System base pressure （Torr）	3×10^{-6}
Working pressure （mTorr）	5
Deposition temperature （℃）	RT
Ar gas flow（sccm）	50
O_2 gas flow (sccm)	1
RF deposition power （W）	100、125、150、200

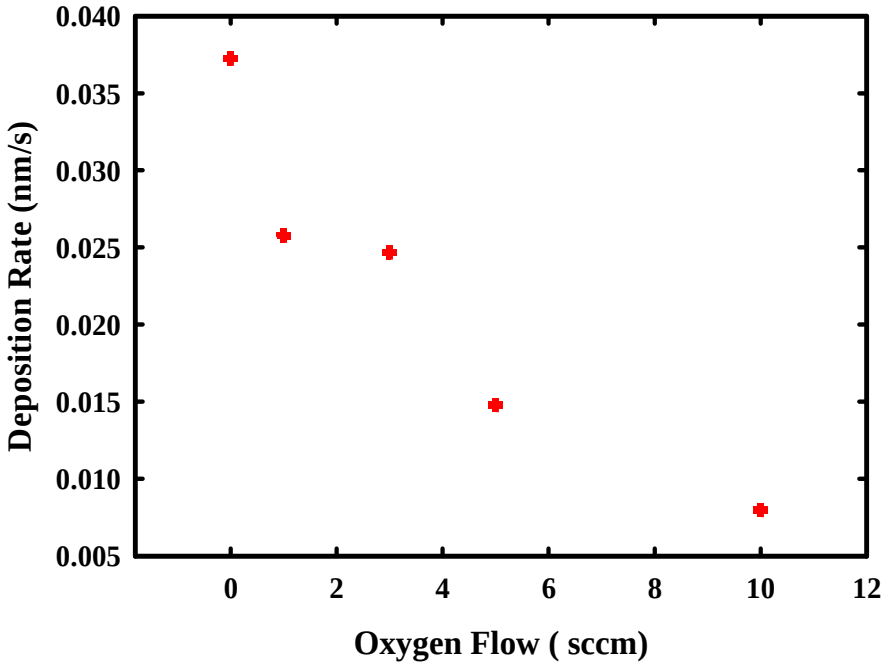
(a)

System base pressure （Torr）	3×10^{-6}
Working pressure （mTorr）	5
Deposition temperature （℃）	RT
Ar gas flow（sccm）	50
O_2 gas flow (sccm)	1、3、5、10
RF deposition power （W）	100

(b)

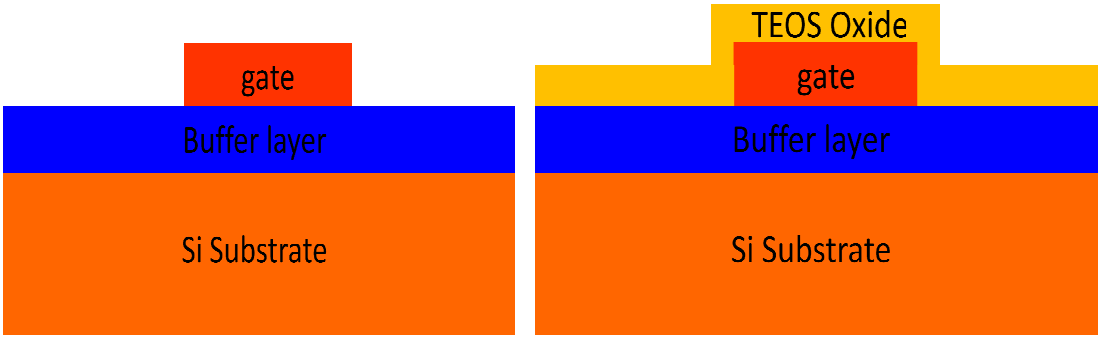


(a)



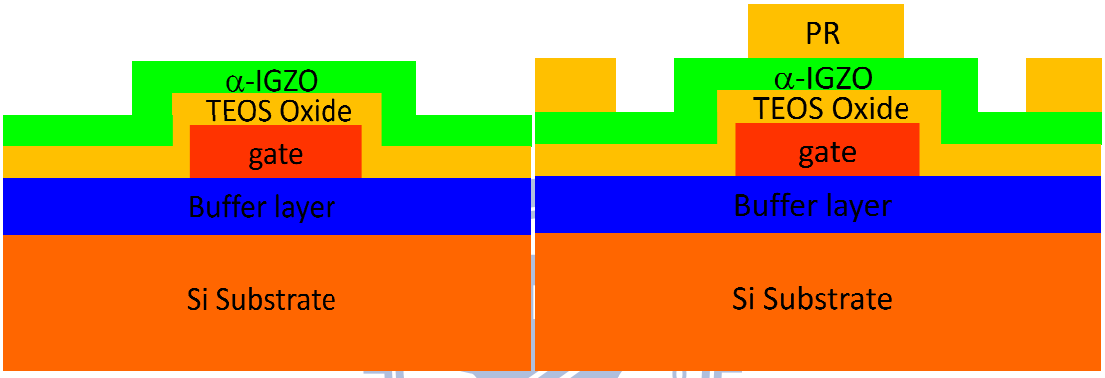
(b)

Fig 2.1. (a) The deposition rate as a function of power at constant oxygen flow (1sccm) and (b) the deposition rate as a function of oxygen flow at fixed deposition power (100W).



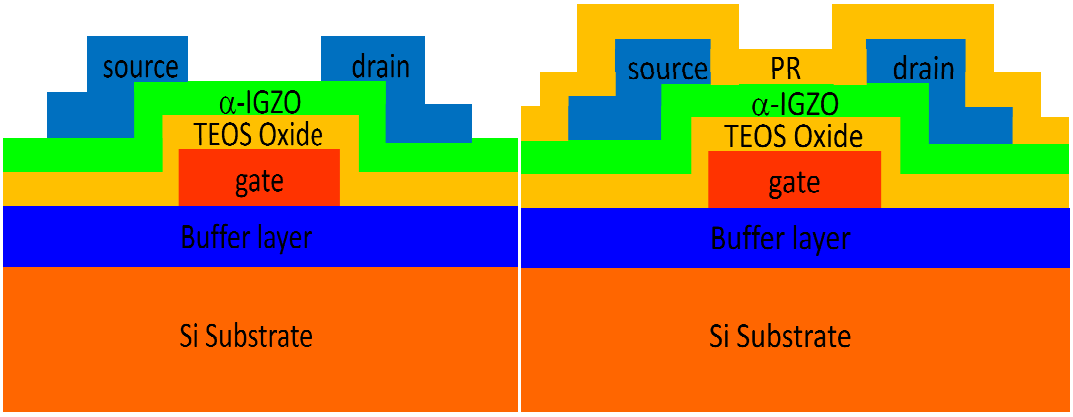
(a) (b)

Fig. 2.2. (a) Gate definition and (b) deposition of a 100 nm TEOS oxide by PECVD.



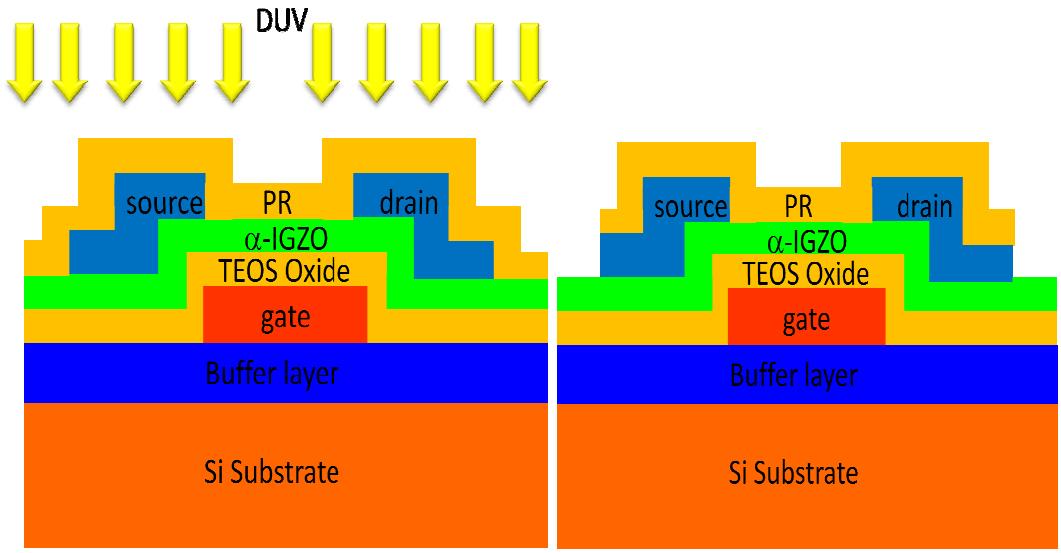
(c) (d)

Fig. 2.2. (c) 50 nm α-IGZO channel film was deposition by RF sputter. (d) PR coating for defining the source/drain regions.



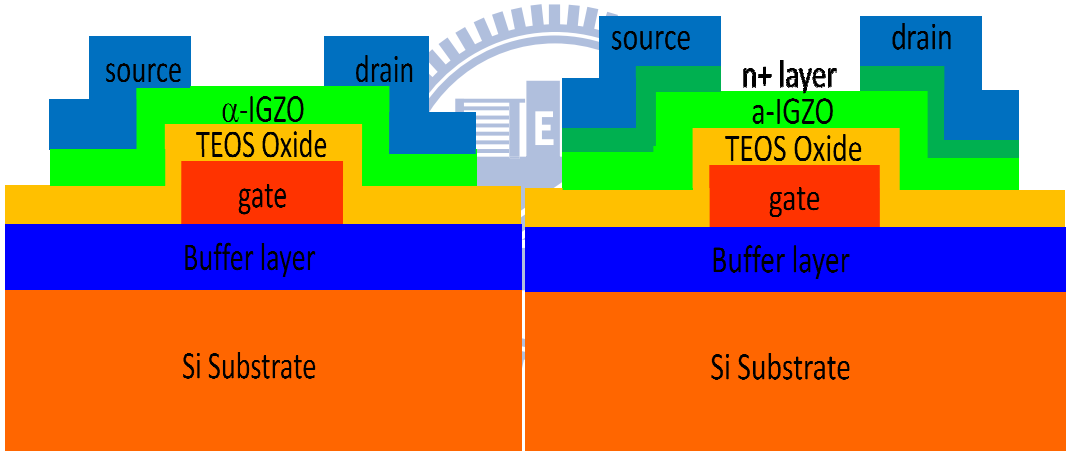
(e) (f)

Fig. 2.2. (e) Formation of source/drain metal deposition with the lift-off method. (f) Coating of a PR layer.



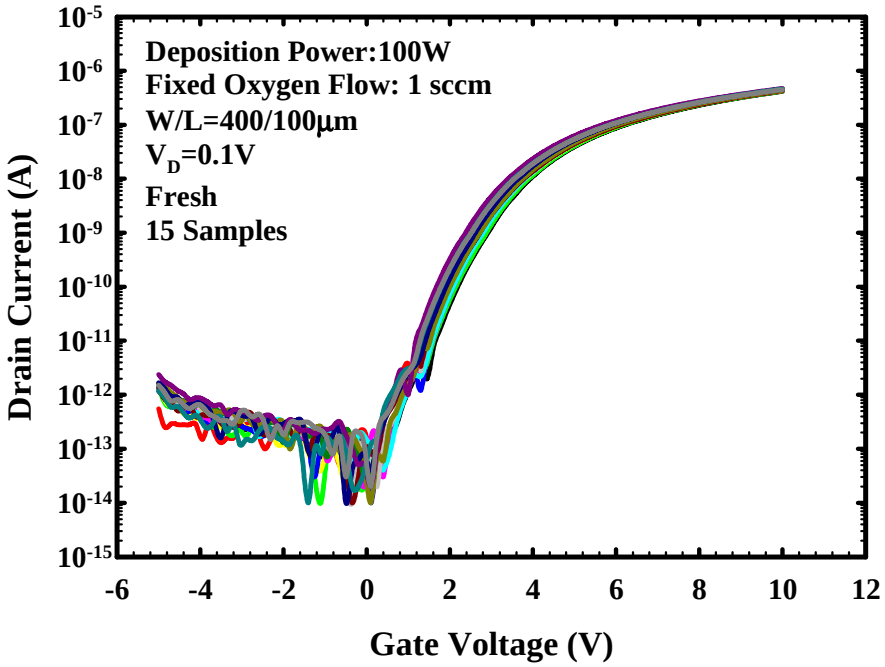
(g) (h)

Fig 2.2. (g) Exposure and (h) Patterning of the active region by wet etching.

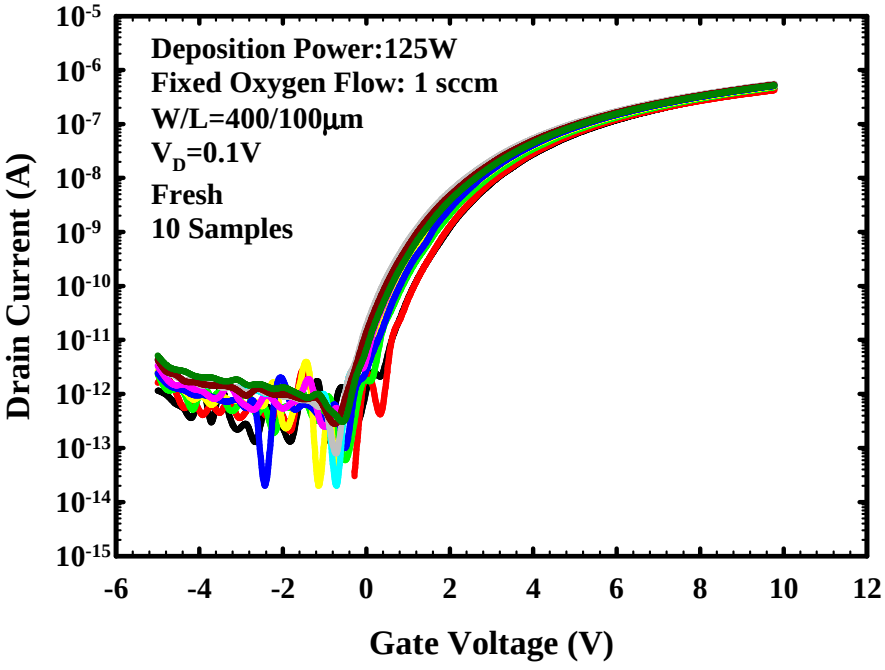


(i) (j)

Fig 2.2. (i) Cross-sectional view of the α-IGZO TFTs device without n^+ layer and (j) with n^+ layer.

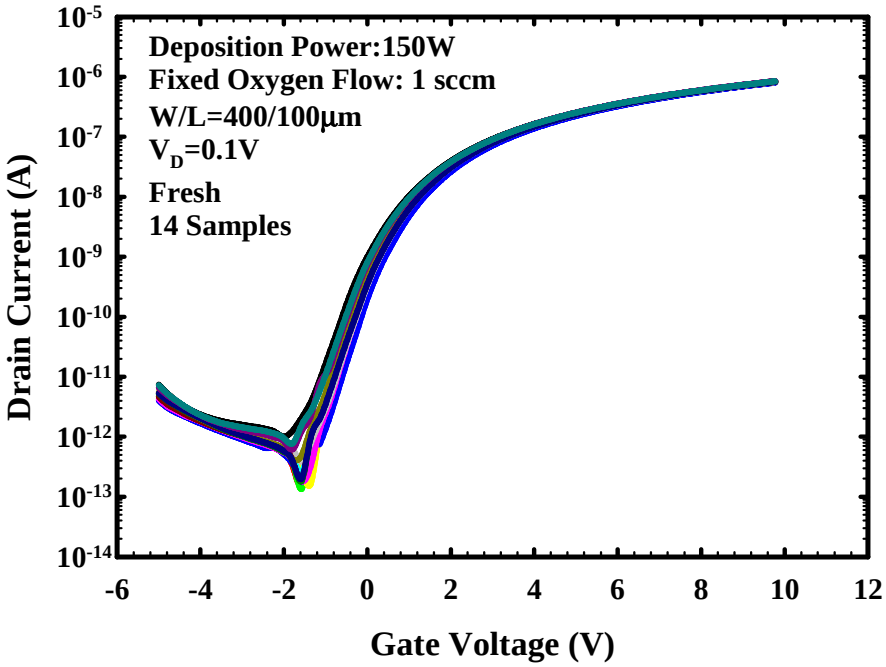


(a)

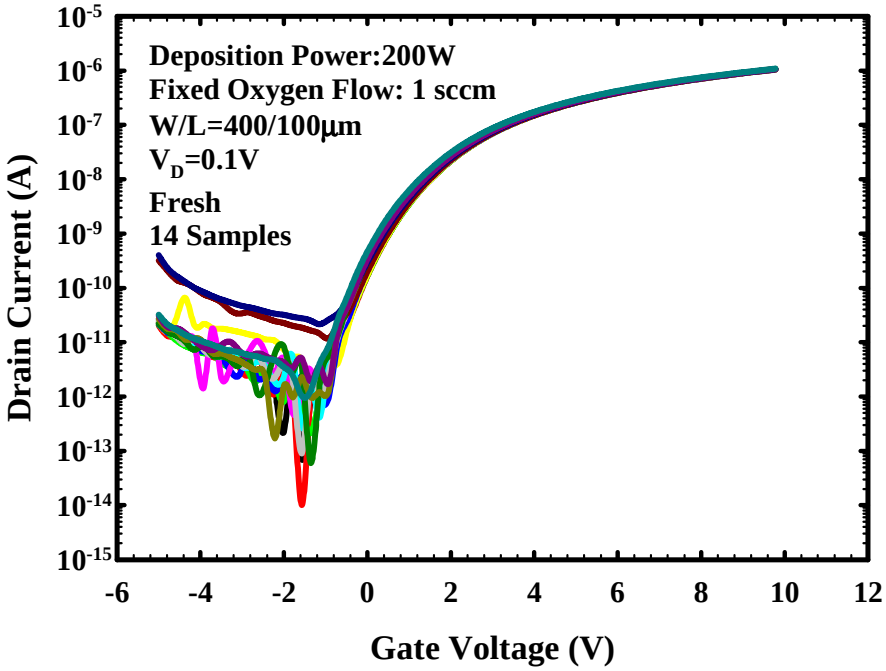


(b)

Fig. 3.1. Transfer characteristics of the α-IGZO devices deposited with deposition power of (a) 100W, (b) 125W, (c) 150W and (d) 200W at a constant oxygen flow of 1sccm.



(c)



(d)

Fig. 3.1. Transfer characteristics of α-IGZO devices deposited with deposition power of (a) 100W, (b) 125W, (c) 150W and (d) 200W at a constant oxygen flow of 1sccm.

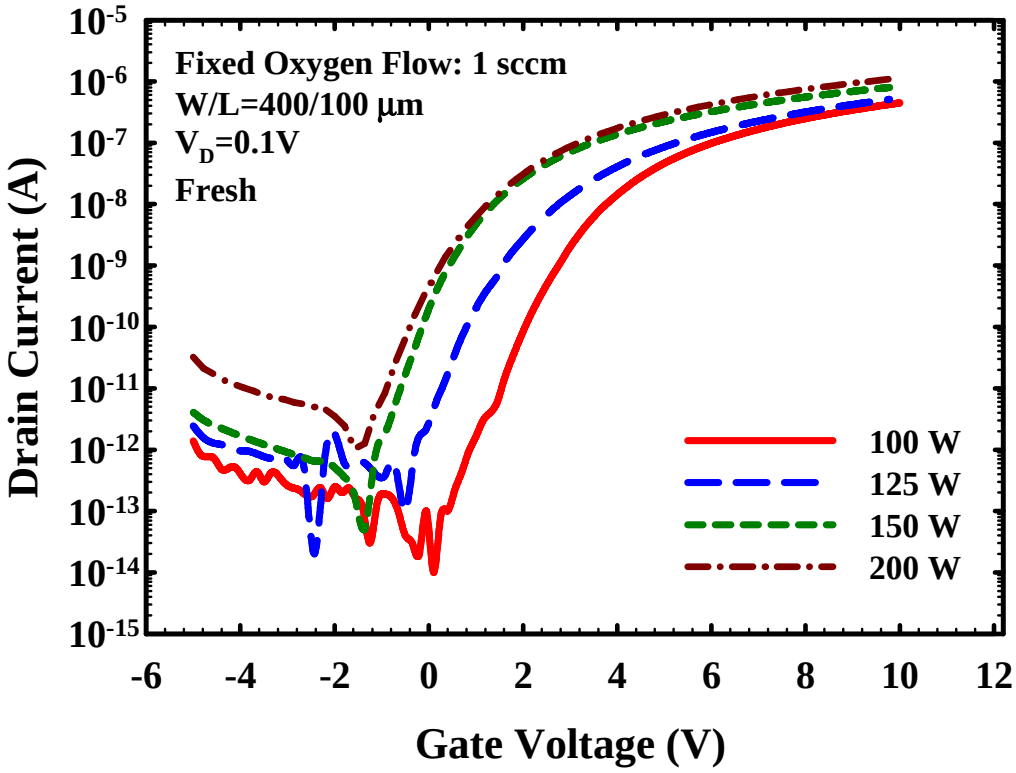
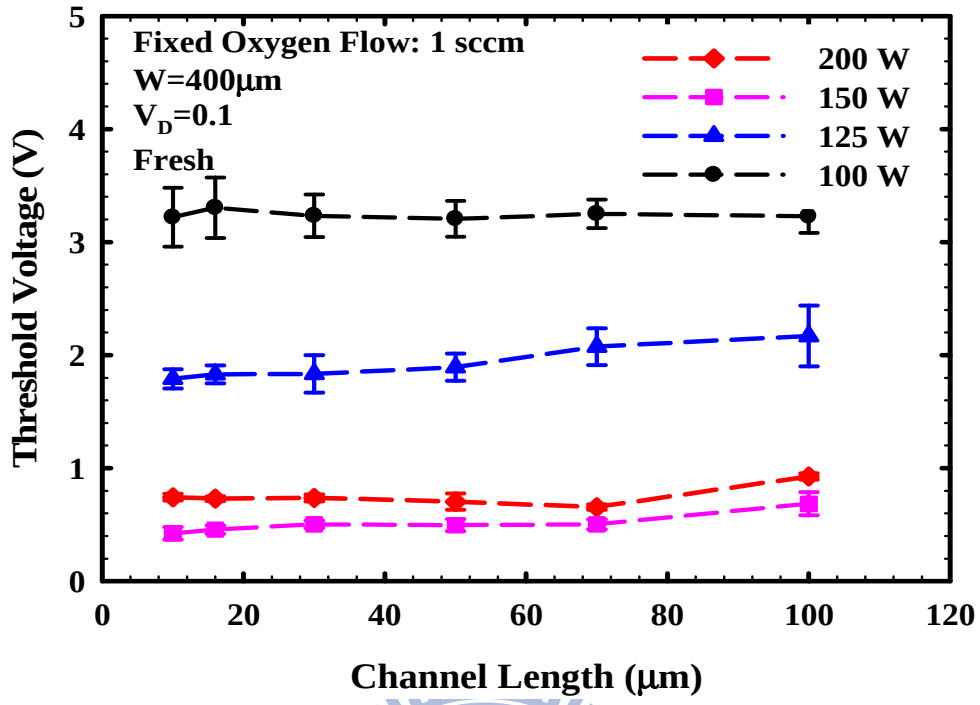
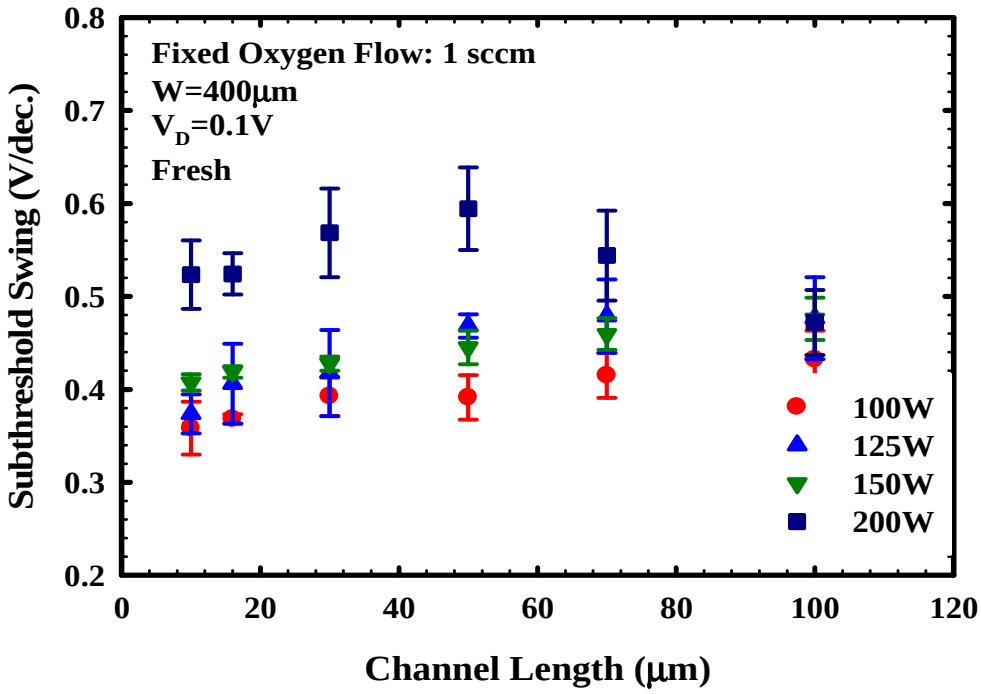


Fig 3.2. Typical transfer characteristics of α-IGZO devices deposited with different deposition power.

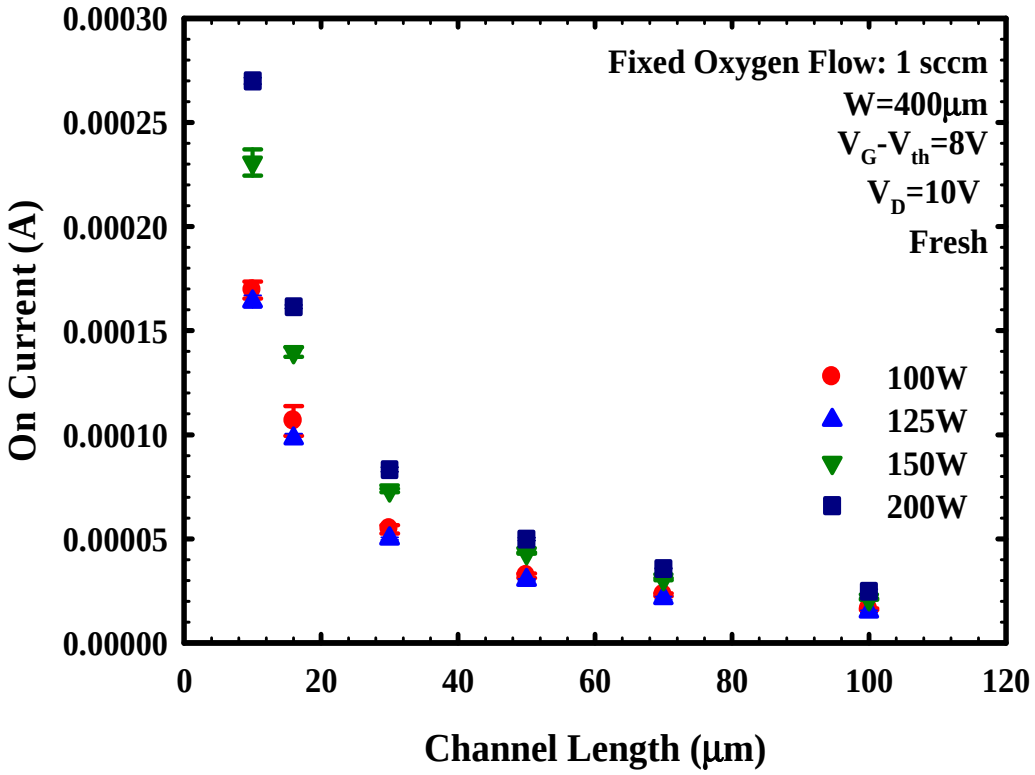


(a)



(b)

Fig. 3.3. (a) Extracted threshold voltage and (b) sub-threshold swing as a function of channel length for devices deposited with various rf powers.



(c)

Fig. 3.3. (c) Extracted on-current measured at V_G-V_{th}=8V and V_D=10V as a function of channel length for devices deposited with various rf powers.

Table 3.1. Summary of material analysis for α-IGZO films with different deposition power.

XPS	RT						AFM	
	Power (W)	O_2 Flow (sccm)	In(%)	Ga(%)	Zn(%)	O(%)	RMS (nm)	In/(In+Ga+Zn)
	50	1	20.03	11.76	8.11	60.1	0.589	0.502
	100	1	19.43	10.26	7.84	62.47	0.763	0.518
	125	1	21.23	10.61	9.28	58.88	0.612	0.516
	150	1	21.29	10.07	9.17	59.47	0.581	0.525
	200	1	20.73	9.14	8.09	62.04	0.574	0.546

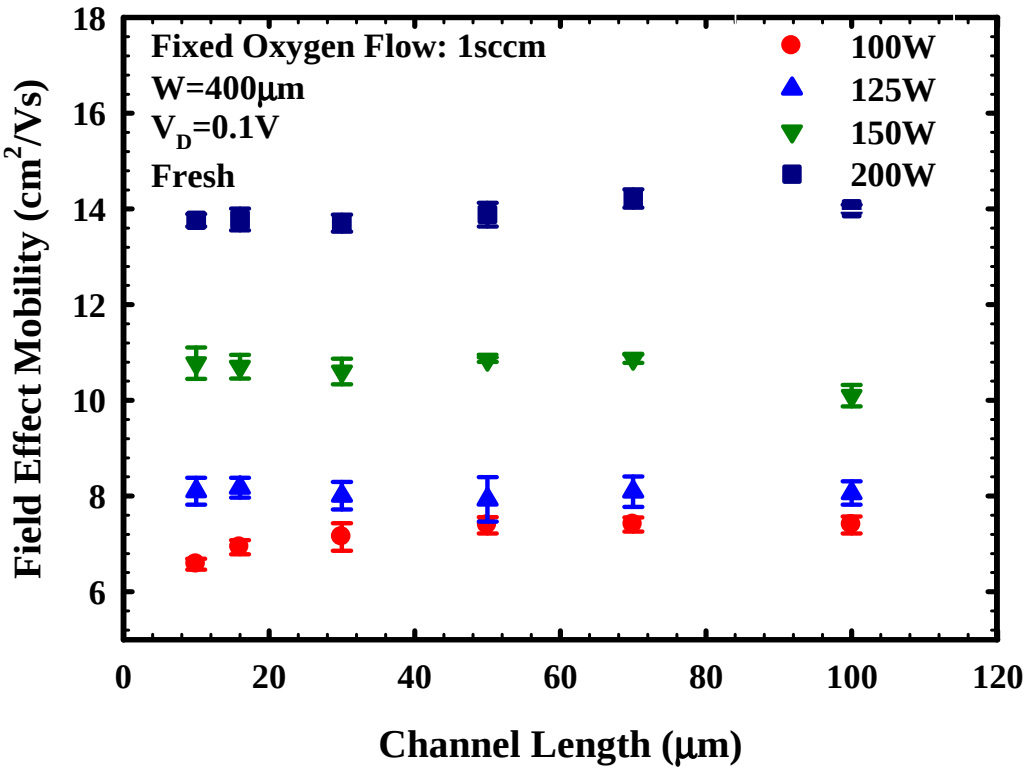
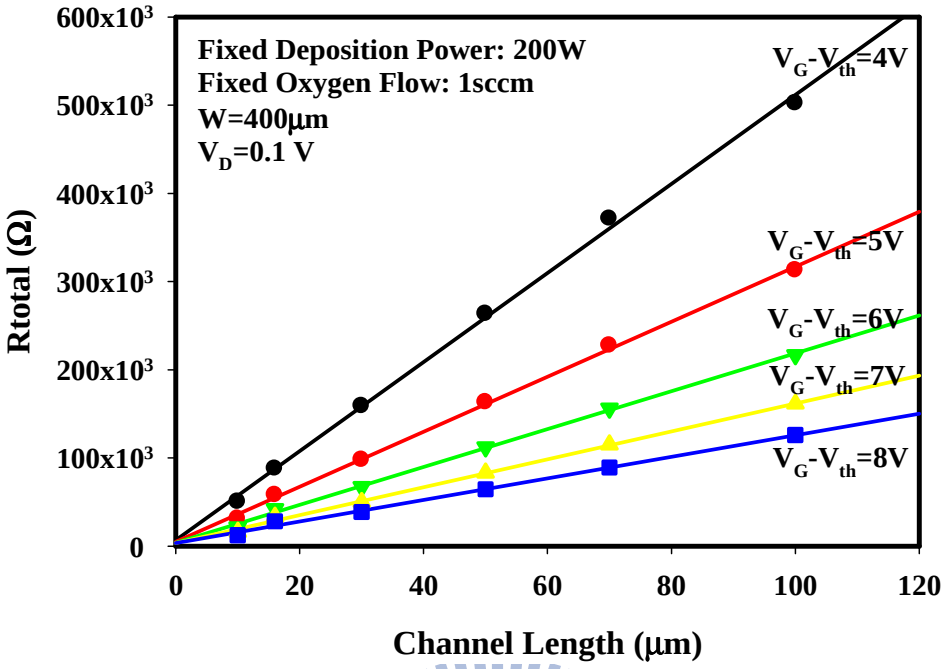
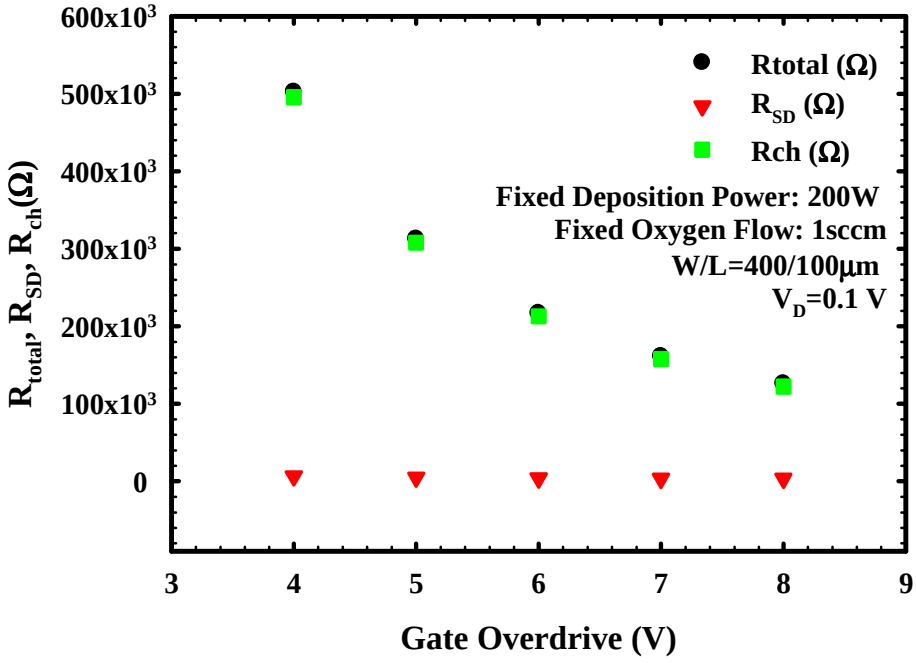


Fig. 3.4. Field-effect mobility for devices deposited at different rf powers as a function of channel length.



(a)



(b)

Fig. 3.5. Results of (a) the R_{total} measurements and (b) extracted R_{total}, R_{ch}, and R_{SD} as a function of gate overdrive for a device with W/L of 400/100μm.

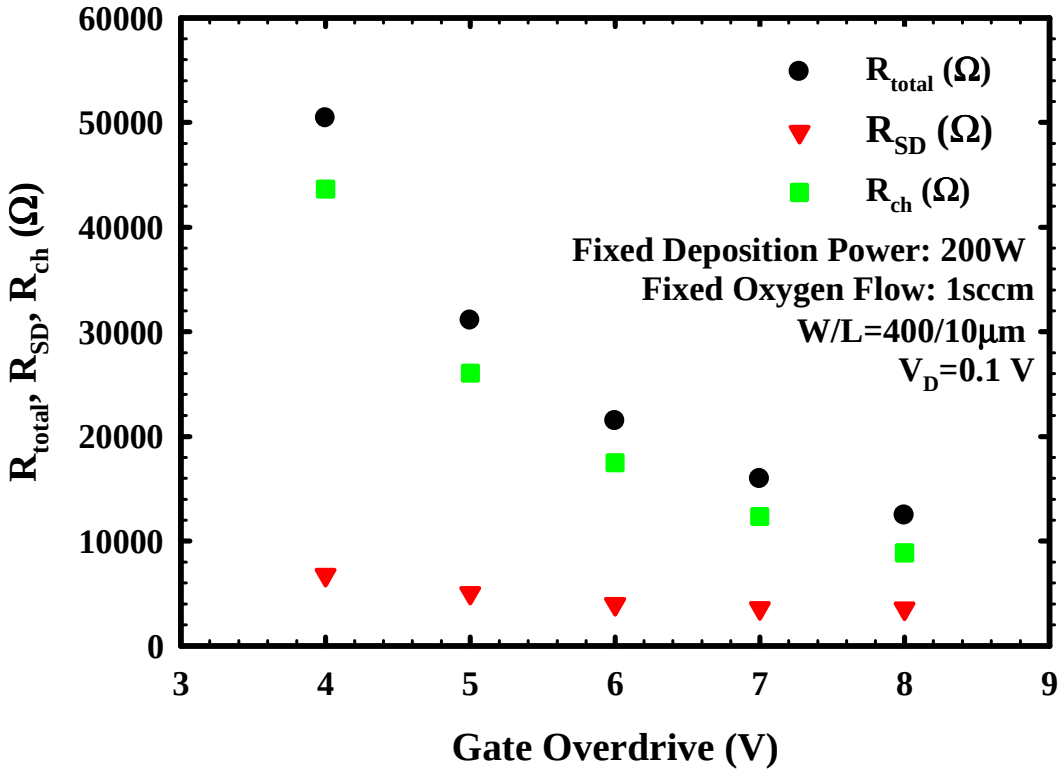
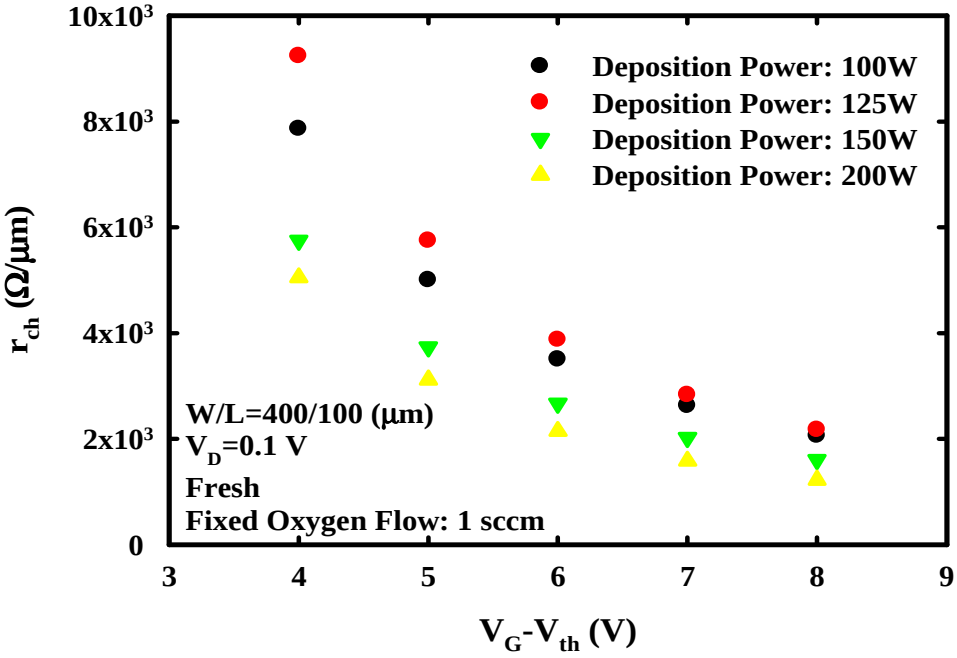
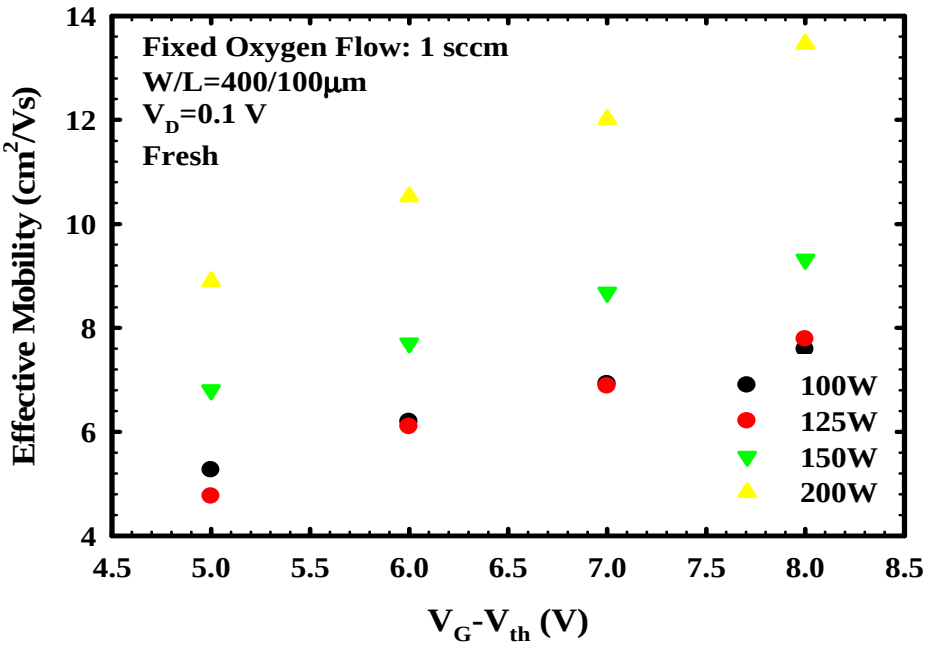


Fig. 3.6. Extracted R_{total}, R_{ch}, and R_{SD} as a function of gate overdrive for a device with W/L of 400/10μm.

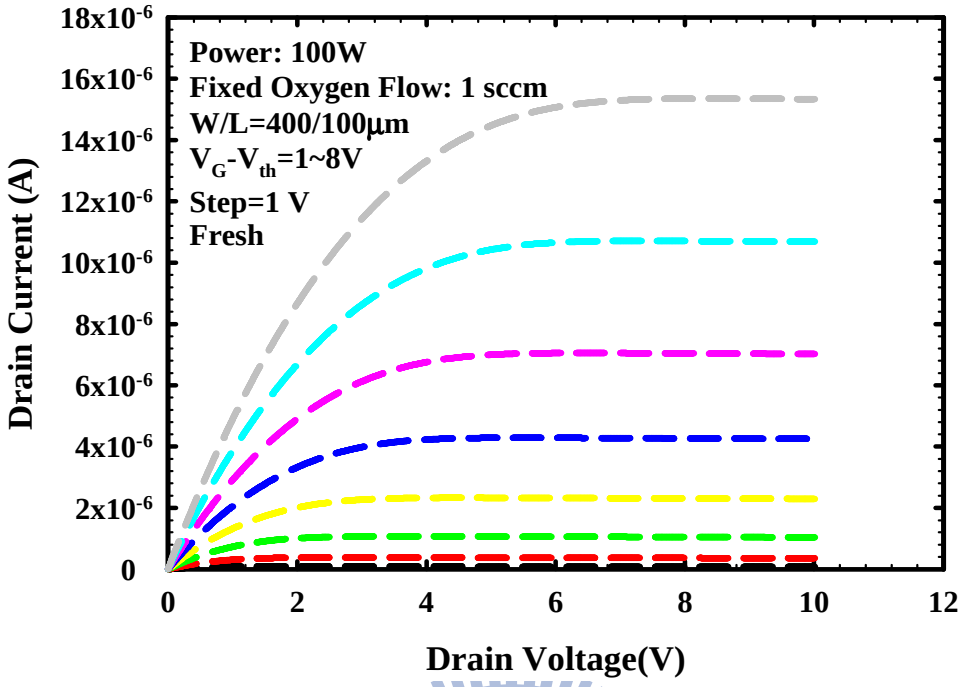


(a)

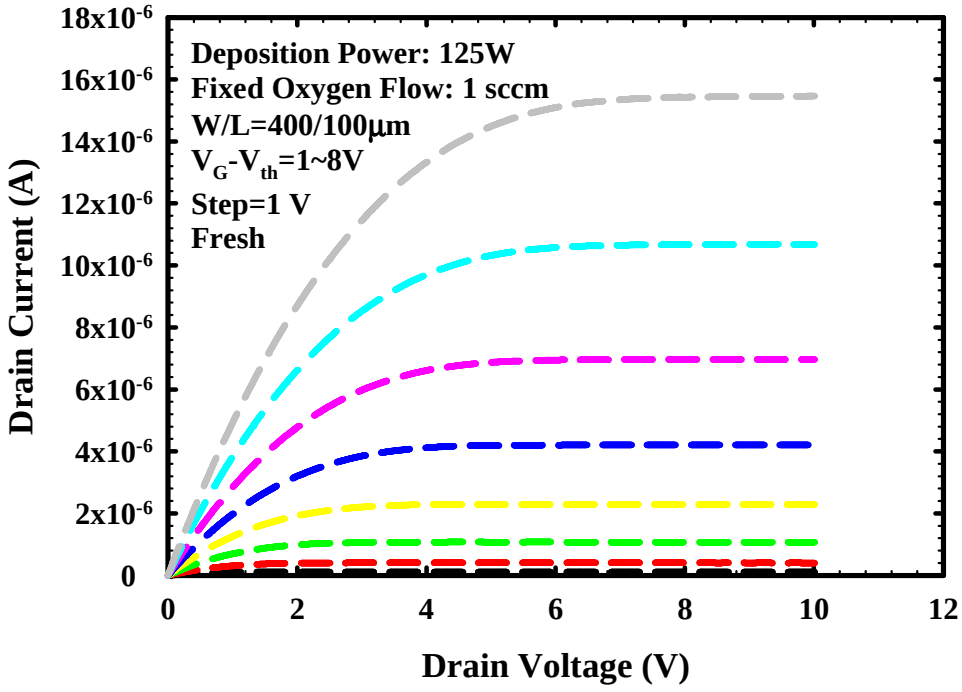


(b)

Fig. 3.7. (a) Extracted channel resistance per micrometer and (b) effective mobility as a function of gate overdrive.

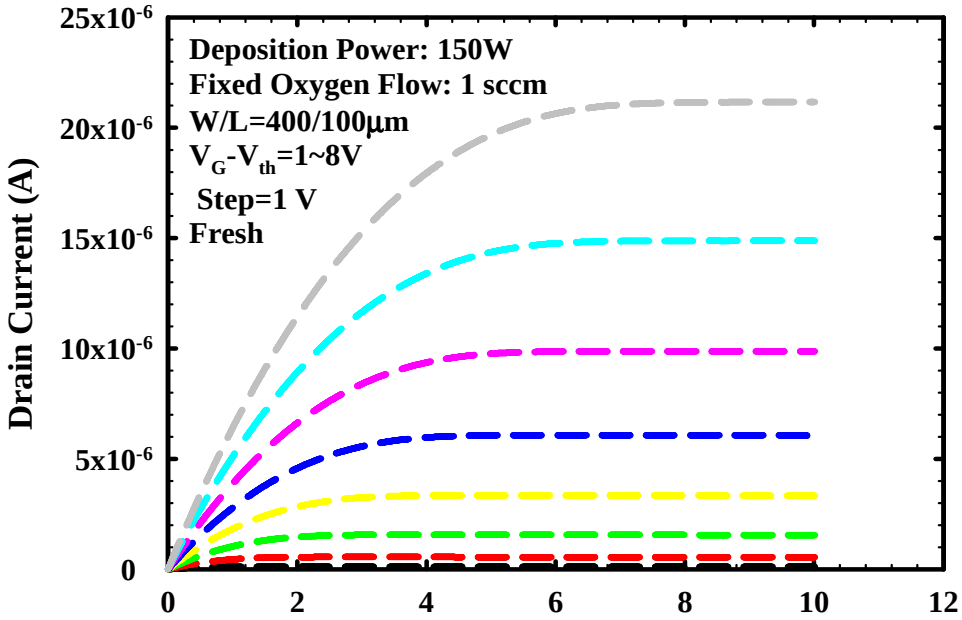


(a)

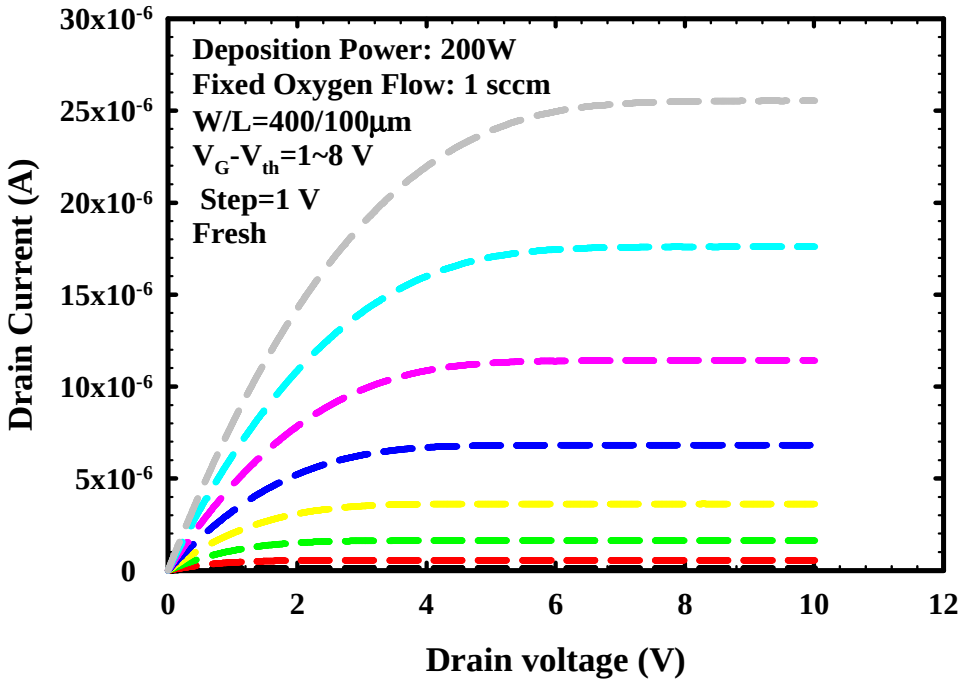


(b)

Fig. 3.8. Output characteristics of devices deposited with rf power of (a) 100W, (b) 125W, (c) 150W and (d) 200W.

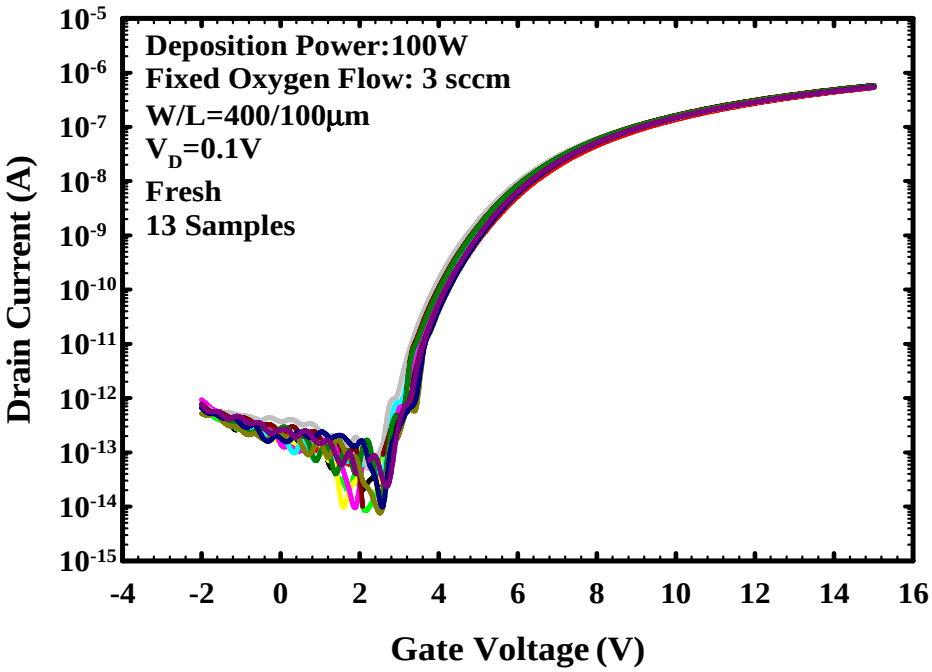


(c)

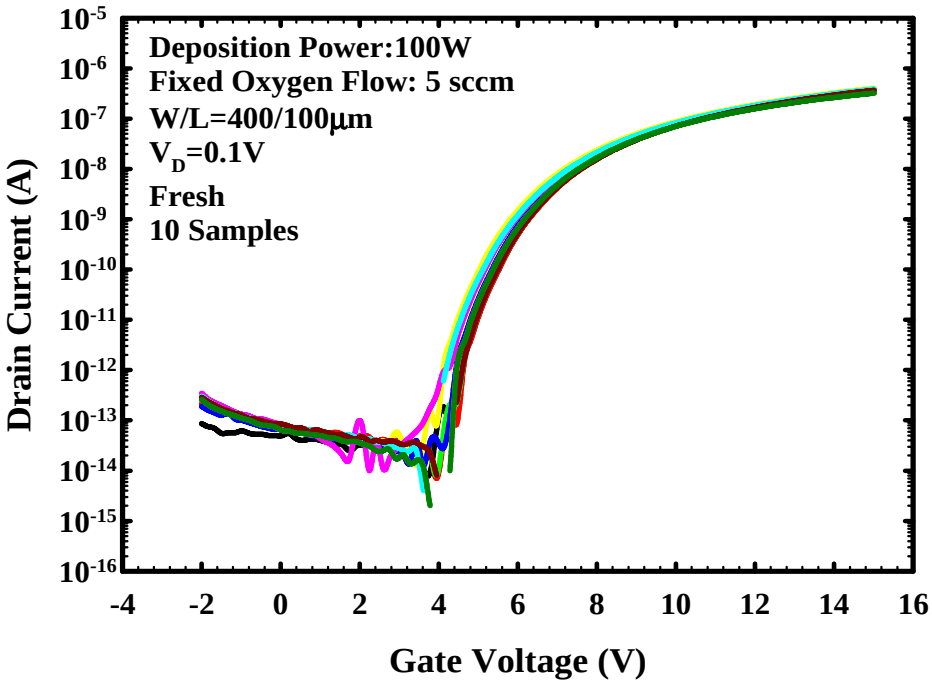


(d)

Fig. 3.8. Output characteristics of devices deposited with rf power of (a) 100W, (b) 125W, (c) 150W and (d) 200W.



(a)



(b)

Fig. 3.9. Transfers characteristics of several α-IGZO devices with oxygen flow of (a) 3sccm and (b) 5sccm, respectively.

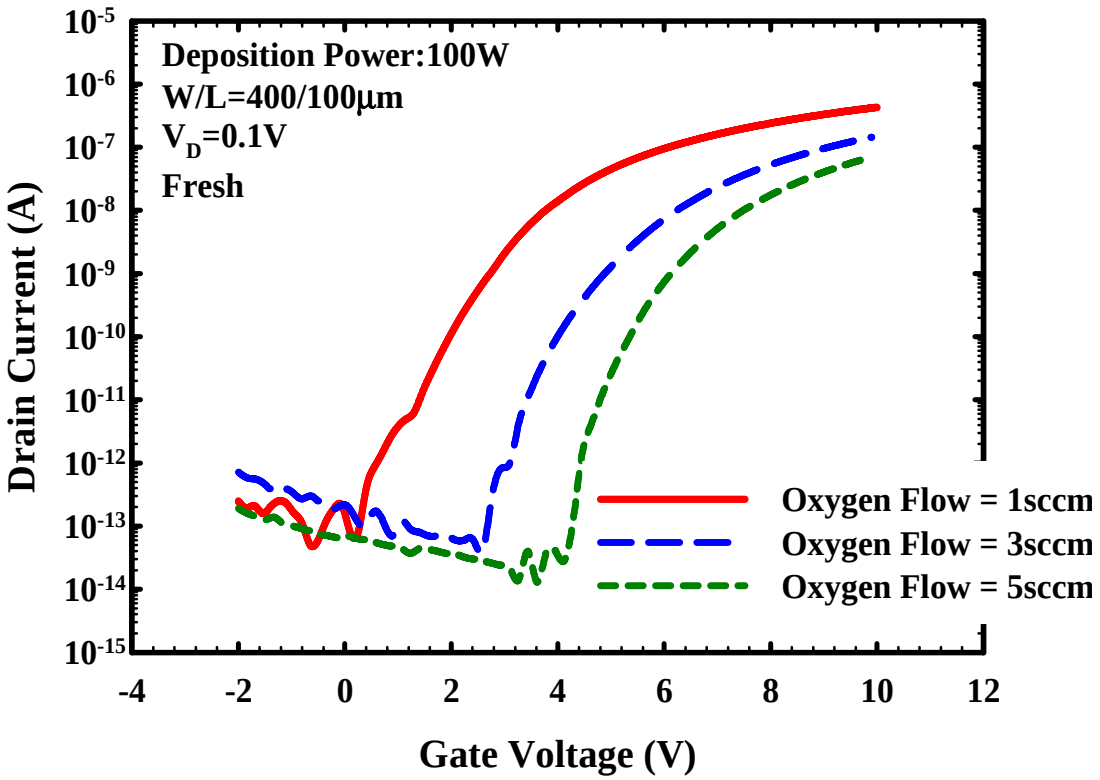
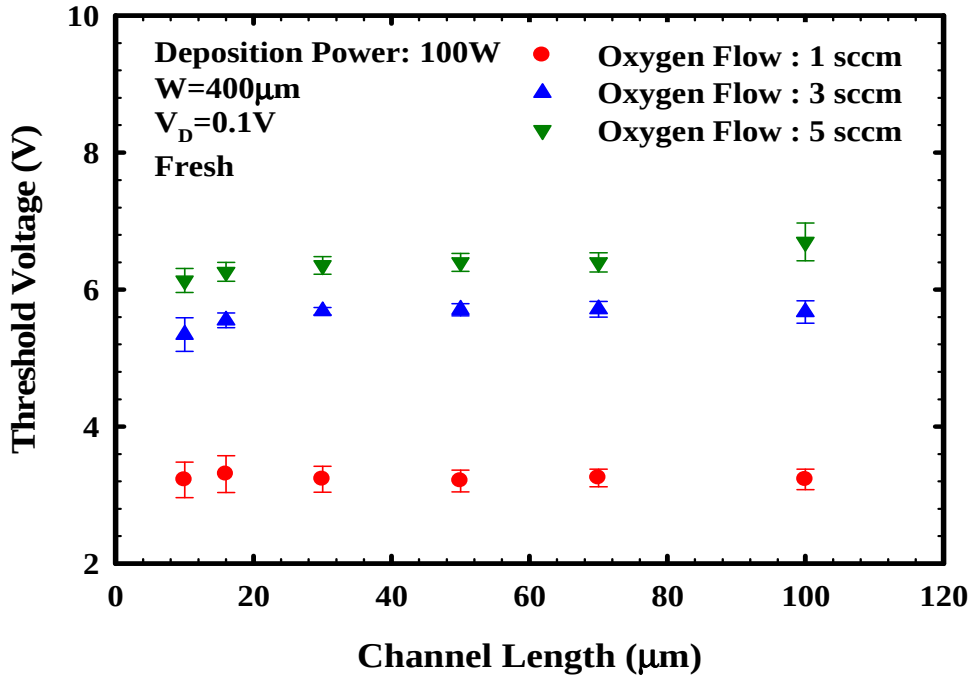
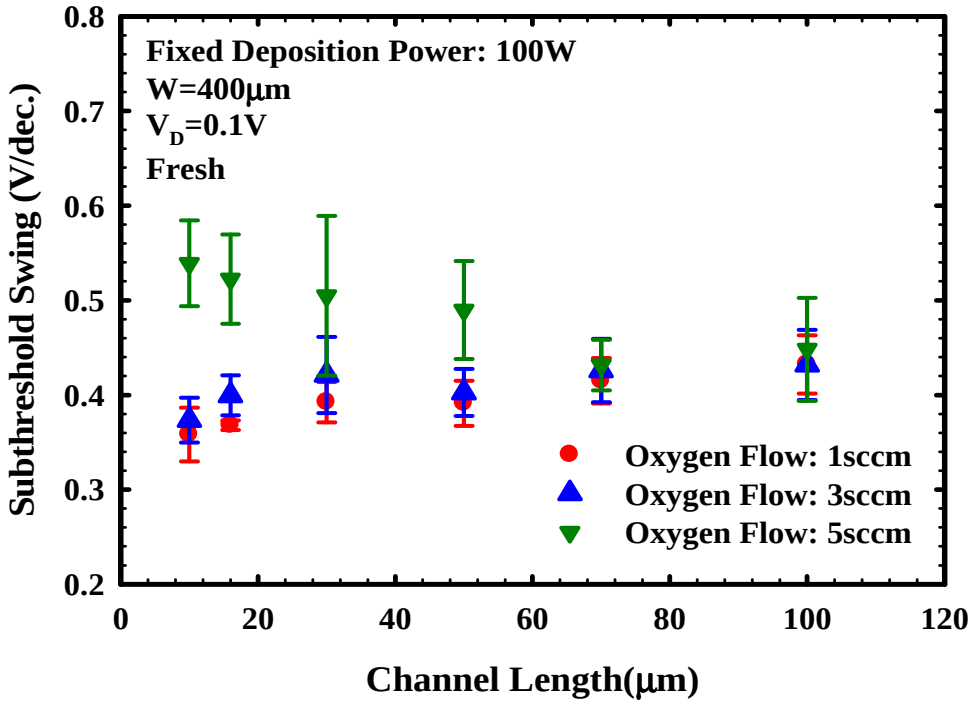


Fig 3.10. Transfer characteristics of α-IGZO devices deposited with in different oxygen flow.

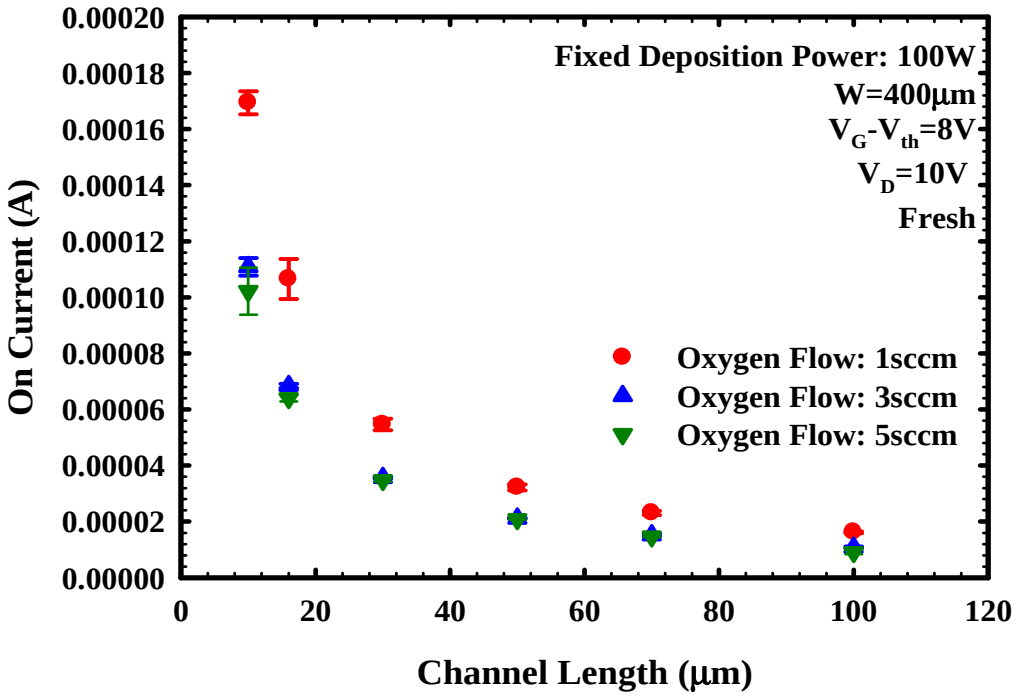


(a)

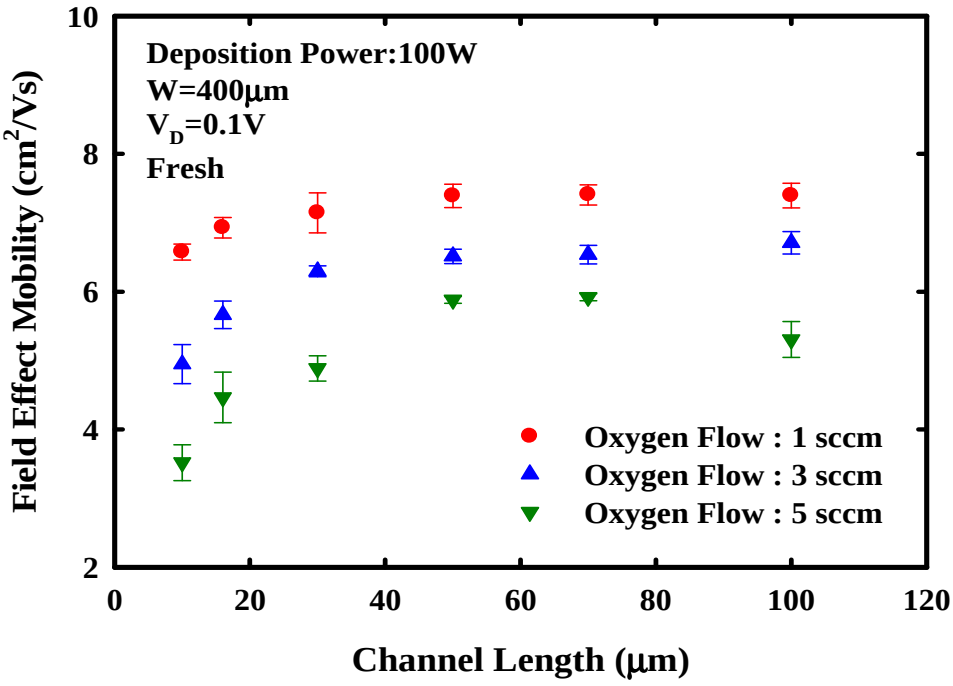


(b)

Fig. 3.11. (a) Extracted threshold voltage and (b) sub-threshold swing as a function of the channel length.

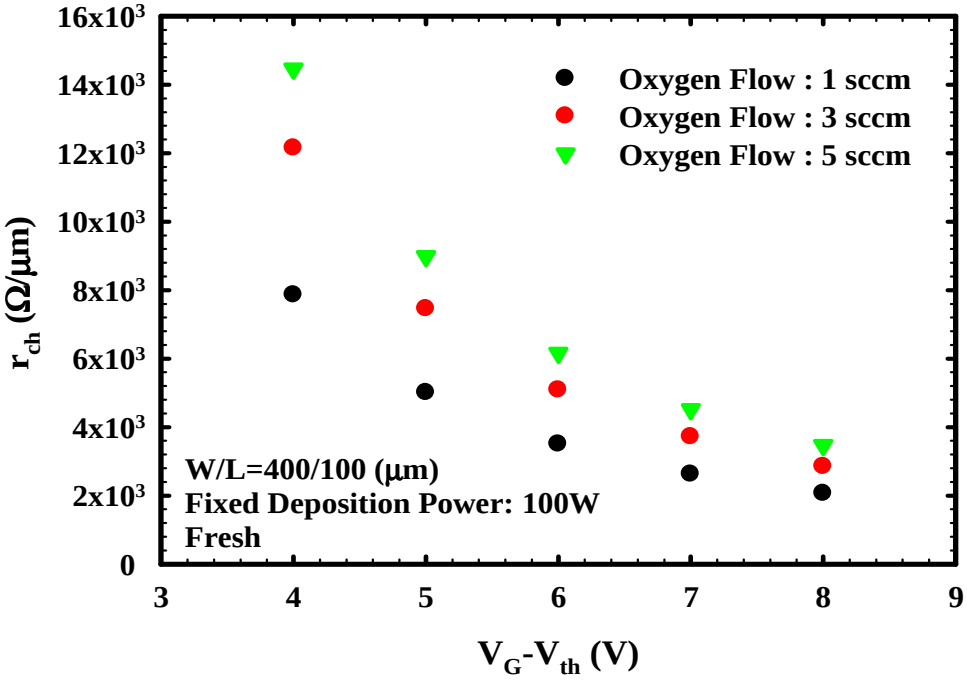


(c)

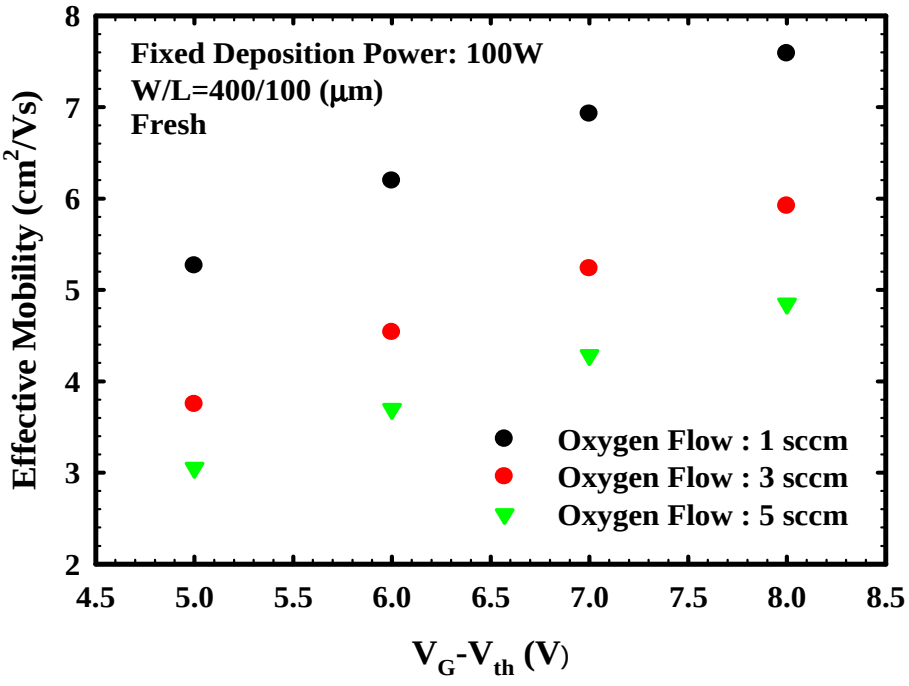


(d)

Fig. 3.11. (c) Extracted on-current measured at V_D=10V and (d) field-effect mobility as a function of the channel length.

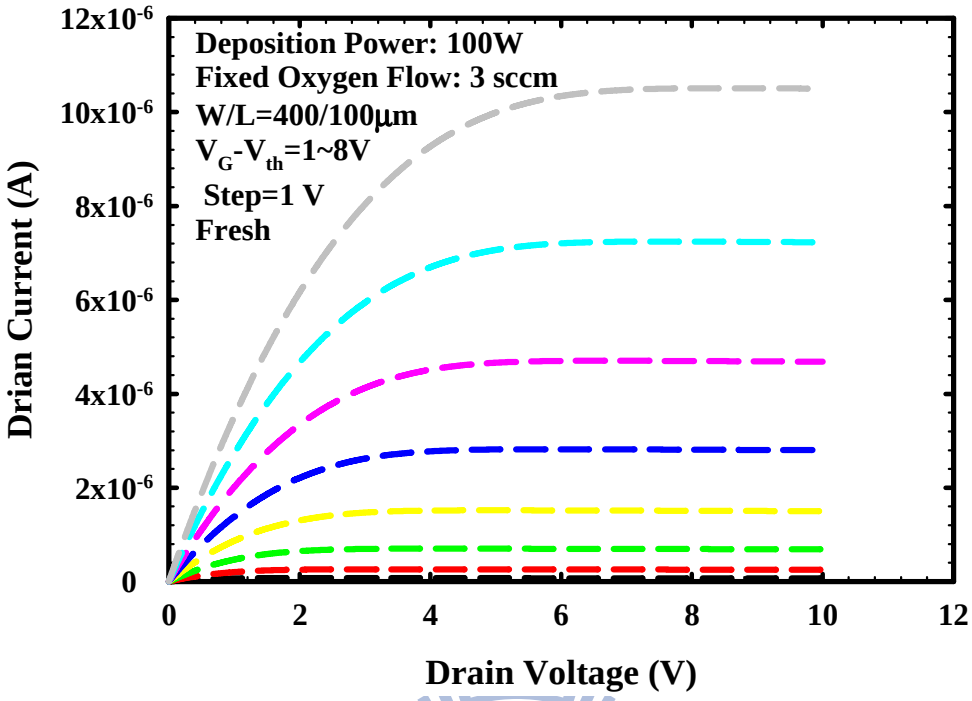


(a)

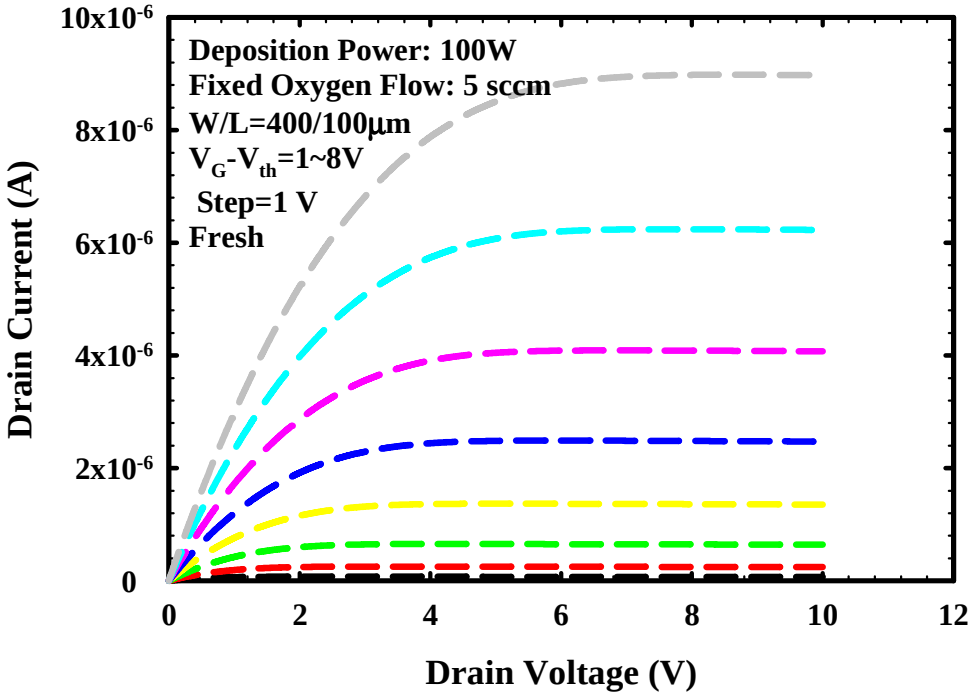


(b)

Fig. 3.12. Extracted (a) channel resistance per micrometer and (b) effective mobility as a function of gate overdrive.



(a)

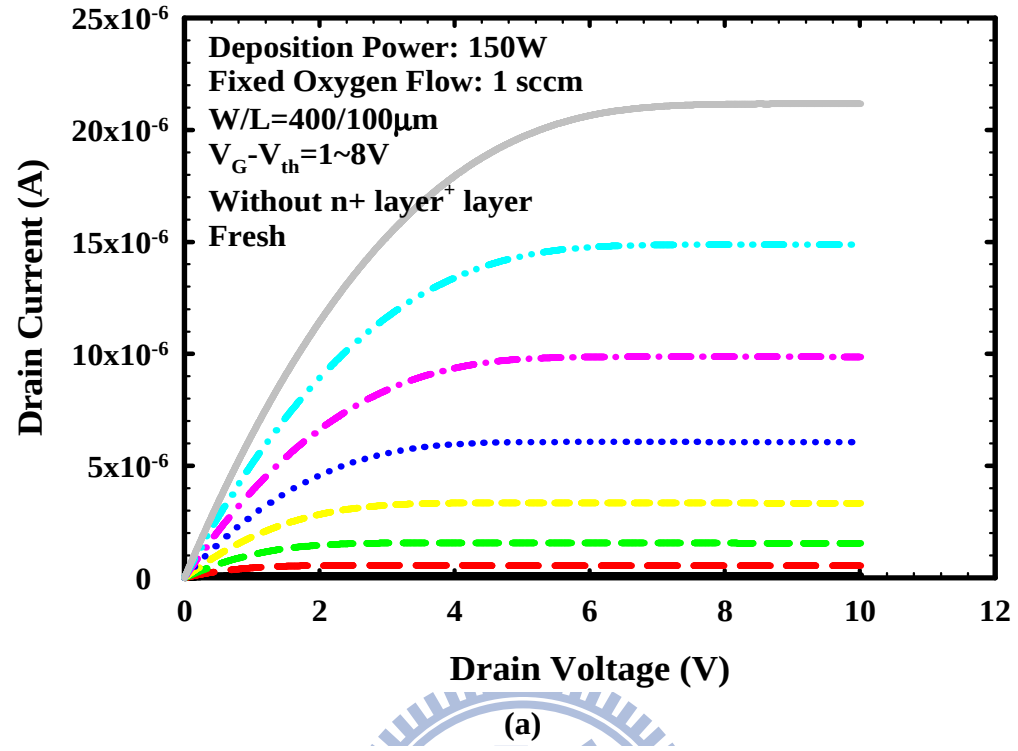


(b)

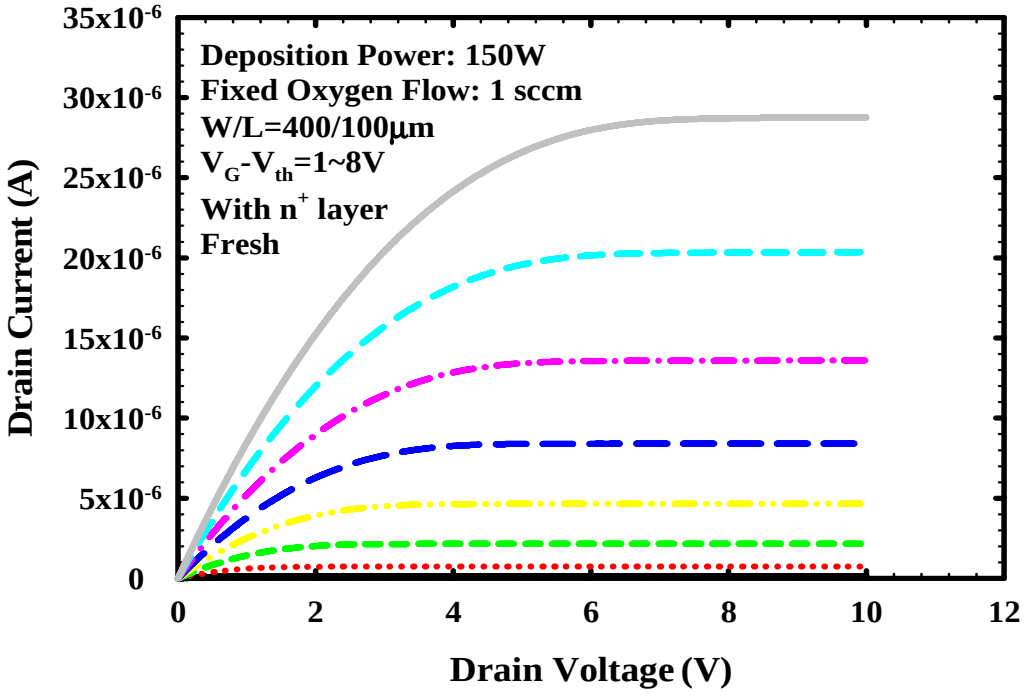
Fig. 3.13. Output characteristic of devices with the channel film deposited at an oxygen flow of (a) 3sccm and (b) 5sccm.

Table 3.2 Summary of electrical characteristics of α-IGZO TFTs with different sputtering deposition parameters. W/L=400μm/100μm.

Deposition Conditions	100W O_2=1 sccm	100W O_2=3 sccm	100W O_2=5 sccm	125W O_2=1 sccm	150W O_2=1 sccm	200W O_2=1 sccm
V_{th} (V)	3.23±0.15	5.67±0.17	6.70±0.28	2.13±0.28	0.66±0.15	0.97±0.07
μ_{FE} (cm^2/Vs)	7.40±0.18	6.71±0.16	5.31±0.26	7.89±0.59	10.22±0.36	14.17±0.08
SS (V/decade)	0.429±0.033	0.432±0.037	0.388±0.039	0.477±0.044	0.476±0.023	0.472±0.035
On current $\times 10^{-5}$ (A)	1.62±0.04	1.08±0.04	0.91±0.08	1.51±0.66	2.10±0.03	2.47±0.11



(a)



(b)

Fig. 3.14. Output characteristics of devices (a) without and (b) with n^+ insertion layer.

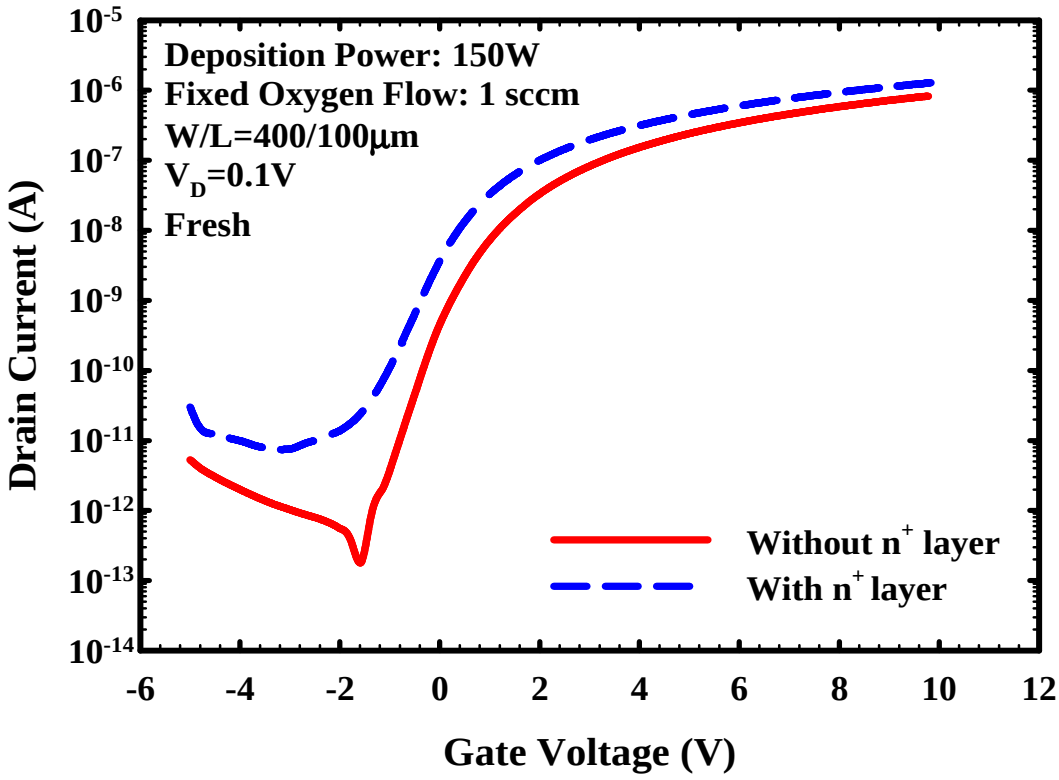
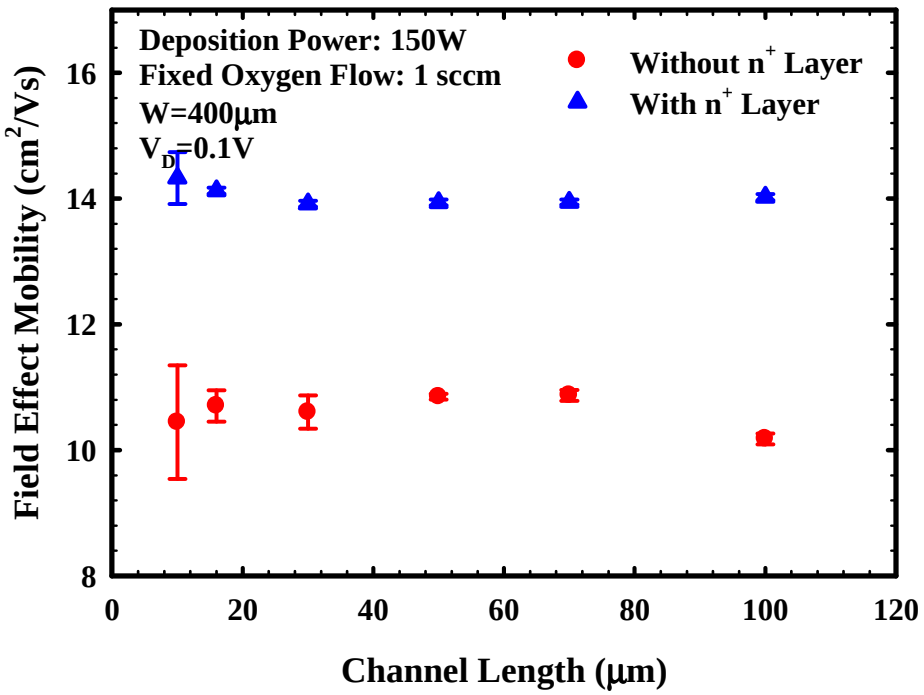
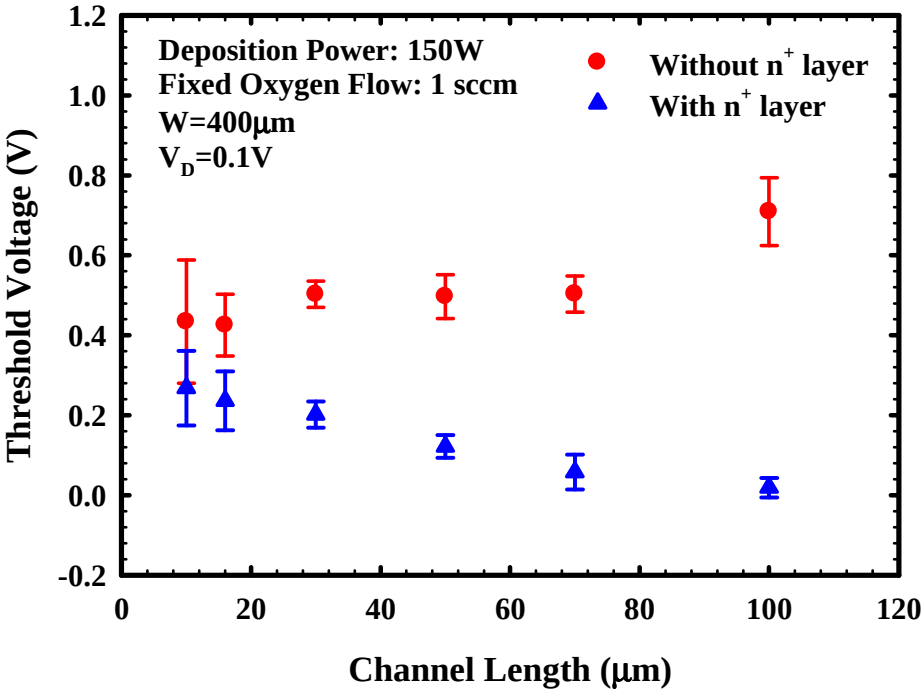


Fig. 3.15. Transfer characteristics of devices with and without n^+ insertion layer.

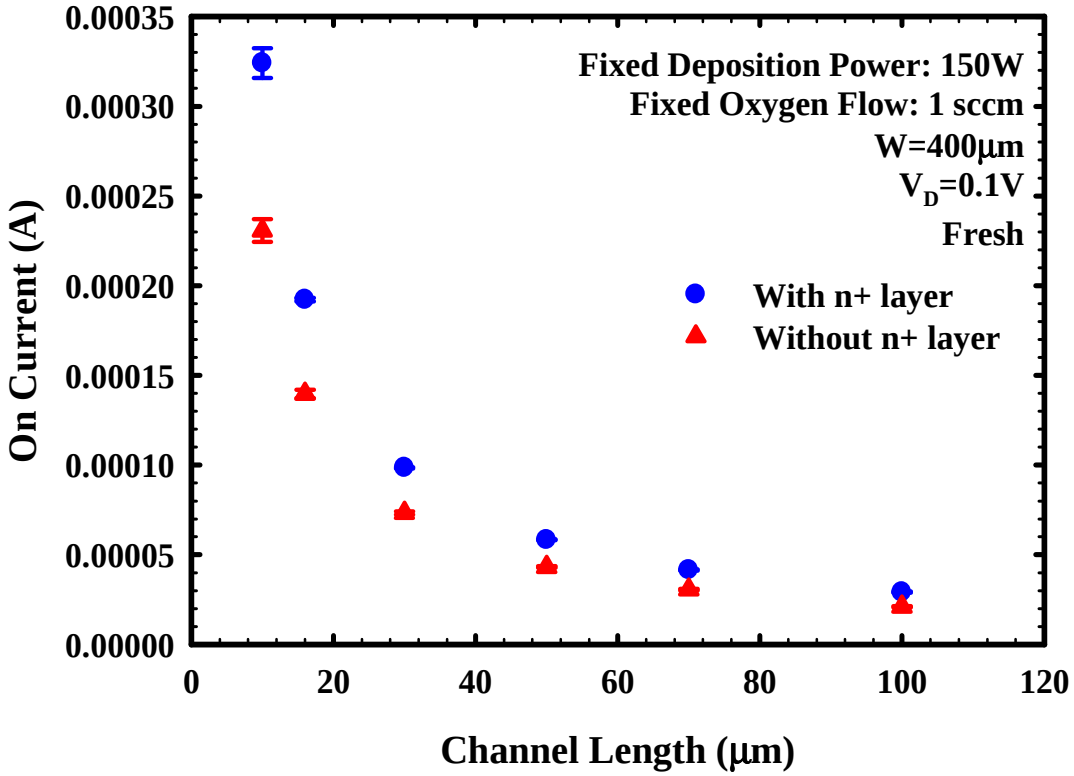


(a)



(b)

Fig. 3.16. (a) Field-effect mobility, (b) threshold voltage, and (c) on-current as a function of channel length.



(c)

Fig. 3.16. (a) Field-effect mobility, (b) threshold voltage, and (c) on-current as a function of channel length.

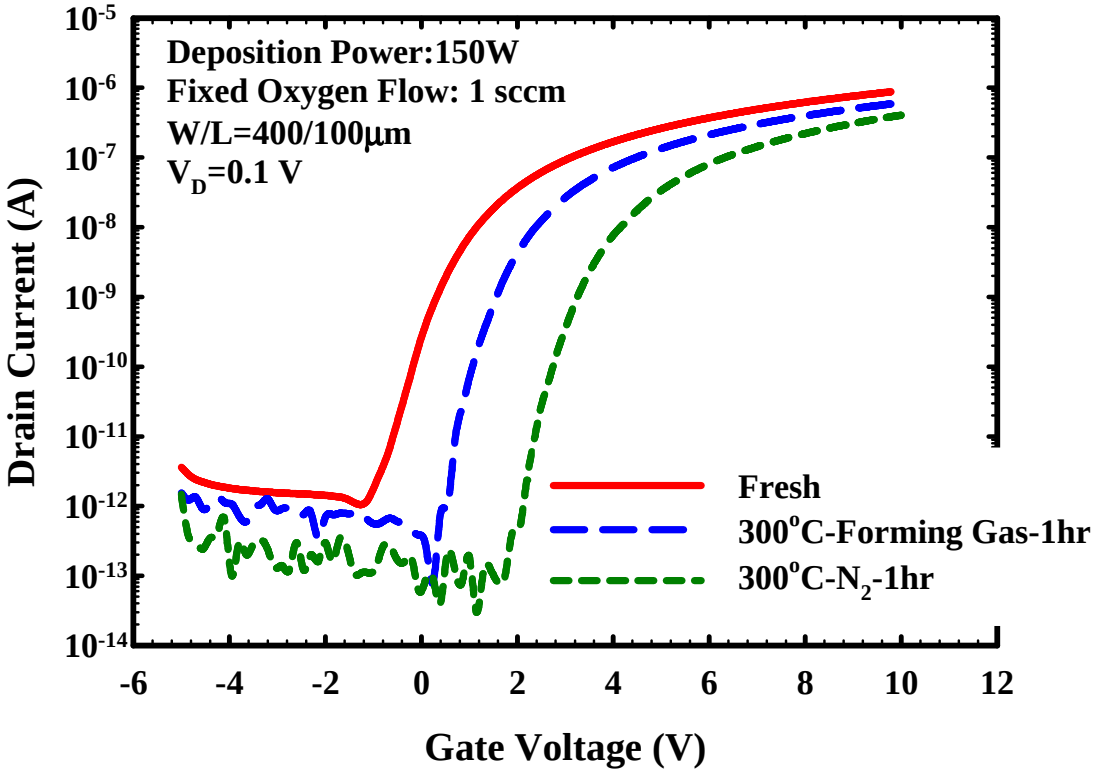
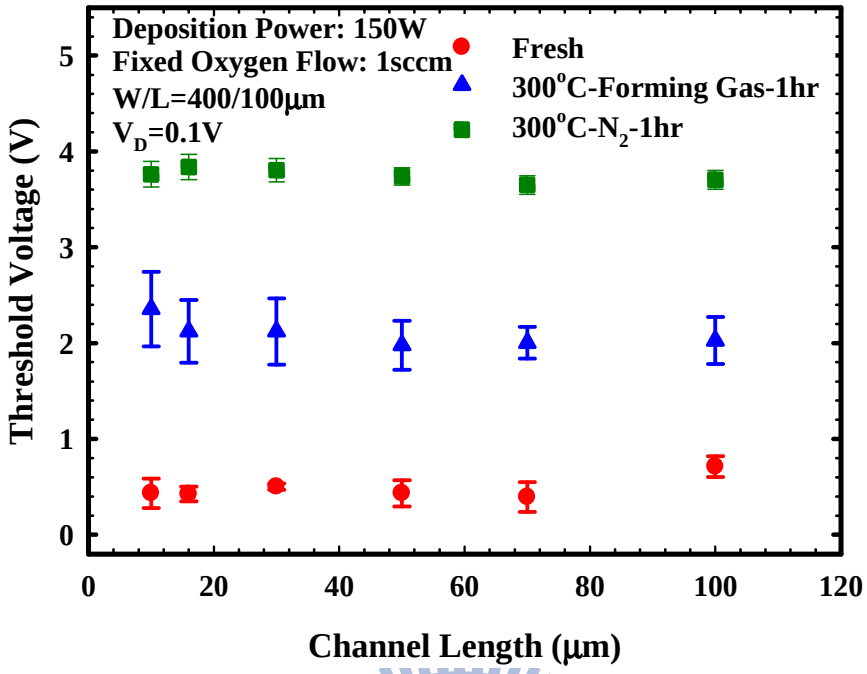
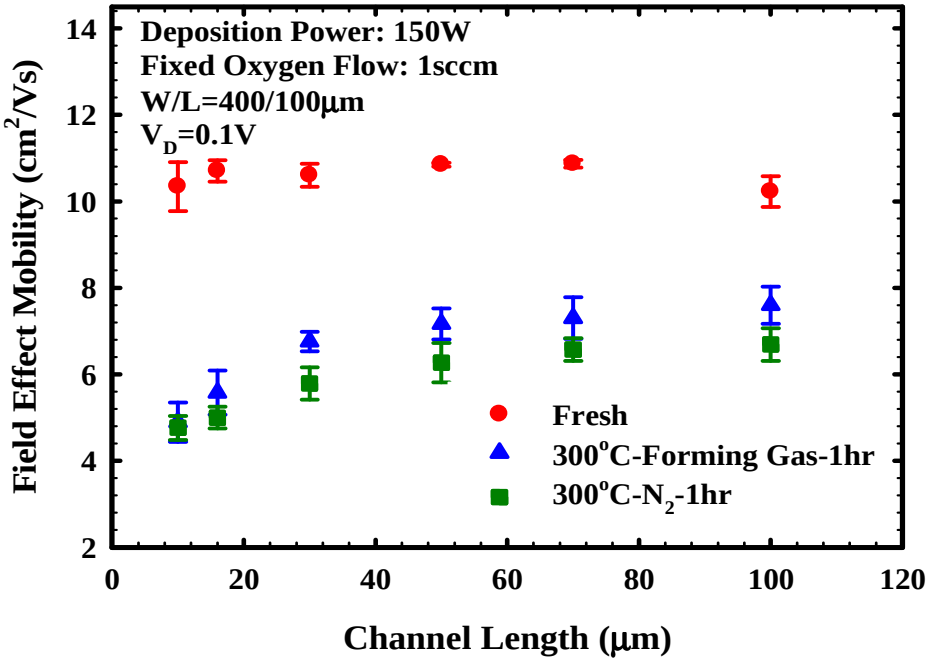


Fig. 3.17. Transfer curves of fresh and post-annealed devices. The annealing time is one hour.

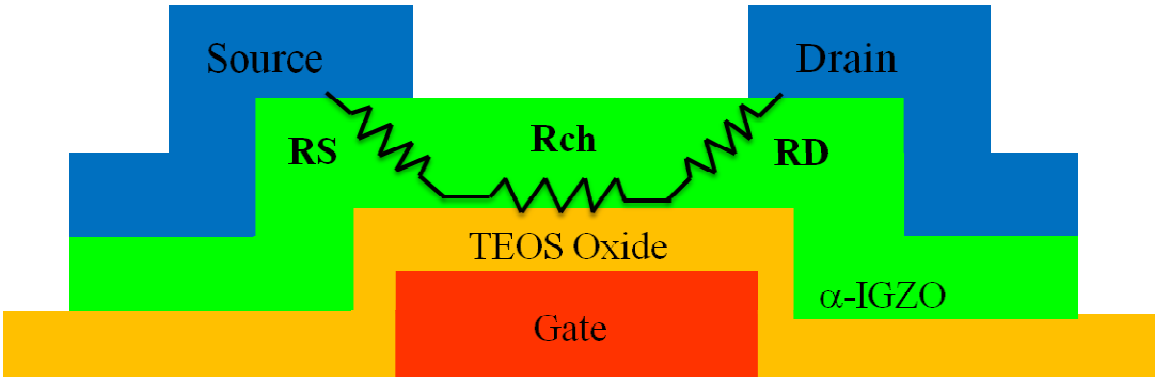


(a)

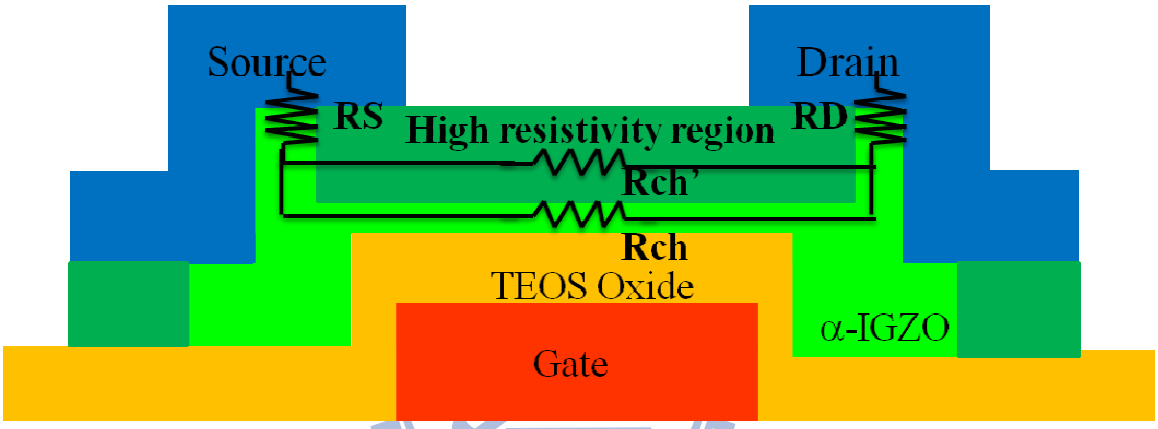


(b)

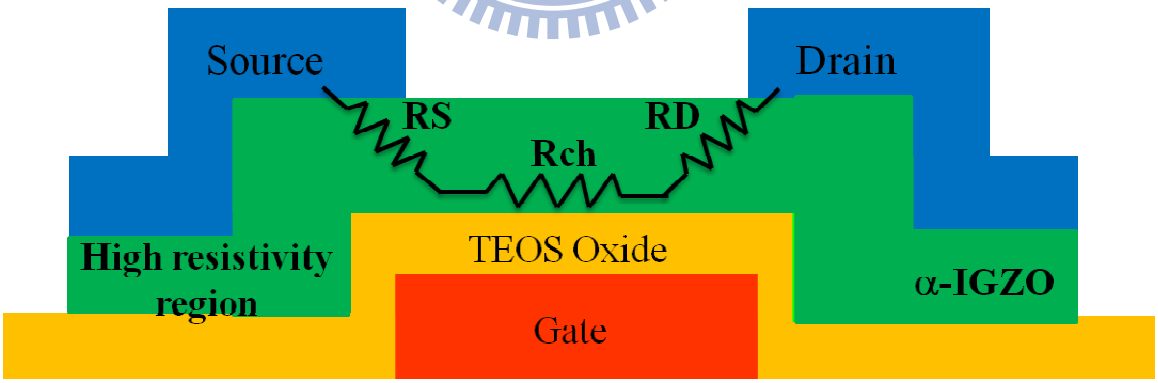
Fig. 3.18. (a) Threshold voltage and (b) field-effect mobility as a function of channel length for fresh and post-annealed devices.



(a)

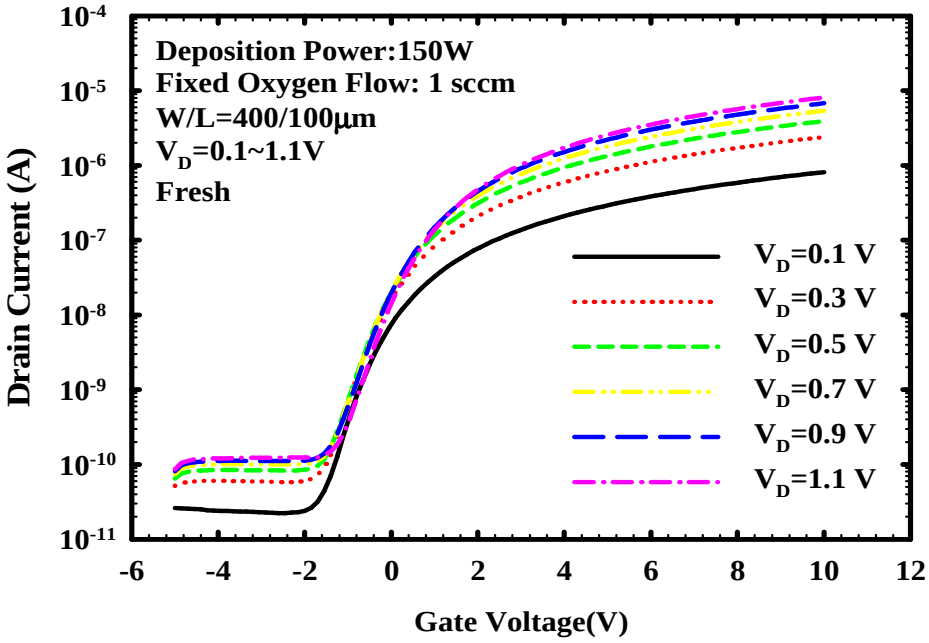


(b)

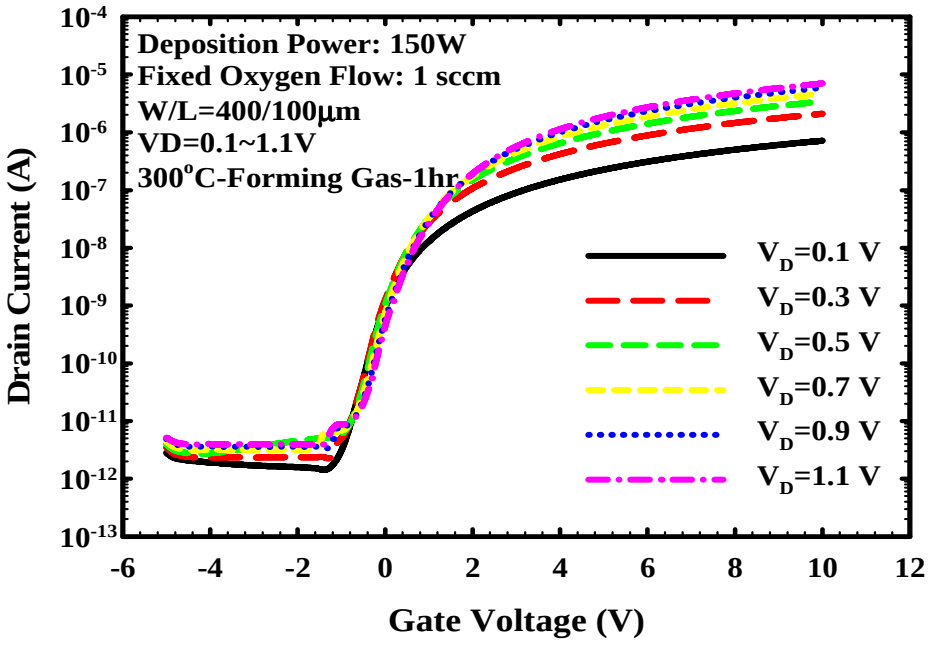


(c)

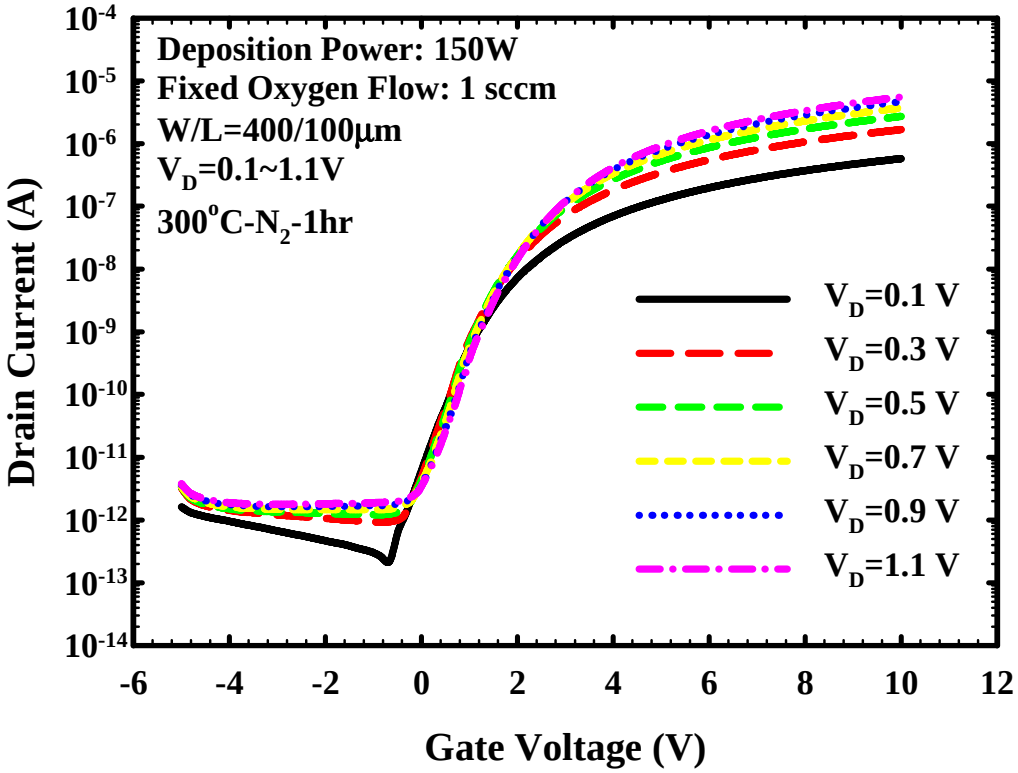
Fig. 3.19. Schematic illustration of the channel composition. (a) A low-resistivity (ρ) channel film for the fresh device. (b) A high-ρ/ low-ρ stacked channel film for the post-annealed device. (c) A high-ρ channel film for the post-annealed device.


Deposition Power:150W
Fixed Oxygen Flow: 1 sccm
W/L=400/100μm
V_D=0.1~1.1V
Fresh
V_D=0.1 V
V_D=0.3 V
V_D=0.5 V
V_D=0.7 V
V_D=0.9 V
V_D=1.1 V
Drain Current (A)
Gate Voltage(V)

(a)


Deposition Power: 150W
Fixed Oxygen Flow: 1 sccm
W/L=400/100μm
VD=0.1~1.1V
300°C-Forming Gas-1hr
V_D=0.1 V
V_D=0.3 V
V_D=0.5 V
V_D=0.7 V
V_D=0.9 V
V_D=1.1 V
Drain Current (A)
Gate Voltage (V)

(b)



(c)

Fig. 3.20. Transfer curves of (a) a fresh α-IGZO TFT, and post-annealed α-IGZO TFTs receiving treatment in (b) forming gas and (c) N_2, respectively.

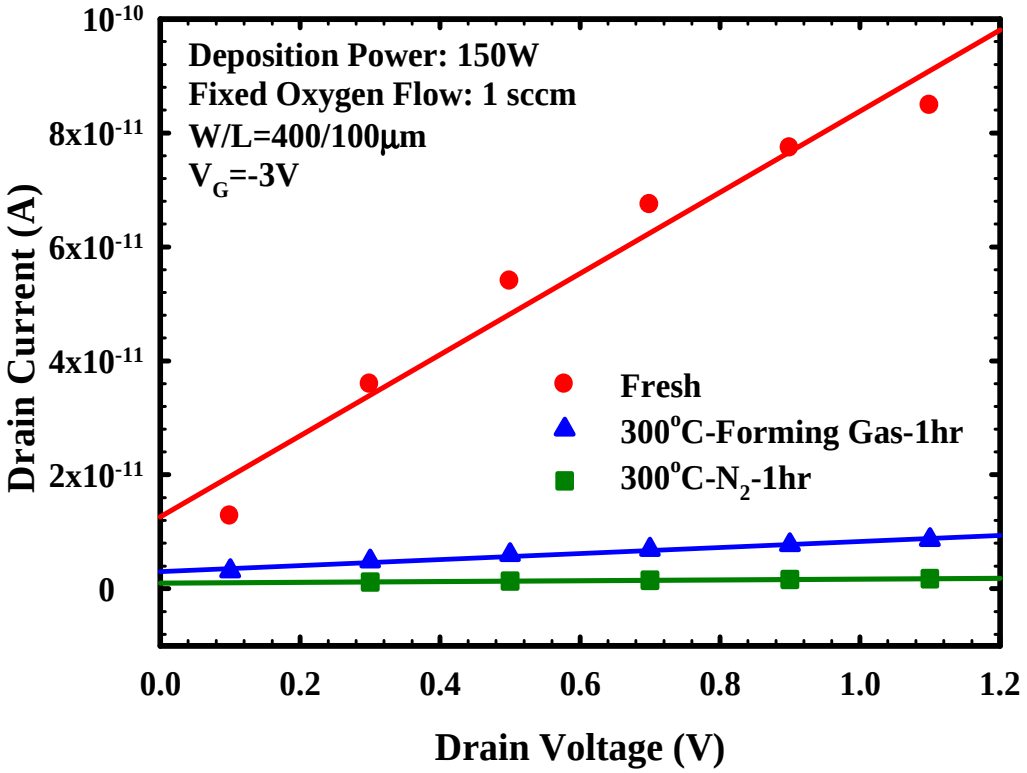


Fig. 3.21. Relations between drain current and drain voltage for fresh and post-annealed devices.

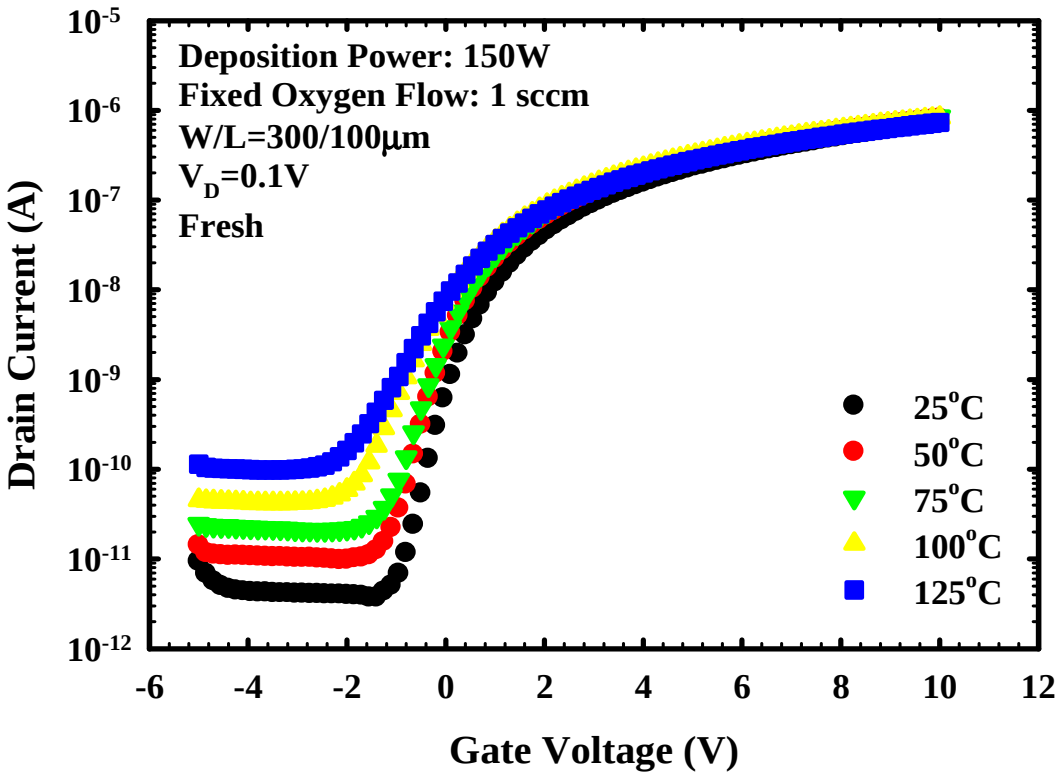
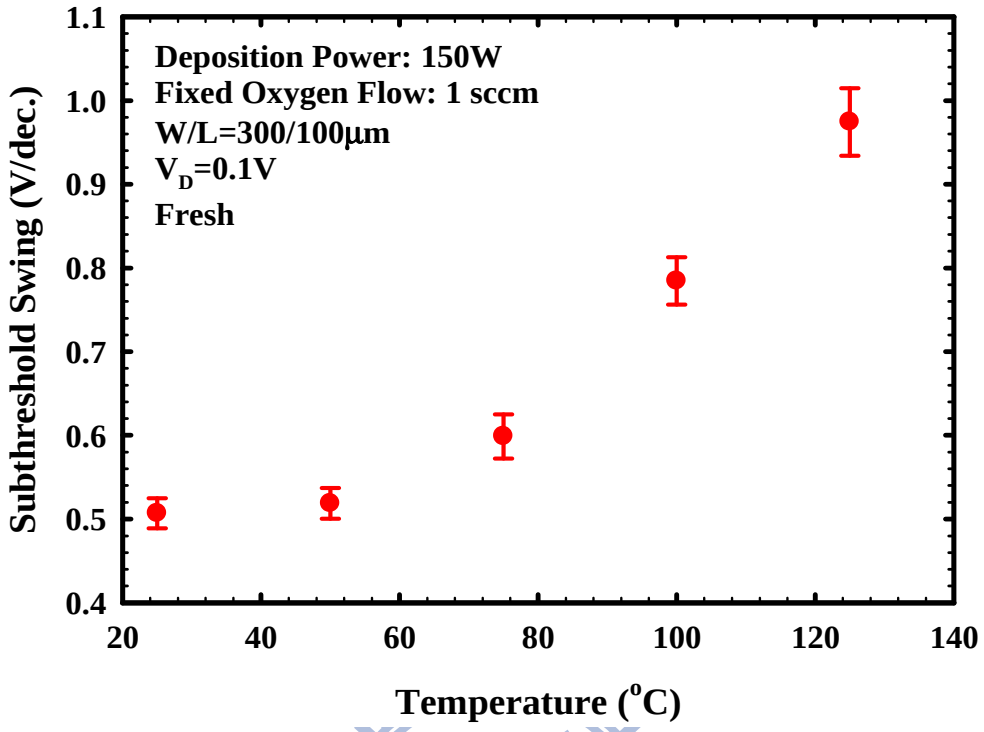
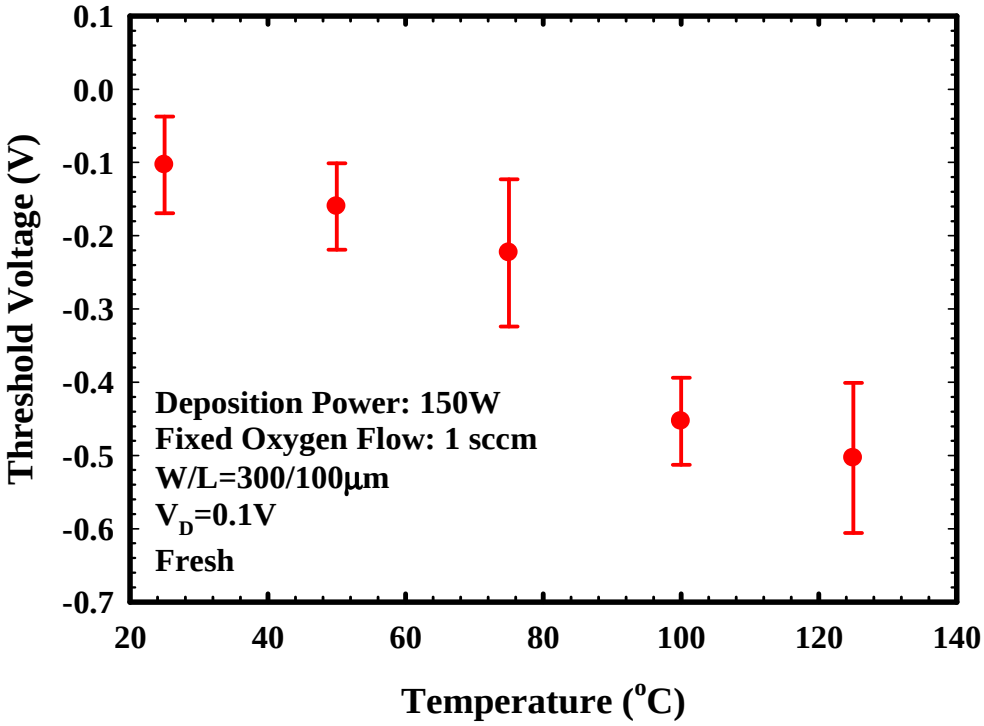


Fig. 3.22. Transfer curves of an α-IGZO device as a function of measurement temperature ranging from 25°C to 125°C.



(a)



(b)

Fig. 3.23. Temperature dependence of (a) SS and (b) V_{th} extracted from α-IGZO devices.

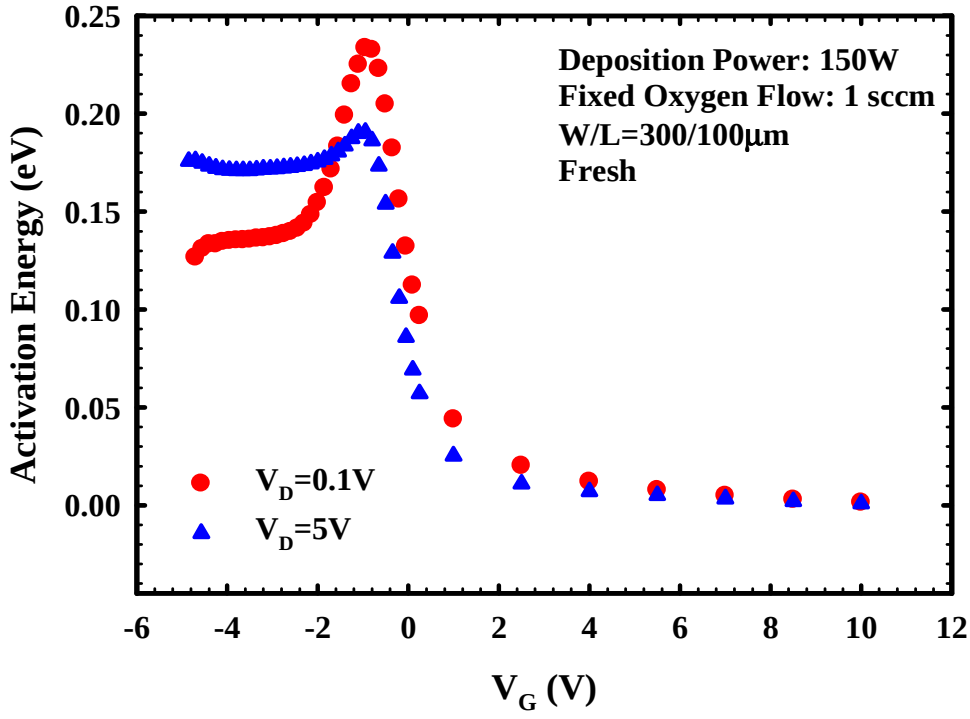


Fig. 3.24. Extracted activation energy as a function of V_G for an α-IGZO device.

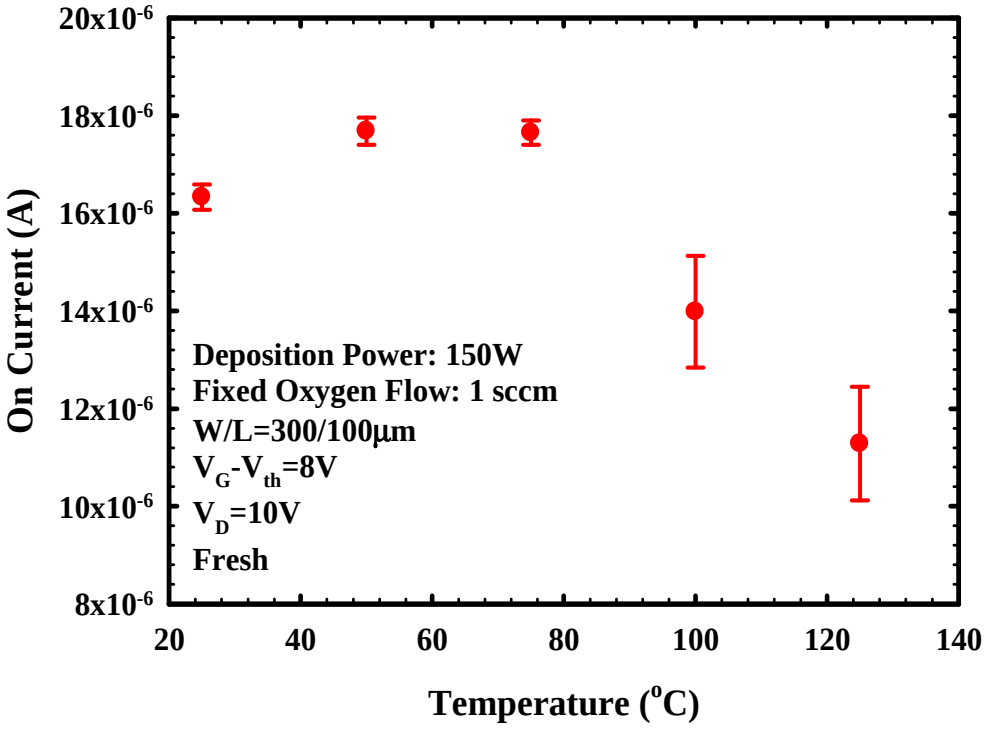


Fig. 3.25. Temperature dependence of on-current for α-IGZO devices.

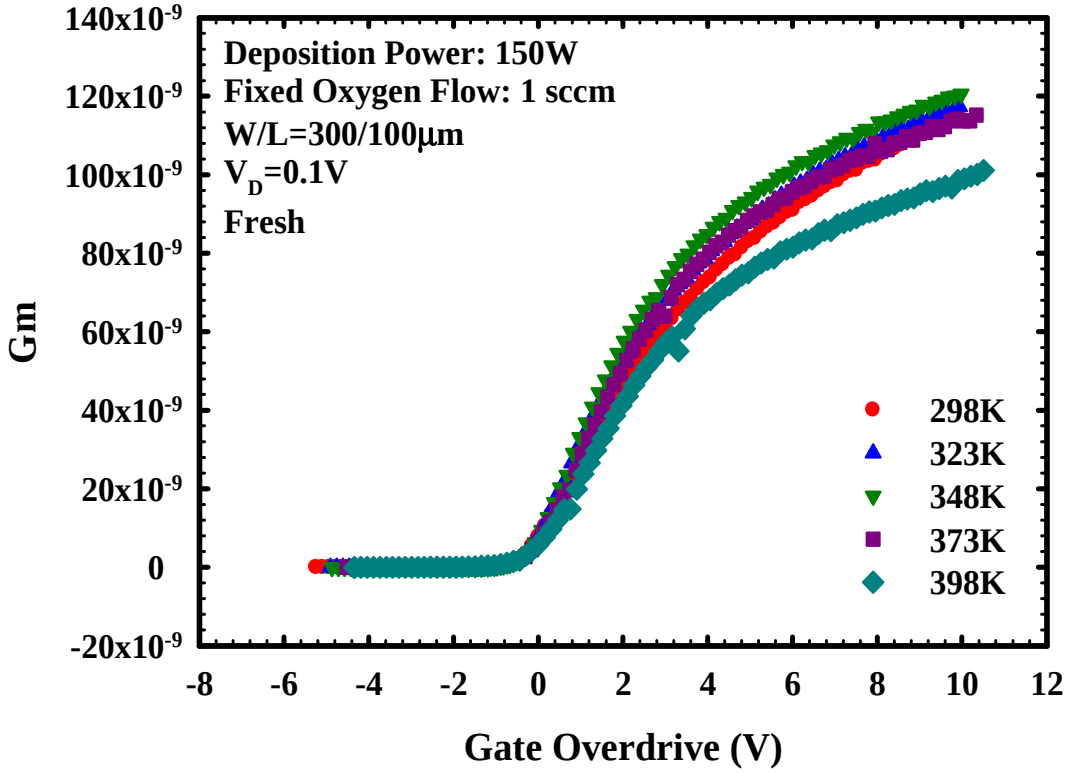
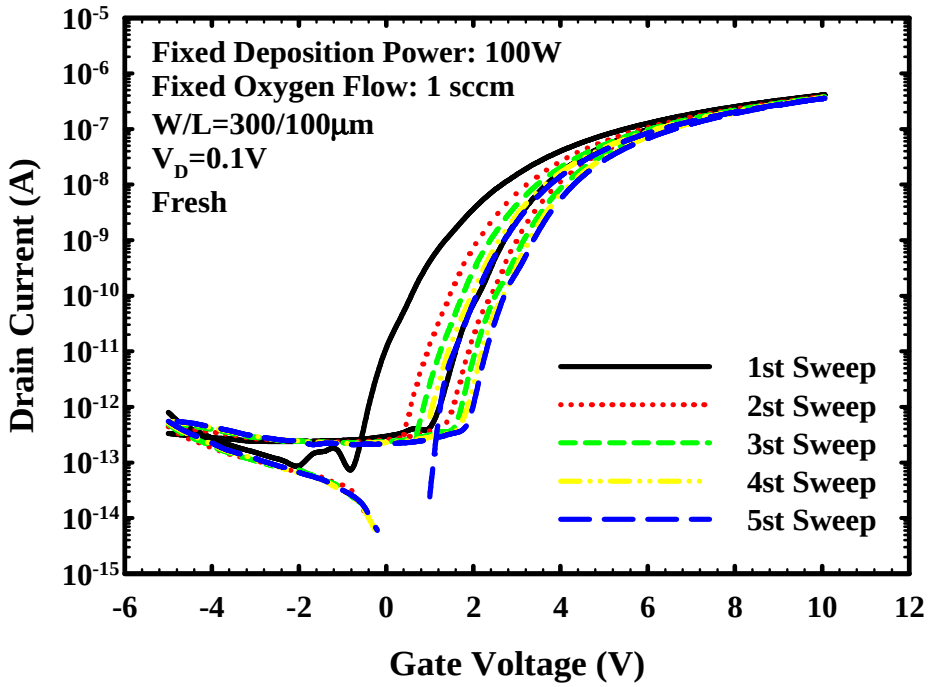
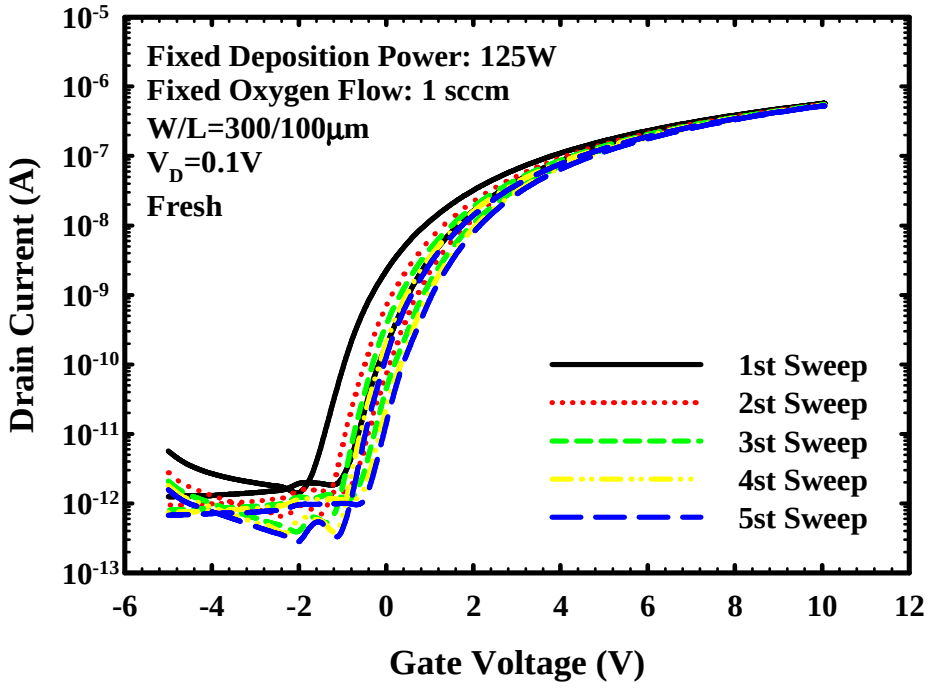


Fig. 3.26. Temperature dependence of transconductance as a function of gate overdrive for an α-IGZO device.

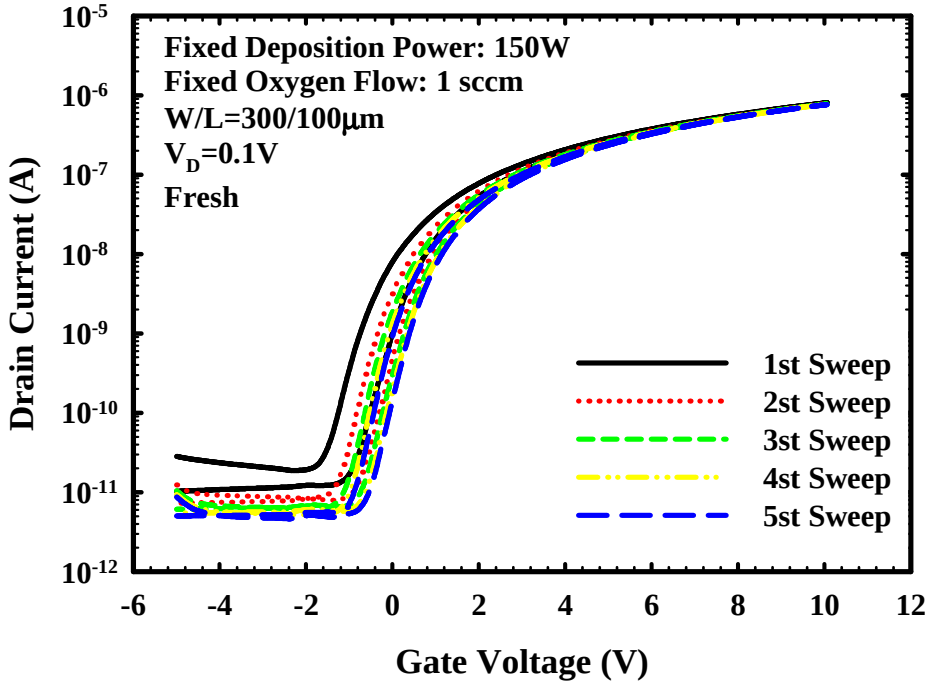


(a)

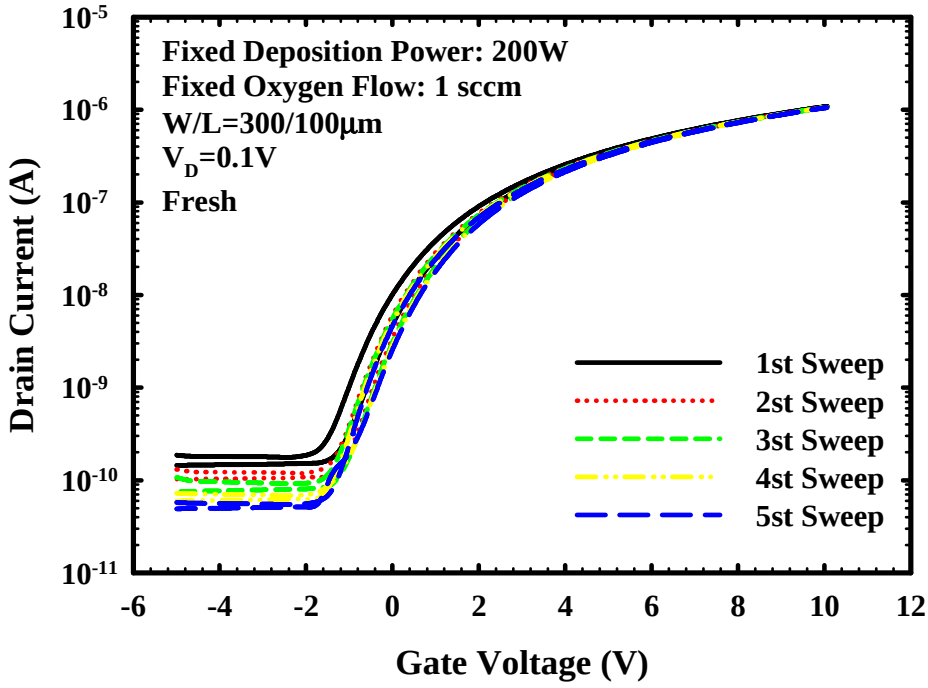


(b)

Fig. 3.27. Transfer characteristics of 5 consecutive FS and RS measurements of α-IGZO TFTs with a fixed oxygen flow and different deposition power of (a) 100W and (b) 125W.

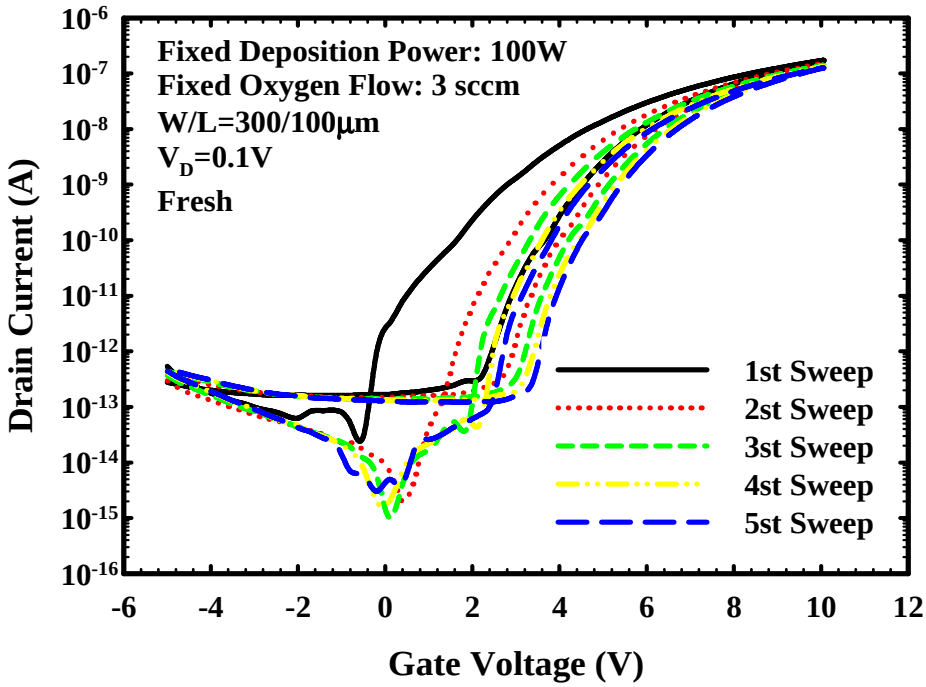


(c)

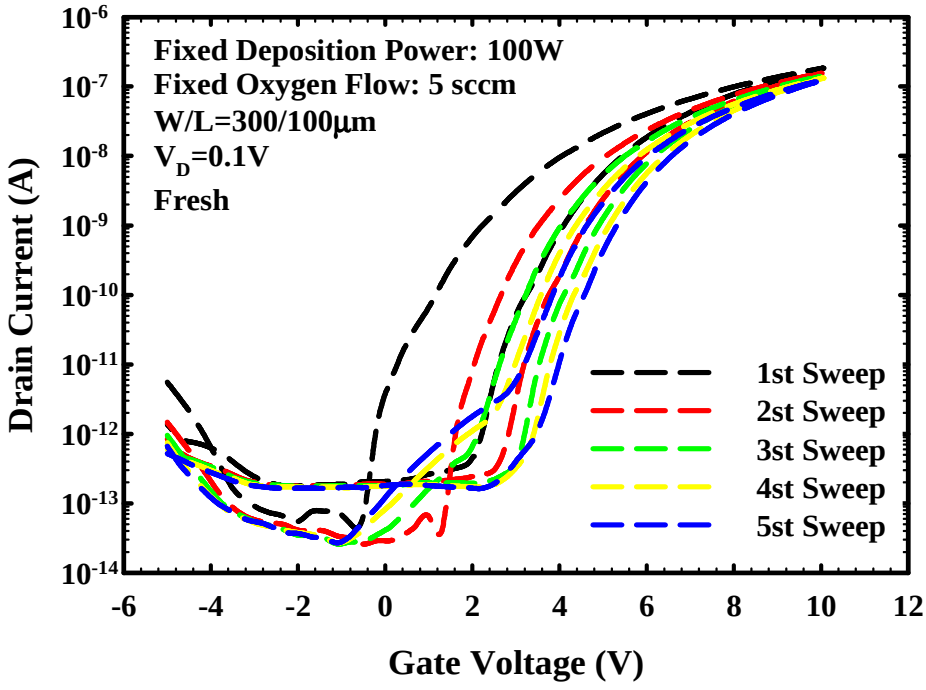


(d)

Fig. 3.27. Transfer characteristics of 5 consecutive FS and RS measurements of α-IGZO TFTs with a fixed oxygen flow and different deposition power of (c) 150W and (d) 200W.

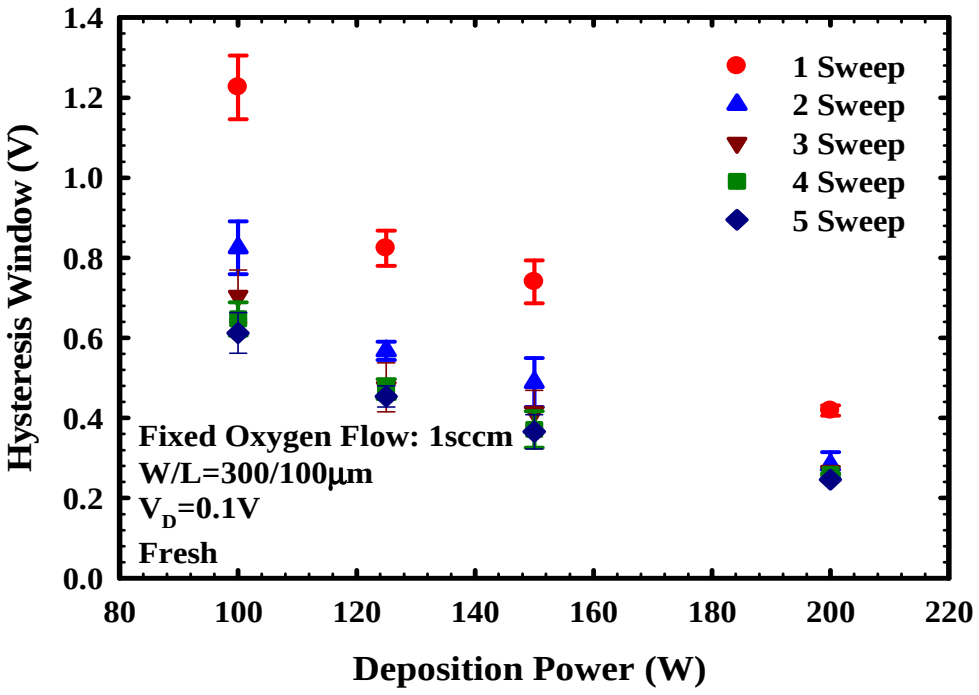


(a)

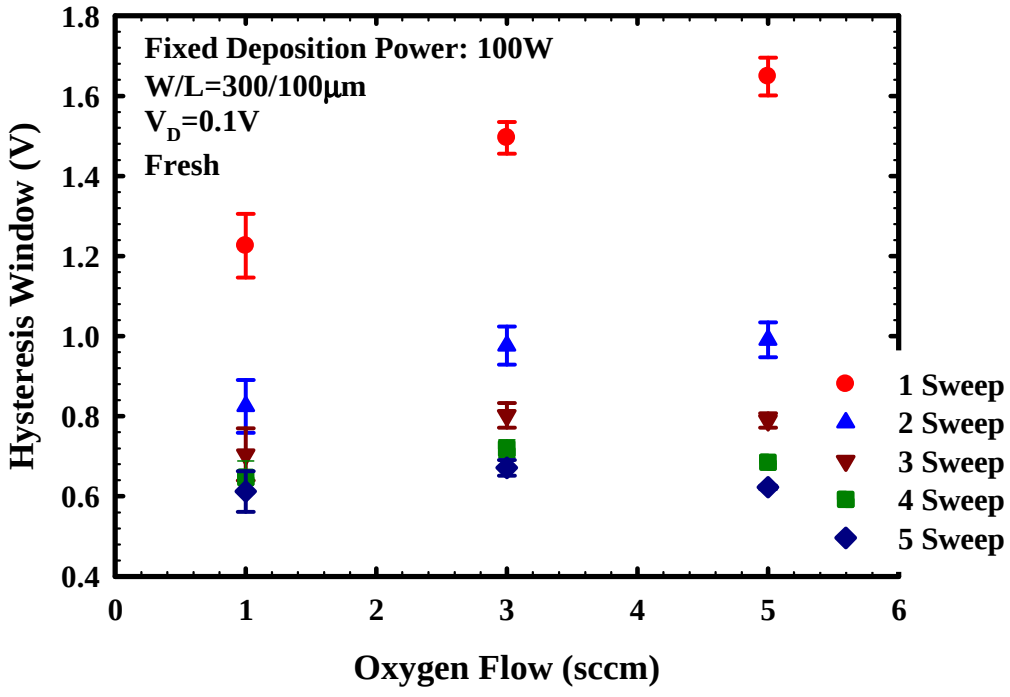


(b)

Fig. 3.28. Transfer characteristics of 5 consecutive FS and RS measurements of α-IGZO TFTs with a fixed deposition power and different oxygen flow of (a) 3sccm and (b) 5sccm.



(a)



(b)

Fig. 3.29. Hysteresis window as a function of (a) deposition power with a fixed oxygen flow of 1sccm and (b) oxygen flow with a fixed deposition power of 100W in α-IGZO devices.

Vita

姓　　名：　顏同偉 Tung-Wei Yen

性　　別：　男

出　　生：　西元 1987 年 2 月 9 日

出 生 地：　台灣 台南市

住　　址：　台南市府安路五段11巷47弄42號

學　　歷：

國立交通大學電子工程研究所	2009 年 9 月 ~ 2011 年 6 月
國立彰化師範大學物理系	2005 年 9 月 ~ 2009 年 6 月
國立台南第二高級中學	2002 年 9 月 ~ 2005 年 6 月
台南市立民德國民中學	1999 年 9 月 ~ 2002 年 6 月
台南市立立人國民小學	1993 年 9 月 ~ 1999 年 6 月

論文題目：

α-IGZO 薄膜電晶體的製作與特性分析

Fabrication and Characterization of α-IGZO Thin Film Transistors

Publication List

[1] Cheng-I Lin, Yee-Shin Lee, Tung-Wei Yen, Horng-Chih Lin, and Tiao-Yuan Huang, “Effect of Annealing Ambient on the Characteristics of a-IGZO Thin Film Transistors.” International NanoElectronics Conference, 21-24 June, 2011.