國立交通大學

電子工程學系　電子研究所

碩士論文

高效能增強型砷化鎵金氧半場效電晶體元件電性研究

The Electrical Characteristics of High Performance Enhancement Mode GaAs Metal-Oxide-Semiconductor Field-Effect-Transistor Devices

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指導教授：簡昭欣 教授

中華民國一〇〇年八月

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摘要

在這篇論文中，我們首先研究以砷化鎵材料沉積氧化鋁介電層的電容其電性特徵。較差的介電層品質會造成頻率響應/頻率分散(frequency dispersion)，延滯現象(hysteresis)，平帶偏移(flab band shift)，和不預期的低介電常數 (dielectric constant)。根據電性上的結果，在做過矽甲烷鈍化的電容展現出不只低的頻率分散而且延滯現象也很小。我們相信做過矽甲烷鈍化的電容可以有效降低砷化鎵氧化物的形成。為了證實我們的推論，我們利用電導的方式去萃取介面缺陷密度的分佈。接著，我們量測原子層沉積氧化鋁介電層於矽甲烷表面鈍化之砷化鎵電容其可靠度，可以透過在不同應力條件下捕捉/釋放電荷清楚了解不同介面的可靠度。我們觀察到矽甲烷表面鈍化後的砷化鎵電容其可靠度有明顯的提升。接下來，我們在砷化鎵的不同晶相上做電性研究，而發現在(111)A 的表面晶相上電容特性獲得了改善。當外加一個更大的正電壓，能帶可

以向下彎曲使表面的本質能階E_i低於費米能階E_F。換句話說，砷化鎵能隙中間的介面缺陷值降低，使費米能階可以移動到接近傳導能階。我們認為是不同晶相的表面的結構產生的改善。

串聯電阻的大小是影響金氧半場效電晶體元件效能的重要因素，源極/集極的電阻將會抑制最大驅動電流。我們利用ＣＴＬＭ這種結構討論其串聯電阻包括片面電阻率(sheet resistivity)和接觸電阻率(contact resistivity)。根據這些電性特徵，我們發現片面電阻率在30keV&80keV的離子佈植能量比在50keV的離子佈植能量來的小，然而接觸電阻卻是相反。除此之外，由活化溫度的條件觀點來看，我們發現片面電阻率在850℃比在950℃活化溫度來的小，然而接觸電阻卻是相反。我們統整可以找到最理想的條件為50keV的離子佈植能量和活化溫度850℃。但接面二極體在950℃活化溫度和合金金屬400℃30s的條件下順向電流沒有明顯的被抑制。我們將片面電阻率、接觸電阻率和歐姆接觸的條件優化，最後利用這些條件在不同晶相上將金氧半場效電晶體元件成功製作出來並量測其特性。除此之外，我們也製作出砷化鎵嵌入鍺源極和集極的金氧半場效電晶體元件並探討其特性。

The Electrical Characteristics of High Performance Enhancement mode GaAs Metal-Oxide-Semiconductor Field-Effect-Transistor Devices

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Abstract

In this thesis, firstly, we have studied the electrical characteristics of GaAs capacitors with Al_2O_3 dielectric. Poor dielectric quality results in frequency dispersion, hysteresis, flab band shift, and unfavorable low dielectric constant. According to these electrical characteristics, the passivation sample displayed not only small frequency dispersion, but also small hysteresis. We believed that the surface treatment of SiH_4 passivation can efficiently diminish the formation of GaAs native oxide, and improve the effect of Fermi-level pinning phenomenon. In order to confirm the speculation, we used the conductance method to extract distributions of D_{it} for different interface passivation. Next, we measured the reliability of silane surface passivated for gallium arsenide capacitors with atomic-layer-deposited Al_2O_3 gate dielectrics. A clear understanding of reliability of different interfaces, via charge trapping/detrapping studies under different stressing condition, we observed the silane passivation can improve the reliability of gallium arsenide capacitors. Then, we studied the electrical characteristics on GaAs MOS capacitor with the different surface orientation of substrates. The characteristics was improved on GaAs MOS capacitor with (111)A surface orientation. When a larger positive voltage is applied, the bands bend more downward so that the intrinsic level E_i at the surface crosses over the Fermi level E_F. On the other hand, the velue of D_{it} in the middle of energy bandgap was reduced, so the E_F of surface on GaAs could reach to near conduction level. We assumed that the improvement resulted from the different structure of surface on orientation.

The series resistance is an importance factor for metal-oxide-semiconductor field effect transistors (MOSFET) device performance. The source/drain (S/D) resistance will suppress the maximum driving current. We discussed series resistance including sheet resistivity and contact resistivity by CTLM structure. According to electrical characteristics, we discovered that the sheet resistivity at 30keV&80keV is lower than 50keV implant energy. However, the contact resistivity is just contrary. In addition, from the point of temperature, we found that the sheet resistivity at 850℃ is lower than 950℃, and the contact resistivity is just contrary. We can conclude the optimized condition for GaAs ohmic contact that was implanted at 50keV and the activation temperature at 850℃. But, the junction of forward current was not suppressed significantly at activation temperature 950^{o}C and alloy metal 400^{o}C 30s. We optimized conditions of sheet resistivity, contact resistivity, and Ohmic RTA time. Finally, we used these conditions to fabricate metal-oxide-semiconductor field effect transistors with the different surface orientation successfully and measured electrical characteristics. In addition, we also fabricated GaAs MOSFET with embedded Ge source/drain and studied electrical characteristics.

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Chapter 1

Introduction

1.1 General Background

As Researchers continue to devotes on scaling transistors to conform with Moore's Law to sub-16-nm dimensions, it becomes very difficult to maintain the required device performance. However, the increase in drive currents for faster switching speeds at lower supply voltage is largely growing leakage current, which leads to a large standby power dissipation. There is an important need to explore novel channel materials and device structures that would provide nanoscale MOSFETs.

In recent years, Shrinking the dielectric thickness and channel length to get better performance, but silicon-based complementary metal oxide semiconductor (CMOS) with planar structures are approaching fundamental physical ultimate scaling limit. III-V metal-oxide-semiconductor field transistors (MOSFET) provide high electron mobility and low power consumption because of small effective mass. Then, due to availability of high electron mobility, this has led to alternative channel materials that exhibit significantly outperform the scaled Si MOSFET. The first GaAs MOSFET was reported by Becke and White in 1965 [1]. Although SiO_2 is used as the gate dielectric with an amount of interface trap, the devices were operated successfully showing feasibility of this approach. But, SiO_2 is not right gate dielectric for III-V materials.

A variety of dielectrics have been investigated. For example, native oxides on GaAs as gate dielectrics were studied. However, none of method is optimistic approach to achieve GaAs MOSFET [2-9]. Therefore, deposited oxides were also intensively studied. In 1987, researchers at Bell Labs discovered that sulfides are able to passivate GaAs interface [10-11]. In 1995, Prsslack and M. Hong reported in-situ deposition of Ga_2O_3(Gd_2O_3) dielectric on GaAs surface by MBE[12-14]. Later, a serial of device works were carried out after the breakthrough in material science, including GaAs depletion-mode, enhancement MOSFET, GaAs complementary MOSFETs and GaAs power MOSFETs [15-18]. At the end of 2001, Ye and Wilk started to use ALD to despite high-k such as Al_2O_3, HfO_2 on GaAs. Later, detailed interface studies were carried out to demonstrate the unpinning of Fermi-level in III-V compound semiconductors using ALD high-k dielectrics [19-21].

IMEC had demonstrate the device scaling roadmap of performance as shown Fig.1.1. III-V/Ge materials maybe be applied for sub-11-nm dimensions. Besides, In Fig. 1.2 is combination of III-V and Ge channel structure according to Takagi et al.

1.2 Motivation

III-V metal-oxide-semiconductor field transistors (MOSFETs) have the main obstacle that it is lack of high quality, thermodynamically stable gate dielectrics similar to SiO_2 on Silicon. So one key challenge in the III-V technology is that reduce the interface density of states (D_{it}) that induce the Fermi level pining. The suitability of insulator/III-V interfaces for MOSFETs applications has been addressed by appropriate interface control using some surface passivation such as amorphous mixed oxide Ga_2O_3 (Gd_2O_3) and sulfur. However, the methods are not suitable. It is because former’s cost is large and latter’s interface state densities are usually high. We have to research low cost and efficiently to reduce the density of states.

In addition, we know these resistances affect on forward current of junction such as contact resistances. If the value of resistance is higher, the forward currents decrease. And then, the performance of devices will degrade. Therefore, we have to research reasonable conditions to optimize it.

Although their small transport mass leads to high mobility, III-V materials have low density of states (DOS) and the limited dopant level. Due to GaAs is almost lattice matched of Ge. Therefore, Ge can be applied on n^+-source/drain to provide electrons that maybe solute these intrinsic issues.

1.3 Organization of the Thesis

In **Chapter 2**, we studied MOS capacitors and MOSFETs for different orientation on GaAs (100) and (111)A surface. The results of MOS capacitors electrical characteristics on GaAs (111)A surface are very different that compared to (100) surface. And then, we discussed series resistance including sheet resistivity and contact resistivity. We explored sheet resistivity and contact resistivity by CTLM structure. Next, we studied the junction for different activity temperature. Finally, we optimize conditions of sheet resistivity, contact resistivity, and Ohmic RTA time, and then, we applied these conditions on MOSFET.

In **Chapter 3**, we measured the electrical characteristic of GaAs capacitors with Al_2O_3 dielectric, including C-V measurement and conductance. We also studies electrical characteristic of sample with silane passivation and PDA compared to sample without passivation. Next, we analyzed reliability for silane passivation. A clear understanding of reliability of the different interfaces, via charge trapping/detrapping studies under different stressing condition. Finally, we applied this passivation on MOSFET.

In **Chapter 4**, we fabricate GaAs NMOSFET with embedded-Ge source/drain to solute the issues of low density of states (DOS) and the limited dopant level. But n^+-Ge contact has been a challenge in E_F pinning on metal/ n^+-Ge interface. We used TiO_2 interfacial layer to let the electrical characteristics of GaAs NMOSFET with embedded-Ge source/drain be imporved.

In **Chapter 5**, we conclude these studies including different orientation, silane passivation, sheet resistivity, contact resistivity, junction and MOSFET. Finally, we gave some future works.

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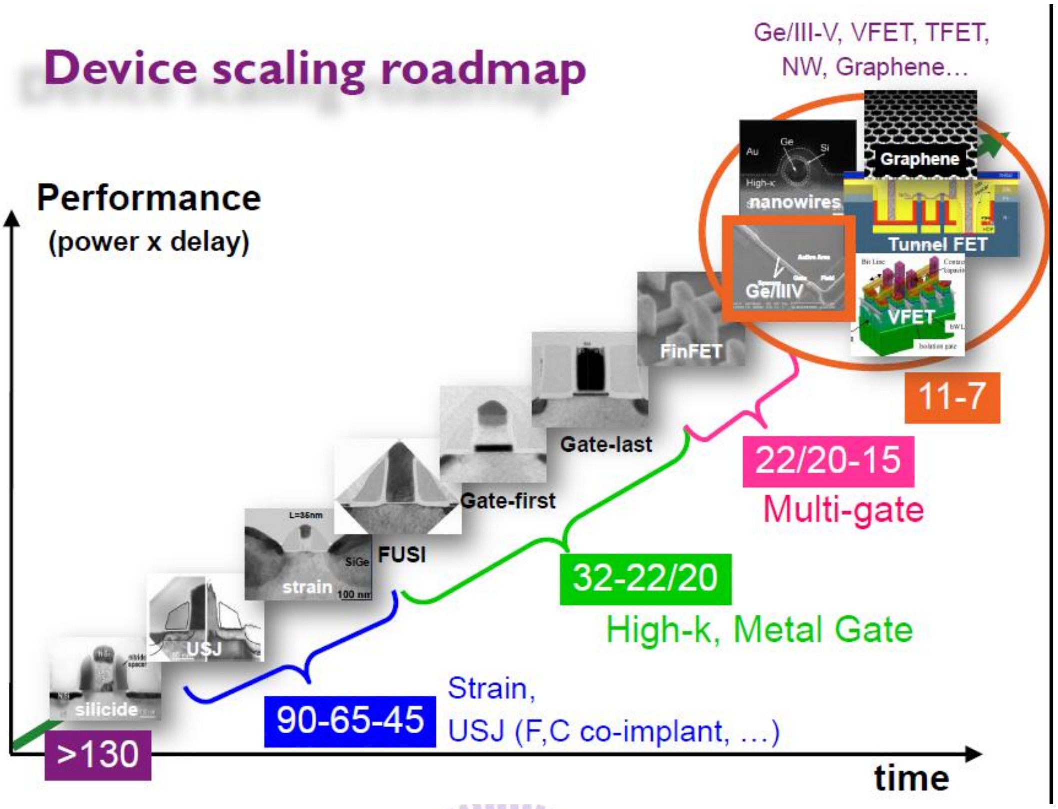

Fig. 1.1 the device scaling roadmap of performance demonstrated by IMEC

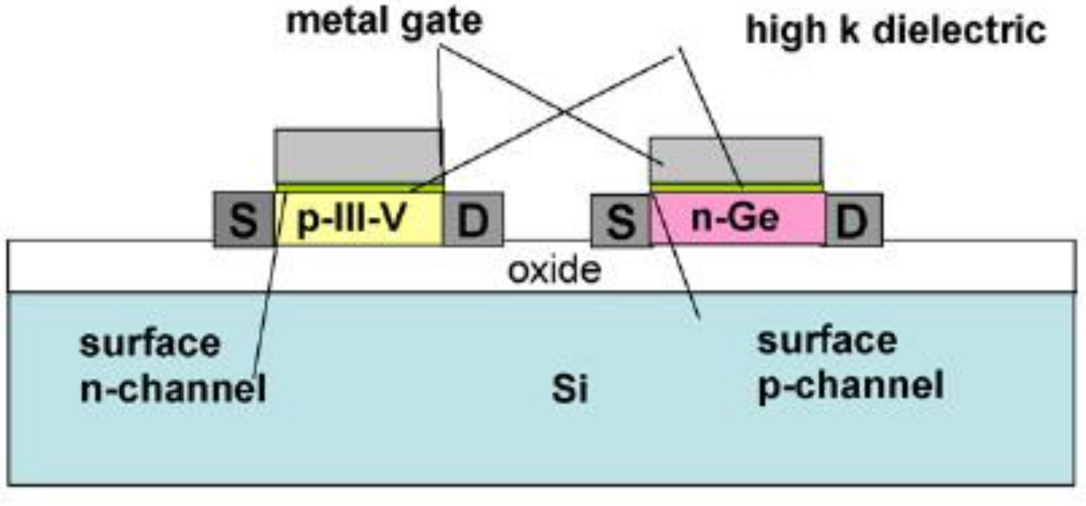

Fig. 1.2 combination of III-V and Ge channel structure by Takagi et al.

Chapter 2

Electrical characteristics of GaAs MOS capacitor for different surface orientation

2.1 Introduction

In order to continue the scaling of silicon-based CMOS and maintain the historic progress in information processing and transmission, innovative device structures and new materials are required. A channel material with high mobility and therefore high injection velocity can increase ON current and reduce delay. Currently, strained-Si is the dominant technology for high performance MOSFETs. However, looking into future high mobility III-V materials can offer several advantages over even very highly strained Si.

The III-V compound semiconductors such as GaAs have high electron mobility, high breakdown field, low power consumption and wide band gap engineering [1, 2, 3]. Recently, GaAs is one of great importance for scientific understanding of III-V interface and GaAs compound semiconductor devices are applied as photodiodes, high electron mobility transistors (HEMT), and other high-frequency devices [4]. But the poor quality of the insulator/ substrate interface deposited such as SiO_2 and Si_3N_4 degraded the performance of MOSFET. Therefore, the literature on the subject that research efforts on achieving low interfacial density of states (D_{it}) covers the past 40 years. The different surface orientation have different density of states (D_{it}), the researchers discovered that the Fermi-level on GaAs(111)A is unpinned compare with GaAs(100) [5-6]. This experimental result demonstrated that Fermi-level pining is not an intrinsic property, but the orientation dependent.

The deposition mechanism of atomic-layer-deposited (ALD) is like chemical vapor deposition (CVD), but is a thin film growth technique that two sequential, self-limiting surface reaction between gas precursor such as tetrakis (ethylmethylamino) hafnium (TEMAH, $Hf[N(C_2H_5)(CH_3)]_4$) and trimethylaluminum (TMA, $Al(CH_3)_3$). ALD is a widely used insulator as gate dielectric due to its good insulated properties, grown films are conformal, pin-hole free, chemically bonding to reduce interfacial trap densities. After all, ALD is one of the CVD, so thermal annealing can further improve the quality of dielectric. Meanwhile, during high temperature process it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides. The impact of thermal annealing on the properties of high-k/III-V interface has been researched [7].

This Electrical characteristics, such capacitance-voltage (C-V) and conductance characteristics, are regularly used in research and development to understand important parameters of MOS capacitor and MOSFETs. For example, capacitance-voltage (C-V) measurements are widely used to quantitatively study the MOS structures. There are several important parameters in evaluating high-k dielectrics on novel channel materials, such as hysteresis, frequency dispersion, and flat band shift and the dielectric/Ⅲ-Ⅴ interface quality. C-V method is powerful to study the properties of the MOS structure, especially to explore the issues with interfacial layers. Otherwise, the C-V and conductance characteristics are the methods of choice to extensively study the interface characteristic because of the inherent sensitivity of the electrical measurements and the ease-of-use of the involved methods [8].

2.2 Experimental process

2.2.1 Surface clean

MOS capacitor sample was prepared on high Si-doped (p-type, $1\sim5\times10^{17}$ cm^{-3} and n-type, $1\sim5\times10^{17}$ cm^{-3}) GaAs with (100) and (111)A crystal orientation substrates. We have three clean steps. At first, the GaAs was rinsed in the diluted HCl (HCl : H_2O = 1 : 3) solution for 3 min for native oxide removal, followed by rinsed in deionized water (D.I. water) for 5 min. Second, the GaAs was rinsed in the diluted NH_4OH (NH_4OH : H_2O = 1 : 10) solution for 10 min for excess elemental arsenic removal, followed by rinsed in D.I. water for 5 min. Third, the GaAs was rinsed in the $(NH_4)_2S$ solution at room temperture for 10 min for ex-situ surface passivation, followed by rinsed in D.I. water for 5 min.

2.2.2 ALD High-k Al_2O_3

The samples mounted in the ALD chamber and gave 20 trimethylaluminum (TMA) precursor pulses for reducing residual native oxide. And then, the Al_2O_3 gate dielectric was deposited by ALD at 250 ℃, followed by post deposition annealing (PDA) in a N_2 ambient. Thermal annealing can further improve the quality of dielectric.

2.2.3 Metal deposition

Thermal evaporated 400 nm Al were patterned as gate electrodes through the lithography. Finally, e-beam evaporated Ti/Pt/Au (50 Å/300 Å/1800 Å) for p-type and Ni/Ge/Au (300 Å/700 Å/1800 Å) for n-type was deposited as backside contact.

The complete process flow was shown in **Fig. 2.1**. The electrical characteristics of Al/Al_2O_3/p-GaAs/TiPtAu and Al/Al_2O_3/ n-GaAs/NiGeAu MOS capacitors were measured using an HP4284 and HP4200, respectively.

2.3 Effective reduction interfacial traps using thermal annealing

ALD is one of the CVD, so thermal annealing can further improve the quality of dielectric. Meanwhile, during high temperature process it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides.

The impacts of initial GaAs post-deposition annealing have been investigated. We used four conditions of PDA to optimize better post annealing condition that efficiently reduced native oxide. Reducing the high density of states on oxide/GaAs, particularly those near the GaAs midgap region, resulting in serious Fermi-level pinning, and thus preventing a proper inversion response required for the inversion-channel GaAs MOSFETs, is an important issue.

In this work, the interfacial traps are qualitative by performing C-V measurement. We designed that post annealing at 500 ℃ for 30s, 600 ℃ for 15s, 600 ℃ for 30s and 700 ℃ for 30s on samples to find the optimal condition to lead to significant reduction of density of states.

Capacitance-Voltage (C-V) characteristics of Al_2O_3/p-GaAs MOS capacitances annealed under various conditions have been summarized in **Fig. 2.2** : (a) annealing at 500 ℃ for 30s, (b) at 600 ℃ for 15s, (c) at 600℃ for 30s, and (d) at 700 ℃ for 30s. All the C-V curves were measured by varies frequency (1kHz ~ 100kHz). According to these figures, we can find that post annealing at 600 ℃ for 15s on sample had better electrical characteristics. Annealing at 500 ℃ for 30s on sample didn’t bend banding to accumulation that value of capacitance was low compared to other samples. Annealing at 600 ℃ for 30s and at 700 ℃ for 30s on samples had obvious stretch out behavior.

In summary, following to these characteristics of Capacitance-Voltage, we can optimize the condition that post annealing at 600 ℃ for 15s on sample had better electrical characteristics. It’s can significantly reduce native oxide, and then efficiently move Fermi-level.

2.4 Capacitance-Voltage characteristics for different surface orientation

2.4.1 A C-V measurement result

First of all, we exhibit the basic properties of the GaAs (100) p-type and n-type MOS capacitor C-V curves with multi-frequency, as shown in **Fig. 2.3 (a) and (b)**, respectively. The quantities of measured capacitances could be used to evaluate the quality of high-k dielectrics and insulator-semiconductor. I defined frequency dispersion ratio≡ΔC . The equation of ΔC is reproduced according to Eq.(2.1)

$$\Delta C \equiv (C\ (@1\text{kHz}) - C\ (@100\text{kHz})\ )/\ C\ (@1\text{kHz}) \qquad (\ 2.1)$$

The p-type GaAs (100) frequency dispersion (3.34%@-3V) are more excellent than n-type GaAs (100) frequency dispersion (9.99%@+3V). We believed that should be a large amount of density of states (Ga-Oxide) existed in upper half interfaces of bandgap. It slows the Fermi-level is pinned at the upper half interface of bandgap when we supply voltage to gate.

After introducing capacitance-voltage curves of GaAs (100), **Fig. 2.4 (a) and (b)** show the MOS capacitor C-V curves of the GaAs (111)A p-type and n-type that is different crystalline surface. The figures compare to **Fig. 2.3 (a) and (b)**, n-GaAs (100) samples can’t reach accumulation even at +3V applied to the gate. This case is because the Fermi-level is pinned for a large amount of interface density of states. The MOS capacitor for n-GaAs (111)A revealed C-V behavior can reach accumulation and had low stretch-out in depletion. The p-type GaAs (111)A frequency dispersion is 3.08% (@-3V) and n-type GaAs (111)A frequency dispersion is 8.28% (@+3V). The values revealed interface of states GaAs(111)A were lower compared to GaAs(100).

2.4.2 Quasi-static C-V measurement result

Interface trapped charge, also known as interface traps or states are attributed to dangling bonds at the semiconductor/insulator interface. GaAs is a large bandgap material. Therefore, there is a large density of very slow interface states inside the GaAs semiconductor bandgap. Quasi-static C-V provides information only on the interface trapped charge density, but not on their capture cross section. The quasi-static C-V for different surface orientation was shown in **Fig. 2.5 (a) and (b)** and calculating the surface potential ψ_s is a function of gate voltage that surface potential was calculated by Berglund method. Berglund is given by Eq.(2.2)

$$\varphi_s = \int_{V_{G1}}^{V_{G2}} \left(1 - {}^{C_{QSCV}}\!/_{C_{ox}} \right) dV_G + \Delta \qquad (2.2)$$

where C_{QSCV} is the quasi-static C-V curve as a function of gate voltage. Integration from $V_{G1} = V_{FB}$ makes $\Delta = 0$, because band bending is zero at flatland. Integration from V_{FB} to accumulation and from V_{FB} to inversion gives the surface potential across the energy bandgap range. **Fig. 2.6** displays the calculated result, surface potential ψ_s versus gate voltage V_G.

According to **Fig. 2.6**, we can obviously know that these experimental results conclusively demonstrate that Fermi-level on the GaAs (111)A surface is indeed unpinned and Fermi-level pinning is not an intrinsic property of GaAs, but is orientation dependent thus related to surface chemistry.

Otherwise, Utilizing high-frequency C-V curve and quasi-static C-V to extract D_{it} as a function of gate voltage by high-low frequency method is described in **Eq. (2.3)**.

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{C_{QS}/C_{ox}}{1 - C_{QS}/C_{ox}} - \frac{C_{hf}/C_{ox}}{1 - C_{hf}/C_{ox}} \right) \qquad (2.3)$$

where the value of C_{ox} is defined on accumulation of quasi-static C-V. After D_{it} extracted by high-low frequency method and x-axis conversion by surface potential ψ_s versus gate voltage V_G, result in D_{it} versus surface potential ψ_s is displayed in **Fig. 2.7 (a) and (b)**.

According to the **Fig. 2.7 (a) and (b)**, we understand the difference between (111)A orientation and (100) orientation. It is the reason that the performance of GaAs on (111)A applied for MOSFETs is quite good compared to (100) orientation.

2.4.3 Charge neutrality level (CNL) measurement

The explanation of the Fermi level pinning phenomenon was first proposed by Bardeen, the pining point was assumed to take place at the charge neutrality level (CNL) of the surface states. Furthermore, extending this idea, Cowley and Sze derived the following well-known equation for a M-S system.

$$\Phi_{Bn0} = c_2(\Phi_m - \chi) + (1 - c_2)\left(\frac{E_g}{q} - \Phi_0\right) \equiv c_2\Phi_m + c_3 \tag{2.4}$$

Where Φ_0 is the location of the CNL measured form the vacuum level given by $\Phi_0 = \chi + (E_c - E_0) = \frac{E_g}{q} - \frac{c_2\chi + c_3}{1 - c_2}$ with known c_2 and c_3 from experiments of varying Φ_m.

First, we found different metals such as Ti, Au, and Pt to extract those schottky barrier heights that we use Capacitance-Voltage method to get Φ_{Bn0}. The experimental results of the metal-n-type GaAs system are shown in **Fig. 2.8**. The slope is c_2 and the intercept is c_3.

Spicer et al. discovered that $q\Phi_0$(CNL) in GaAs is separately 0.5eV and 0.7eV above the valence band maximum (VBM) by photoemission and other experiments. However, According to experiment results, $q\Phi_0 = 0.438$eV for GaAs(100) and $q\Phi_0 = 0.531$eV for GaAs(111)A were not significantly different.

2.5 Admittance Behavior of GaAs MOS capacitor

2.5.1 Conductance Method to Extract D_{it}

The conductance method is one of the most sensitive methods to determine D_{it}, so it is the means of choice to extensively study the interface passivation. Through understanding of the conductance method allow proper extraction of the interface trap across the bandgap. First of all, we have to understand that conductance is extracted since the substrate conductance

G_{sub} only is contributed from interface density and the band diagram of MOS capacitor is showed in **Fig. 2.9**. Where is a gate voltage V_G applied between the metal and the semiconductor, which fixes the value of the surface Fermi level. The C-V measurements consist in applying on top of the static gate bias voltage a small sinusoidal voltage with frequency f and amplitude of 25 mV. This small periodic gate voltage causes the bands and the surface potential in the semiconductor to periodically move up and down, causing the interface traps lying around the value of the surface potential to fill and empty. Only if the traps around the surface potential have a characteristic response time that is of the order of the measurement frequency f can they interact with the measurement ac signal and affect the total impedance of the MOS capacitor. The conductance uses a simplified equivalent circuit of the capacitance and the parallel conductance, as seen in equivalent circuit model of **Fig. 2.10.** It consists of the oxide capacitance C_{ox}, the semiconductor capacitance C_s, and the interface state capacitance C_{it}. The capture-emission of carriers by D_{it} is a losing process, represented by the resistance R_{it}. It is convenient to replace the circuit of **Fig. 2.10(a)** by **Fig. 2.10(b)**, where C_p and G_p are given by

$$C_p = C_s + \frac{C_{it}}{1+(\omega\tau_{it})^2} \tag{2.5}$$

$$\frac{G_p}{\omega} = \frac{q\omega\tau_{it}D_{it}}{1+(\omega\tau_{it})^2} \tag{2.6}$$

where $C_{it} = q^2 D_{it}$, $\omega=2\pi f$, f is measurement frequency, and $\tau_{it} = R_{it}C_{it}$, the characteristic emission frequencies of trapped charge carriers, given by $\tau_{it} = R_{it}C_{it} = \frac{1}{v_{th}\sigma N}e^{\frac{\Delta E}{kT}}$.

Equation (2.5) and Equation (2.6) is valid for an interface trap with single energy level in the bandgap. In reality, interface traps are continuously distributed across the bandgap. If the time constant dispersion and trap energy level distribution across bandgap are taken into account, eq. (2.6) is modified:

$$\frac{G_p}{\omega} = \frac{G_{it}}{\omega} = \frac{qD_{it}}{2\omega\tau_{it}}\ln[1+(\omega\tau_{it})^2] \tag{2.7}$$

When G_p/ω is plotted as a function of f, the maximum appears at $f=\frac{1.98}{2\pi\tau_{it}}$, and at that maximum

$$D_{it} = \frac{2.5}{q}\left(\frac{G_P}{\omega}\right)_{Max} \quad (2.8)$$

G_p/ω plots are repeated at different gate voltages to scan trap energies to obtain an interface state density distribution across the bandgap. By utilizing eq. (2.9), G_p can be determined from the measurement (C_m and G_m) by eliminating the oxide capacitance.

$$\frac{G_P}{\omega} = \frac{G_{it}}{\omega} = \frac{\omega C_{ox}{}^2 G_m}{G_m{}^2+\omega^2(C_{ox}-C_m)^2}$$

(2.9)

The flows of conductance method to extract D_{it} in **Fig. 2.11**.

2.5.2 Conductance method application of GaAs MOS capacitor

It is worthy to note that according to the emission time constant ($\tau = \frac{1}{V_{th}\sigma N}e^{\frac{\Delta E}{kT}}$), the behavior of interface trap time constant as a function of temperature determines the part of interface traps in the bandgap observable in the MOS admittance characteristic. That is, traps located nearer to midgap become observable for higher temperatures while traps more located toward the band edges become observable for lower temperature. We assumed the capture cross section $\sigma = 1\times10^{-15}$ cm^2 and plotted the characteristic emission frequencies of trapped charge carriers in GaAs at the different temperature as a function of the position of the trap in the energy bandgap.For high band gap GaAs, midgap traps are not able to be observed at room temperature; if increasing the temperature, the observable energy windows shift toward the midgap as shown in **Fig 2.12**, where the effective density of states of the conduction (N_c) and the valence (N_v) bands, electron and hole thermal velocity, change in GaAs bandgap with temperature are all taken into account. **Fig 2.13** and **Fig. 2.14** illustrates the G_p/ω versus f plots of MOS capacitor for different orientation and measurement is performed at room temperature. G_p/ω curves are shown at the gate voltages Fermi level is only portions of the bandgap where interface states are able to capture and emission with the small signal AC bias. The peak value of each G_p/ω curve corresponds to the interface state density and thus D_{it} as a function of gate voltage can be plotted. Then, the equation $\Delta E = kT\ln(\frac{V_{th}\sigma N}{\pi f})$ combined with the value of maximum value of G_p/ω transforms the D_{it} (V_G) into D_{it} (E) plot.

2.5.3 High Temperature Measurement of GaAs MOS capacitor

In order to obtain the full distribution of D_{it} in the bandgap, conductance method is applied at high temperatures. The multi frequency CV characteristics measured at 423K are shown in **Fig. 2.15 and Fig.2.16** for different orientation. **Fig. 2.17 and Fig.2.18** G_p/ω curves are shown at the gate voltages Fermi level is near the midgap where interface states are able to capture and emission with the small signal AC bias. The peak value of each G_p/ω curve corresponds to the interface state density and thus D_{it} as a function of gate voltage can be plotted. We interpret the largest G_p/ω value to represent D_{it} at the specific position in bandgap. the D_{it} profile of each sample for GaAs(100) is demonstrated in **Fig 2.19** compared to GaAs(111)A.

According to these figures, we saw that D_{it} was not high for middle of the bandgap obviously for n-type GaAs(111)A and p-type GaAs(111)A compared to the GaAs orientation of (100). Once again, the electrical characteristics proved that the Fermi level pinning is not an intrinsic property of GaAs.

2.6 Electrical characteristics of GaAs MOSFET

2.6.1 Introduction

In general, the condition of suitable gate dielectric on MOSFET will require: (a) the oxides do not react with the substrates. (b) The band offset of the oxide on the semiconductor is required to have over 1eV to inhibit leakage.

The high mobility materials are applied in MOSFET to obtain higher device performance than Silicon. In particular, Ge and III-V based are promising material to use in place of conventional Si MOSFETs. Recently, high-*k*/Ge p-MOSFET characteristics have been reported have high performance characteristic recently [9-10]. However, Ge n-MOSFETs remains have challenging because of the resulting from low electron mobility and the asymmetrical distribution of interface states that result in the Fermi level (E_F) pinning. In addition, III-V materials have higher electron mobility than Ge, we showed some III-V materials' advantages in **Fig. 2.20**. In present, the several promising MESFET and n-MOSFET device characteristics based on III-V channels have been continually demonstrated [11-16], and their performances even exceeded the strained-Si transistors at the nano-scale devices [17]. In order to obtain the superior III-V device performance, it is essential to achieve the unpinned oxide/substrate interface.

In this chapter, we fabricated the circular transmission line method (CTLM) for analyzing contact and sheet resistivity. And then, we fabricated the junction of different conditions. After optimizing the conditions of CTLM and junction, we also succeeded to fabricate the enhancement-mode (E-mode) GaAs n-MOSFET with ALD- Al_2O_3 gate dielectrics on the GaAs substrate.

2.6.2 Source/Drain Ohmic Contact on GaAs

1. Introduction

The resistance is an importance factor for metal-oxide-semiconductor field effect transistors (MOSFET) device performance. The contact resistance is the most importance among series resistances.

How to decide it is a good contact? The ohmic contact is a right method to determine. Ohmic contacts have a linear current-voltage characteristic. The contacts have to be able to supply the necessary device current, and the voltage drop across the contact should be small compared to the voltage drops across the active regions. We fabricated the circular transmission line method (CTLM) for analyzing contact and sheet resistivity. The problem of

W≠L of TLM can be avoided with circular test structure [18], including of a conducting circular inner region of radius r, a gap of width d, and a conducting circular outer region R in **Fig. 2.21**. The total resistance between the internal and the external contacts is

$$R_T = \frac{\rho_s}{2\pi}\left[\frac{L_T}{r}\frac{I_0\left(L/L_T\right)}{I_1\left(L/L_T\right)} + \frac{L_T}{R}\frac{K_0\left(L/L_T\right)}{K_1\left(L/L_T\right)} + \ln\left(1+\frac{d}{L}\right)\right] \ , \ L_T=\sqrt{\frac{\rho_c}{\rho_s}} \tag{2.10}$$

where I and K are the Bessel functions of the first order. Due to L ≫ $4L_T$, the Bessel function ratios I_0/I_1 and K_0/K_1 tend to unity and R_T simplifies to

$$R_T = \frac{\rho_s}{2\pi}\left[\frac{L_T}{r} + \frac{L_T}{R} + \ln\left(1+\frac{d}{L}\right)\right] \tag{2.11}$$

In the circular transmission line test structure, due to r ≫ d, the equation becomes

$$R_T = \frac{\rho_s}{2\pi r}\left[d + 2L_T\right]C \quad \text{, where } C=\frac{r}{d}\ln\left(1+\frac{d}{r}\right) \tag{2.12}$$

For d / r ≪ 1, the above equation simplifies to

$$R_T = \frac{\rho_s}{2\pi r}\left[d + 2L_T\right] \ , L_T=\sqrt{\frac{\rho_c}{\rho_s}} \tag{2.13}$$

According to above equation, we firstly measured the relationship of R_T and d, and find line to fit it. The ρ_s and L_T can be extracted. Finally, the value of ρ_c utilizes L_T to obtain in **Fig. 2.22**.

2. Experimental Procedures

The samples, firstly, were implanted the Silicon doses 1 × 10^{14} cm^{-2} at 50 keV After deposit SiO_2 capping layer, activation was using RTA at 750℃,850℃ and 950℃ for 15 s in N_2 ambient. Then, we used Acetone to remove metal-organic residues and the metal of Ni/Ge/Au (30 nm/70 nm/180 nm) was deposited by using E-gun system and lift-off process, the CTLM structure in Fig. showed. Alloy metal was formed by RTA at 400 ℃ for 30s.

3. Results and Discussions

First, due to activation was using RTA at 750℃showed current characteristics couldn’t limiting, so we remove the condition of 750℃. We designed the conditions of different activity temperature and implant energy on SI-(111)A substrate in shown **Fig. 2.23 (a), (b), (c), (d)** and **Table 1**.

In these result, from the point of implant energy, we discovered that the sheet resistivity at 30keV&80keV is lower than 50keV implant energy. However, the contact resistivity is just contrary. In addition, from the point of temperature, we found that the sheet resistivity at 850℃ is lower than 950℃, and the contact resistivity is just contrary. We can conclude the optimized condition for GaAs ohmic contact that was implanted at 50keV and the activity temperature at 850℃. **Fig. 2.24** show the optimized condition on SI-(100) GaAs substrate.

Next, we only designed the conditions of different implant energy for 850℃ in shown **Fig.2.25**, **Fig. 2.26** and **Table2**. It is because that some of condition for 950℃ showed current characteristics couldn't limiting(sheet resistivity is large). Similarly, the optimized condition for GaAs ohmic contact was implanted at 50keV and the activity temperature at 850℃.

2.6.3 Source/Drain Junction on GaAs

1. Introduction

One of the most important properties is that their conductivity can be controlled by adding dopants. The conduction mechanisms for a metal on n-type semiconductor are described. For the low-doped semiconductor, the current mechanism is thermionic emission (TE). For the high-doped N^+, the width was sufficiently narrow for tunneling directly, known as field emission (FE). In the intermediate-doped range, thermionic-field emission (TFE) dominates. Although many exciting results on GaAs MOS capacitors and enhance mode GaAs MOSFETs without source/drain implantation have been reported [19-21], and also the cost is higher and the throughput is lower. GaAs material have a challenge in fabricating is dopant's low activation efficiency. It is because common source such as Si or Ge can replace either Ga atom or As atom to be donor or acceptor, respectively [22]. Hence, the net donor concentration would be the number of Si atoms occupying the Ga minus the number of Si atoms occupying the As. In order to increase the number of Si atoms occupying the Ga and increase the activation efficiency, we design the conditions of different activity temperature including 750℃, 850℃ and 950℃.

2. Experimental Procedures

In GaAs Junction fabrication, we used PECVD to deposit SiO_2 420 nm as isolation layer, and then, we defined the Si implantation regions by photolithography, which were implanted the doses 1×10^{14} cm^{-2} at 50keV . After deposit SiO_2 encapsulation layer, S/D activation was using RTA at different temperatures in N_2 ambient. the metal of Ni/Ge/Au (30 nm/70 nm/180 nm) was deposited at the S/D region by using E-gun system and lift-off process. Alloy metal was formed by RTA at 400 ℃ for 30s and 60s.

3. Results and Discussions

The GaAs P(111) N^+/P junction current-voltage characteristic with Si implantation are shown in **Table 3** and **Fig. 2.27** measured by 4200. The alloy metal annealing time by RTA is 30s and 60s was also examined. From the experiments, we can conclude the optimized condition for GaAs Ohmic contact that was annealed at 400℃ for 30s. In addition, we found that the ratio of forward to reverse current at this N+ /P junction is achieved to be as high as $I_{\text{forward}} / I_{\text{reverse}}=10^7$, indicating an activation temperature of 950 ℃ is enough to activate Si in GaAs and a high quality N+ /P junction. The reason is because that the defect was repaired, the junction reverse current could be reduced.

2.6.4 MOSFET on GaAs with atomic-layer-deposited Al_2O_3 as gate dielectrics

GaAs is one of materials for high performance due to its high electron mobility, high saturation velocity, and wide bandgap. GaAs MOSFET can be applied on a sensitive test. In this section, we fabricate GaAs MOSFETs for different orientation include (111)A and (100).

In GaAs MOSFET fabrication, we used ALD and PECVD to deposit Al_2O_3 10 nm and SiO_2 420 nm as isolation layer, respectively, and then, defined the Si and P implantation regions, which were implanted the doses 1 × 10^{14} cm^{-2} at 50 keV and 1 × 10^{15} cm^{-2} at 60 keV, respectively. S/D activation was using RTA at 850℃ for 10 s in N_2 ambient. And then the sample was cleaned by diluted HCl, diluted NH_4OH, $(NH_4)_2S$ solution. After surface cleaning, the sample was loading into the ALD chamber, followed by surface pretreatment with TMA pulse 20 cycles. Next, the Al_2O_3 gate dielectric was deposited by ALD at 250 ℃, followed by PDA at 600 °C for 15 s in an N_2 ambient. Thermal coatered Al about 4000 Å were patterned as T-gate electrodes through the lithography. After excavating the S/D contact holes, the tri-layer of Ni/Ge/Au (30 nm/70 nm/180 nm) was deposited at the S/D region by using E-beam system and lift-off process, followed by PDA at 400°C for 60 s in an N_2 ambient to form Ohmic contact. The fully process flow of GaAs MOSFET was shown in **Fig. 2.28**.

Fig. 2.29 illustrates the I_D-V_G transfer characteristic of 4μm gate length for E-mode ALD-Al_2O_3/GaAs (111)A nMOSFET with TMA 20-cycles-pulse pretreatment and the ratio I_{on} (I_D at $V_G = 3V$, $V_D = 2V$)/I_{off} (I_D at $V_G = 0V$, $V_D = 2V$) is 2.8×10^5. For device with the gate length/width of 4/100 μm, the value of V_{th} was 0.895 V which is extracted by linear extrapolation.

In **Fig. 2.30**, the well saturation and pinch-off characteristics were presented in I_D-V_D curves with the gate drive V_G ranging from 0 to 3 V in steps of 0.5 V display and the maximum drain current was 46 μA/ μm measured at $V_G = 3$ V, $V_D = 3$ V.

The gate-to-channel capacitance and inversion charge density by **Eq. (4.3)**

$$Q_{inv} = \int_{-\infty}^{V_G} C_{GC}(V_G)dV_G \qquad (2.14)$$

and solving for the effective mobility μ_{eff} gives

$$\mu_{eff} = \frac{g_d L}{W Q_{inv}} \qquad (2.15)$$

where the drain conductance g_d is defined as

$$g_d = \frac{\partial I_D}{\partial V_D}\Big|_{V_G=\text{constant}} \qquad (2.16)$$

Fig. 2.31 (a) depicts the effective mobility is obtained.

The series resistance not only degrades the MOSFET current-voltage behavior, but also affects the mobility, since the effective mobility depends on drain conductance g_d. I_D depends on series resistance R_{SD}, so μ_{eff} also depends on R_{SD}. The drain conductance becomes

$$g_d(R_{SD}) = \frac{g_{d0}}{1+g_{d0}R_{SD}} |_{V_G=\text{constant}} \qquad (2.17)$$

Where g_{d0} is the drain conductance for R_{SD}=0.

An early method is total resistance method that due to Terada and Muta, and Chern et al. in 1980, with $R_m = V_{DS}/I_D$

$$R_m = R_{ch} + R_{SD} = \frac{L-\Delta L}{W_{eff}\mu_{eff}C_{ox}(V_{GS}-V_T)} + R_{SD} \qquad (2.18)$$

where R_{ch} is the channel resistance, the intrinsic resistance of the MOSFET.

Equation (2.18) gives $R_m = R_{SD}$ for $L=\Delta L$.Therefore, measuring a set of device with same channel width and different channel length (Fix V_{DS} at 0.05V and V_{GS}-V_{th} is set in the range from 0V to V_{DD}), and then a plot of R_m versus L for devices with differing L and for varying gate voltages in Fig. . The intersection point represent R_{SD} and ΔL.

Since S/D parasitic resistance can result in a significant reduction in the drain voltage falling across the channel and influence the drive current as well as the effective mobility extraction, the effective inversion mobility with R_{SD} eliminated is depicted in **Fig. 2.31 (b)**, utilizing eq. (4.1).

$$\mu_{eff} = \frac{L_{eff}}{W_{eff}Q_{inv}\left(\frac{1}{g_d}-R_{SD}\right)} \qquad (2.19)$$

2.7 Summary

According to the electrical characteristics, we discovered the Fermi-level on GaAs(111)A is unpinned compare with GaAs(100). GaAs(111)A had the best surface band bending and lower value of D_{it} in the middle of bandgap. In order to confirm the electrical characteristics, we used the high-low method and the conductance method to extract distributions of D_{it} for different orientation. At the first, we used the QSCV and high-frequency CV to extract band bending and Dit distribution. And then, we measured the multi-voltate of C_m-f and G_m-f which are measured at the different temperature conditions. Next, we calculated the $G_p/\omega$and extracted D_{it} by conductance method, we can accurately determined D_{it} distribution across the bandgap. According to the result, GaAs(111)A had the best surface band bending and lower value of D_{it} in the middle of bandgap, we assumed that the improvement resulted from the different structure of surface on orientation. The Fermi level pinning is not an intrinsic property of GaAs.

Finally, we optimize conditions of sheet resistivity, contact resistivity, and Ohmic RTA time. And then, we used these conditions to fabricate metal-oxide-semiconductor field effect transistors with the (111)A surface orientation successfully and measured electrical characteristics.

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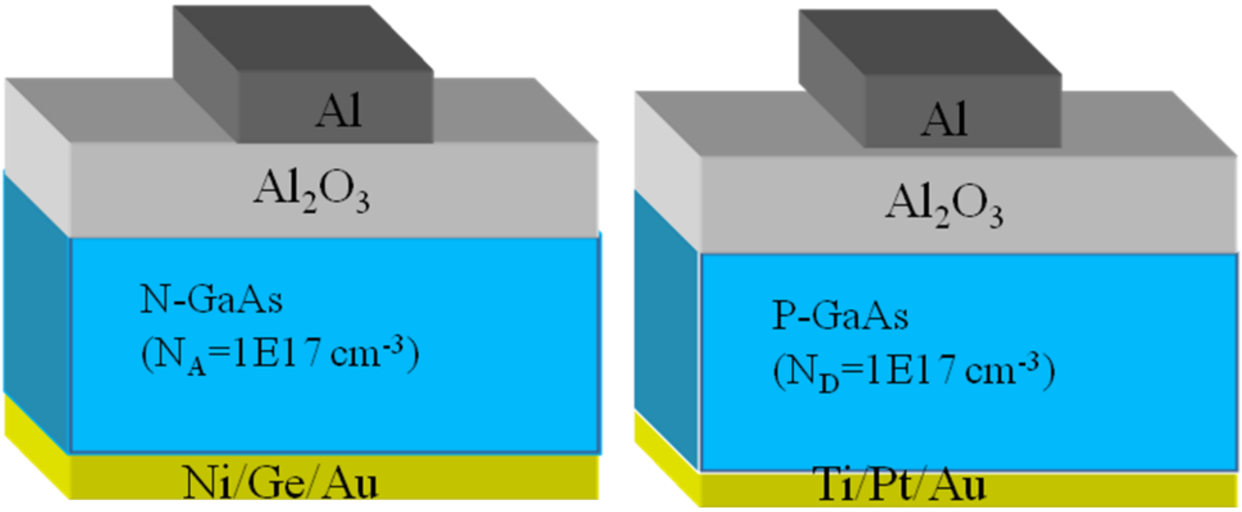


1)Clean: HCl(aq.)+NH_4OH(aq.)+$(NH_4)_2S$(aq.)
2)Si passivation: annealing 600°C,1min +purge SiH_4 420°C,90s
3)Al_2O_3 film: ALD at 250°C, 150 cycles(preTMA20cycle)
4) Post-deposition annealing (PDA):
600°C, 15s in N_2 ambient (W&W/O)
5)Al metal: 450 nm
6)Ni/Ge/Au metal(for N-type) ; Ti/Pt/Au metal(for P-type)
7)Alloy: 400°C,30s in N_2 ambient

Fig. 2.1 The structure and process flow of MOS capacitor.

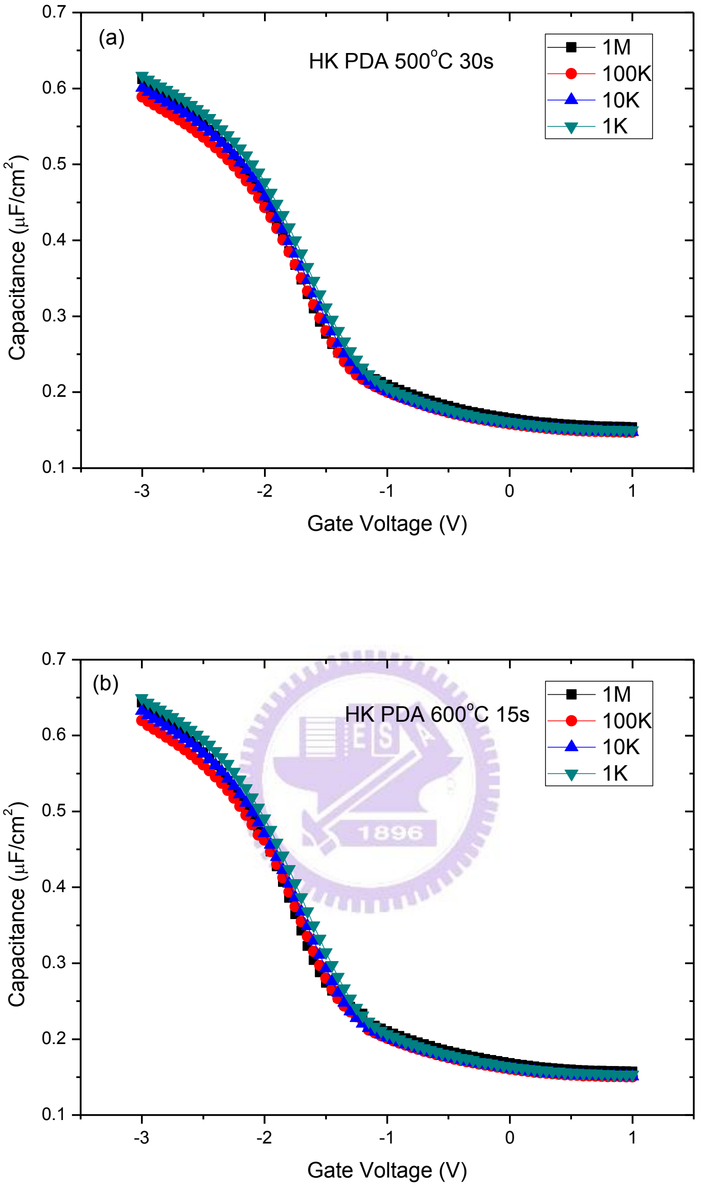


Fig. 2.2 C-V curve of MOS capacitor (a) 500 ℃, 30s (b)600 ℃, 15s

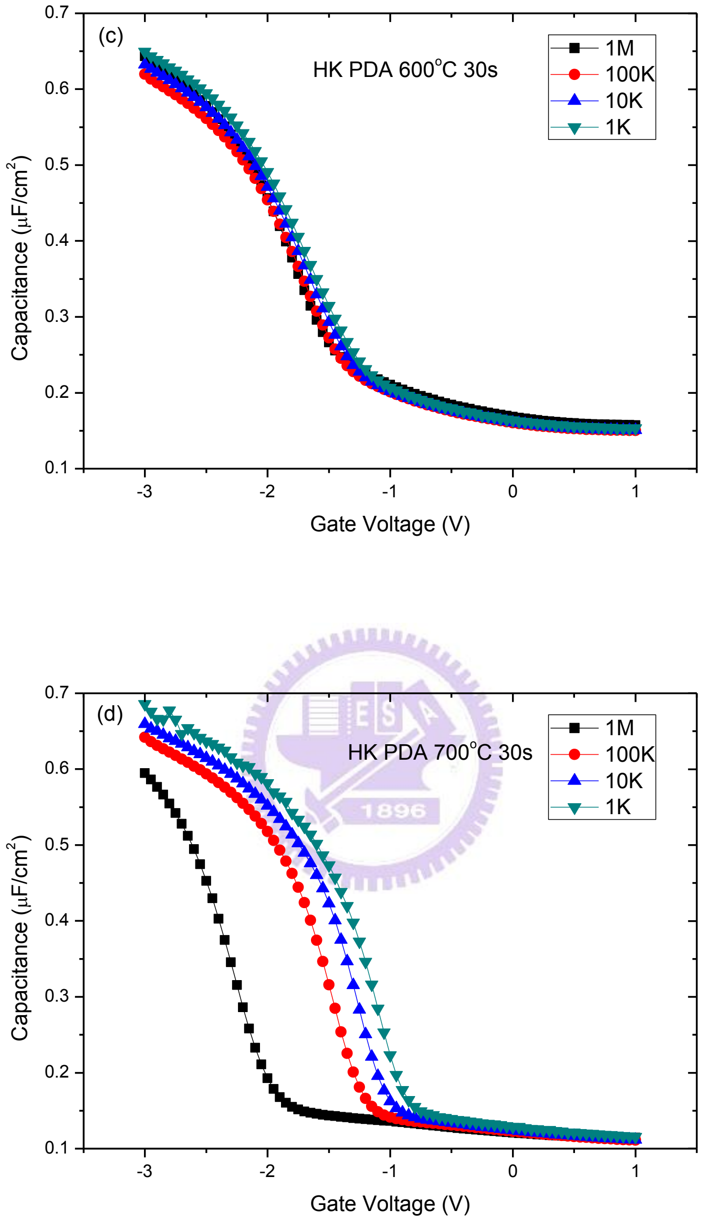


Fig. 2.2 C-V curve of MOS GaAs capacitor (c) 600 ℃, 30s (d)700 ℃, 30s

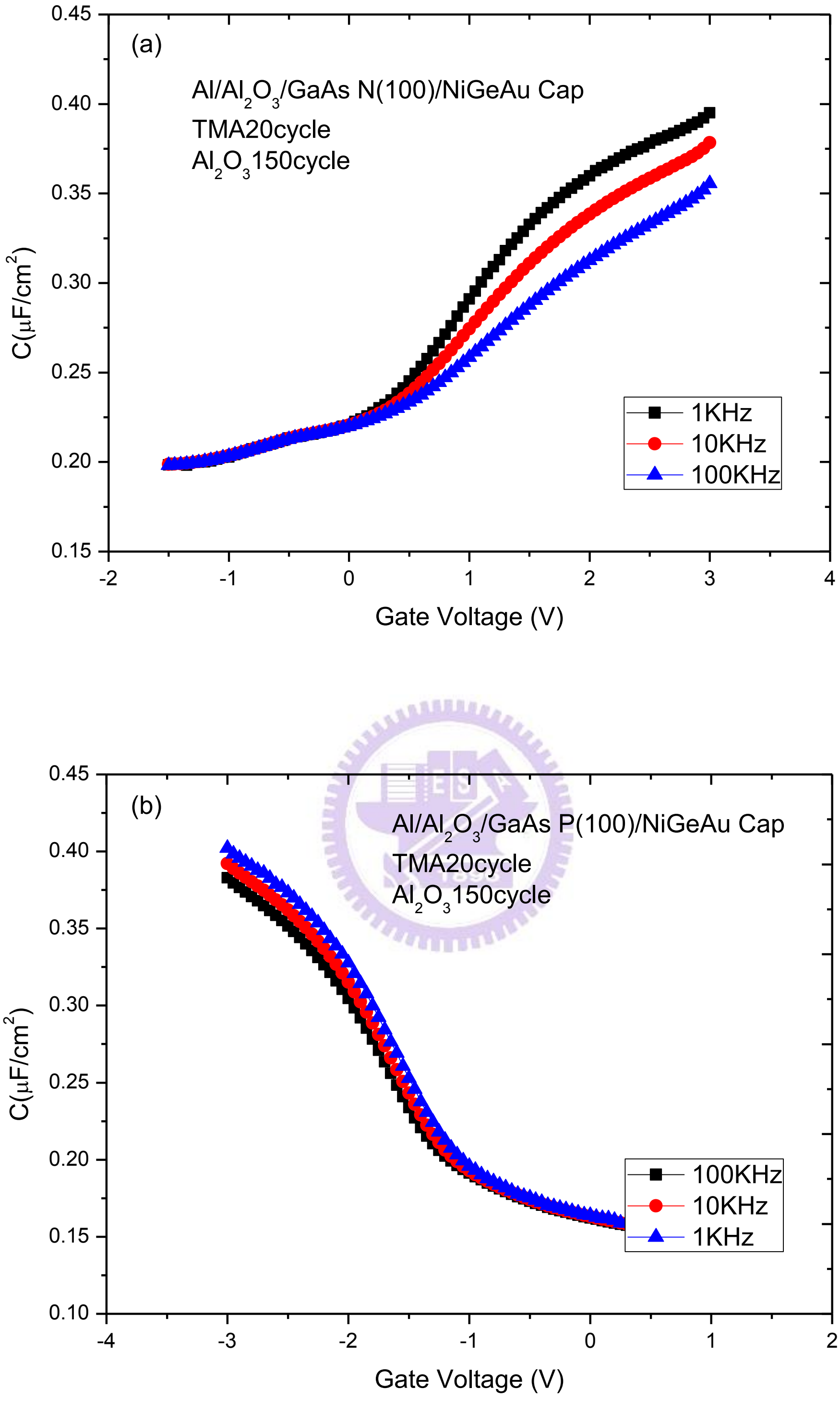


Fig. 2.3 C-V curve of MOS GaAs(100) capacitor (a) n-type (b) p-type

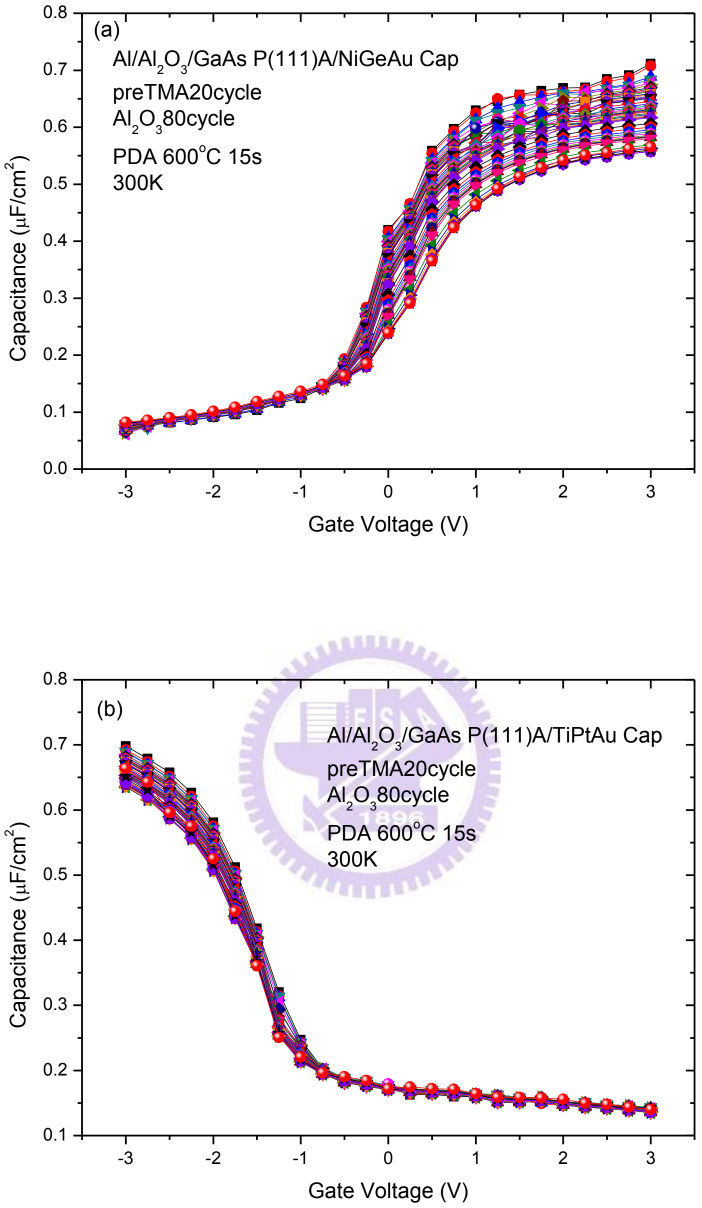


Fig. 2.4 C-V curve of MOS GaAs(111)A capacitor (a) n-type (b) p-type

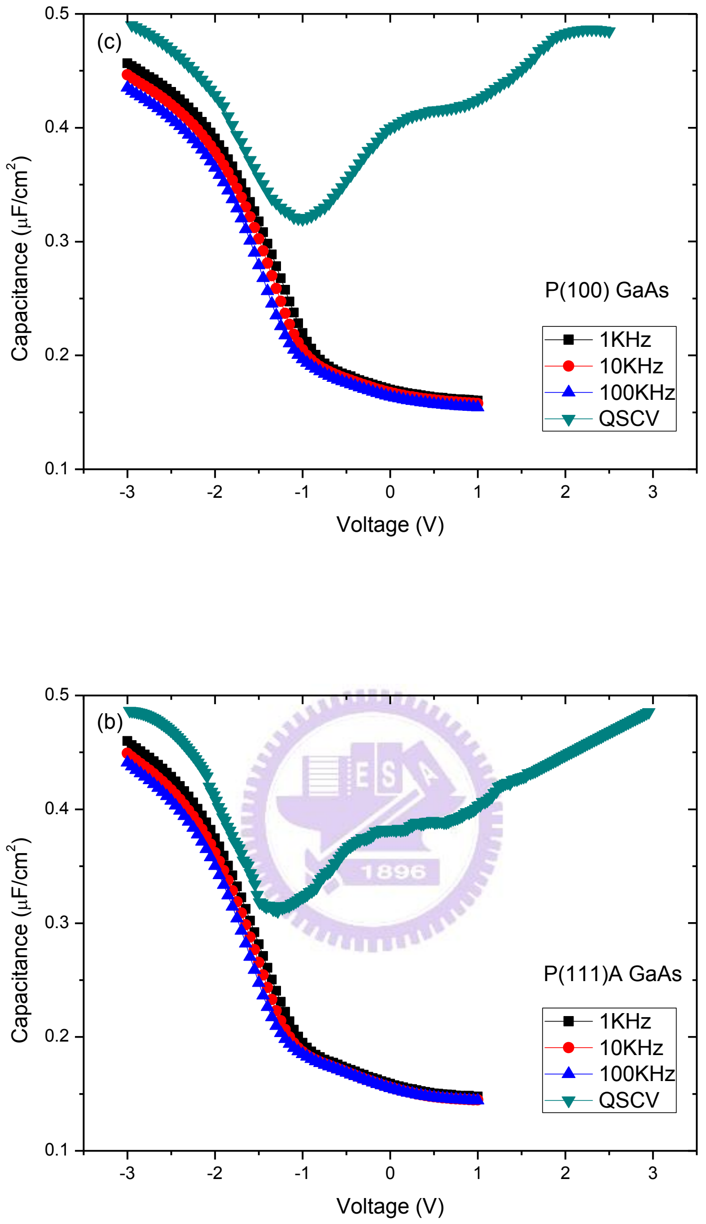


Fig. 2.5 QSC-V curve of MOS GaAs capacitor (a) (100) (b) (111)A

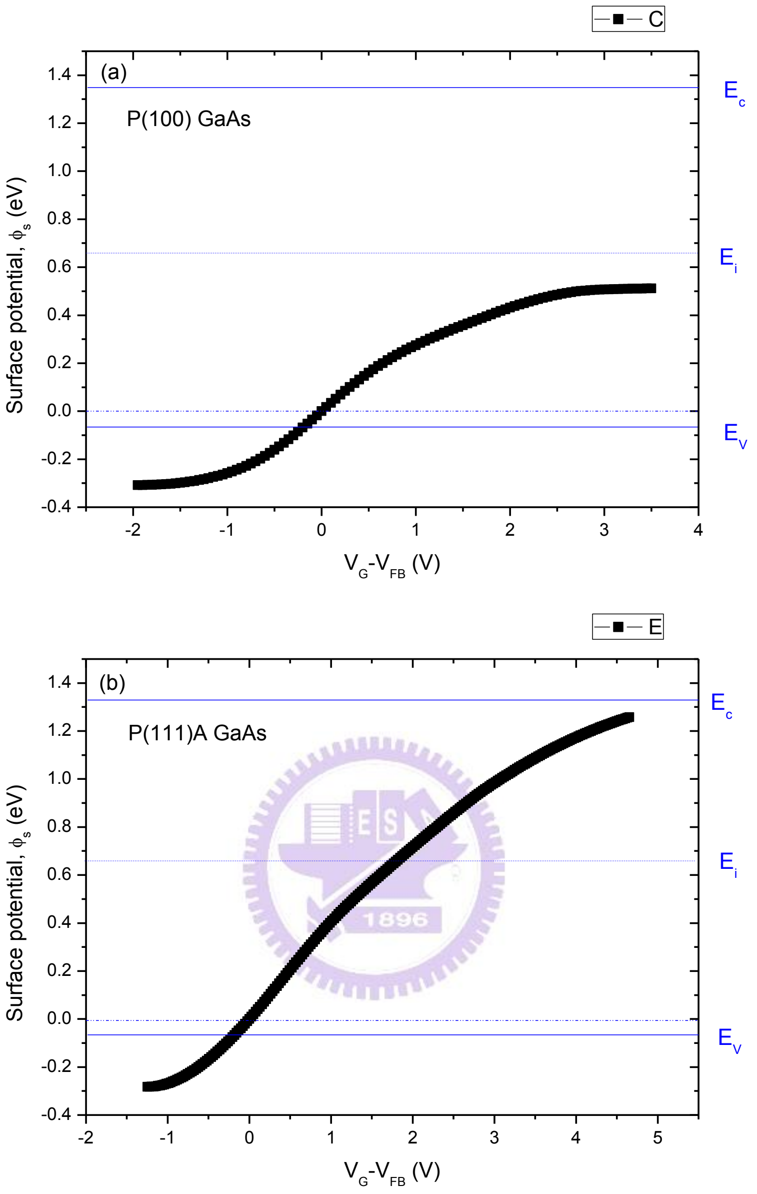


Fig. 2.6 surface potentialψ_s versus gate voltage V_G (a) (100) (b) (111)A

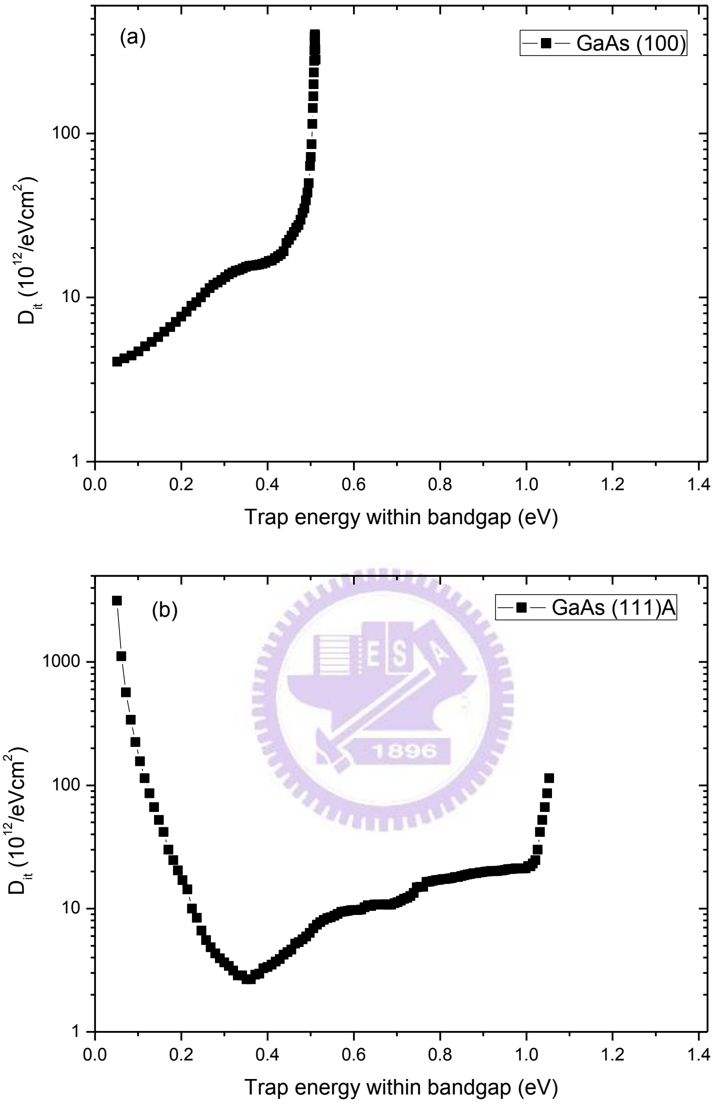


Fig. 2.7 Comparsion of D_{it} distribution of surface orientation effect (a) (100) (b) (111)A

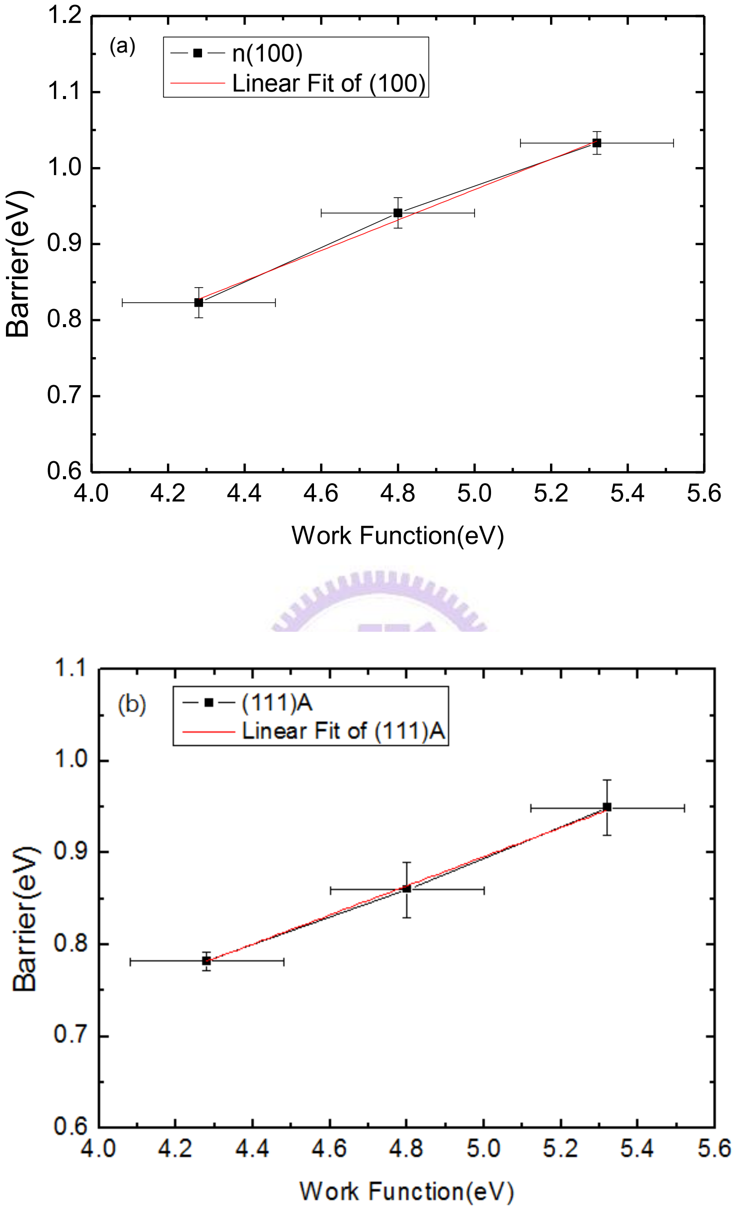


Fig. 2.8 Comparison of Barrier verses Work Function (a) (100) (b) (111)A

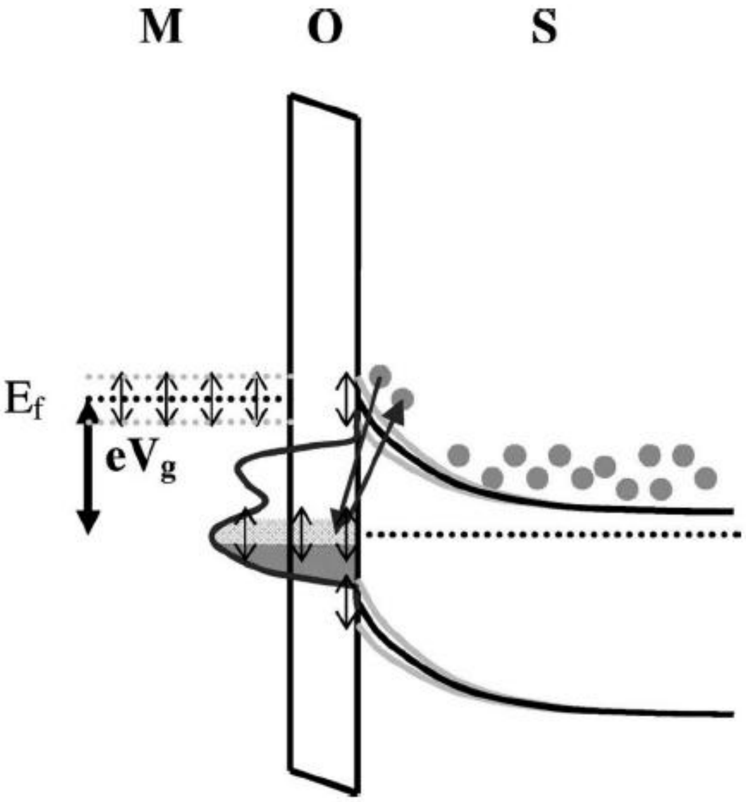


Fig. 2.9 The band diagram of a typical MOS structure is illustrated, with surface potential in the semiconductor to periodically move up and down because of a small sinusoidal voltage on top of the static gate bias.

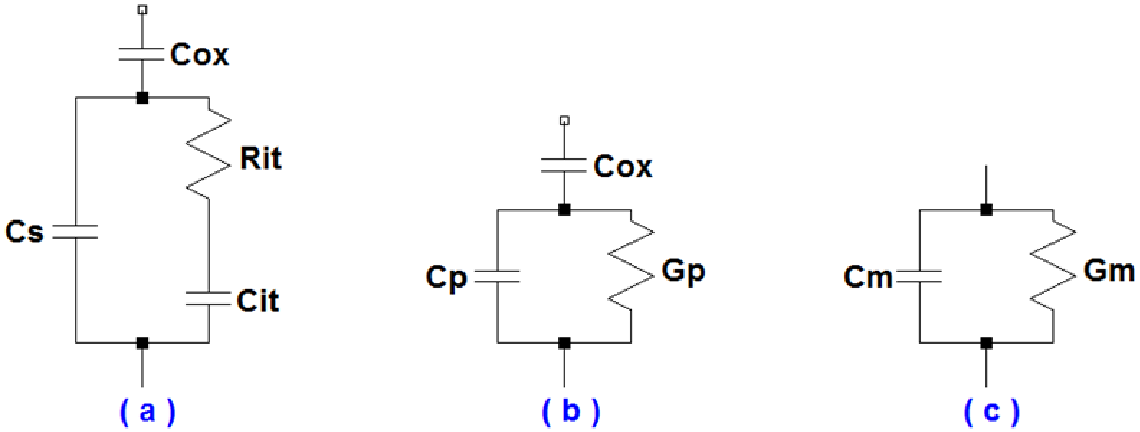


Fig. 2.10 Equivalent circuits for conductance measurements; (a) MOS capacitor, (b) simplified circuit, (c) measured circuit.

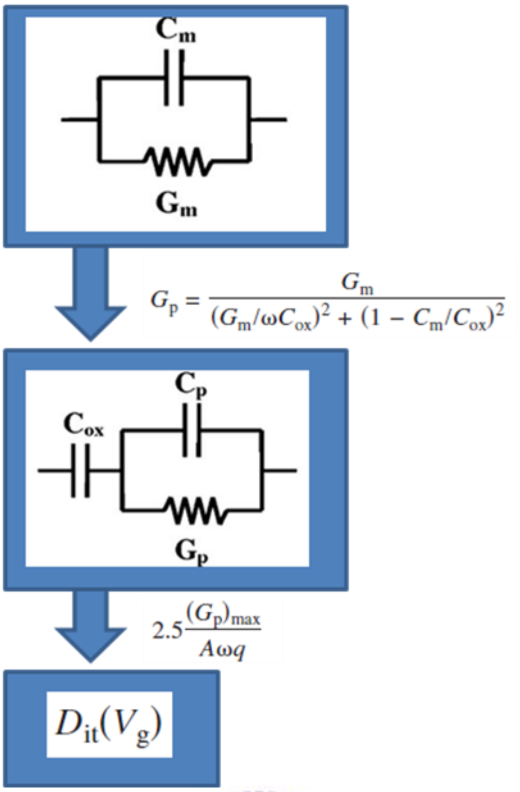


Fig. 2.11 The flows of Conductance Method to Extract D_{it}

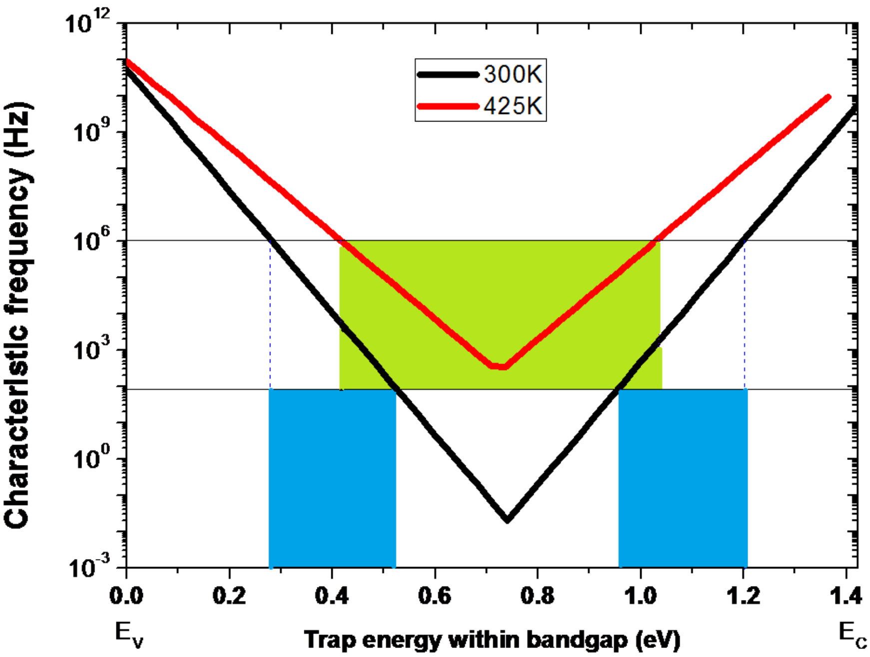
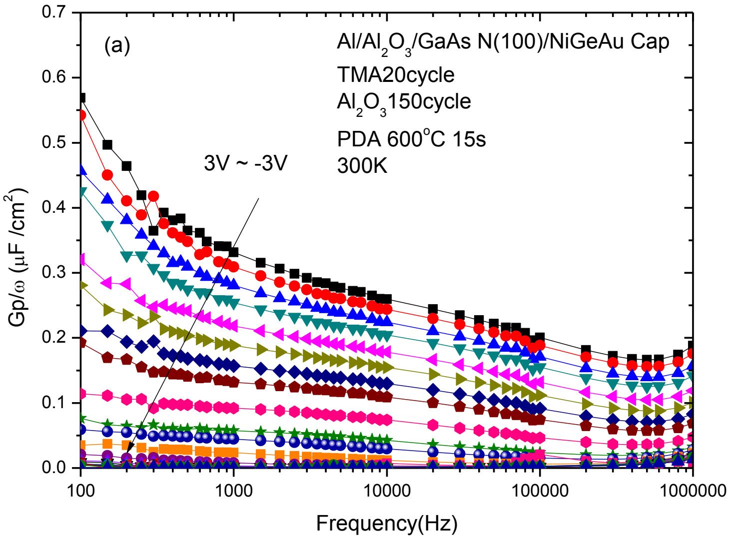


Fig. 2.12 Characteristic emission frequencies of trapped charge carriers in GaAs at the different temperature



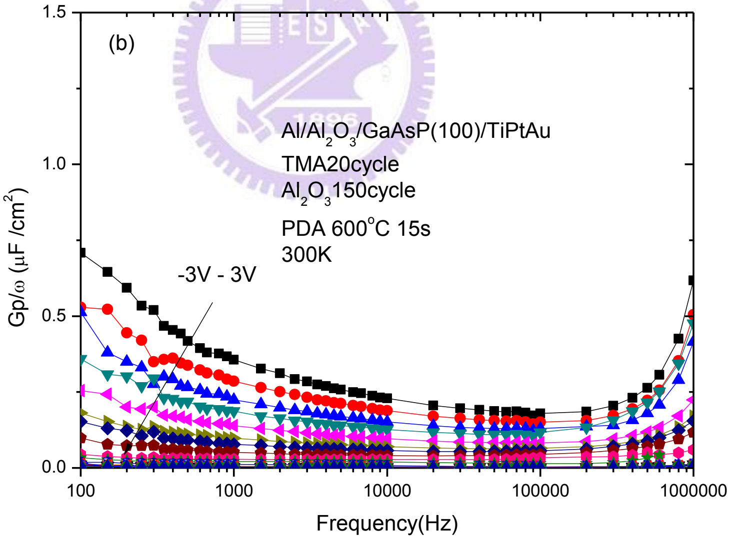


Fig. 2.13 G_p/ω as a function of frequency at 25℃ (a) N-type GaAs(100) (b) P-type GaAs(100)

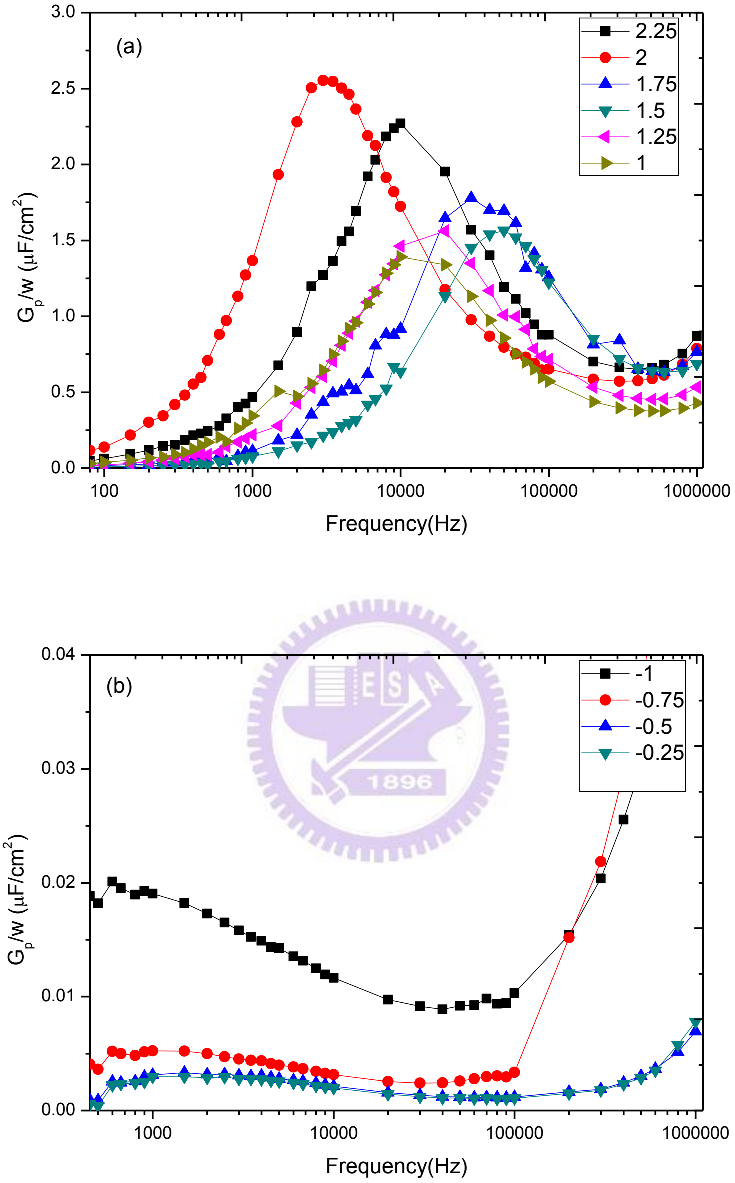
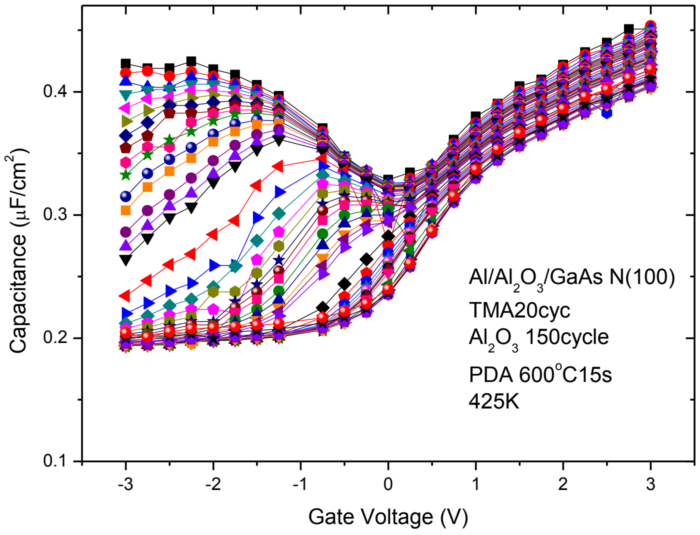


Fig. 2.14 G_p/ω as a function of frequency at 25℃ (a) N-type GaAs(111A) (b) P-type GaAs(111)A



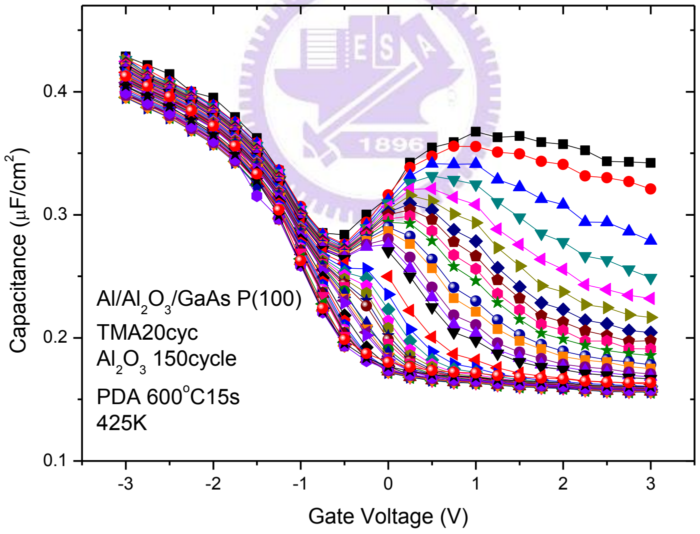


Fig. 2.15 Multi-frequency C-V curve 425K (a) N-type GaAs(100) (b) P-type GaAs(100)

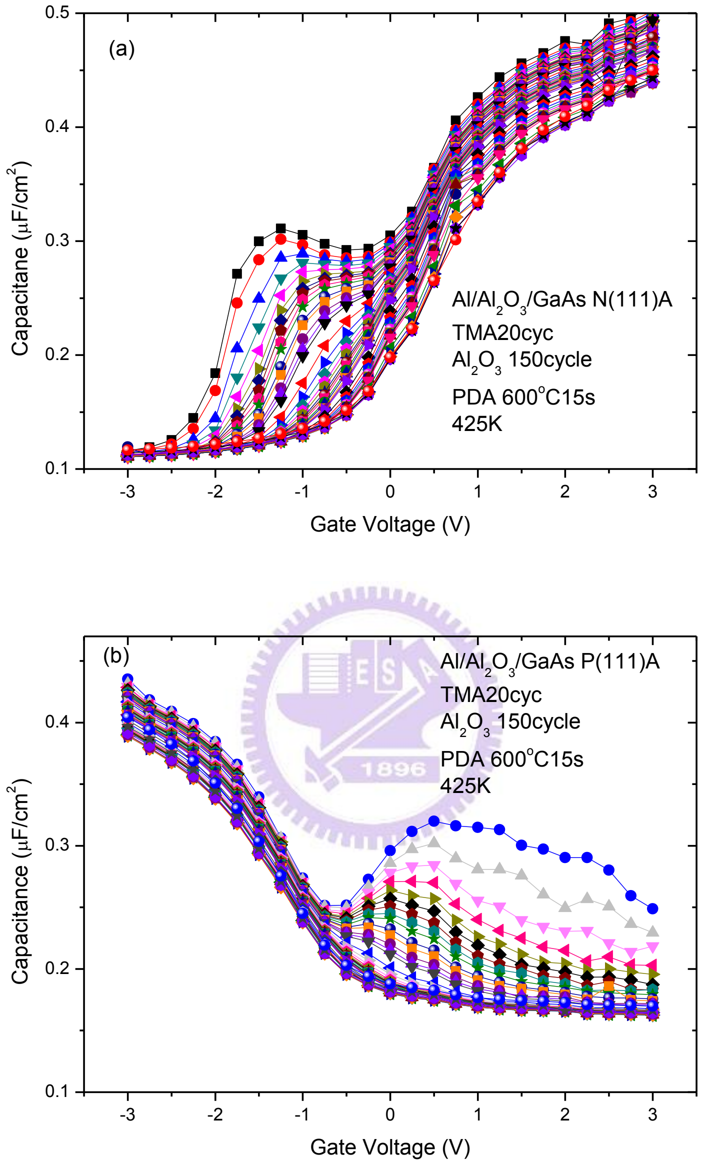


Fig. 2.16 Multi-frequency C-V curve 425K (a) N-type GaAs(111)A (b) P-type GaAs(111)A

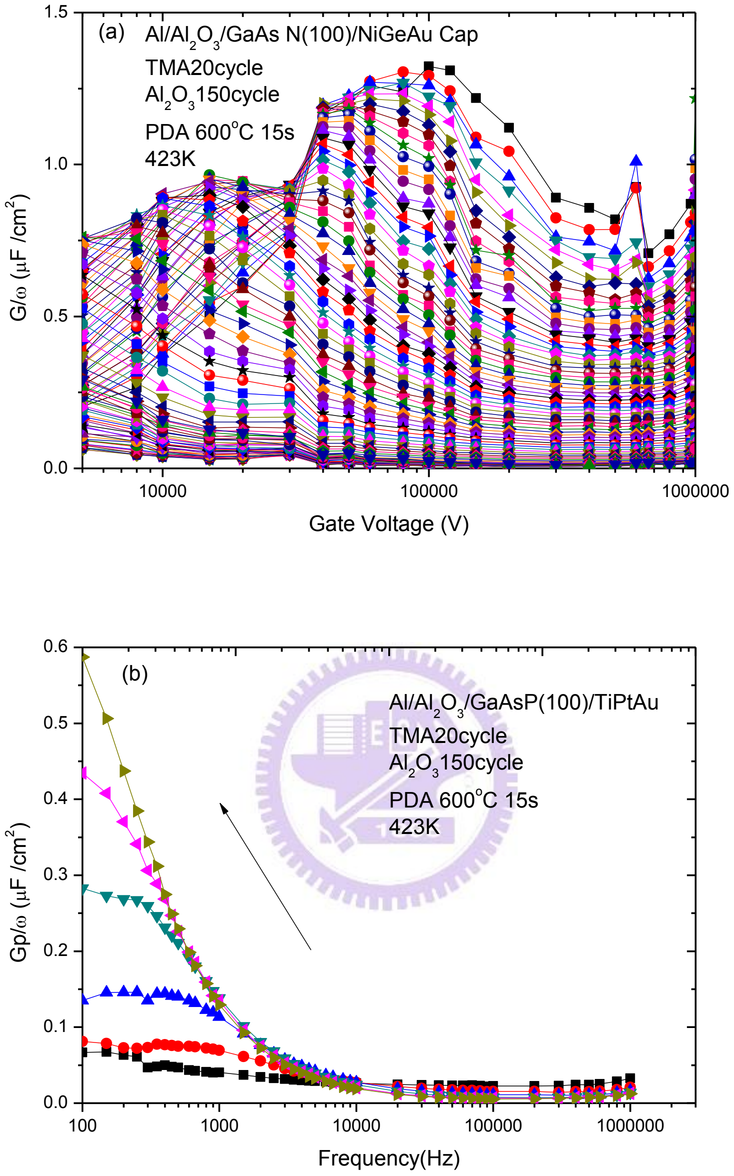


Fig. 2.17 G_p/ω as a function of frequency at 150℃ (a) N-type GaAs(100) (b) P-type GaAs(100)

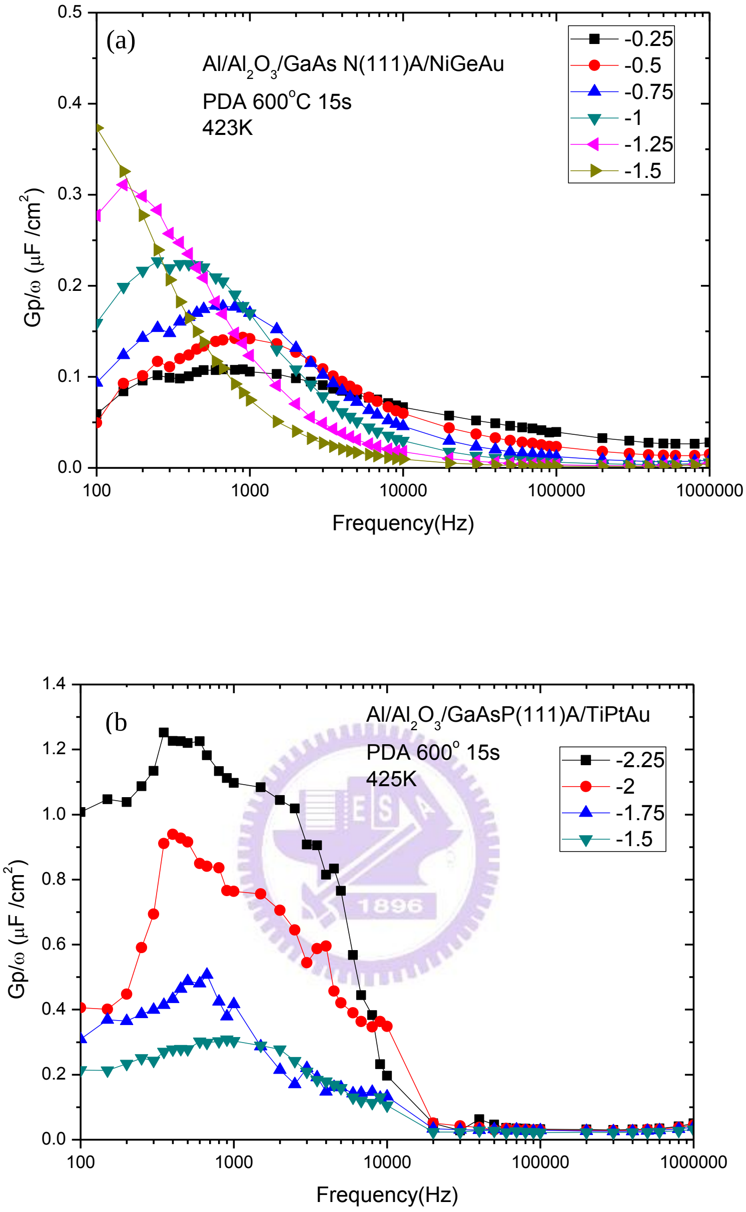


Fig. 2.18 G_p/ω as a function of frequency at 150℃ (a) N-type GaAs(111)A (b) P-type GaAs(111)A

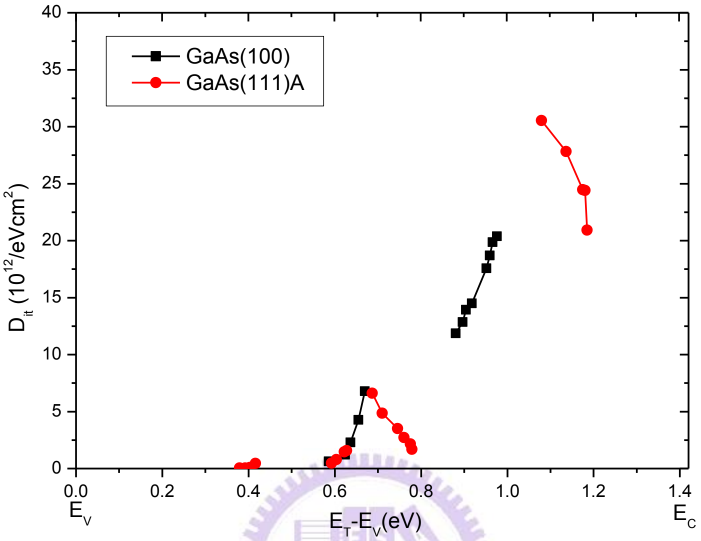
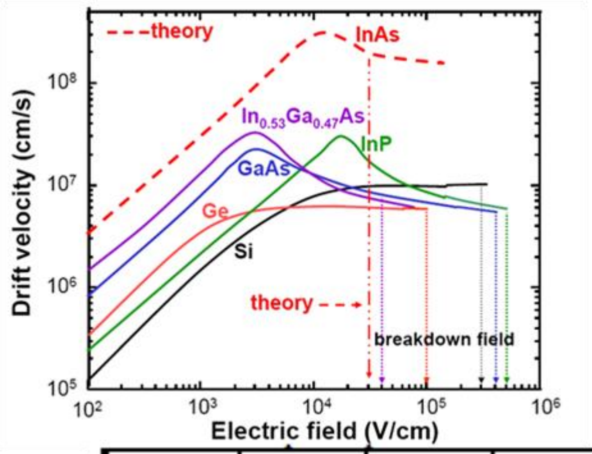


Fig. 2.19 Comparsion of D_{it} distribution of different surface orientation



◆ **Higher electron mobility(light m*)**

➡ **$v = \mu E$ ($\mu = q\tau/m^*$)**

◆**High velocity satuation**

◆**Lower intrinsic delay(light m*)**

➡ **$\tau_i \sim Q/I_{Dsat} \sim C_G V_D/I_{Dsat}$**

	Si	Ge	GaAs	InP	InAs	InSb
Electron mobility (cm²/Vs)	1600	3900	9200	5400	40000	77000
Electron mass (/m₀)	m_t: 0.19 m_l: 0. 916	m_t: 0.082 m_l: 1.467	0.067	0.082	0.023	0.014
Hole mobility (cm²/Vs)	430	1900	400	200	500	850
Hole mass (/m₀)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.28 m_{LH}: 0.044	0.45 0.082	0.45 0.12	0.57 0.35	0.44 0.016
bandgap (eV)	1.12	0.66	1.42	1.34	0.36	0.17

Fig. 2.20 III-V materials' advantages

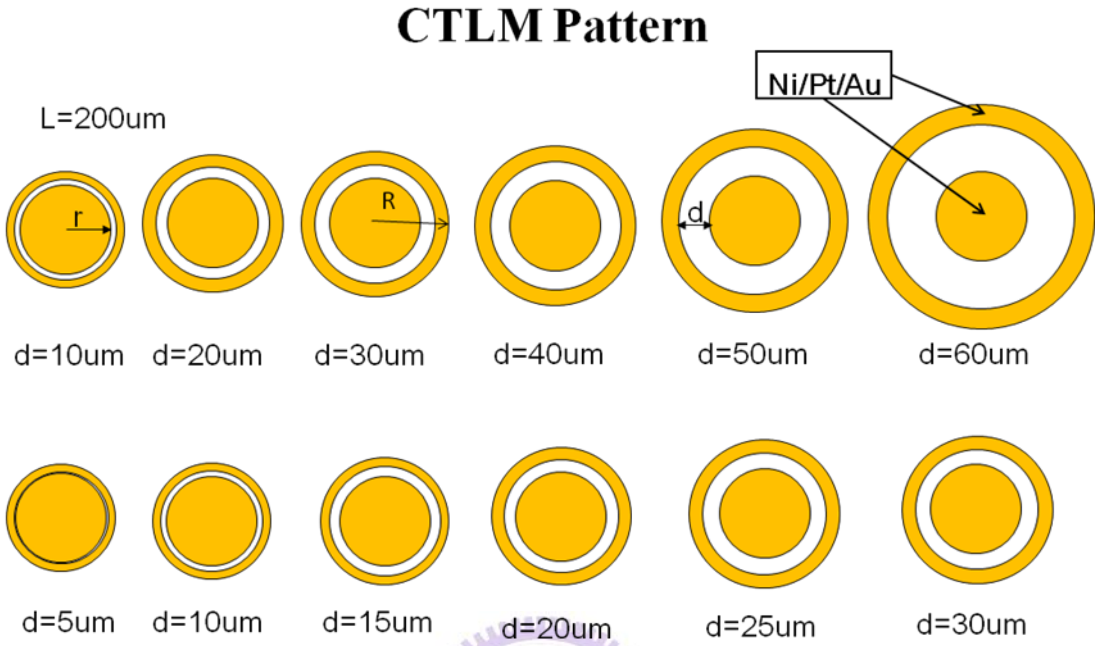
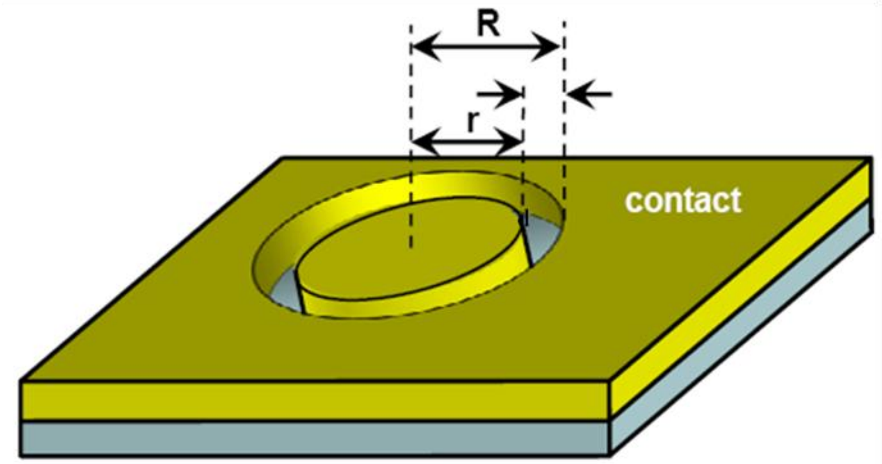


Fig. 2.21 CTLM Pattern



$$\frac{V}{I} = R_T = \frac{\rho_S}{2\pi}\left[\frac{L_T}{r} + \frac{L_T}{R} + \ln\left(1 + \frac{d}{r}\right)\right], \textit{where } L_T = \sqrt{\frac{\rho_C}{\rho_S}}$$

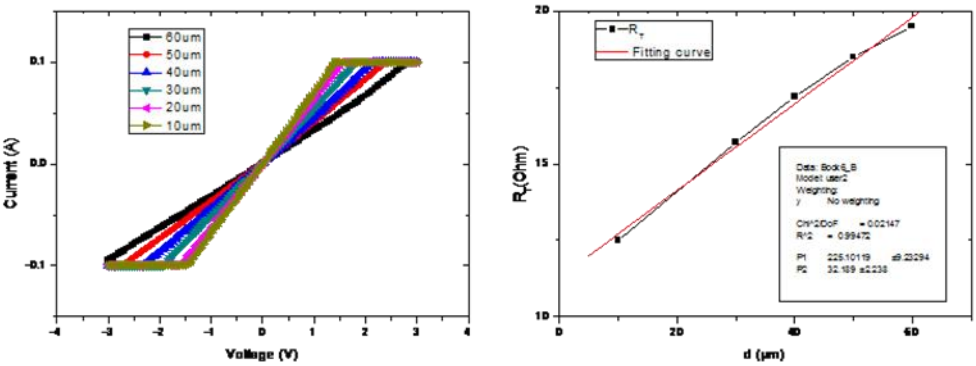
$$\rho_S = \text{Sheet resistance}\ , \rho_C = \text{Specific contact resistivity}$$

$$\mathrm{L_T} = \text{transfer length}$$

Fig. 2.22 Contact Resistance Extraction

(a)

Implant	Dopant Act.	Litho. Define
Si, 1E14cm^{-2} 30keV&80keV	950℃, 15S	Ni/Ge/Au contact



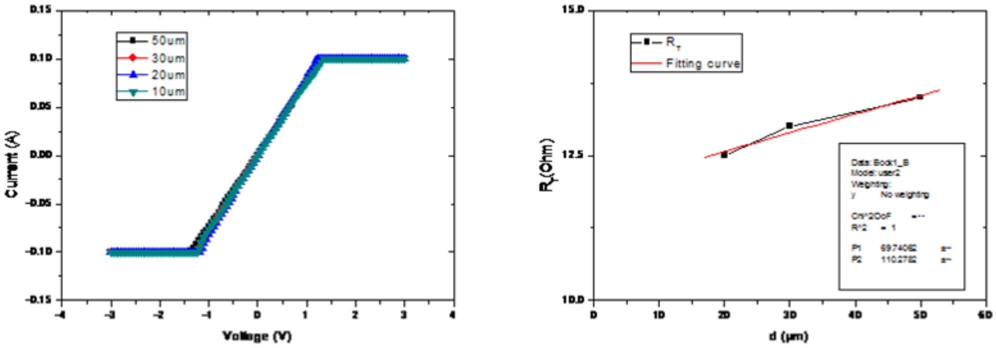
ρ_s =225.1(Ω/square)

L_T = 32.189um

$\rho_c = L_T{}^2 * \rho_s$ =2.33E-3(Ω-cm^2)

(b)

Implant	Dopant Act.	Litho. Define
Si, 1E14cm^{-2} 30keV&80keV	850℃, 15S	Ni/Ge/Au contact



ρ_s =69.74(Ω/square)

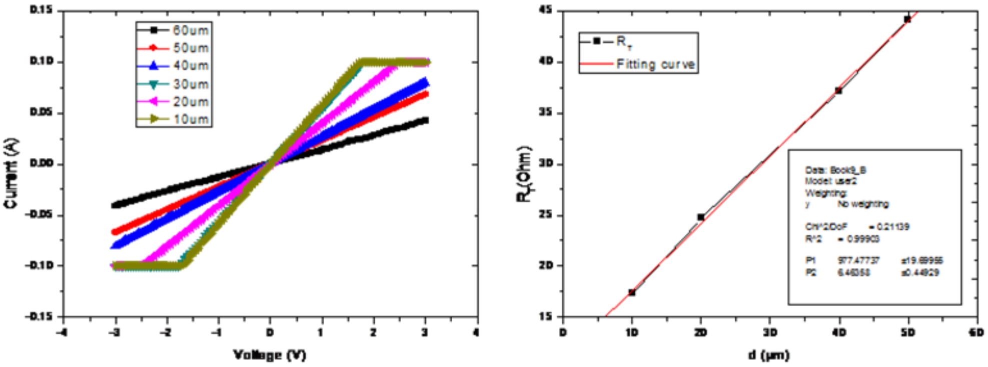
L_T = 110.27um

$\rho_c = L_T{}^2 * \rho_s$ =8.48E-3(Ω-cm^2)

Fig. 2.23 SI-GaAs(111)A (a) 30keV&80keV 950°C (b) 30keV&80keV 850°C

(c)

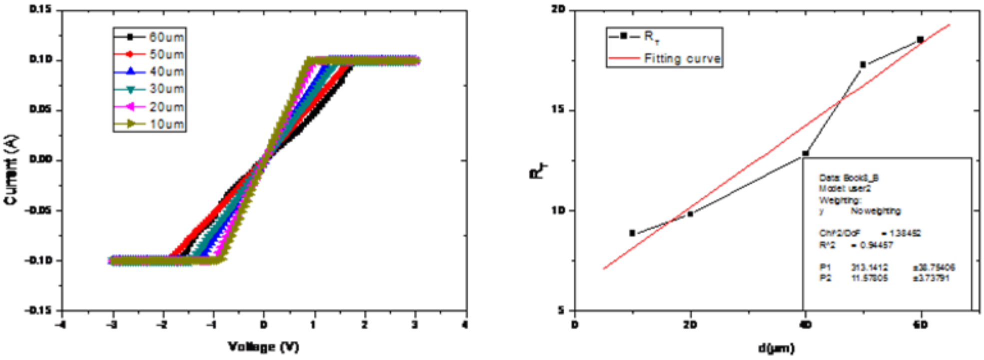
Implant	Dopant Act.	Litho. Define
Si, 1E14cm^{-2} 50keV	950℃, 15S	Ni/Ge/Au contact



ρ_s =977.47(Ω/square)
L_T = 6.46um
$\rho_c = L_T{}^2 * \rho_s$ =4E-4(Ω-cm^2)

(d)

Implant	Dopant Act.	Litho. Define
Si, 1E14cm^{-2} 50keV	850℃, 15S	Ni/Ge/Au contact



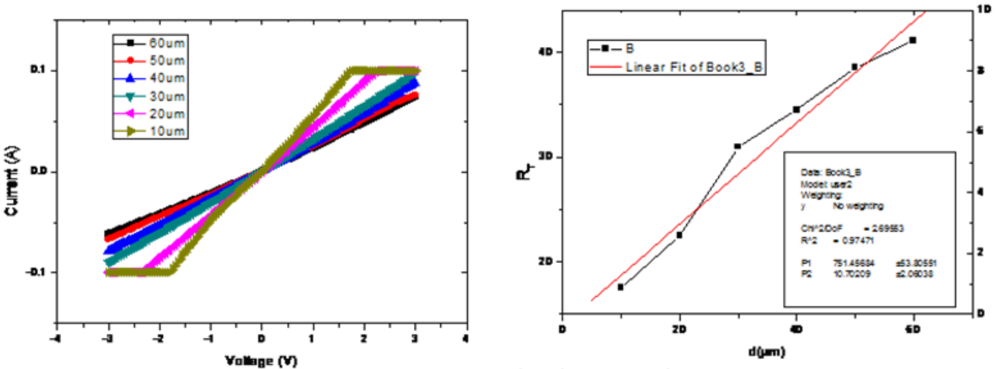
ρ_s =313.14(Ω/square)
L_T = 11.57um
$\rho_c = L_T{}^2 * \rho_s$ =4.19E-4(Ω-cm^2)

Fig. 2.23 SI-GaAs(111)A (c) 50keV 950^{o}C (d) 50keV 850^{o}C

SI-(111)A				
Implant source: Si				
Implant dose=1E14 cm-2				
number	Implant energy	Activity temperature	ρ_s (Ω/square)	ρ_c (Ω-cm2)
a	30keV&80keV	950^{o}C	225.1	2.3E-3
b	30keV&80keV	850^{o}C	69.74	8.48E-3
c	50keV	950^{o}C	977.47	4E-4
d	50keV	850^{o}C	313.14	4.19E-4

Table 2.1 Integration of SI-GaAs(111)A

Implant	Dopant Act.	Litho. Define
Si, 1E14cm^{-2} 50keV	850℃, 15S	Ni/Ge/Au contact



$$\rho_s = 751.45\ (\Omega/\text{square})$$

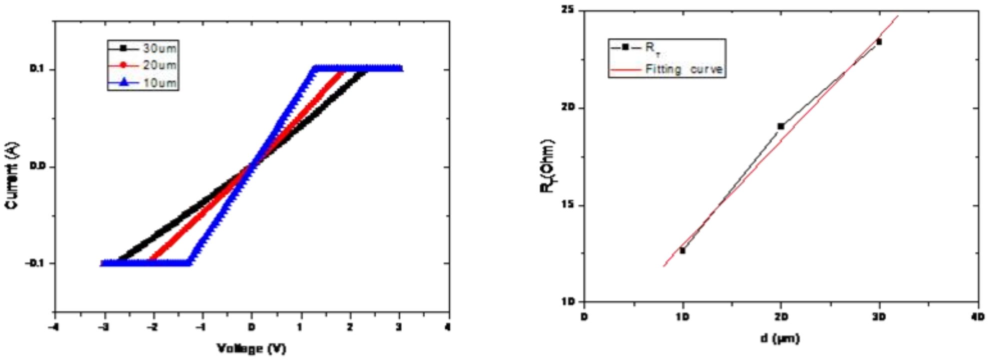
$$L_T = 10.70\text{um}$$

$$\rho_c = L_T^2 * \rho_s = 8.607\text{E-}4\ (\Omega\text{-cm}^2)$$

Fig. 2.24 SI-GaAs(100) at 50keV 950^{o}C

(a)

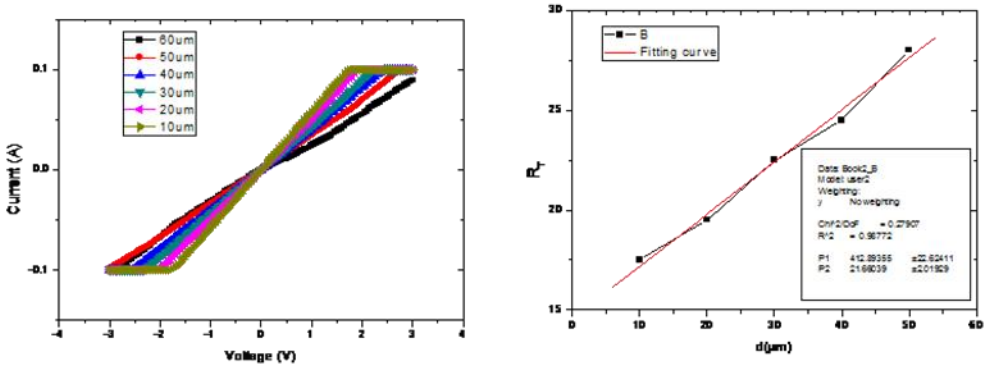
Implant	Dopant Act.	Litho. Define
Si, 1E14cm^{-2} 50keV	850℃, 15S	Ni/Ge/Au contact



$$\rho_s = 762.21\ (\Omega/\text{square})$$
$$L_T = 5.919\text{um}$$
$$\rho_c = L_T^2 * \rho_s = 2.67\text{E-}4\ (\Omega\text{-cm}^2)$$

(b)

Implant	Dopant Act.	Litho. Define
Si, 1E15cm^{-2} 30keV&80keV	850℃, 15S	Ni/Ge/Au contact

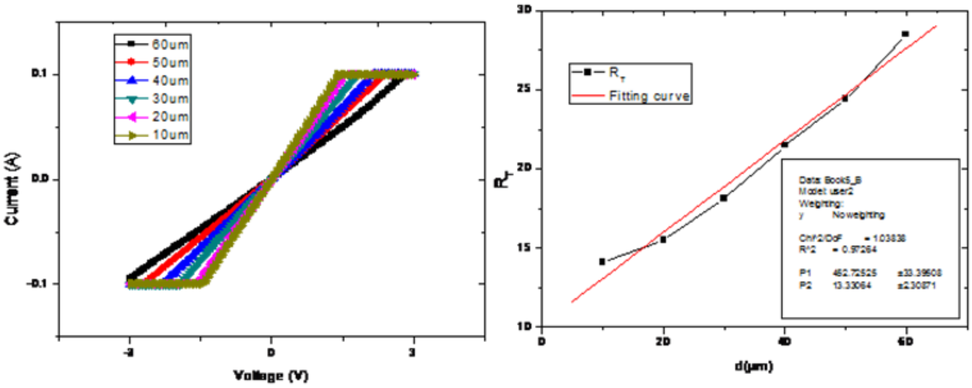


$$\rho_s = 413.4\ (\Omega/\text{square})$$
$$L_T = 21\text{um}$$
$$\rho_c = L_T^2 * \rho_s = 1.8\text{E-}3 (\Omega\text{-cm}^2)$$

Fig. 2.25 P-GaAs(100) at 850 °C (a) 50keV (b) 30keV&80keV

(a)

Implant	Dopant Act.	Litho. Define
Si, 1E15cm^{-2} 50keV	850℃, 15S	Ni/Ge/Au contact



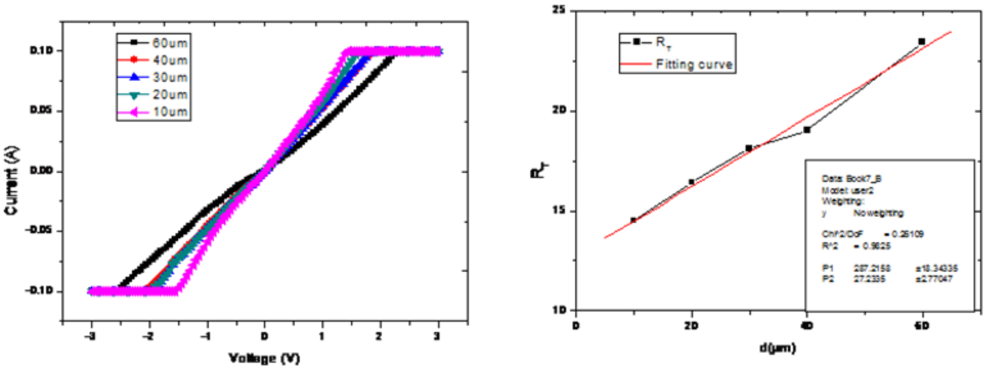
ρ_s = 452.72 (Ω/square)

L_T = 13.33um

$\rho_c = L_T^2 * \rho_s$ = 8.045E-4(Ω-cm^2)

(b)

Implant	Dopant Act.	Litho. Define
Si, 1E15cm^{-2} 30keV&80keV	850℃, 15S	Ni/Ge/Au contact



ρ_s =287.21(Ω/square)

L_T = 27.23um

$\rho_c = L_T^2 * \rho_s$ =2.13E-3(Ω-cm^2)

Fig. 2.26 P-GaAs(111)A at 850 °C (a) 50keV (b) 30keV&80keV

P-type GaAs				
Implant source: Si				
Implant dose=1E14 cm-2				
Orientation	Implant energy	Activity temperature	ρ_s (Ω/square)	ρ_c (Ω-cm2)
(100)	50keV	850°C	762.21	2.67E-4
(100)	30keV&80keV	850°C	413.4	1.8E-3
(111)A	50keV	850°C	452.72	8.045E-4
(111)A	30keV&80keV	850°C	287.21	2.13E-3

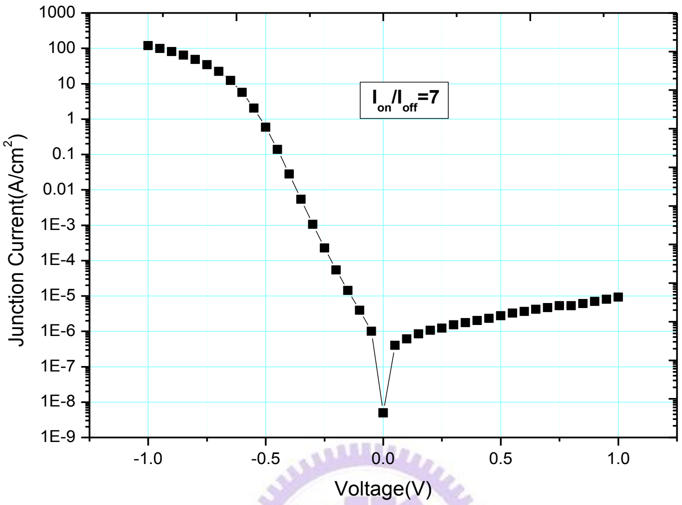
Table 2.2 Integration CTLM of P-GaAs at 850 °C

P-type GaAs(111)A		
Implant source: Si		
Implant dose=1E14 cm-2		
Implant energy 50keV		
Activity temperature	Alloy temperature and time	I_{on} / I_{OFF} ratio
950°C	400°C, 30s	7
950°C	400°C, 30s	0.5
850°C	400°C, 30s	6
850°C	400°C, 30s	0.5
750°C	400°C, 30s	6
750°C	400°C, 30s	0.5

Table 2.3 Integration juictions of P-GaAs(111)A

(a)

Implant	Dopant Act.	Litho. Define	alloy
Si, 1E14cm^{-2} 50keV	950℃, 15S	Ni/Ge/Au contact	**30s**



(b)

Implant	Dopant Act.	Litho. Define	alloy
Si, 1E14cm^{-2} 50keV	950℃, 15S	Ni/Ge/Au contact	**60s**

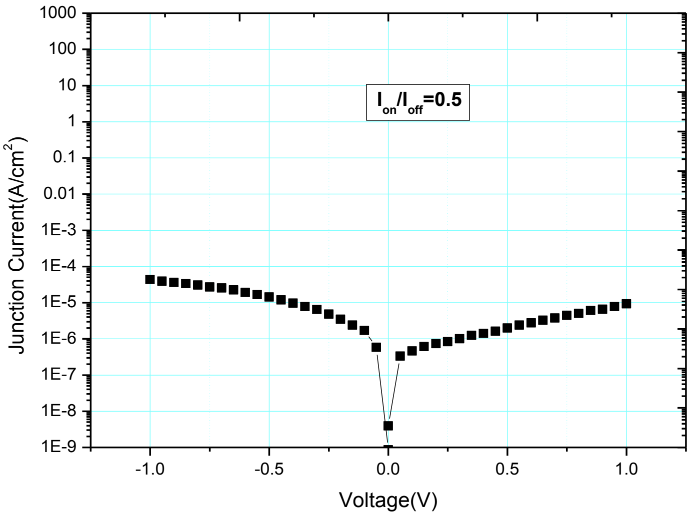
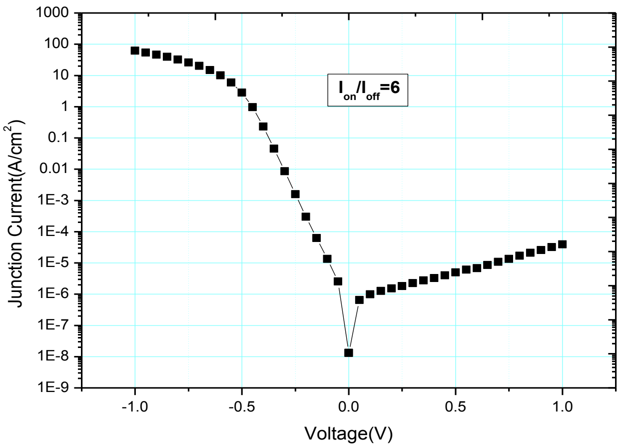


Fig. 2.27 Junction current vs the voltage applied at N+ layer of the fabricated N+ /P GaAs junctions with Si implant at activity temperature 950^{o}C(a) 30s (b)60s

(a)

Implant	Dopant Act.	Litho. Define	alloy
Si, 1E14cm^{-2} 50keV	850℃, 15S	Ni/Ge/Au contact	**30s**



(b)

Implant	Dopant Act.	Litho. Define	alloy
Si, 1E14cm^{-2} 50keV	850℃, 15S	Ni/Ge/Au contact	**60s**

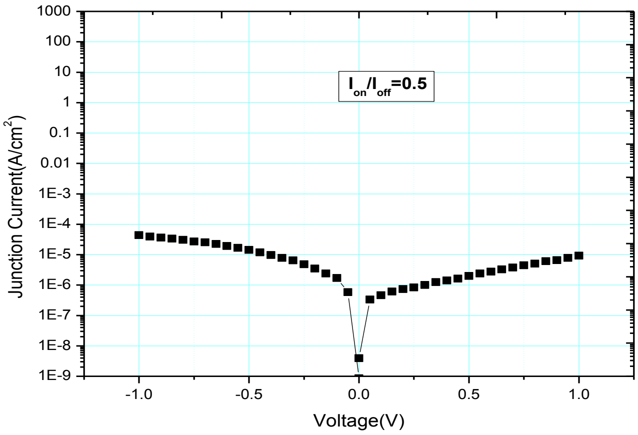
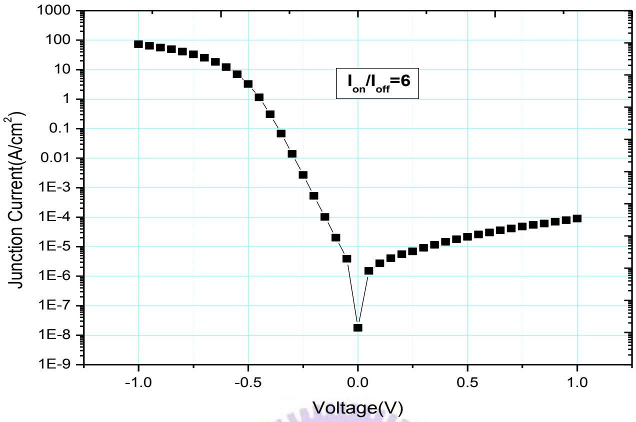


Fig. 2.27 Junction current vs the voltage applied at N+ layer of the fabricated N+ /P GaAs junctions with Si implant at activity temperature 850^{o}C(a) 30s (b)60s

(a)

Implant	Dopant Act.	Litho. Define	alloy
Si, 1E14cm^{-2} 50keV	750℃, 15S	Ni/Ge/Au contact	**30s**



(b)

Implant	Dopant Act.	Litho. Define	alloy
Si, 1E14cm^{-2} 50keV	750℃, 15S	Ni/Ge/Au contact	**60s**

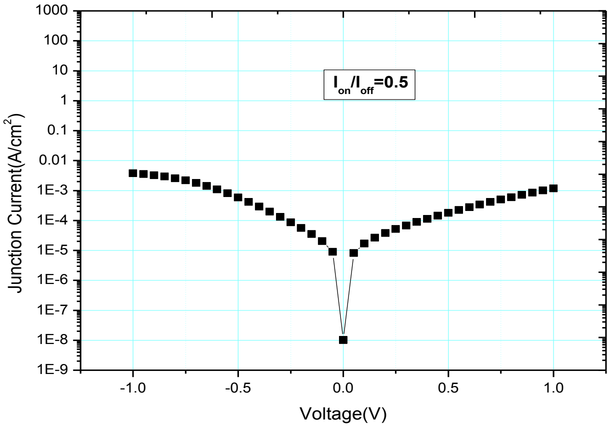


Fig. 2.27 Junction current vs the voltage applied at N+ layer of the fabricated N+ /P GaAs junctions with Si implant at activity temperature 750^{o}C(a) 30s (b)60s

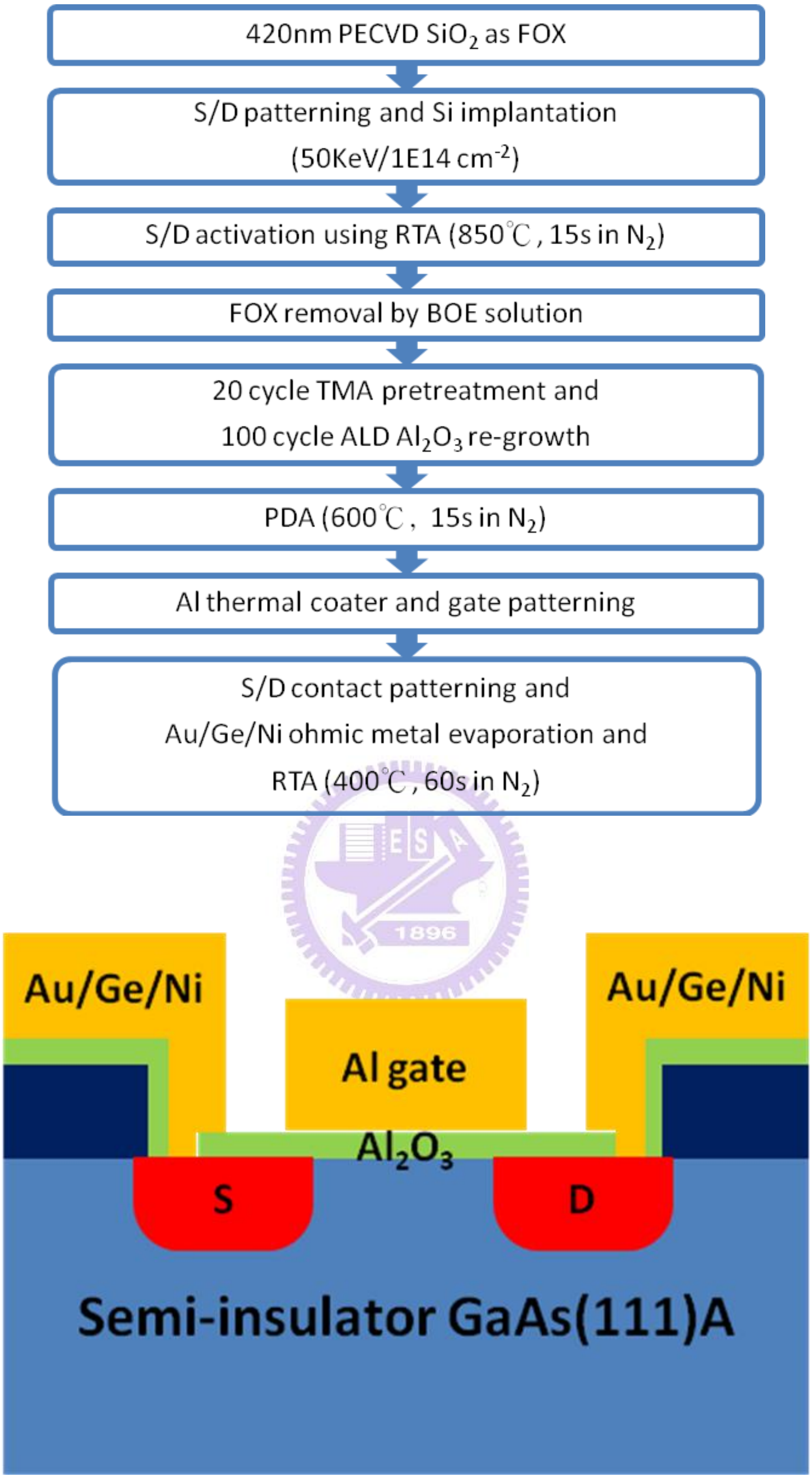


Fig. 2.28 The scheme and process flow of GaAs MOSFET

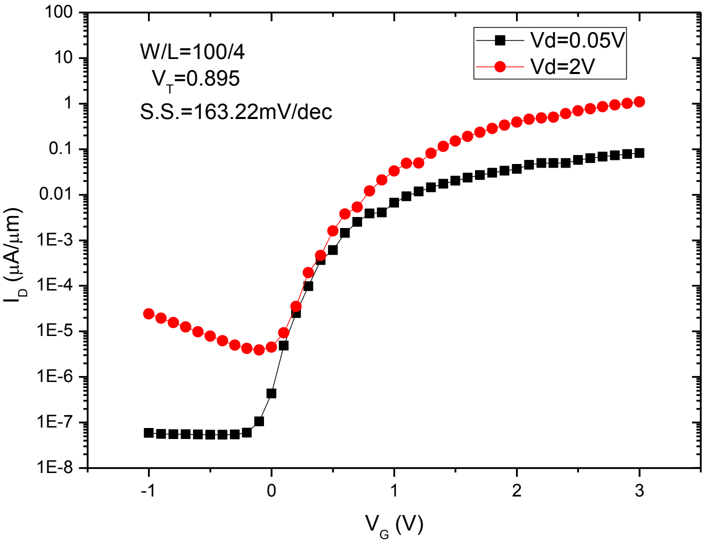


Fig. 2.29 Id-Vg of enhancement mode GaAs n-MOSFET

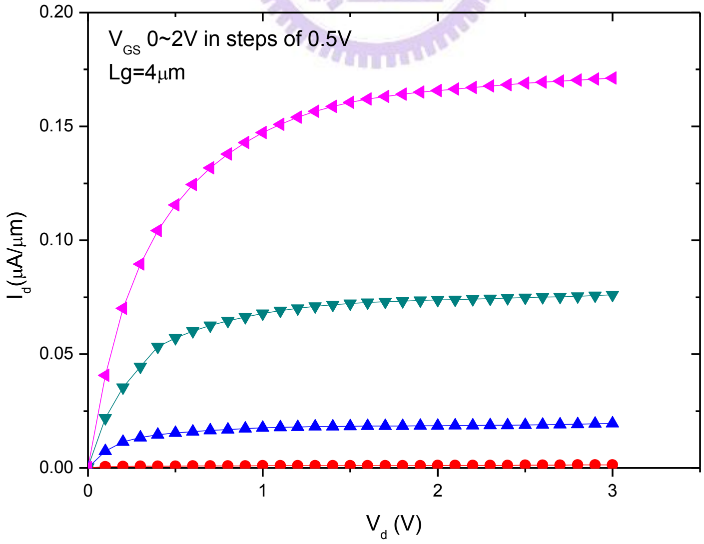


Fig. 2.30 Id-Vd characteristics of enhancement mode GaAs n-MOSFET

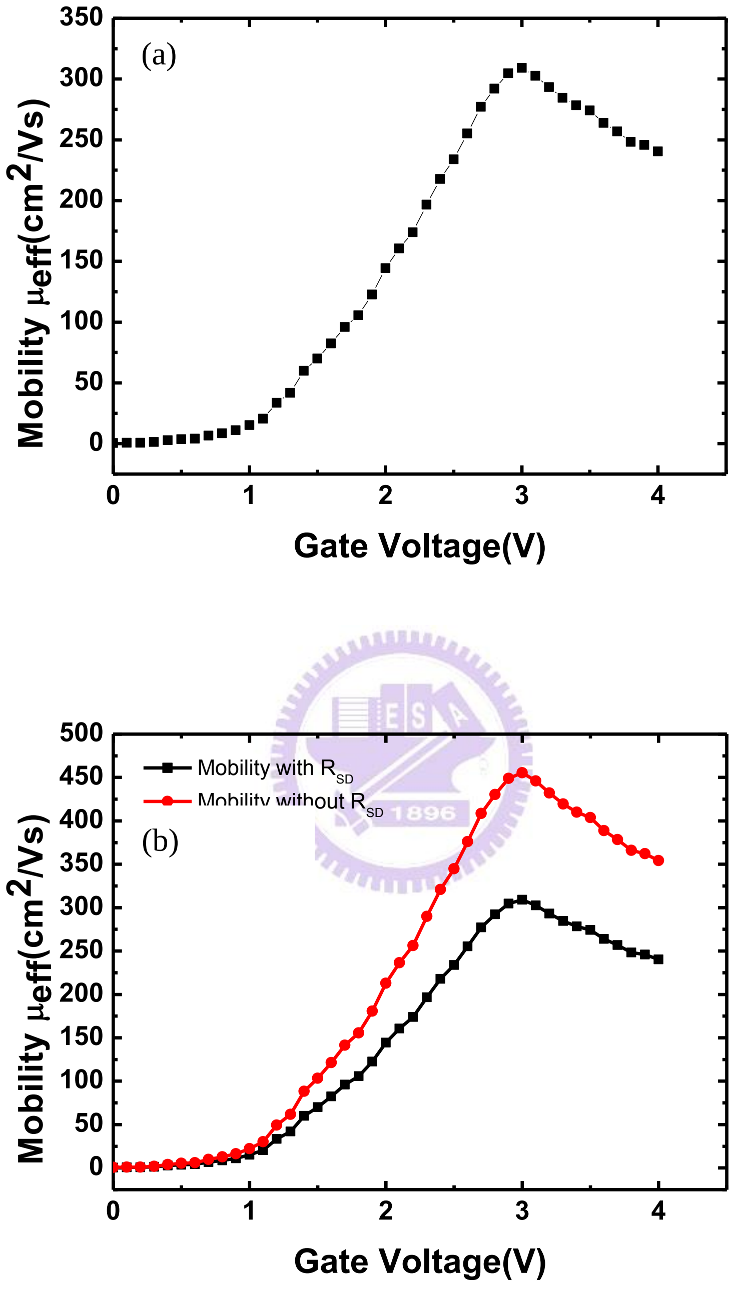


Fig. 2.31 The effective mobility on E-mode GaAs n-MOSFET (a) Mobility with R$_{SD}$ (b) Mobility without R$_{SD}$

Chapter 3

Improved electrical characteristics of GaAs(100) MOS capacitors with silane passivation

3.1 Introduction

CMOS (complementary metal oxide semiconductor) devices have been scaled down. The scaling down of physical thickness of SiO2 gate dielectrics has improved the speed of output drive current by shrinking of transistor area in front-end-process of integrated circuits. Silicon dioxide gate dielectric having the excellent material and electrical properties such as good interface (D_{it} ~2×10^{10} $eV^{-1}cm^{-2}$), low gate leakage current, higher dielectric breakdown immunity (≥10 MV/cm) and excellent thermal stability at typical Si processing temperature has been commonly used as the leading gate oxide material.

The prospect of improved device performance from III-V materials have five decades. A key restriction enabling widespread use of III-V materials is the lack of a high quality, natural insulator for III-V substrates like Silicon system. The literature on the subject that research efforts on achieving low interfacial density of states (D_{it}) covers the past 40 years. The treatment or passivation methods developed on GaAs maybe are applied to other III-V compound semiconductors [1]. In order to improve interface of III-V, atomic-layer-deposited (ALD) Al_2O_3, HfO_2 high-k dielectrics are potential candidates. Why does ALD process can reduce interface states? It is because that ALD precursor can “self-clean” interfacial native oxide, like As-oxide [2-4]. Sulfide chemical and in-situ or ex-situ deposition of ultrathin Si or

Ge interfacial control layer are also good methods for reducing interface states and improve electrical characteristics [5-10]. The interfacial control layers form bonding which can resist oxidation.

In this chapter, we will discuss the electrical characteristics and reliability of $Al/Al_2O_3/GaAs$ MOS capacitors with silane treatment under post deposition annealing (PDA) condition.

3.2 Experimental Procedures

3.2.1 Surface pretreatment

MOS capacitor sample was prepared on high Si-doped (p-type, $1\sim5\times10^{17}$ cm^{-3} and n-type, $1\sim5\times10^{17}$ cm^{-3}) GaAs with (100) crystal orientation substrates. We have three clean steps. At first, the GaAs was rinsed in the diluted HCl (HCl : H_2O = 1 : 3) solution for 3 min for native oxide removal, followed by rinsed in deionized water (D.I. water) for 5 min. Second, the GaAs was rinsed in the diluted NH_4OH (NH_4OH : H_2O = 1 : 10) solution for 10 min for excess elemental arsenic removal, followed by rinsed in D.I. water for 5 min. Third, the GaAs was rinsed in the $(NH_4)_2S$ solution at room temperture for 10 min for ex-situ surface passivation, followed by rinsed in D.I. water for 5 min.

After above surface pretreatment, we have two steps of surfaces pre-treatment. To reduce native oxide formation, the wafers were then quickly loaded into the chamber of UHVCVD. At first, vacuum annealing: thermal desorbed native oxide on the surface of substrate at 600 ℃ for 1 min ,and then silane passivation at 420°C for 90s(the flow rates of SiH_4 were 10 sccm)

3.2.2 ALD High-k Al_2O_3

The samples mounted in the ALD chamber and gave 20 trimethylaluminum (TMA) precursor pulses for reducing residual native oxide. And then, the Al_2O_3 gate dielectric was deposited by ALD at 250 ℃, followed by post deposition annealing (PDA) at 600 °C for 15 s in a N_2 ambient and not PDA. Thermal annealing can further improve the quality of dielectric.

3.23 Metal deposition

Thermal evaporated 400 nm Al were patterned as gate electrodes through the lithography. Finally, e-beam evaporated Ti/Pt/Au (50 Å/300 Å/1800 Å) for p-type and Ni/Ge/Au (300 Å/700 Å/1800 Å) for n-type was deposited as backside contact.

The complete process flow was shown in **Fig. 3.1**. The electrical characteristics of Al/Al_2O_3/p-GaAs/TiPtAu and Al/Al_2O_3/ n-GaAs/NiGeAu MOS capacitors were measured using an HP4284 and HP4200, respectively.

3.3 Capacitance-Voltage characteristics for GaAs(100) with silane passivation

3.3.1 Capacitance –Voltage characteristics for GaAs(100)

First of all, we exhibit the basic properties of the GaAs (100) p-type and n-type MOS capacitor C-V curves with multi-frequency, as shown in **Fig. 3.2 (a) and (b)**, respectively. The quantities can evaluate the quality of high-k dielectrics and I-S interface. I will choose two quantities to explain electrical characteristics. First, I defined frequency dispersion ratio≡ΔC . The equation of ΔC is reproduced according to Eq.(2.1)

$$\Delta C \equiv (C\ (@1kHz) - C\ (@100kHz)\ )/\ C\ (@1kHz) \qquad (3.1)$$

The p-type GaAs (100) frequency dispersion (3.34%@V_{FB}) are more excellent than n-type GaAs (100) frequency dispersion (9.99%@+3V). We believed that the upper half interfaces of bandgap exist a large amount of density of states (Ga-Oxide). It slow the Fermi-level is pinned at the upper half interface of bandgap when we supply voltage to gate.

The second is the hysteresis that results when the MOS capacitor is biasd from accumulation to inversion and then swept back. First, we must calculate V_{FB}. The equation(3.2) is show below:

$$\max[[1/(C/C_{ox})^2] / dV_g]|_{V_g = V_{FB}} \qquad (3.2)$$

Fig. 3.3 (a) and (b) show the results of n-type and p-type $V_{FB.}$ After V_{FB} are calculated, The p-type GaAs (100) hysteresis is 450mV, and n-type GaAs (100) hysteresis is 750mV as shown in **Fig. 3.4 (a) and (b)**

3.3.2 Capacitance –Voltage characteristics for GaAs (100) with silane passivation

After introducing capacitance-voltage of GaAs(100), **Fig. 3.5 (a) and (b)** show the MOS capacitor C-V curves of the GaAs (100) p-type and n-type with silane passivation. The figures compare to **Fig. 3.2 (a) and (b)**, No silane passivation’s samples can’t reach accumulation even at +3V applied to the gate. This case is because the Firmi-level is pinned for a large of interface density of states. The MOS capacitor with silane passivation revealed C-V behavior can reach accumulation and had low stretch-out in depletion. The p-type GaAs (100) frequency dispersion is 5.08% (@-3V) and n-type GaAs (100) frequency dispersion is 5.9% (@+3V). The values revealed interface of states maybe were lower compared to sample without silane. **Fig. 3.5 (c) and (d)** show that The p-type GaAs (100) hysteresis is 300mV, and n-type GaAs (100) hysteresis is 650mV. However, p-type GaAs(100) with silane passivation degraded of electrical characteristics that maybe were due to generate As-As bond, so the interface trap states increased.

3.4 Effective reduction interfacial traps using thermal annealing

Thermal annealing can further improve the quality of dielectric and reduce the interface density of states. Meanwhile, during high temperature process it is important to inhibit the loss of As within the GaAs substrate and also suppress the formation and subsequent incorporation of native oxides.

3.4.1 Capacitance –Voltage characteristics for GaAs(100) PDA

Recently, post-deposition anneal (PDA) can further improve the quality of dielectric materials. So, we used PDA into our processing procedure. we exhibit the basic properties of the GaAs (100) p-type PDA and n-type PDA MOS capacitor C-V curves with multi-frequency, as shown in **Fig. 3.6 (a) and (b).** In the figure, the p-type GaAs (100) frequency dispersion (3.2%@-3V) are more excellent than n-type GaAs (100) frequency dispersion (11%@+3V). **Fig. 3.6 (c) and (d)** showed that the p-type GaAs (100) hysteresis is 300mV, and n-type GaAs (100) hysteresis is 600mV. We summarized 3.4.1 and 3.4.2 n-type have larger frequency dispersion and hysteresis than p-type GaAs(100). According to the literature, the Ga_2O_3 didn't be removed completely, so the frequency dispersion is much worse on n-type GaAs substrate. After PDA process, the frequency dispersion and hysteresis of n-type GaAs(100) both have significant improvement, but p-type GaAs(100) are not.

3.4.2 Capacitance –Voltage characteristics for GaAs (100) with silane passivation

Fig. 3.7 (a) and (b) show the MOS capacitor C-V curves of the GaAs (100) p-type As and n-type As with silane passivation. Similarly, we quantitated the electrical characteristics. The p-type GaAs (100) frequency dispersion is 3.54%(@-3V) and n-type GaAs (100) frequency dispersion is 5.78%(@+3V). **Fig. 3.7 (c) and (d)** show that The p-type GaAs (100) hysteresis is 300mV, and n-type GaAs (100) hysteresis is 350mV. However, the electrical characteristics of p-type GaAs(100) with silane passivation was degraded that the frequency dispersion was increased. We optimized conditions of annealing and silane time can reduce the density of states for good electrical characteristics of p-type and n-type.

3.5 Admittance Behavior of GaAs MOS capacitor

3.5.1 Conductance method application of GaAs MOS capacitor

First, we measured C-V at 25℃ for different types in **Fig. 3.8**. According to the figures, Fermi-level is completely pinned, so the C-V behaviors can't vary by gate bias. Why were the Fermi-level pinned? At present, we believe that the density of states (D_{it}) were large at interface of bandgap. In addition, we also measured C-V with at 25℃ for different types in **Fig. 3.9**.

Fig 3.10 and **Fig. 3.11** illustrates the G_p/ω versus f plots of MOS capacitor without and with silane passivation, and measurement is performed at room temperature. G_p/ω curves are shown at the gate voltages Fermi level is only portions of the bandgap where interface states are able to capture and emission with the small signal AC bias. The peak value of each G_p/ω curve corresponds to the interface state density and thus D_{it} as a function of gate voltage can be plotted. Then, the equation $\Delta E = kT\ln(\frac{V_{th}\sigma N}{\pi f})$ combined with the value of maximum value of G_p/ω transforms the D_{it} (V_G) into D_{it} (E) plot. The peak value of G_p/ω can't be observed for GaAs(100) without silane. This reason maybe is a large of density of state nearer to midgap, so the Firmi-level is pinned. Therefore, the D_{it} profile of GaAs(100) without silane passivation can't be extracted, and we only show **Fig. 3.12** for GaAs(100) with SiH_4 passivation.

3.5.2 High Temperature Measurement of GaAs MOS capacitor

In order to obtain the full distribution of D_{it} in the bandgap, conductance method is applied at high temperatures. The multi frequency CV characteristics measured at 423K are shown in **Fig. 3.13 and Fig. 3.14** including without and with silane passivation. **Fig. 3.15 and Fig.3.16** G_p/ω curves are shown at the gate voltages Fermi level is near the midgap where interface states are able to capture and emission with the small signal AC bias. The peak value of each G_p/ω curve corresponds to the interface state density and thus D_{it} as a function of gate voltage can be plotted. We interpret the largest G_p/ω value to represent D_{it} at the specific position in bandgap. the D_{it} profile of each sample near midgap for without passivation is demonstrated in **Fig 3.17** and with passivation is demonstrated in **Fig 3.18**.

According to these figures, we saw D_{it} decreased obviously for n-type GaAs(100) with silane passivation. Simultaneously, we saw D_{it} increased for p-type GaAs(100). Although, the value of D_{it} increase didn’t affect the capacitor reach accumulation. We still optimize the condition of annealing and silane time for future.

3.6 Reliability characteristics of GaAs(100) with silane passivation

The reliability of ultra-thin high-k gate dielectrics have become more important, as high field applied to gate dielectric results in higher trap generation and oxide breakdown[11-15]. In the section, the charge trapping/detrapping behavior in ultra-thin dielectric with silane has been studied by constant-voltage stressing (CVS) compared to ultra-thin dielectric without silane passivation since the presence of oxide traps significantly affect the device performance. Recently, stress induced leakage current (SILC) produced is one of the major reliability concerns in thin dielectrics, we will discuss the phenomenon later.

In order to discuss the interfacial characteristics during operation, the MOS capacitor structure were supplied by constant-voltage stressing (CVS) at different voltages (-3V~-5V). **Fig 3.19** shows the high frequency (100MHz) C-V characteristics of GaAs (100) MOS capacitor including flash and 100s constant-voltage stressing. It is well-known that the applied voltage stress generates a large number of traps in the high-k dielectric as the stress mode. The shift is believed that positive charges or the hole trapping were generated in the gate dielectric. According to these figures, we observed that GaAs(100) with passivation have excellent electrical characteristic compared to without passivation.

3.7 Electrical characteristics of GaAs MOSFET

3.7.1 Introduction

In order to obtain the superior III-V device performance, it is essential to achieve the unpinned oxide/substrate interface. Today, the pinning issue is still interest and challenging for the dielectrics stack on III-V substrate that because of a larger energy difference between the charge neutrality level and the conductance band edge [16]. Using various kinds of the passivation methods, such sulfur treatment [18-17], silane [19-20], and Si passivation [21-23], reduce the native oxides and other surface defects for decreased intermixing and lower D_{it}. In this chapter, in order to obtain high performance characteristic, we will use vacuum annealing and SiH_4 passivation to reduce density of state.

In this chapter, we fabricated the circular transmission line method (CTLM) for analyzing contact and sheet resistivity. And then, we fabricated the junction of different conditions. After optimizing the conditions of CTLM and junction, we also succeeded to fabricate the enhancement-mode (E-mode) GaAs n-MOSFET with ALD- Al_2O_3 gate dielectrics on the GaAs substrate.

3.7.2 Experimental Procedures

In GaAs MOSFET fabrication, we used ALD and PECVD to deposit Al_2O_3 10 nm and SiO_2 420 nm as isolation layer, and then, defined the Si which were implanted the doses 1×10^{14} cm^{-2} at 50keV. After deposit SiO_2 encapsulation layer, S/D activation was using RTA at 850℃ for 15 s in N_2 ambient. The SiO_2 was subsequently removed from the active region and then the sample was cleaned by diluted HCl, diluted NH_4OH, $(NH_4)_2S$ solution. After surface cleaning, the sample was loaded in UHVCVD for vacuum annealing and SiH_4 passivation. And then mounted in the ALD chamber and gave 20 trimethylaluminum (TMA) precursor pulses for reducing residual native oxide. And then, the Al_2O_3 gate dielectric was deposited by ALD at 250 ℃, followed by two conditions include post deposition annealing (PDA) at 600 ℃ for 15 s in a N_2 ambient and not PDA. Thermal coatered Al about 4000 Å were patterned as gate electrodes through the lithography. After etching the S/D contact holes, the S/D matel of Ni/Ge/Au (30 nm/70 nm/180 nm) was deposited at the S/D region by using E-gun system and lift-off process, followed by PDA at 400℃ for 30 s in an N_2 ambient to form Ohmic contact. The fully process flow of GaAs MOSFET was shown in **Fig. 3.20**.

3.7.3 Result and conclusions

Fig. 3.21 displayed the I_D-V_G characteristics with a drain bias of 0.1V and 2V. The gate length of the device is 10μm and the gate width is 100μm the value of V_{th} was 1.25 V which is extracted by linear extrapolation.

The I_D versus V_D output characteristics of the device are presented in **Fig. 3.22** with V_g from 0V to 3V and a step of 1 V. The drive current at V_g =3V is ~3.5nA/μm measured at V_D = 3V.

3.8 Summary

Unlike SiO_2 on Si, III-V materials such as GaAs don't have such a native oxide that have high quality, thermodynamically stable properties that can be stable on the device criteria as SiO_2 on Si. Poor dielectric quality results in frequency dispersion, hysteresis, flab band shift, and unfavorable low dielectric constant. In the section 3.3 and 3.4, we can obviously see these phenomenon for GaAs(100) without passivation. We investigated the surface treatment effects on the electrical characteristics of GaAs(100) capacitors with silane passivation and PDA. The pretreatment diminished the formation of GaAs native oxide, thus improve the effect of Fermi-level pinning appearance. According to these electrical characteristics, the passivation sample displayed not only small frequency dispersion, but also small hysteresis. In order to confirm the electrical characteristics, we used the conductance method to extract distributions of D_{it} for different interface passivation. At the first, we measured the multi-frequency of C_m-f and G_m-f which are measured at the different temperature conditions. Next, we calculated the $G_p/\omega$and extracted D_{it} by conductance method, we can accurately determined D_{it} distribution across the bandgap. And then, we measured the reliability of P-GaAs(100) without and with silane passivation. A clear understanding of reliability of this different interfaces, via charge trapping/detrapping studies under different stressing condition, we observed the silane passivation can improve the reliability of GaAs(100). Finally, utilizing the electrical characteristic of the GaAs MOS capacitor to decide the experimental condition is suitable in manufacture procedure of enhance-mode GaAs(100) MOSFET.

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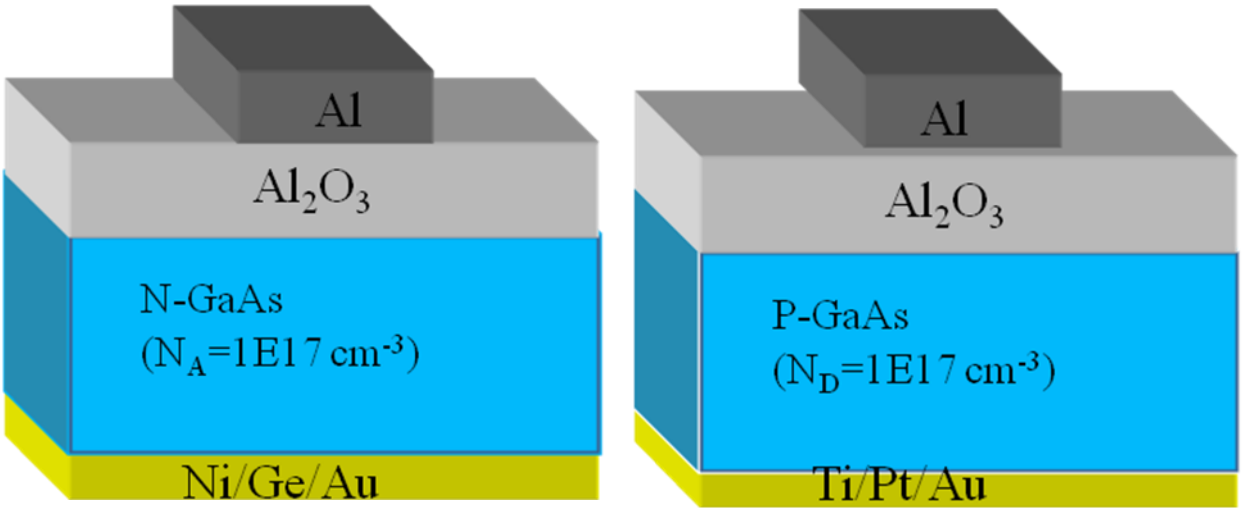
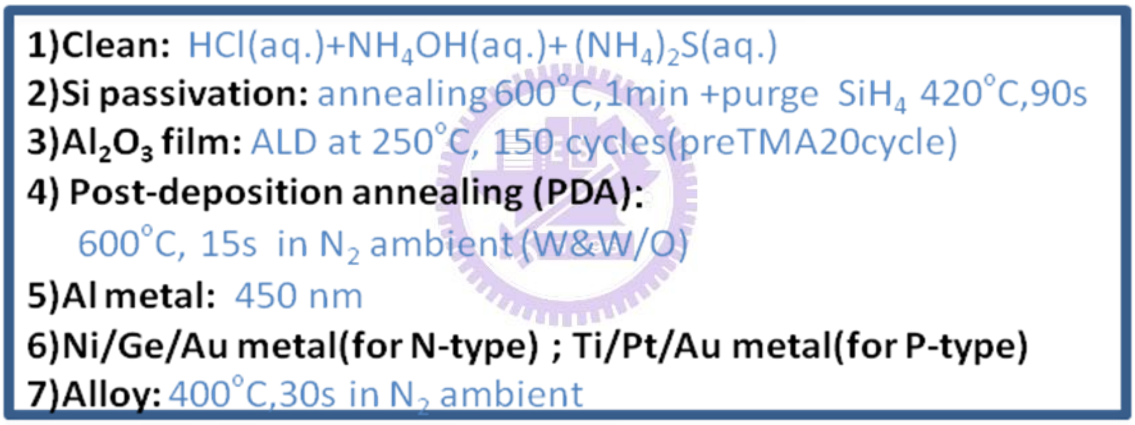




1)Clean: HCl(aq.)+NH_4OH(aq.)+ $(NH_4)_2S$(aq.)

2)Si passivation: annealing 600°C,1min +purge SiH_4 420°C,90s

3)Al_2O_3 film: ALD at 250°C, 150 cycles(preTMA20cycle)

4) Post-deposition annealing (PDA):

600°C, 15s in N_2 ambient (W&W/O)

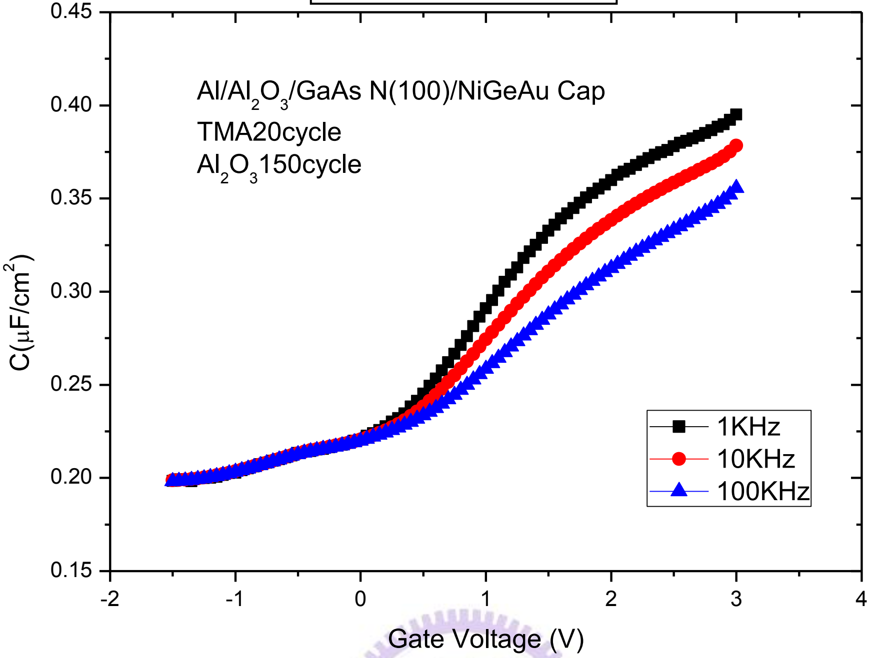
5)Al metal: 450 nm

6)Ni/Ge/Au metal(for N-type) ; Ti/Pt/Au metal(for P-type)

7)Alloy: 400°C,30s in N_2 ambient

Fig. 3.1 The structure and process flow of MOS capacitor.

(a)N-type



(b)P-type

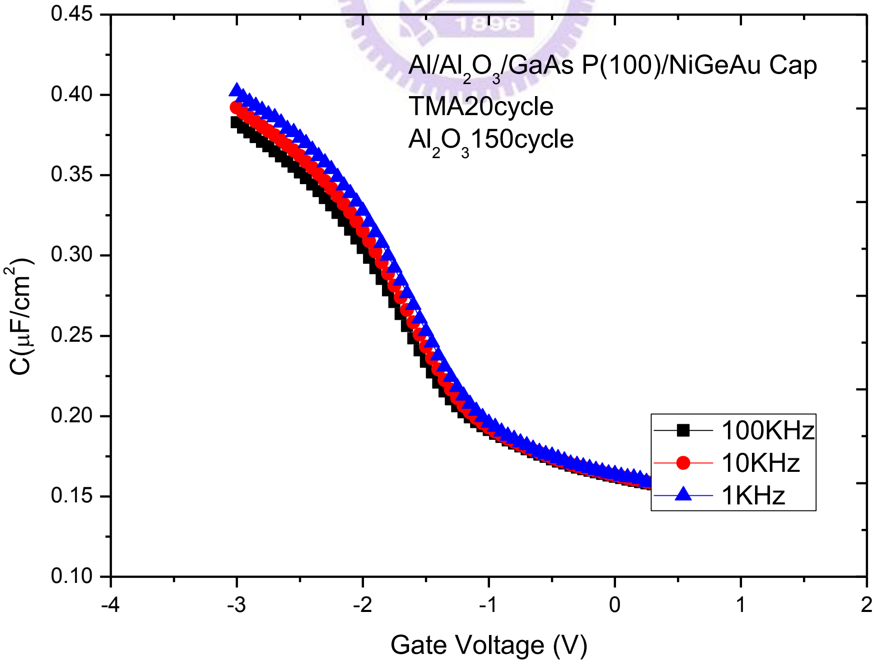


Fig. 3.2 Multi-frequency C-V curve (a) N-type GaAs(100) (b) P-type GaAs(100)

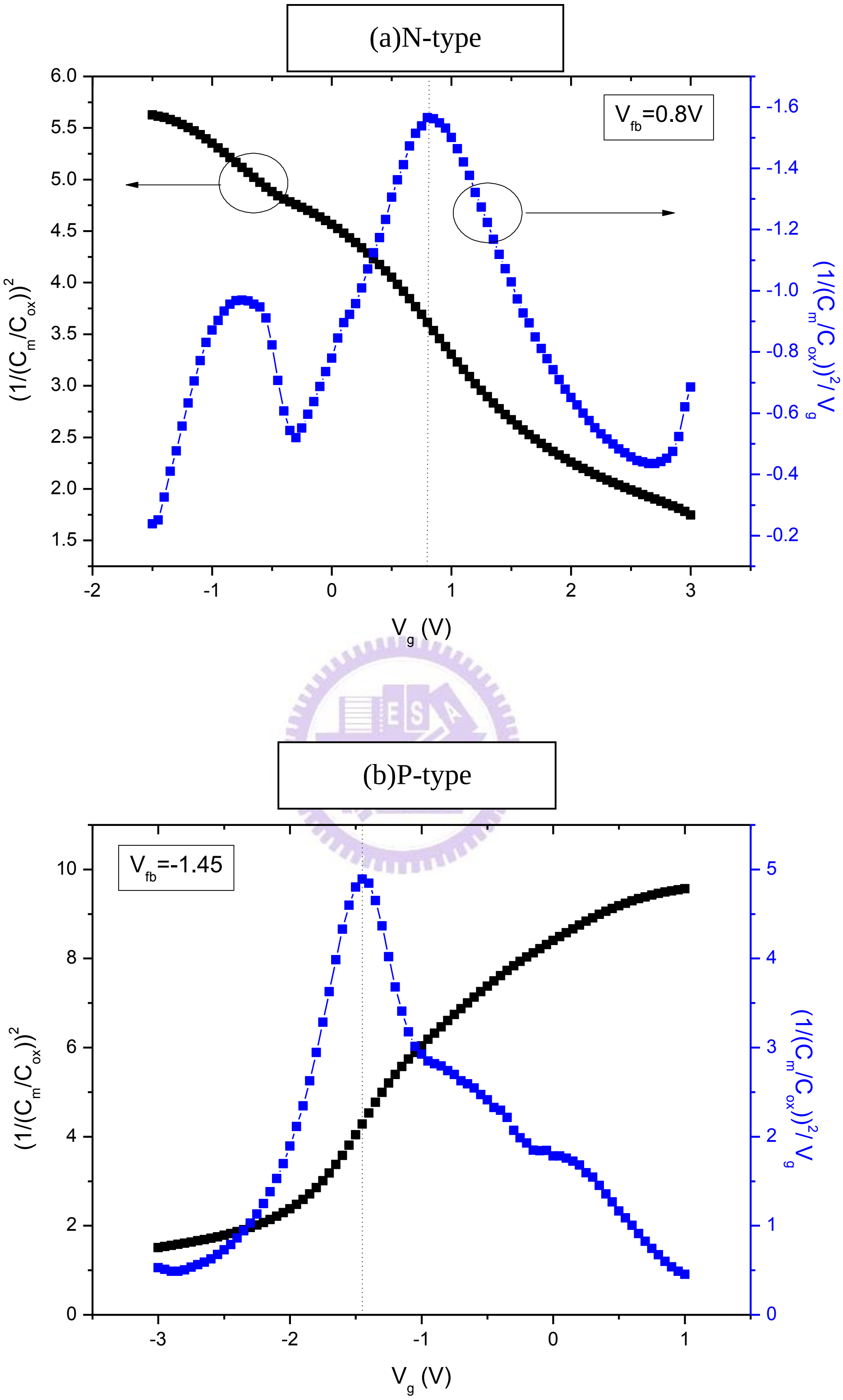
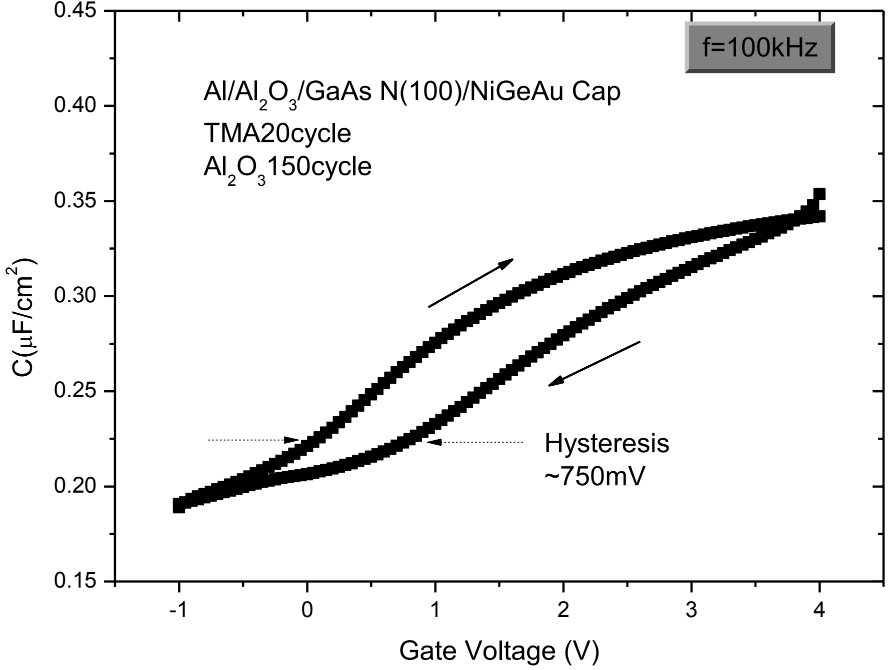


Fig. 3.3 Extraction of V_{FB}; (a) N-type V_{FB} (b) P-type V_{FB}

(a)N-type



(b)P-type

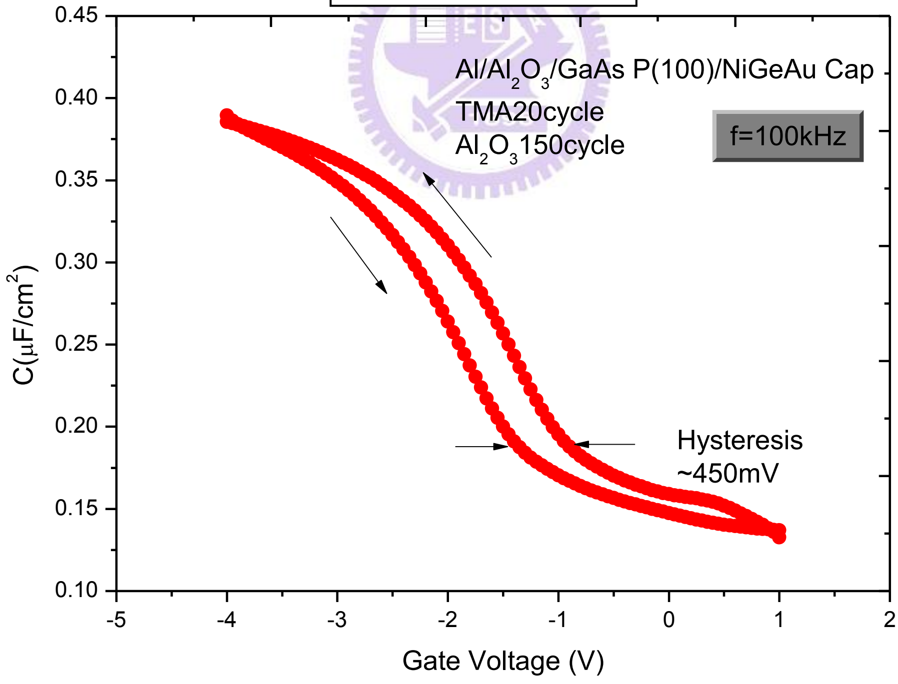
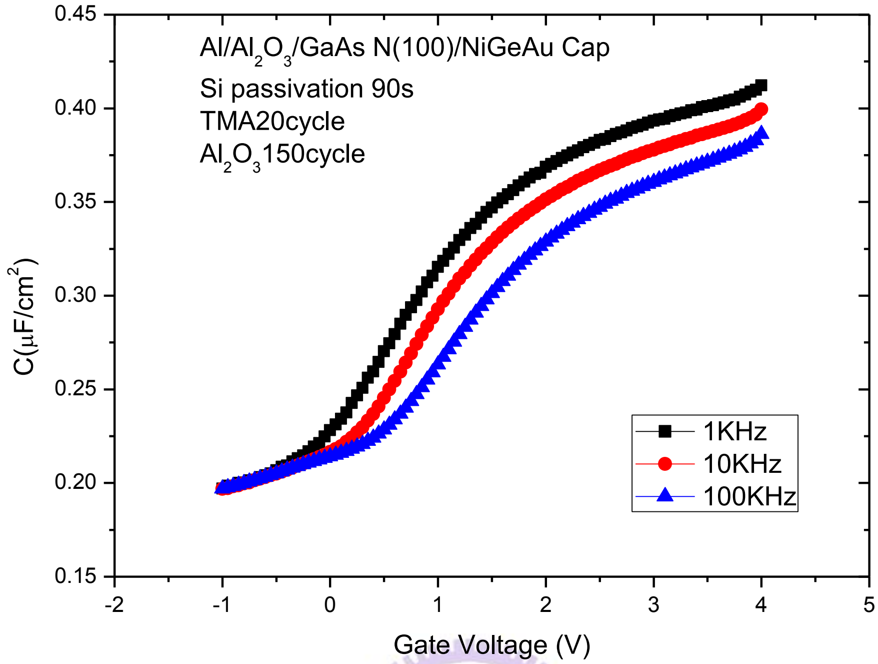


Fig. 3.4 Hysteresis C-V curve (a) N-type GaAs(100) (b) P-type GaAs(100)

(a)N-type



(b)P-type

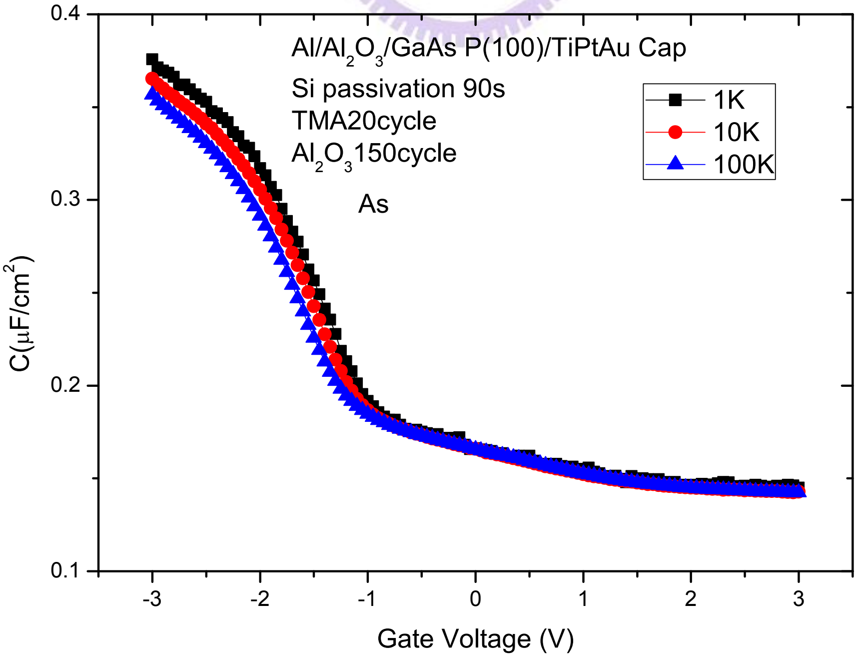
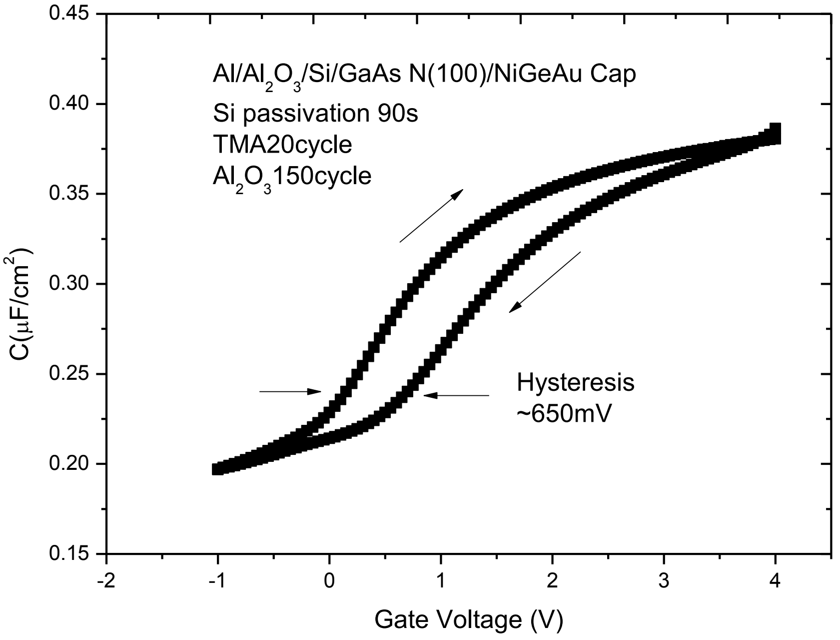


Fig. 3.5 Multi-frequency C-V curve (a) N-type GaAs(100)with SiH_4 passivation (b) P-type GaAs(100) with SiH_4 passivation

(c)N-type



(d)P-type

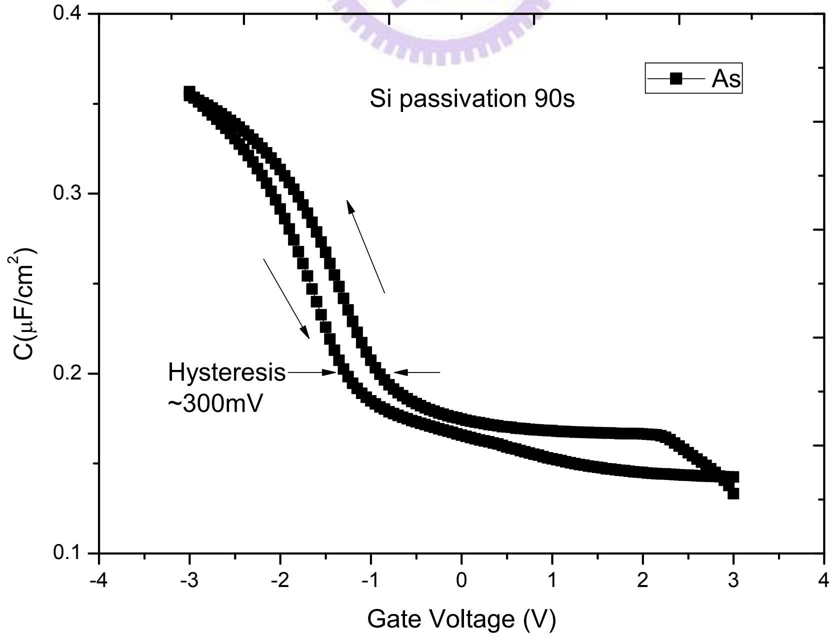
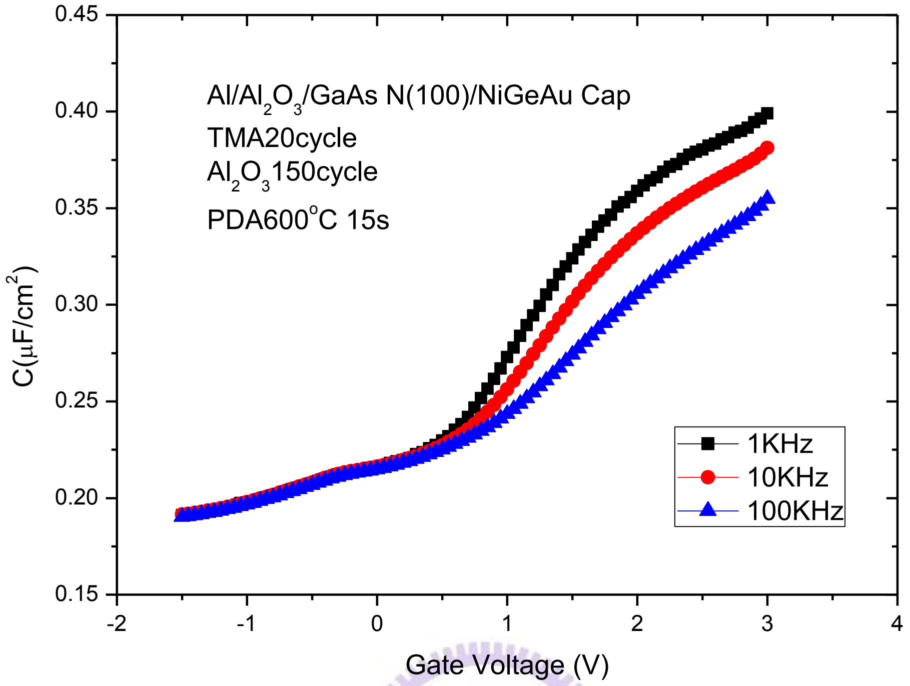


Fig. 3.5 Hysteresis C-V curve (c) N-type GaAs(100) with SiH$_4$ passivation (d) P-type GaAs(100) with SiH$_4$ passivation

(a)N-type



(b)P-type

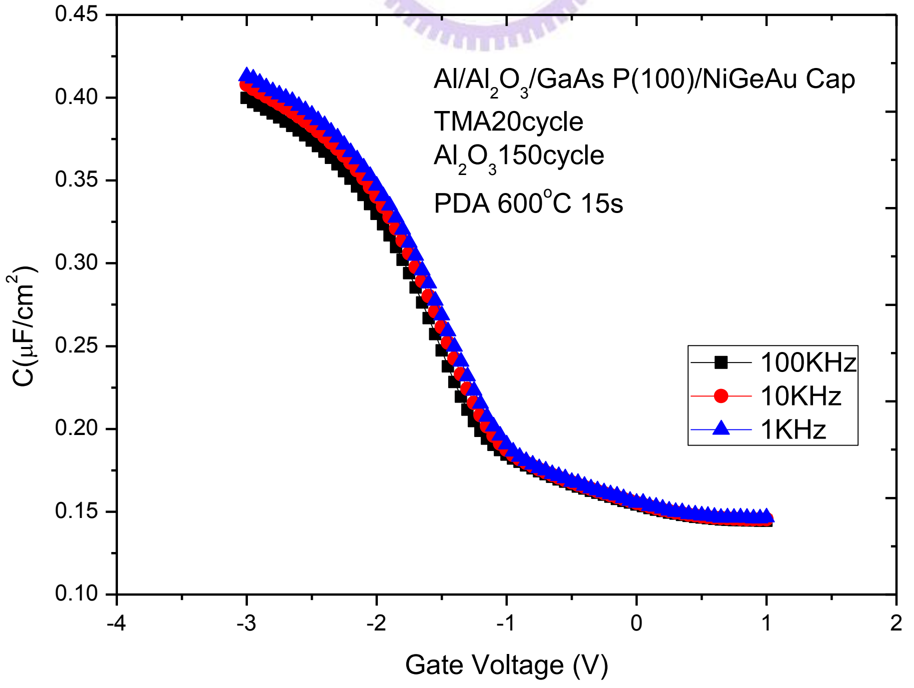
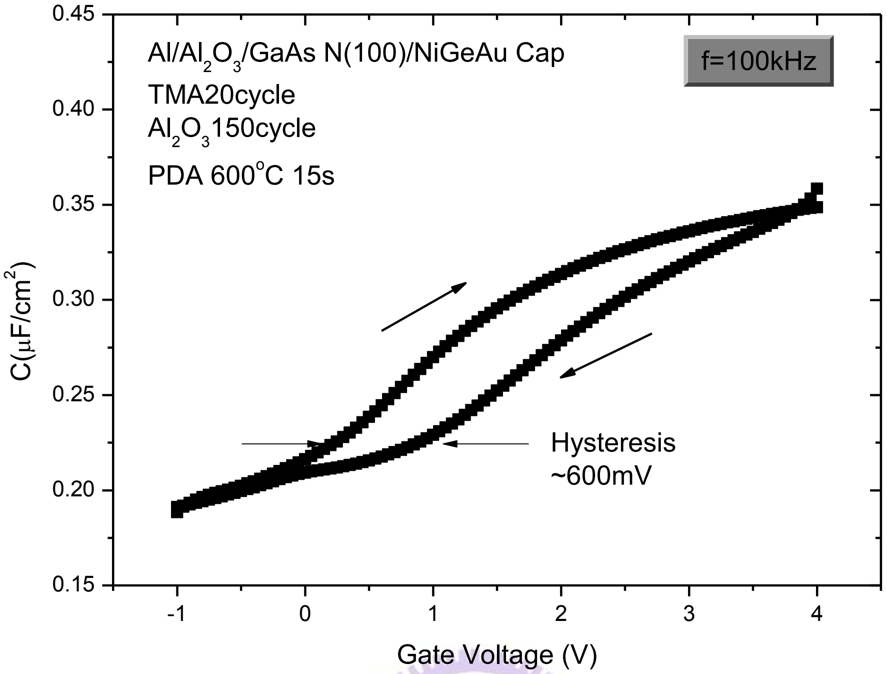


Fig. 3.6 Multi-frequency C-V curve (a) N-type GaAs(100)PDA (b) P-type GaAs(100)PDA

(c)N-type



(d)P-type

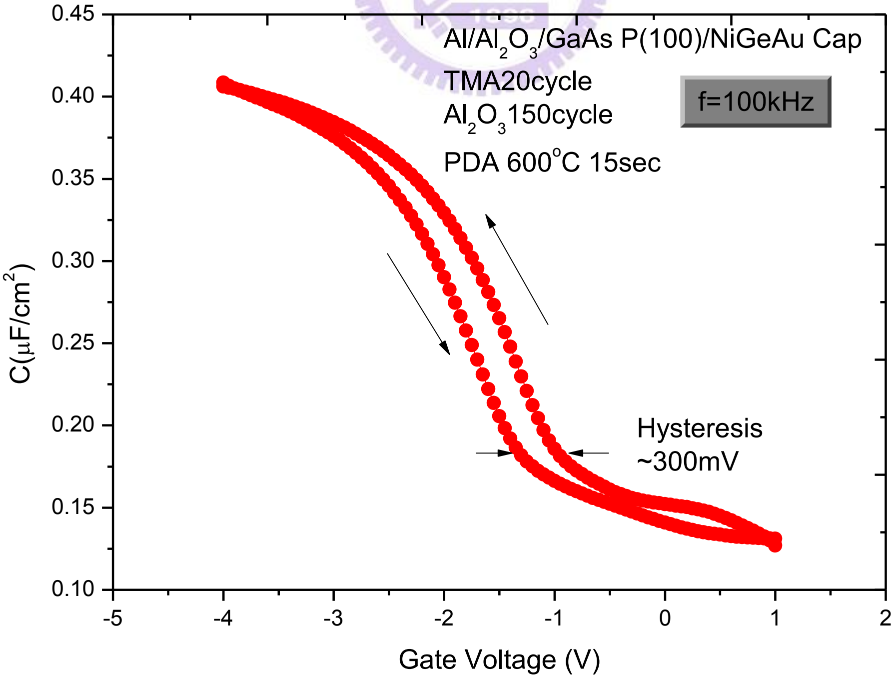
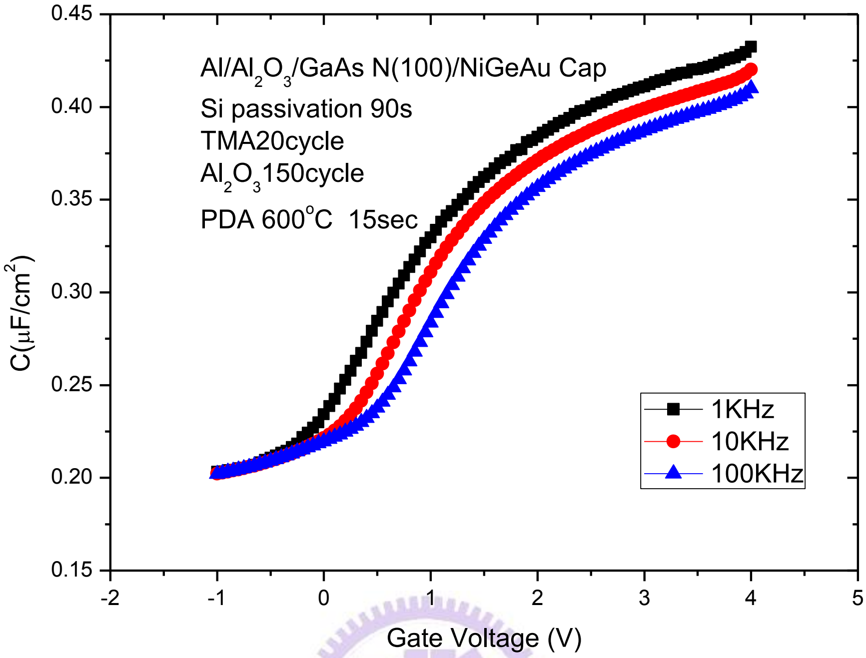


Fig. 3.6 Hysteresis C-V curve (c) N-type GaAs(100)PDA (d) P-type GaAs(100)PDA

(a)N-type



(b)P-type

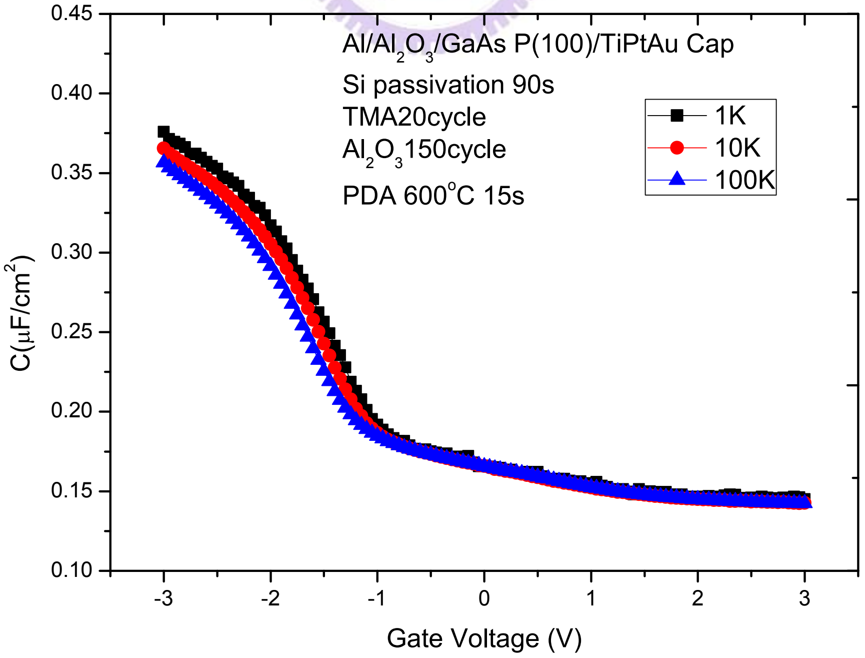
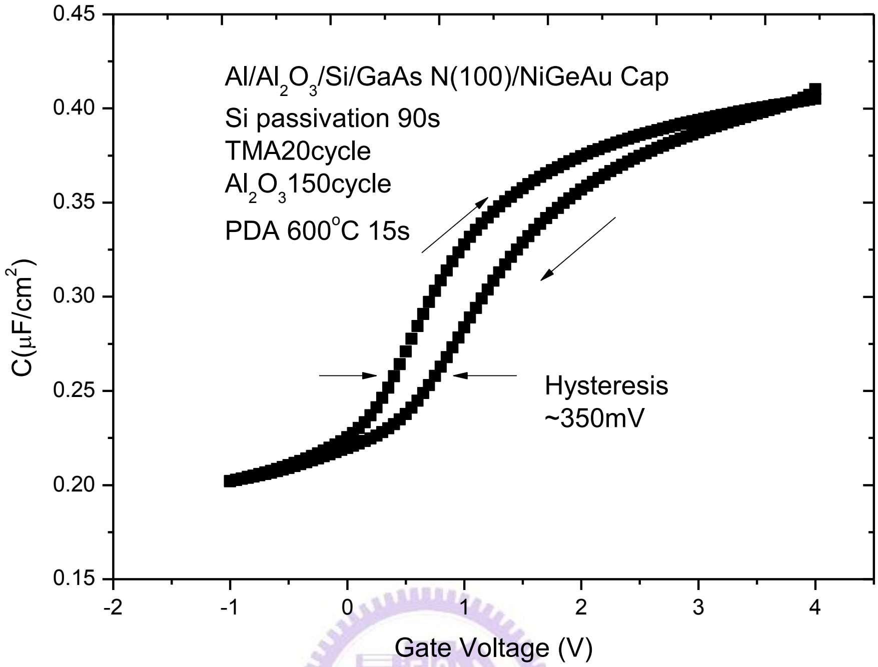


Fig. 3.7 Multi-frequency C-V curve (a) N-type GaAs(100)with SiH_4 passivation and PDA
(b) P-type GaAs(100) with SiH_4 passivation and PDA

(c)N-type



(d)P-type

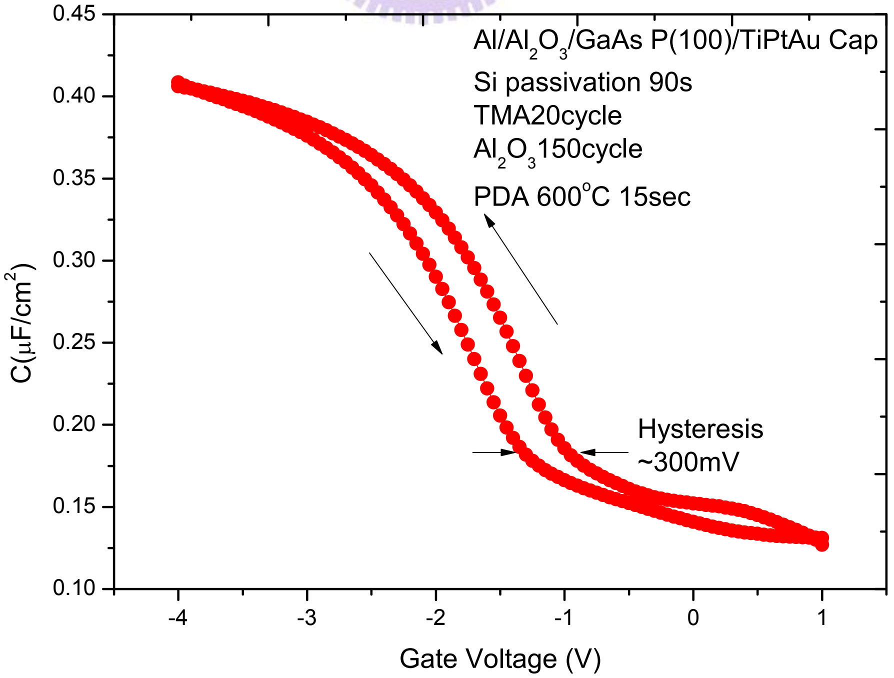
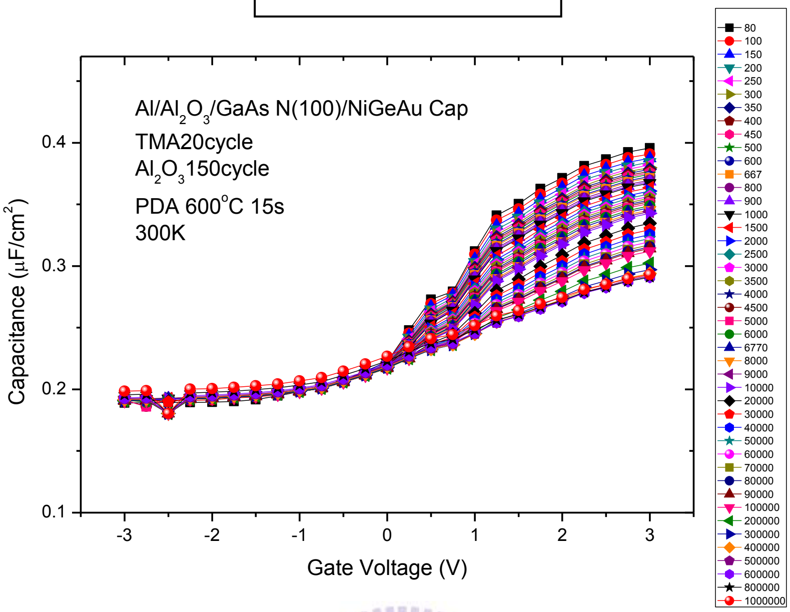


Fig. 3.7 Hysteresis C-V curve (c) N-type GaAs(100) with SiH_4 passivation and PDA
(d) P-type GaAs(100) with SiH_4 passivation and PDA

(a)N-type



(b)P-type

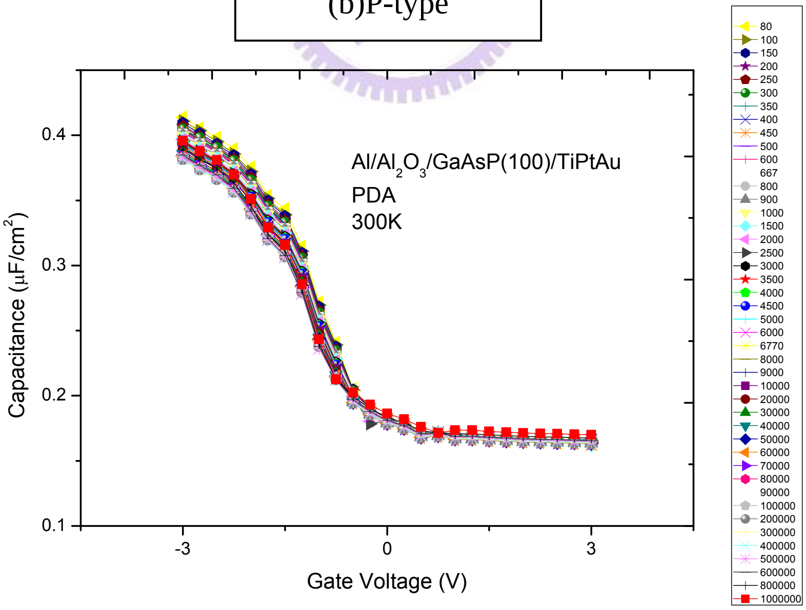
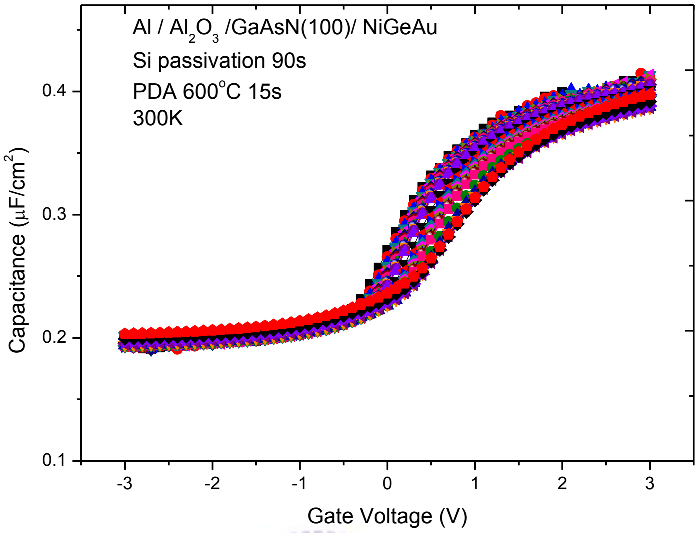


Fig. 3.8 Multi-frequency C-V curve 300K (a) N-type GaAs(100)PDA (b) P-type GaAs(100)PDA

(a)N-type



(b)P-type

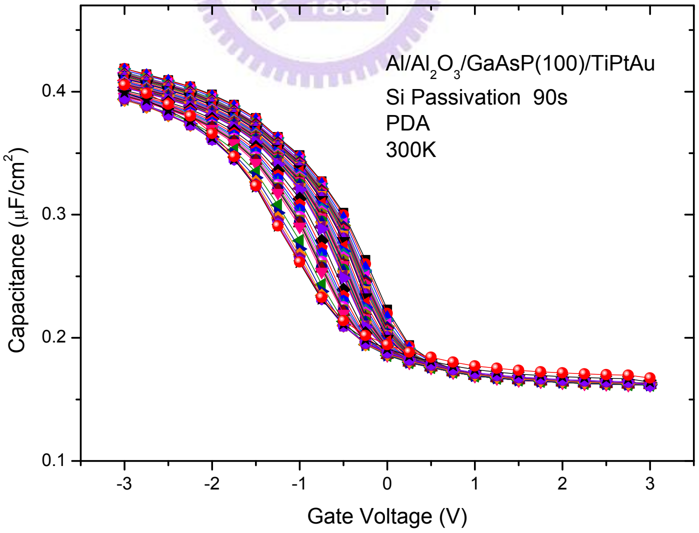
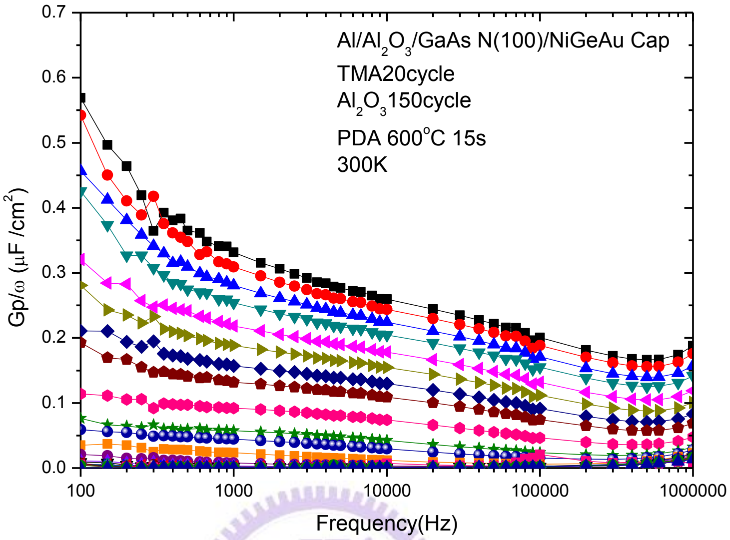


Fig. 3.9 Multi-frequency C-V curve 300K (a) N-type GaAs(100)with SiH_4 and PDA (b) P-type GaAs(100) with SiH_4 and PDA

(a)N-type



(b)P-type

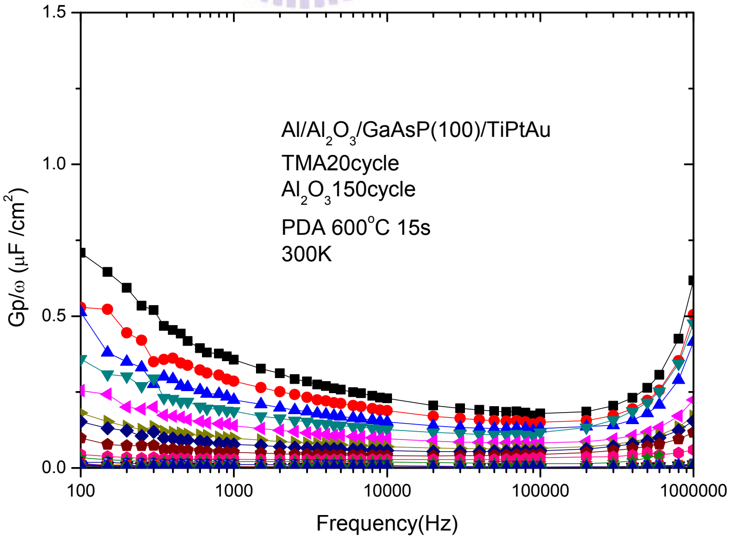
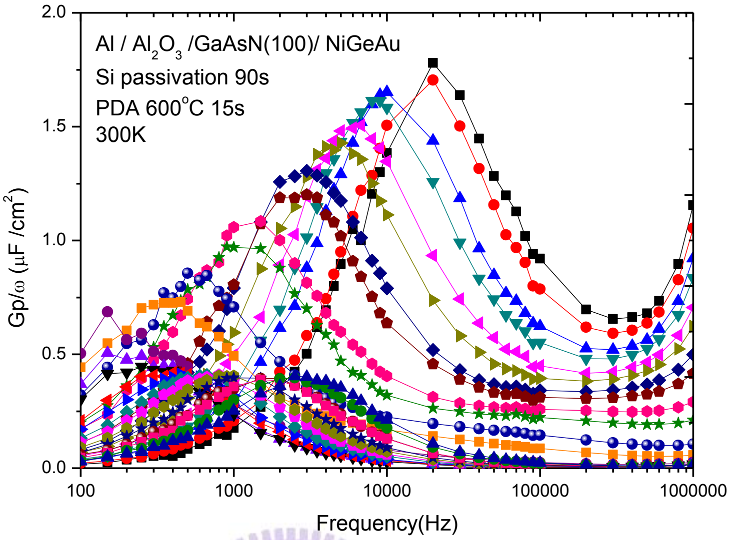


Fig. 3.10 G_p/ω as a function of frequency at 25℃ (a) N-type GaAs(100)PDA (b) P-type GaAs(100)PDA

(a)N-type



(b)P-type

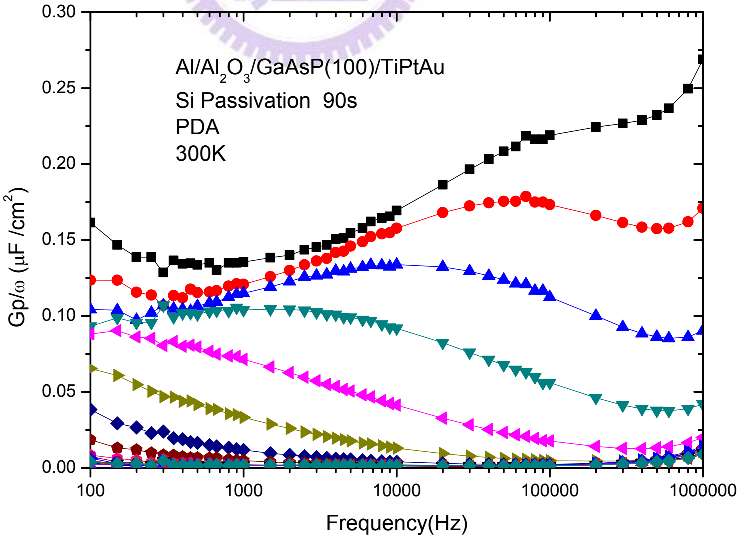


Fig. 3.11 G_p/ω as a function of frequency at 25℃ (a) N-type GaAs(100)PDA (b) P-type GaAs(100)PDA

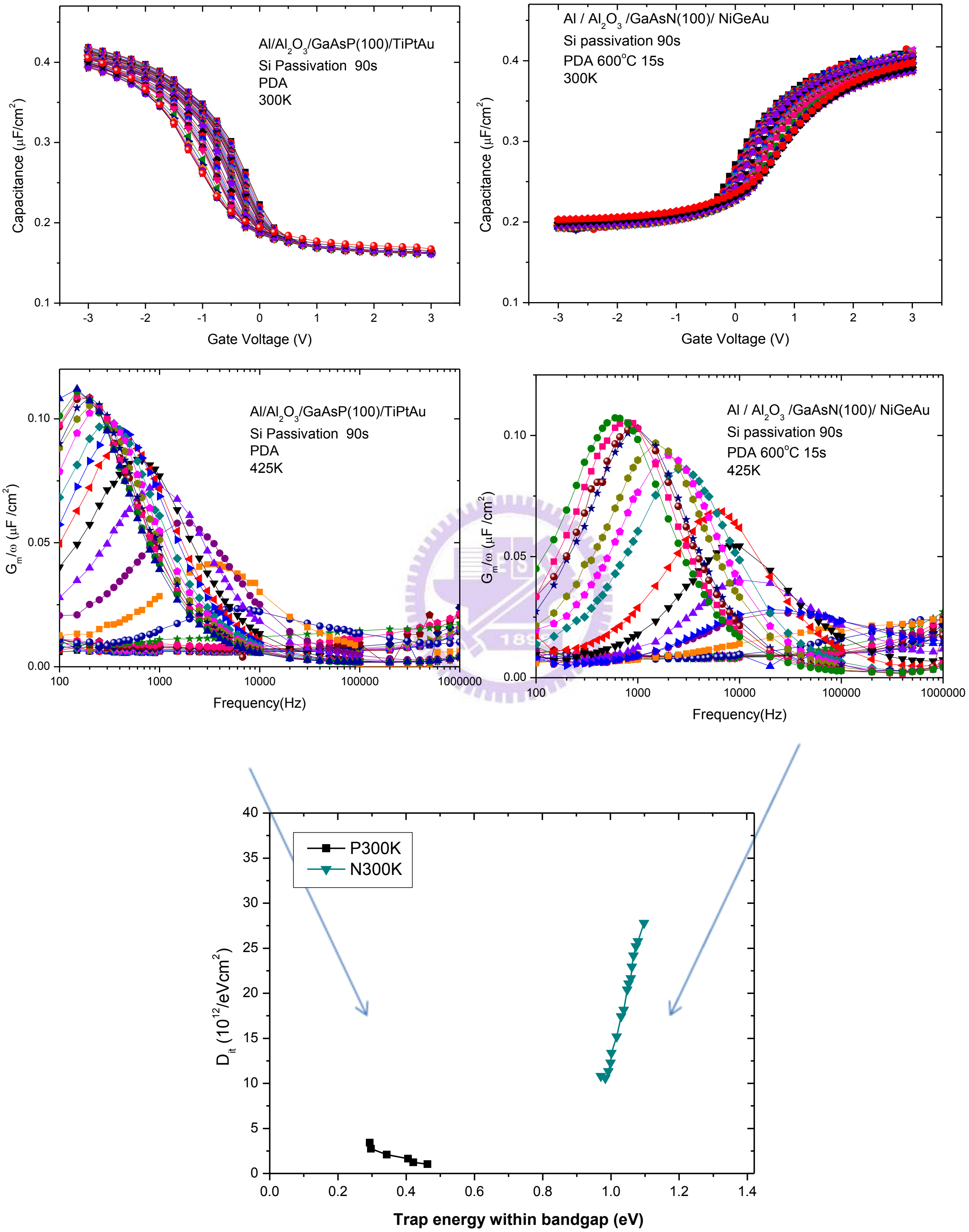
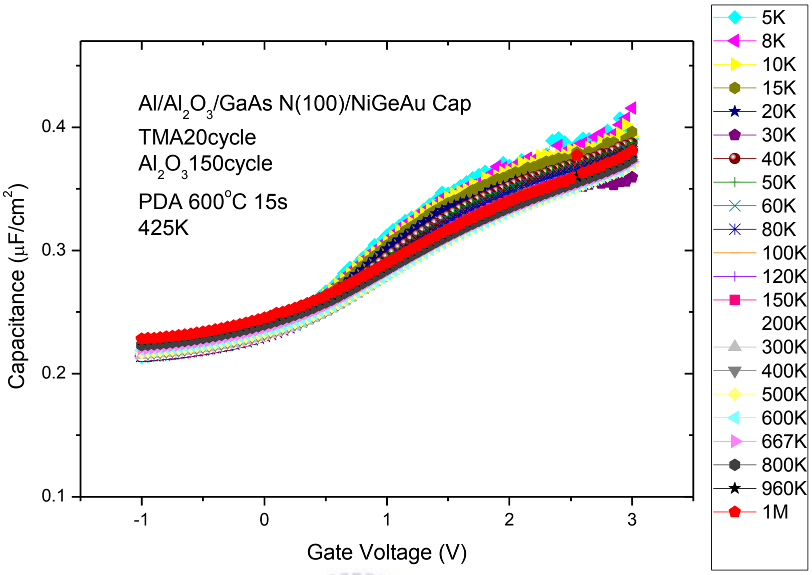


Fig. 3.12 the D_{it} profile of GaAs(100) with SiH_4 passivation at 300K

(a)N-type



(b)P-type

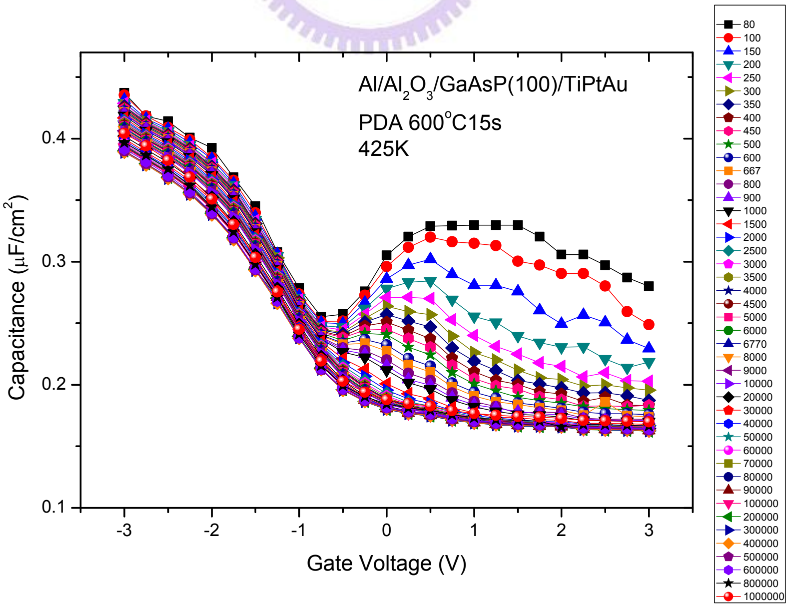
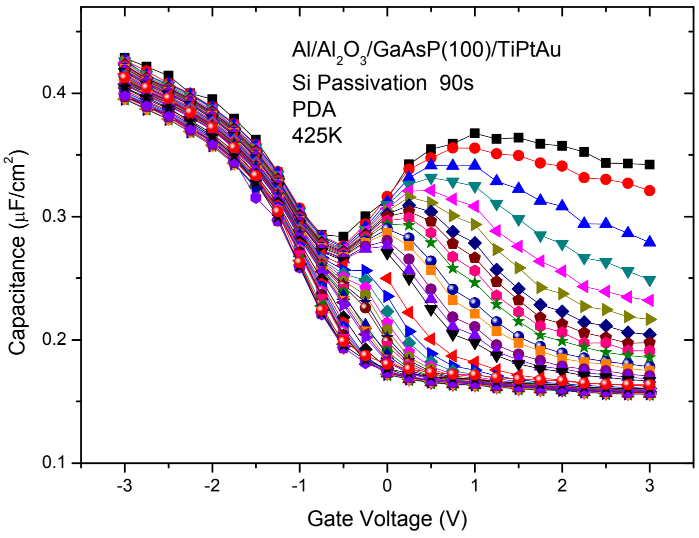


Fig. 3.13 Multi-frequency C-V curve 425K (a) N-type GaAs(100) (b) P-type GaAs(100)

(a)N-type



(b)P-type

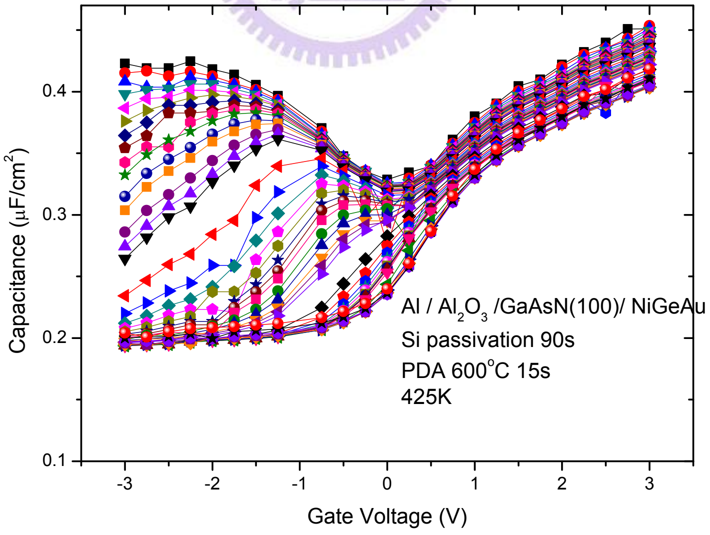
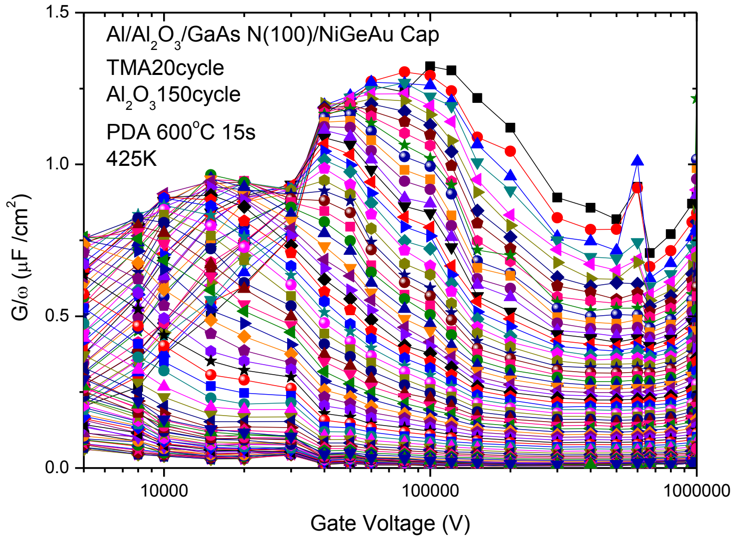


Fig. 3.14 Multi-frequency C-V curve 425K (a) N-type GaAs(100)with SiH_4 passivation (b) P-type GaAs(100) with SiH_4 passivation

(a)N-type



(b)P-type

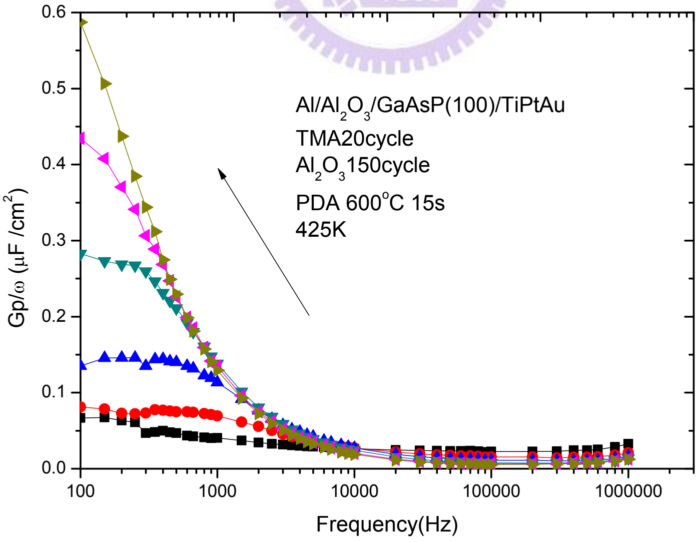
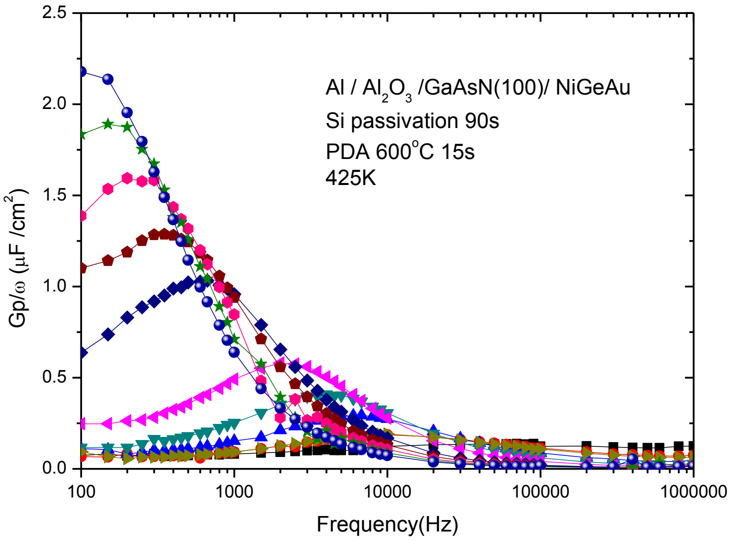


Fig. 3.15 G_p/ω as a function of frequency at 150℃ (a) N-type GaAs(100) (b) P-type GaAs(100)

(a)N-type



(b)P-type

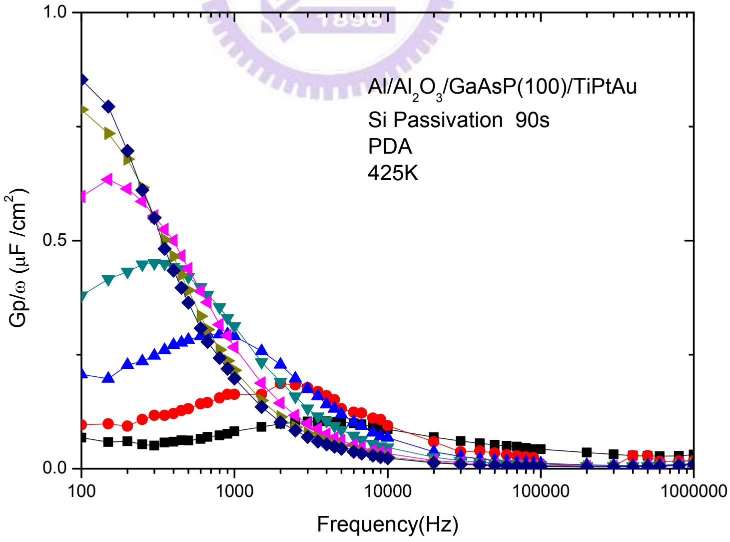


Fig. 3.16 G_p/ω as a function of frequency at 150℃ (a) N-type GaAs(100)with SiH_4 and PDA (b) P-type GaAs(100) with SiH_4 and PDA

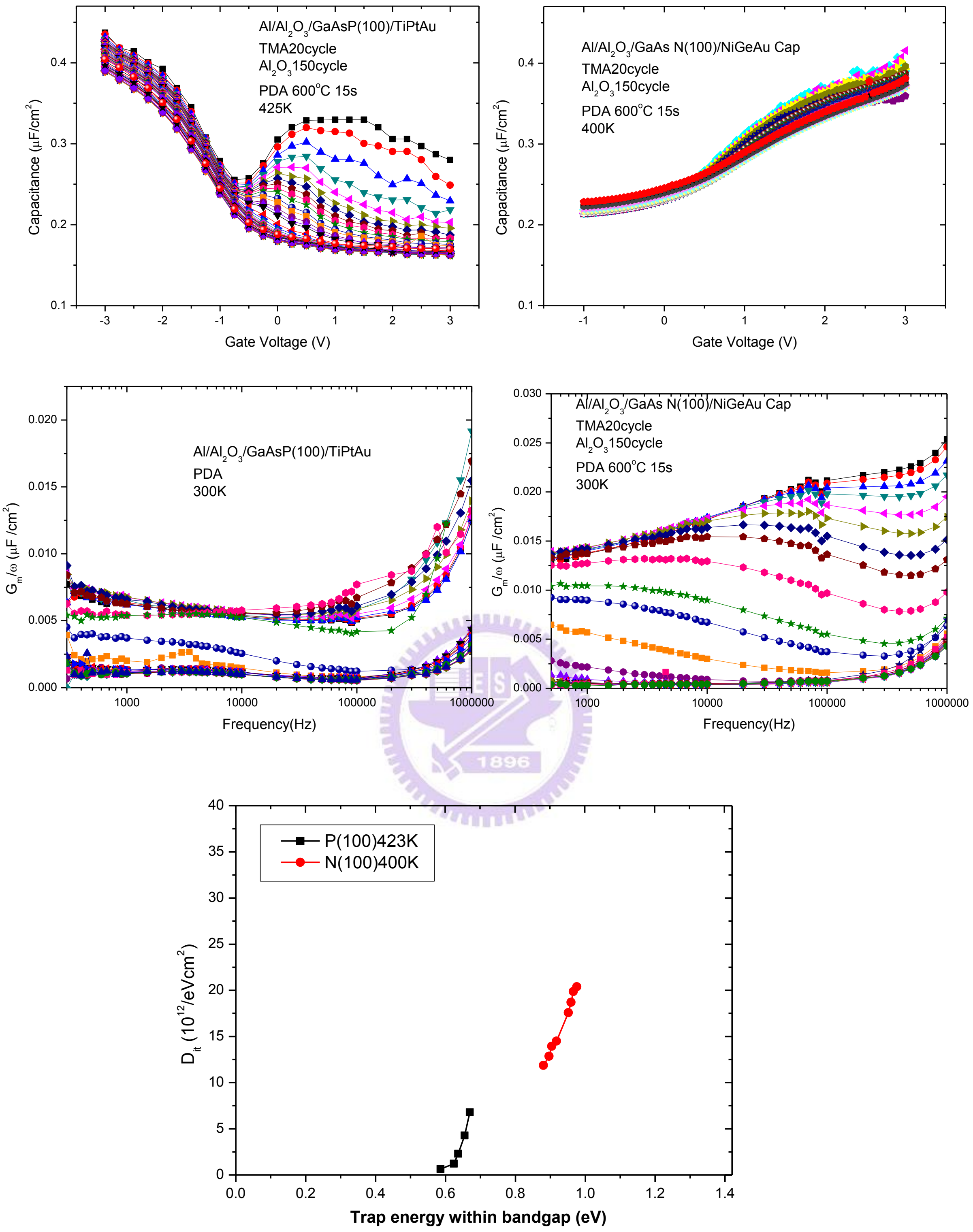


Fig. 3.17 the D_{it} profile of GaAs(100)

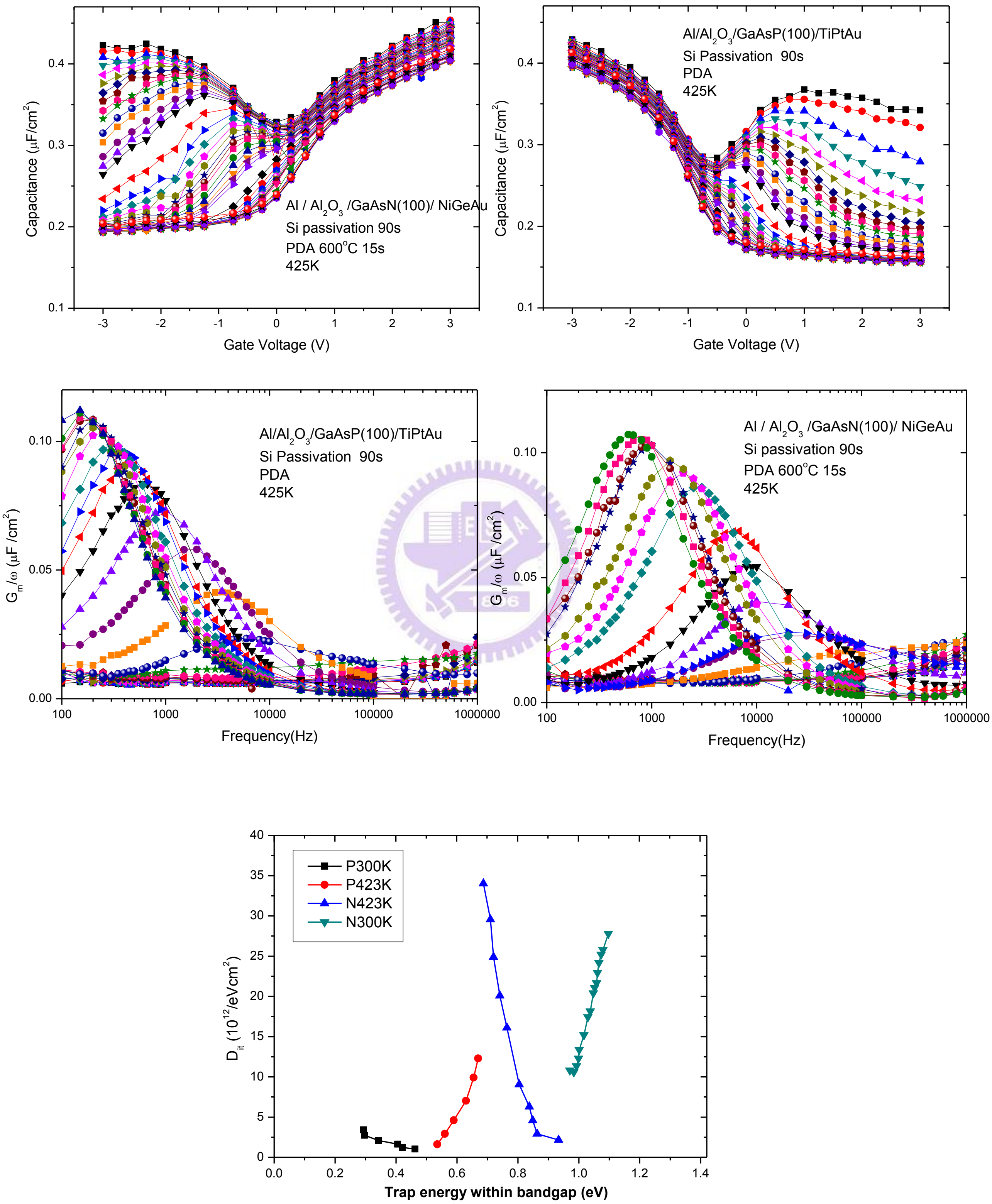
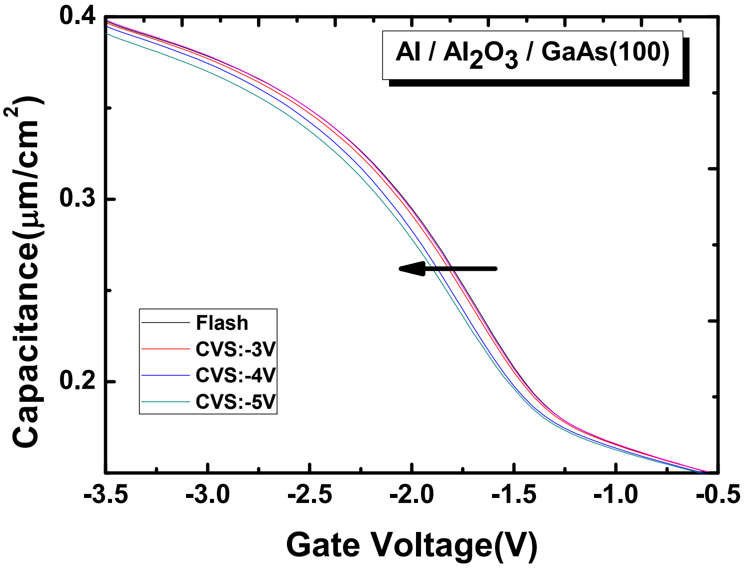


Fig. 3.18 the D_{it} profile of GaAs(100)with SiH_4 and PDA at 425K

(a) P-type GaAs(100)PDA



(b) P-type GaAs(100)with SiH_4 passivation and PDA

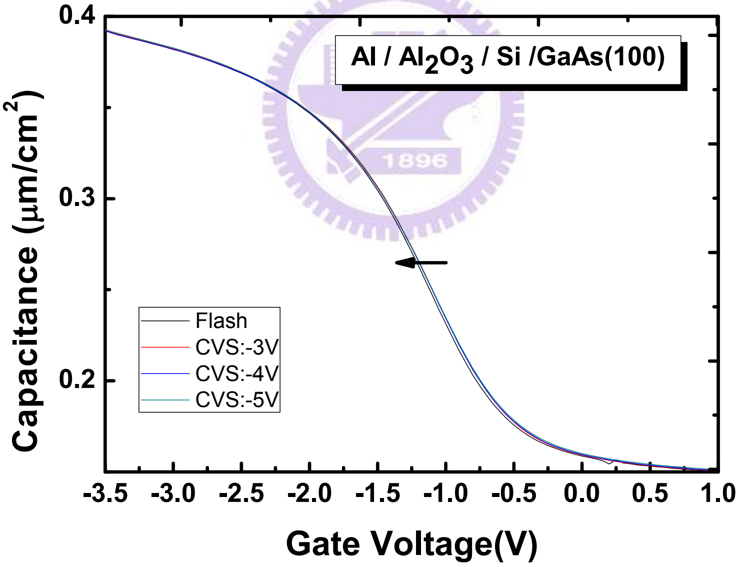


Fig. 3.19 High frequency capacitance–voltage (C–V) characteristics of MOS capacitors employing (a) Al_2O_3/P-GaAs and (b) Al_2O_3/Si/P-GaAs structures.

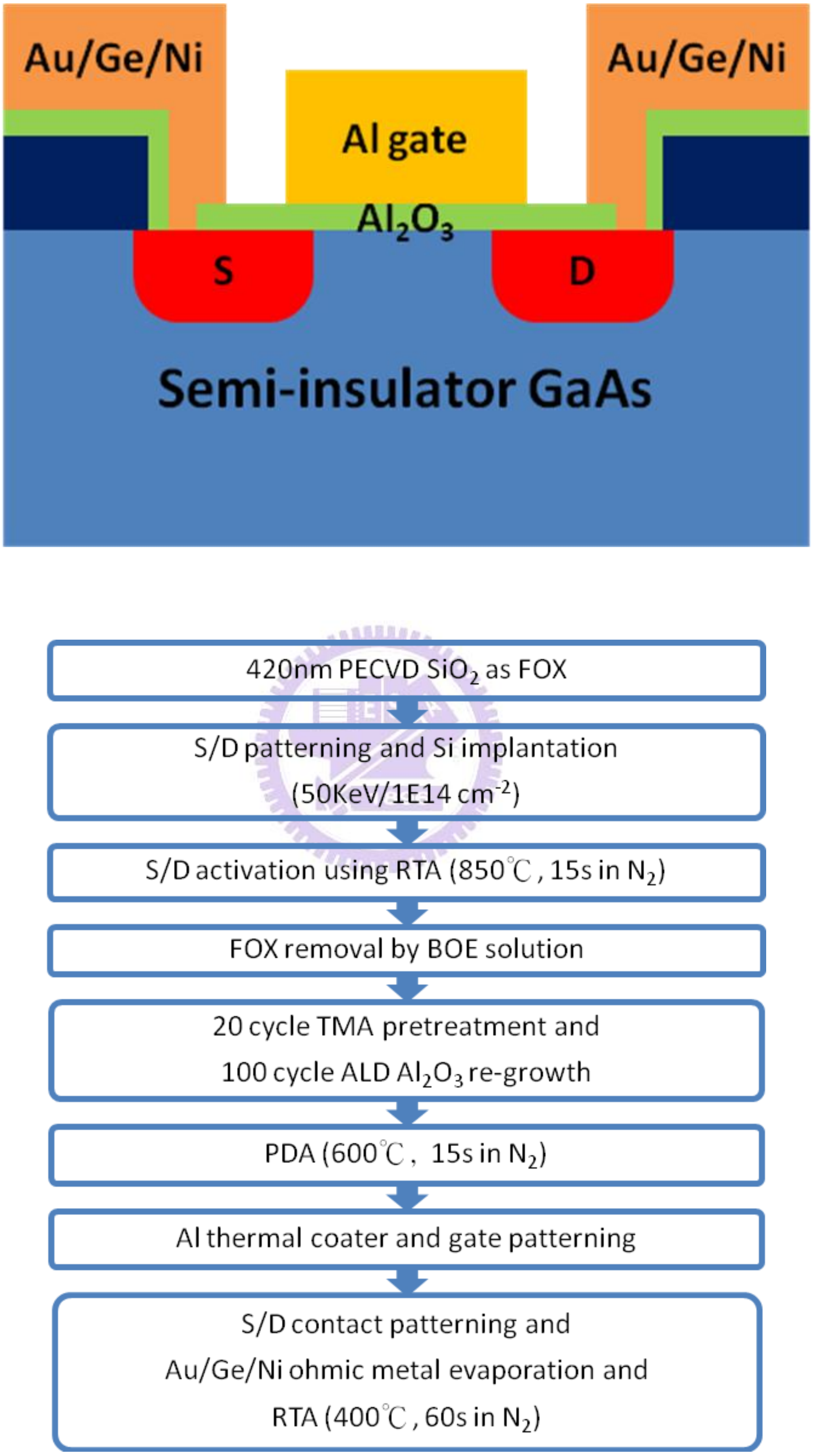


Fig. 3.20 The scheme and process flow of GaAs MOSFET.

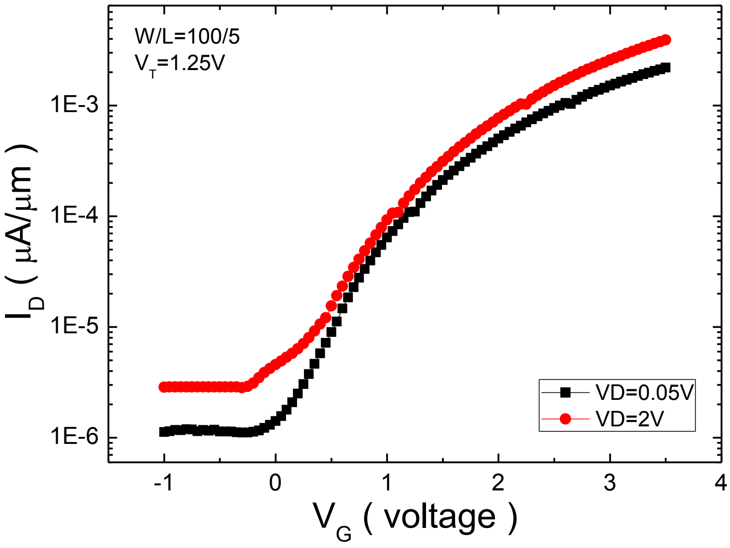


Fig. 3.21 Id-Vg of enhancement mode GaAs n-MOSFET

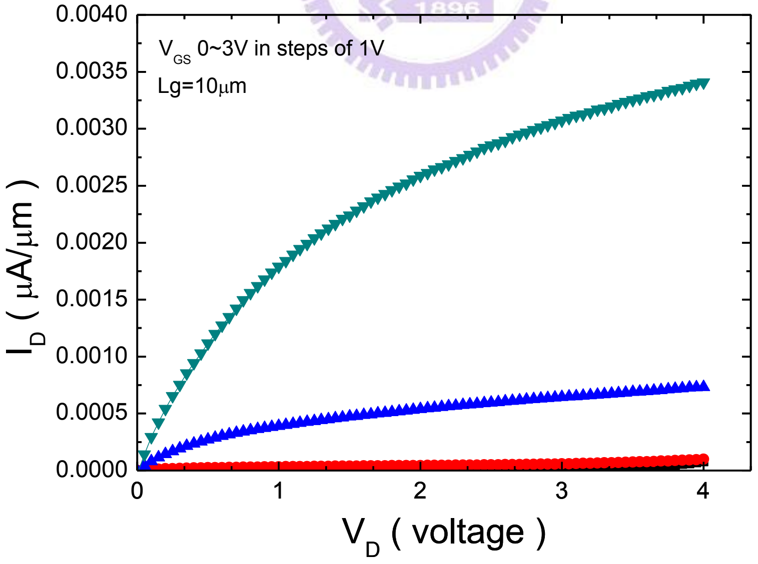


Fig. 3.22 Id-Vd characteristics of enhancement mode GaAs n-MOSFET

Chapter 4

GaAs NMOSFET with Embedded-Ge Source/Drain

4.1 Introduction

III-V materials have significantly smaller effective mass and higher electron mobility compared to Si and Ge. Although their small transport mass leads to high injection velocity (v_{inj}), III-V materials have low density of states (DOS), tending to reduce the inversion charge (Q_{inv}) and hence reduce drive current. It result high source/drain resistance and source starvation. The source starvation is that the inability of the source region to sustain a large flow of carriers in 'longitudinal' velocity states in the channel, unless the momentum relaxation rate and/or the doping density in the source are sufficiently large.

Therefore, we propose that Ge selective epitaxial growth be used as source/drain of III-V MOSFETs. Ge have more high solid solubility than III-V materials. In addition, III-V materials such as GaAs are lattice matched to Ge. The NMOSFETs possess higher solid solubility and higher channel mobility. However, In the case of Ge we have found that the Fermi level at metal-Ge Schottky barriers is pinned near the valence band of Ge for a variety of metals. It will bring large parasitic resistance in the S/D regions that can be significantly worse in III-V NMOSFET [1-5]

Recently, researchers used a ultrathin dielectrics inserted between metal and substrate such as Ge_3N_4, Al_2O_3, GeO_2 and Si_3O_4 [6-9]. In this chapter, we use TiO_2 [10] as the insulating layer for n^+ source/drain regions for application in n-channel GaAs MOSFETs.

4.2 Experimental process

In Ge-S/D MOSFET fabrication, the first step is the S/D region etching by the solution with H_3PO_4:H_2O_2:H_2O = 1:1:160 (the etching rate ~0.5 nm/s). After surface cleaning, the growth of Ge was carried out by using a UHV/CVD system with a base pressure of less than 5×10^{-8} Torr. After GaAs wafers were loaded into the growth chamber, they were first in situ prebaked at 550℃ for 10 min. Then, the Ge layer was grown at the same temperature with a constant GeH_4 flow rate. Throughout the entire growth process, the gas pressure in the growth chamber was kept at 30 mTorr.

Next, the S/D regions were implanted with phosphorus at doses of 5×10^{14} cm^{-2} and 1×10^{15} cm^{-2} at 50keV and 30keV, respectively. Subsequently, a Al_2O_3 layer was deposited by atomic layer deposited (ALD), and then, the sample was annealed in a N_2 ambient at 600 ℃ for 30 s by rapid thermal annealing (RTA).

After etching the S/D contact holes, Thermal coatered Al about 4000 Å were patterned as gate electrodes and Source/Drain pattern through the lithography. The fully process flow of Ge-S/D MESFET was shown in **Fig. 4.1**.

4.3 TiO_2 interfacial layer on GaAs for low resistivity Contacts

Comparing with controlled sample which is analyzed above, the sample with Ge S/D has the poorer sheet resistance. The reason is probably that we did not exactly control the dose of implantation and time of S/D activation; it leaded to the more impurity in the S/D region. The issue of large specific contact resistivity for Al/n^+-Ge contact has been a challenge in E_F pinning on metal/ n^+-Ge interface.

In this work, we use TiO_2 interfacial layer on GaAs for MIS structure to reduce electron schottky barrier height (Φ_{BN}) that due to the Fermi level unpinning phenomenon. In addition, the conduction band offset is between 0.26 and 0.06eV at the TiO_2/Ge interface, this low conductance band offset value may be able to achieve high current as long as Φ_{BN} can be reduced. In order to observe this phenomenon, we fabricated the circular transmission line method (CTLM) for analyzing contact and sheet resistivity. According to mentioned above chapter, we firstly measured the relationship of R_T and d, and find line to fit it. The ρ_s and L_T can be extracted. Finally, the value of ρ_c utilizes L_T to obtain.

The samples, firstly, were implanted the phosphorus doses 1×10^{15} cm^{-2} at 50 keV After deposit Al_2O_3 capping layer, activation was using RTA at 600℃ for 30 s in N_2 ambient. Next, we deposited TiO_2 by ALD. Then, we used Acetone to remove metal-organic residues and the metal of Al was deposited by using thermal coater and lift-off process.

In the result, we cannot observe the forward current increases up to increase TiO_2 thickness. **Fig. 4.2** show the I-V characteristics of the Al/TiO_2/Ge structures. Although with TiO_2 could not efficiently reduce electron schottky barrier height (Φ_{BN}), the forward current could not significantly degrade by increasing TiO_2 thickness.

In addition, we analyzed contact and sheet resistivity. The value of ρ_s and ρ_c were not also significant change. The experiment is not be expected. But the TiO_2 applied on MOSFETs, the forward current obviously increased compared without TiO_2 interfacial layer.

4.4 Ge-Source/Drain GaAs MOSFETs

Fig. 4.3 illustrates the I_D-V_G transfer characteristic of 5 μm gate length for GaAs MOSFET with Ge-S/D, and the ratio I_{on} (V_D = 2 V)/I_{off} (V_D = 2 V) is about 2.59×10^1, It is because Ge have found that the Fermi level at metal-Ge Schottky barriers is pinned near the valence band of Ge for a variety of metals. So Ge Source/Drain has the poorer sheet resistance. Therefore, we must research methods to reduce conduction band offset. The technique by inserting ultrathin dielectrics result in low Φ_{BN}. **Fig. 4.4** illustrates the I_D-V_G transfer characteristic of 10 μm gate length for GaAs MOSFET with Ge-S/D by inserting TiO_2 interfacial layer, and the ratio I_{on} (V_D = 1 V)/I_{off} (V_D = 1 V) ratio is about 2.5×10^2.

According to Fig. 4.3 and Fig. 4.4, the contact resistivity was significantly reduced by inserting TiO_2 interfacial layer, so on-state current is more large than without TiO_2 interfacial layer.

4.5 Summary

GaAs have low density of states (DOS), tending to reduce the inversion charge (Q_{inv}) and hence reduce drive current. In addition, Ge have more high solid solubility and lattice match to GaAs. Thus, we propose that Ge selective epitaxial growth be used as source/drain of III-V MOSFETs.

The Fermi level at metal-Ge Schottky barriers is pinned near the valence band of Ge for a variety of metals. We use TiO_2 interfacial layer on GaAs for MIS source/drain structure to reduce electron schottky barrier height (Φ_{BN}). Finally, the GaAs MOSFET with embedded Ge source/drain successfully was improvement.

Reference

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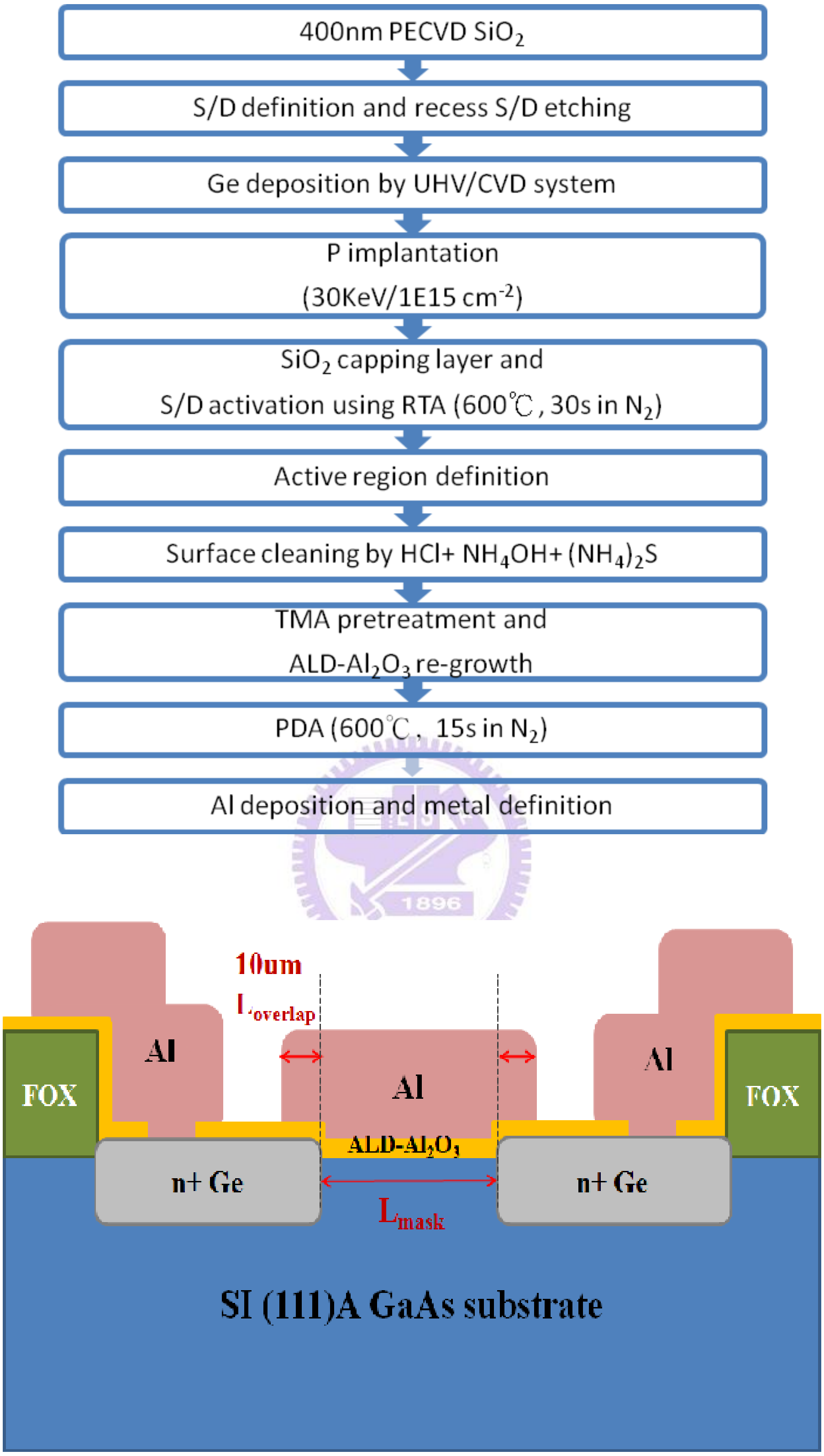

Fig. 4.1 The scheme and process flow of GaAs MOSFET.

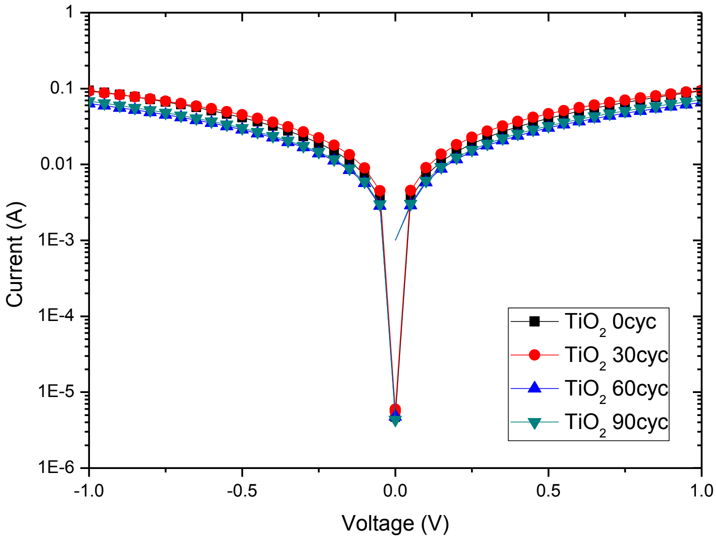

Fig. 4.2 the I-V characteristics of the Al/TiO$_2$/Ge structures

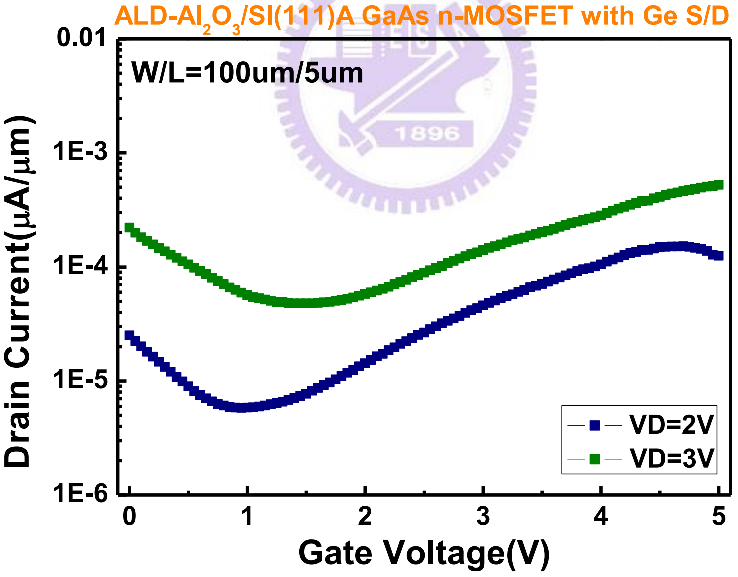

Fig. 4.3 Transfer characteristic for E-mode GaAs n-MOSFET with Ge-S/D.

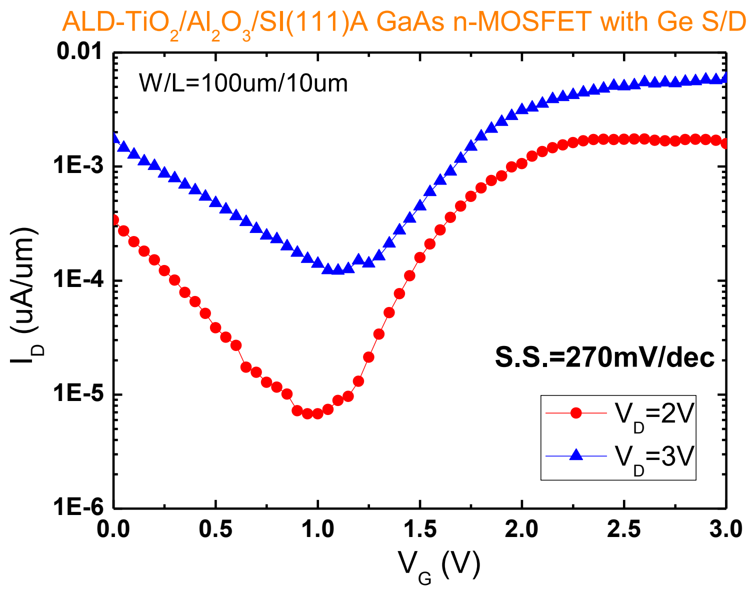

Fig. 4.4 Transfer characteristic for E-mode GaAs n-MOSFET with Ge-S/D by inserting TiO_2 interfacial layer

Chapter 5

Conclusions and Future work

5.1 Conclusions

In this thesis, firstly, we have studied the electrical characteristic of GaAs capacitors with Al_2O_3 dielectric. Unlike SiO_2 on Si, III-V materials such as GaAs don't have such a native oxide that have high quality, thermodynamically stable properties that can be stable on the device criteria as SiO_2 on Si. Poor dielectric quality results in frequency dispersion, hysteresis, flab band shift, and unfavorable low dielectric constant. According to the result of C-V and conductance measurement, we believed that the surface treatment of silane passivation and PDA can efficiently diminish the formation of GaAs(100) native oxide, thus improve the effect of Fermi-level pinning appearance. Next, we analyzed reliability for silane passivation. A clear understanding of reliability of this different interfaces, via charge trapping/detrapping studies under different stressing condition, we observed the SiH_4 passivation can improve the reliability of GaAs(100). But GaAs(111)A had the best surface band bending and lower value of D_{it} in the middle of bandgap, we assumed that the improvement resulted from the different structure of surface on orientation. The Fermi level pinning is not an intrinsic property of GaAs.

After we improved interface of III-V, we explored S/D resistance and junction. According to electrical characteristics, we discovered that the sheet resistivity at 30keV&80keV is lower than 50keV implant energy. However, the contact resistivity is just contrary. In addition, from the point of temperature, we found that the sheet resistivity at 850℃ is lower than 950℃, and the contact resistivity is just contrary. But, the junction of forward current didn't suppress significantly at alloy metal 400^{o}C 30s. We optimize conditions of sheet resistivity, contact resistivity, and Ohmic RTA time.

Finally, we used these conditions to fabricate metal-oxide-semiconductor field effect transistors with the different surface orientation successfully and measured electrical characteristics. In addition, we also fabricated GaAs MOSFET with embedded Ge source/drain and studied electrical characteristics. But the resistances were lager for all MOSFET that we fabricated.

5.2 Future work

Although III-V compound semiconductors have high electron mobility and high velocity satuation. But one of the most critical challenge is the lower values of solid solubility and the density of states (DOS). For example, the maximum solid solubility and the DOS are 1×10^{19} and 4.7×10^{17} cm^{-3}, respectively, on GaAs substrate, which are lower, compared to Si [18]. Therefore, these material properties contribute the more source/drain (S/D) resistance and hence suppress the maximum operate current. Therefore, we proposed a new structure of the III-V channel MOSFET to solve these problems and hence enhance the current drive. In present, in order to overcome the solid solubility limit, the metal S/D structure is one of the most promising ways to reduce the resistance of S/D.

In addition, the Ge-S/D structure of GaAs MOSFET can solve the most critical challenge. And III-Vs cannot make good p-channels, which are also needed for CMOS, because their hole mobilities are relatively low. Using the epitaxial technology to form the Ultimate CMOS structure composed of the combination of III-V semiconductors n-MOSFETs and Ge p-MOSFETs on insulators.

Except for improving the performance of the GaAs nMOSFET, the reliability characteristics of MOSFET with ALD-Al_2O_3 films is also worth investigating. Accelerated life-test of MOS devices is conventionally performed by applying a constant gate voltage (CVS) or injecting a constant gate current (CCS) over a period of time to monitor the oxide degradation. In addition, time to dielectric breakdown (TDDB) under constant-voltage stressing is considered a very important parameter in determining the gate oxide reliability and integrity.

Non-planar, multi-gate architectures have been investigated for improved electrostatics in Si MOSFETs. In recently, III-V MOSFETs start to be reported. The structure can efficiently increase gate control ability and move the Fermi-level effectively.

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